Tutorial Overview Of Analog PLLs

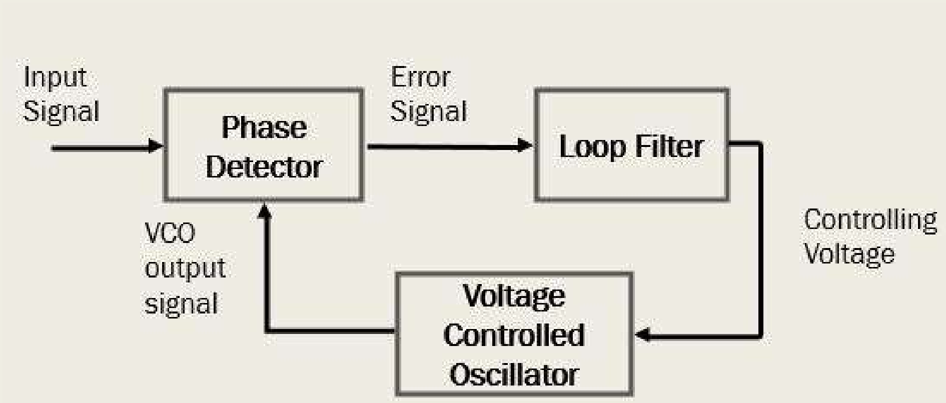
ECG 721

Shada Sharif

Outline

- Introduction about PLLs, Types, and Applications
- PLL Components
- PD
- LF
- VCO
- Equations and Simulations

What is a PLL?



Basic block diagram of PLL

- A phase-locked loop (PLL) is a negative feedback system that synchronizes the voltage controlled oscillator (VCO) output signal to the phase of a reference input signal.

Ref [1], [2]

Types of PLLs

PLL Types	Phase Detector	Loop Filter	Controlled Oscillator
Analog/Linear PLL (APLL)	Analog multiplier	Passive/active RC	Voltage controlled
Digital PLL (DPLL)	Digital detector	Passive/active RC	Voltage controlled
All digital PLL (ADPLL)	Digital detector	Digital filter	Digitally controlled
Software PLL (SPLL)	Software multiplier	Software filter	Software oscillator

Ref [2]

Benefits of Analog PLL and Applications

- Benefits
  - *Low jitter*
  - *Tunability*
- Applications
  - *RF systems*
  - *Modulation/Demodulation*
  - *Frequency synthesis*
  - *And much more …*

Ref [10], [11]

Describing a PLL

- PLLs are described by type and order
- Type
  - *Number of poles of the open-loop transfer function located at origin*
  - *Number of integrators in the loop*
- Order
  - *Number of poles in closed-loop transfer function*
  - *Highest degree polynomial in the characteristic equation*

Type 1 → $G(s)H(s) = \frac{10}{s(s+10)}$

Order 2 → $s^2 + 10s + 10$

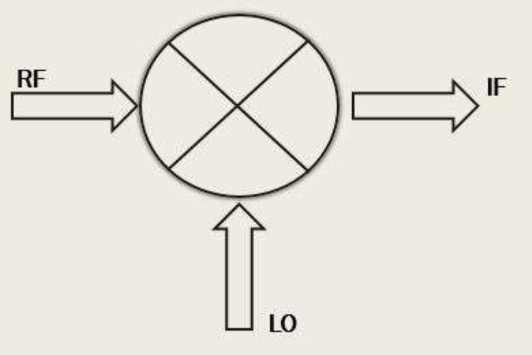
Ref [3], [4], [11]

PLL Components

- PD
  - *Used to generate the phase difference between input signals*
- LPF
  - *Cancels high frequencies and keeps DC component of error signal*
- VCO
  - *Provides local frequency for the circuit*
  - *Controlled by the error signal from the PD*

Ref [15]

Analog Multiplier/Mixer



Ideal Mixer Process

- Mixes RF and LO signal to produce their frequency sum and difference
- Produces an error signal proportional to phase deviation
  - *Phase difference between input and output signal of PLL*
- Signals in phase, output error is constant
- Signals not in phase, output error is varying
  - *Negative feedback reduces error build up till phases match*

Ref [5]

Basic Multiplier Mathematics

$$\sin(x) * \sin(y) = \frac{1}{2}xy(\cos(x-y) - \cos(x+y))$$

$$\omega = 2\pi f$$

$$V_{RF} = A sin(\omega_1 t + \theta_1)$$

$$V_{LO} = B sin(\omega_2 t + \theta_2)$$

If $\omega_1 = \omega_2$

$$V_{RF} * V_{LO} = \frac{AB}{2}[\cos(2\omega t + \theta_1 + \theta_2) - \cos(\theta_1 - \theta_2)]$$

Canceled in loop filter

DC component/phase error

Ref [7]

Mixer Performance Parameters

- Conversion gain/loss
  - *ratio between IF and RF signals (voltage or power)*
  - *Impacts noise*
- Noise figure
  - *Measure of SNR degradation*
  - *Impacts receiver sensitivity*
- Port isolation
  - *Minimize feedthrough between ports*
- Linearity
- Power
  - *Low power dissipation desired*

Ref [6]

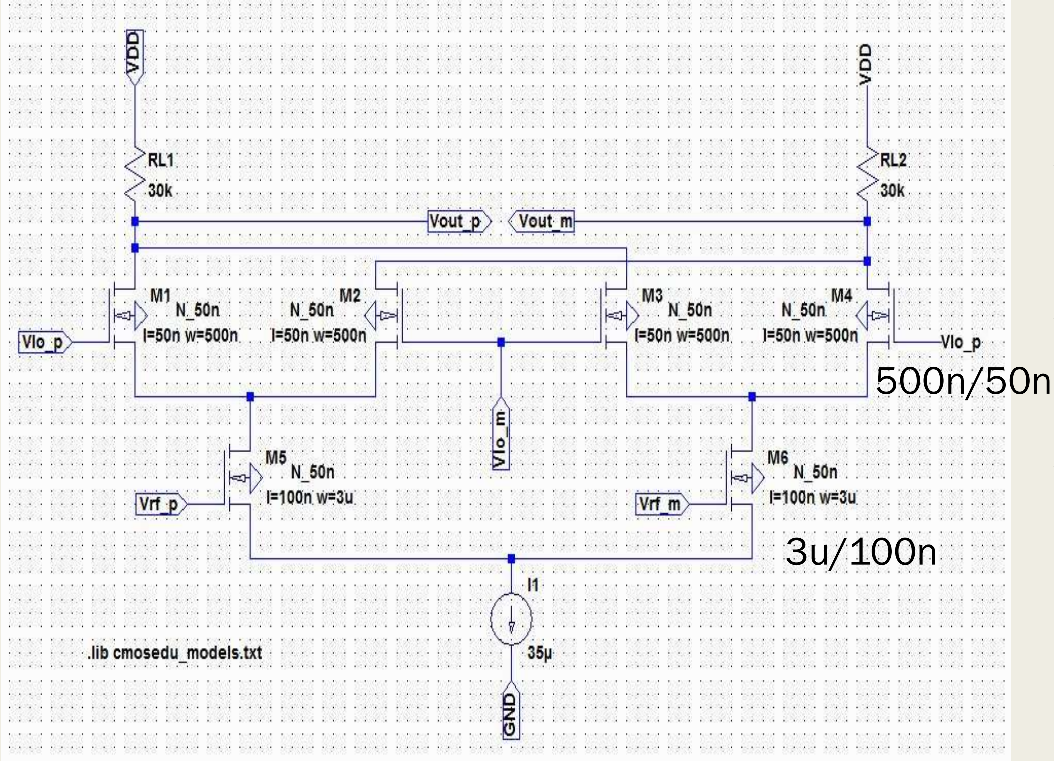
Multiplier types

- Discrete
  - *Single diode*
    - Bad isolation
    - No conversion gain
  - *Diode-ring Mixer*
    - Poor gain
    - Good isolation
    - Good linearity

- IC
  - *Mosfet passive mixer*
    - Acts as a switch
    - Low power consumption
  - *Active mixer*
    - Single balanced
      - *Intermediate isolation*
    - Double balanced
      - *Good isolation*
      - *Good linearity*

Ref [6]

Double Balanced Multiplier



Load resistors for gain

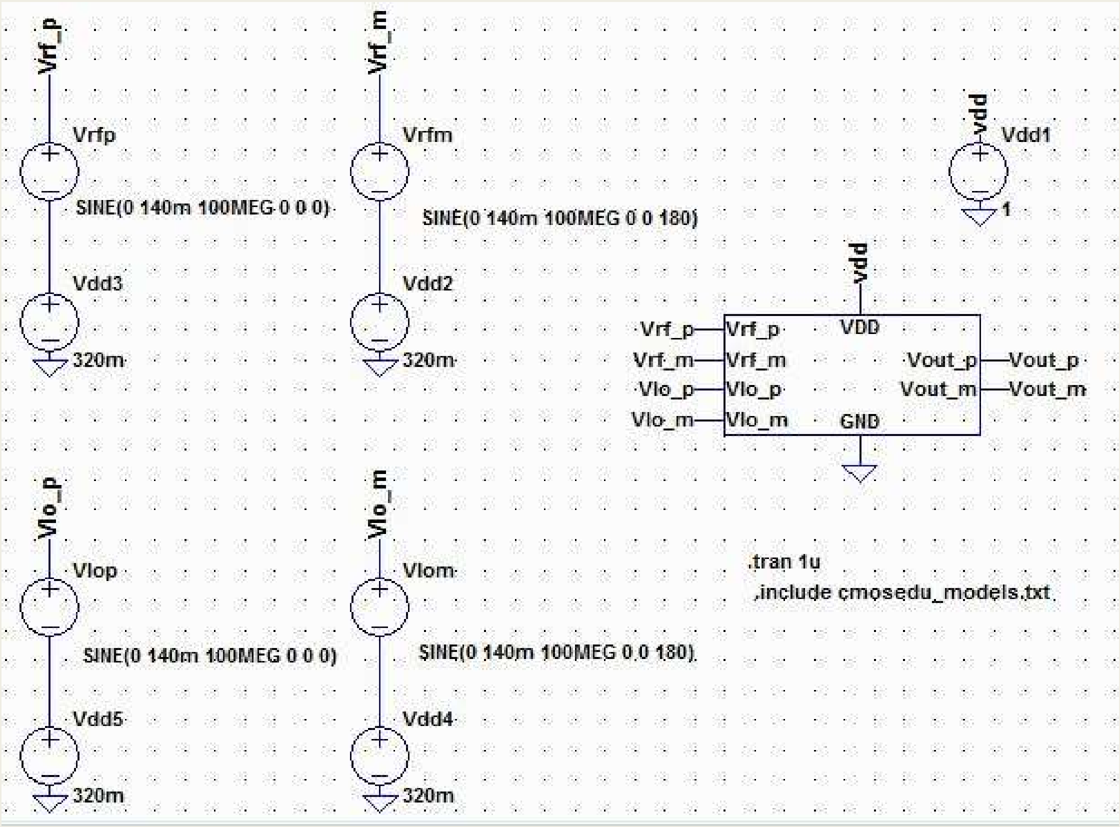
Switching stage

Transconductance stage/Gain

Single-quadrant (x & y uni-polar)
Two-quadrant (x or y bipolar)
Four-quadrant (x & y bipolar)

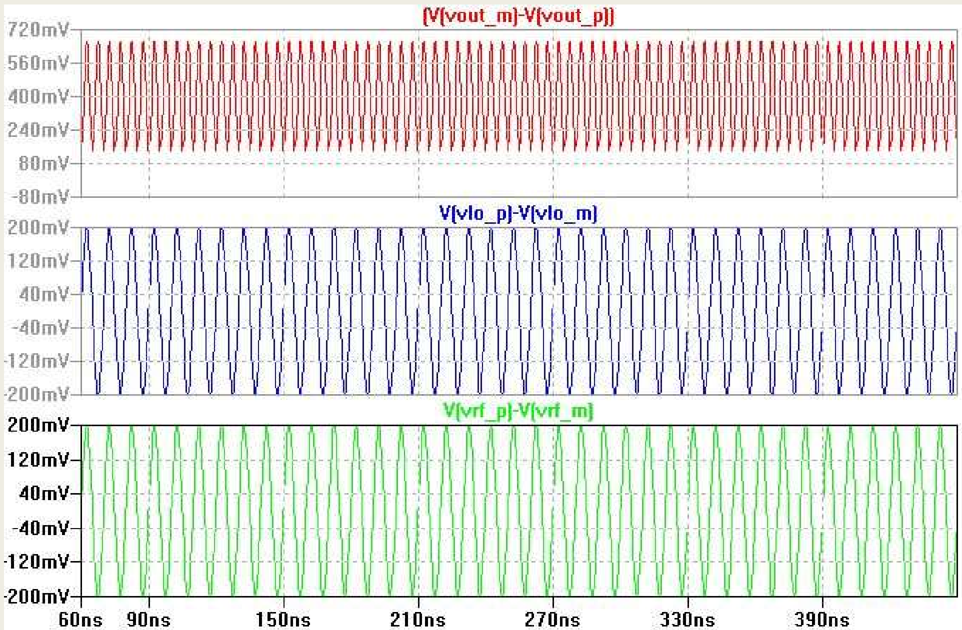
Ref [7], [12]

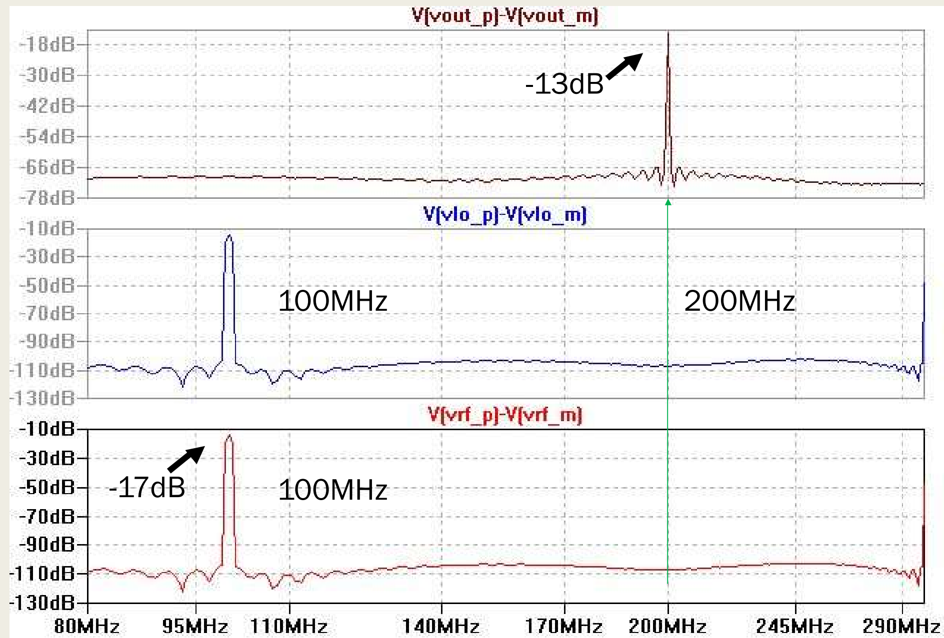
Mixer Simulation I



Ref [8]

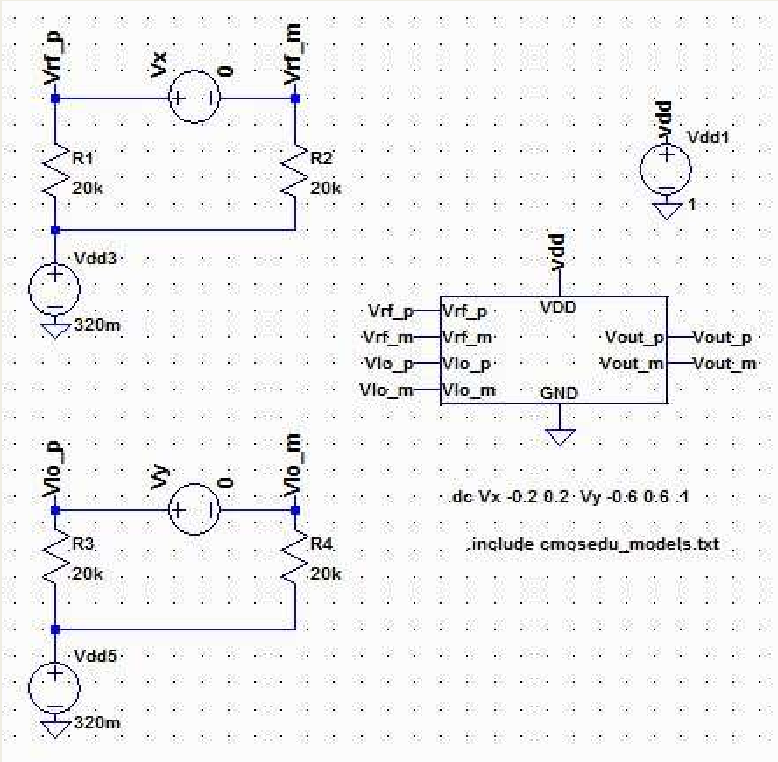
Mixer Simulation I Continued





Ref [8], [9]

DC Characteristics of DBM I



Ref [8]

DC Characteristics of DBM II

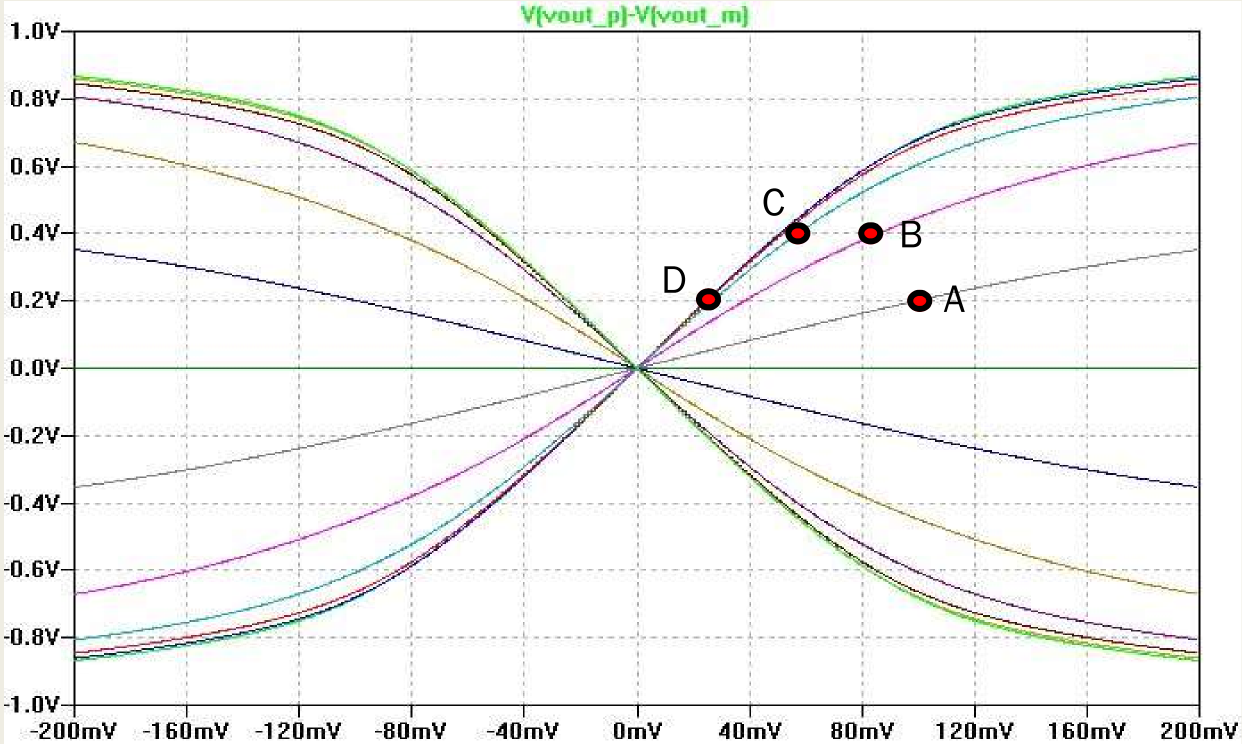
$$K \times V_y \times X_{int} = Y_{int}$$

Ex-

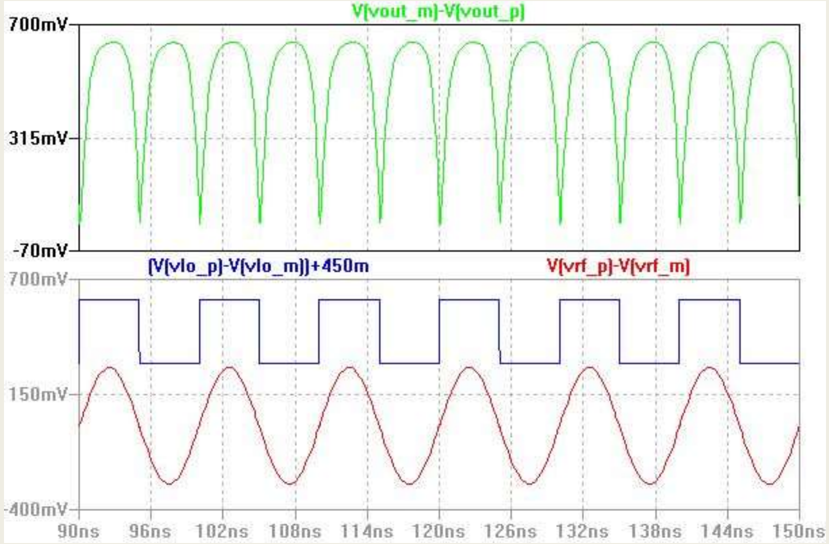
$$K \times 0.1 \times 99.8m = 0.2$$

$$\rightarrow \boldsymbol{K = 20}$$

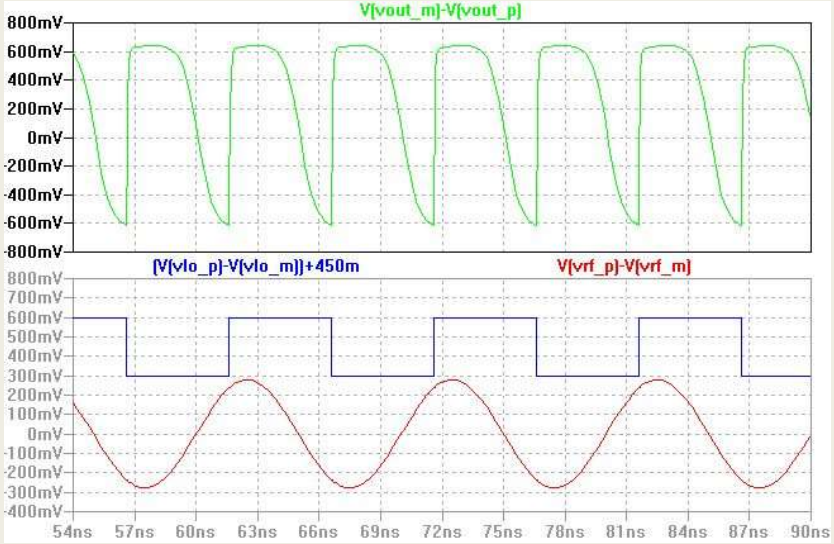
A	K=20
B	K=23.3
C	K=22.7
D	K=20.2



Different DBM phases



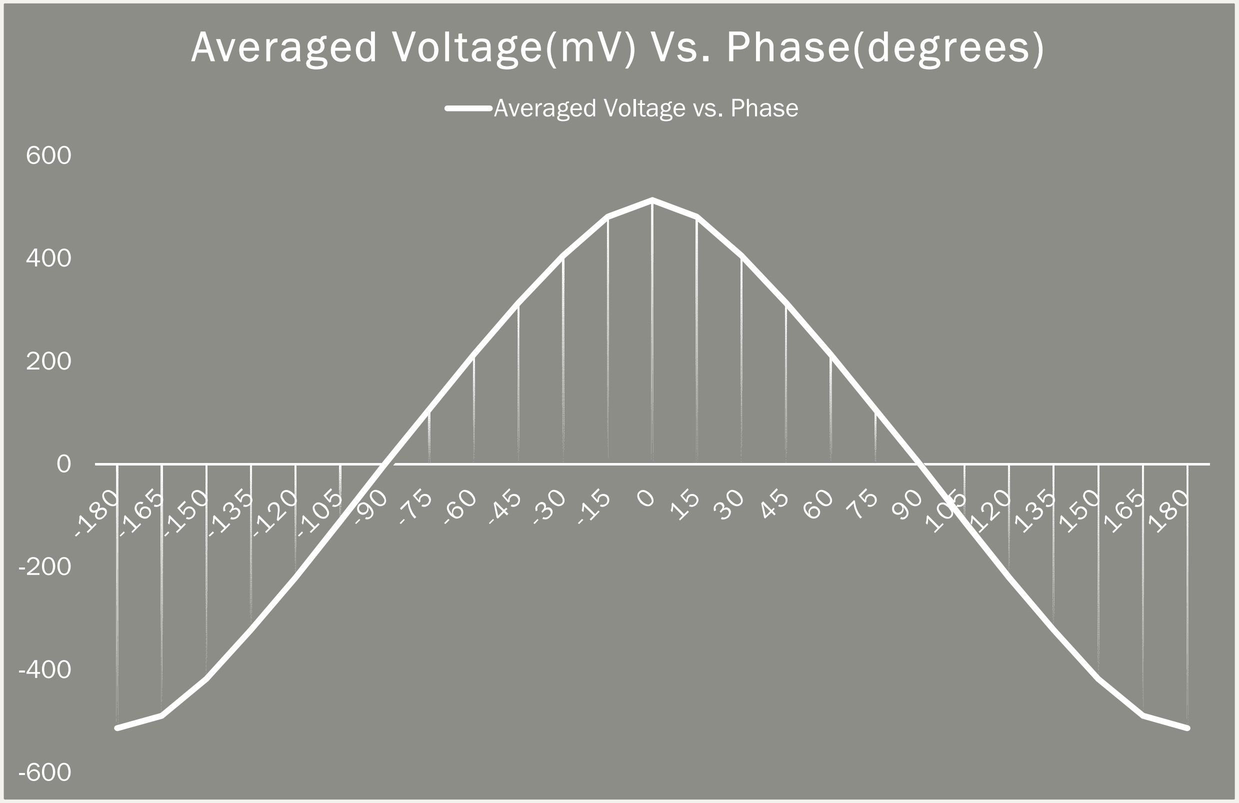
0° *phase difference*



30° *phase difference*

Ref [9]

Phase Detector Gain



$$K_{PD} = \frac{0.513 - 0}{\frac{\pi}{2}}$$

$$K_{PD} = \frac{1.026}{\pi} \approx \frac{1}{\pi}$$

Ref [8], [9]

Voltage Controlled Oscillator (VCO)

- The VCO generates a sinusoidal/pulse signal that is controlled by its input voltage
- The higher the control signal, the higher the frequency

- VCO Specifications
  - *Phase noise*
    - In frequency domain when phase and amplitude are time variant
  - *Tuning range*
    - Output frequency is controlled by the input
  - *Power consumption*
    - Low power consumption is desired

Ref [13]

VCO Types

- Ring VCO
  - *Wide tuning range*
  - *High phase noise*
- LC VCO
  - *Large area*
  - *Narrow tuning range*
  - *Low phase noise*
- Current-starved ring VCO
  - *High phase noise*
  - *High frequency*

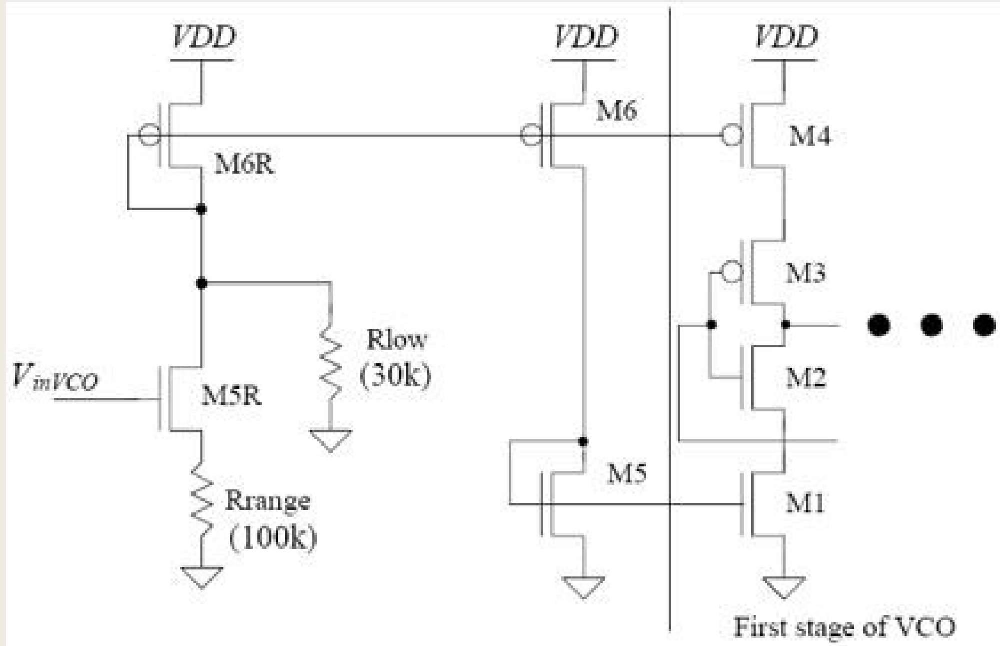
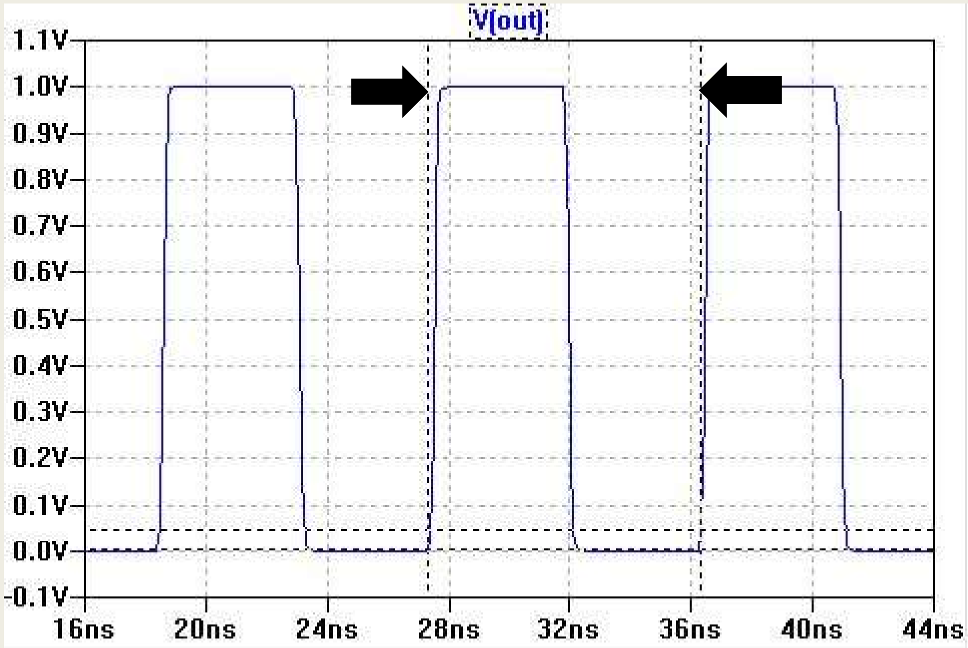


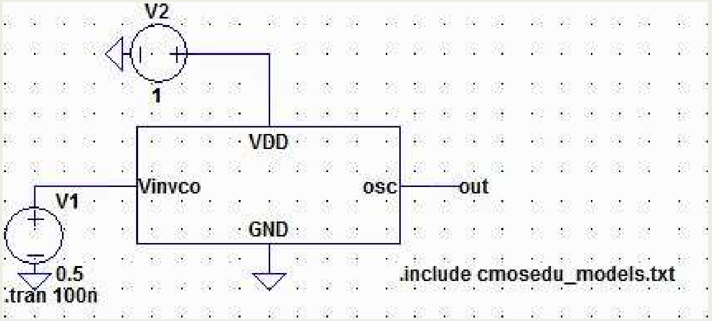
Figure 19.25 Limiting the current in a current-starved VCO.

Ref [8], [14]

Current starved VCO Simulation

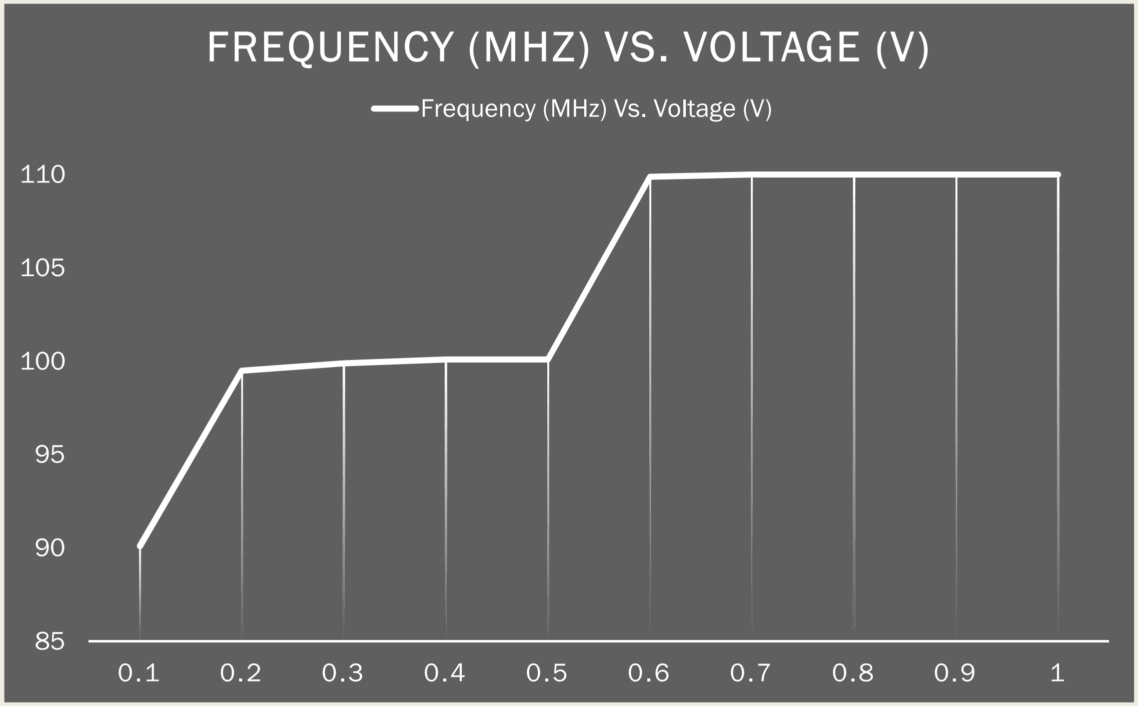
VCO output at 110 MHz





Ref [8]

Gain of VCO

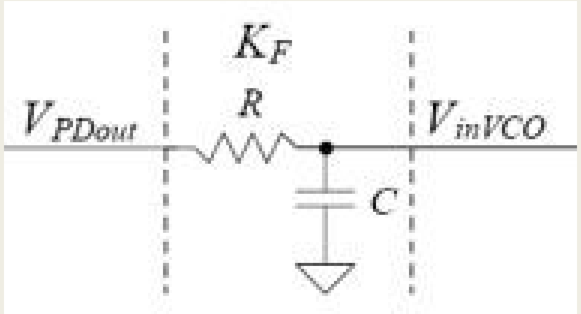


$K_{VCO} \cong 100MHz/V$

Ref [8]

Loop Filter

- Low pass filter used to suppress noise and unwanted multiplier outputs.
- Passive
  - *Uses R and C*
- Active
  - *Uses amplifier*
- First order RC low pass filter was used
  - $K_F = \frac{1}{1+s}$



Ref [8]

PLL Equations

$$H(s) = \frac{K_{PD}K_F K_{VCO}}{s + K_{PD}K_F K_{VCO}}$$

Second order, type II system TF

$$\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{RC}}$$

Natural Frequency

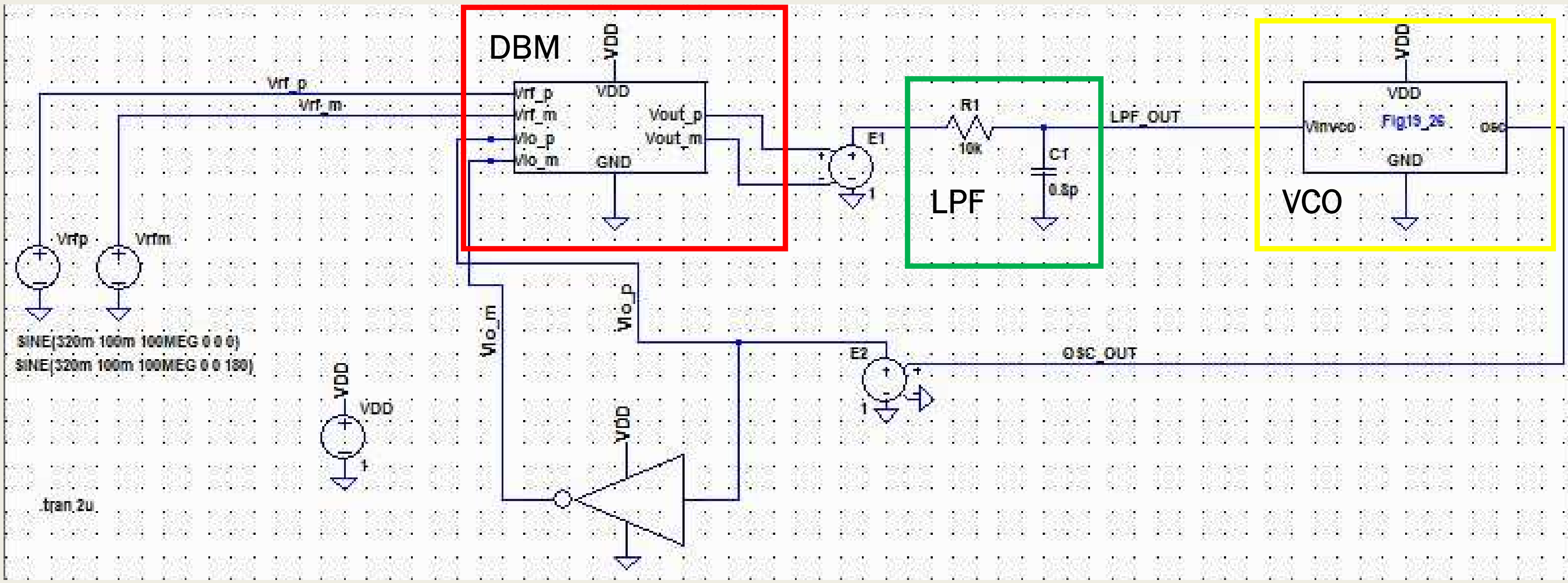
$$H(s) = \frac{K_{PD}K_{VCO}\frac{1}{1+sRC}}{s + K_{PD}K_{VCO}\frac{1}{1+sRC}}$$

Second order, type II system TF

$$\zeta = \frac{1}{2RC\omega_n}$$

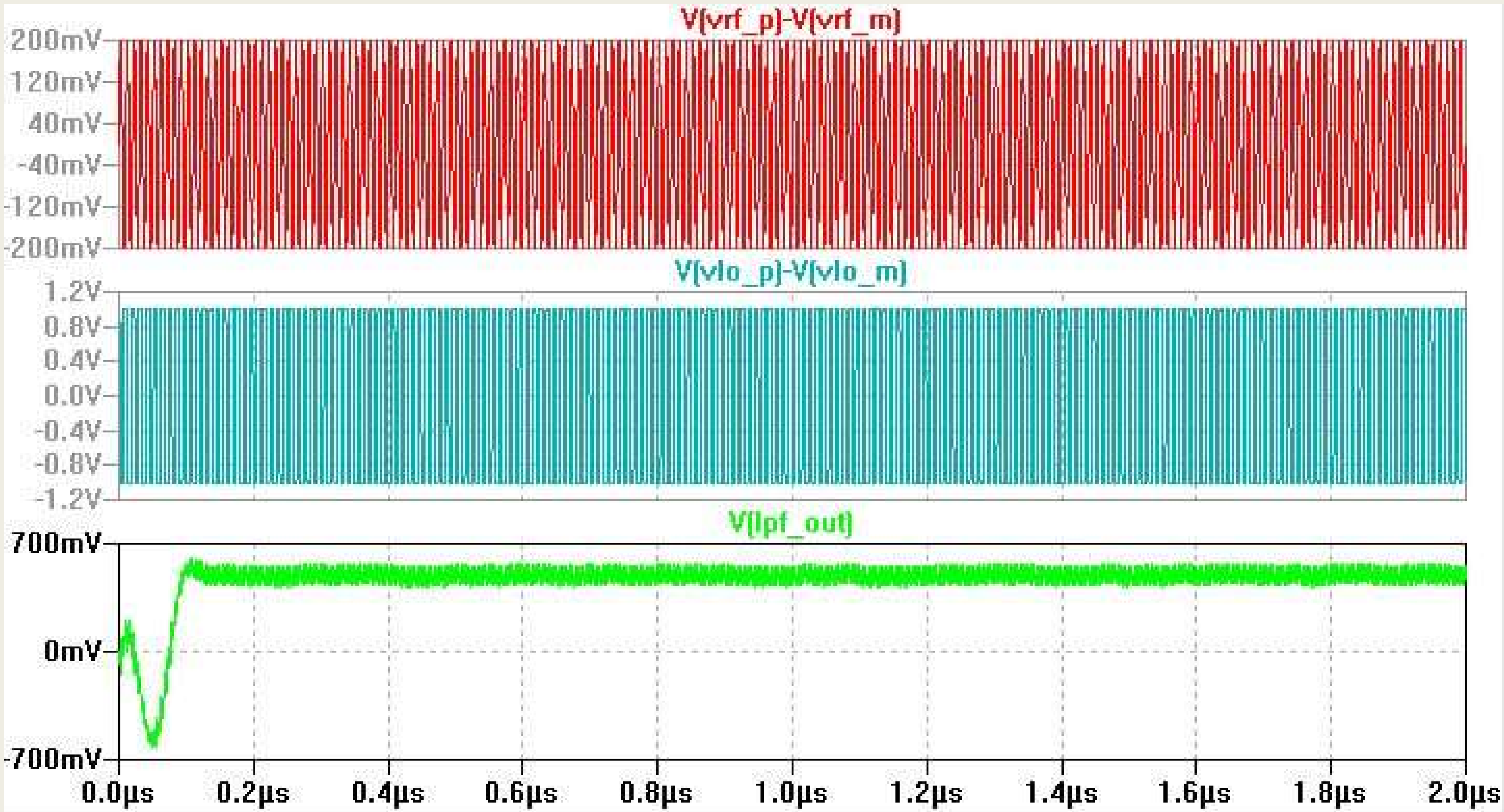
Damping Ratio

Analog PLL

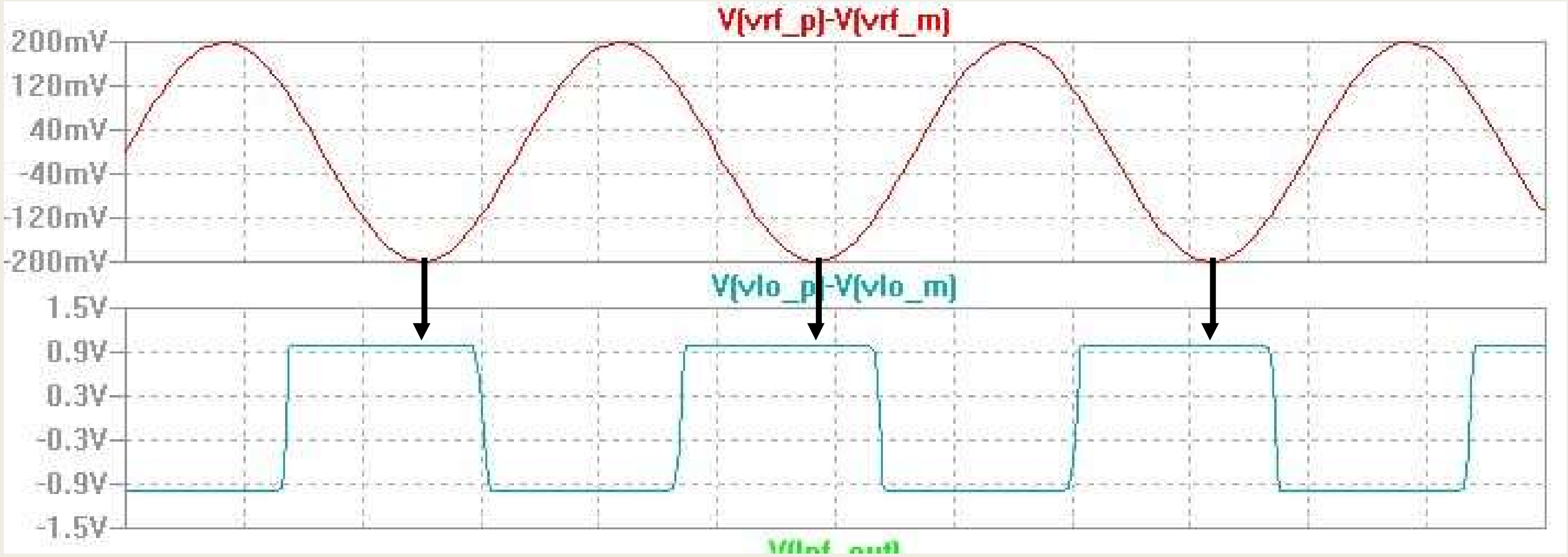


Ref [8]

APLL Waveform I

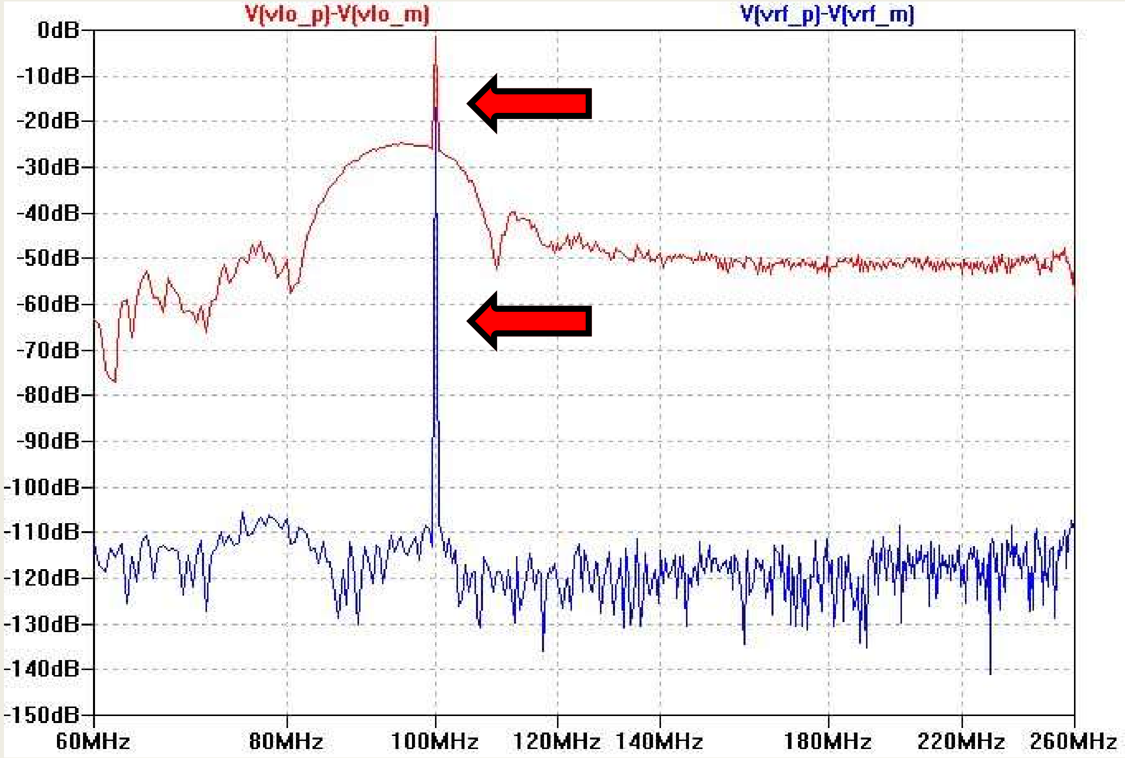


APLL Waveform I Zoomed in



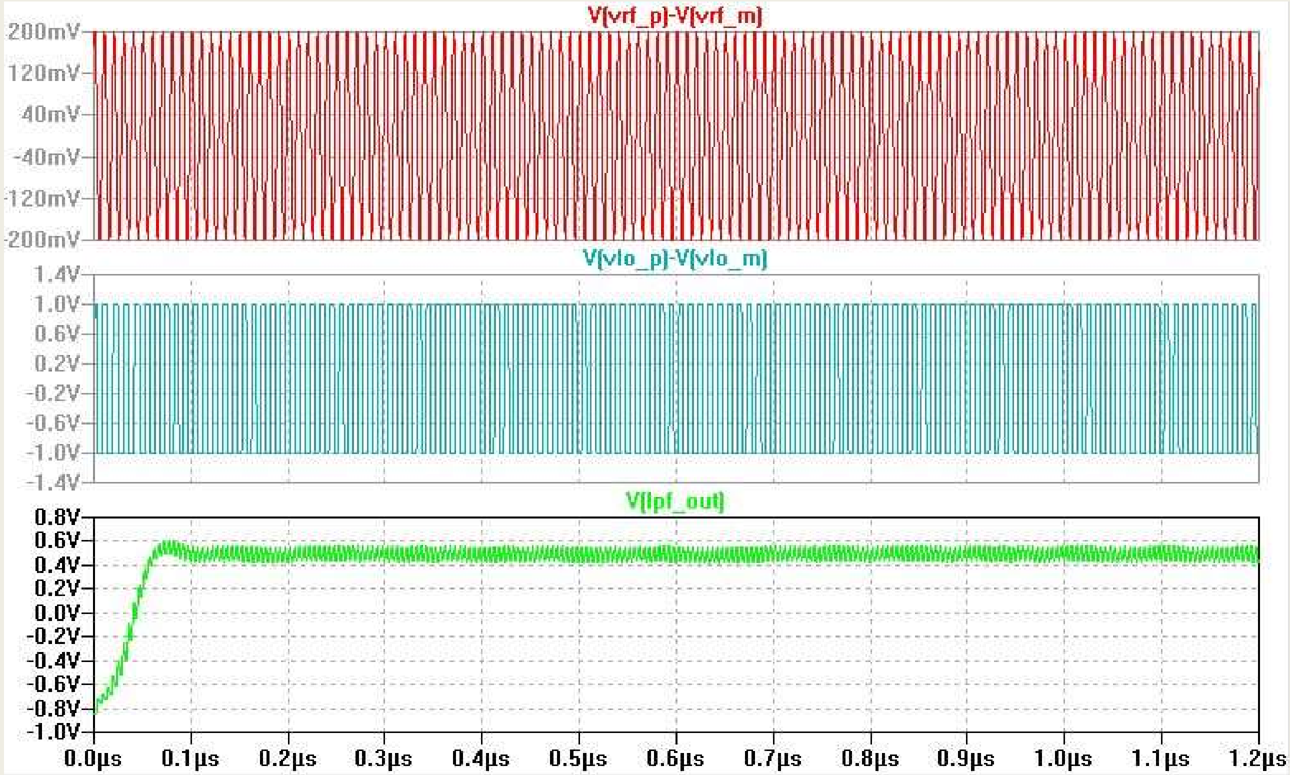
LO and RF waves line up at the same point for every cycle so the loop is locked

FFT Check



The frequency of LO signal is exactly equal to RF signal so the loop is locked

PLL with Phase Difference



Adding a 60 degrees phase to the RF signal

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THANK YOU