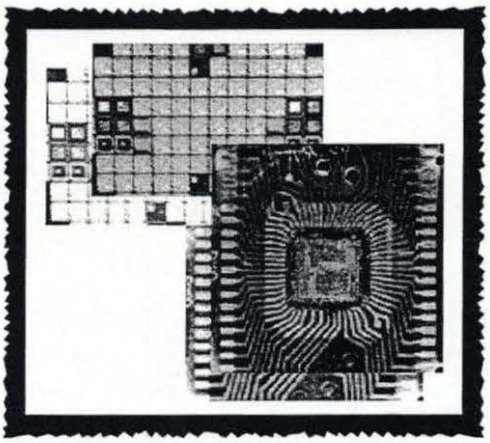
CMOS

Digital Circuit Design

Developed by
R. Jacob Baker
University of Idaho



Tutorial Notes

IEEE
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The following pages contain hardcopy of the visuals presented in the video assignments. You may find it helpful to refer to these visuals when viewing the video segments.

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CMOS Digital Circuit Design

Lesson 2:
The Well

Hardcopy Visuals

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Lesson 2:
The Well

Hardcopy Visuals

Si - 4 val. e^-

p-type — Boron - 3 e^-

N-type - phosphorous - 5e^-.

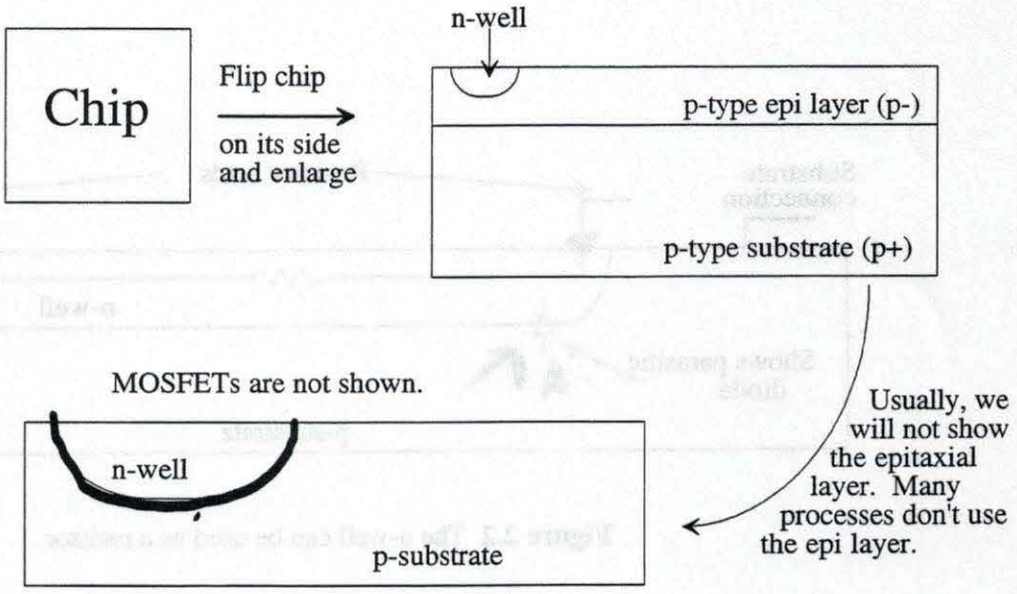


Figure 2.1 Illustration of the top and side view of a die.

Resistor

Body p-channel

diode

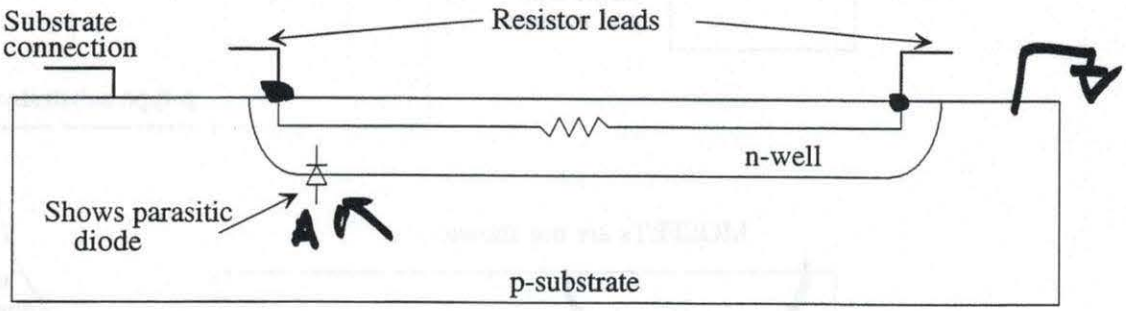
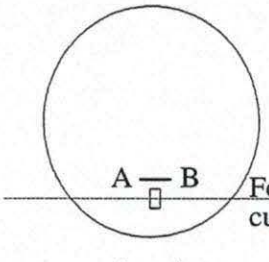
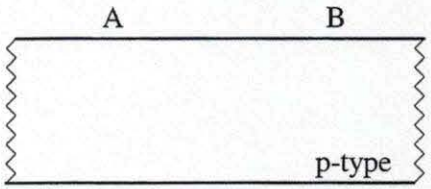


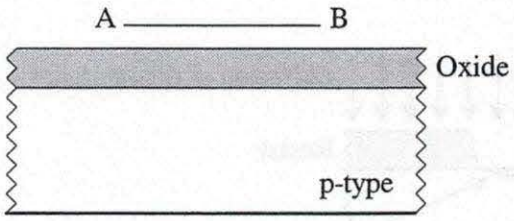
Figure 2.2 The n-well can be used as a resistor.



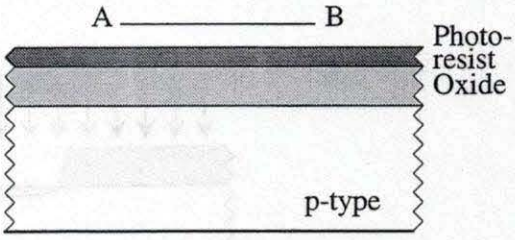
(a) Unprocessed wafer



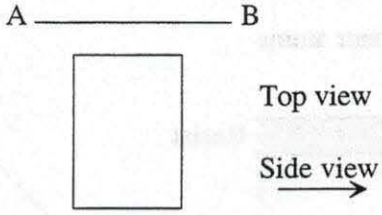
(b) Cross-sectional view of (a)



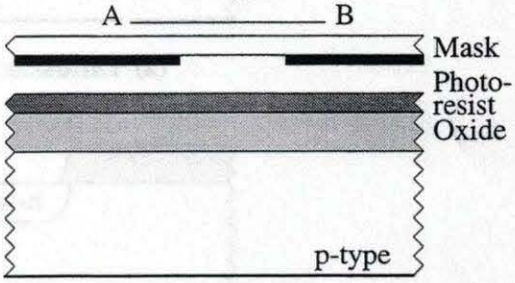
(c) Grow oxide (glass or SiO_2) on wafer.



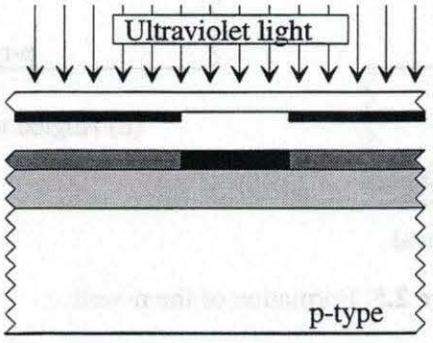
(d) Deposit photoresist



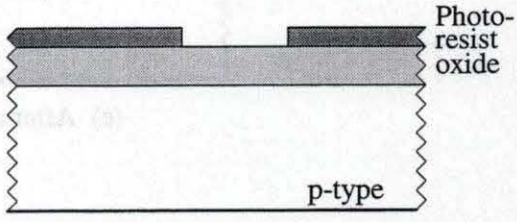
(e) Mask made resulting from LASI layout.



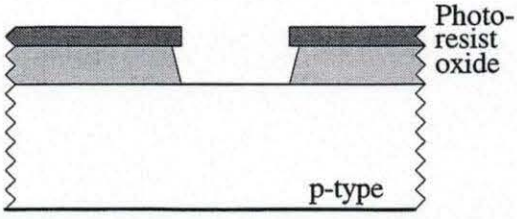
(f) Placement of the mask over the wafer.



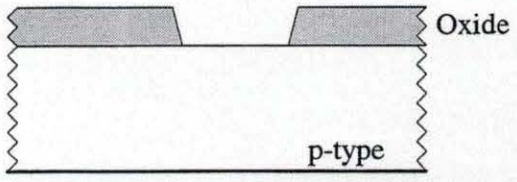
(g) Exposing photoresist.



(h) Developing exposed photoresist.



(i) Etching oxide to expose wafer.



(j) Removal of photoresist.

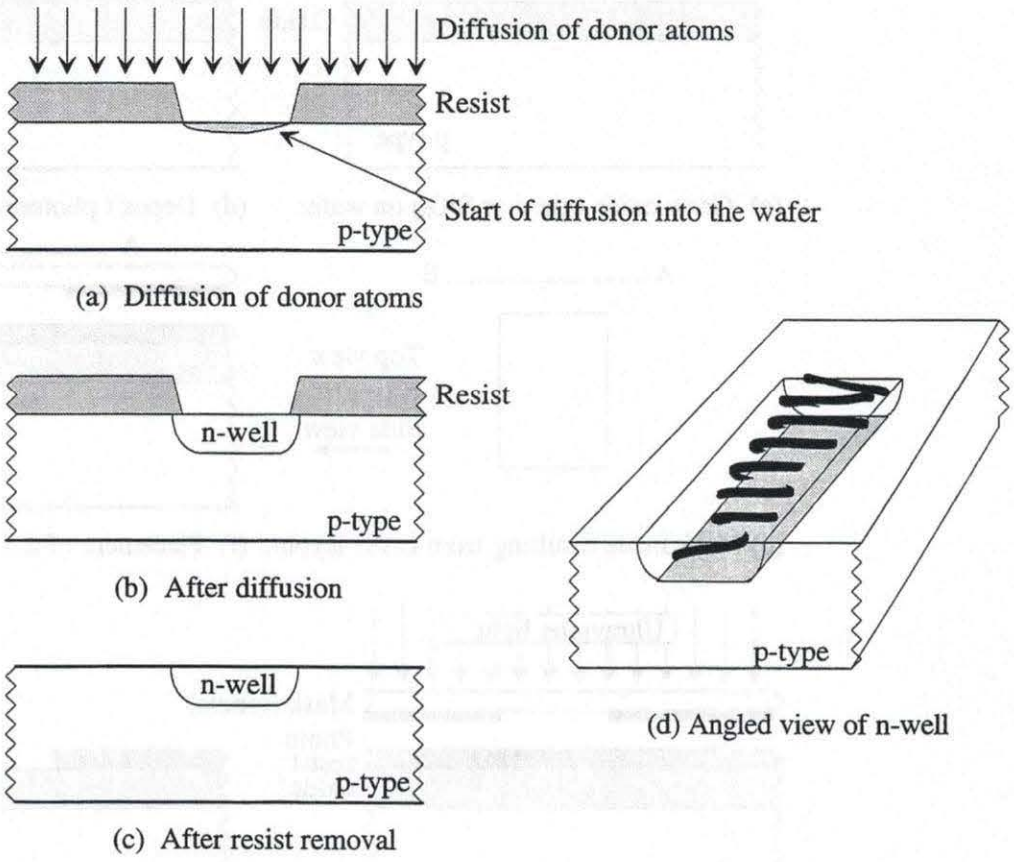
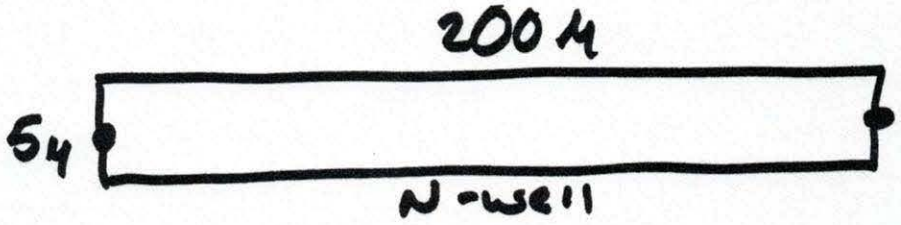


Figure 2.5 Formation of the n-well.

$1\mu = 10^{-6}\,m$



CN20

App. A

$$R = R_{\square} \cdot \frac{200}{5}$$

$$= 2.5K \cdot 40 = \underline{\underline{100K\Omega}}$$

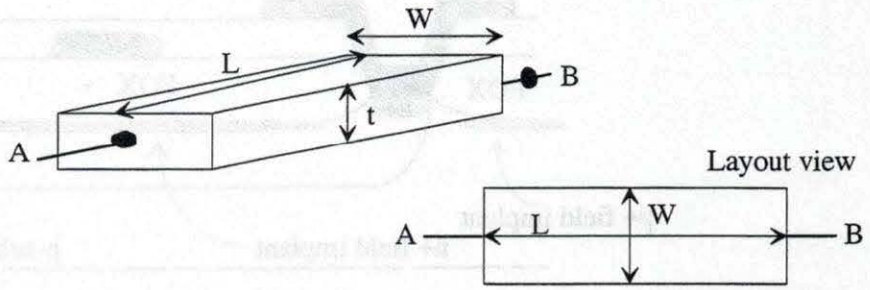


Figure 2.8 Calculation of the resistance of a rectangular block of material.

$$R = \frac{\rho}{t} \cdot \frac{L}{W}$$

$$R = R_{\square} \cdot \frac{L}{W}$$

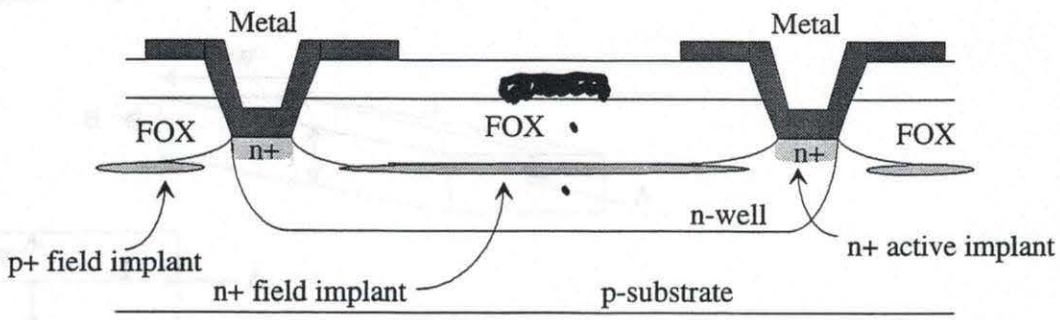


Figure 2.10 Cross-sectional view of n-well showing field implant. The field implantation is sometimes called the "channel stop implant".

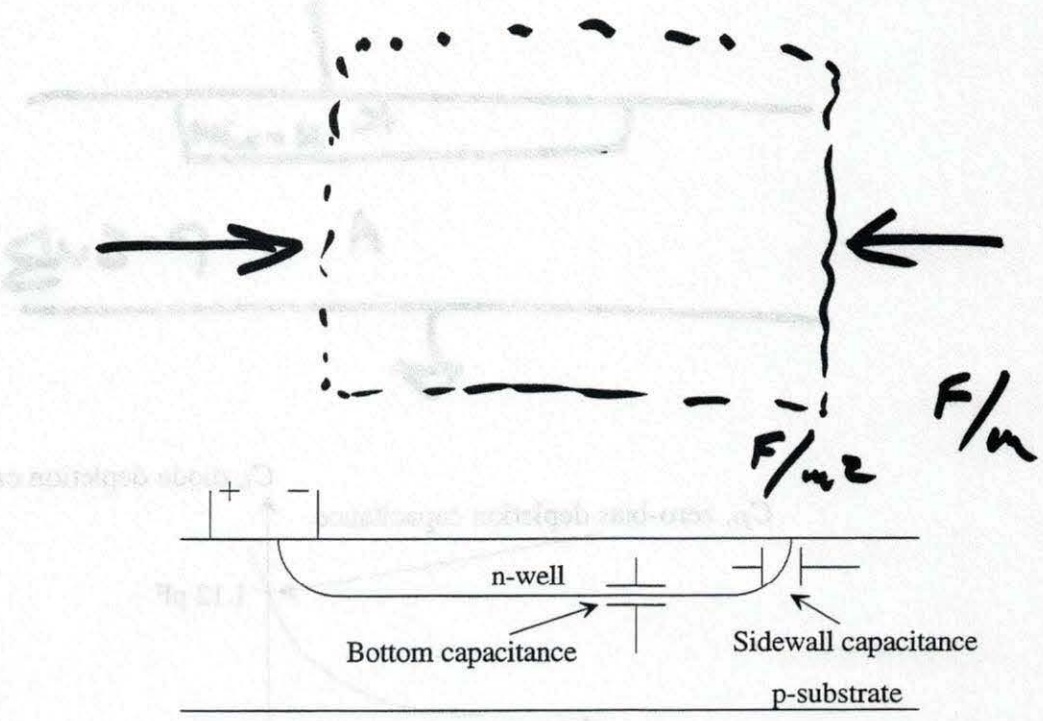
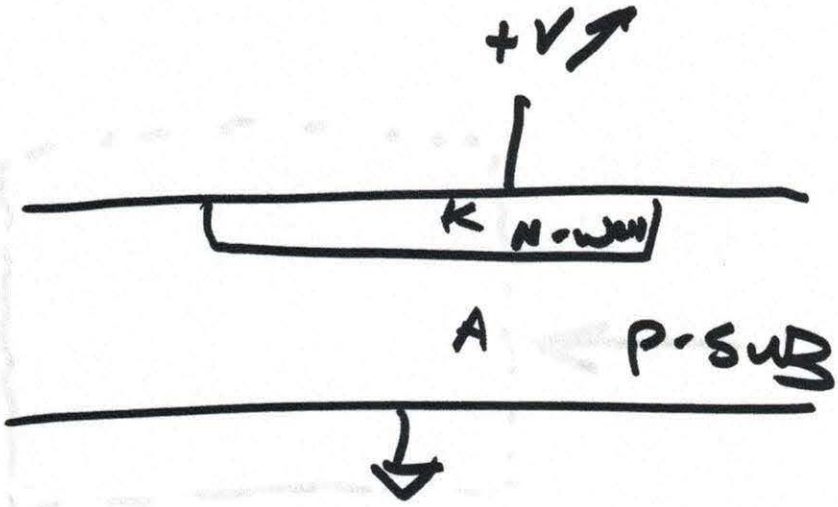


Figure 2.12 A pn junction on the bottom and sides of the junction.



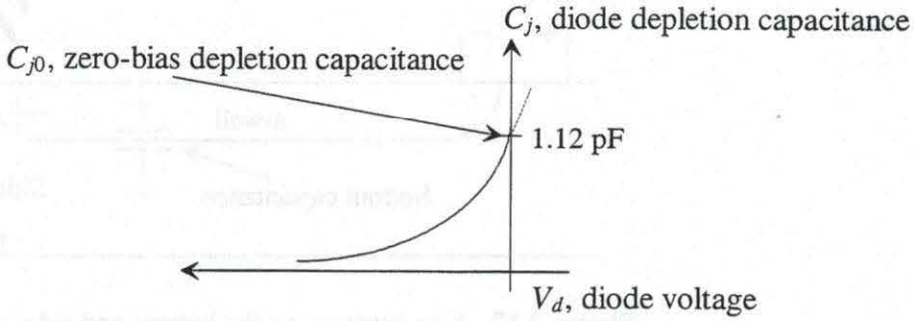


Figure 2.13 Sketch of diode depletion capacitance against diode reverse voltage.

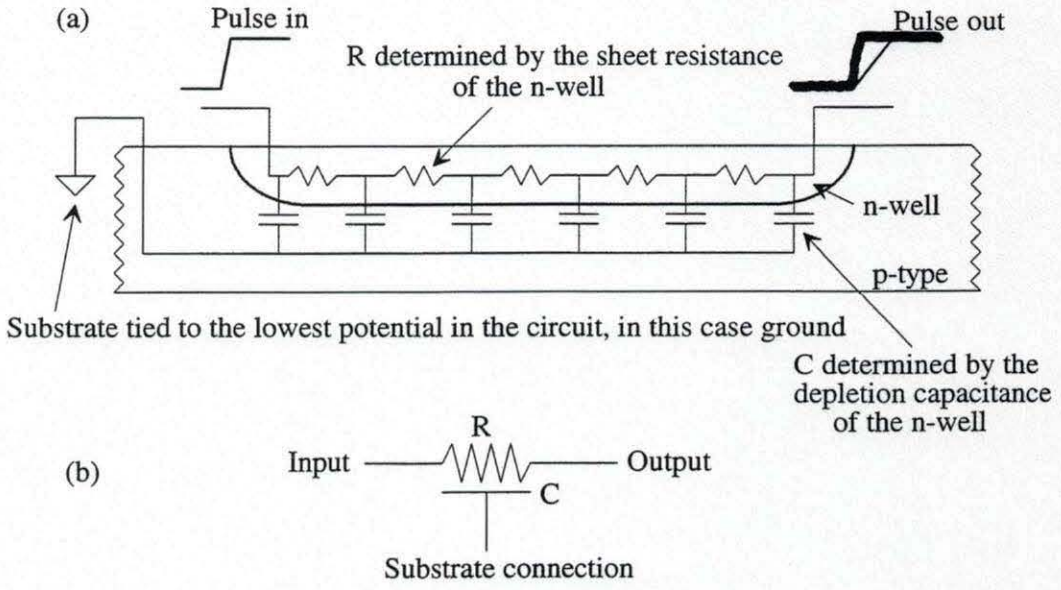


Figure 2.17 (a) Parasitic resistance and capacitance of the n-well and (b) schematic symbol.

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Lesson 3:
The Metal Layers

Hardcopy Visuals

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Lesson 3:
The Metal Layers

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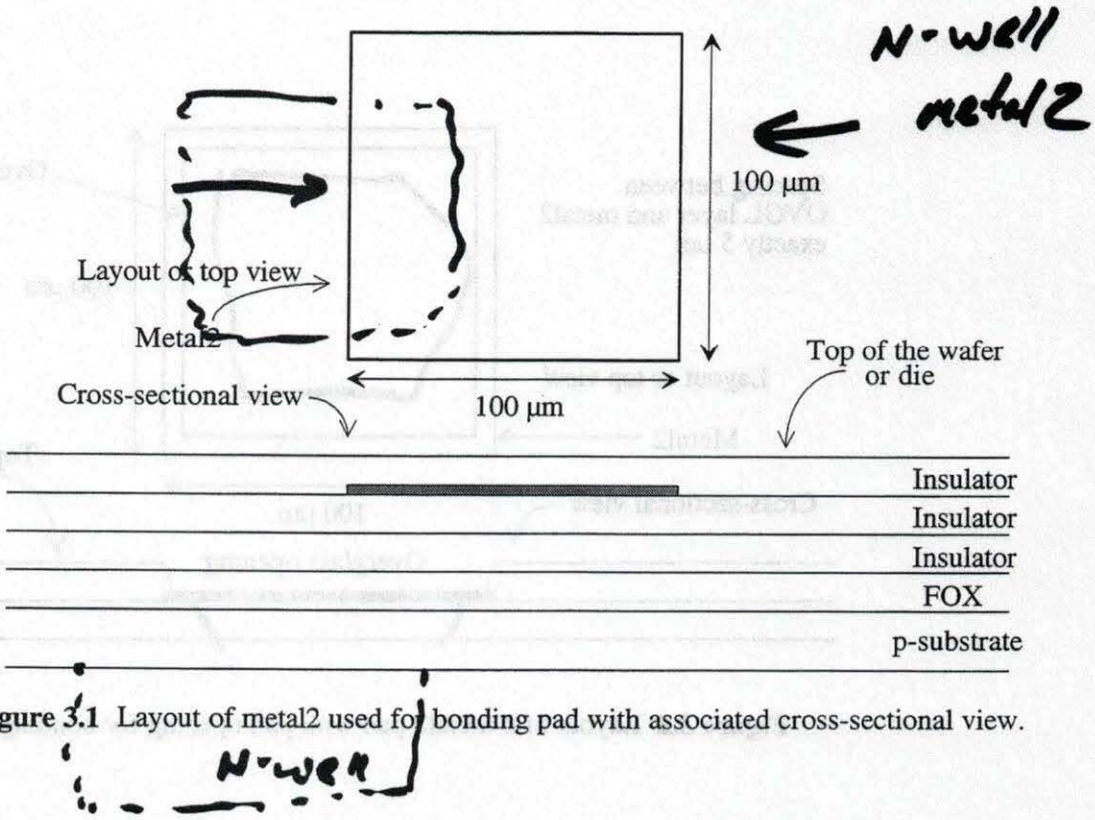

Figure 3.1 Layout of metal2 used for bonding pad with associated cross-sectional view.

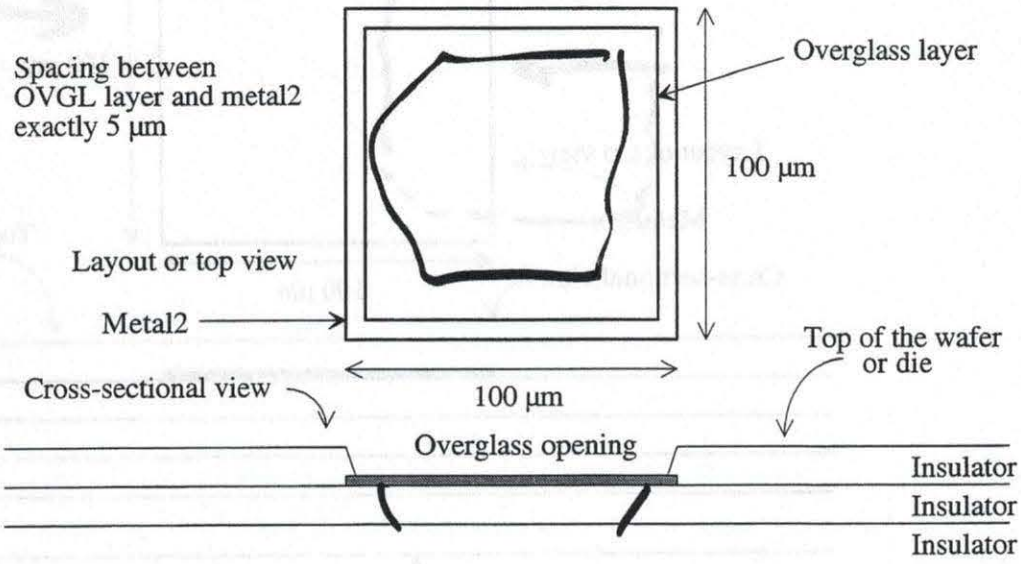

Figure 3.2 Layout of a metal2 pad with pad opening for bonding connection.

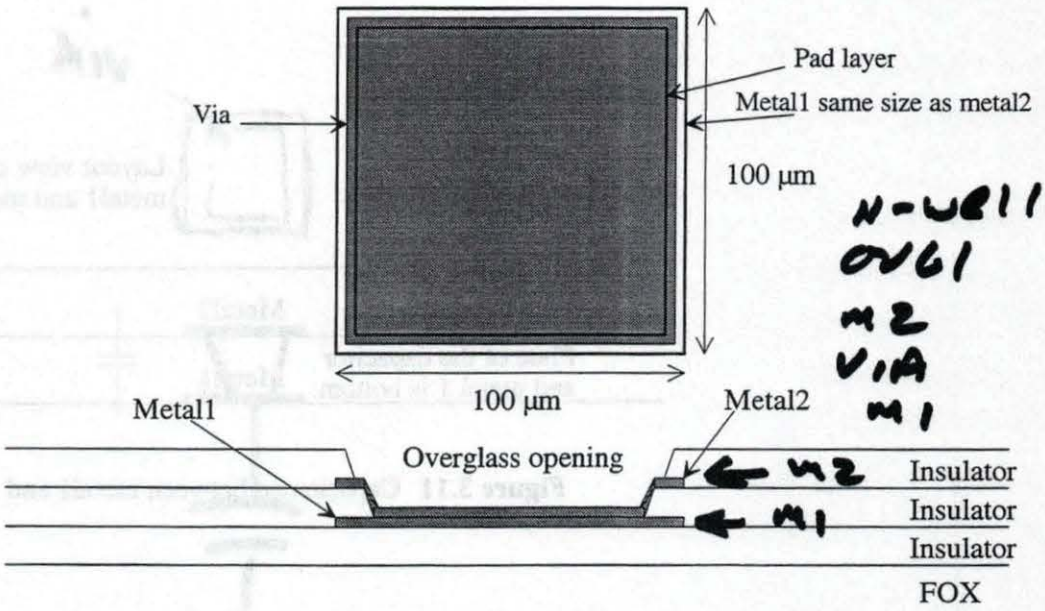

Figure 3.3 A bonding pad using metal1 and metal2.

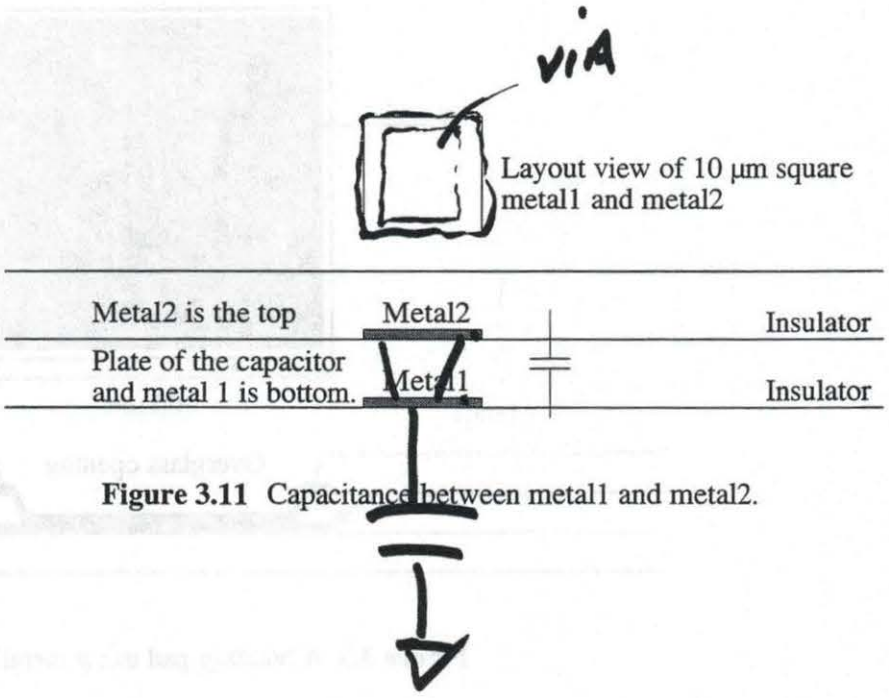

Figure 3.11 Capacitance between metal1 and metal2.

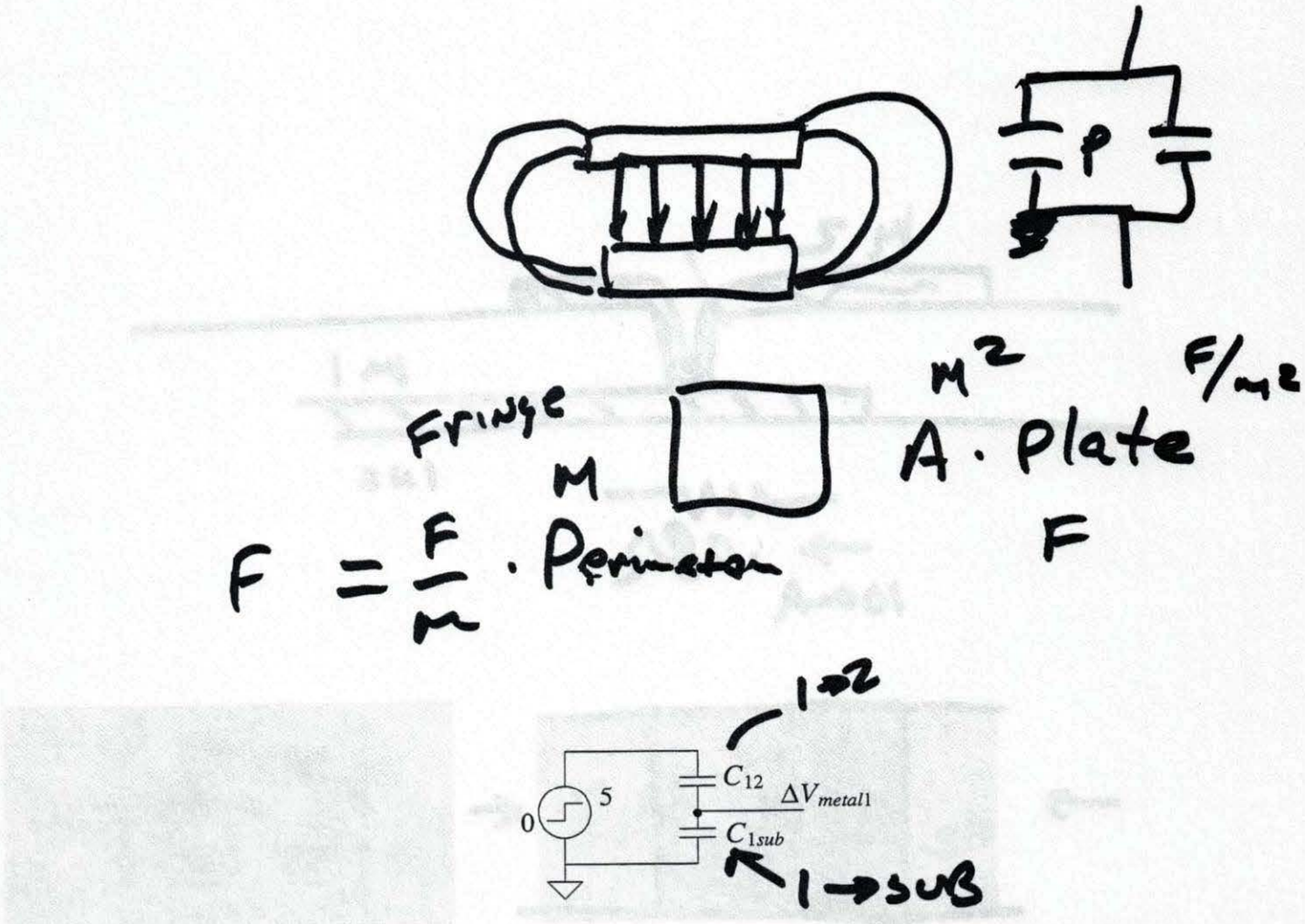

Figure 3.12 Equivalent circuit used to calculate the change in metal1 voltage.

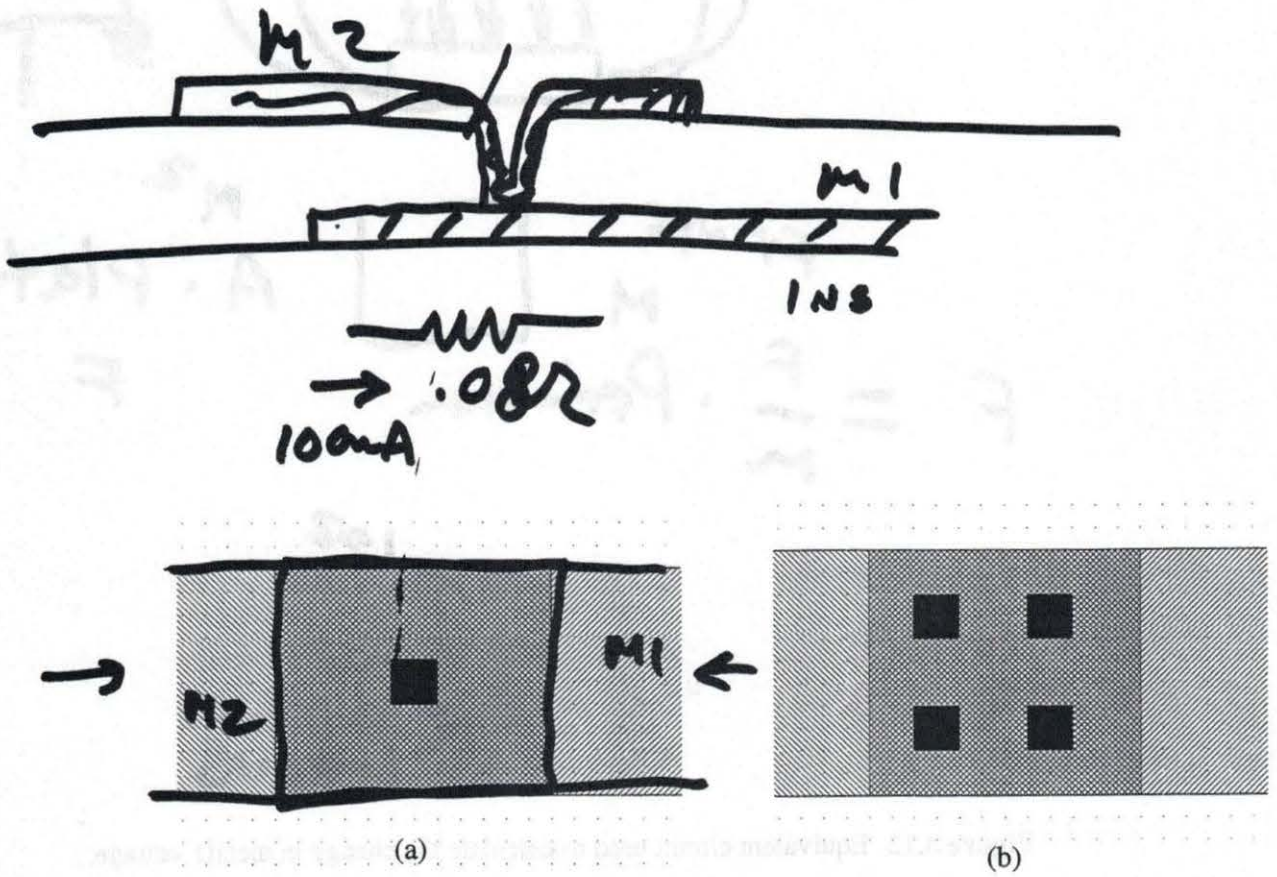

Figure 3.13 Layouts used in Example 3.7.

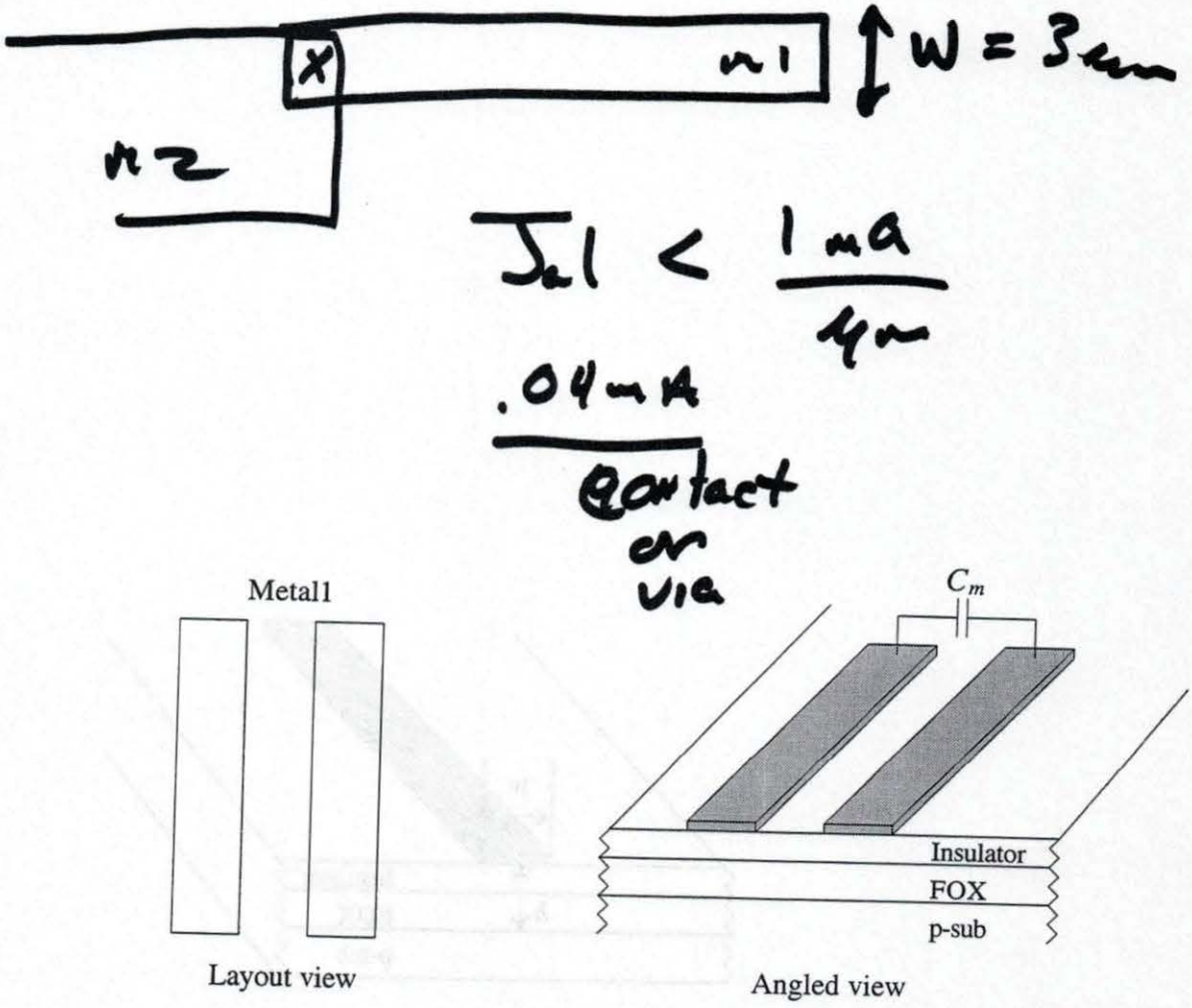

Figure 3.14 Conductors used to illustrate crosstalk.

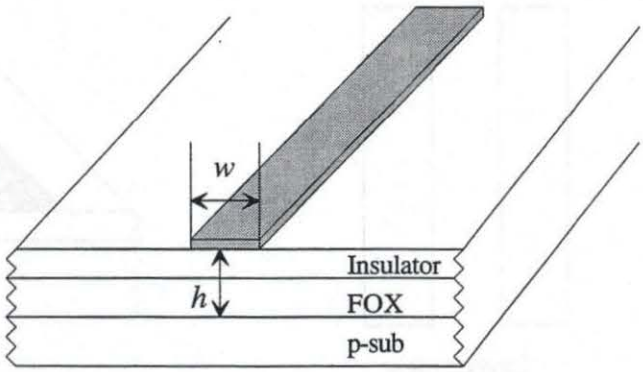

Figure 3.15 Conductors used in calculation of inductance.

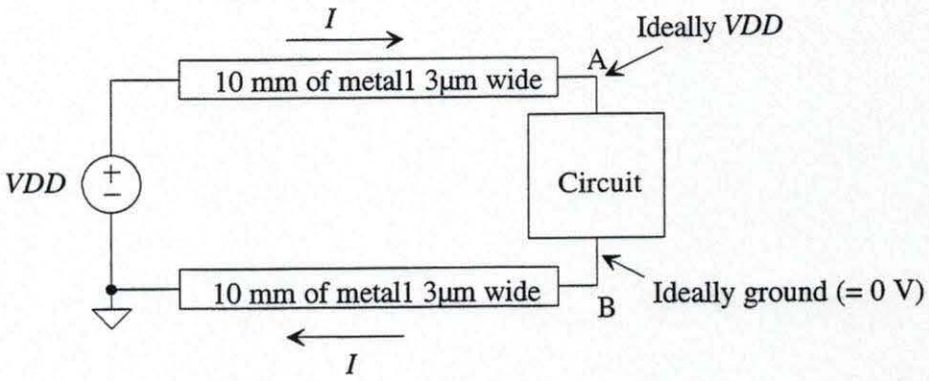

Figure 3.16 Block diagram used to illustrate ground bounce.

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Lesson 4:
The Active and Poly Layers

Hardcopy Visuals

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The Active and Poly Layers

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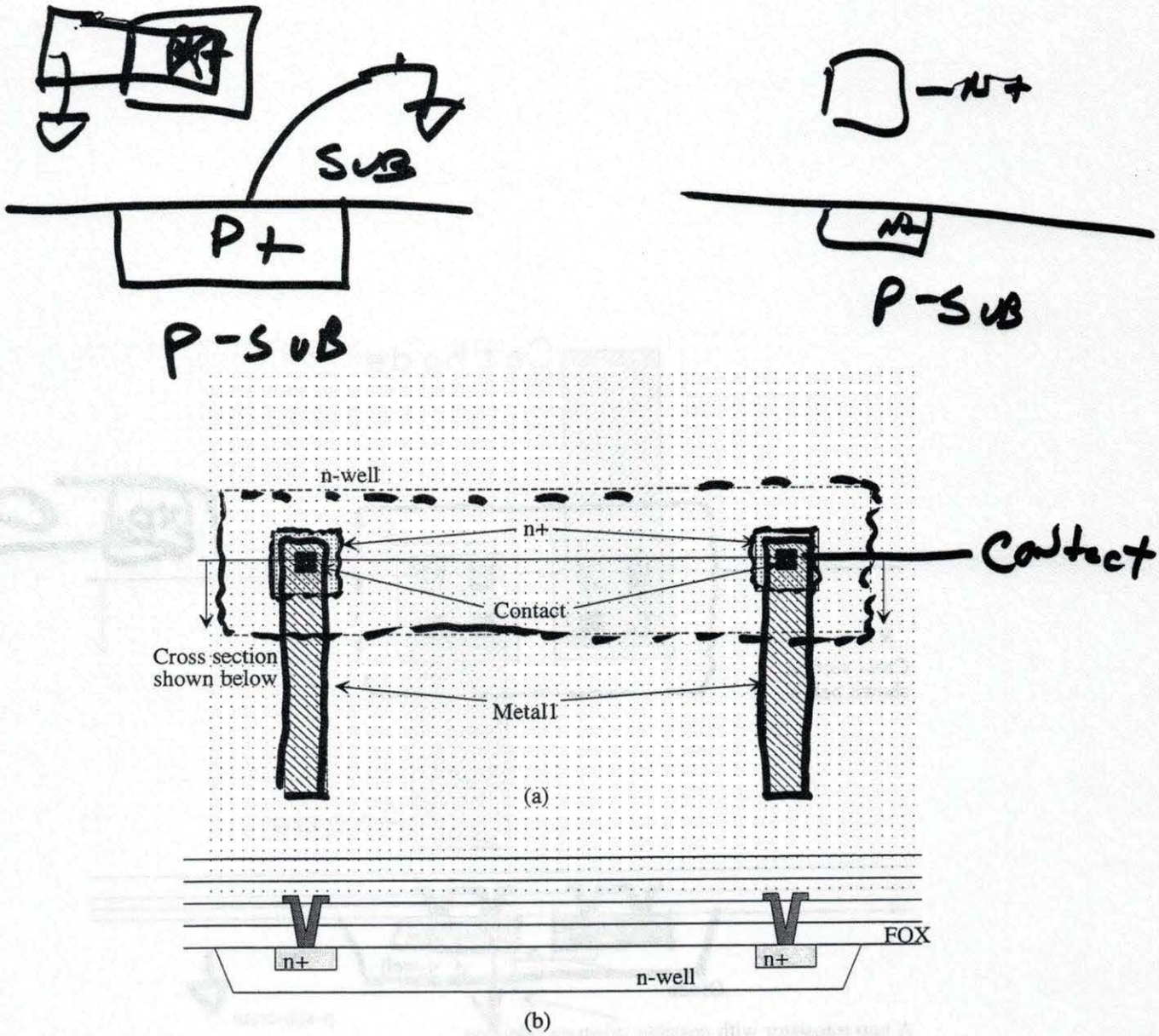

Figure 4.1 Layout of an n-well resistor with active contacts to metal1 (a) Actual layout using LASI, (b) cross-sectional view across the contacts.

OVGL P+

M2 N+

VIA N-well

M1 Poly

CONT

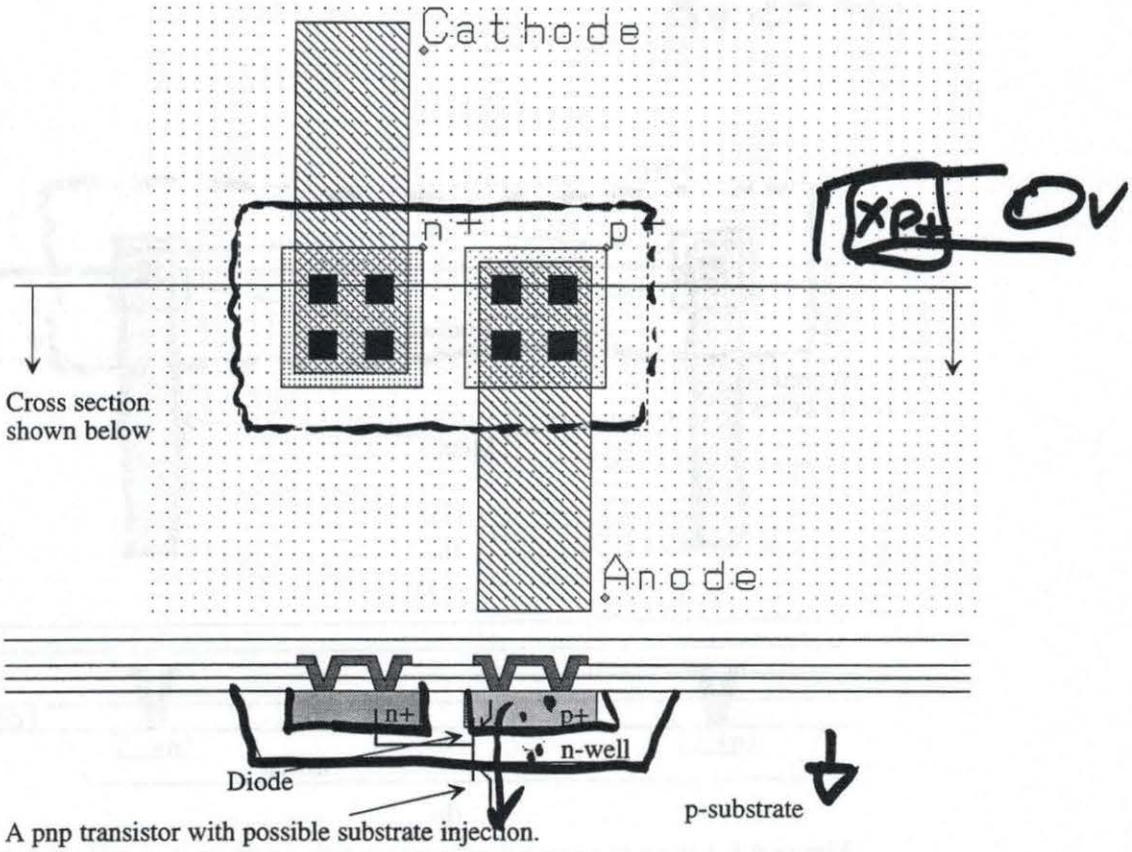

Figure 4.3 Layout of a 10 um by 10 um diode using the n-well as the cathode.

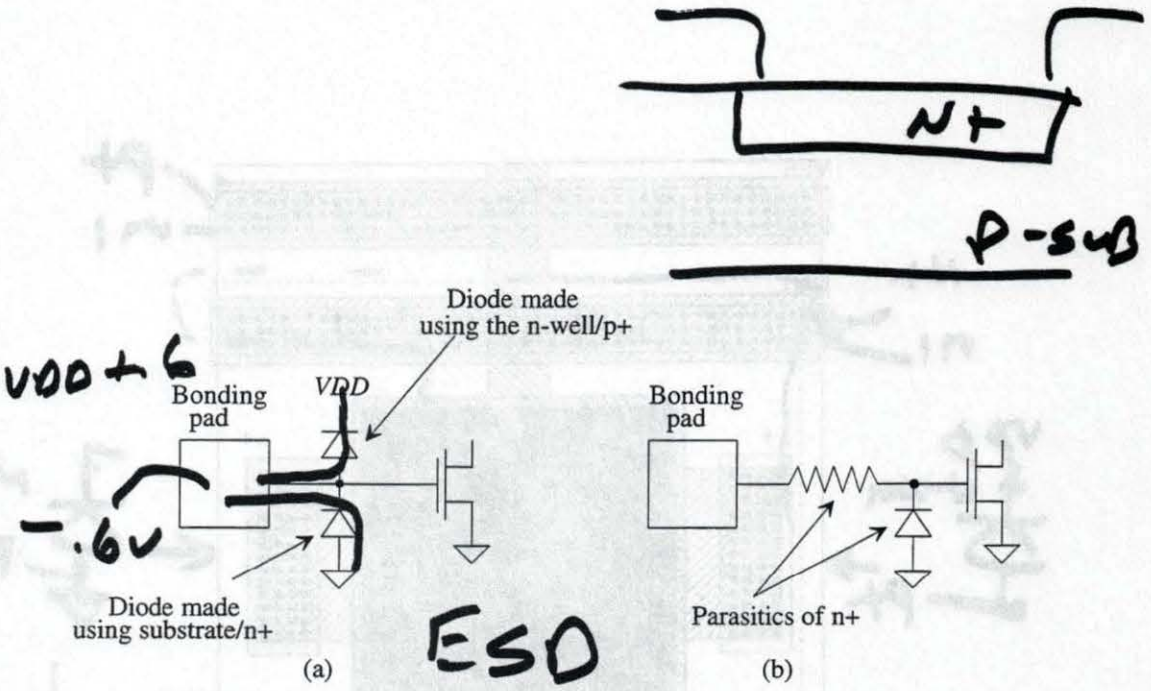

Figure 4.5 Two methods of protecting against ESD damage.

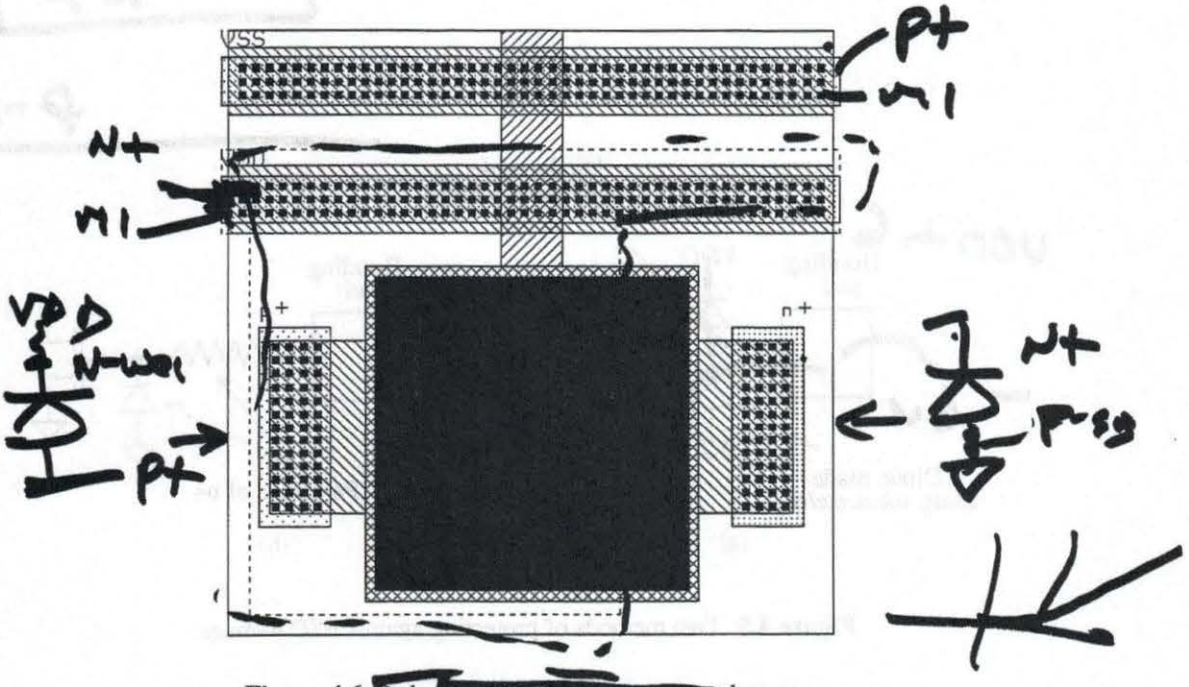

Figure 4.6 Pad with ESD diodes and power busses.

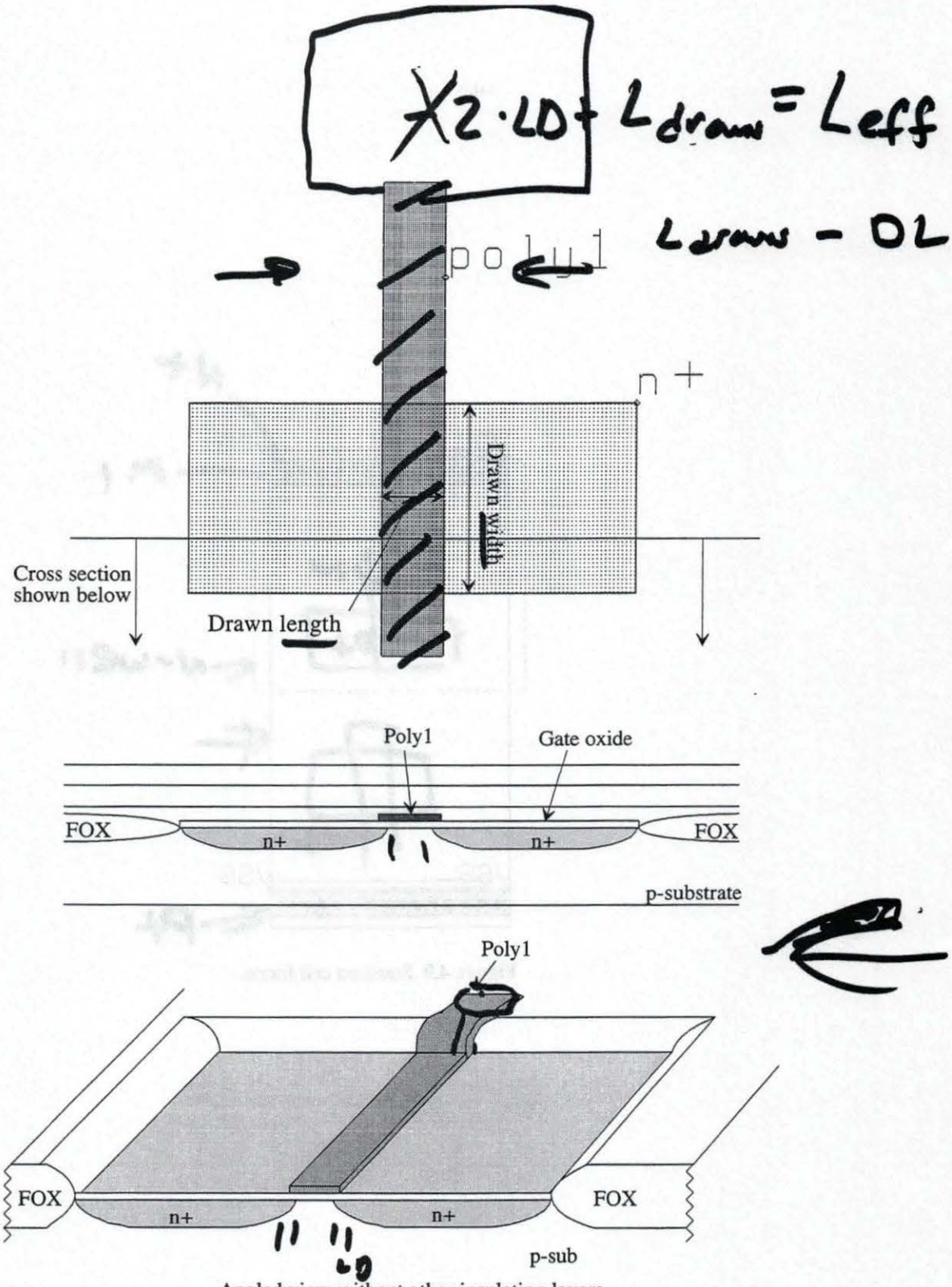

Figure 4.8 Layout of a MOSFET, cross-sectional and angled view.

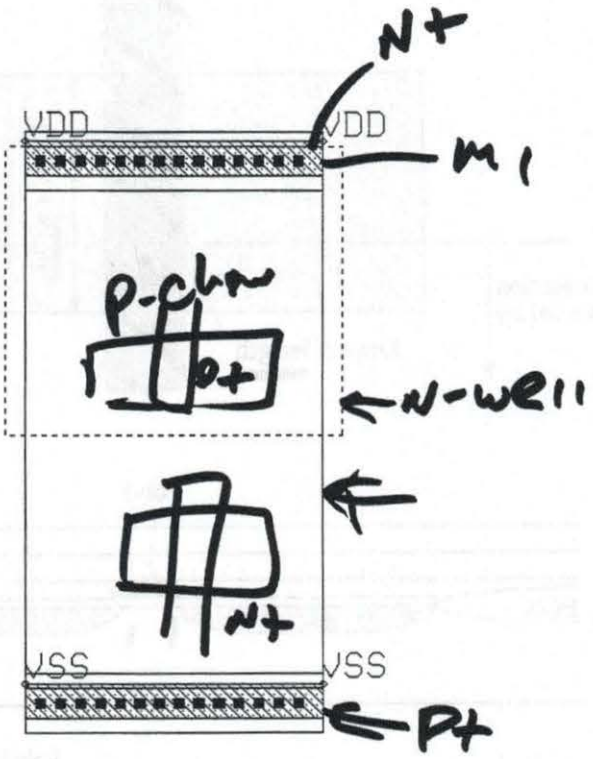

Figure 4.9 Standard cell frame.

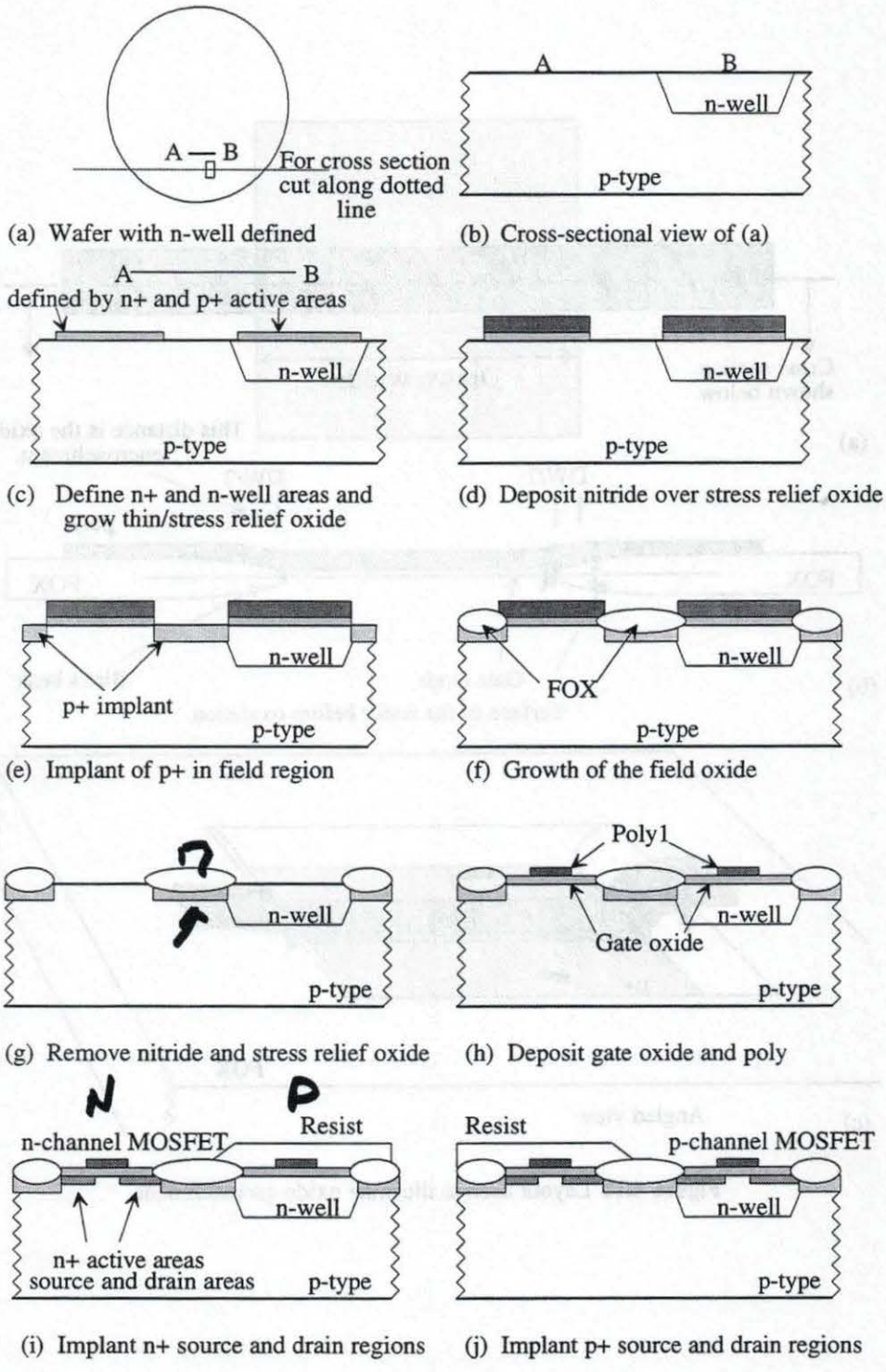

Figure 4.10 Sequence of events used in MOSFET formation.

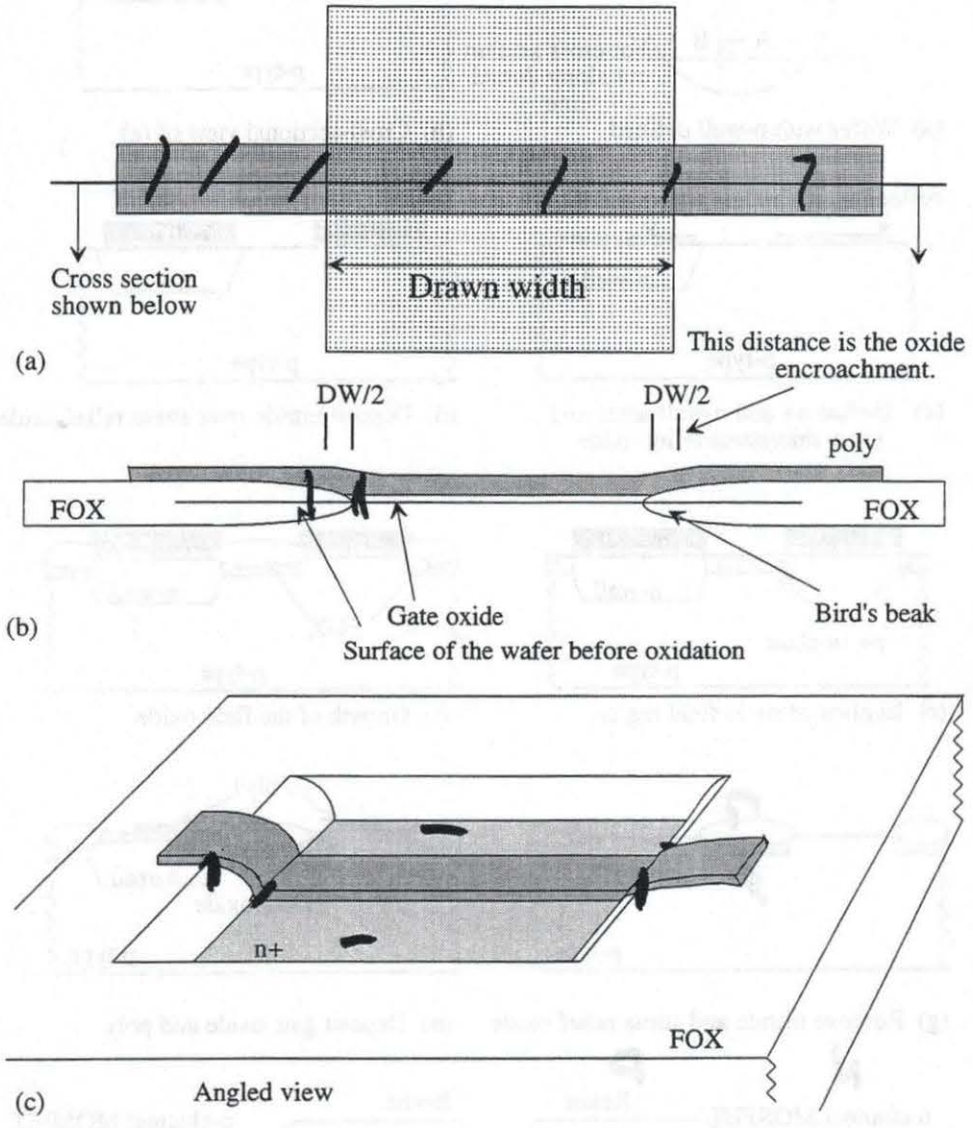

Figure 4.11 Layout used to illustrate oxide encroachment.

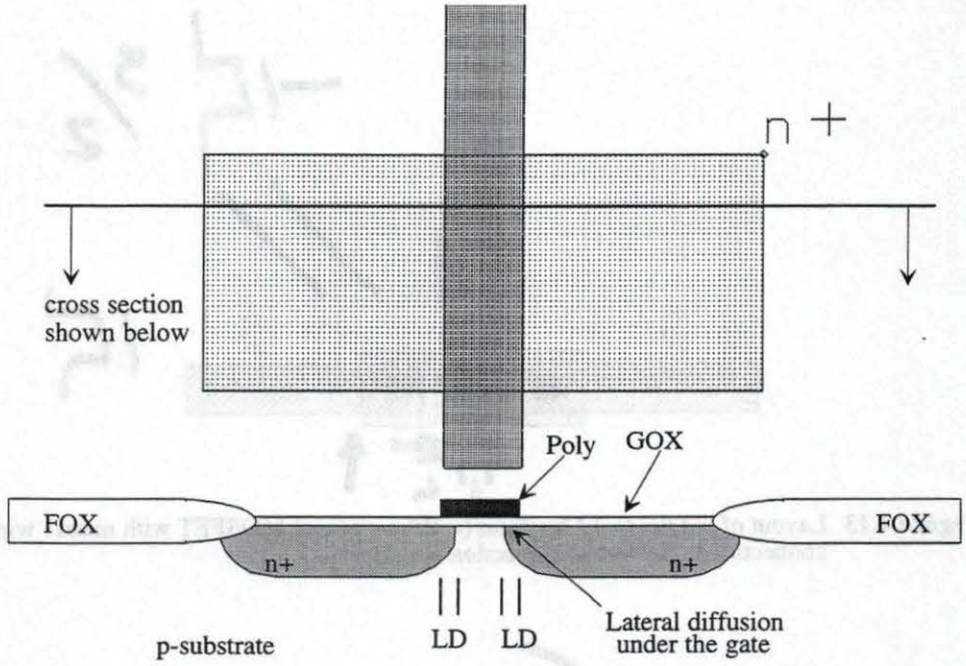

Figure 4.12 Layout used to illustrate lateral diffusion.

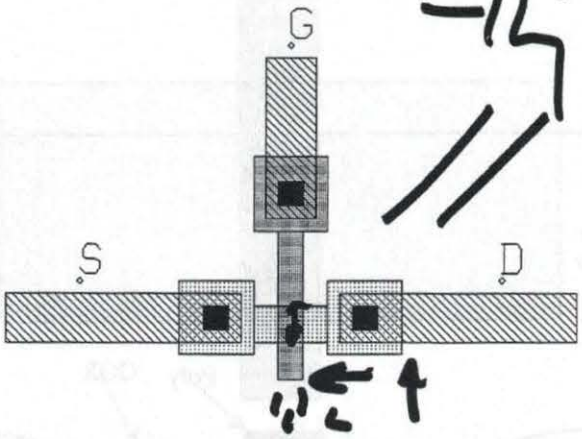

Figure 4.13 Layout of a 2 μm (= L) by 3 μm (= W) n-channel MOSFET with metal1 wire connections. Substrate connection not shown.

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Lesson 5:
The MOSFET as a Capacitor

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Lesson 5:
The MOSFET as a Capacitor

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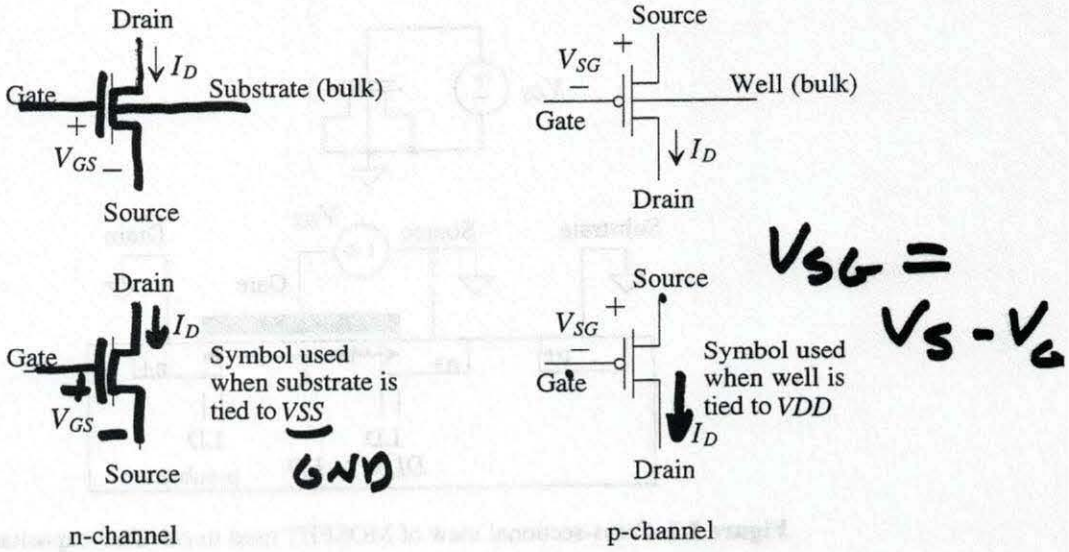
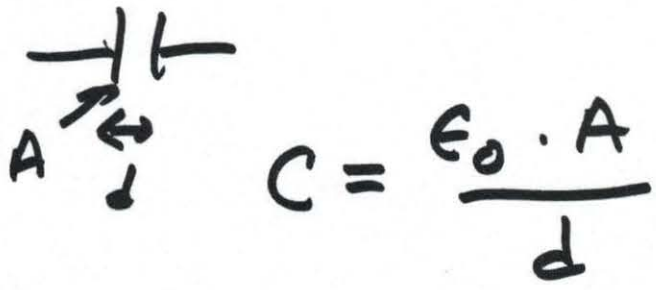


Figure 5.1 Symbols used for n- and p-channel MOSFETs.



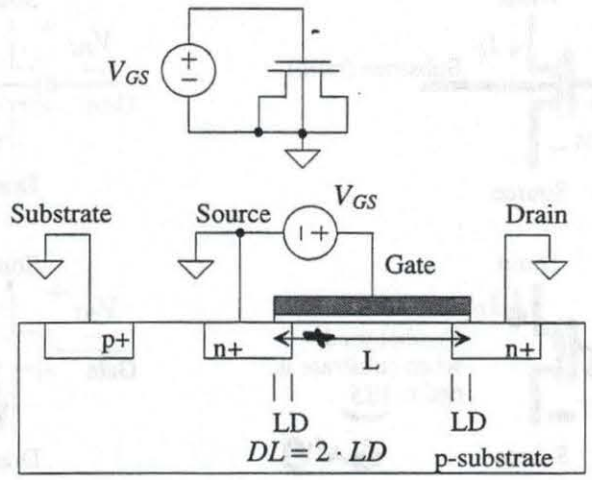


Figure 5.2 Cross-sectional view of MOSFET used to calculate capacitances.

$$= W \cdot L \cdot \frac{\epsilon_{ox}}{t_{ox}} = C_{ox}$$

$$C_{ox}' \quad \frac{F}{m^2}$$

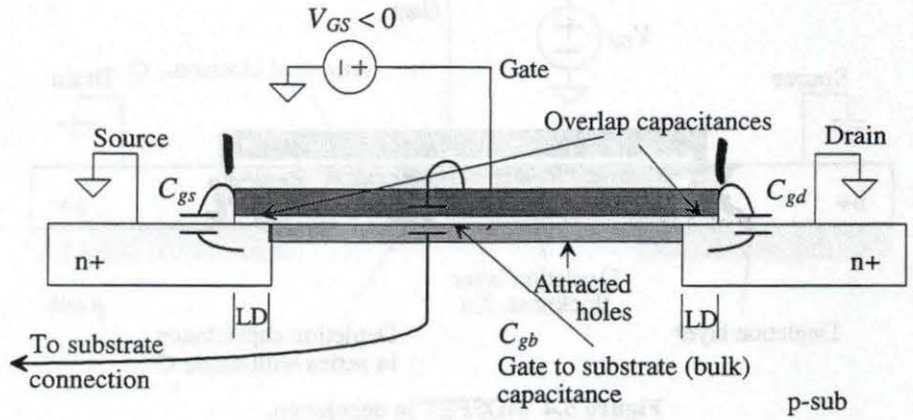
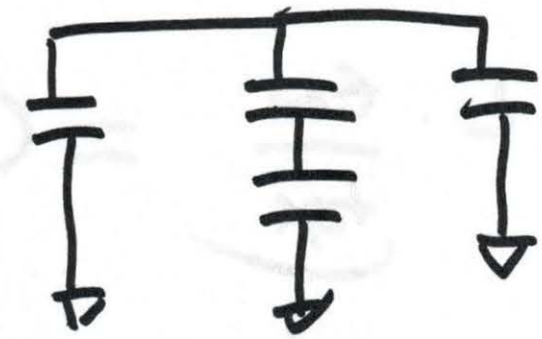


Figure 5.3 MOSFET in accumulation.

$$C_{gs} = C_{gd} = \text{overlap CAP.}$$

$$= \frac{L_D \cdot W \cdot \epsilon_{ox}}{t_{ox}}$$

$$C = \frac{W \cdot (L - 2 \cdot L_D)}{t_{ox}} \cdot \epsilon_{ox}$$



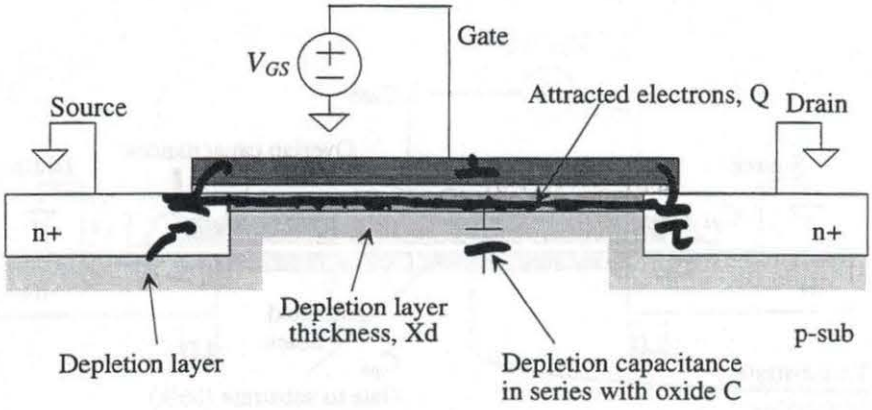
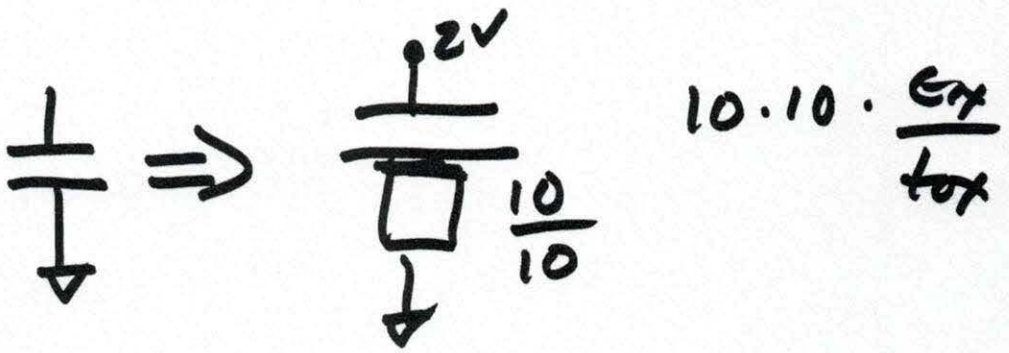


Figure 5.4 MOSFET in depeletion.



$$C_{ox}' = \frac{\varepsilon_x}{t_{ox}}$$

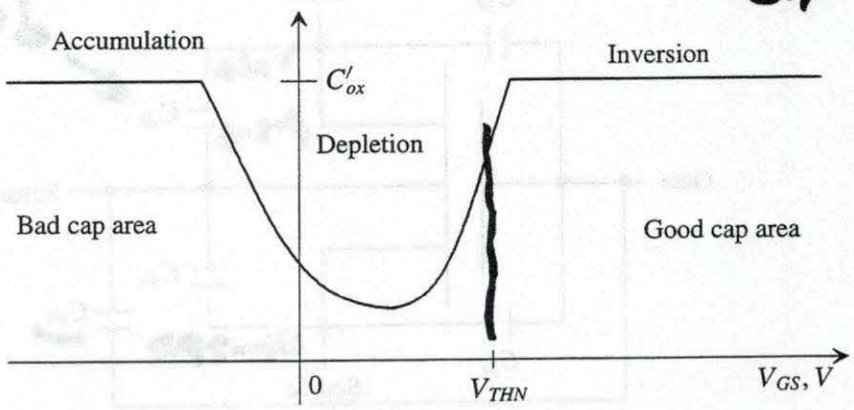
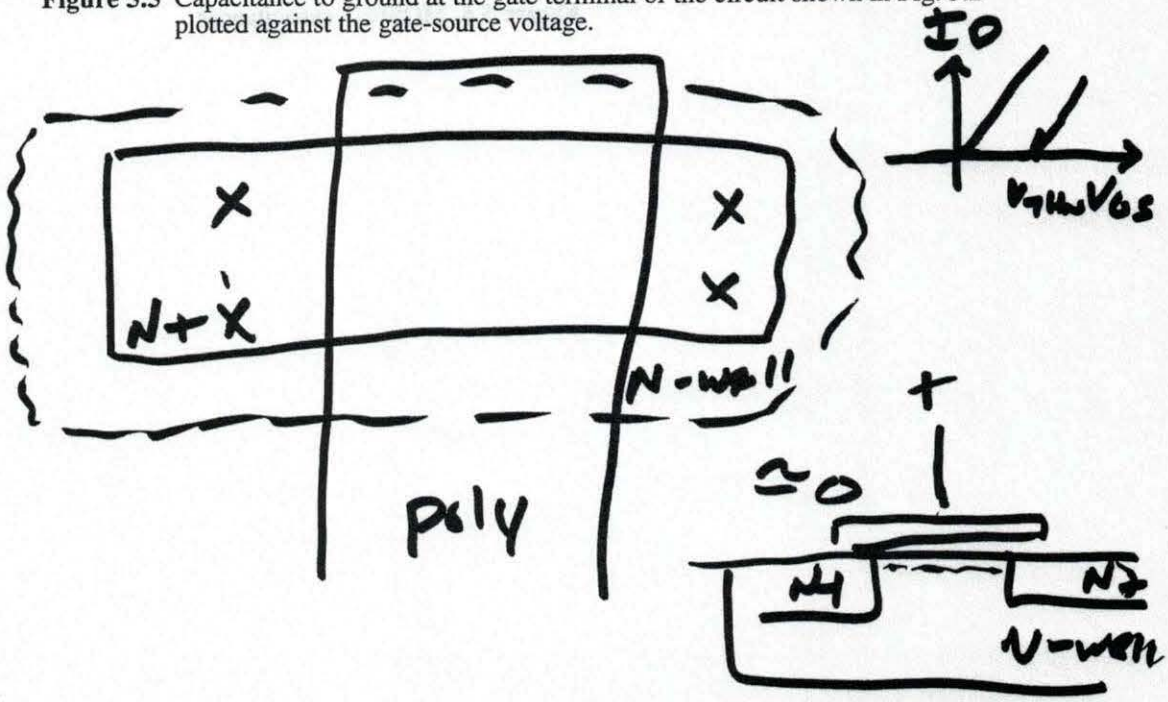


Figure 5.5 Capacitance to ground at the gate terminal of the circuit shown in Fig. 5.2 plotted against the gate-source voltage.



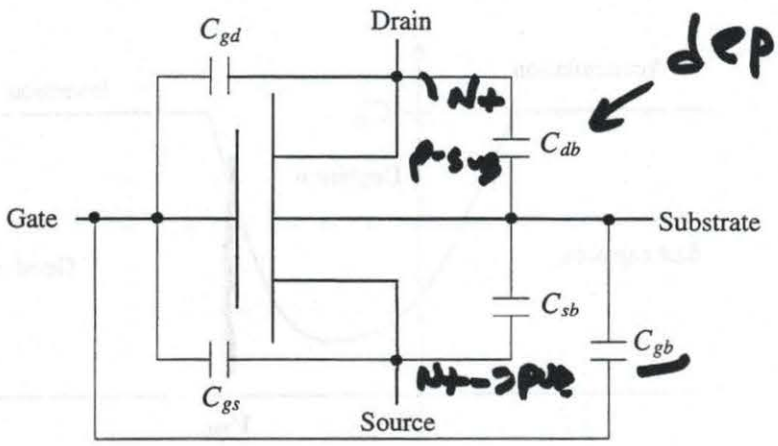
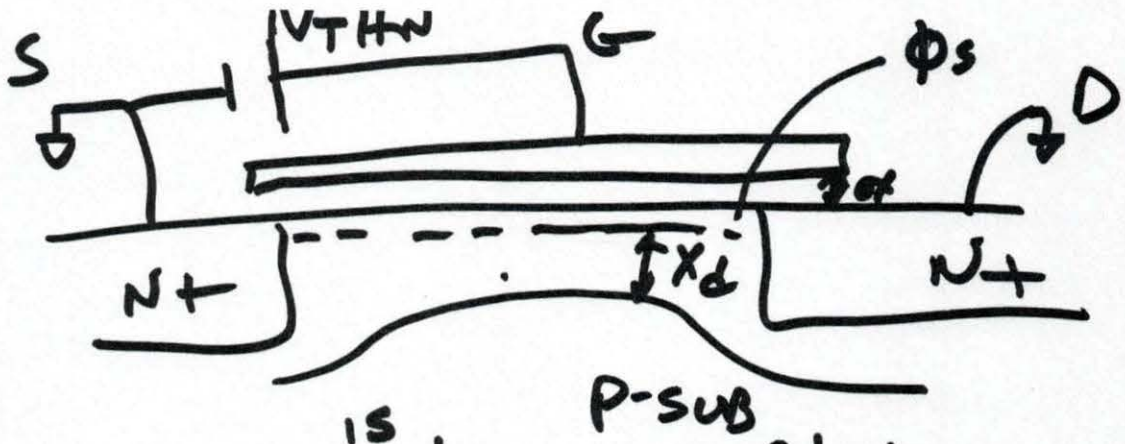


Figure 5.6 MOSFET capacitances.



$N_A = 10^{15} \frac{atoms}{cm^3}$ = # of holes

P-SUB

$$\phi_F = -\frac{KT}{q} \ln \frac{N_A}{N_i}$$

$|2\phi_F|$ $\frac{KT}{q}$ = .026V N_i = 14.5×10^9 carriers/cm³

$$\phi_s\Big|_{V_{THN}} = -\phi_F$$

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Lesson 6:
The MOSFET

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The MOSFET

Hardcopy Visuals

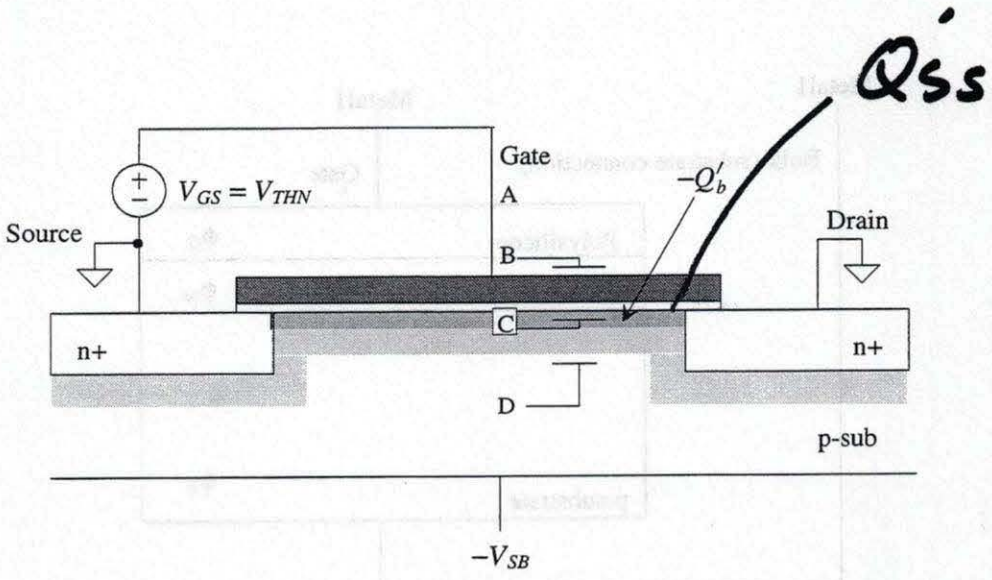


Figure 5.7 Calculation of the threshold voltage.

$$\phi_{ms} = (\phi_G - \phi_{ox}) - (\phi_{ox} - \phi_F)$$

$$= \phi_G - \phi_F$$

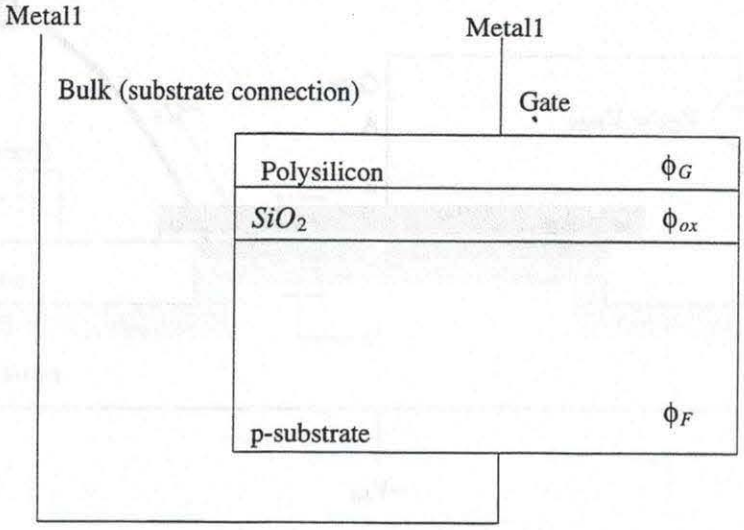
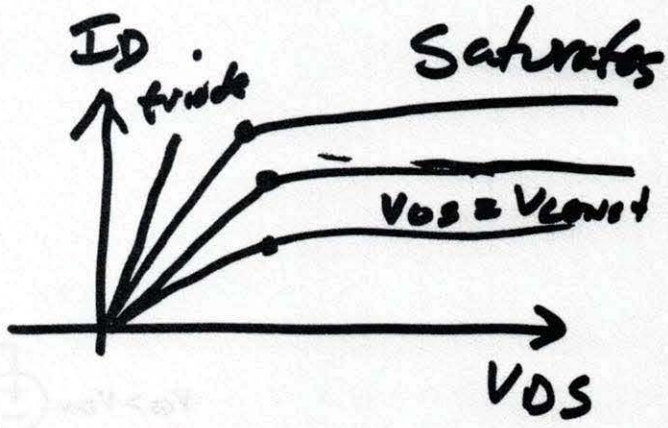


Figure 5.8 Determining the contact potential between poly and substrate.

triode or linear region of operation



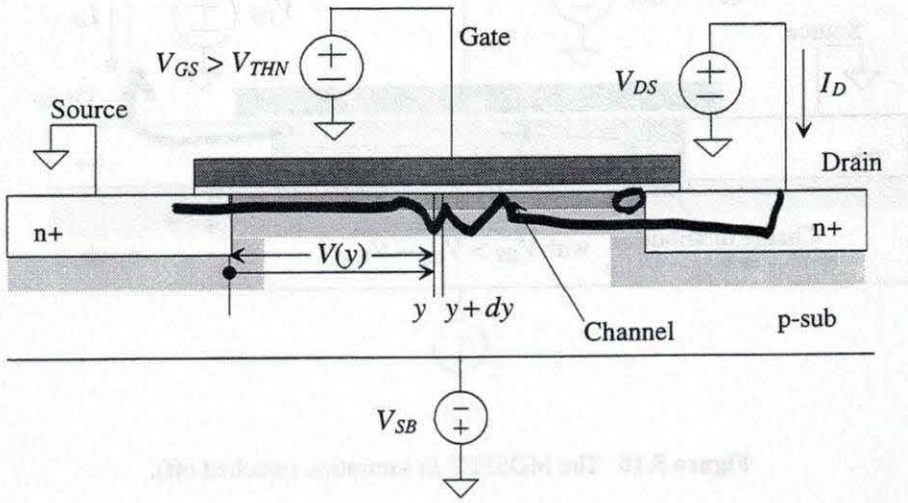


Figure 5.9 Calculation of the large-signal behavior of the MOSFET in the triode (ohmic) region.

$$I_D = K_{PN} \cdot \frac{W}{L}\left[(V_{GS} - V_{THN})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$K_{PN} = \mu_N \cdot C_{ox}'$ $\quad V_{DS} > V_{THN}$

$C_{ox}' = \frac{\varepsilon_{ox}}{t_{ox}}$ $\quad V_{DS} \leq V_{GS} - V_{THN}$

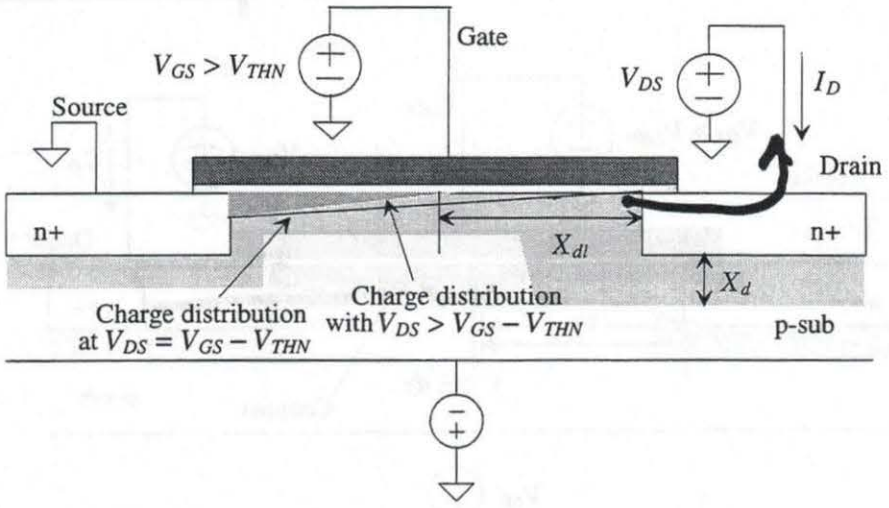


Figure 5.10 The MOSFET in saturation (pinched off).

$$I_D = \frac{KP}{2} \cdot \frac{W}{L} \left(V_{GS} - V_{THN}\right)^2$$

Saturation $V_{GS} > V_{THN}$

$$V_{DS} \geq V_{GS} - V_{THN}$$

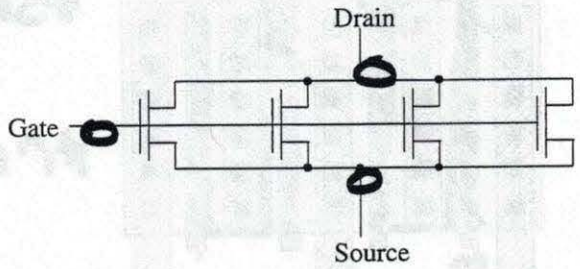


Figure 5.15 Parallel connection of MOSFETs used for layout of a large device.

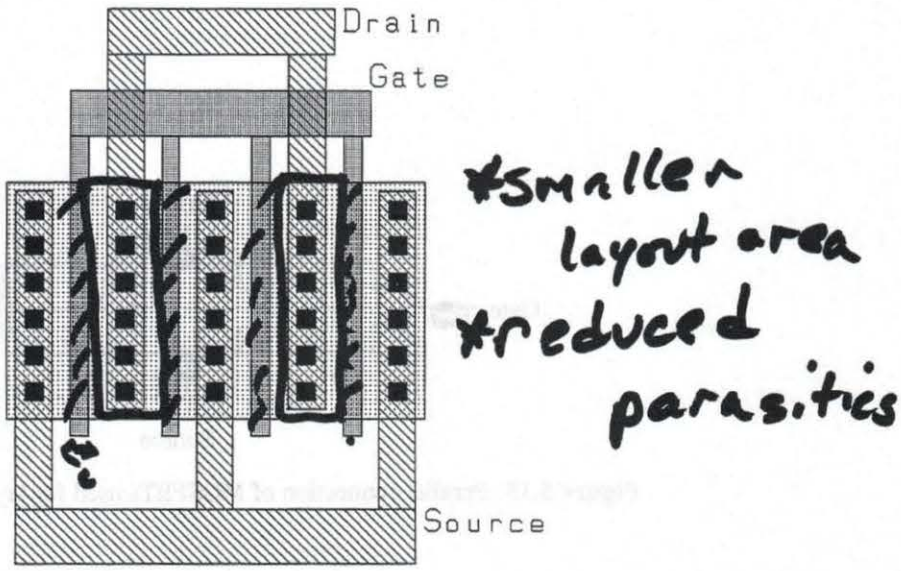


Figure 5.16 Layout of a large (width) MOSFET.

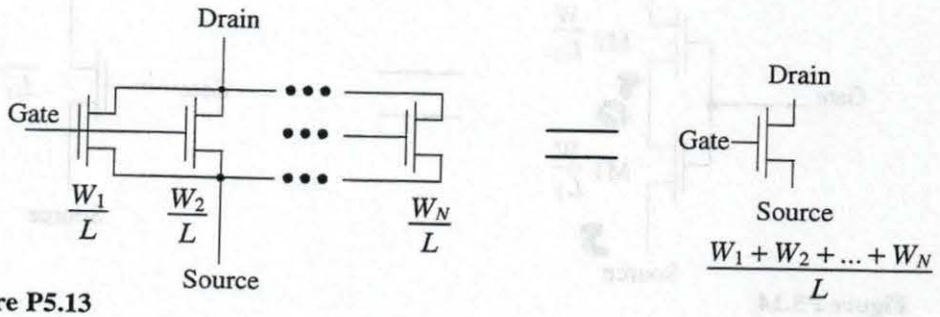


Figure P5.13

$$I_D = \frac{W_1 + W_2 + W_3 \cdots}{L} \left(\quad \right)$$

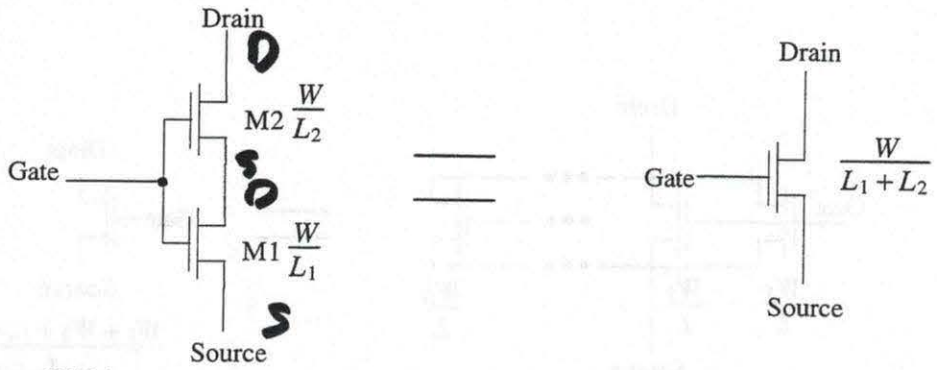
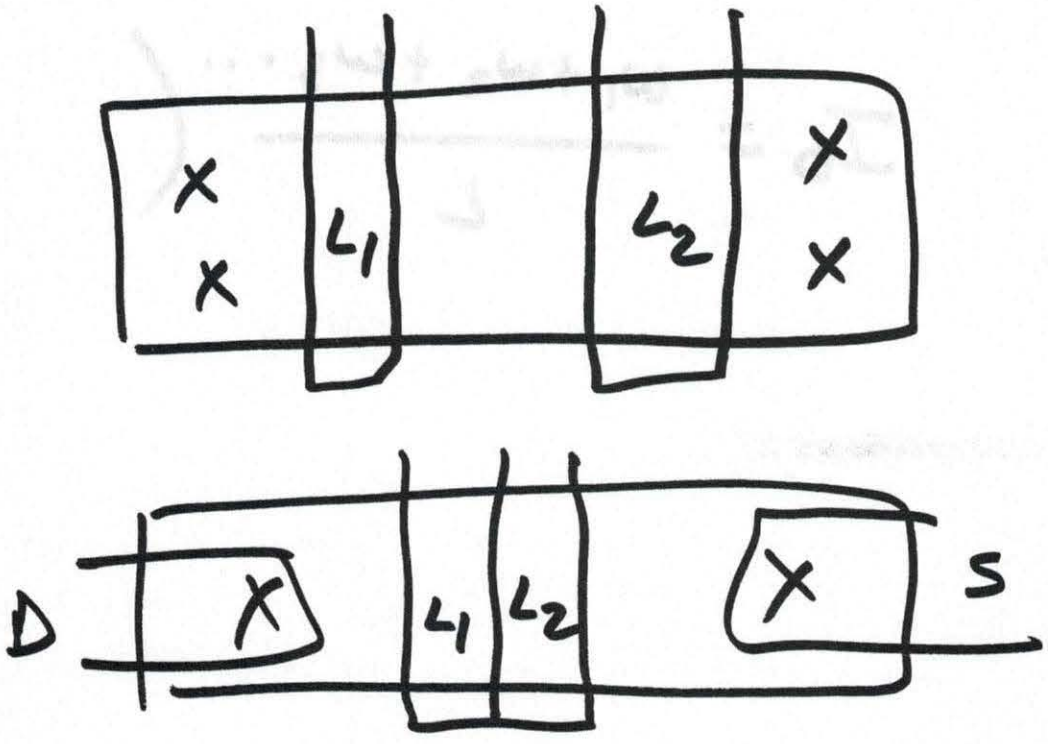

Drain
D
M2 $\frac{W}{L_2}$
Gate
SD
M1 $\frac{W}{L_1}$
S
Source
Drain
Gate
$\frac{W}{L_1+L_2}$
Source

Figure P5.14


X
X
L1
L2
X
X
D
X
L1
L2
X
S

How to make a small $\frac{W}{L}$ MOSFET

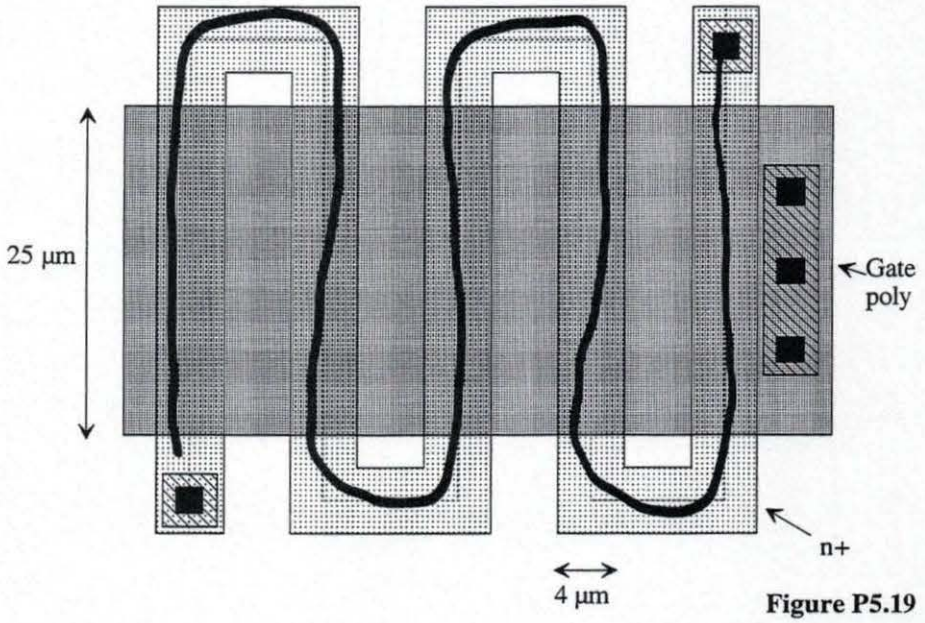


Figure P5.19

$$\frac{W}{L} = \frac{4}{100}$$

CMOS Digital Circuit Design

Lesson 7:
The Short Channel MOSFET

Hardcopy Visuals

CMOS Digital Circuit Design

Lesson 7:
The Short Channel MOSFET

Hardcopy Visuals

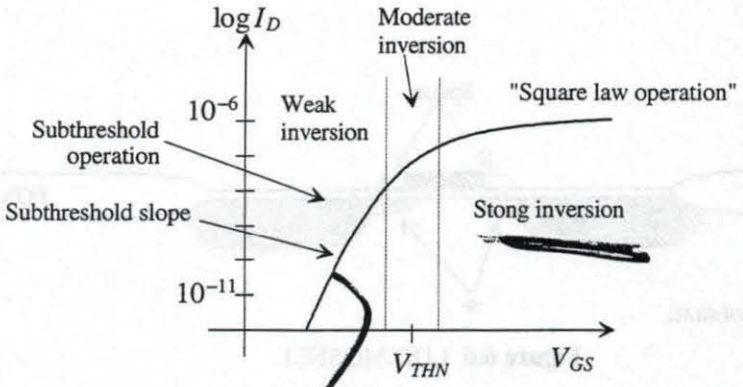


Figure 6.5 Drain current plotted from weak to strong inversion.

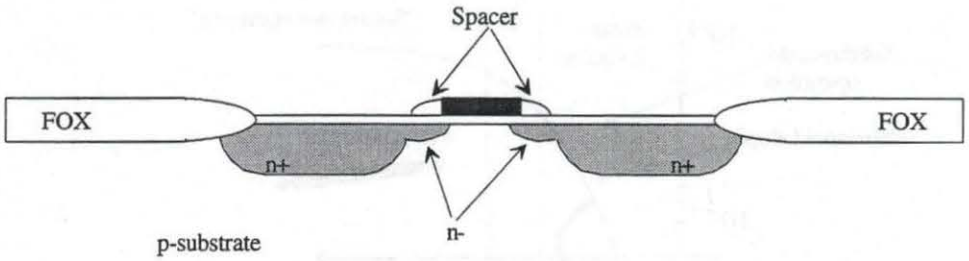


Figure 6.6 LDD MOSFET.

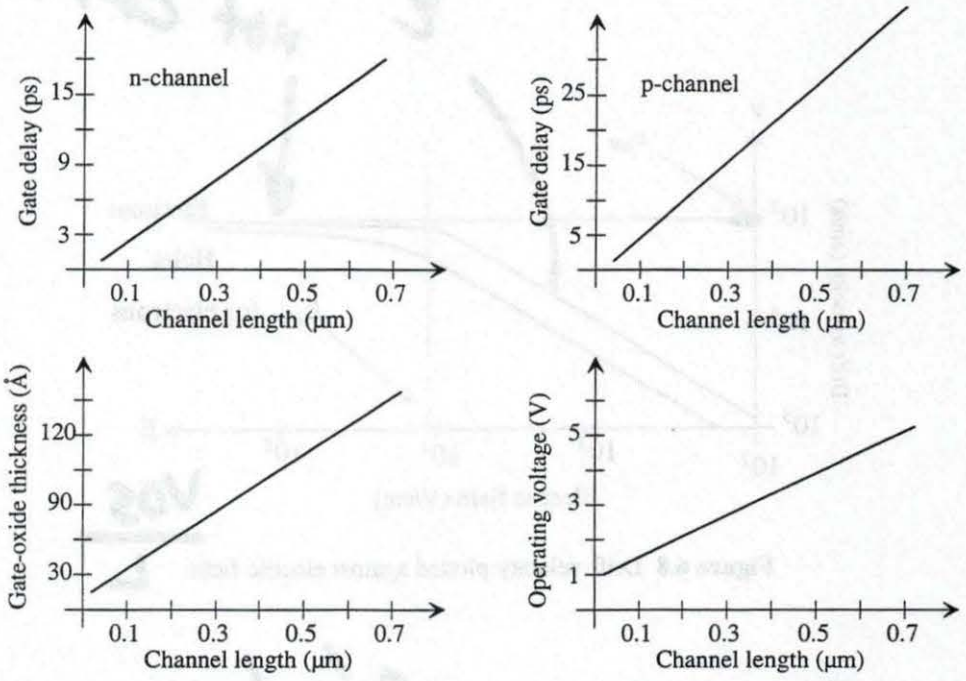
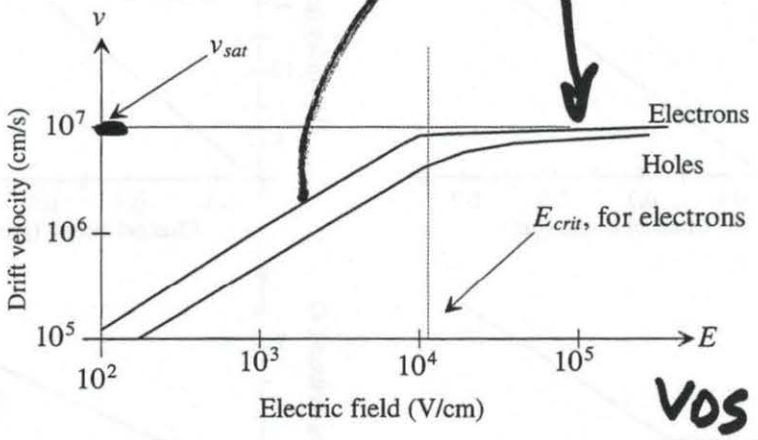


Figure 6.7 Trends in MOS device scaling.



$\frac{v}{\mathcal{E}} = \text{const}$

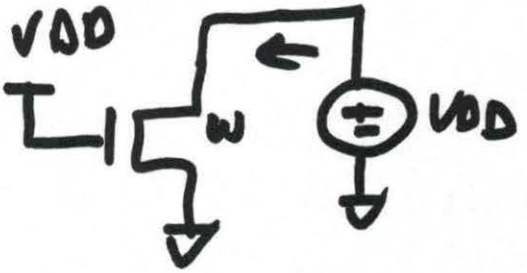
not const.

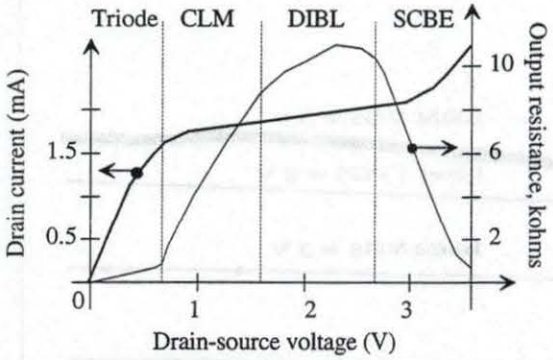
$\frac{V_{OS}}{L}$

Figure 6.8 Drift velocity plotted against electric field.

$$I_D = \frac{W}{} \cdot v_{SAT} \cdot C_{ox}' \left(V_{GS} - V_{THN} - V_{DS_{SAT}} \right)$$

$$I_D = I_{Drive} \cdot W$$





CLM - Channel length modulation dominates output resistance.

DIBL - Drain-induced barrier lowering dominates output resistance.

SCBE - Substrate current -induced body effect dominates output resistance.

Figure 6.9 Characteristics of a MOSFET with W/L = 10 μm / 0.43 μm and TOX = 75 Å [8].

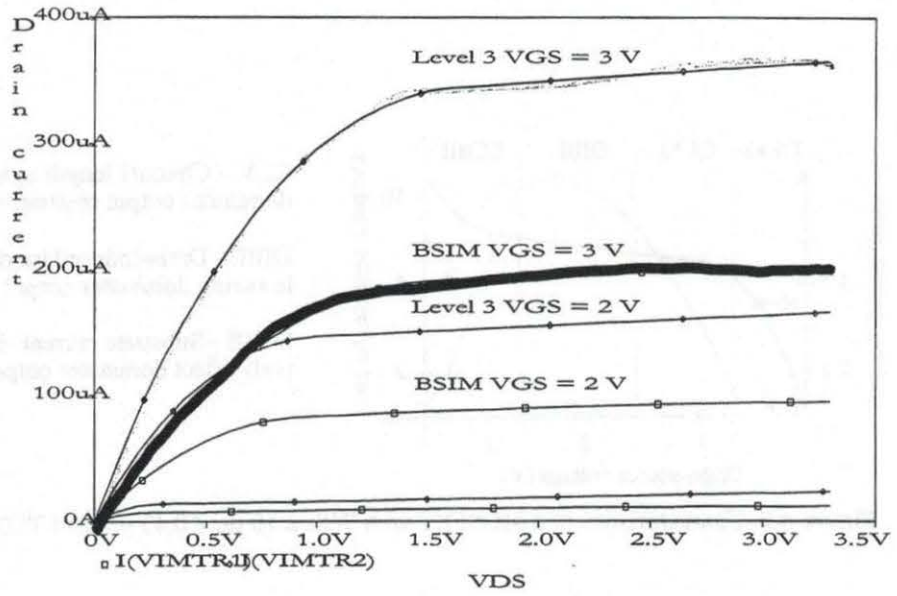


Figure C.1 Curves for a 0.9/0.6 n-channel MOSFET fabricated in CMOS14TB.

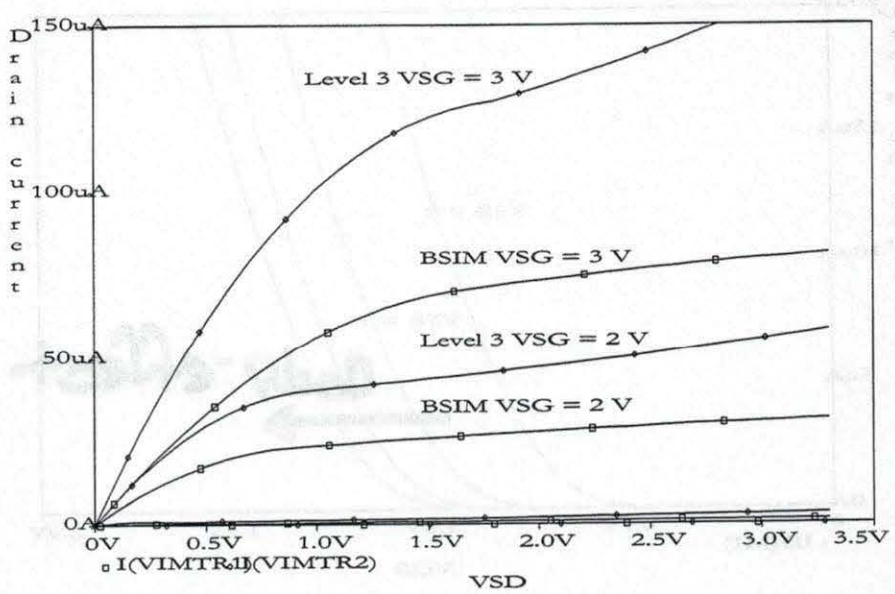


Figure C.2 Curves for a 0.9/0.6 p-channel MOSFET fabricated in CMOS14TB.

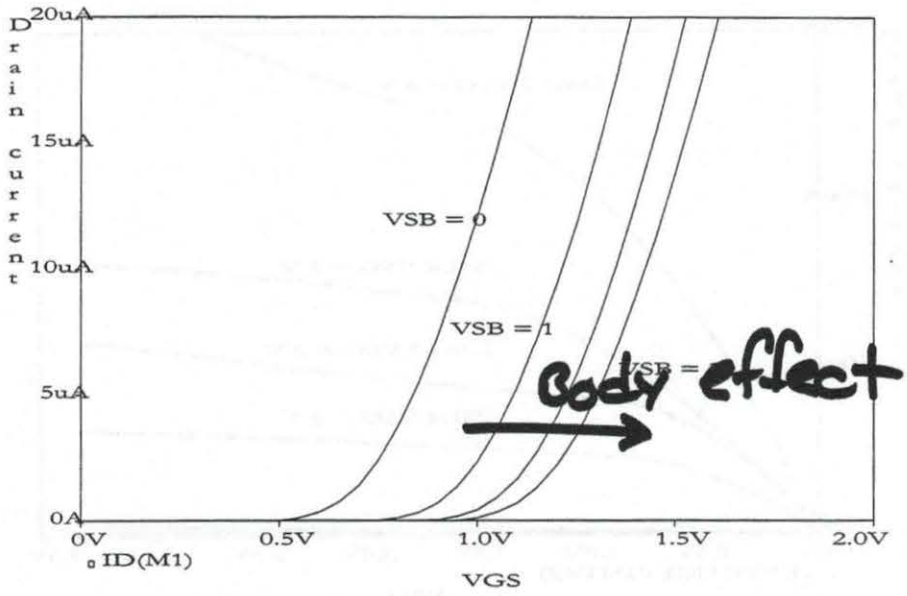


Figure C.3 Curves for a 0.9/0.6 n-channel MOSFET fabricated in the CMOS14TB process.

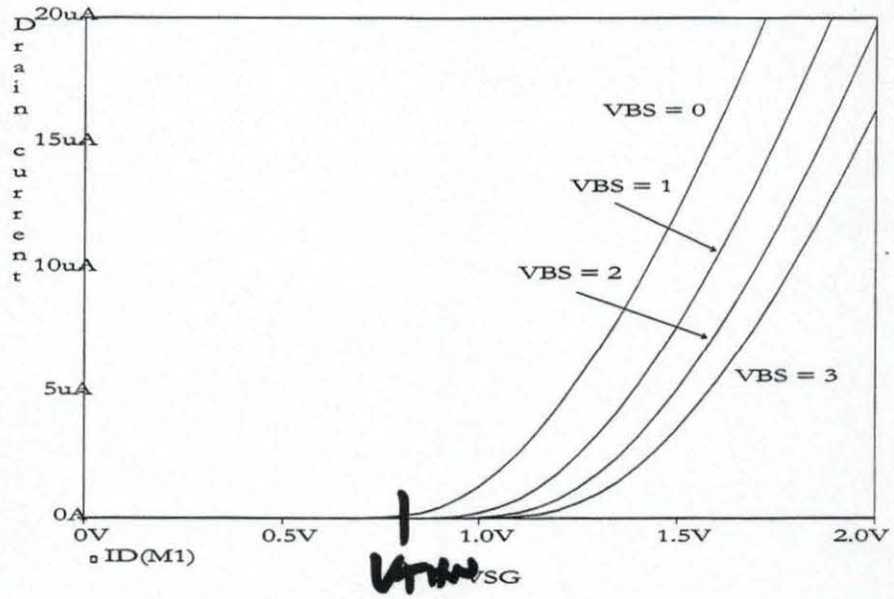


Figure C.4 Curves for a 0.9/0.6 p-channel MOSFET fabricated in the CMOS14TB process.

CMOS Digital Circuit Design

Lesson 8:
The Digital Model of a MOSFET

Hardcopy Visuals

CMOS Digital Circuit Design

Lesson 8:
The Digital Model of a MOSFET

Hardcopy Visuals

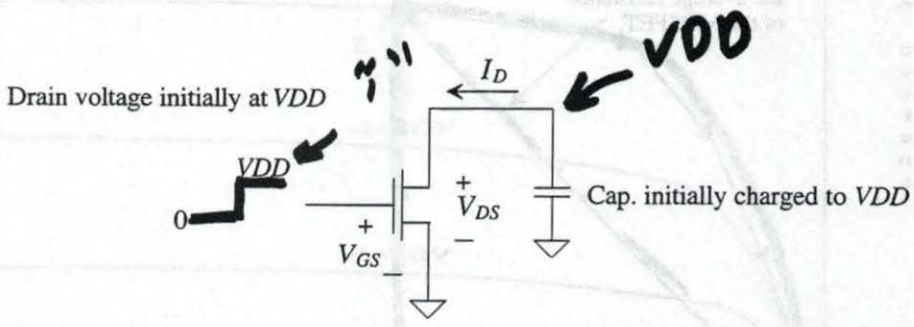
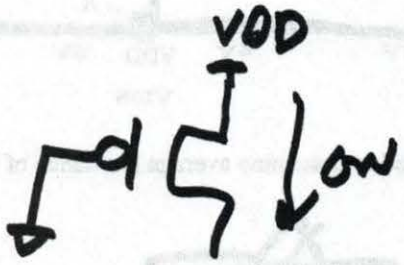


Figure 10.1 MOSFET switching circuit.



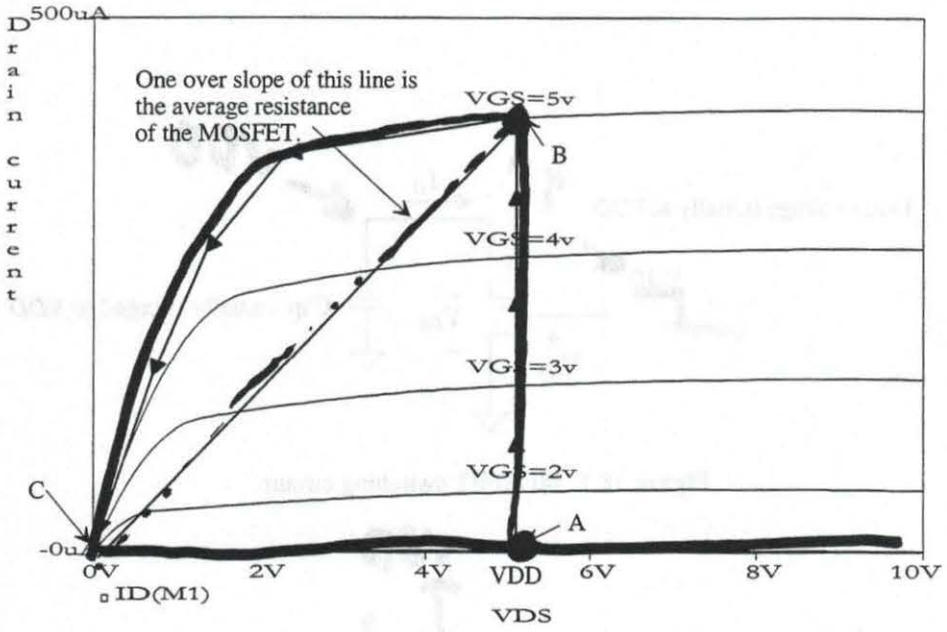
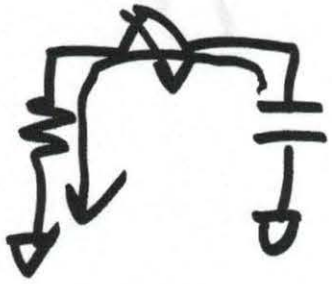


Figure 10.2 Diagram used to determine average resistance of a MOSFET during switching.



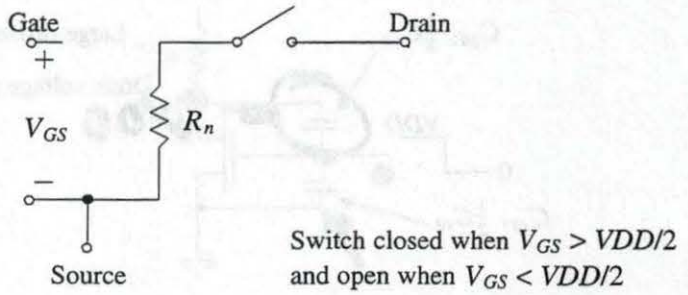


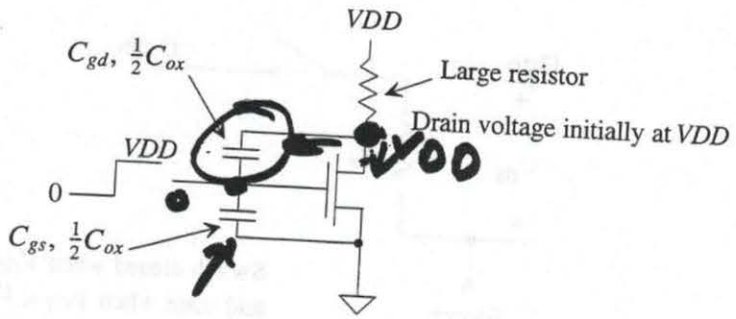
Figure 10.3 Simple digital MOSFET model.

$$R_N = \frac{VDD}{\frac{KP}{2}\frac{W}{L}(VDD - V_{THN})^2}$$

$$R_N = R_N' \cdot \frac{L}{W} = \underline{\underline{12k \cdot \frac{L}{W}}}$$

$$R_P' = 36k$$

$$R_P = R_P' \cdot \frac{L}{W}$$

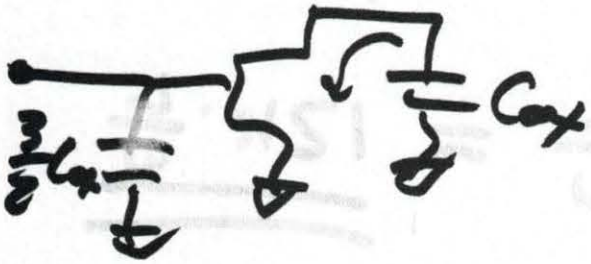


$CV = Q$

Figure 10.4 MOSFET switching circuit with capacitances.

$$VDD \cdot \frac{1}{2}C_{ox} + \frac{1}{2}C_{ox} \cdot 2VDD$$

$$VDD \cdot \frac{3}{2}C_{ox} = C_{INV}$$



$$C_{OUT} = C_{ox}$$

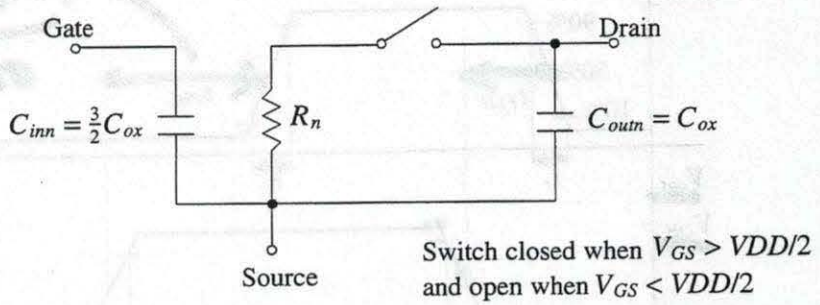


Figure 10.5 Simple digital MOSFET model.

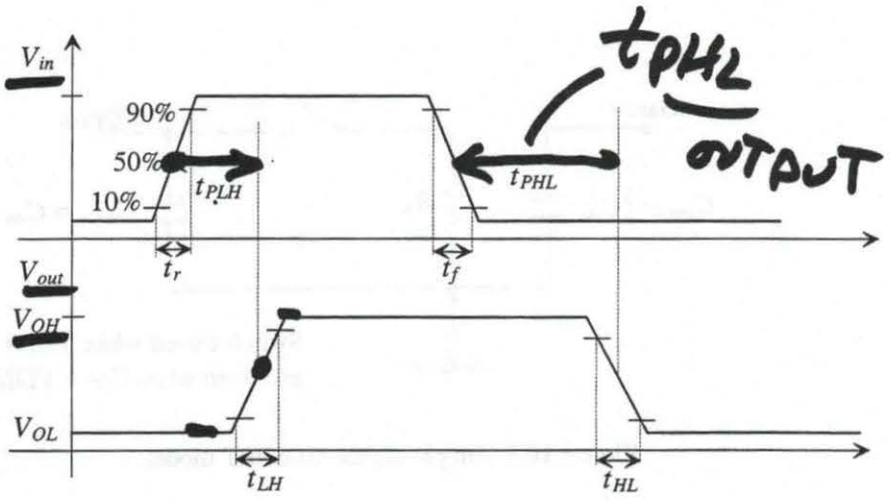


Figure 10.6 Definition of delays and transition times.

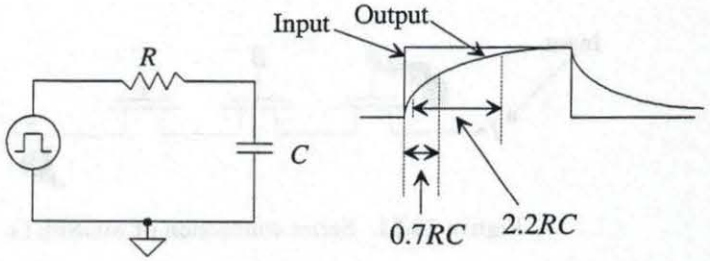


Figure 10.7 Delay- and risetime for a simple RC circuit.

$t_{delay} \simeq RC$

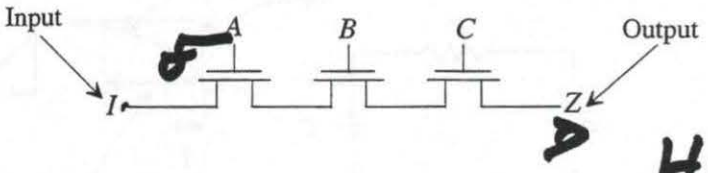


Figure 10.11 Series connection of MOSFETs.

Hi-Z
tri-state

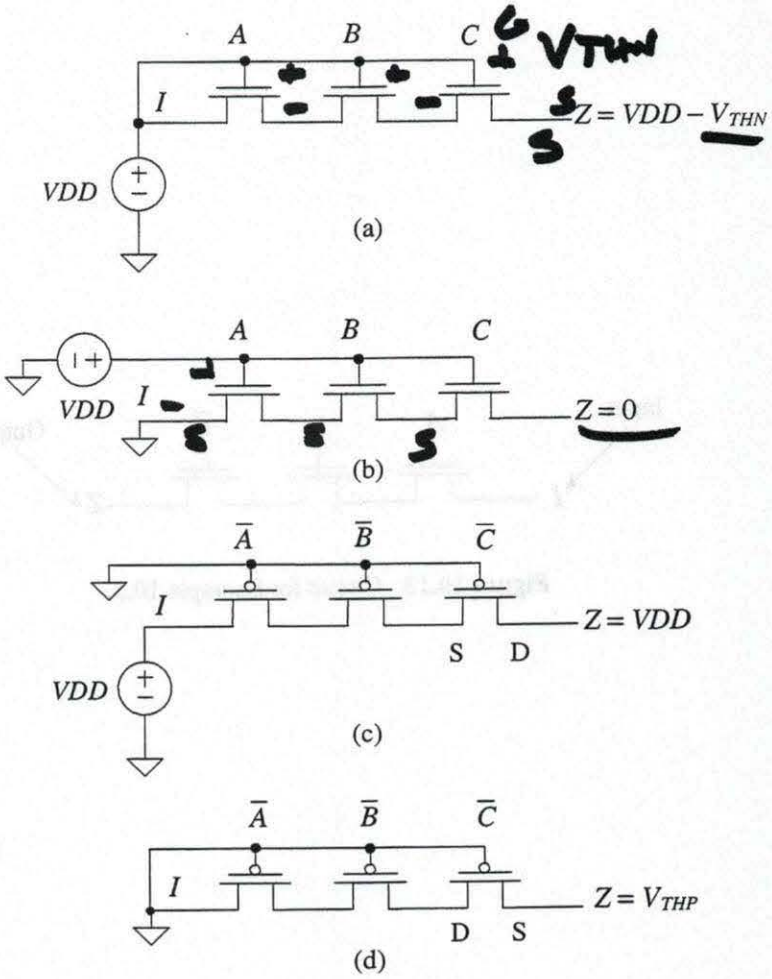


Figure 10.12 DC operation of series-connected MOSFETs.

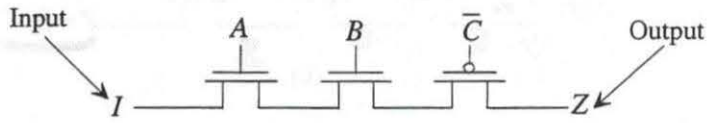


Figure 10.13 Circuit for Example 10.3.

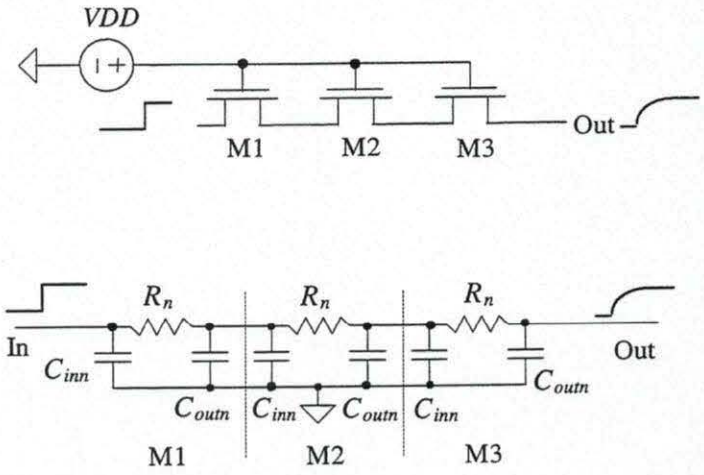


Figure 10.14 Modeling delay through series-connected MOSFETs.

CMOS Digital Circuit Design

Lesson 9:
Inverter Operation I

Hardcopy Visuals

CMOS Digital Circuit Design

Lesson 9:
Inverter Operation I

Hardcopy Visuals

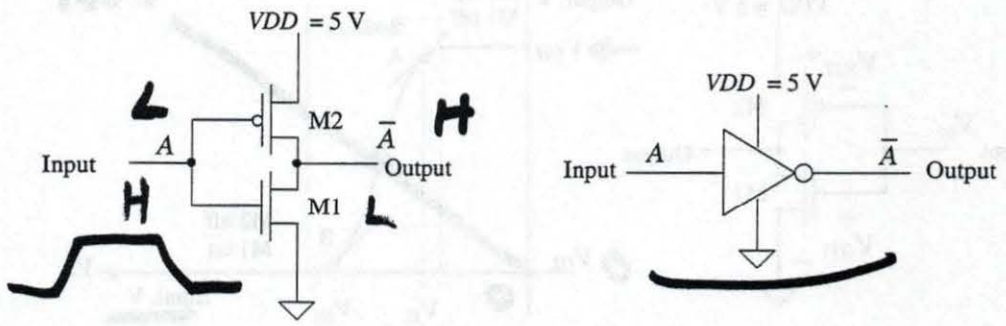


Figure 11.1 The CMOS inverter, schematic, and logic symbol.

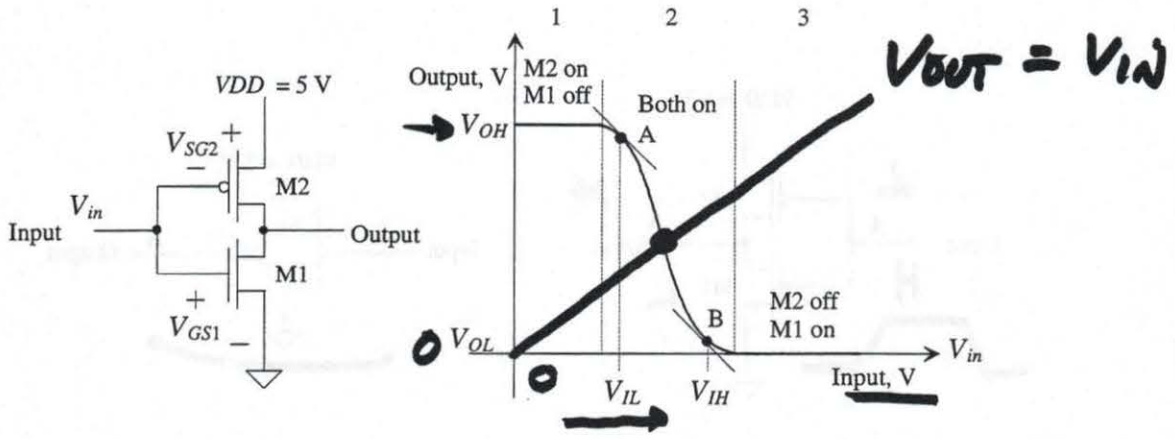
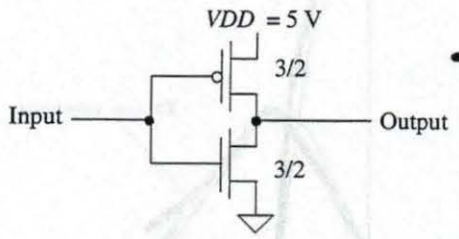


Figure 11.2 The CMOS inverter transfer characteristics.



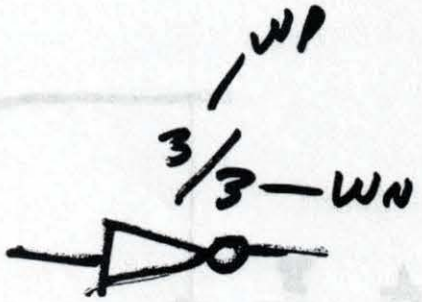


Figure Ex11.1

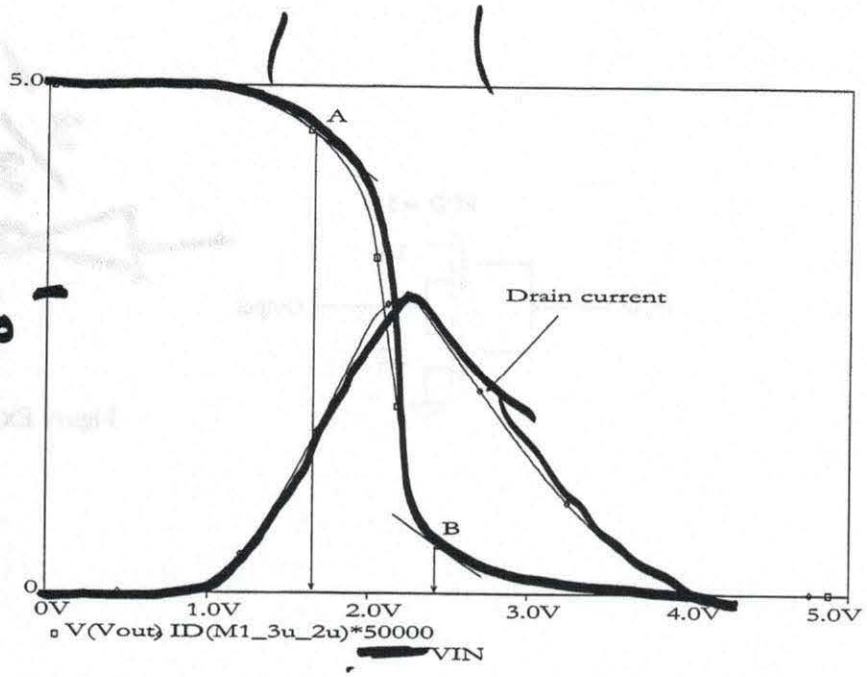


Figure 11.3 Transfer characteristics of a minimum-size inverter used in Example 11.1.

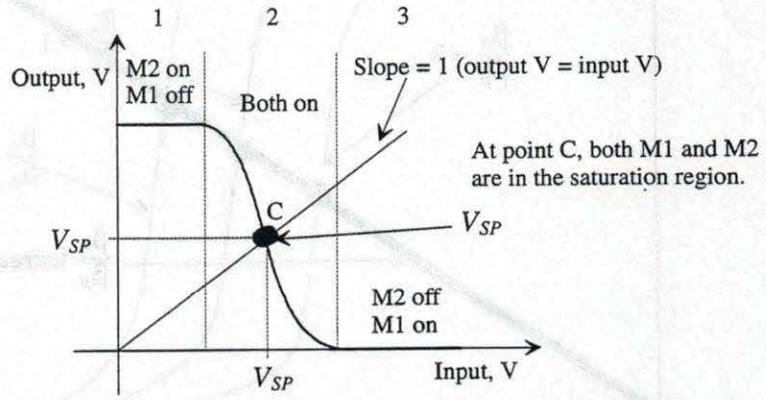
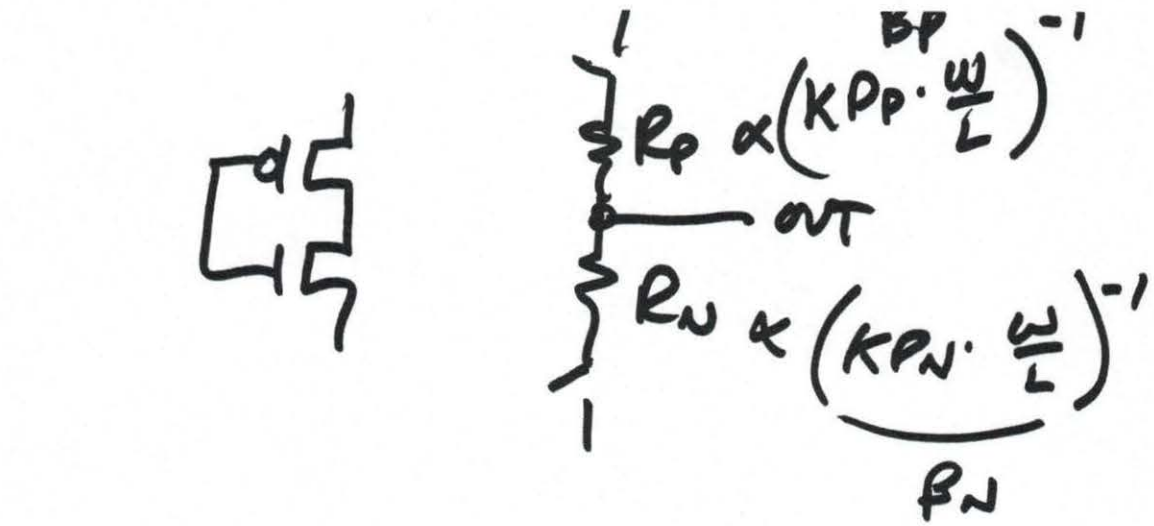


Figure 11.4 Transfer characteristics of the inverter showing the switching point.



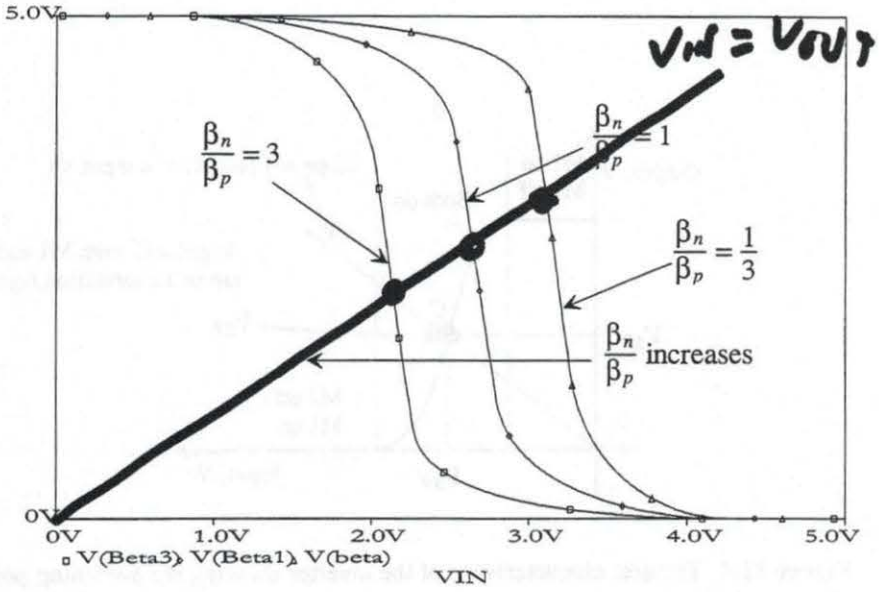


Figure 11.5 Sizing of the CMOS inverter.

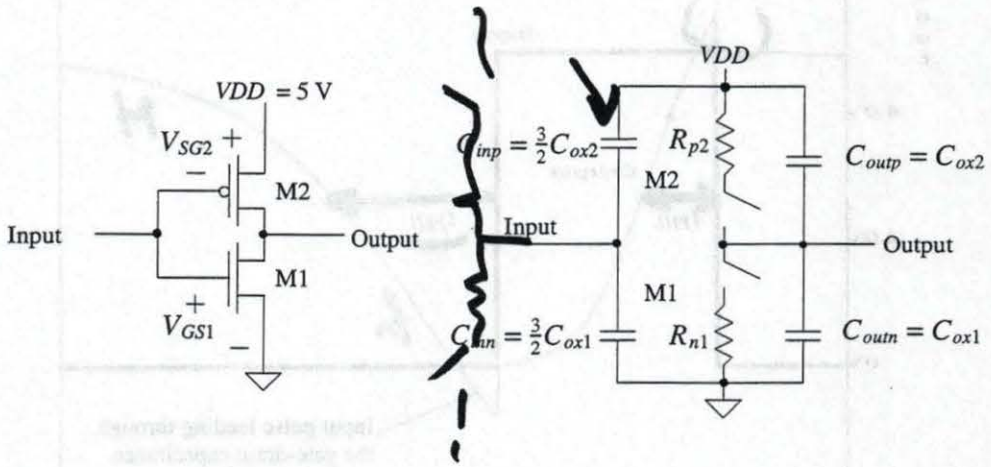


Figure 11.6 The CMOS inverter switching characteristics using the digital model.

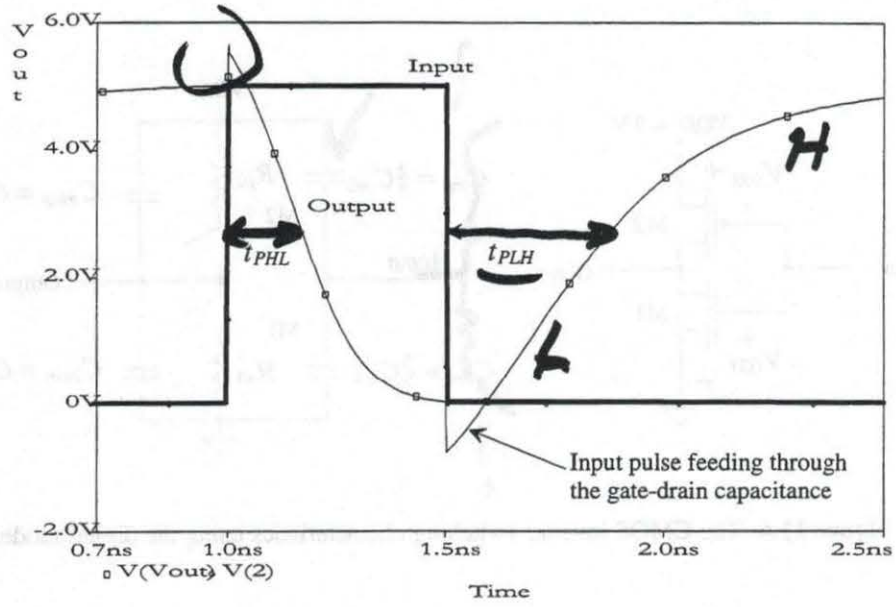


Figure 11.7 Intrinsic inverter delay.

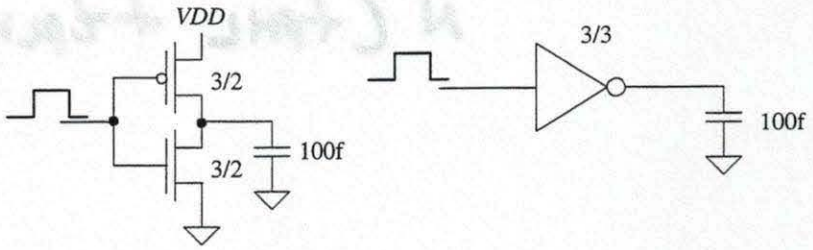


Figure 11.8 Inverter driving a 100 fF load capacitance in Ex. 11.6.

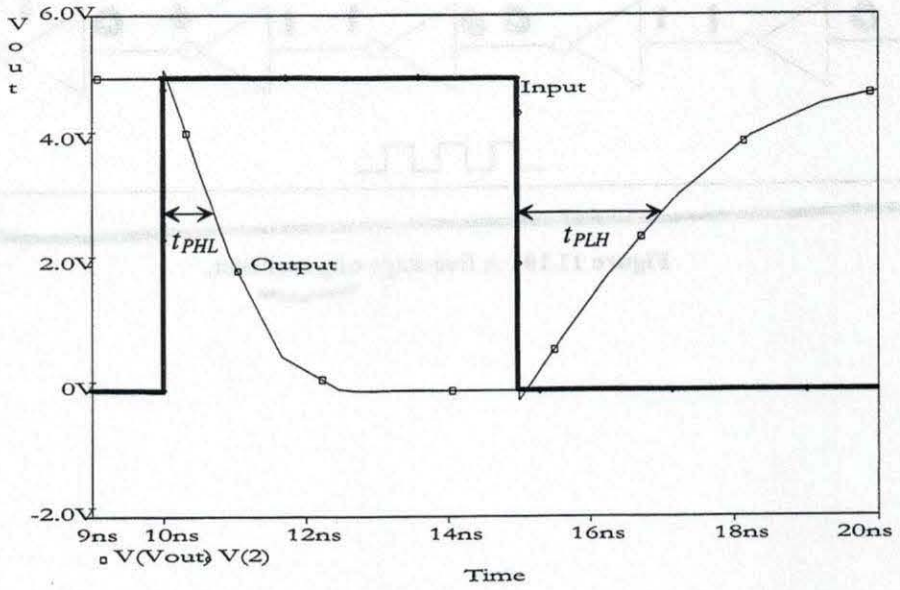


Figure 11.9 Simulation results of minimum-size inverter driving 100 fF.

$$\frac{1}{N(t_{PHL} + t_{PLH})} = f_{OSC}$$

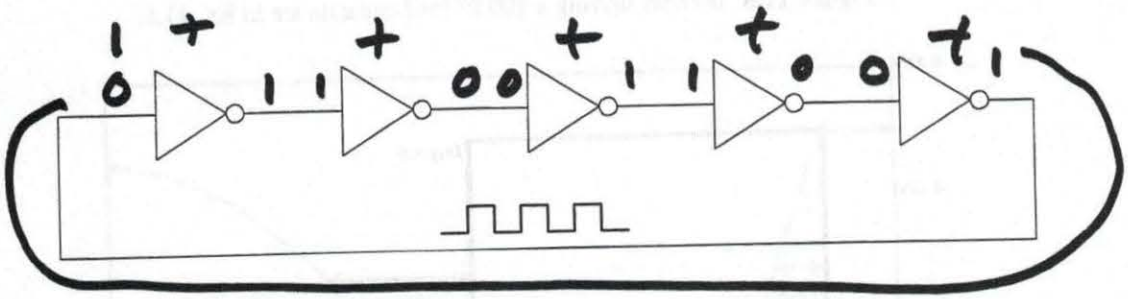


Figure 11.10 A five-stage ring oscillator.

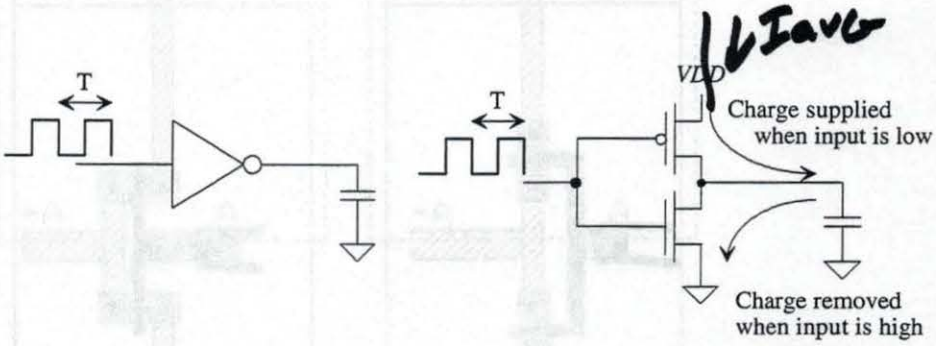


Figure 11.11 Dynamic power dissipation of the CMOS inverter.

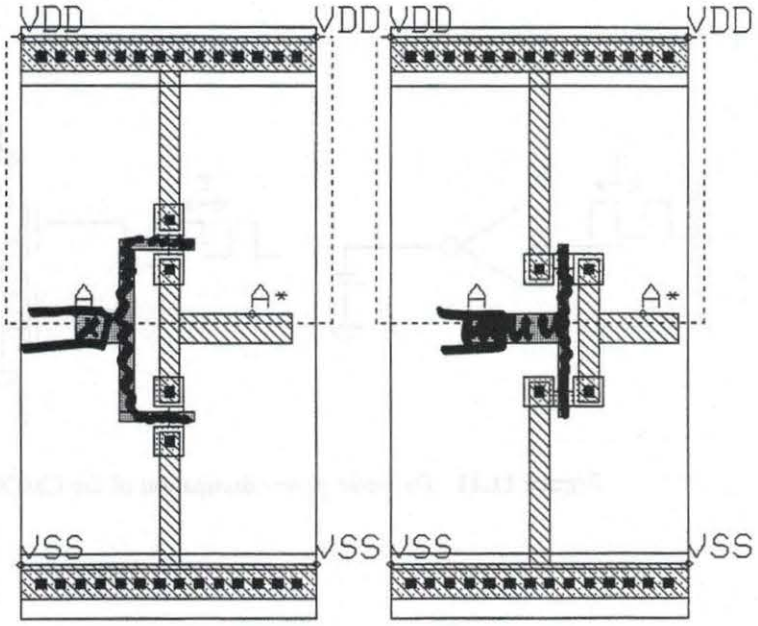


Figure 11.13 Two inverter layout styles.

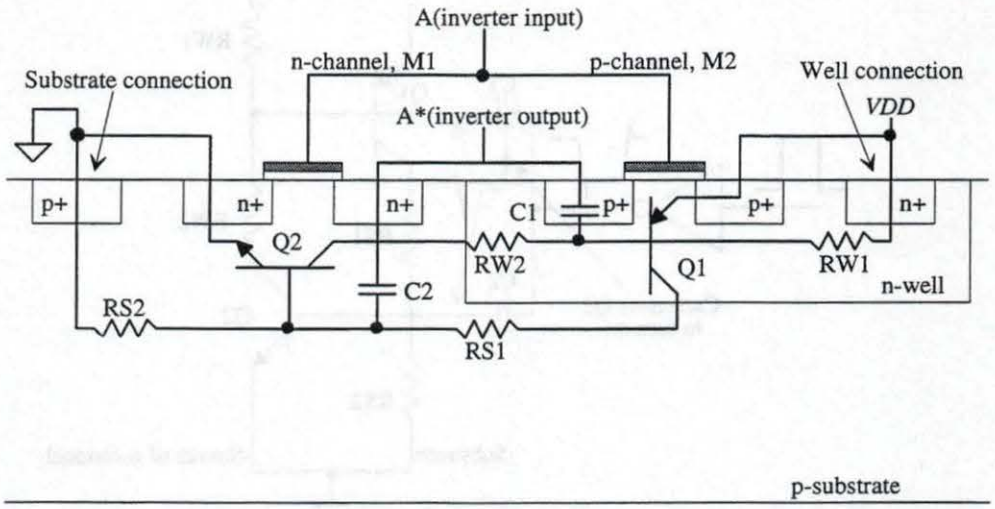


Figure 11.14 Cross-sectional view of an inverter showing parasitic bipolar transistors and resistors.

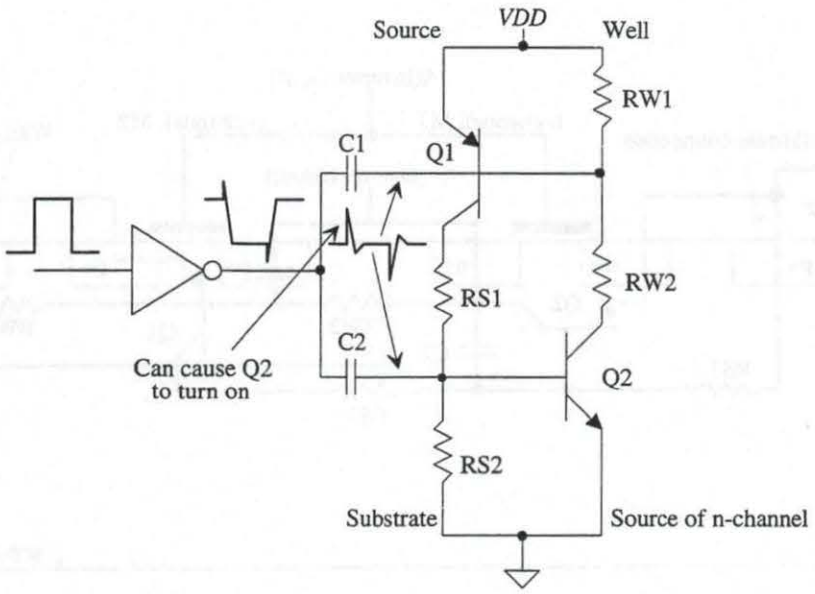


Figure 11.15 Schematic used to describe latch-up.

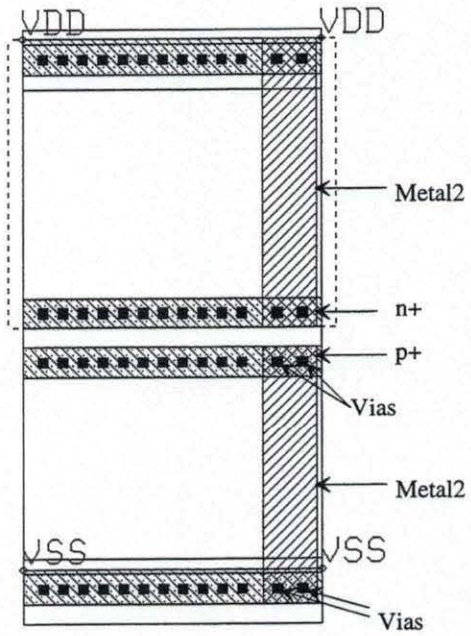


Figure 11.16 Alternative standard-cell frame used for better latch-up protection.

CMOS Digital Circuit Design

Lesson 10:
Inverter Operation II

Hardcopy Visuals

CMOS Digital Circuit Design

Lesson 10:
Inverter Operation II

Hardcopy Visuals

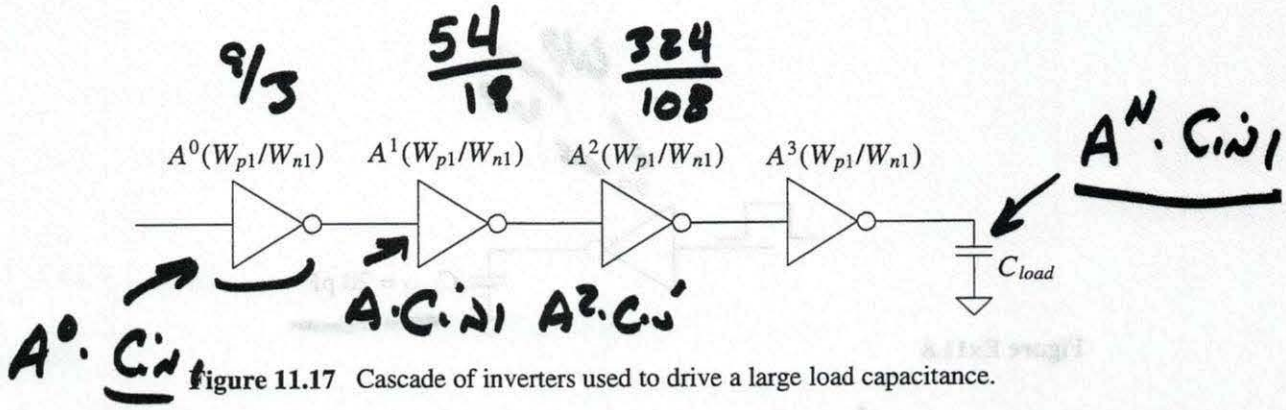


Figure 11.17 Cascade of inverters used to drive a large load capacitance.

$$N = \ln \frac{C_{load}}{C_{in1}}$$

$$A = \left[\frac{C_{load}}{C_{in1}}\right]^{1/N}$$

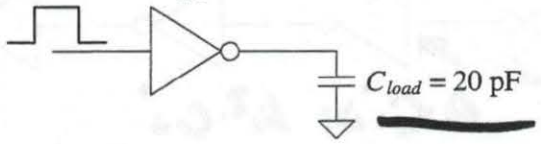


Figure Ex11.8

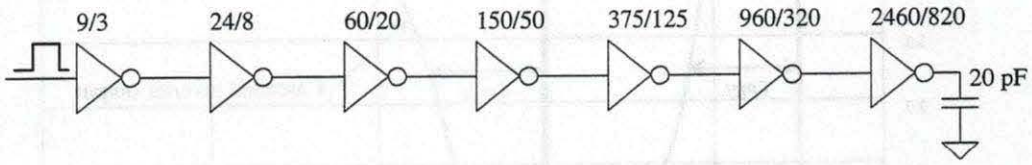


Figure 11.18 Buffer designed in Ex. 11.8.

$$t_{pHL} = t_{pLH} = \underline{5.2\,ns}$$

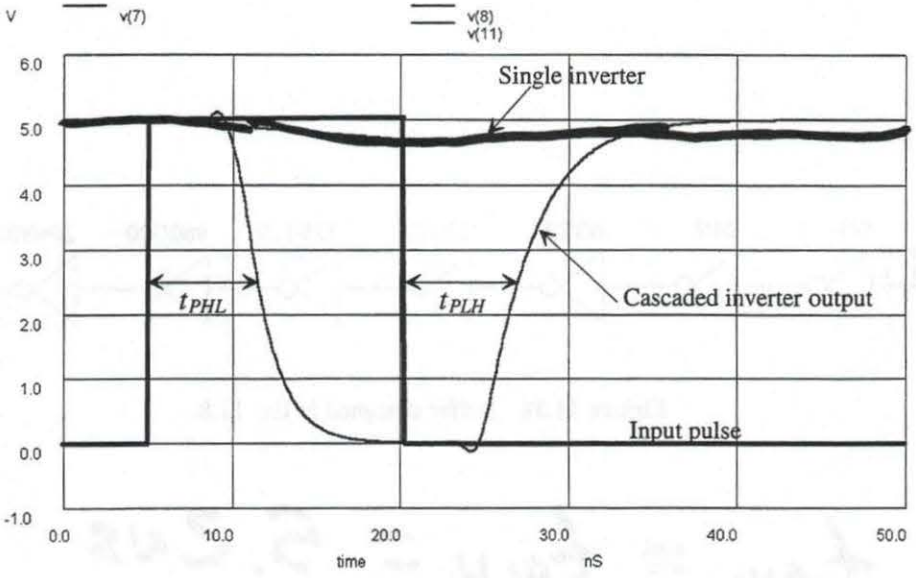


Figure 11.19 Simulation results from Ex. 11.8.

Example 11.9

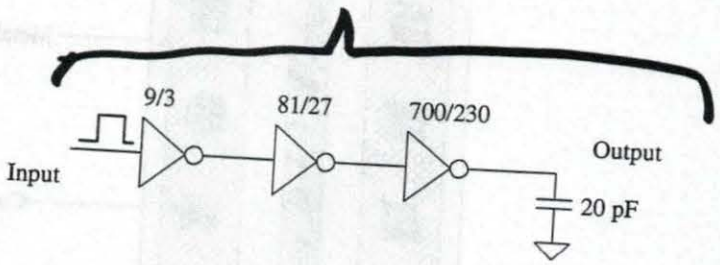


Figure 11.20 Buffer design of Ex. 11.9.

13.2ns

3ns more

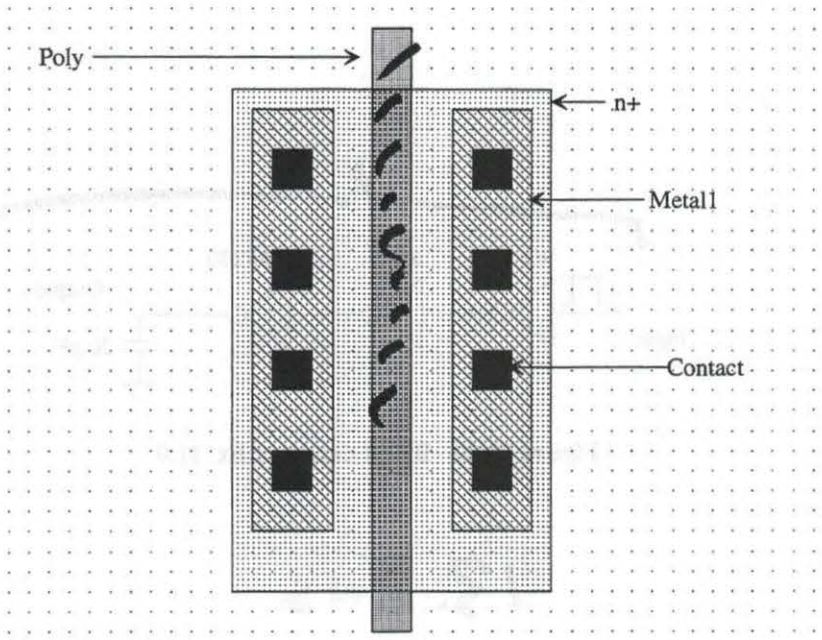


Figure 11.21 Layout of an n-channel MOSFET measuring 25 μm (width) by 2 μm (length).

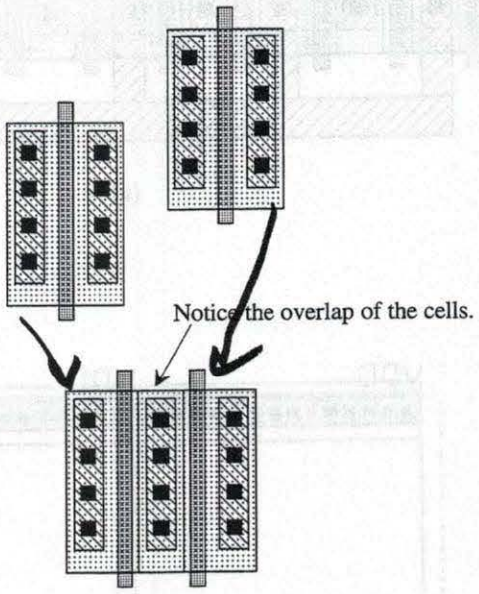
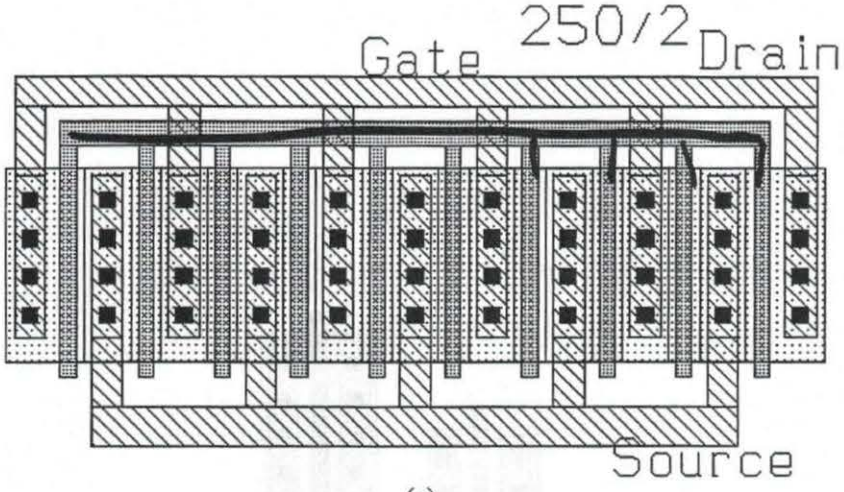
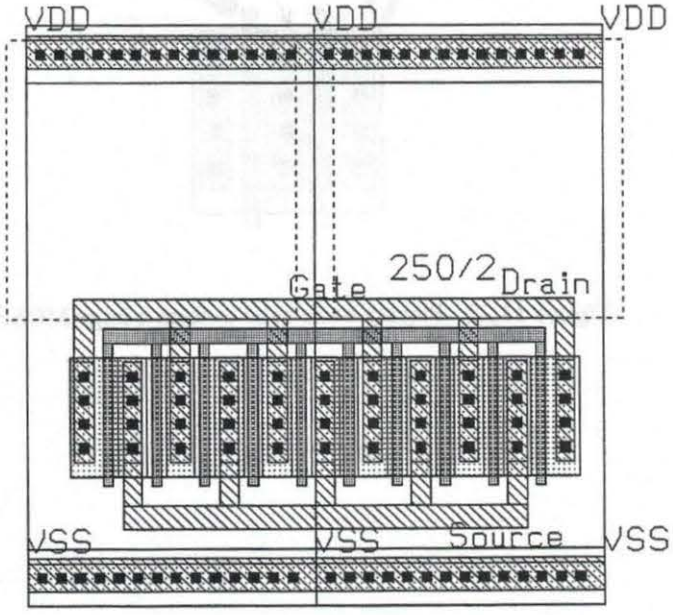


Figure 11.22 Placing basic cells to form a large MOSFET.



(a)



(b)

Figure 11.23 (a) Layout of a 250 by 2 n-channel MOSFET and (b) using a standard-cell frame.

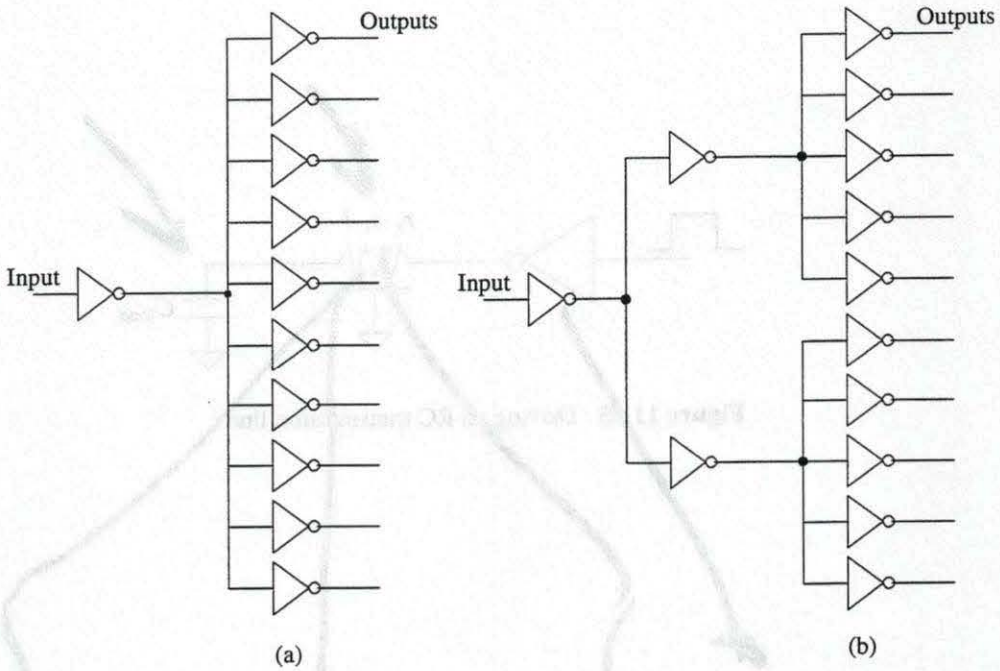


Figure 11.24 Distributed drivers.

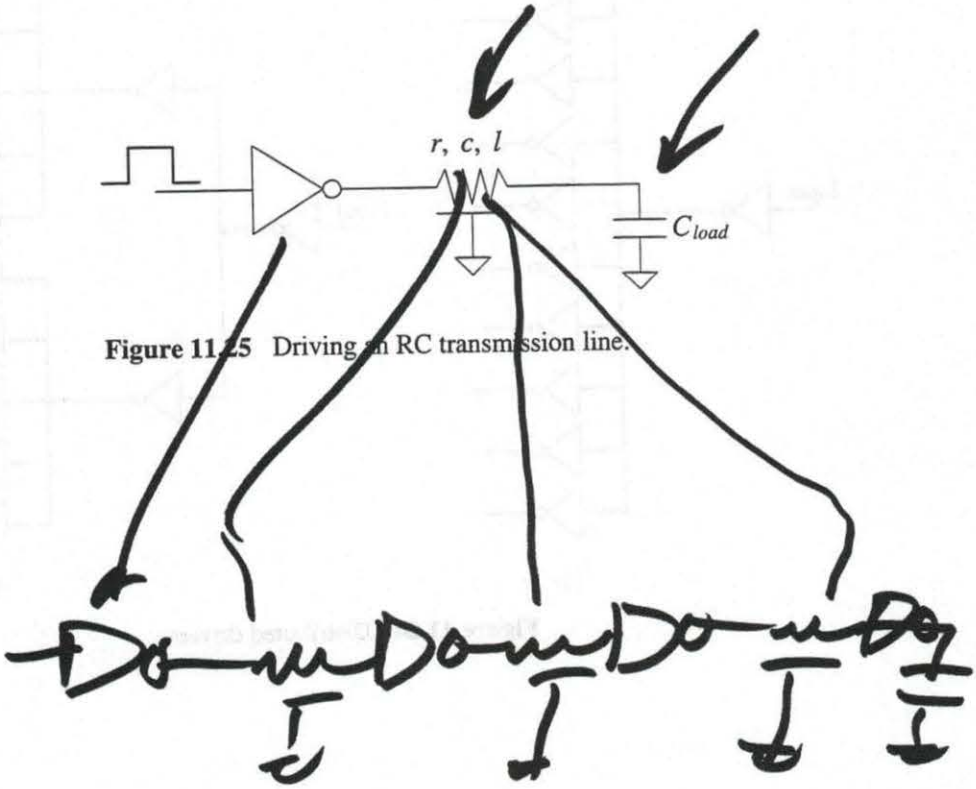


Figure 11.25 Driving an RC transmission line.

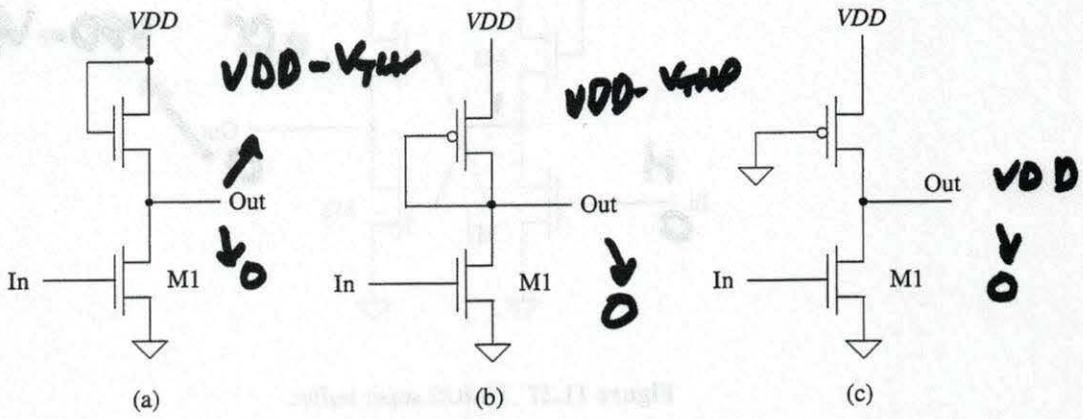


Figure 11.26 Other inverter configurations.

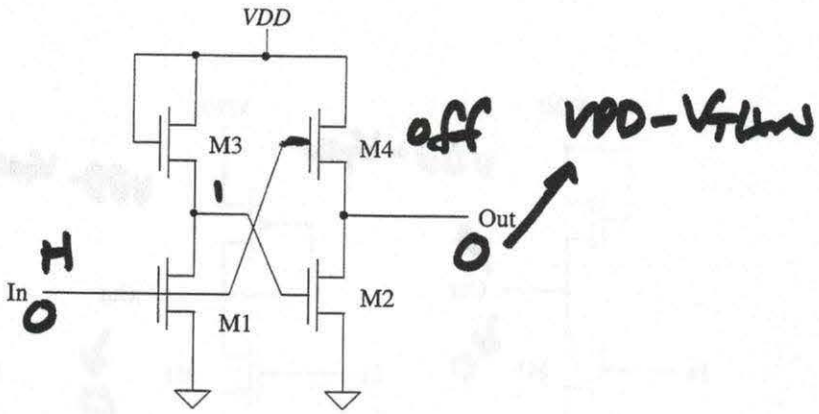


Figure 11.27 NMOS super buffer.

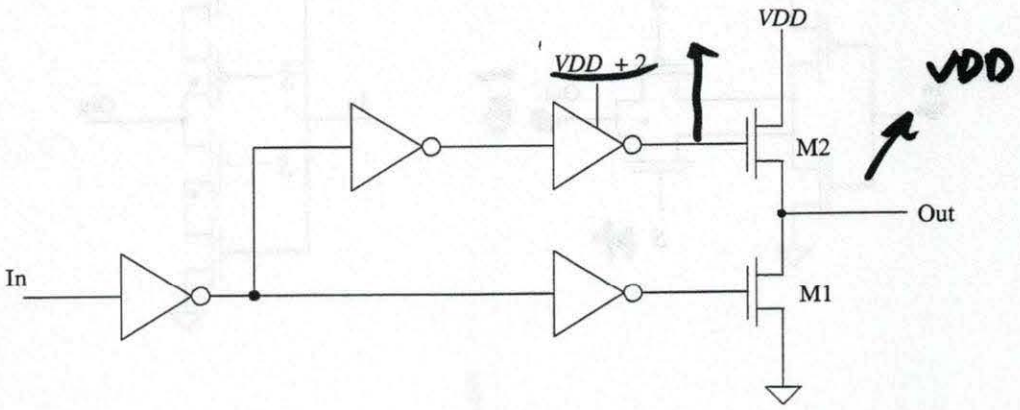


Figure 11.28 Alternative output buffer.

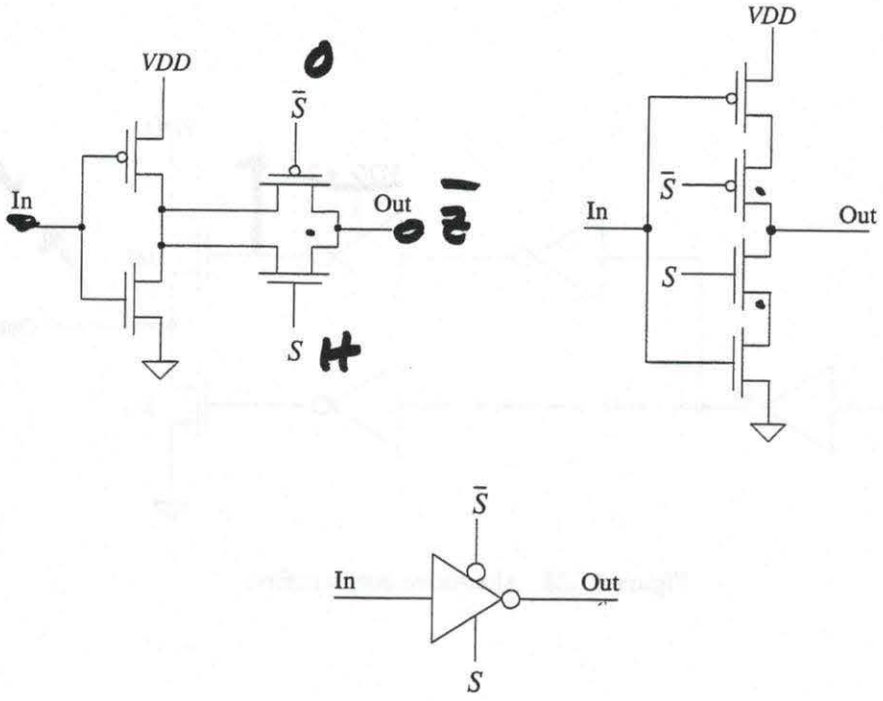


Figure 11.29 Circuits and logic symbol for the tri-state inverter.

CMOS Digital Circuit Design

Lesson 11:
Static Logic Gates

Hardcopy Visuals

CMOS Digital Circuit Design

Lesson 11:
Static Logic Gates

Hardcopy Visuals

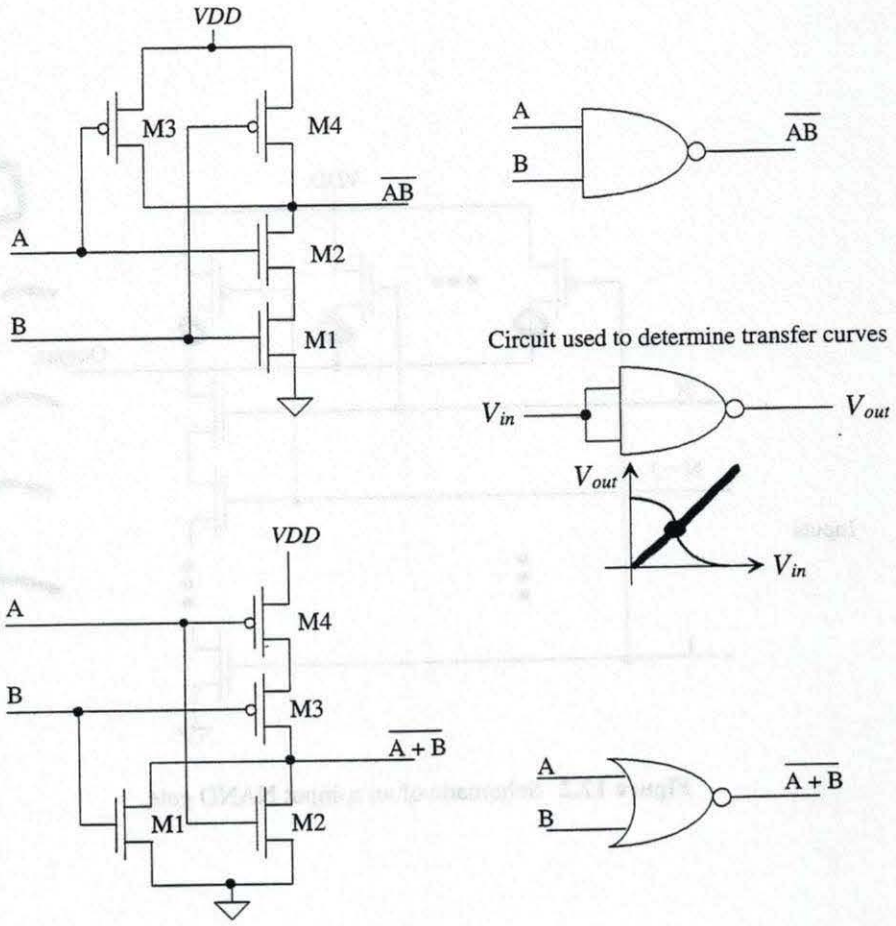


Figure 12.1 NAND and NOR gate circuits and logic symbols.

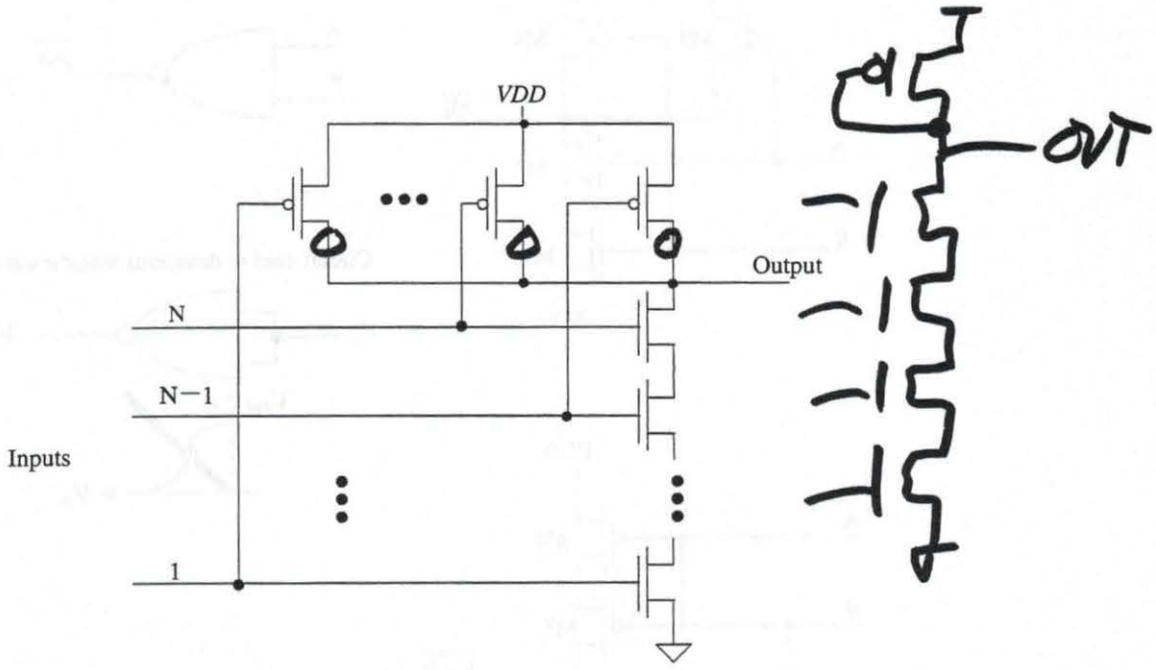


Figure 12.2 Schematic of an n-input NAND gate.

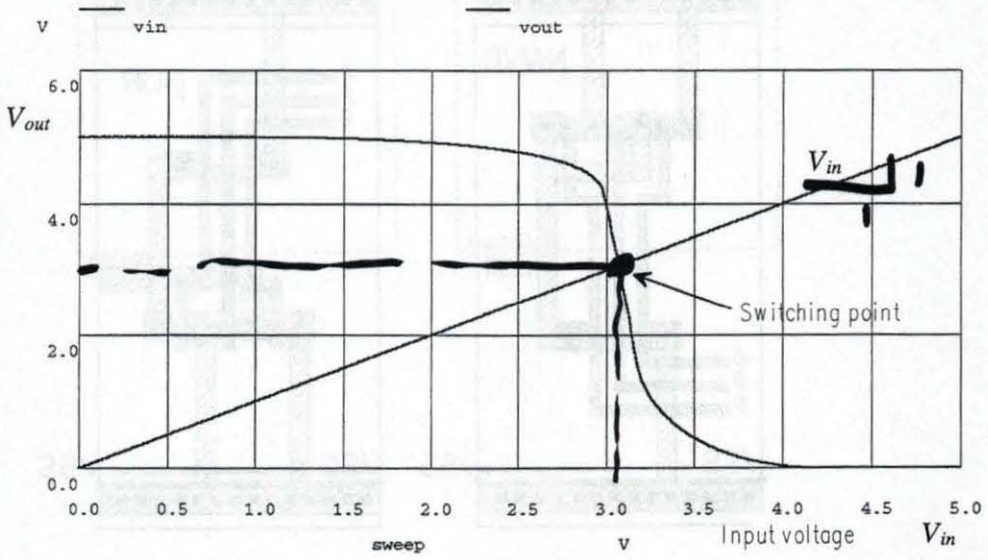


Figure 12.3 Voltage transfer characteristics of the three-input minimum-size NAND gate.

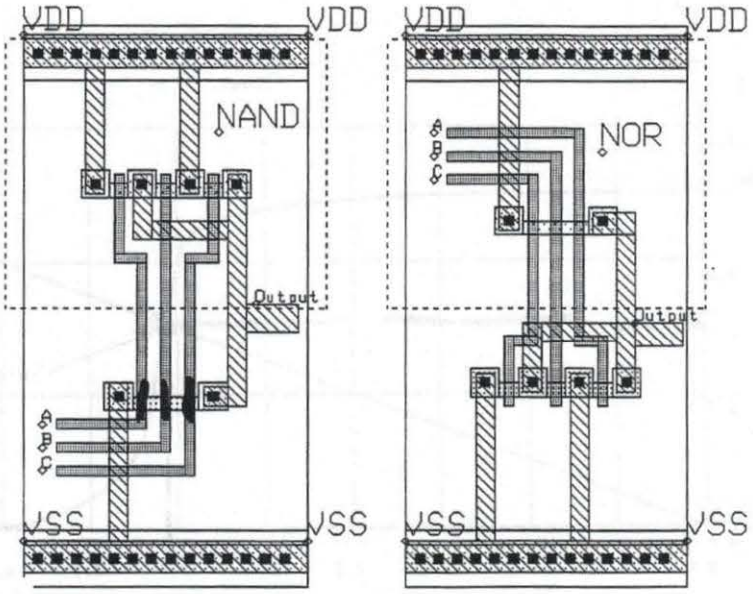


Figure 12.5 Layout of the NAND and NOR gate.

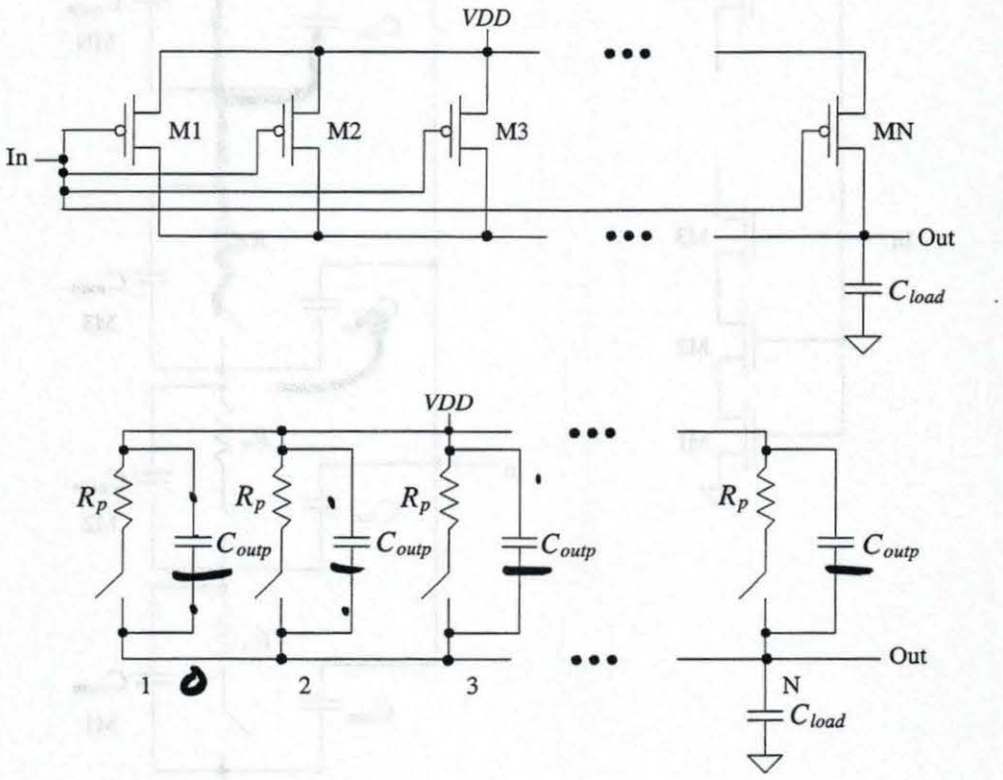


Figure 12.6 Parallel connection of MOSFETs and equivalent digital model.

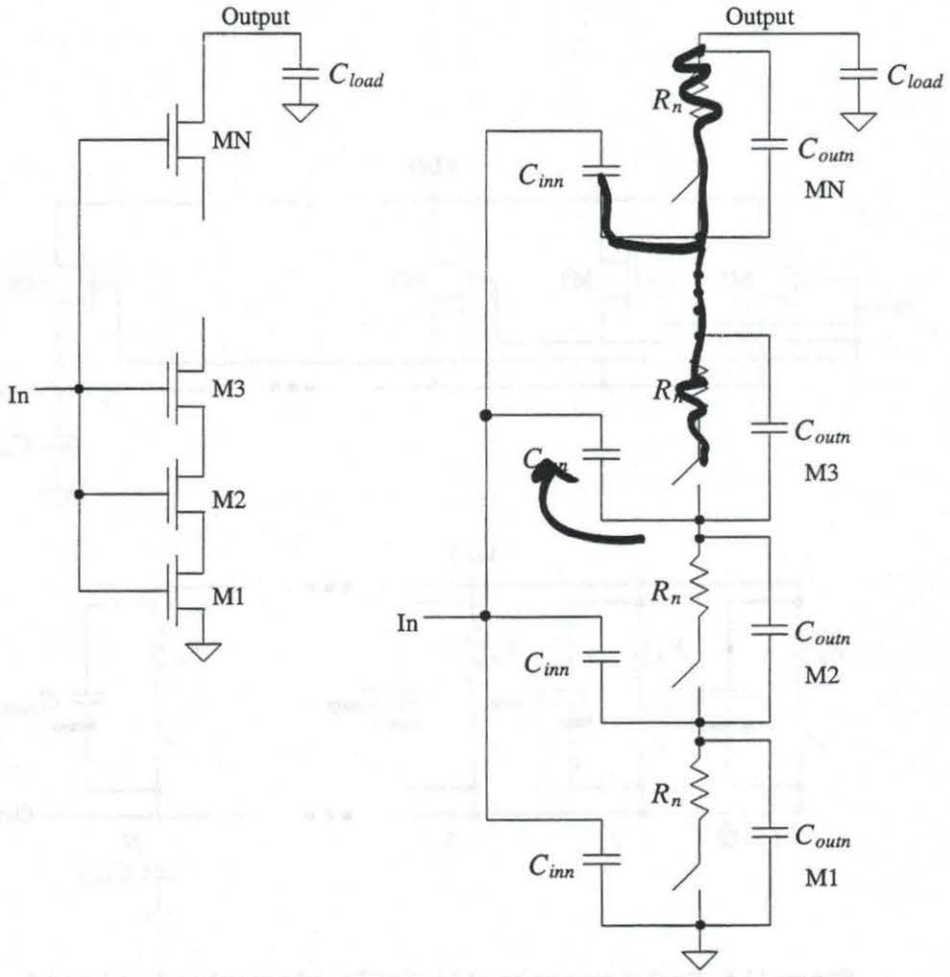


Figure 12.7 Series connection of MOSFETs and equivalent digital model.

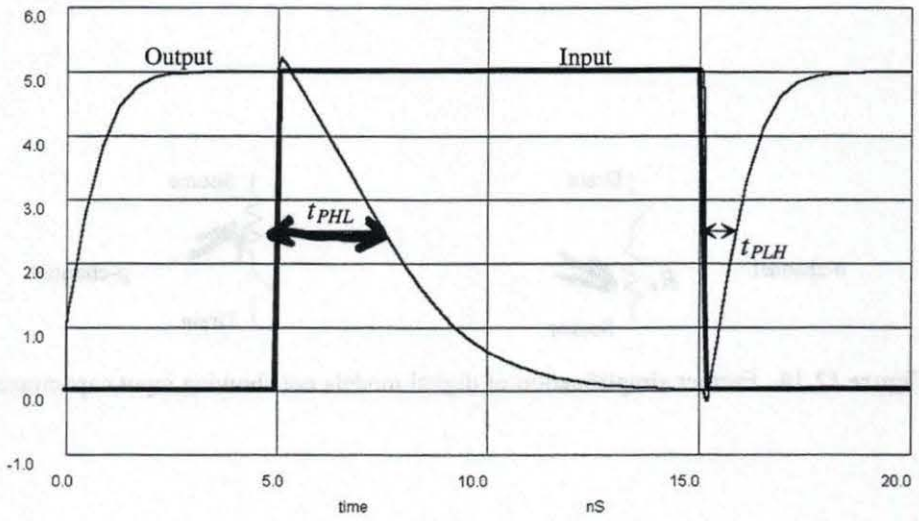


Figure 12.9 Output of the minimum-size NAND gate driving a 100 fF capacitor.

Figure 12.10 Further simplification of digital models not showing input capacitance.

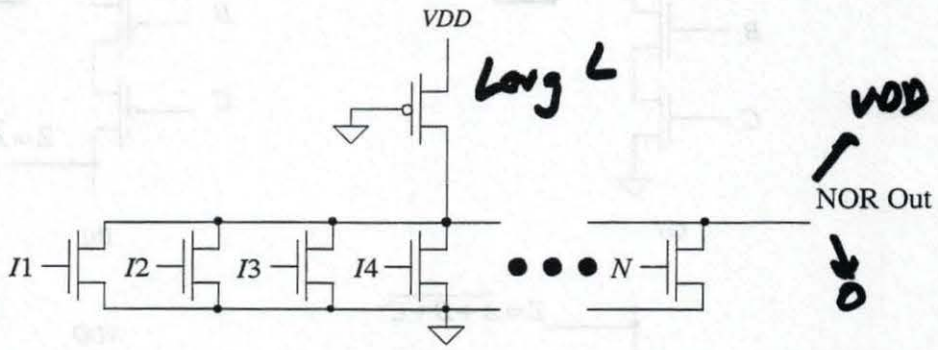


Figure 12.11 NOR configuration used for a large number of inputs.

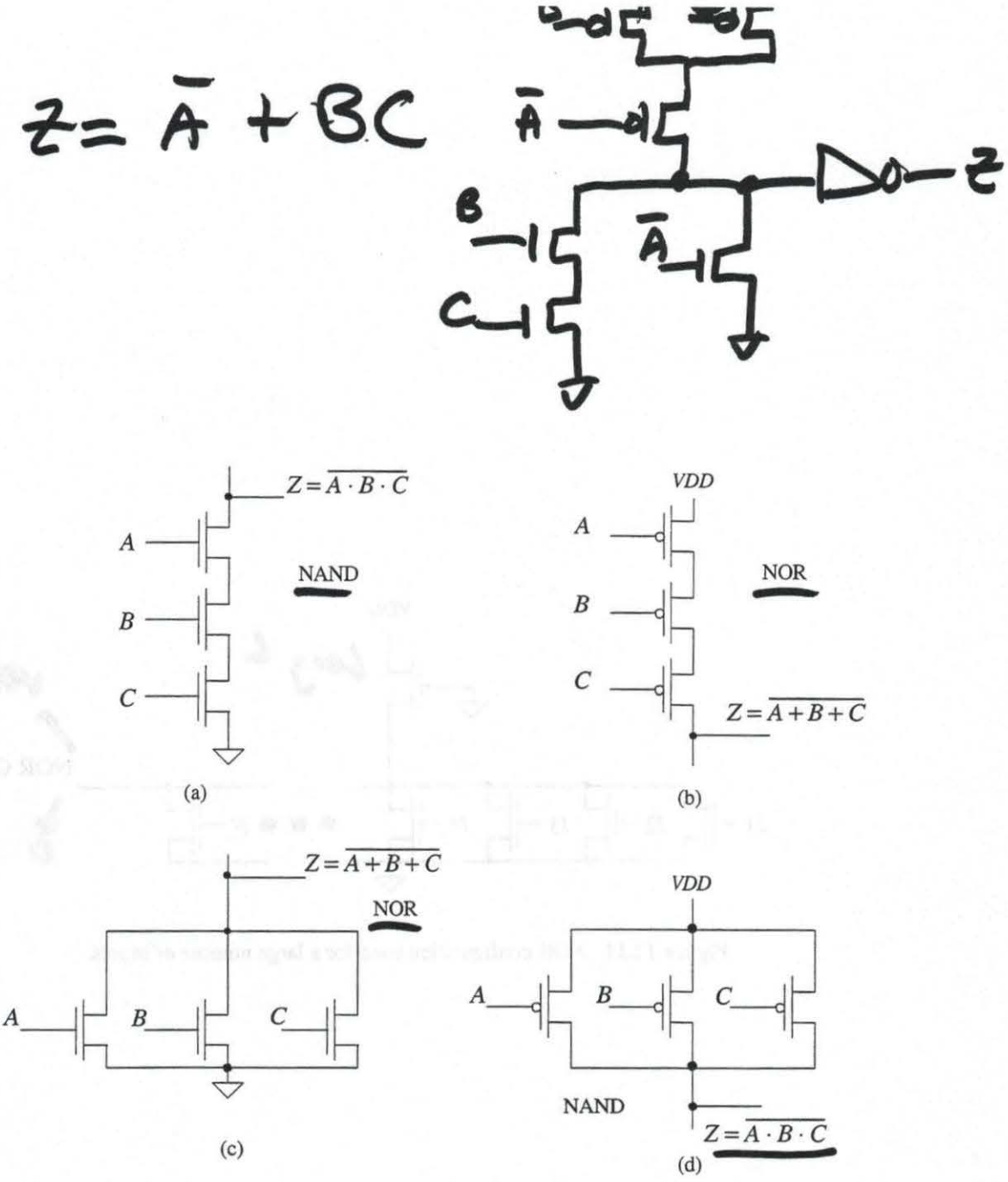
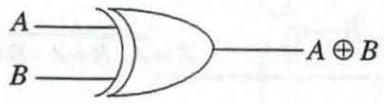


Figure 12.12 Logic implementation in CMOS.



A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Figure 12.15 Exclusive OR gate.

$$A \oplus B = \overline{\bar{A}\bar{B} + AB} = Z$$

$$\bar{Z} = \bar{A}\bar{B} + AB$$

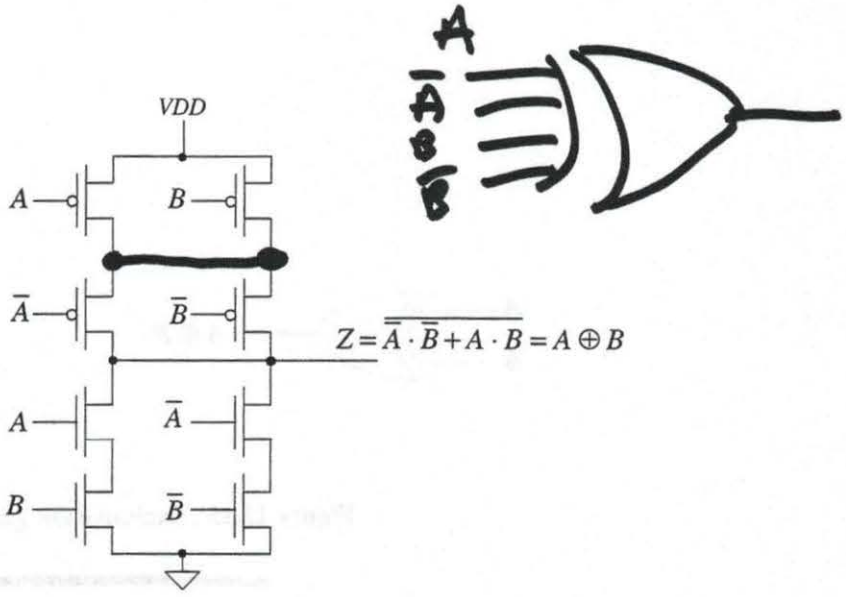


Figure 12.16 CMOS AOI XOR gate.

CMOS Digital Circuit Design

Lesson 12:
The Transmission Gate

Hardcopy Visuals

CMOS Digital Circuit Design

Lesson 12:
The Transmission Gate

Hardcopy Visuals

P-channel passes a "1"
N-channel passes a "0"

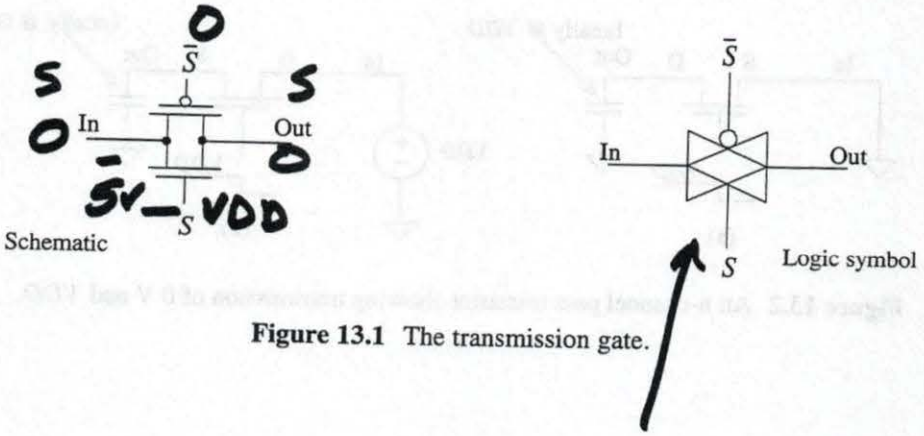


Figure 13.1 The transmission gate.

VDD - V_{Tn}

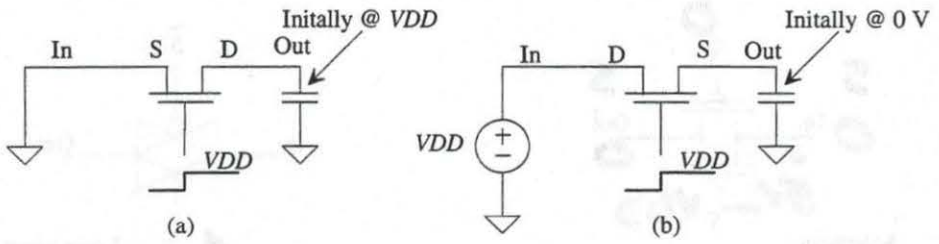


Figure 13.2 An n-channel pass transistor showing transmission of 0 V and *VDD*.

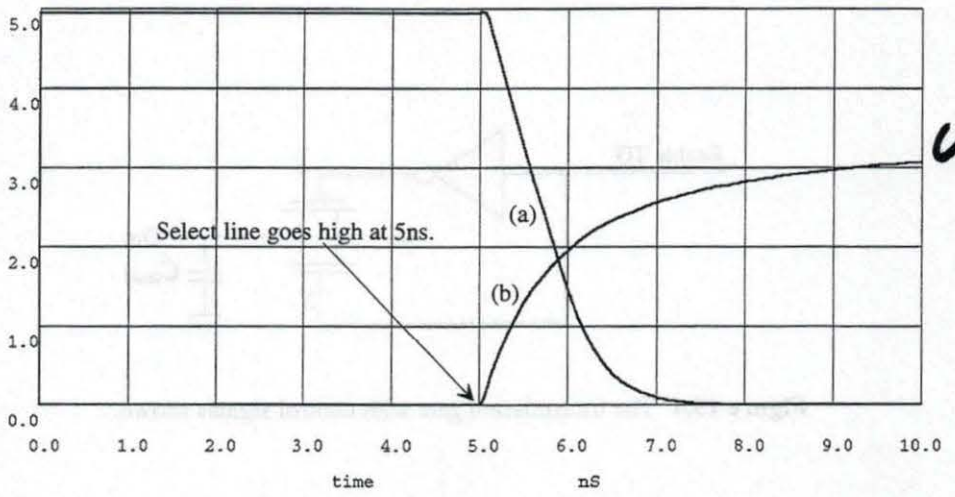


Figure 13.3 Simulation results of an n-channel MOSFET driving a 100 fF load capacitance, (a) with output initially at 5 V passing 0 V, (b) with output initially at 0 V passing 5V.

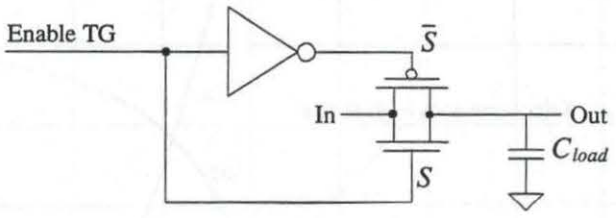


Figure 13.4 The transmission gate with control signals shown.

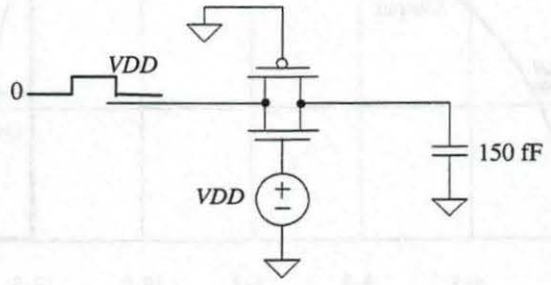


Figure Ex13.2

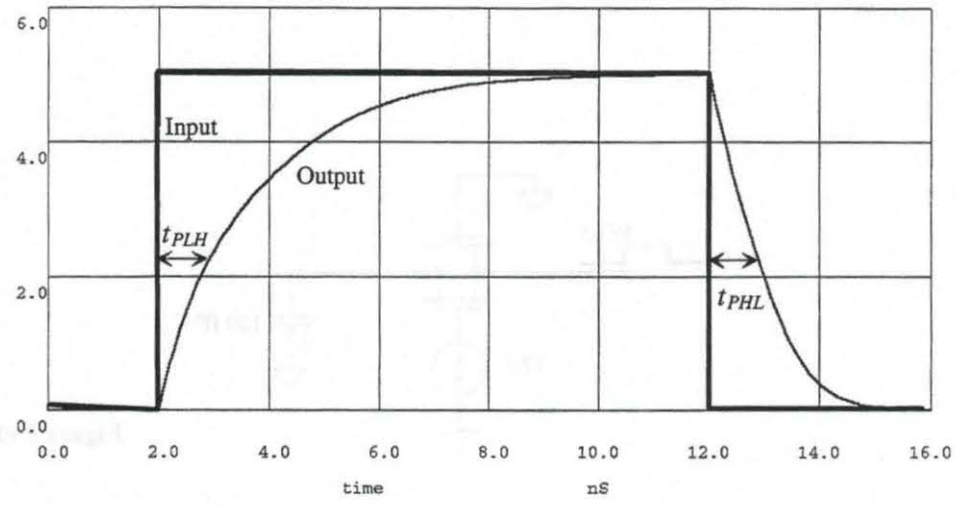


Figure 13.5 Simulation results of CMOS minimum-size TG driving a 150 fF load.

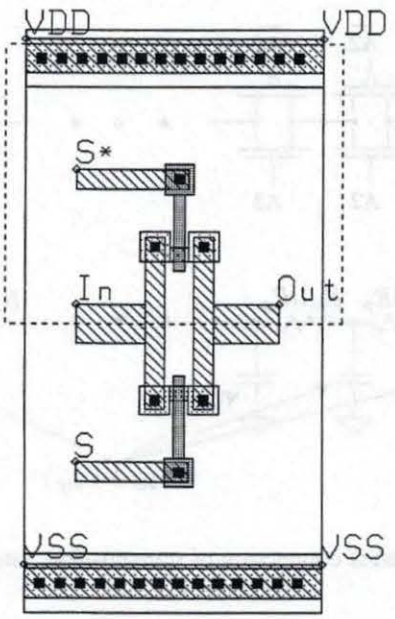


Figure 13.6 Layout of the CMOS transmission gate.

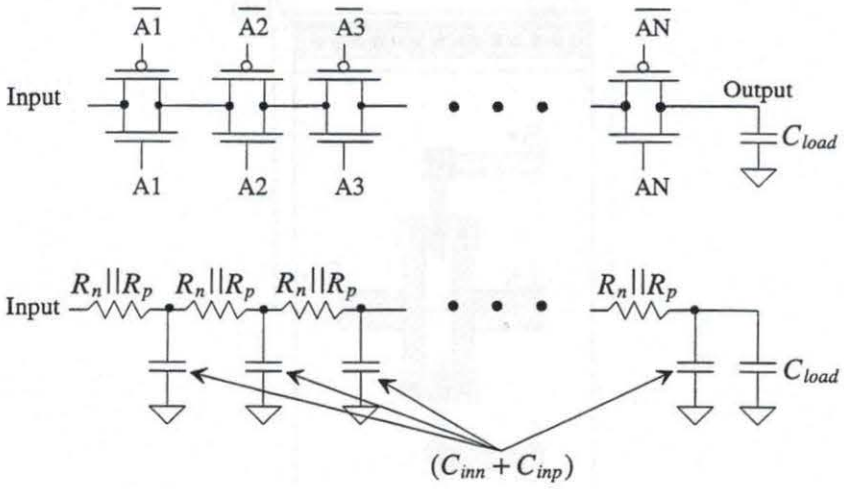


Figure 13.7 Series connection of transmission gates with digital model.

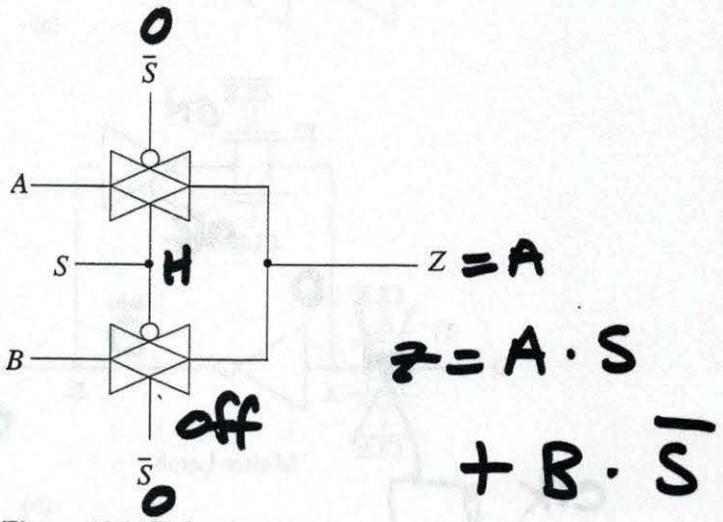


Figure 13.8 Path selector.

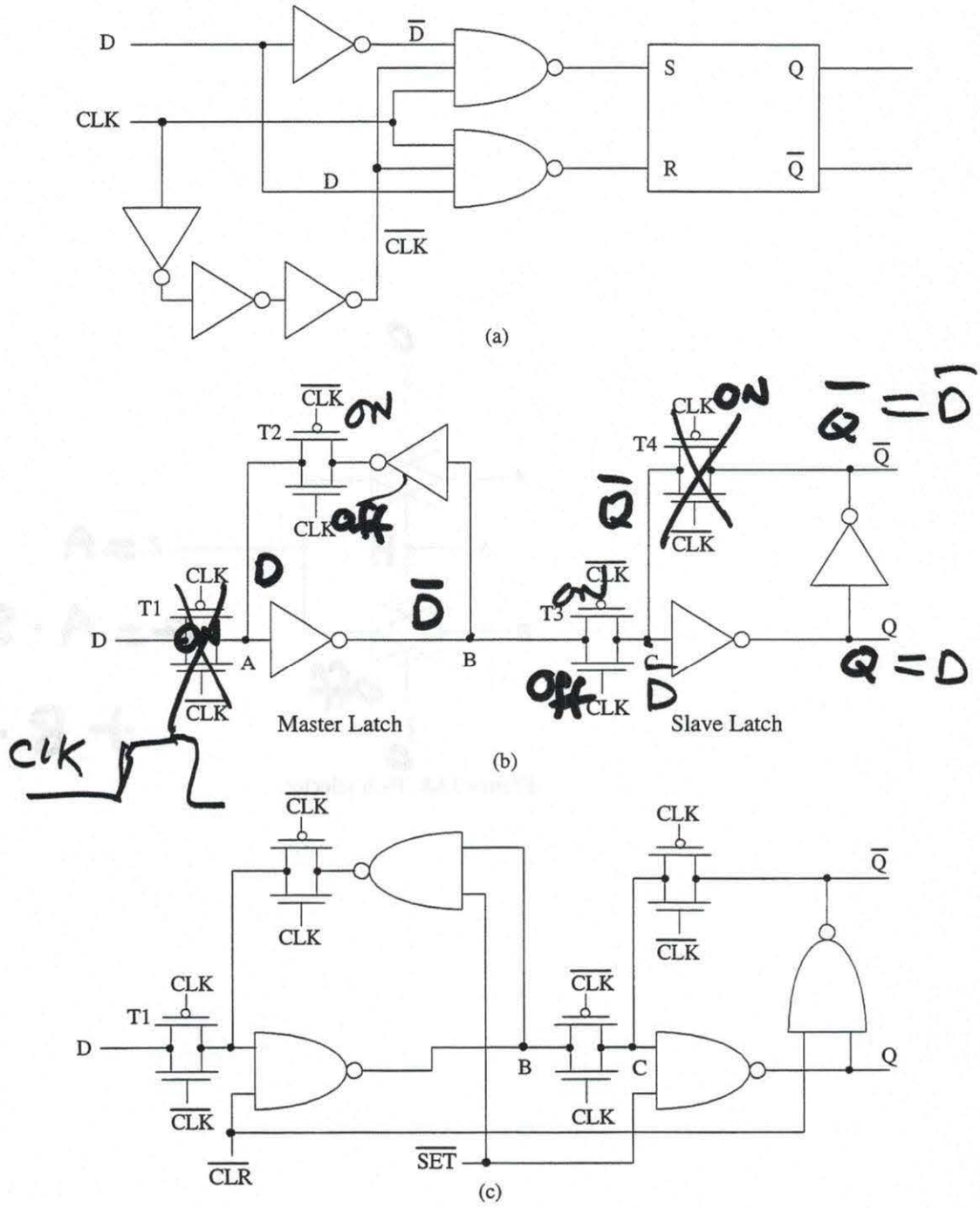


Figure 13.20 Edge-triggered D flip-flops, (a) Gate implementation, (b) TG implementation, and (c) TG implementation with set and clear.

CMOS Digital Circuit Design

Lesson 13:
Dynamic CMOS Logic

Hardcopy Visuals

CMOS Digital Circuit Design

Lesson 13:
Dynamic CMOS Logic

Hardcopy Visuals

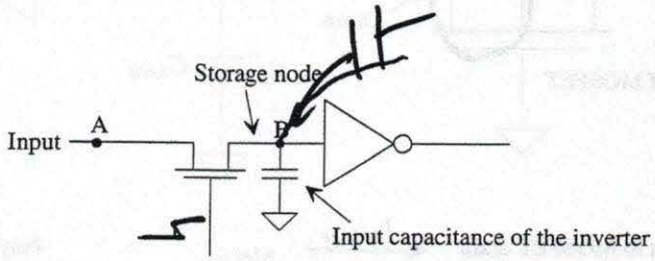


Figure 14.1 Example of a dynamic circuit and associated storage capacitance.

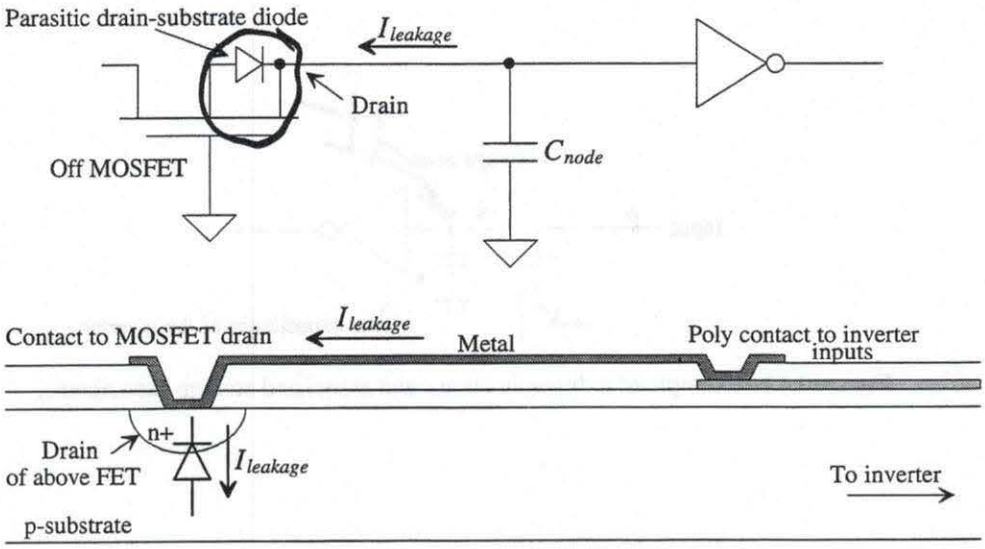


Figure 14.2 Leakage from a storage node through the drain-substrate diode.

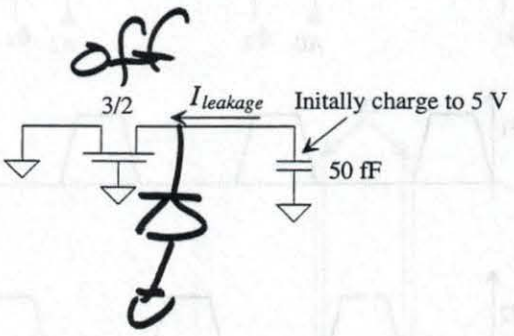


Figure Ex14.1

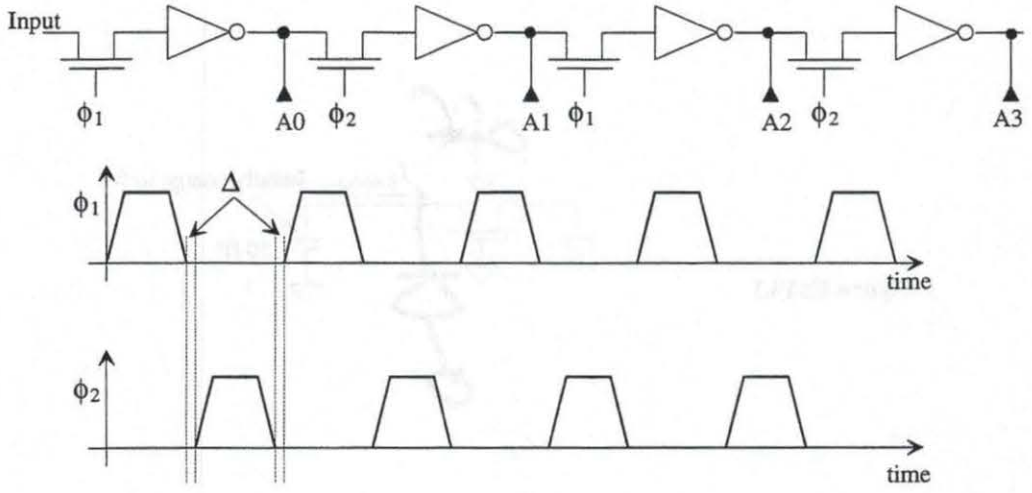


Figure 14.4 Dynamic shift register with associated nonoverlapping clock signals.

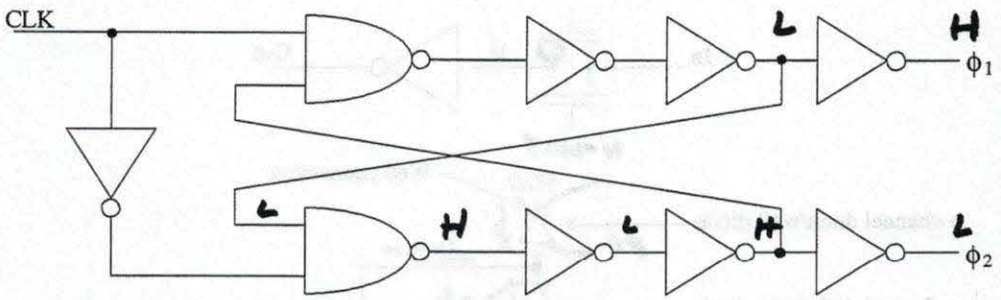


Figure 14.5 Nonoverlapping clock generation circuit.

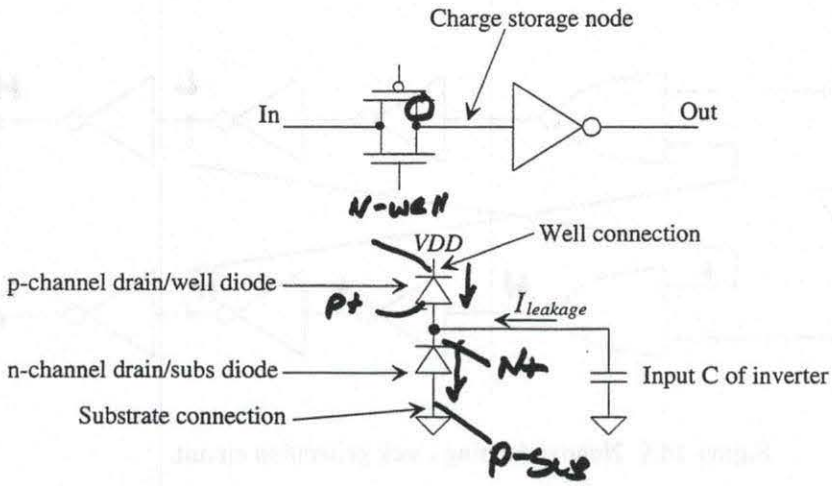


Figure 14.6 CMOS TG used in dynamic logic.

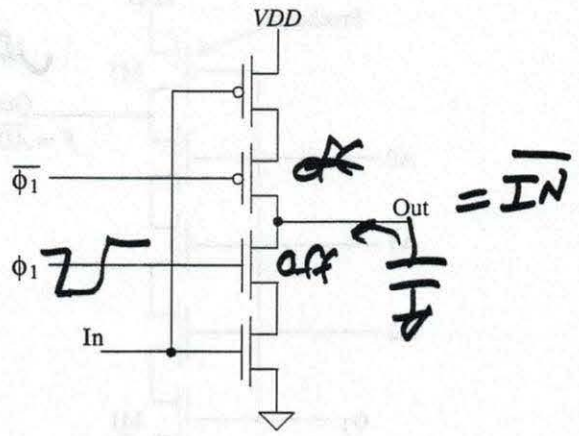


Figure 14.7 A clocked CMOS latch. The clock signals can be generated with an RS FF so that the edges occur essentially at the same moment in time.

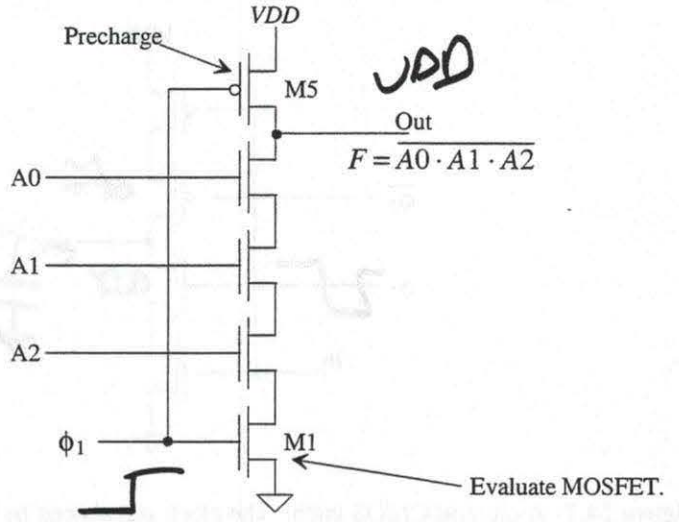


Figure 14.8 Precharge-evaluate three-input NAND gate.

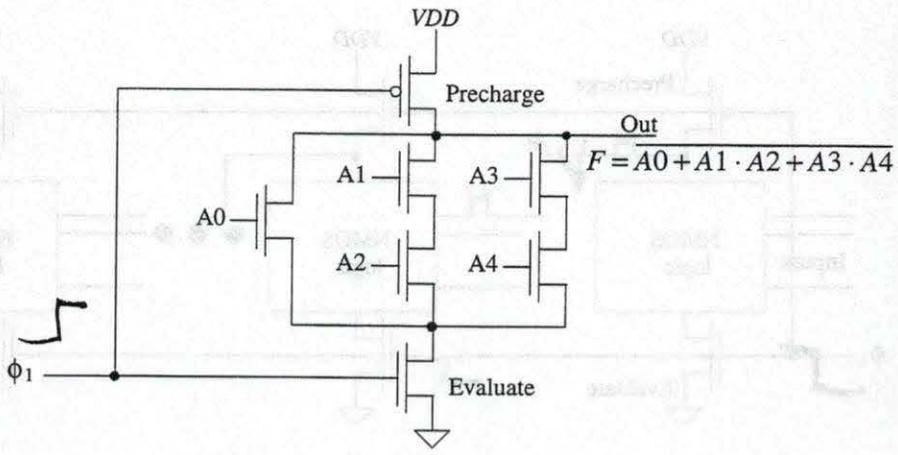


Figure 14.9 A complex PE gate.

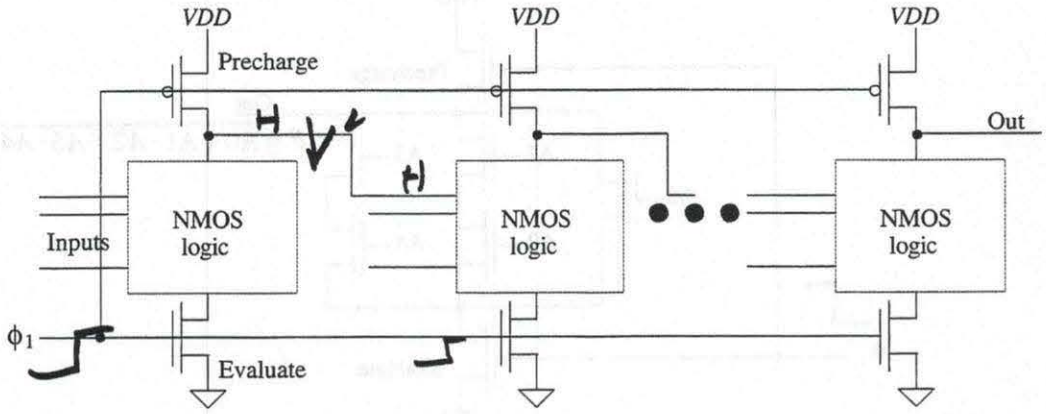


Figure 14.10 Problems with a cascade of PE gates.

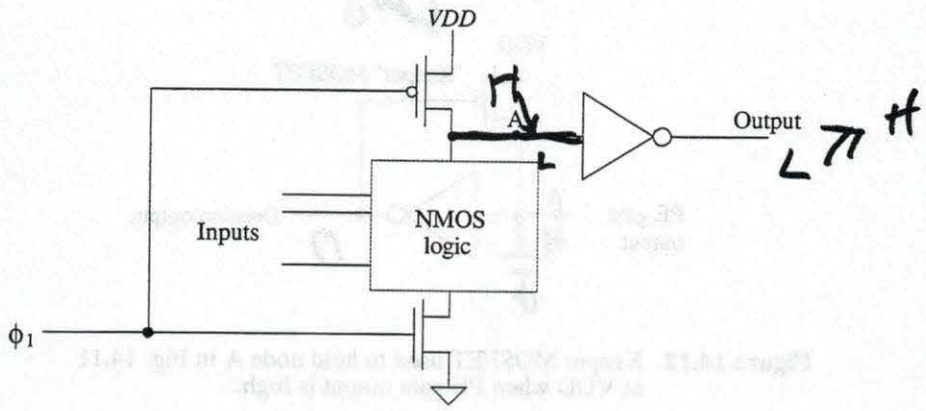


Figure 14.11 Domino logic gate.

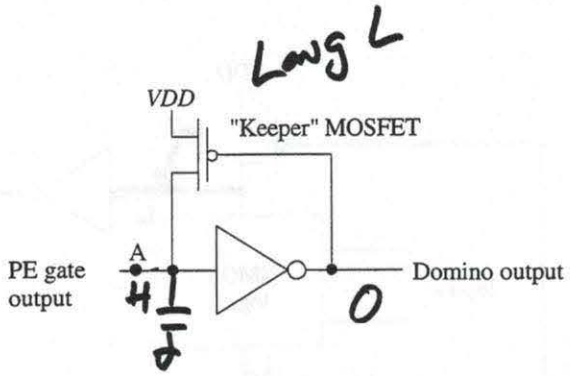


Figure 14.12 Keeper MOSFET used to hold node A in Fig. 14.11 at VDD when PE gate output is high.

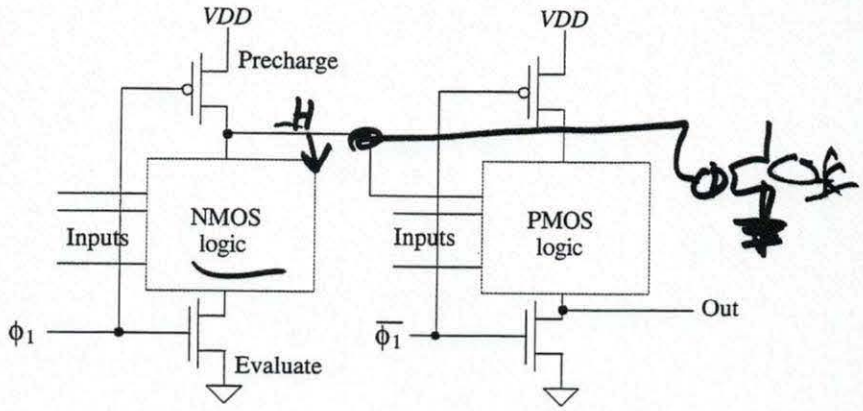


Figure 14.13 NP logic.

NORA

CMOS Digital Circuit Design

Lesson 14:
VLSI Layout

Hardcopy Visuals

CMOS Digital Circuit Design

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Hardcopy Visuals

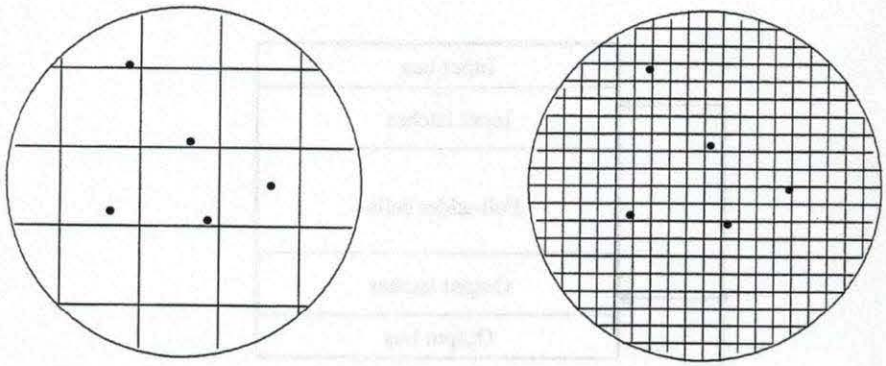


Figure 15.1 Defect density effects on yield.

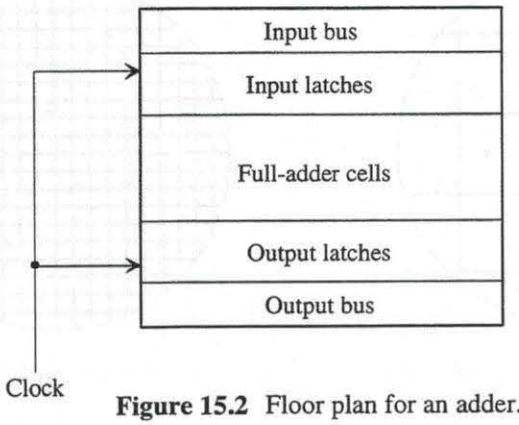


Figure 15.2 Floor plan for an adder.

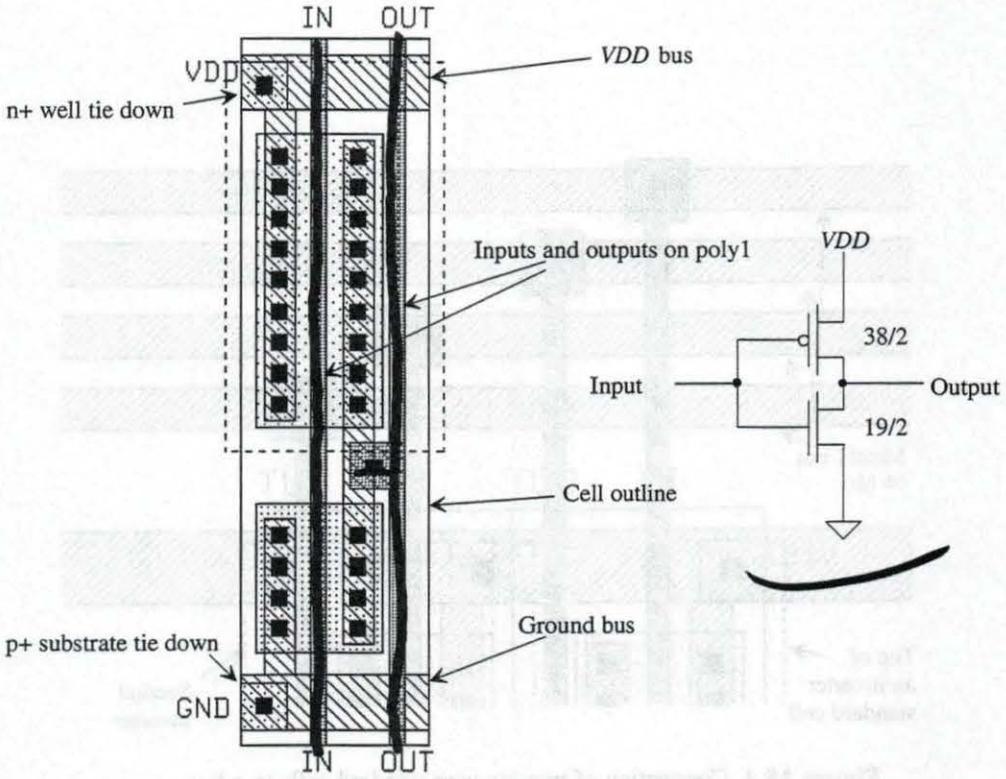


Figure 15.3 Standard-cell layout of an inverter.

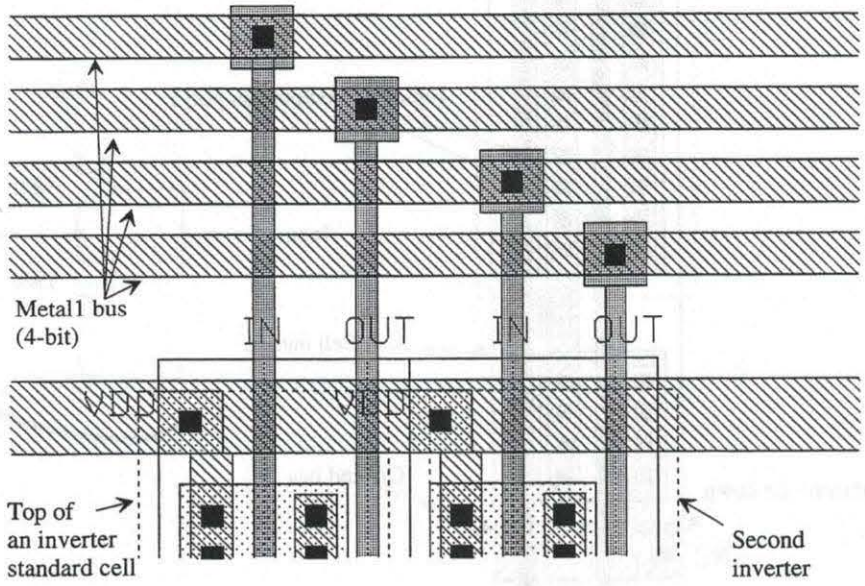


Figure 15.4 Connection of two inverter standard cells to a bus.

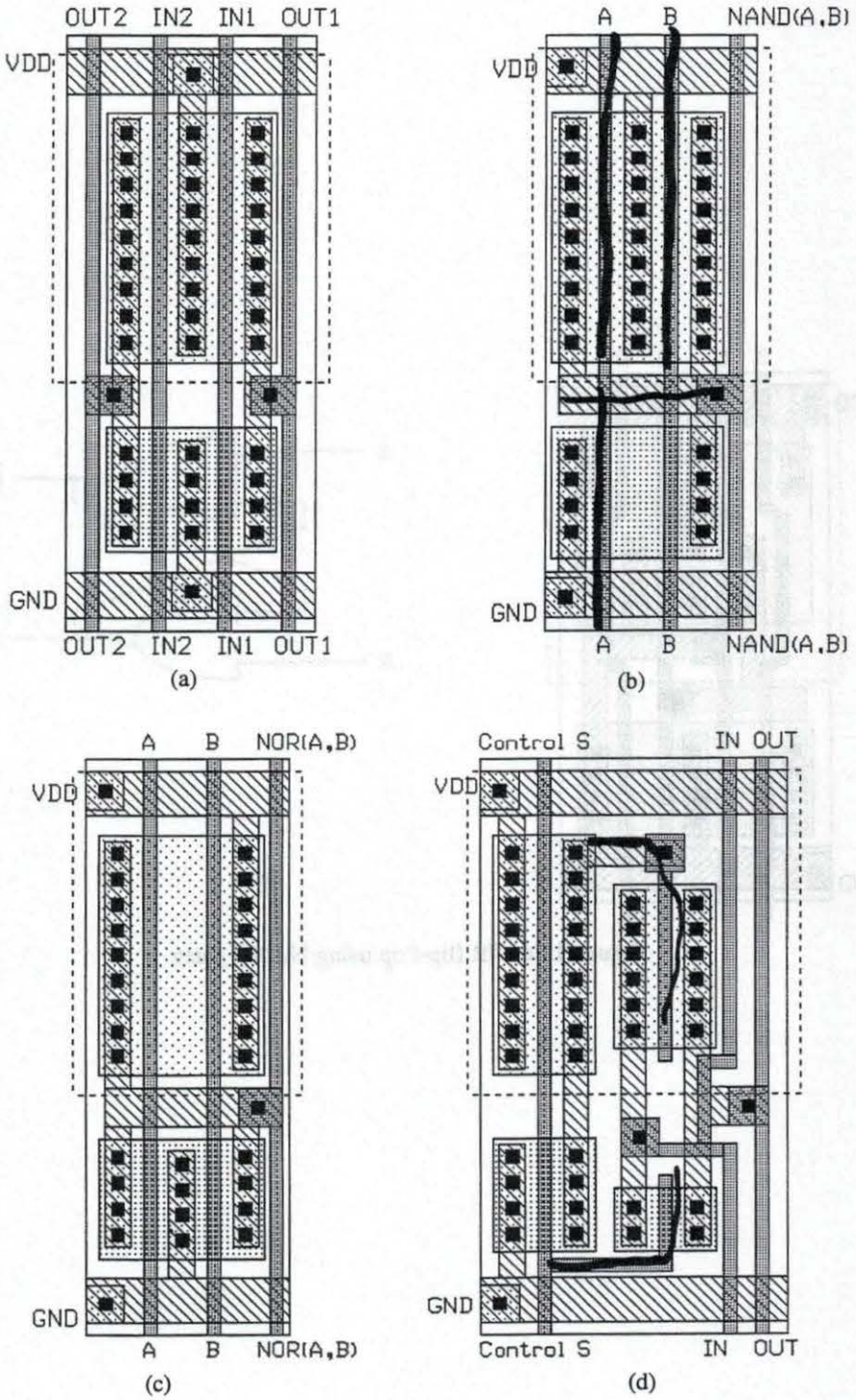
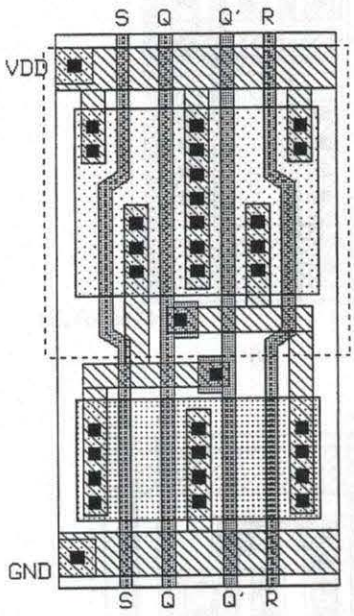


Figure 15.5 (a)Double inverter, (b) two-input NAND, (c) two-input NOR, and (d) transmission gate.



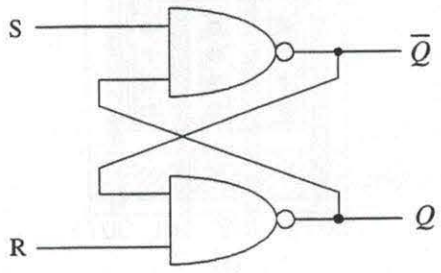


Figure 15.6 SR flip-flop using NAND gates.

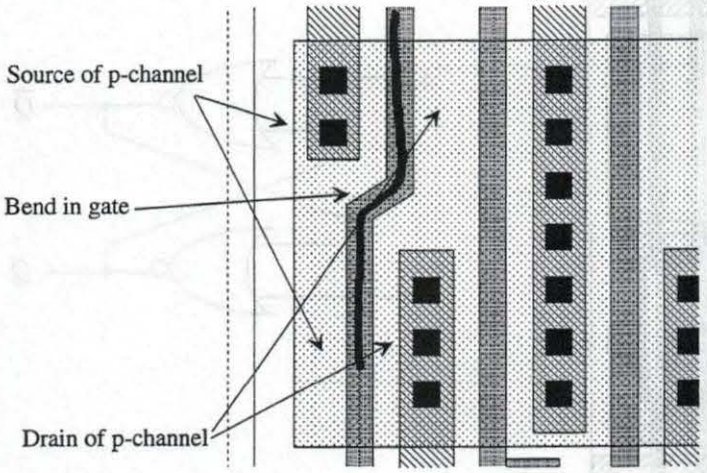


Figure 15.7 Section of the layout shown in Fig. 15.6.

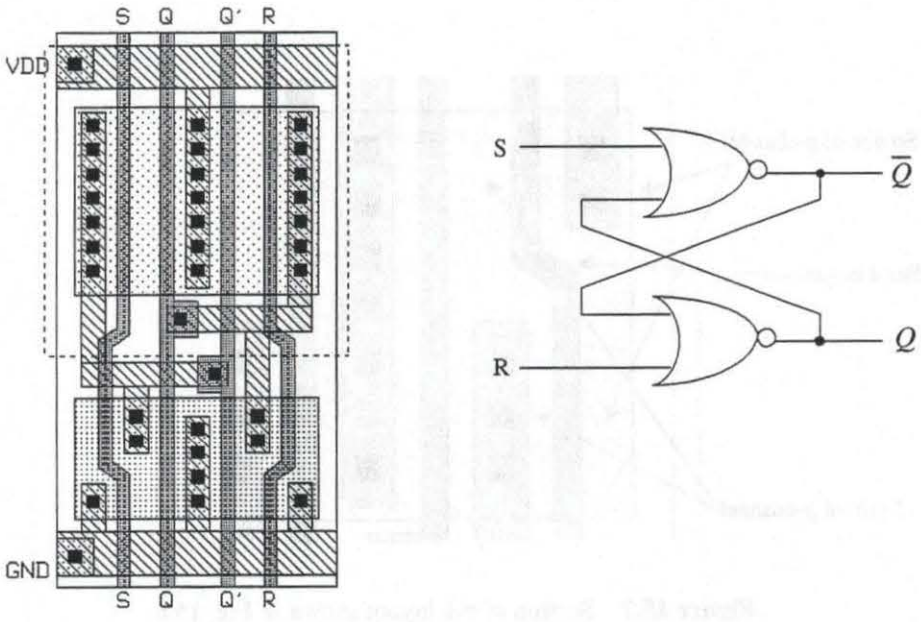
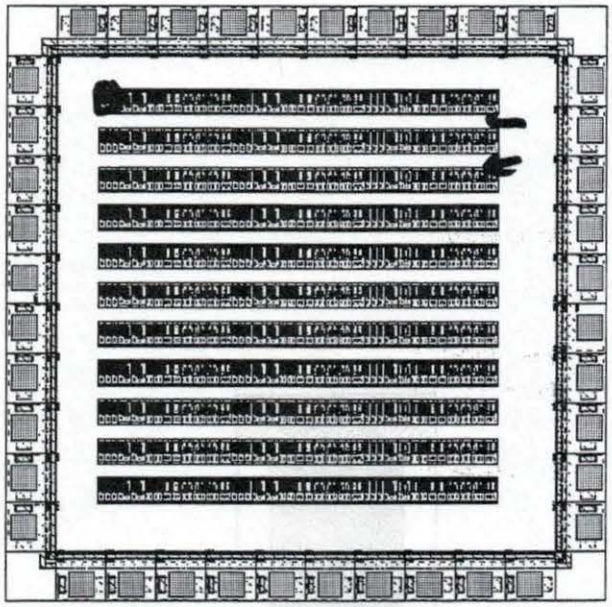
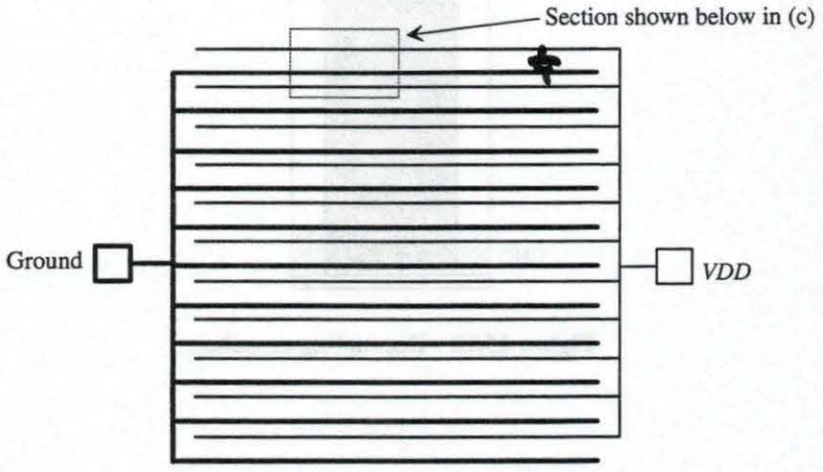


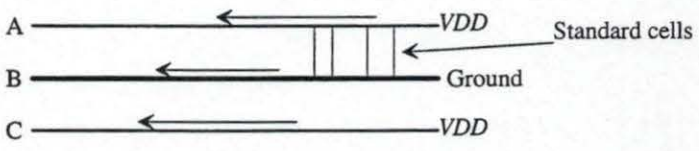
Figure 15.8 SR flip-flop using NOR gates.



(a)



(b)



(c)

Figure 15.9 Connection of power and ground to standard cells.

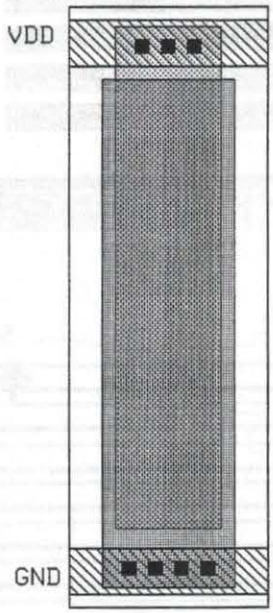


Figure 15.10 Decoupling capacitor.

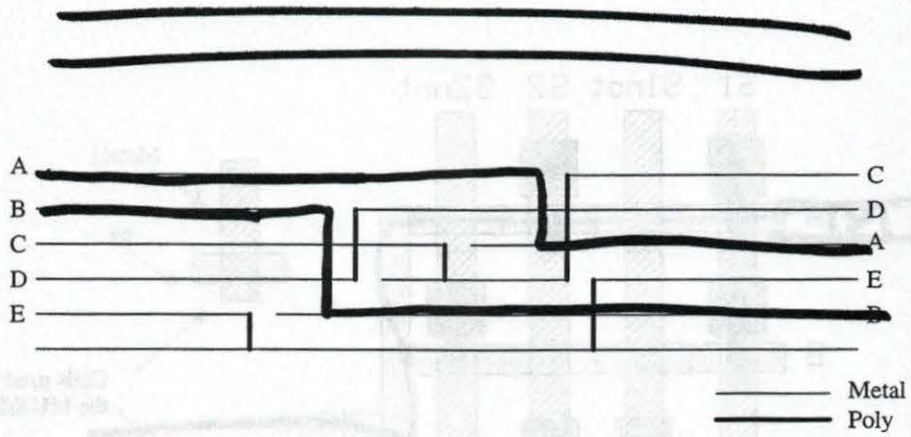


Figure 15.11 Bussing structure used to decrease signal coupling.

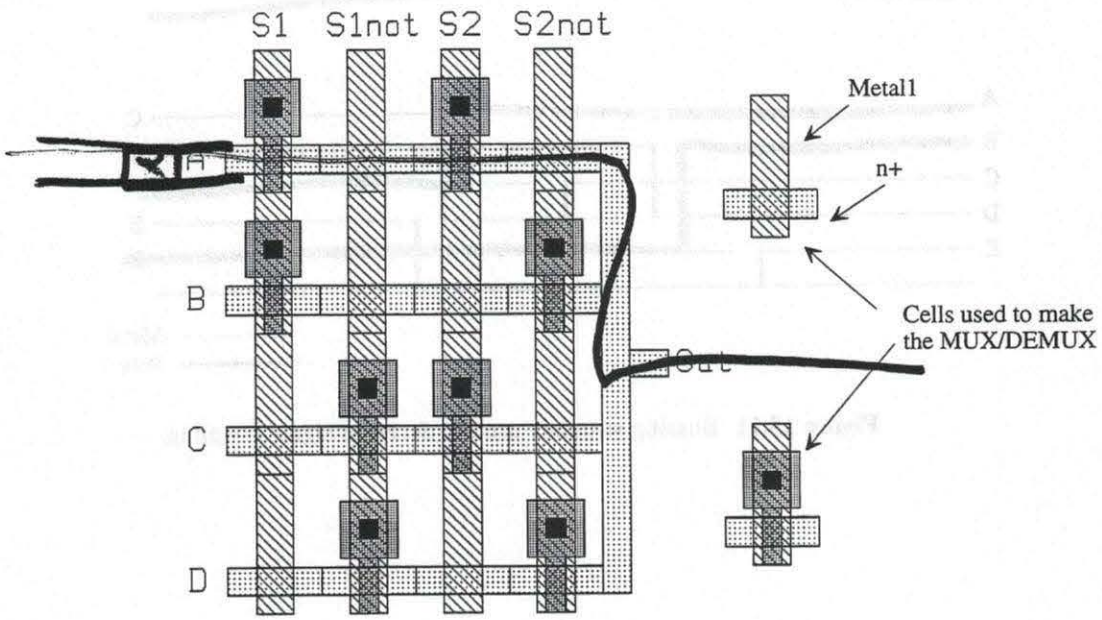


Figure 15.15 Layout of a 4 to 1 MUX/DEMUX.