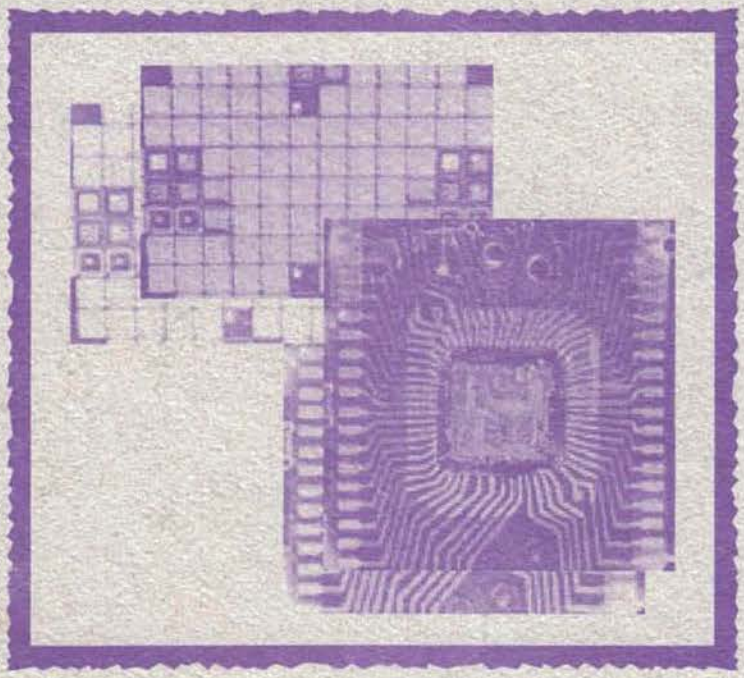
CMOS

Digital Circuit Design

Developed by
R. Jacob Baker
University of Idaho



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An IEEE/EAB
Self-Study Course

Prepared for the Educational
Activities Board of the
Institute of Electrical and
Electronics Engineers, Inc.

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CONTENTS

CMOS Digital Circuit Design

A Self-Study Course

This course was designed around Chapters 1 - 6 and 10 - 15 of *CMOS: Circuit Design, Layout, and Simulation*, by Baker, Li and Boyce, IEEE Press, 1998. The goal of this self-study course is to provide information on custom CMOS (Complimentary Metal Oxide Semiconductor) digital circuit design with an emphasis on the physical implementation of integrated circuits (ICs).

Prerequisites
This course assumes the student has an electrical engineering background with fundamental knowledge in the areas of digital logic design, linear circuits, and basic electronics. No knowledge of integrated circuit design is assumed.

Course Objectives
After completing this course you should be able to:

- Discuss the basic fabrication layers in a CMOS process.
- Sketch a schematic from an integrated circuit layout.
- Demonstrate an understanding of the origins of the unwanted parasitics in a CMOS IC.
- Describe qualitatively how a MOSFET operates.
- Design static and dynamic logic gates.
- Explain timing constraints in a CMOS IC.
- Size n- and p-channel MOSFETs for specific drive levels.

Features of this course
This course includes:

- a study guide including learning objectives, reading assignments, and practice problems (with solutions).
- the course textbook.
- a video tutorial for each lesson to help reinforce the concepts presented in the book and study guide.
- a final exam which, upon completion, will lead to a certificate of achievement from the IEEE and 8 continuing education units (CEUs).

How to use this course
This course was developed assuming the reader would complete the lessons sequentially, that is, Lesson 1 followed by Lesson 2, etc. Similarly the lessons should be completed sequentially in the following order:

1. Read the objectives of the lesson, designated by the  icon.

2. Read the assigned sections of the text, designated by the  icon.

3. Watch the video taped tutorial corresponding to the lesson number, designated by the  icon.

4. Review the key points of the chapter, designated by the  icon.

5. Solve the practice problems, designated by the  icon.

6. Review the practice problem solutions, designated by the  icon.

7. Review the objectives of the lesson and determine if they have been met. If so proceed to the next lesson. If not review 2 through 5 above until the objectives are met.

After finishing Lesson 14 review the final exam instructions given in the final exam booklet. Information on taking and submitting the exam for grading/credit is given in this booklet.

Acknowledgments

I would like to take this opportunity to thank Jill Bagley and Barbara Stoler of the Educational Activities Department of the IEEE for their time, effort and encouragement in developing this course. Also, special thanks go to my wife Julie and children Kyri and Josh for their patience and encouragement while this course was being developed.

Lesson 1

AN OVERVIEW OF CMOS CIRCUIT DESIGN

Learning Objectives

After completing this lesson you will be able to:

- Demonstrate an understanding of the course and its goals.
- Discuss what is meant by CMOS technology and why CMOS is popular for making integrated circuits.
- Explain what a die, wafer and leadframe are and how they are used in making a packaged integrated circuit.
- Determine the difference between layout and cross-sectional views of an integrated circuit.

Reading Assignment

Read section 1.1 of the text. If you want to learn how to use the LASI (Layout System for Individuals, pronounced "Lazy") layout tools discussed in the book read all of Chapter 1 and download the layout tools from the address given in the text. This course will not discuss the use of LASI.

Video Assignment

Watch the Lesson 1 tutorial on the video tape. These short tutorials are an important part of the course. Many of the final exam questions are based on the material presented in these tutorials.

Key Points

- Complimentary Metal Oxide Semiconductor (CMOS) is a manufacturable integrated circuit process consisting of n-channel and p-channel MOSFETs. CMOS is used in the fabrication of most processors and memory.
- CMOS integrated circuits are fabricated in a wafer. The wafer is cut-up into die which are connected to a lead frame and encapsulated in plastic.
- The layout view of an integrated circuit is the "top view" while the cross-sectional view is the side view.

Lesson 2 - THE WELL

Learning Objectives

After completing this lesson you will be able to:

- Describe what an n-well is and how it is fabricated.
- Lay out an n-well.
- Discuss sheet resistance and how to calculate the value of an n-well resistor.
- Analyze how the n-well forms a diode with the substrate
- Determine the origins of depletion capacitance.
- Explain RC delay through an n-well.

Reading Assignment

Read chapter 2 of the text. Also review the parameters related to the n-well, such as sheet resistance, given in Appendix A for the CN20 process.

Video Assignment

Watch the Lesson 2 tutorial on the video tape. Again, these videos are an important portion of the course and will cover material that will be on the final exam.

Key Points

- The n-well is used for the making the body of p-channel MOSFETs, as a resistor or as a diode when used with the p-substrate.
- The thickness of any fabricated layer in a CMOS process is constant. This fact leads to the use of sheet resistance with units of ohms/square to specify a resistance of a material.
- A parasitic depletion capacitance exists between any pn junction such as the junction between the p-substrate and the n-well.
- Because of the parasitic depletion capacitance an n-well resistor will exhibit delay, i.e. an input signal to one side of the resistor will take a finite amount of time to reach the other side of the resistor.

Practice Problems

Complete problems 2.4, 2.5, 2.10 (without the SPICE simulation).

Practice Problem Solutions

Problem 2.4: The minimum, typical and maximum values of resistivity ρ for an n-well with a thickness of 3 μm is equal to $R_{square} \cdot thickness$. From Appendix A, Table A.7, ρ is 6,000, 7,500, and 9,000 $\Omega \cdot \mu m$.

Problem 2.5: $I_s = J_s \cdot L \cdot W = 10^{-8} A/m^2 \times 10^{-4} m \times 10^{-4} m = 10^{-16}\ A$.

Problem 2.10: For a $5\mu m \times 2000\mu m$ n-well, the capacitance C is simply the product of the bottom area of the resistor with the zero bias depletion capacitance, or,

$$C = 100\,aF \times 5^2 \times 400 = 1\,pF$$

or if R = 1 Megaohm the delay is given by

$$t_d = 0.35RC = 0.35 \times 1\,pF \times 1\,M\Omega = 350\,ns$$

Lesson 3 - THE METAL LAYERS

Learning Objectives

After completing this lesson you will be able to:

- Determine what the metal and via layers are and how they are laid out in a CMOS process.
- Discuss the parasitics associated with the metal layers.
- Explain electromigration and how to size metal wires.
- Analyze cross talk and ground bounce.

Reading Assignment

Read Chapter 3 in the text. Review the information given in Appendix A Tables A.3, A.7 and A.8.

Video Assignment

Watch the Lesson 3 tutorial on the video tape.

Key Points

- The bonding pad is used to connect the chip to the lead frame.
- The metal layers are used to "wire" the integrated circuits together.
- There is a limit on the amount of current that can flow through a wire due to either the wire's sheet resistance or electromigration.

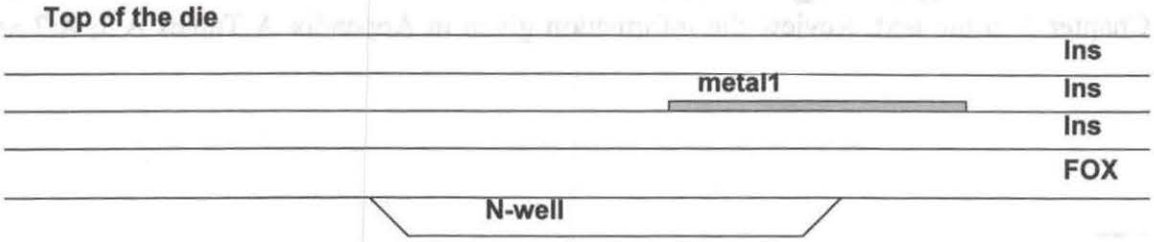
- The parasitic resistance of a wire can cause "ground bounce".
- The parasitic capacitance associated with a wire can result in coupled "noise" on the wire.
- Use of the CMOS layers: n-well, metal1, via, metal2, and overglass should be understood.

Practice Problems

Complete problems 3.2, 3.6, 3.7, and 3.11.

Practice Problem Solutions

Problem 3.2:



Problem 3.6: Considering only the plate capacitance, assume the area of metal1 and metal2 is A um^2. The capacitance between metal1 and metal2, from App. A, is 38 aF/um^2. The capacitance between metal1 and substrate is 26 aF/um^2. The voltage change on metal1 = 1V $\times(38AaF/\mu m^2/(38A+26A)aF/\mu m^2) = 0.594V$.

Problem 3.7: Taking J_{al} = 1mA/um the maximum current = 5 um x 1mA/um = 5 mA. The limitation for the contacts = 5 mA/(0.4 mA/contact) = 12.5 =>> 13 contacts needed.

Problem 3.11: From Fig. P3.11 the area between metal1 and metal2 is 72 um while the perimeter is 36 um. The area between metal1 and substrate is 12 um x 18 um or 216 um and the perimeter is 60 um. C_{12} = (38 x 6 x 12 + 104 x 36) aF = 6.48 fF, C_{1sub} = (26 x 12 x 18 + 82 x 60) aF = 10.536 fF. The voltage change on metal1 is $\Delta V_{metal1} = 5V \times C_{12}/(C_{12}+C_{1sub}) \approx 1.9V$

Lesson 4 - THE ACTIVE AND POLY LAYERS

Learning Objectives

After completing this lesson you will be able to:

- Discuss layers: n+, p+, contact, poly1.
- Lay out a MOSFET and a standard cell frame.
- Describe oxide encroachment and lateral diffusion.
- Explain why modern CMOS is termed a "self-aligned gate" process.

Reading Assignment

- Read Chapter 4 of the textbook and review Appendix A tables A.3, A.4, A.5, A.7 and A.8.

Video Assignment

Watch the lesson 4 tutorial.

Key Points

- Metal1 must connect downwards to n+, p+ or poly. It cannot be connected directly to the n-well or the p-substrate.
- A MOSFET is formed by laying out polysilicon (poly) over active (n+ or p+).
- A standard cell frame is used to route ground and power throughout the layout and to provide substrate and well tie-downs close to the areas where the MOSFETs are laid out.

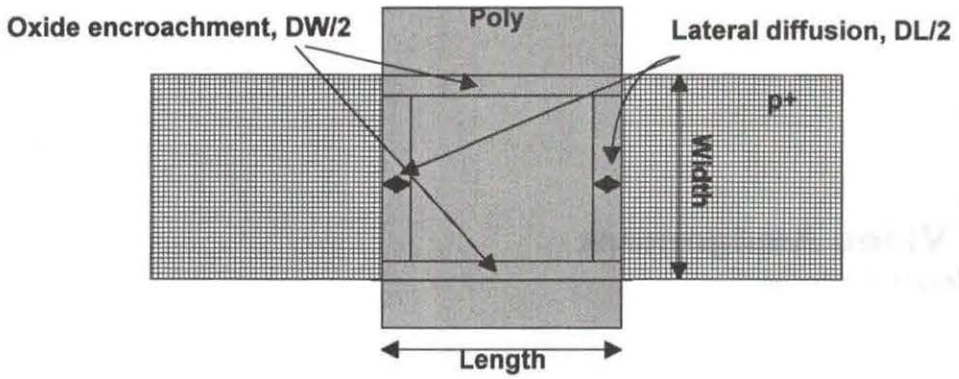
- Lateral diffusion affects the length of a MOSFET while oxide-encroachment affects the width.

Practice Problems

Complete problems 4.4, 4.5, and 4.8.

Practice Problem Solutions

Problem 4.4: (a) From the BSIM model parameters for the p-channel MOSFET in Appendix A, the delta-width due to the oxide encroachment, DW (dw), is 0.162551 um. (b) The oxide encroachment does not affect the length of the MOSFET. From the following layout, the location of the oxide encroachment illustrates this clearly.



Problem 4.5: See figure above. (a) From the BSIM model parameters for the p-channel MOSFET in appendix A, DL (dl) = 0.84424 um. (b) The lateral diffusion does not affect the width of the MOSFET. From the above layout, the location of the lateral diffusion can illustrate this clearly.

Problem 4.8: cj of the n+ implant is 1.0375×10^{-4} F/m^2, and cjsw is 2.1694×10^{-10} F/m, from page 710 and also page 77, AD = 10 x 10 um2, PD = 4 x 10 um, therefore, the maximum capacitance, i.e. the zero bias depletion capacitance = 1.0375×10^{-4} F/m^2 + 2.1694×10^{-10} F/m x 40 um = 10.375 fF + 8.6776 fF = 19.0526 fF. This depletion capacitance will decrease if the n+ implant is held at a constant potential while the potential of the substrate is reduced.

Lesson 5 - THE MOSFET AS A CAPACITOR

Learning Objectives

After completing this lesson you should be able to:

- Explain the difference between strong inversion, weak inversion, and the depletion modes of MOSFET operation.
- Lay out a "natural" MOSFET capacitor.
- Discuss how the threshold voltage is derived.

Reading Assignment

Read Sections 5.1 and 5.2 of the text.

Video Assignment

Watch the Lesson 5 tutorial. This tutorial will cover information not contained in Chapter 5 of the book.

Key Points

- Applying a potential greater than the MOSFET threshold voltage causes the surface at the oxide and semiconductor to "invert" forming a channel that connects the drain to the source of a MOSFET.
- When used correctly a MOSFET can make a very good capacitor.

- The body effect results in an increase in the threshold voltage of a MOSFET.
- A p-channel MOSFET can be laid out in its own well to eliminate body effect.

Practice Problems

Complete problems 5.3, 5.4, 5.5, and 5.8.

Practice Problem Solutions

Problem 5.3: Since the MOSFET is operating in the strong inversion region a large amount of electrons are attracted under the gate and an induced channel is formed below the gate oxide. This channel connects the source and drain so the gate overlap of the source drain has no effect on the capacitance. The capacitance between the gate electrode and the source/drain is simply $C_{ox} = C'_{ox} \cdot W \cdot L$

Problem 5.4: When the MOSFET is operating in the accumulation region, a large number of holes are attracted below the gate oxide. There is no induced channel between the drain and source. Therefore, the capacitance between gate and source/drain is equal to the overlap capacitance, $(\varepsilon_{ox} \cdot W \cdot LD)/TOX$

Problem 5.5: $C'_{ox} = \varepsilon_{ox}/TOX = (8.85 \times 3.97\ aF/\mu m)/(400 \times 10^{-10} m) = 878\ aF/\mu m^2$

Problem 5.8: The electrostatic potential at the oxide-semiconductor interface when $V_{GS} = V_{THN}$ is:

$$\phi_s = -\phi_F = \frac{kT}{q} \ln \frac{N_A}{n_i}$$

where N_A is the number of acceptor atoms in the substrate, n_i is the intrinsic carrier concentration of silicon.

Lesson 6 - THE MOSFET

Learning Objectives

After completing this lesson you will be able to:

- Determine the basic operation of an n-channel MOSFET.
- Recognize how changing the gate-source or drain-source voltage of a MOSFET changes the MOSFETs drain current.
- Discuss channel length modulation; what it is and where it comes from.

Reading Assignment

Read Section 5.3 and Appendix A of the text.

Video Assignment

Watch the Lesson 6 tutorial.

Key Points

- The inverted channel under the gate oxide has a sheet resistance that is a function of the applied V_{GS}.
- The MOSFET enters the saturation region when the charge in the channel becomes zero at the channel-drain interface.

- Channel length modulation results from the electrical channel length changing with drain to source potential.

Practice Problems

Complete problems 5.13, 5.14, 5.15.

Practice Problem Solutions

Problem 5.13: Since every MOSFET shown in Fig. P5.13 has the same V_{DS}, V_{GS}, KP, L and V_{THN}, the current flowing in each MOSFET is:

$$I_{Dn} = KP \cdot \mu_n \cdot \frac{W_n}{L}(V_{GS} - V_{THN})^2 \text{ or } I_{Dn} = KP \cdot \mu_n \cdot \frac{W_n}{L}\left[(V_{GS} - V_{THN})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

or since $I_{Dtotal} = I_{D1} + I_{D2} + ... + I_{dn}$

$$I_{Dtotal} = KP \cdot \mu_n \cdot \frac{W_1 + W_2 + ... + W_n}{L}(V_{GS} - V_{THN})^2$$

and for the triode region

$$I_{Dn} = KP \cdot \mu_n \cdot \frac{W_1 + W_2 + ... + W_n}{L}\left[(V_{GS} - V_{THN})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

Problem 5.14: Calling the node connected to the drain of M1 and the source of M2 "V_1" then $V_{GS1} = V_G$ (the voltage on the gates assuming the source of M1 is grounded), $V_{DS1} = V_1$, $V_{GS2} = V_G - V_1$, $V_{DS2} = V_D - V_1$ (where V_D is the voltage on the drain of M2 to ground). *If M1 operates in the saturation region*, then $V_{DS1} \geq V_{GS1} - V_{THN}$, i.e. $V_1 \geq V_G - V_{THN}$. For M2, $V_{GS2} - V_{THN} = V_G - V_1 - V_{THN} \leq 0$. This means that M2 cannot conduct a current if M1 is operating in the saturation region so, therefore, M1 can either operate in either the cutoff region or the triode region but not the saturation region.

Problem 5.15: From Figure P5.14, we assume the most general case when both MOSFETs are operating in the triode region. We know from the previous problem that M1 can't operate in the saturation region. We can write:

$(I_D \times L1)/(KP \times W) = [(V_G - V_{THN})V_1 - V_1^2/2]$ and

$(I_D \times L2)/(KP \times W) = [(V_G - V_{THN} - V_1)(V_D - V_1) - (V_D - V_1)^2/2]$.

Adding these two equations results in $I_D \times (L_1 + L_2)/(KP \times W) = V_G V_D - V_{THN} V_D - V_D^2/2$ which can easily be put into the desired form, i.e., $I_D = [(KP \times W)/(L_1 + L_2)] \cdot [(V_G - V_{THN})V_D - V_D^2/2]$

Lesson 7 - THE SHORT CHANNEL MOSFET

Learning Objectives

After completing this lesson you will be able to:

- Explain what short-channel effects are and their origins.
- Demonstrate an understanding of the concept of scaling MOSFETs.
- Discuss "drive current" and how it is used to characterize modern CMOS devices.

Reading Assignment

Read section 6.3 and review the information given on the CMOS14TB process in Appendix C.

Video Assignment

Watch the Lesson 7 tutorial.

Key Points

- Scaling is useful in CMOS design to reduce die size.
- As the channel length of a MOSFET is reduced the velocity of carriers traveling between the source and drain saturates causing the mobility of the carriers in the device to drop. This results in a reduction in current for a given gate to source voltage.
- The drain current is linearly related to the gate to source voltage in a short channel MOSFET.

Practice Problems

Complete problems 6.5, 6.6 and 6.11.

Practice Problem Solutions

Problem 6.5: The drive current of a short channel MOSFET is given by Eq. 6.4:

$$I_{drive} = v_{sat} \times C'_{ox} \times (V_{GS} - V_{THN} - V_{DS,sat})$$
$$C'_{ox} = \varepsilon_{ox}/TOX = (8.85 \times 3.97\ aF/\mu m)/(75 \times 10^{-10} m) = 4.685\ fF/\mu m^2$$
$$I_{drive} = 10^7\ cm/s \times 4.685 fF/\mu m^2 \times (2.5 - 0.5 - 1.5)V = 234\ \mu A/\mu m$$

For the long channel MOSFET described in Ch. 5 we assumed the mobility was a constant, i.e. not a function of V_{DS}. For short channel MOSFETs $V_{DS,sat}$ is not directly dependent on V_{GS} and V_{THN}, but it is related to the carrier drift velocity. From Fig. 6.8 and Eq. 6.39 $V_{DS,sat}$ is dependent directly on the critical electrical field which causes the drift velocity to become v_{sat}.

Problem 6.6: From Fig. 6.8, at 10^5 V/cm, both electron and hole velocities are saturated where v_{nsat} and v_{psat} are approximately 10^7 and 9 x 10^6 cm/s respectively. From Eq. 6.39 the mobility of the electrons is 100 cm²/Vs and the mobility of the holes is 90 cm²/Vs.

Problem 6.11: This problems solution is shown in Appendix C.

Lesson 8 - THE DIGITAL MODEL OF A MOSFET

Learning Objectives

After completing this lesson you will be able to:

- Model the MOSFET for digital circuit design.

Reading Assignment

Read Chapter 10 of the text.

Video Assignment

Watch the Lesson 8 video tutorial.

Key Points

- The MOSFET can be modeled by a switch in series with a resistor and two capacitors; one used for modeling the input capacitance of the MOSFET and one used for modeling the output capacitance.
- An n-channel MOSFET passes a logic high with a threshold voltage drop while a p-channel MOSFET passes a logic low with the addition of a threshold voltage.
- Series connection of MOSFETs can be used to implement multiplexers.

Practice Problems

Complete problems 10.1, and 10.7 (without SPICE simulations).

Practice Problem Solutions

Problem 10.1: For a 10um/2um MOSFET, the effective resistance of the NMOS is

$$R_n = 12\,k\Omega \times \frac{2}{10} = 2.4\,k\Omega$$

and for the PMOS, $R_p = 36\,k\Omega \times 0.2 = 7.2\,k\Omega$. The capacitance between the drain and ground is the same for both NMOS and PMOS (since they have the same width and length) and is equal to C_{ox} + 150 fF or 166 fF. From Eq. 10.8 and 10.9, for NMOS,

$$t_{PHL} = 2.4k \times 166f \approx 398\,ps, \text{ and } t_{HL} = 2 \times 2.4k \times 166fF \approx 797\,ps$$

and for the PMOS,

$$t_{PLH} = 7.2k \times 166f \approx 1.2ns, \text{ and } t_{LH} = 2 \times 7.2k \times 166fF \approx 2.4\,ns$$

Problem 10.7: For a 3um/2um MOSFET, the effective resistance of the NMOS is

$$R_n = 12\,k\Omega \times \frac{2}{3} = 8\,k\Omega$$

and for the PMOS, $R_p = 36\,k\Omega \times 0.66 = 24\,k\Omega$. The capacitance between the drain and ground is the same for both NMOS and PMOS (since they have the same width and length) and is equal to C_{ox} + 1 pF or approximately 1pF total. From Eq. 10.8 and 10.9, for NMOS,

$$t_{PHL} = 8k \times 1pF \approx 8\,ns, \text{ and } t_{HL} = 2 \times 8k \times 1pF \approx 16ns$$

and for the PMOS,

$$t_{PLH} = 24k \times 1pF \approx 24ns, \text{ and } t_{LH} = 2 \times 24k \times 1pF \approx 48\,ns$$

Lesson 9 - INVERTER OPERATION I

Learning Objectives

After completing this lesson you will be able to:

- Recognize the circuit topology of an inverter.
- Determine the operation of the inverter and how sizing the p- and n-channel MOSFETs affects the switching point voltage and speed of the inverter.
- Examine the layout of an inverter.

Reading Assignment

Read sections 11.1 - 11.3 of the text.

Video Assignment

Watch the lesson 9 video tutorial.

Key Points

- The maximum output voltage of a CMOS inverter is VDD while the minimum output voltage is ground. The switching point voltage lies somewhere between these boundaries and is set by the size of the MOSFETs.
- By changing the size of the MOSFETs we can change the "drive" or effective resistance of a MOSFET.

Practice Problems

Complete problems 11.1 and 11.2 without SPICE simulations and repeat Example 11.3 with a switching point voltage of 2.0V.

Practice Problem Solutions

Problem 11.1: From Eq. 11.4 with V_{SP} approximately equal to V_{THN}, β_n should be much larger than β_p. In a basic inverter, for both NMOS and PMOS, if the length of devices is the same and W_n = 400 um and W_p= 3 um then $V_{SP} = (20V_{THN} + VDD - V_{THP})/(1 + 20) = 1.05$ V.

Problem 11.2: With W = 10 um and a load capacitance of 1 pF, C_{tot} = 1pF+(2 x 10 x 2 x 800aF)=1.032pF. R_{n1} = 12kΩ x 2/10 = 2.4 kΩ, R_{p2} = 7.2 kW. The propagation delay times are $t_{PHL} = 2.4k\Omega \times 1.032pF = 2.5ns$ and $t_{PLH} = 7.2k\Omega \times 1.032pF = 7.43ns$

Example 11.3 (repeat) with VSP = 2.0 V: We can re-write equation 11.4 (with $V_{THN} = 0.8$, VDD = 5 and $V_{THP} = 0.9$) so it reads

$$2 = \frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot 0.8 + 4.1}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

solving for the transconductance ratios yields, $\beta_n/\beta_p \approx 3.0$. Since $KP_n = 3KP_p$ so setting $W_n = W_p$, and $L_n = L_p$ yields the $V_{SP} = 2$V.

Lesson 10 - INVERTER OPERATION II

Learning Objectives

After completing this lesson you will be able to:

- Design CMOS off-chip buffers.
- Lay out large MOSFETs.
- Recognize other inverter configurations.

Reading Assignment

Read sections 11.4 and 11.5 in the text.

Video Assignment

Watch the lesson 10 video tutorial.

Key Points

- A buffer, made from a string of inverters, is used to isolate on-chip logic signals from large off-chip capacitances.
- Minimum delay through a buffer is sacrificed for smaller layout area in most practical buffer designs.
- Other inverter topologies can be used when a large number of inputs is needed or a tri-state output is required.

Practice Problems

Complete problems 11.5 (without simulations) and repeat examples 11.8 and 11.9 with an increase in load capacitance to 50 pF.

Practice Problem Solutions

Problem 11.5: For the first inverter with size 150/50, the total resistance is (assuming 2 um length), R = (12k x 2/50 + 36k x 2/150) = 0.96k, and the output capacitance is C = 2 x 50 x 800 aF + 2 x 150 x 800 aF = 320 fF = .32 pF. To drive 50 pF load capacitance, try a three stage buffer, i.e. N = 3. Area = [50 pF/(0.32 x 3/2)pF] = 4.705. Using Eq. 11.25, the delay is,

$$t_{PHL} + t_{PLH} = 3 \times (.96k) \times (.32pF + 4.705 \times 0.48pF) = 7.426ns < 10ns$$

using a two stage buffer, A = 10.206.

$$t_{PHL} + t_{PLH} = 2 \times (.96k) \times (.32pF + 10.206 \times 0.48pF) = 10.02ns > 10ns$$

therefore, a three stage buffer must be used.

Example 11.8 (repeat) with a 50 pF load: $t_{PHL} + t_{PLH} = (8k + 8k)50pF = 800\,ns$

Example 11.9 (repeat) with a 50 pF load:
If we try three stages the area factor is $A = (50p/28.8f)^{1/3} = 12$ with a resulting delay of 3(16k) x (19.2f + 12 x 28.8f) = 17.5 ns > 15 ns. If we try five stages than $A = (50p/28.8f)^{1/5} = 4.44$ with a resulting delay of 3(16k) x (19.2f + 4.44 x 28.8 f) = 7.06 ns.

Lesson 11 - STATIC LOGIC GATES

Learning Objectives

After completing this lesson you should be able to:

- Discuss the basic operation and topologies of CMOS static logic gates.
- Recognize switching characteristics of CMOS static logic.
- Design and operate CMOS complex logic gates.

Reading Assignment

Read Chapter 12 in the course textbook.

Video Assignment

Watch the lesson 11 video tutorial.

Key Points

- Static gates are formed by complementary connections of series (parallel) NMOS with parallel (series) connections of PMOS.
- Large numbers of series connected MOSFETs can result in long propagation delays.
- Complex CMOS logic gates can be use to implement logic functions in a single gate that are not possible to implement NANDs and NORs alone.

Practice Problems

Complete problems 12.3 (without simulations) and problem 12.6.

Practice Problem Solutions

Problem 12.3: For an n-input NOR gate, we have:

$t_{PLH} = NR_p(C_{outp}/N + N \cdot C_{outn} + C_{load}) + 0.35R_pC_{inp}(N-1)^2$

$t_{PHL} = (R_n/N)(NC_{outn} + C_{outp}/N + C_{load})$

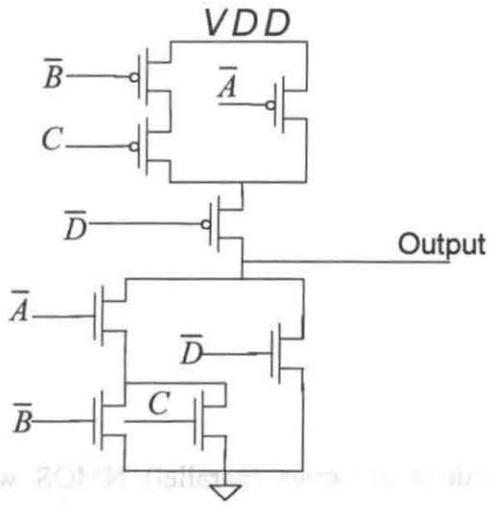
with minimum size MOSFETs, $R_n = 8k\Omega$, $R_p = 24k\Omega$, $C_{outn} = C_{outp} = 4.8fF, C_{inp} = 7.2fF$ for 3 inputs.

a) With $C_{load} = 0$: $t_{PLH} = 3 \times 24k(4.8/3 + 3 \times 4.8 + 0) + 0.35 \times 24k \times 7.2(3-1)^2 = 1.394ns$

$t_{PHL} = (8k/3)(3 \times 4.8 + 4.8/3 + 0) = 42.67ps$

b) $t_{PLH} = 8.594ns$ and $t_{PHL} = 309ps$

Problem 12.6: Assuming minimum size MOSFETs t_{PLH} = 3 x 24k x 50f = 3.6ns while t_{PHL} is 1.2 ns.



Lesson 12 - THE TRANSMISSION GATE

Learning Objectives

After completing this lesson you will be able to:

- Discuss how a transmission gate (TG) operates.
- Determine the design of logic elements, such as path selectors, using the TG.
- Explain how a TG is used in an edge triggered flip flop.

Reading Assignment

Read Chapter 13 in the text.

Video Assignment

Watch the lesson 12 video tutorial.

Key Points

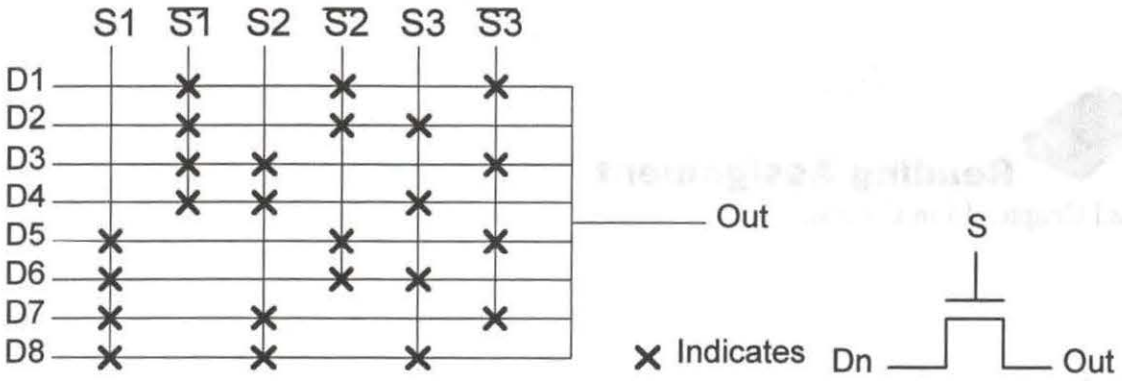
- Using both an n-channel and p-channel switch in parallel will allow passing both a logic high (VDD) and a logic low (0 V).
- The TG can be used in path selector circuits and in a multiplexor/demultiplexor.
- Edge triggered flip-flops rely on the TG to gate input signals between master and slave latches.

Practice Problems

Complete problem 13.4 and describe how the edge triggered flip-flop shown in Figure 13.20 operates.

Practice Problem Solutions

Problem 13.4: The sketch is shown below.



If C_{load} = 50 fF the total delay is (assuming minimum size)

$$t_d = 0.35 \times 2.5 C_{ox} \times R_n \times N^2 + N \times R_n \times C_{load}$$
$$= 0.35 \times 2.5 \times 800\, af/\mu m \times 6\mu m^2 \times 8k \times 9 + 3 \times 8k \times 50\, fF = 1.5\, ns$$

Description of the operation of Fig. 13.20(b): This is a master/slave implementation of a D-FF. When CLK is a low T1 is on, allowing the D input to drive node B. Also when CLK is a low T4 is on, allowing the Q output to circulate in the output or slave latch. When CLK goes high T1 and T4 turn off and T2/T3 turn on. This removes the D input from the master latch and allows point B to drive the output Q. The value of the D input just prior to clock going high is passed to the Q output.

Lesson 13 - DYNAMIC CMOS LOGIC

Learning Objectives

After completing this lesson you will be able to:

- Discuss the fundamentals of dynamic logic.
- Determine why a nonoverlapping clock is needed in some dynamic logic circuits.
- Recognize the different topologies for dynamic logic (e.g., clocked, PE, NP, etc.)

Reading Assignment

Read Chapter 14 in the text.

Video Assignment

Watch the lesson 13 video tutorial.

Key Points

- Dynamic circuits utilize high-impedance (capacitive) nodes to store a charge corresponding to a logic level.
- High-impedance nodes are subject to charge leakage.
- High-speed and very dense logic can be implemented using dynamic circuits.

Practice Problems

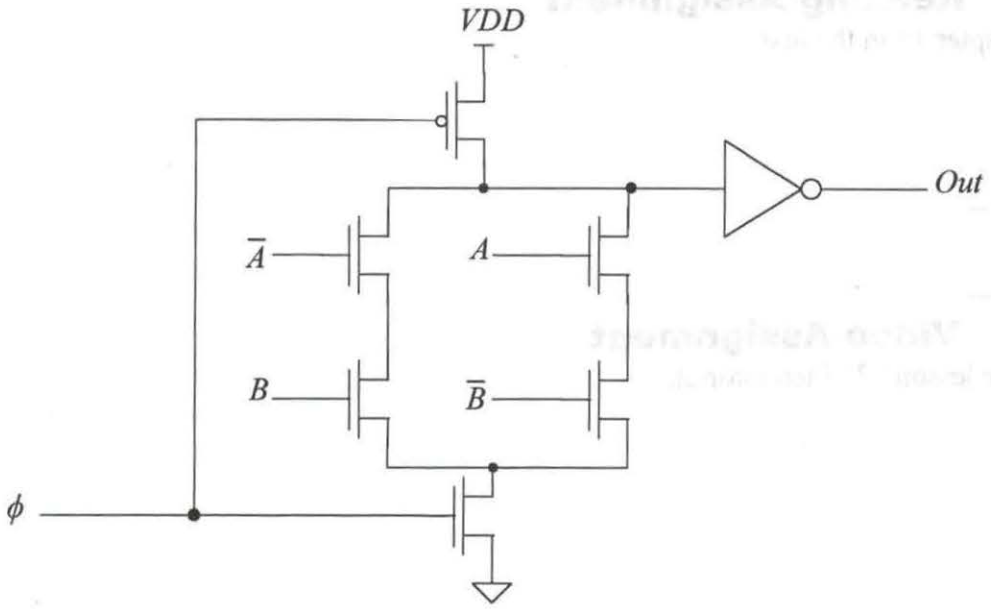
Complete problems 14.5 and 14.6 (without simulation results.)

Practice Problem Solutions

Problem 14.5: Assuming minimum size devices are used (3um/2um) then the worst case t_{PHL} is:

$$t_{PHL} \approx 3 \cdot R_n \times C_{load} = 3 \times 8k \times 50fF = 1.2\,ns$$

Problem 14.6: The schematic of the design is shown below.



Lesson 14 - VLSI LAYOUT

Learning Objectives

After completing this lesson you will be able to:

- Discuss the design of standard cells.
- Recognize example layouts of digital logic.
- Determine bussing considerations when laying out a chip.

Reading Assignment

Read chapter 15 of the textbook.

Video Assignment

Watch the lesson 14 video tutorial.

Key Points

- Reducing die size increases the number of die on a wafer. The yield and profit increase with number of die/wafer.
- Utilizing standard cells can help speed up the time it takes to lay out a chip..
- Bussing can be an important concern when designing a large chip.

Practice Problems

Explain how connections would be made to the MUX/DEMUX layout shown in Fig. 15.15.

Practice Problem Solutions

The connections would be made using metal1 to the n+ active area through a contact. The active area can be thought of as a wire connection. The connection to the A input, for example, would come through the metal1 to a contact and then down to the n+. Note: in order to avoid design rule violations we might have to extend the n+ associated with the A input to the left in this figure.

CMOS

Digital Circuit Design

Final Examination

FINAL EXAM DIRECTIONS

This examination covers the material presented in the Study Guide for "CMOS Digital Circuit Design." This exam is divided into sections which correspond to the Study Guide lessons. It consists of 100 multiple choice questions, each worth 1 point.

A passing grade of 70% is required to receive a Certificate of Achievement from the IEEE. Please take your time, read the questions carefully and then review your answers when you are finished. Record your answers on the perforated answer sheet at the end of the final exam.

This exam is open book, notes, and Study Guide (meaning you can use these as references while taking the exam). Complete and submit the Answer Sheet.

Completed answer sheets may be returned to the IEEE in one of the following ways:

By Mail - send to:

IEEE Education Department
445 Hoes Lane, PO Box 1331
Piscataway, NJ 08855-1331

By Fax - send to "Education" at 732-981-1686

or

By E-mail - send your list of answers along with the appropriate contact information to:
ssc-exam@ieee.org

Note: Unless otherwise stated, use the CN20 process parameters given in Appendix A of the text for the problems in this exam.

GOOD LUCK!

Lesson 1 - An overview of CMOS circuit design

1. Which of the following is connected, via a bonding wire, to a lead frame?

   A. a wafer

   B. a die

   C. plastic encapsulation

   D. probe card

2. Of the following, which occurs first?

   A. cutting the wafer

   B. encapsulating the die

   C. processing the bare wafer

   D. drawing layout

Lesson 2 - The Well

3. The n-well is used mainly for:

   A. The body of the p-channel MOSFETs

   B. Making a bipolar transistor

   C. As a substrate to make CMOS integrated circuits

   D. Making a switch when used with the substrate

4. What is the resistance of an n-well resistor assuming the n-well's sheet resistance is 2,200 ohms per square if the resistor is 5 um wide and 200 um long?

A. 44k

B. 100k

C. 250k

D. 88k

5. Why is sheet resistance used in a CMOS process?

A. Because layout sheets are used to specify how the chip is assembled

B. Because all the layers fabricated have a known thickness.

C. Because it is a technical term that may confuse the novice.

D. Because the field implant changes the resistance of the layout.

6. A depletion layer is formed between:

A. the n-well and the field oxide

B. the p-type substrate and the field oxide

C. the n-well and the p-substrate

D. the diode and the n-well

7. The depletion capacitance of a diode

A. increases with increasing reverse bias across the diode

B. is not a function of the reverse bias across the diode

C. decreases with increasing reverse bias across the diode

D. is not concern in a diode

8. Estimate the delay through a 100k n-well resistor if the zero bias depletion capacitance between the n-well and substrate is 1 pF.

A. 3.5 ns

B. 35 ns

C. 100 ns

D. 700 ns

9. If the p-substrate of a wafer is held at ground potential the minimum voltage an n-well can be held at to avoid substrate injection is

A. -0.6 V

B. 0 V

C. The positive power supply voltage

D. -2 V

10. The n-well mask patterned on a reticle is used to pattern what on the wafer?

A. a resist

B. the field oxide

C. the substrate

D. the implant

Lesson 3 - The Metal Layers

11. Laying out a bonding pad without using the overglass layer would result in:

A. A direct connection to the metal layers.

B. Not making a connection to the bonding pad because of an insulating layer covering the boding pad.

C. Not making a connection between metal1 and metal2.

D. A connection directly to the n-well.

12. Metal1 is closer to the p-substrate so it:

A. is better for routing signals than is metal2.

B. has more resistance than other layers in a CMOS process.

C. has more capacitance to the substrate than does metal2.

D. has more relaxed design rules than does the other layers in a CMOS process.

13. Electromigration can cause erosion in a metal wire and lead to a wire breaking?

A. True

B. False

14. For a long length of metal used to transmit a signal, in general, the

A. electromigration concerns generally set the minimum wire width.

B. the parasitic resistance of the wire sets the minimum wire width.

C. the number vias along the wire sets the width of the wire even if the wire is only connected to circuitry at its ends.

D. the parasitic capacitance sets the wires width.

15. Ground bounce can be described as fluctuations in the voltage on the ground bus as a result of variations in the sheet resistance of the ground conductor.

A. True

B. False

16. Vias are used to make a connection between metal1 and metal2. What sets the number of vias needed to connect a wire of metal1 to a wire of metal2?

A. the area available sets the required number.

B. the size of the n-well that is being connected to sets the number.

C. the coupling between metal1 and metal2 can be reduced by increasing the number of vias.

D. the parasitic contact resistance and electromigration concerns set the minimum number.

Lesson 4 - The Active and Poly Layers

17. Polysilicon is a material that is made up of:

A. silicon drawn with polygons.

B. a p-channel MOSFETs.

C. crystalline silicon made up of unit atoms.

D. small crystalline regions of silicon.

18. A metal1 connection directly to the n-well results in

A. a ohmic contact.

B. a rectifying contact.

C. a connection to n+.

D. a connection to active.

19. A MOSFET is formed by polysilicon over active (n+ or p+).

A. True

B. False

20. Active areas define openings in the field oxide where:

A. an implant (n+ or p+) can penetrate into the substrate.

B. metal can be laid out to block MOSFET formation.

C. polysilicon can be doped n+ or p+.

D. a standard cell frame can be placed.

21. Lateral diffusion affects the width and length of a MOSFET.

A. True

B. False

22. Oxide encroachment has the effect of reducing the MOSFETs:

A. length.

B. opening in the field oxide.

C. width.

D. width and length.

23. The sheet resistance of the n+ layer is less than the sheet resistance of the n-well because:

A. the n-well is thicker than the n+ layer.

B. the n-well is doped lighter than the n+ layer.

C. the n+ layer has more free electrons than the n-well layer.

D. the substrate doesn't affect the n+ layer as much as it does the n-well layer.

24. The n+ to substrate depletion capacitance is made up of:

A. a bottom capacitance.

B. a bottom and top capacitance.

C. a bottom and sidewall capacitance.

D. a bottom, sidewall and top capacitance.

25. If the potential between an n+ implant is raised with respect to the substrate the depletion capacitance goes down because the depletion layer width between the n+ and substrate increases.

A. True

B. False

26. What determines the width and length of an n-channel MOSFET?

A. The size of the n+ area.

B. The size of the polysilicon.

C. The intersection of polysilicon and n+.

D. The product of the areas of the polysilicon and n+.

27. A resistor can be made with p+ if

A. the p+ resistor is laid out in an n-well so that the p+ is isolated from the p-substrate.

B. the p+ resistor is laid out next to an n+ resistor.

C. the p+ resistor is used with n+ connections to metal1.

D. the p+ resistor is laid out next to an n-well.

28. Polysilicon is considered an active layer.

A. True

B. False

29. The area of an n+ implant is to the bottom capacitance as the perimeter of an n+ implant is

A. to the depletion capacitance.

B. total resistance of the implant.

C. grading of the implant.

D. the sidewall capacitance.

30. Which one of the following is not a reason to use a standard cell frame.

A. It provides substrate and well connections.

B. It conveniently routes power and ground through the circuit.

C. It provides a well-defined location to put n- and p-channel MOSFETs.

D. It is a well known standard required in most CMOS processes.

Lesson 5 - The MOSFET as a Capacitor

31. When an n-channel MOSFET is operating in the "accumulation region"

A. holes are accumulated at the oxide-semiconductor interface.

B. electrons are accumulated at the oxide-semiconductor interface.

C. the MOSFET is in the strong inversion region.

D. the carriers at the oxide-semiconductor interface have a net negative charge.

32. When a MOSFET is operating in the accumulation region it can also be said that the MOSFET is operating in

A. weak inversion.

B. moderate inversion.

C. strong inversion.

D. a region where the surface is not inverted.

33. A natural MOSFET capacitor is formed by poly over n+ in an n-well.

A. True

B. False

34. The oxide capacitance is set by:

A. the oxide thickness.

B. the lateral diffusion.

C. the oxide encroachment.

D. the applied gate to source potential.

35. Strong inversion occurs in an n-channel MOSFET because:

A. electrons from the substrate are repelled by a large gate to source voltage.

B. holes in the substrate are attracted under the gate.

C. a channel of electrons is formed deep in the substrate.

D. a voltage greater than the threshold voltage is applied between the gate and source which attracts electrons under the gate oxide.

36. The threshold voltage can be defined as the voltage at which a noticeable amount of current begins to flow in a MOSFET with a non zero drain to source potential.

A. True

B. False

37. The threshold voltage can also be defined as the voltage at which the surface electrostatic potential, at the oxide semiconductor interface, is the same potential as the substrates electrostatic potential.

A. True

B. False

38. The contact potentials between the gate and substrate in an MOS system result in:

A. a voltage generator useful for powering circuitry on-chip.

B. a potential that must be overcome in order to invert the MOSFET's channel.

C. metal1 to metal1 shorting.

D. changes in the bulk, or substrate, electrostatic potential.

39. The source and drain depletion capacitances have:

A. no practical effect on the threshold voltage of the device.

B. have a small effect on the threshold voltage resulting from the added doping atoms close to the channel.

C. result in a change in the device's contact potential.

D. change the requirements used to define threshold voltage.

40. When a MOSFET is used as a capacitor, while operating in the strong inversion region, the lateral diffusion has no effect on the value of the capacitance.

A. True

B. False

Lesson 6 - The MOSFET

41. When the MOSFET operates in the triode region the inverted channel under the gate oxide extends from:

A. The source to the edge of the depletion region.

B. The drain to the substrate.

C. The source to the drain.

D. The source to the substrate.

42. When the MOSFET enters the saturation region:

A. The available charge in the inverted channel becomes zero at the drain/channel interface.

B. The charge in the inverted channel becomes zero at all points under the gate.

C. The threshold voltage increases resulting in a "flattening out" of drain current.

D. The sheet resistance decreases because the mobility is changing.

43. The level of gate to source potential required to make an n-channel MOSFET enter the saturation region is $V_{DS} + V_{THN}$ assuming

A. the MOSFET is conducting a significant current.

B. $V_{GS} > V_{THN}$

C. the amount needed to overcome the contact potential.

D. the oxide thickness doesn't vary while the circuit is operating.

44. Channel length modulation is caused by the electrical channel length changing with applied drain to source potential resulting in a change in the MOSFETs drain current.

A. True

B. False

45. Varying the applied V_{GS} to an n-channel MOSFET modulates the MOSFETs channel resistance, i.e. changes the resistivity of the inverted channel.

A. True

B. False

46. The hole's mobility is larger than the electron's mobility since the hole is in the valence band and the electron is in the conduction band.

A. True

B. False

47. The units of the transconductance parameter $\mu A/V^2$, KP, are the same as the units of the transconductance parameter β.

A. True

B. False

Lesson 7 - The Short Channel MOSFET

48. Short channel effects are caused by:

A. reducing the MOSFET's L

B. the carrier velocity saturating

C. the electric field becoming too large between the MOSFETs drain and the inverted channel.

D. all of the above.

49. An LDD MOSFET is used to reduce hot carrier effects.

A. True

B. False

50. Scaling CMOS processes is common because

A. it allows the process designer to scale the process without re-engineering any steps.

B. it tells the designer everything he/she needs to know about the next process.

C. it allows, with little additional design, digital cells to be used in smaller more modern processes.

D. none of the above

51. Active power is significantly reduced as the process is scaled.

A. True

B. False

52. The drain current for a modern MOSFET changes with the square of the gate-source voltage.

A. True

B. False

Lesson 8 - The Digital Model of a MOSFET

53. When the gate of an n-channel MOSFET is at 0V and its source is connected to ground we think of the MOSFET as:

A. a resistor.

B. a switching resistance of value R_n.

C. an open switch.

D. a floating variable resistance.

54. When the gate of a p-channel MOSFET is at 0V and its source is connected to VDD we think of the MOSFET as:

A. a resistor.

B. a switching resistance of value R_n.

C. an open switch.

D. a floating variable resistance.

55. When the gate of an n-channel MOSFET is at VDD and its source is connected to ground we think of the MOSFET as:

A. off device.

B. a switching resistance of value R_n.

C. an open switch.

D. a floating variable resistance.

56. The MOSFET input capacitance is $(3/2)C_{ox}$ because the voltage across the gate-drain capacitance changes by 2VDD and:

A. The gate-drain capacitance is $C_{ox}/2$.

B. The gate-drain capacitance is $C_{ox}/2$ resulting in a net input charge of C_{ox}VDD.

C. The gate-drain capacitance is $C_{ox}/2$ resulting in an input charge of C_{ox}VDD to the gate drain capacitance. This added to the charge required by the gate-source capacitance (also $C_{ox}/2$) results in a total charge of $(3/2)C_{ox}$VDD.

D. None of the above.

57. An n-channel MOSFET passes a logic "1"

A. as a logic "1".

B. as a logic "1" with a threshold voltage drop of V_{THN}.

C. as a logic "0" with a threshold voltage increase of V_{THP}.

D. as a logic "0".

58. A p-channel MOSFET passes a logic "0"

A. as a logic "1".

B. as a logic "1" with a threshold voltage drop of V_{THN}.

C. as a logic "0" with a threshold voltage increase of V_{THP}.

D. as a logic "0".

59. A p-channel MOSFET passes a logic "1"

A. as a logic "1".

B. as a logic "1" with a threshold voltage drop of V_{THP}.

C. as a logic "0" with a threshold voltage increase of V_{THP}.

D. as a logic "0".

60. The process characteristic time constant represents how fast a MOSFET can discharge its own capacitances.

A. True

B. False

Lesson 9 - Inverter Operation I

61. A p-channel MOSFET is used to pull the output voltage of an inverter down to ground while the n-channel MOSFET is used to pull the output voltage of an inverter up to VDD.

A. True

B. False

62. The switching point voltage is defined as:

A. the input voltage that causes current to flow in both MOSFETs used in the inverter.

B. the voltage levels at the input of the inverter and the output of the inverter are the same.

C. the point on the inverters transfer curve where the MOSFETs are sized the same.

D. the point on the inverter when both MOSFETs are off.

63. The resistance of the p-channel is larger than the resistance of a same size n-channel because:

A. the oxide thickness of the p-channel is larger than the oxide thickness of the n-channel.

B. the threshold voltage of the p-channel is larger than that of the n-channel.

C. the mobility of the hole is larger than the mobility of the electron.

D. the mobility of the electron is larger than the mobility of the hole.

64. A ring oscillator has a frequency that is dependent on the:

A. number of inverters used in the ring.

B. oxide thickness of the MOSFETs.

C. the length of the MOSFETs used in the ring oscillator.

D. all of the above.

65. The power dissipation of an inverter that is not changing states is practically zero.

A. True

B. False

66. The power delay product is a function of

A. operating frequency.

B. power supply voltage.

C. oxide thickness

D. all of the above.

67. Latch-up can occur in an n-channel MOSFET by itself.

A. True

B. False

Lesson 10 - Inverter Operation II

68. It is always true that one inverter has less delay than three inverters.

A. True

B. False

69. It is a bad idea to connect on-chip logic directly off-chip because:

A. the large off-chip capacitance loads the on-chip logic resulting in large delays.

B. on-chip logic has too much drive capability resulting in a waste of power.

C. on-chip logic is made from special MOSFETs in an on-chip process that can't drive off chip loads. We must use a buffer process to drive loads off-chip.

D. it is too fast to drive off-chip loads.

70. What is the benefit of using an NMOS inverter over a CMOS inverter?

A. better noise margins.

B. better pull-up capability.

C. lower input capacitance and no latch-up.

D. better static power dissipation.

71. A tristate output inverter can have three possible output states.

A. True

B. False

72. A bootstrapped inverter has better output voltage swing than a simple NMOS inverter under all possible operating conditions.

A. True

B. False

Lesson 11 - Static Logic Gates

73. Logic gates in CMOS are called complimentary because:

A. NOR gates are the compliment of NAND gates.

B. inverters are used to make logic gates.

C. if a series connection of n-channel MOSFETs is used then a parallel connection of p-channel MOSFETs should also be used when implementing static logic.

D. None of the above are correct.

74. NAND gates are preferred in CMOS because:

A. they are useful in implementing logic.

B. the mobility of the electron is greater than the mobility of the hole.

C. they are not preferred, NOR gates are preferred.

D. they have slower transitions than NOR gates.

75. The largest number of inputs that we can design a NAND to have is three, although two input NANDs are the most common.

A. True

B. False

76. Charging or discharging a load capacitance through a string of MOSFETs can lead to RC transmission line delays.

A. True

B. False

77. When designing a gate with a large number of inputs using complimentary logic can result in a gate with too many MOSFETs and very slow transition times. Often to circumvent these problems a pull-up transistor which acts like a resistor can be used.

A. True

B. False

78. Complex CMOS logic gates can be used:

A. to implement an and-or-invert logic equation with a single gate.

B. to implement logic more efficiently and with less delay than using NANDs, NORs and inverters.

C. to implement an exclusive OR gate.

D. all of the above.

79. Cascode Voltage Switch Logic can be used when:

A. fully differential outputs are needed.

B. slower switching times are needed.

C. only p-channel MOSFETs can be used.

D. only n-channel MOSFETs can be used.

80. Static logic dissipates little static or dynamic power.

A. True

B. False

Lesson 12 - The Transmission Gate

81. The benefit of using a TG over a p-channel or n-channel pass transistor alone is:

A. the added control signals required.

B. the increased layout area.

C. the TG will pass a logic 1 or 0 without a voltage drop or increase.

D. the resistance of the TG is greater than the n- or p-channel pass transistor alone.

82. Using a TG made with minimum size MOSFETs results in more effective digital resistance then using a p-channel or n-channel pass transistor alone.

A. True

B. False

83. A TG fabricated in an n-well process requires an n-well for the p-channel MOSFET.

A. True

B. False

84. A TG can be used in a:

A. path selector.

B. multiplexor or demultiplexor.

C. decoder.

D. all of the above.

85. Static gates can be implemented using TGs.

A. True

B. False

86. A latch is made with:

A. a TG.

B. a pass transistor.

C. two inverters and at least one TG.

D. an NAND gate.

87. Design of an edge triggered flip-flop (FF) requires a master FF and a slave FF.

A. True

B. False

88. When using a TG a logic high applied to the gates of the MOSFETs used in the TG will allow the TG to turn fully on passing a logic high or low without a voltage drop or increase.

A. True

B. False

89. The hold time is:

A. the time the clock must be held off before it is applied to a flip-flop.

B. the time the data input to a flip-flop must be held after the clocking edge occurs.

C. the time the data input must be held valid before the clocking edge occurs.

D. the time the clock edge must not be present before the D input changes.

90. The setup time is:

A. the time the clock must be setup before it is applied to a flip-flop.

B. the time the data input to a flip-flop must be present before the clocking edge occurs.

C. the time the data input must be absent before the clocking edge occurs.

D. the time the clock edge must not be present before the D input changes.

Lesson 13 - Dynamic CMOS Logic

91. A dynamic CMOS circuit is one that:

A. relies heavily on static CMOS logic.

B. stores charge on the output of a static logic gate.

C. uses charge leakage to store a logic level.

D. uses a capacitive node to store a logic level.

92. High-impedance nodes are subject to charge leakage which may result in loss of information.

A. True

B. False

93. A nonoverlapping clock is used in dynamic circuits to:

A. keep from transferring charge from one node to several nodes at the same time.

B. to provide added complexity in the clocking scheme.

C. to regenerate logic levels.

D. all of the above.

94. Clocked CMOS logic requires a nonoverlapping clock generator.

A. True

B. False

95. Dynamic logic can result in smaller layout area and faster operation.

A. True

B. False

Lesson 14 - VLSI Layout

96. The benefit of reducing the size of a die is that it will ultimately increase the yield of a part.

A. True

B. False

97. The location of the inputs of a standard cell

A. is somewhat arbitrary.

B. is important for yield reasons.

C. is important for routing reasons.

D. isn't important.

98. The height of a standard cell is variable while the width is fixed.

A. True

B. False

99. Stick diagrams are useful when doing layout because:

A. the sticks resemble a stick man.

B. the sticks help identify layout problems before layout is actually started.

C. layout is not challenging unless the sticks are used.

D. they eliminate the different combinations of layout solutions possible.

100. Custom layout results, in general, in getting a tighter layout than possible using standard cells.

A. True

B. False

Answer Sheet

CMOS DIGITAL CIRCUIT DESIGN

NAME_____
ADDRESS_____
CITY_____STATE/PROV_____POSTAL CODE_____
DATE_____

INSTRUCTIONS

1. Read each question in the Final Examination and select the correct answer. Place a check adjacent to your answer.
2. Using a pencil, circle the letter corresponding to your answer choice. Be careful in transferring your answer. If you should circle the wrong choice, erase your mark completely. Double check this answer sheet against your choices on the Final Examination.
3. Fill in the remainder of this answer sheet. Write your complete name and address in the spaces provided. Sign the exam in the space provided at the end of the Examination Answer Sheet.
4. Make a copy of this answer sheet for your records.
5. Return this answer sheet to IEEE by Mail, Fax or Internet (ssc-exam@ieee.org). If submitting by internet, please remember to provide your full name and mailing address.

1.	A	B	C	D	26.	A	B	C	D	51.	A	B			76.	A	B		
2.	A	B	C	D	27.	A	B	C	D	52.	A	B			77.	A	B		
3.	A	B	C	D	28.	A	B			53.	A	B	C	D	78.	A	B	C	D
4.	A	B	C	D	29.	A	B	C	D	54.	A	B	C	D	79.	A	B	C	D
5.	A	B	C	D	30.	A	B	C	D	55.	A	B	C	D	80.	A	B		
6.	A	B	C	D	31.	A	B	C	D	56.	A	B	C	D	81.	A	B	C	D
7.	A	B	C	D	32.	A	B	C	D	57.	A	B	C	D	82.	A	B		
8.	A	B	C	D	33.	A	B			58.	A	B	C	D	83.	A	B		
9.	A	B	C	D	34.	A	B	C	D	59.	A	B	C	D	84.	A	B	C	D
10.	A	B	C	D	35.	A	B	C	D	60.	A	B			85.	A	B		
11.	A	B	C	D	36.	A	B			61.	A	B			86.	A	B	C	D
12.	A	B	C	D	37.	A	B			62.	A	B	C	D	87.	A	B		
13.	A	B			38.	A	B	C	D	63.	A	B	C	D	88.	A	B		
14.	A	B	C	D	39.	A	B	C	D	64.	A	B	C	D	89.	A	B	C	D
15.	A	B			40.	A	B			65.	A	B			90.	A	B	C	D
16.	A	B	C	D	41.	A	B	C	D	66.	A	B	C	D	91.	A	B	C	D
17.	A	B	C	D	42.	A	B	C	D	67.	A	B			92.	A	B		
18.	A	B	C	D	43.	A	B	C	D	68.	A	B			93.	A	B	C	D
19.	A	B			44.	A	B			69.	A	B	C	D	94.	A	B		
20.	A	B	C	D	45.	A	B			70.	A	B	C	D	95.	A	B		
21.	A	B			46.	A	B			71.	A	B			96.	A	B		
22.	A	B	C	D	47.	A	B			72.	A	B			97.	A	B	C	D
23.	A	B	C	D	48.	A	B	C	D	73.	A	B	C	D	98.	A	B		
24.	A	B	C	D	49.	A	B			74.	A	B	C	D	99.	A	B	C	D
25.	A	B			50.	A	B	C	D	75.	A	B			100.	A	B		

SIGNATURE_____