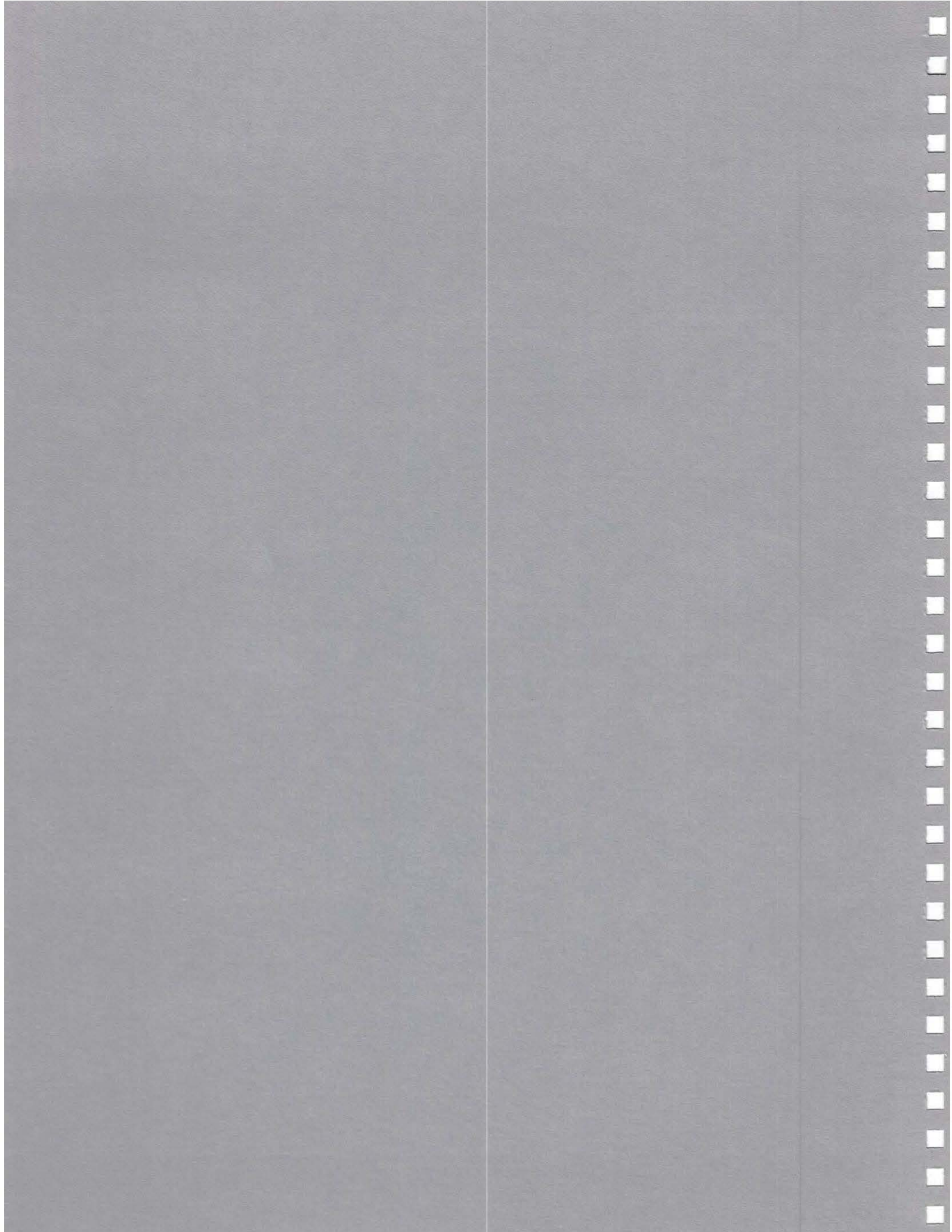


# CMOS

## Analog Circuit Design

Developed by  
R. Jacob Baker  
*University of Idaho*

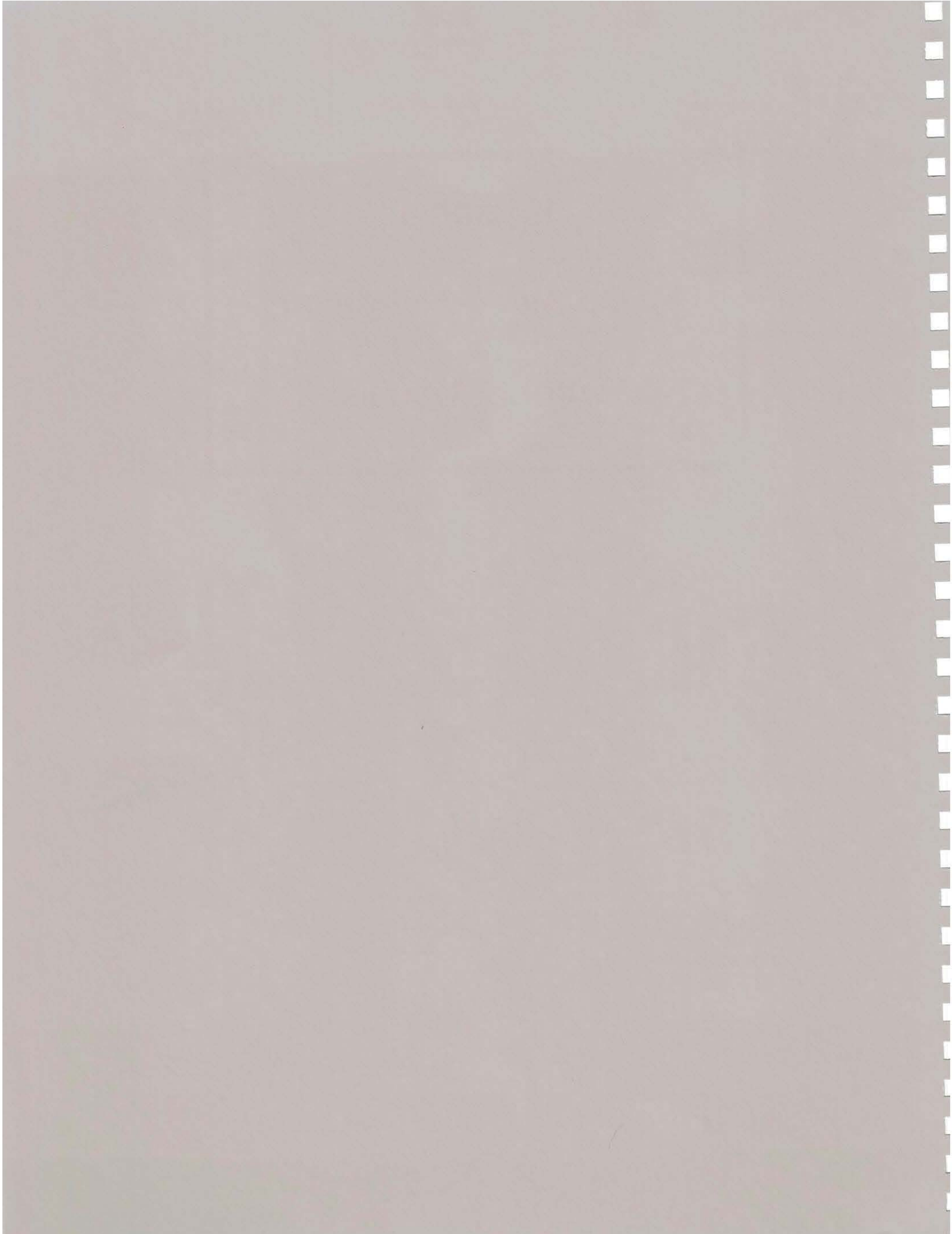
Video Tutorial Hardcopy Visuals



Lesson 1

CMOS Analog Modeling

Tutorial Visuals



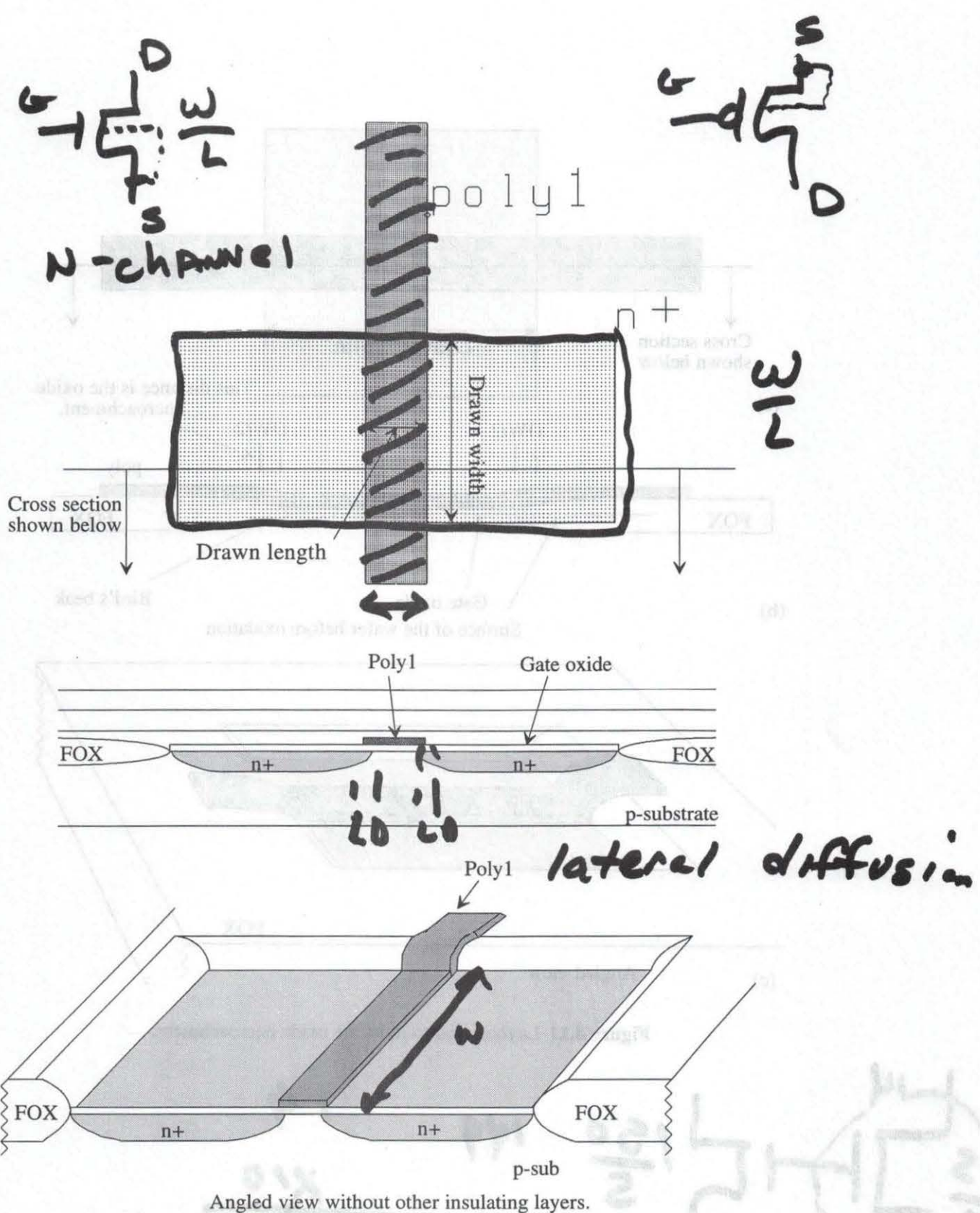


Figure 4.8 Layout of a MOSFET, cross-sectional and angled view.

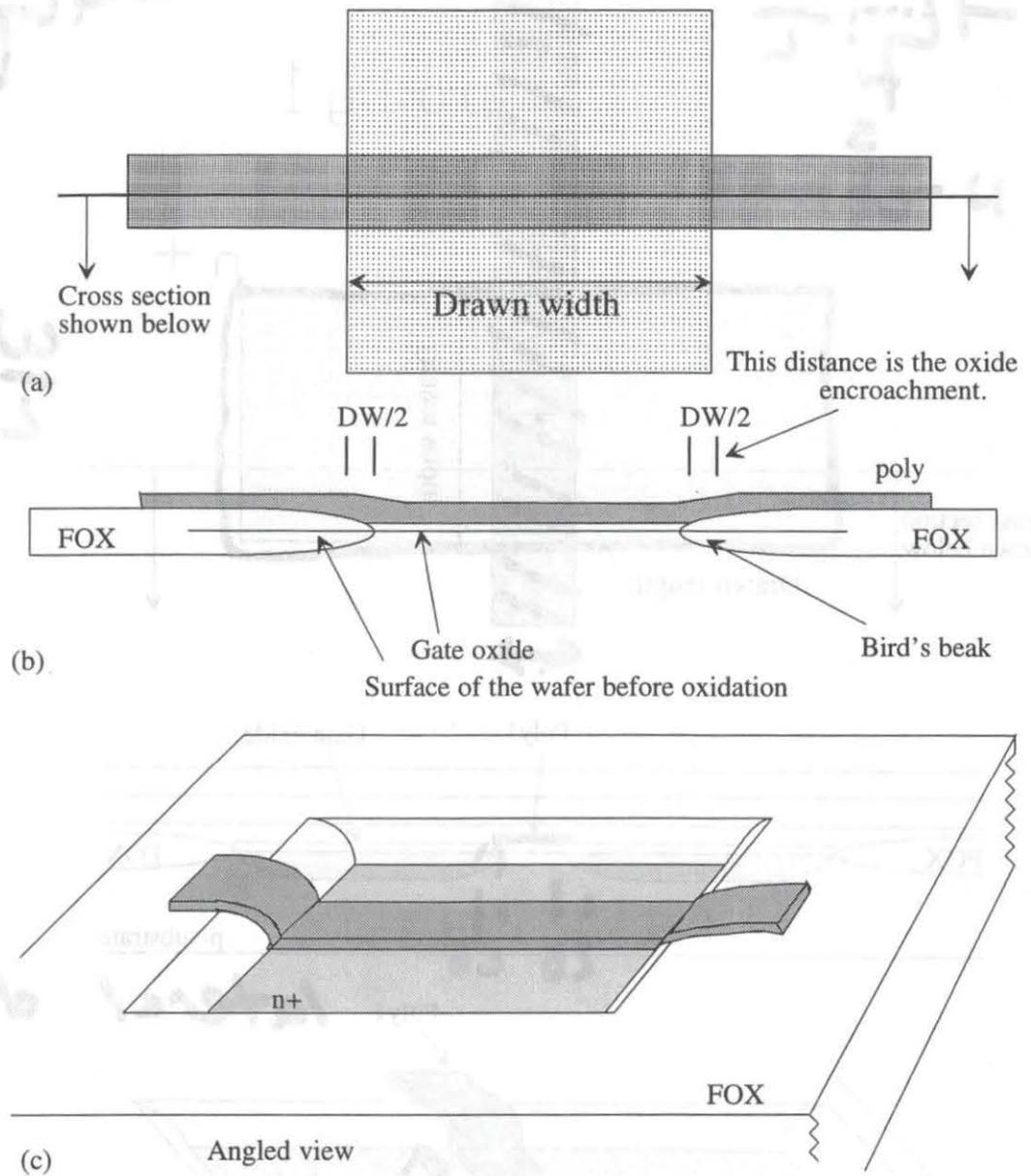
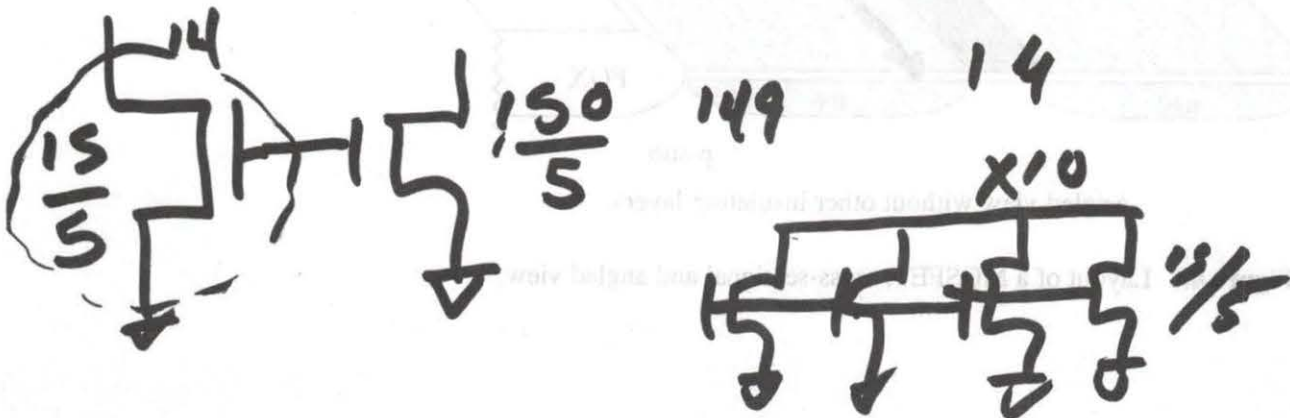
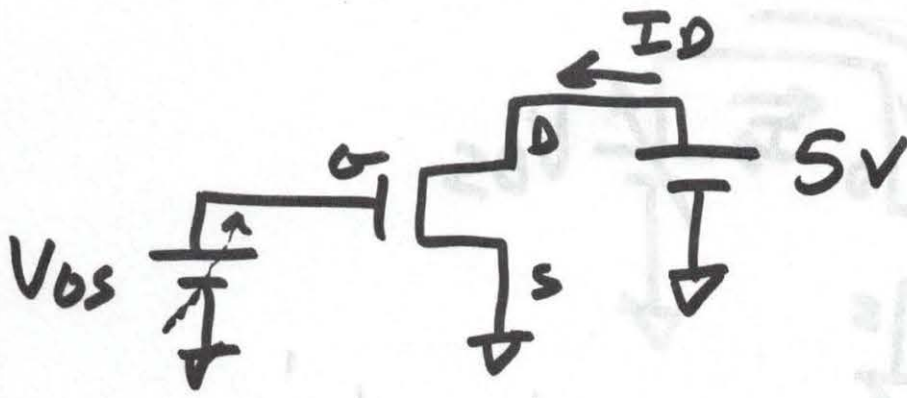


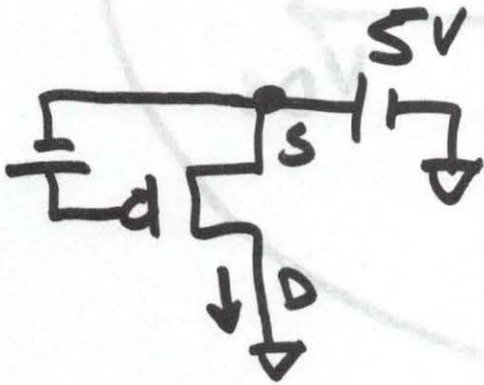
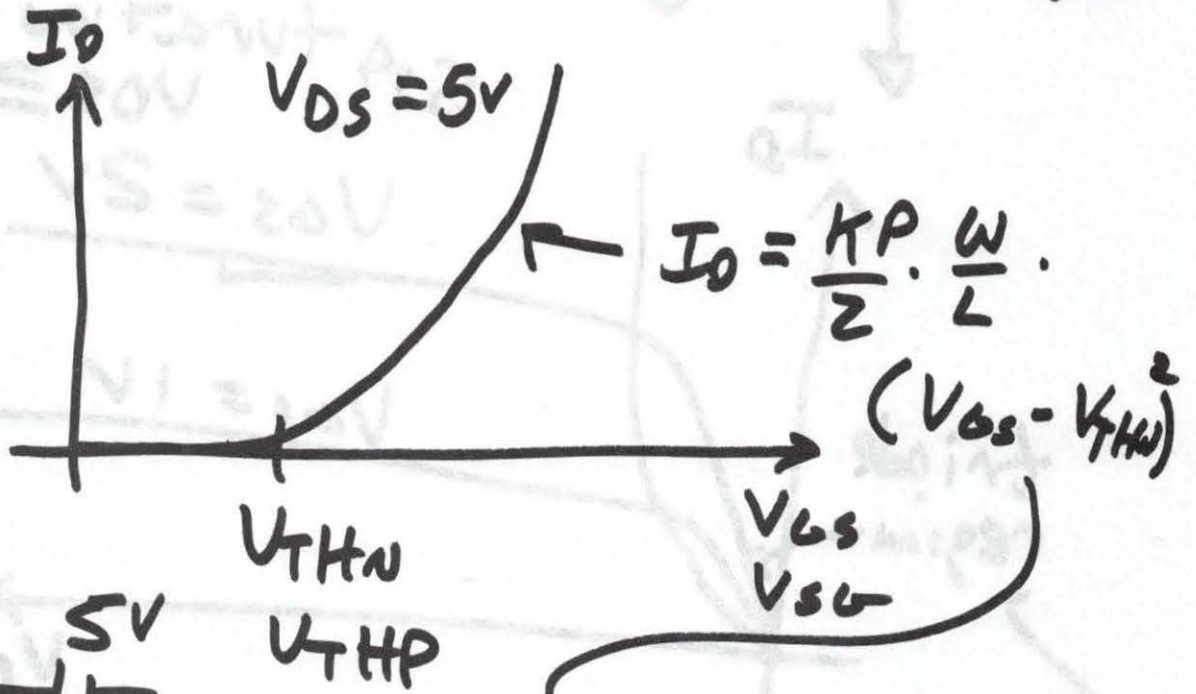
Figure 4.11 Layout used to illustrate oxide encroachment.





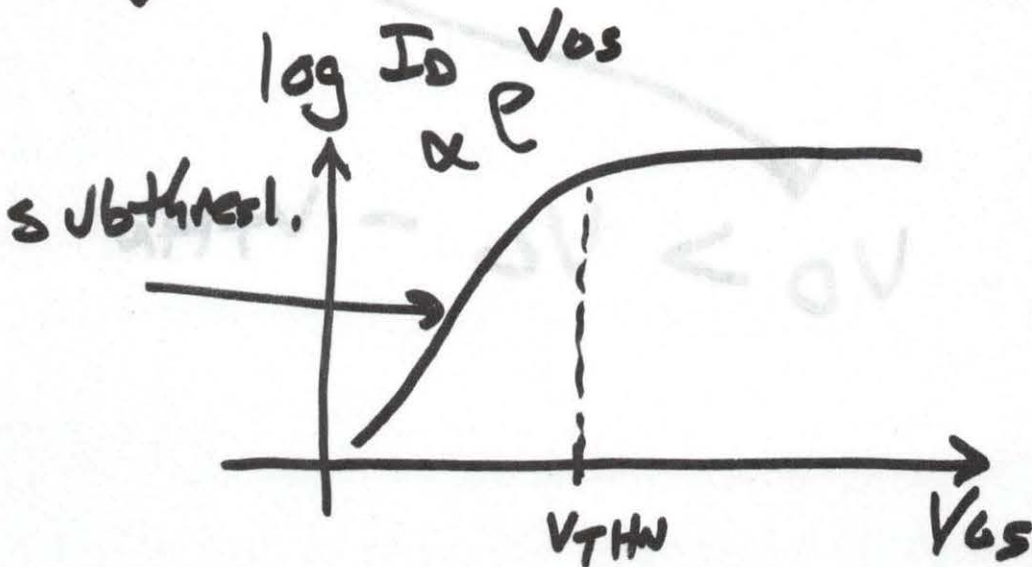
$$K_{PN} = \frac{50 \mu A}{V^2}$$

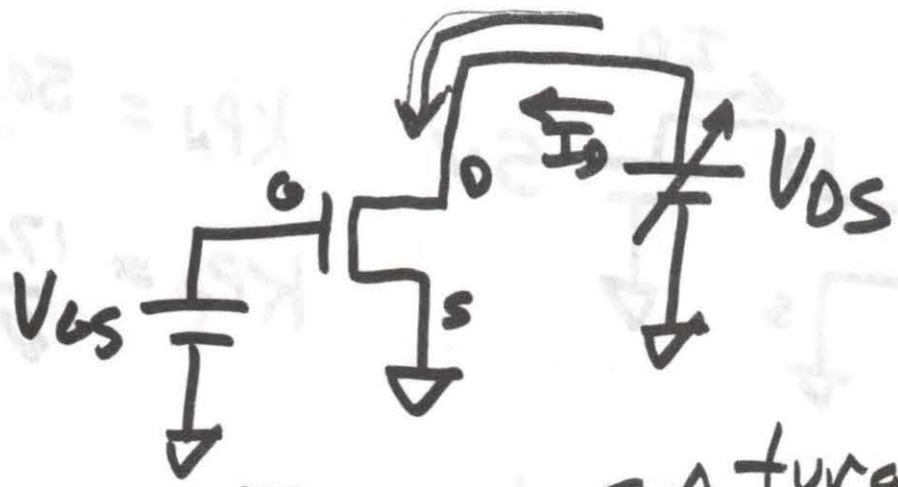
$$K_{PP} = \frac{174 \mu A}{V^2}$$



$$V_{GS} \geq V_{THN}$$

$$V_{DS} \geq V_{GS} - V_{THN}$$





SATURATION  
 $V_{DS} \cong V_{GS} - V_{THN}$

$V_{GS} = 2V$

$V_{GS} = 1V$

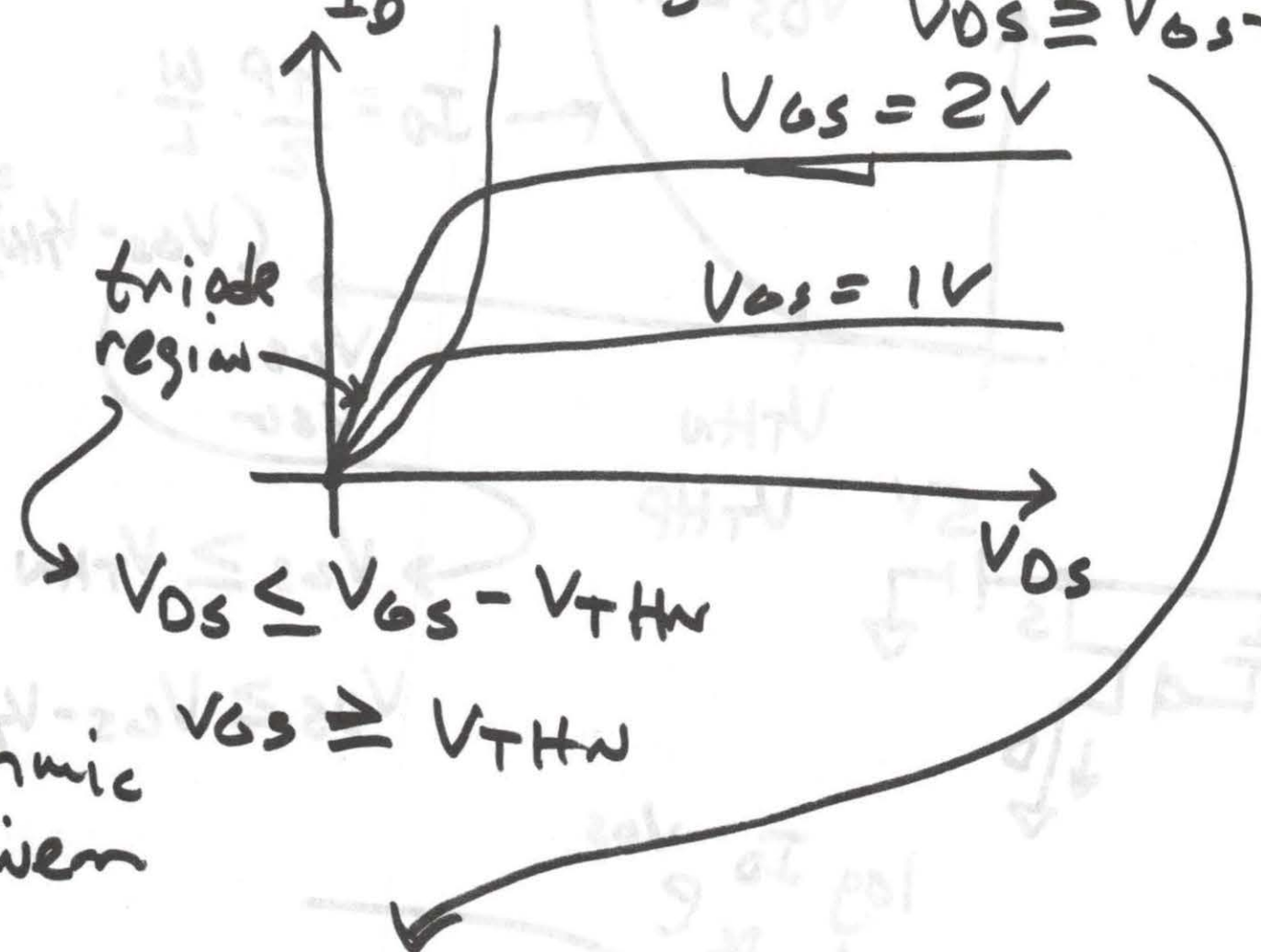
triode region

$V_{DS} \leq V_{GS} - V_{THN}$

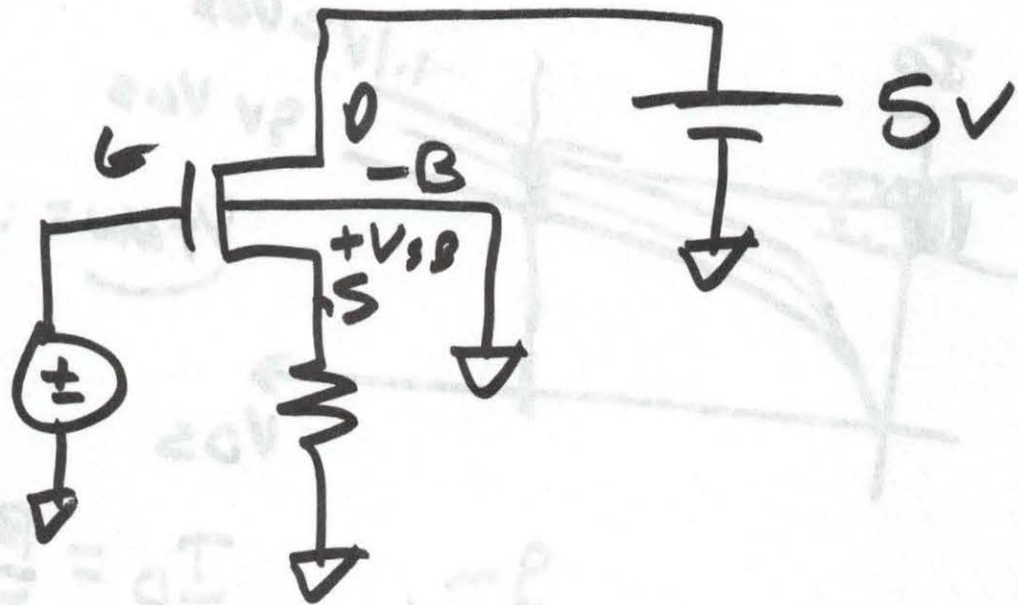
$V_{GS} \geq V_{THN}$

ohmic  
 linear

$V_{DS} > V_{GS} - V_{THN}$



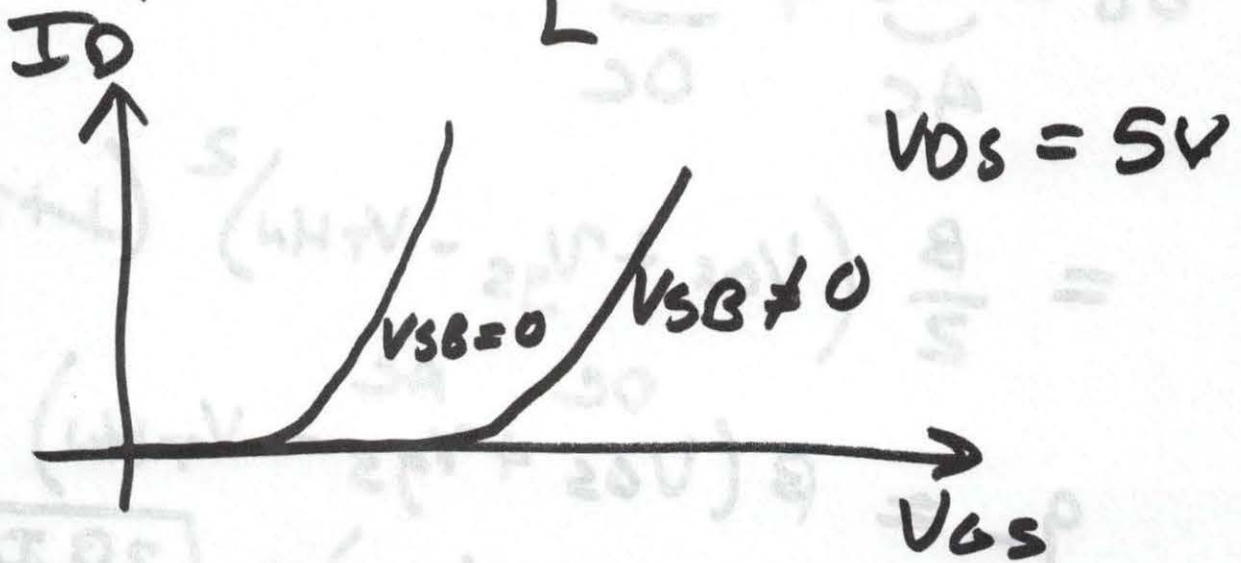


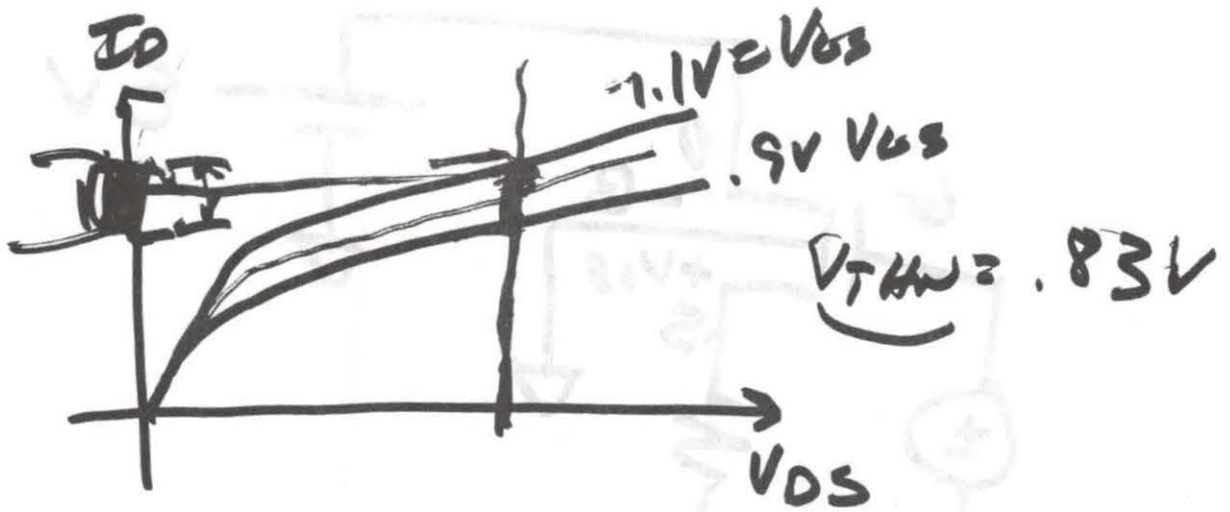


Body effect - causes the  $V_{THN}$  to change.

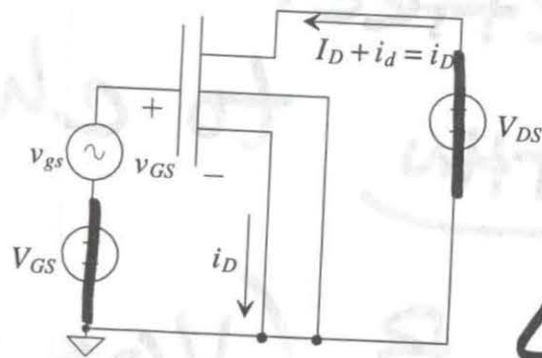
$$I_D = \frac{\beta}{2} (V_{GS} - V_{THN})^2$$

$$\beta = \kappa_P \cdot \frac{W}{L}$$





$$g_m \quad I_D = \frac{\beta}{2} (V_{GS} - V_{THN})^2$$



$$g_m = \frac{dI_D}{dV_{GS}}$$

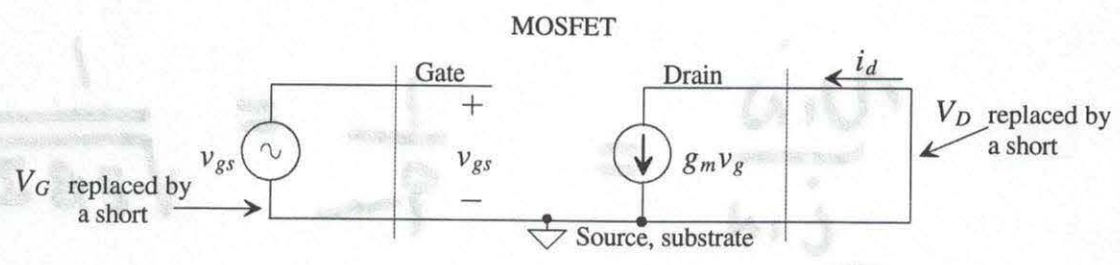
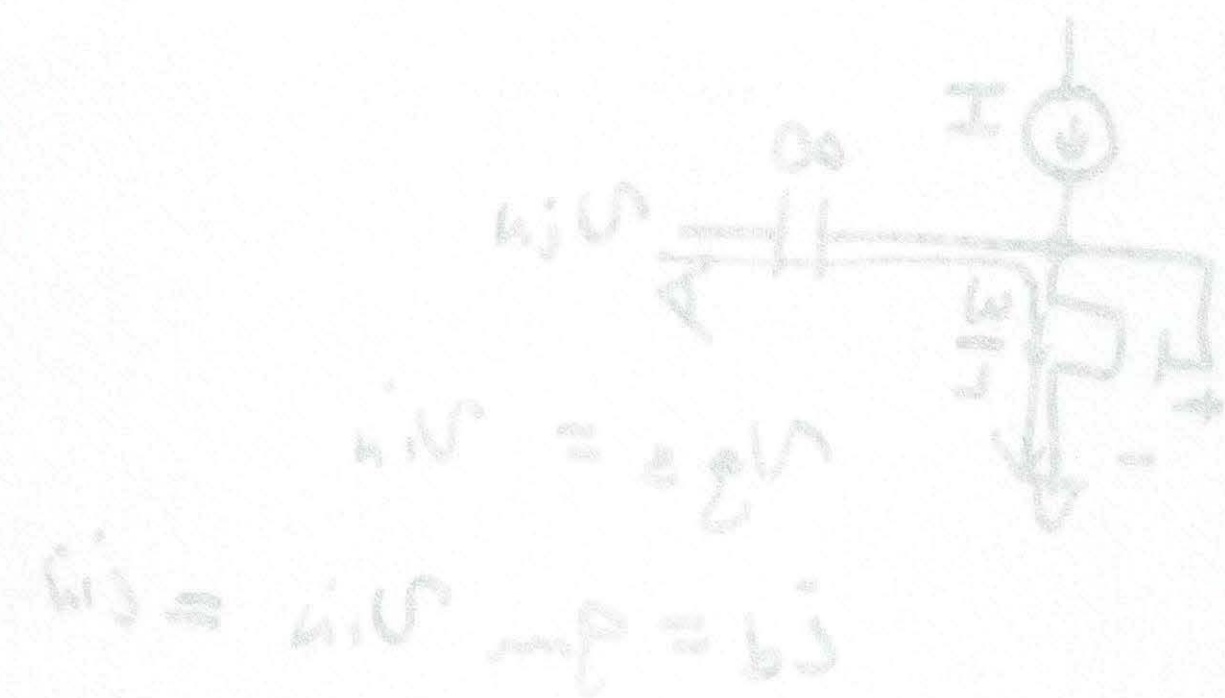
Figure 9.1 Circuit used to determine the forward transconductance.

$$i_D = \underbrace{i_d}_{AC} + \underbrace{I_D}_{DC}$$

$$= \frac{\beta}{2} (V_{GS} + v_{gs} - V_{THN})^2 \quad \left( \frac{d}{dV_{GS}} \right)$$

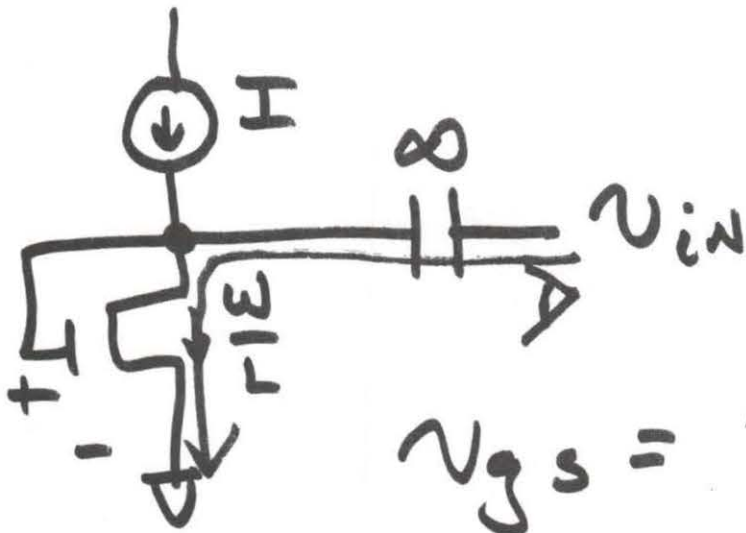
$$g_m = \beta (V_{GS} + v_{gs} - V_{THN})$$

$$g_m = \beta (V_{GS} - V_{THN}) = \sqrt{2\beta I_D}$$



**Figure 9.2** Small-signal model of the circuit in Fig. 9.1.

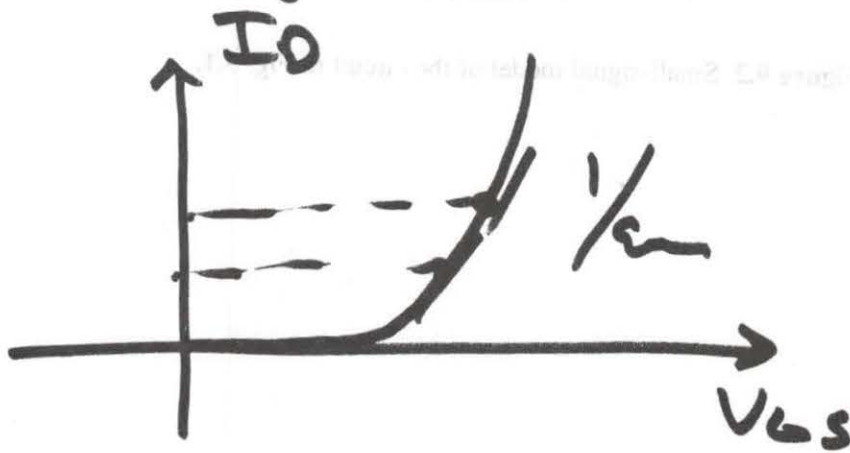




$$v_{gs} = v_{in}$$

$$i_d = g_m v_{in} = i_{in}$$

$$\frac{v_{in}}{i_{in}} = \frac{1}{g_m} = \frac{1}{\sqrt{2\beta I_D}}$$



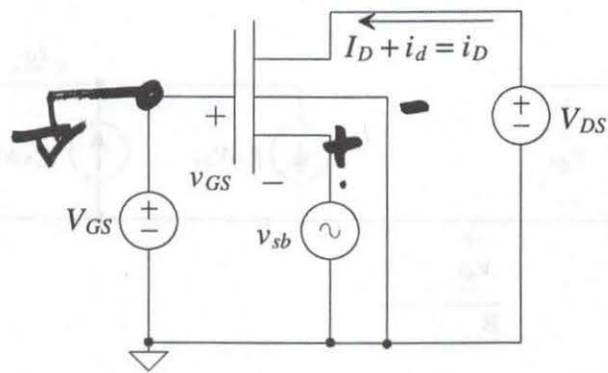
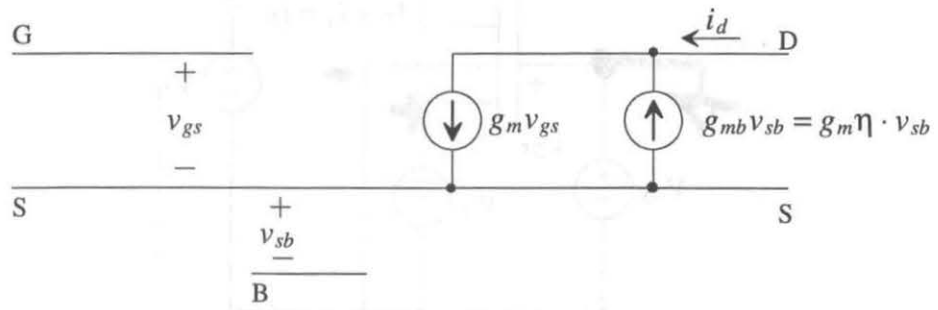


Figure 9.3 Circuit used to determine the body-source transconductance.

$$i_d = g_{mb} \cdot v_{sb}$$

$$g_{mb} = g_m \cdot \eta$$



**Figure 9.4** Small-signal MOSFET with body-effect current source.

$\frac{d^2V}{dV} \cdot dV = bV$   
 $\frac{dV}{dV} \cdot dV = dV$

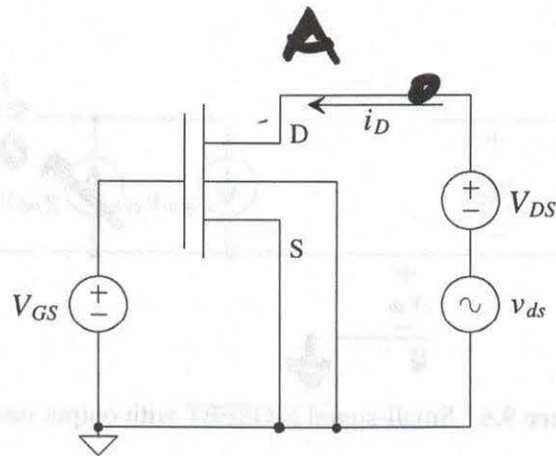
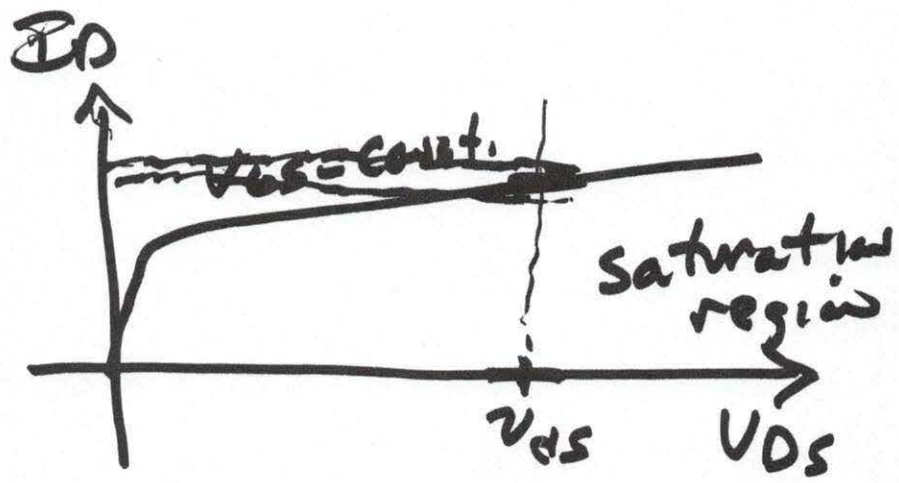
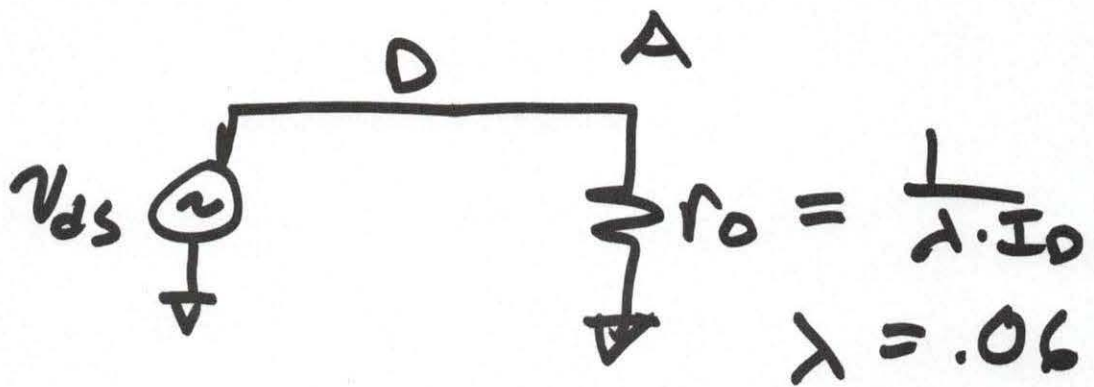


Figure 9.5 Circuit used to determine output resistance of the MOSFET.



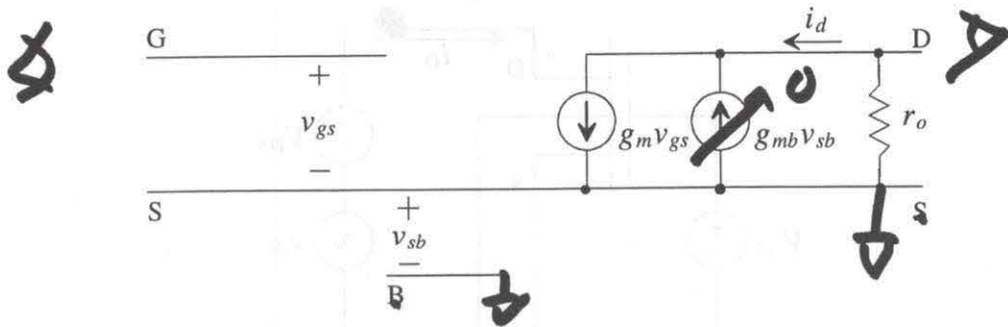
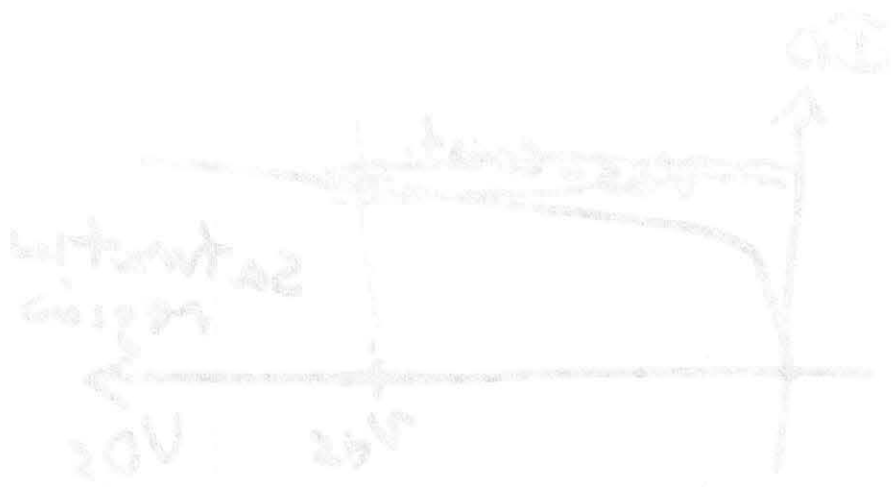
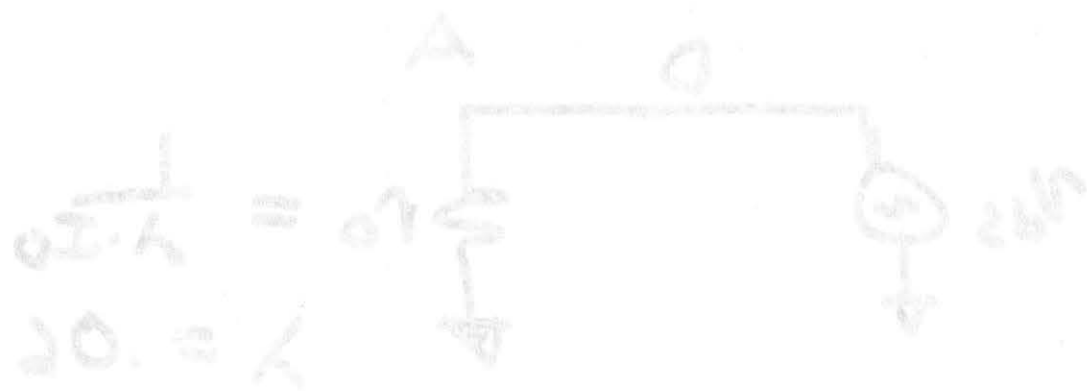


Figure 9.6 Small-signal MOSFET with output resistance.

Figure 9.6 Small-signal MOSFET with output resistance.





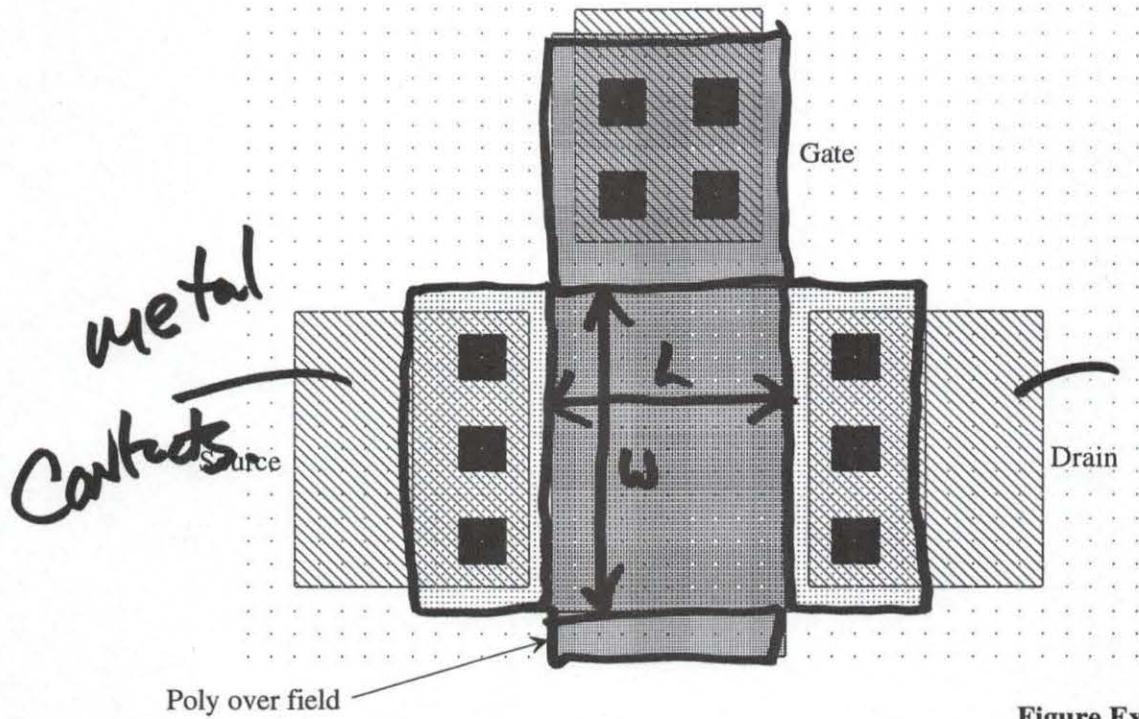
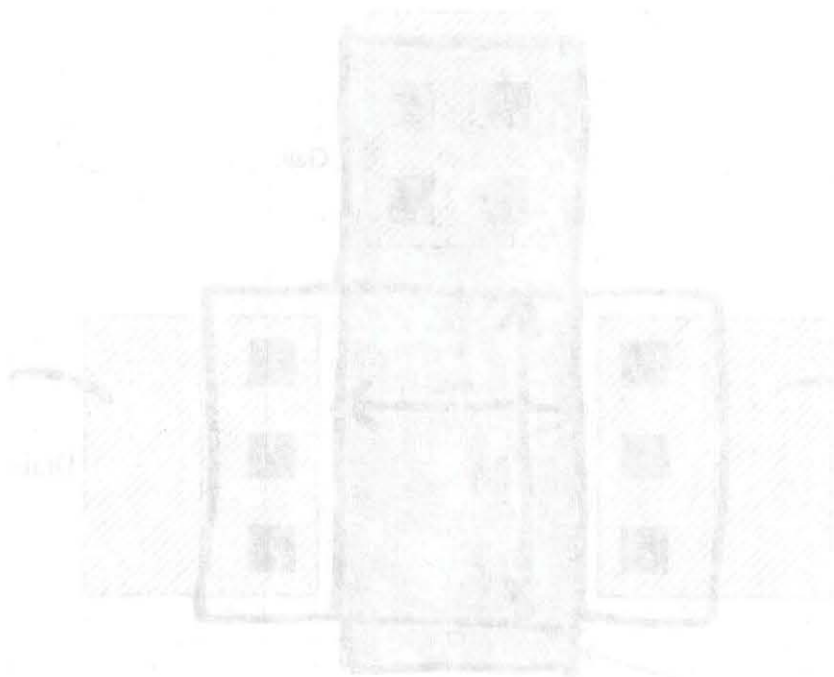


Figure Ex9.3



Handwritten text, possibly a name or label, written in cursive. It appears to say "Catherine" and "10/24/11".

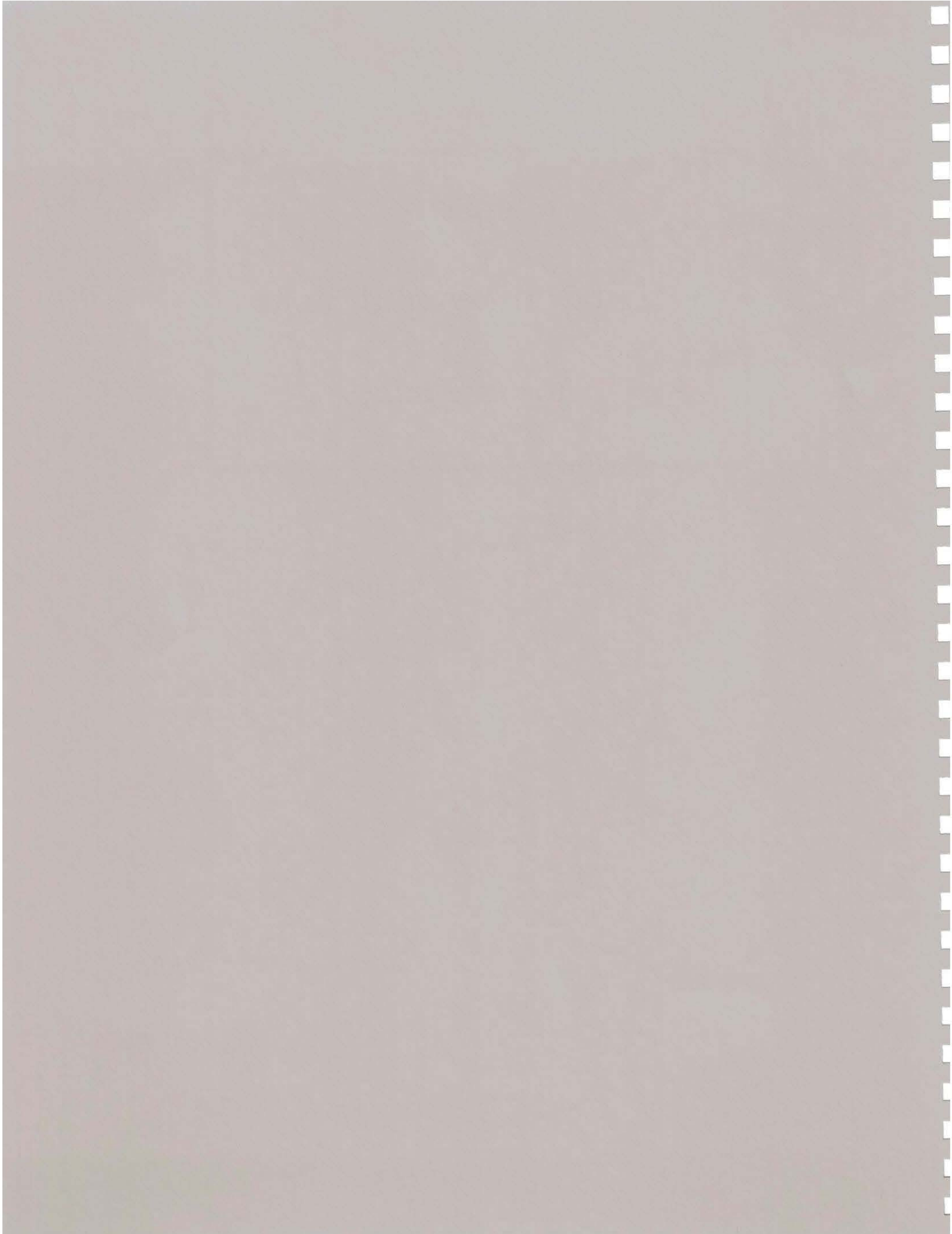
Figure 1

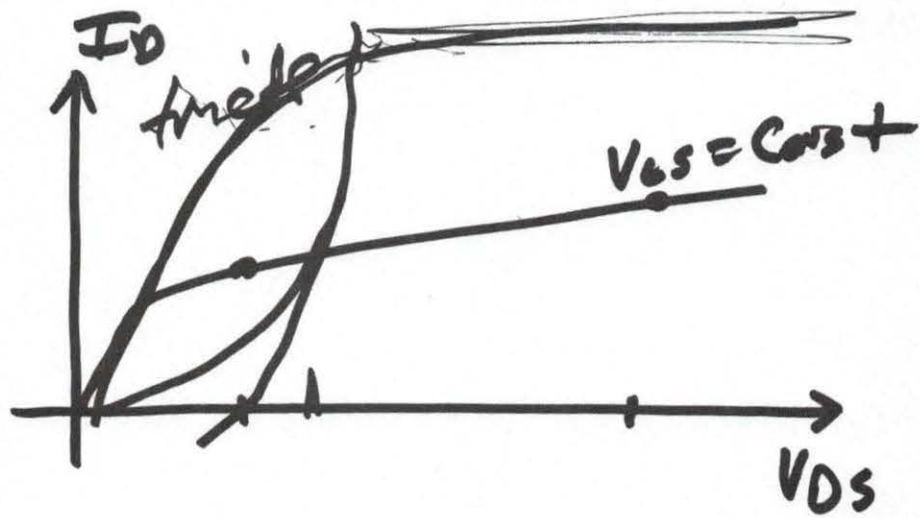
Figure 1

## Lesson 2

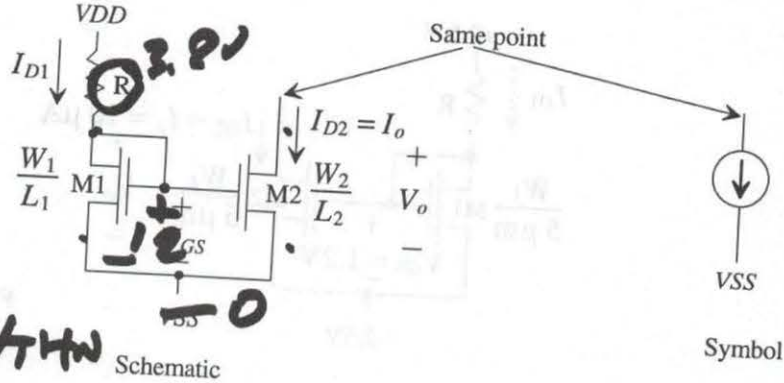
### Current Sources and Sinks I

#### Tutorial Visuals





5V 104A  $\Rightarrow$  94A



$f_T \propto V_{GS} - V_{THN}$

Figure 20.1 The basic current mirror schematic and symbol.

Ch 9.

$$I_D = \frac{K_P \cdot W}{2L} (V_{GS} - V_{THN})^2$$

for saturation

$$V_{DS} \geq V_{GS} - V_{THN}$$

$$\Delta V = V_{GS} - V_{THN} \approx 370mV$$

$$\underline{1.2} - .83$$

$$I_D = 104A \Rightarrow \frac{W}{L} = \frac{154}{54}$$

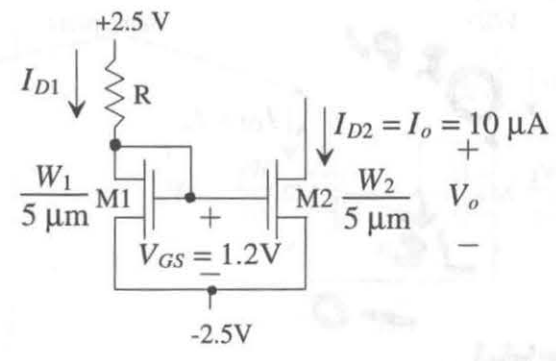
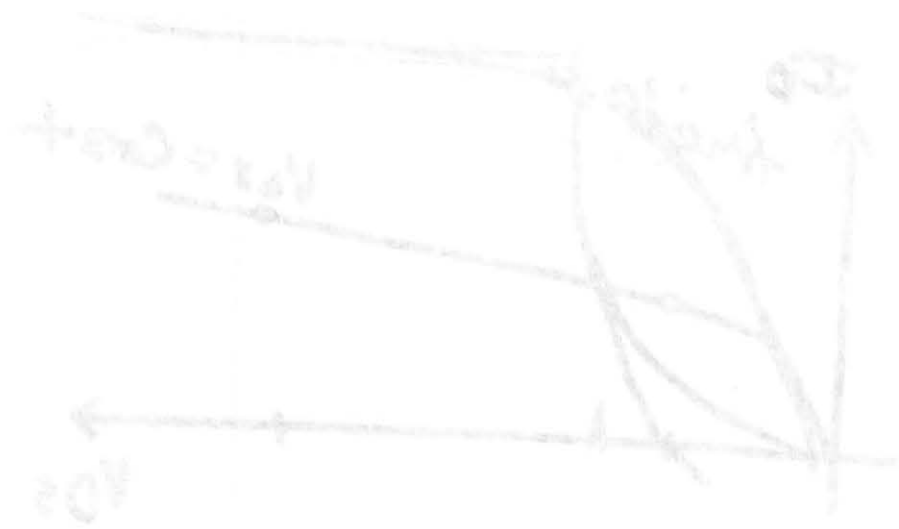


Figure Ex20.1

$$W_1 = W_2 = 15 \mu\text{m}$$

$$R = 380\text{K}$$

Handwritten notes and calculations:

$$V_{GS} = 1.2\text{V}$$

$$\Delta V = V_{GS} - V_{TH} = 1.2\text{V} - 0.5\text{V} = 0.7\text{V}$$

$$\frac{10 \mu\text{A}}{2\text{V}} = \frac{10 \mu\text{A}}{3\text{V}} \Rightarrow \mu_n C_{ox} = 10 \mu\text{A} = 0.2$$

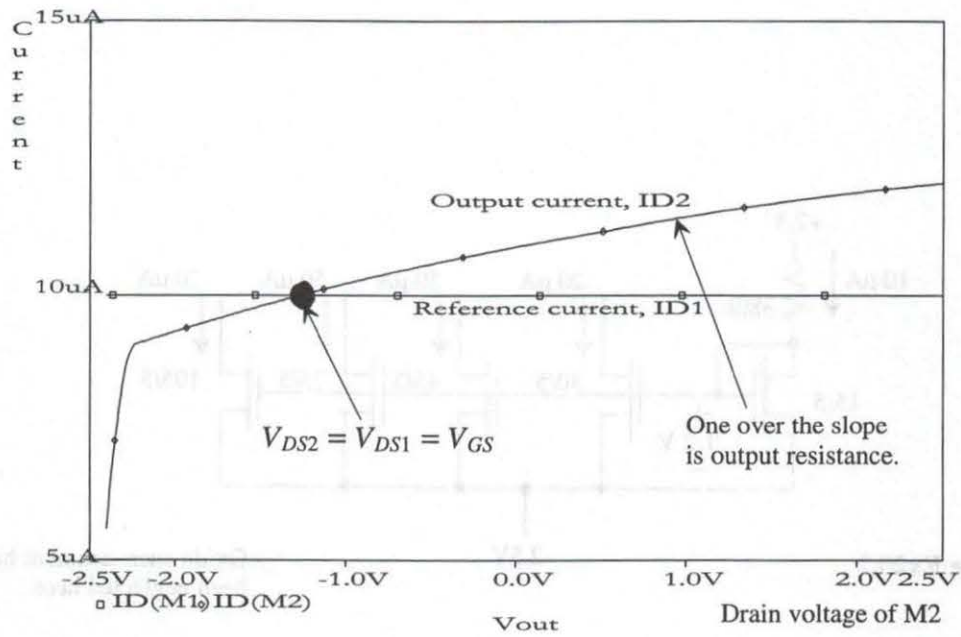


Figure 20.2 Example 20.1 SPICE simulation results.

$$r_o = \frac{1}{\lambda I} = \frac{1}{.06 \cdot 104 \mu A} = \underline{\underline{1.66 \text{ MEG}}}$$

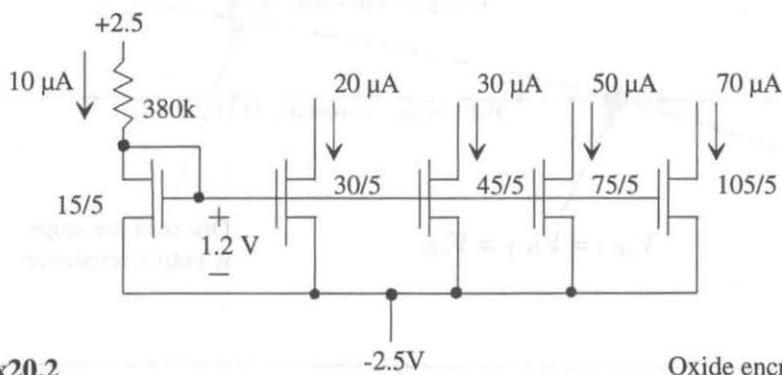


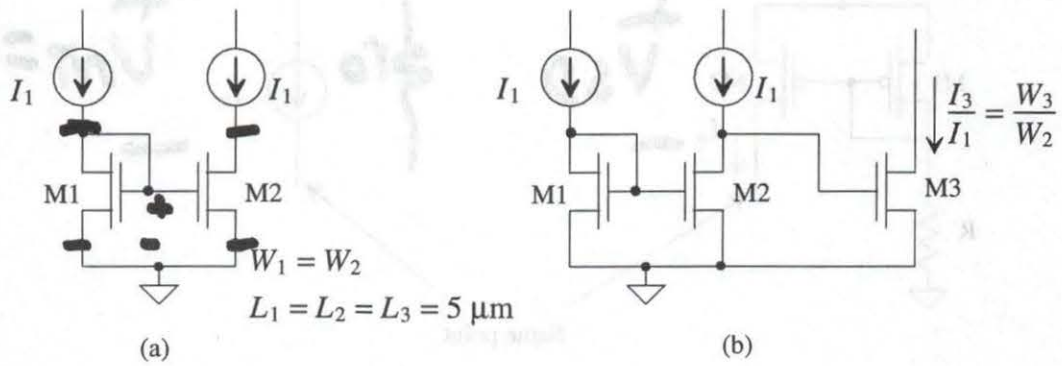
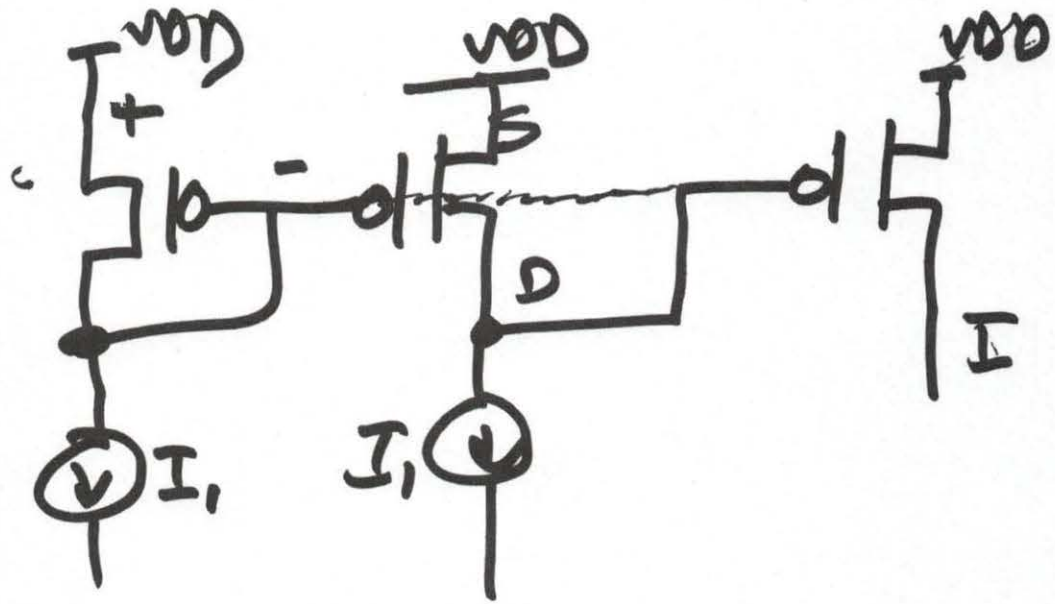
Figure Ex20.2

Oxide encroachment has been neglected here.

$$I_D = \frac{K_P}{2} \cdot \frac{W}{L} (V_{GS} - V_{THN})^2$$

1.66 nA





**Figure 20.3** (a) The drain of M2 is at the same potential as the gate of M1 or M2 and (b) using this to bias M3. For biasing purposes, we treat M3 as if its gate were tied to the gates of M1 and M2.

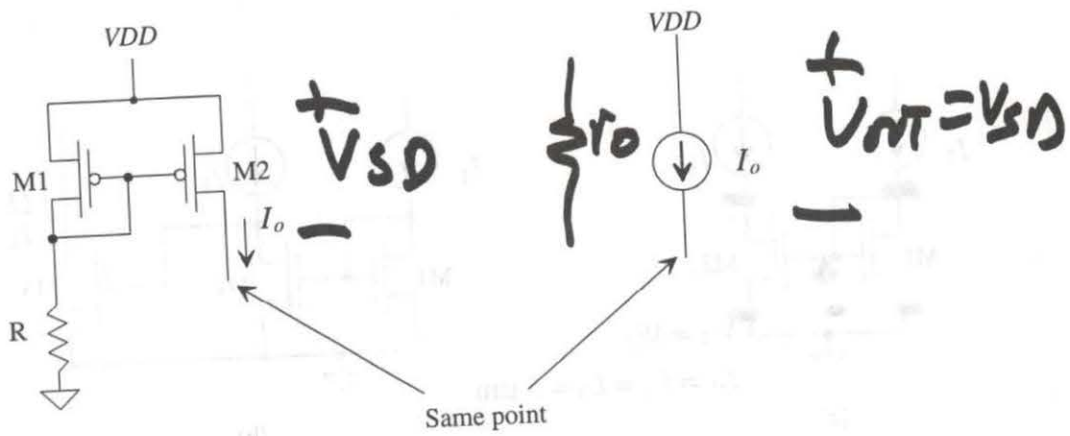
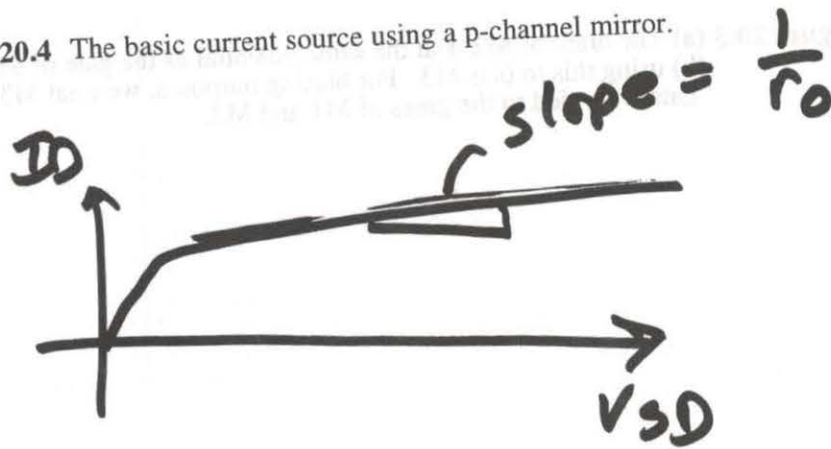
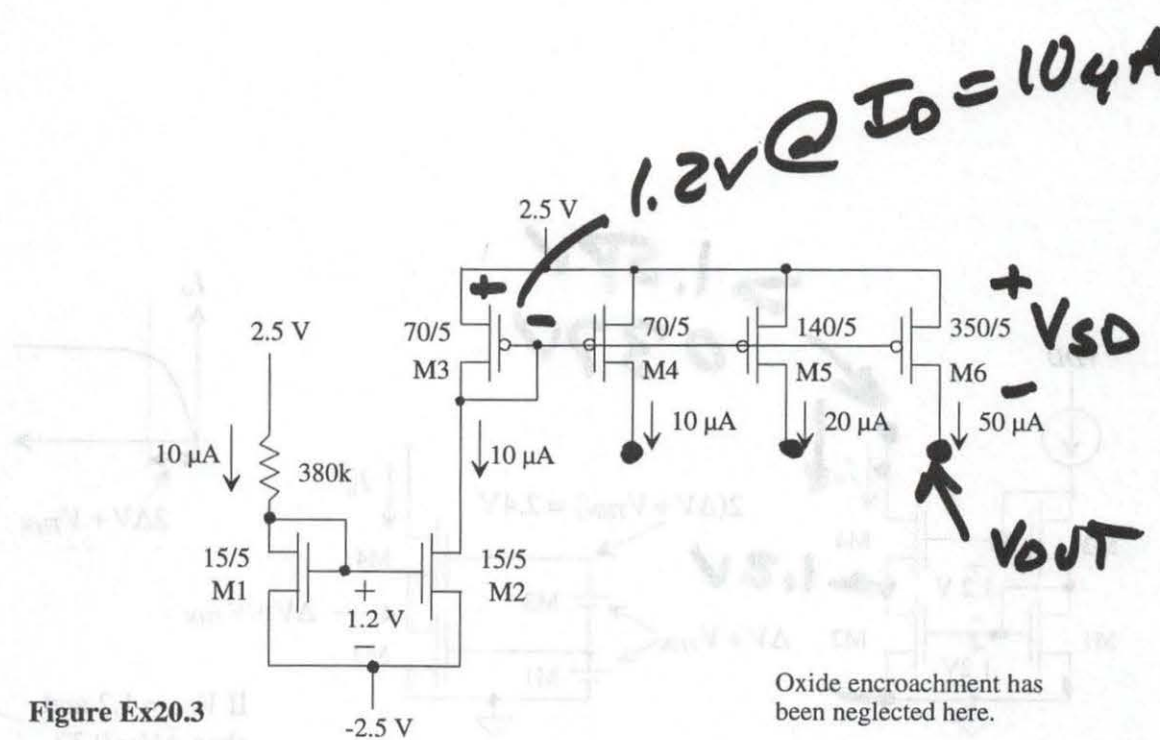


Figure 20.4 The basic current source using a p-channel mirror.



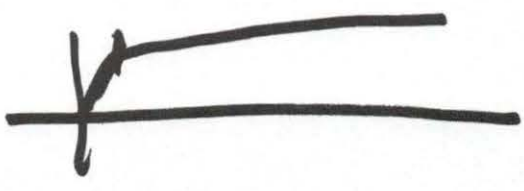


$$V_{SD} \geq V_{SG} - V_{THP}$$

$$1.2V - .91$$

$$\underline{V_{SD}} \geq \underline{\underline{.29V}}$$

$$V_o < 2.5 - .29 = 2.21V$$



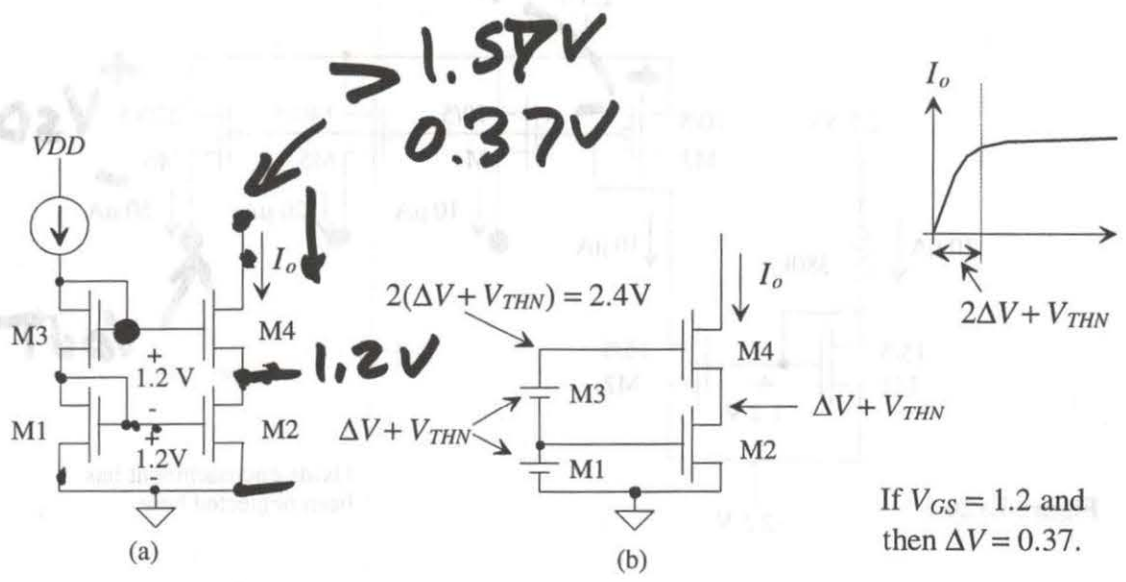


Figure 20.5 The cascode current source.

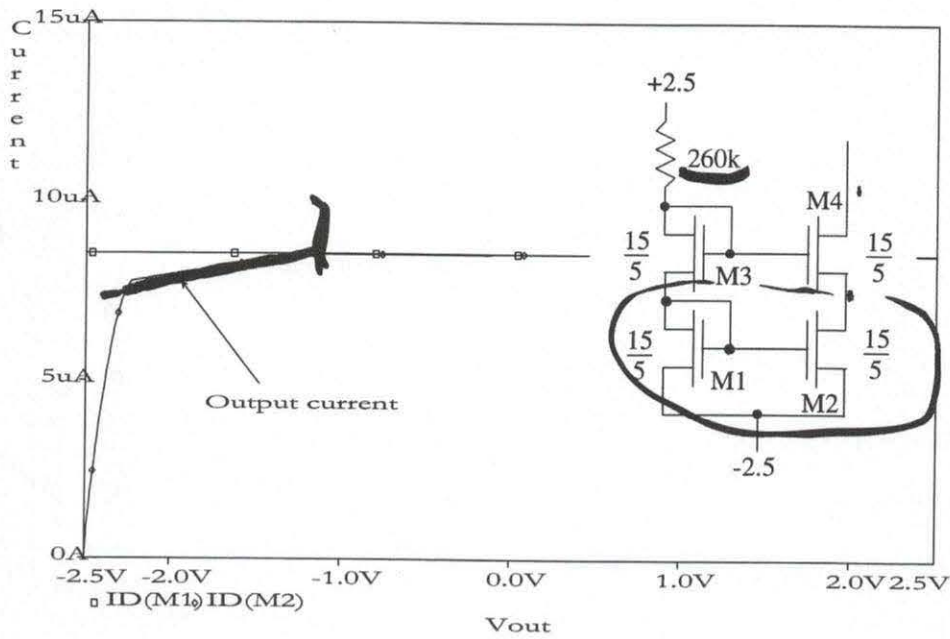


Figure Ex20.4

BIAS  $\rightarrow$   $r_o = \frac{1}{\lambda I_D}$

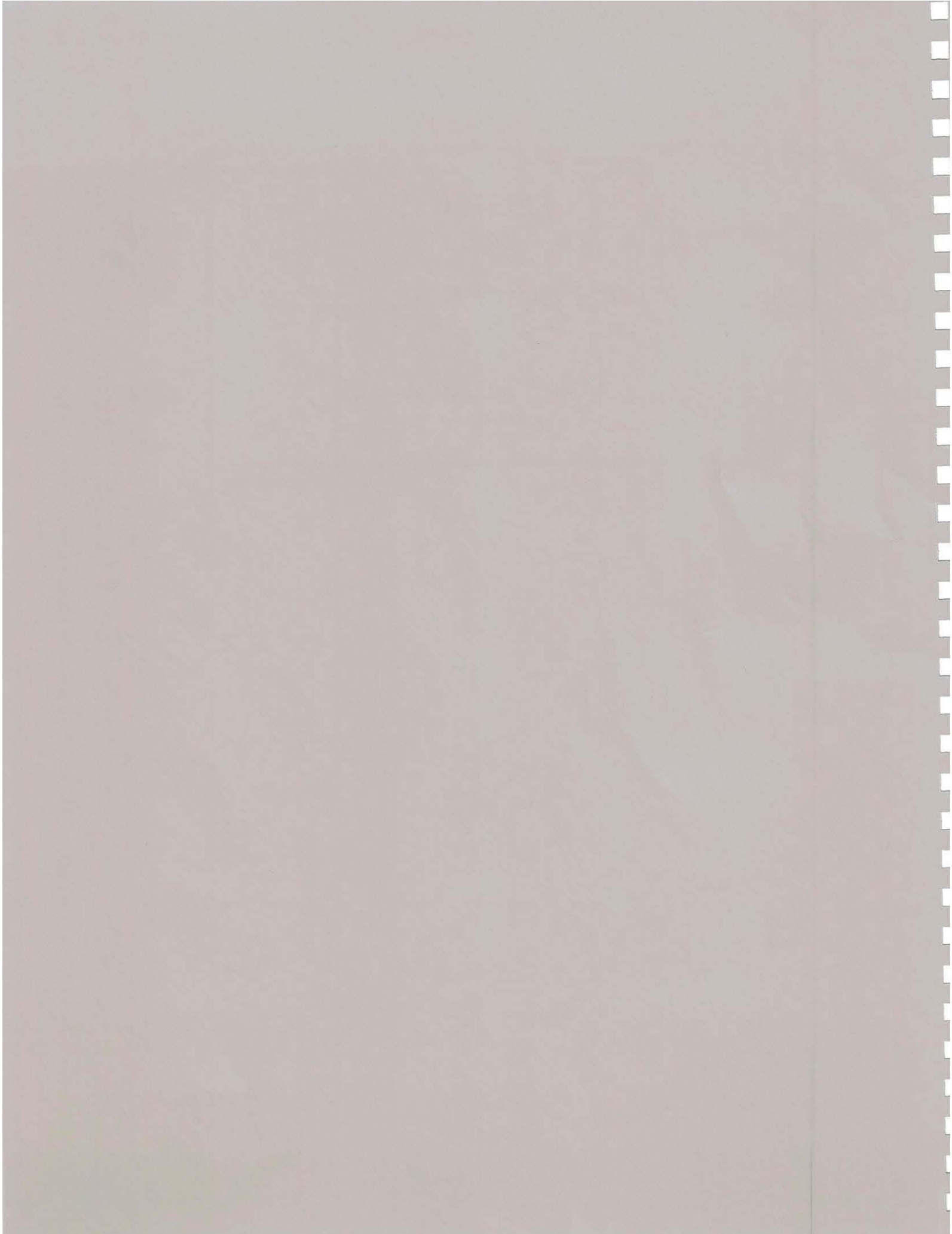
$\rightarrow$   $r_o = 10^9 \Omega$



## Lesson 3

### Current Sources and Sinks II

#### Tutorial Visuals





$$V_{THN}(T) = V_{TH0} (1 + TC_{V_{THN}} (T - T_0))$$

$$TC_{V_{THN}} = \frac{1}{V_{TH0}} \cdot \frac{\delta V_{THN}}{\delta T}$$

$$-3,000 \frac{\text{ppm}}{^\circ\text{C}}$$

$$-0.003$$

$$10^{-6} = \text{ppm}$$

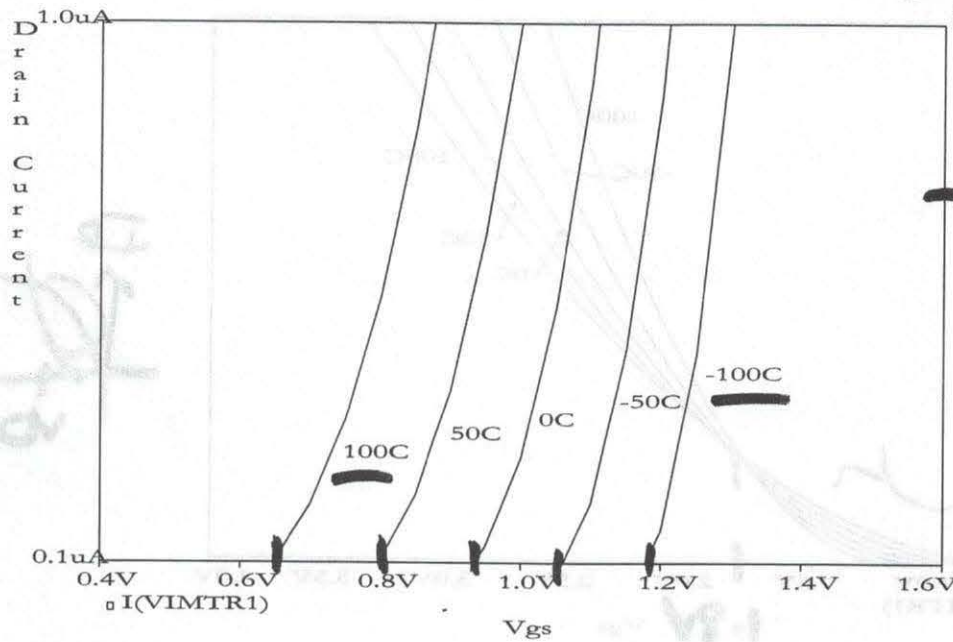
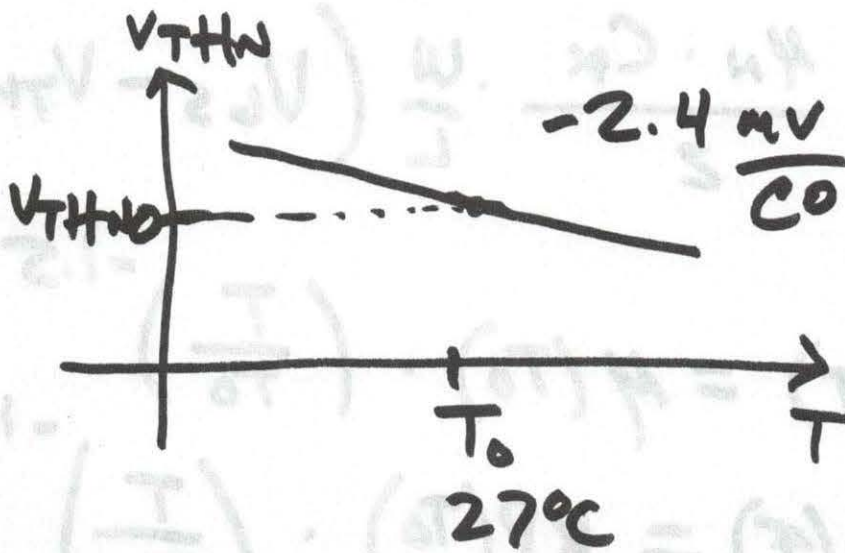


Figure 9.10 Threshold voltage change with temperature for  $V_{GS}$  approximately  $V_{THN}$ .



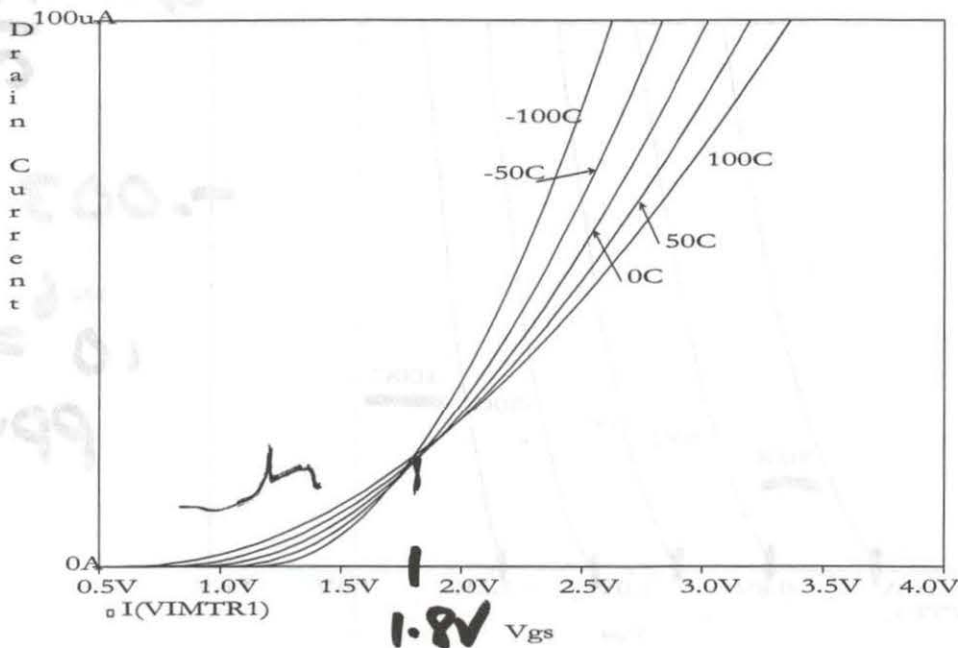


Figure 9.11 Mobility effects when  $V_{GS} \gg V_{THN}$ .

$$I_D = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} (V_{GS} - V_{THN})^2$$

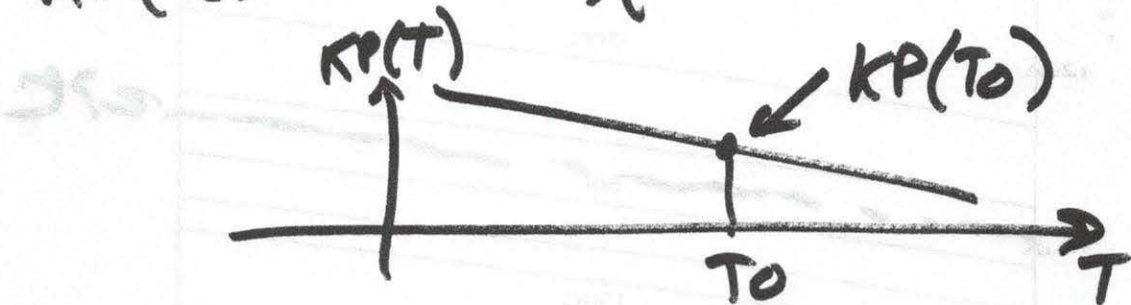
$$\mu(T) = \mu(T_0) \cdot \left(\frac{T}{T_0}\right)^{-1.5}$$

$$K_P(F) = K_P(T_0) \cdot \left(\frac{T}{T_0}\right)^{-1.5}$$

$$TC_{KP} = \frac{-1.5}{T} \leftarrow \text{kelvin}$$

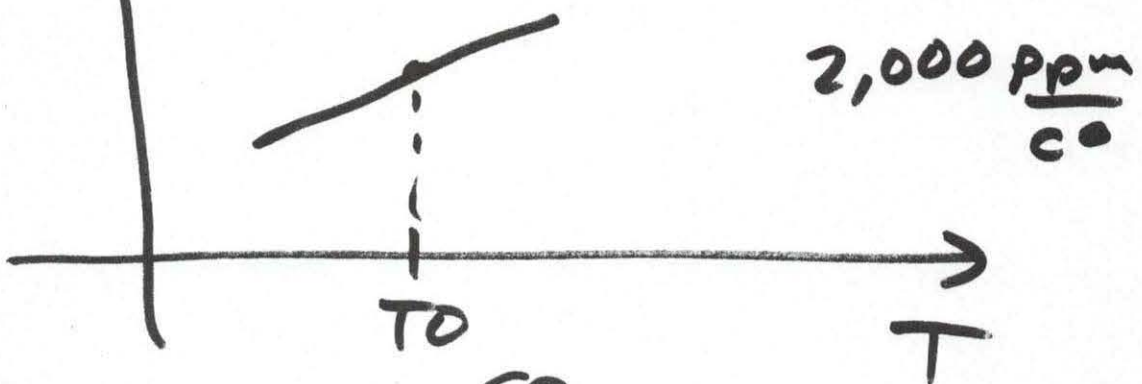
$$-5,000 \frac{\text{ppm}}{C^{\circ}}$$

$$KP(T) = KP(T_0) (1 + TC_{KP} (T - T_0))$$

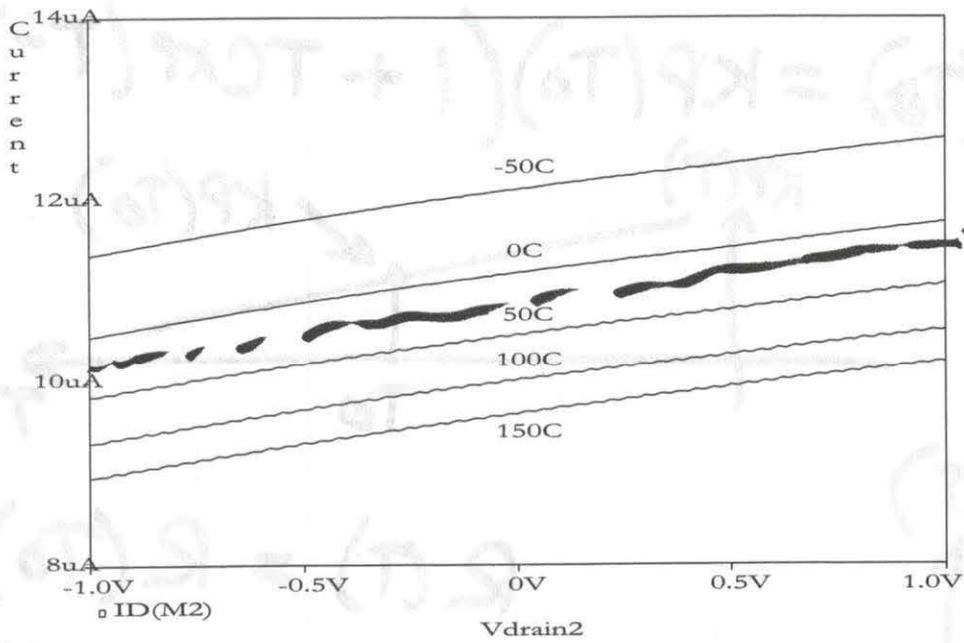

 $R(T)$ 

$$R(T) = R(T_0) \cdot$$

$$(1 + TCR (T - T_0))$$



$$TCR = \frac{1}{R} \cdot \frac{\delta R}{\delta T} = \text{ppm} \cdot \frac{0.002}{C^{\circ}}$$



**Figure 20.10** Temperature characteristics of the simple current mirror of Ex. 20.1. Notice that the voltage on the drain of M2 is swept from -1 V to +1 V.

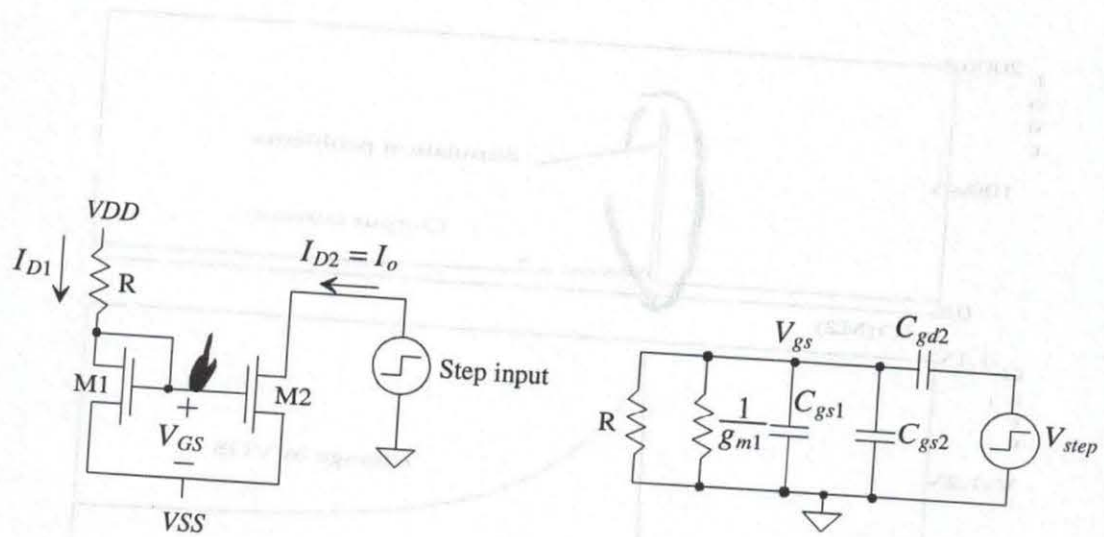
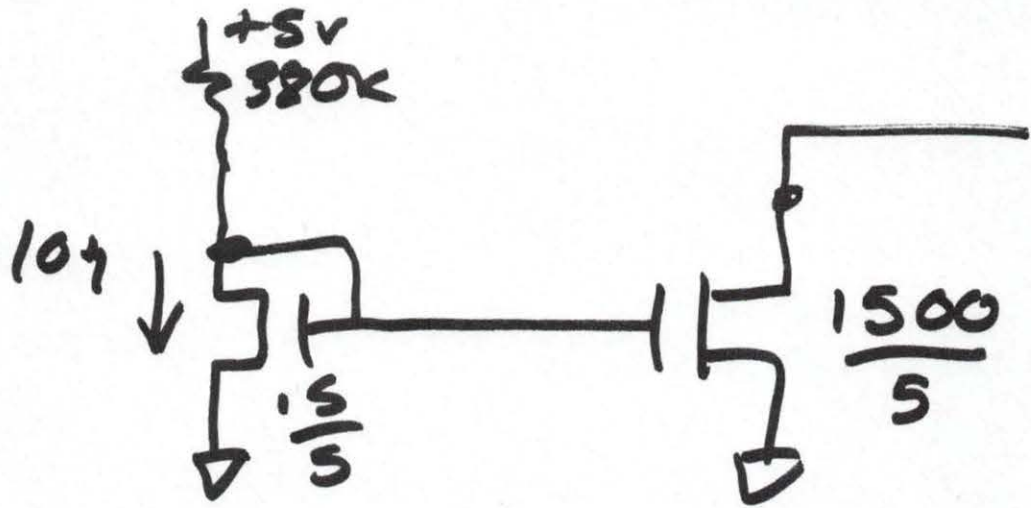
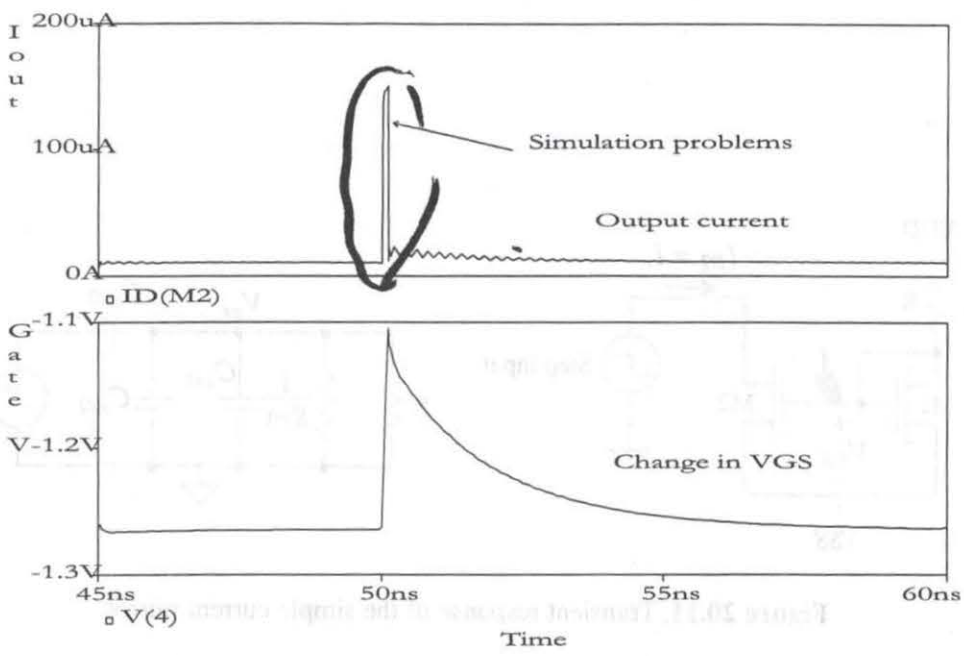


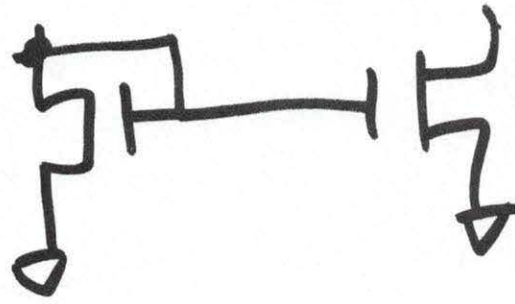
Figure 20.11 Transient response of the simple current mirror.



**Figure 20.12** Simulated pulse response of the current mirror in Ex. 20.1.

$$\frac{4.5}{5}$$

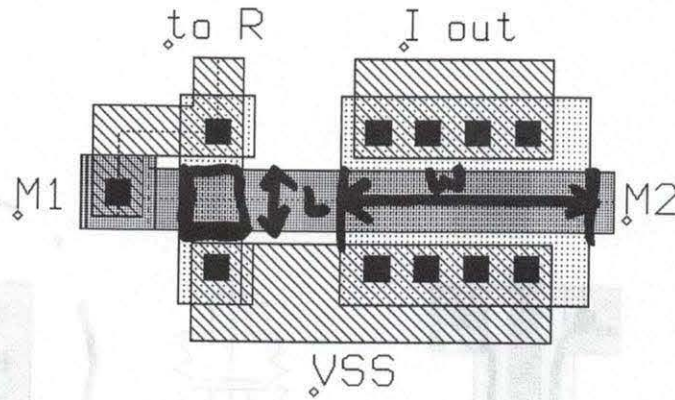
$$\frac{3}{5}$$



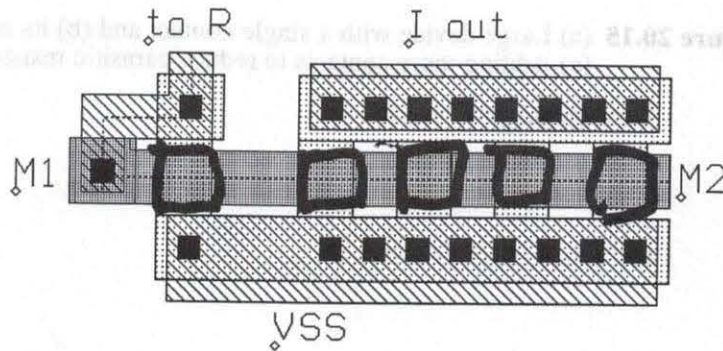
$$\frac{20}{5}$$

$$\frac{19.5}{5}$$

Simple current mirror

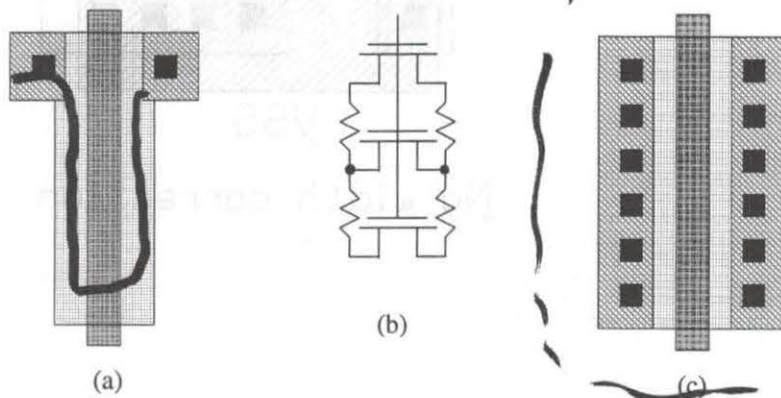


No width correction



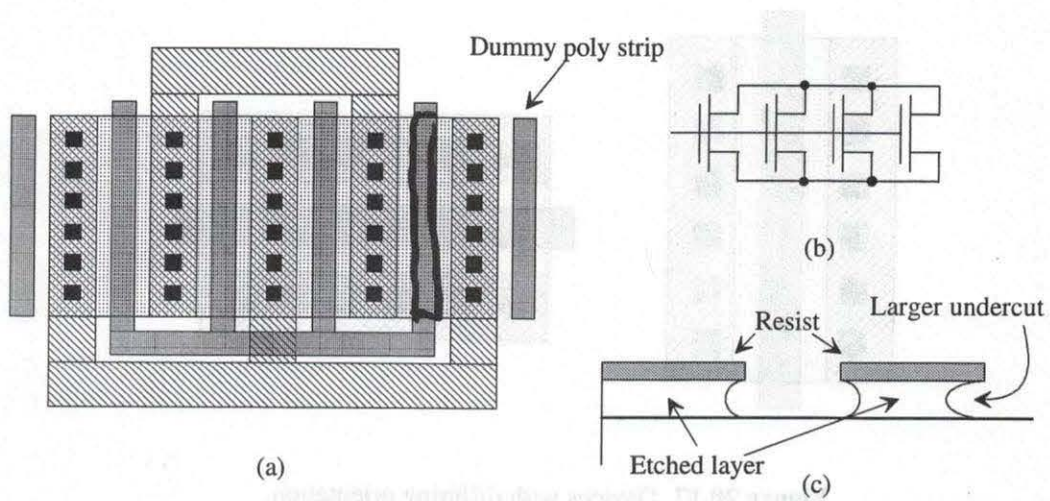
Mirror with width correction

Figure 20.13 Layout of a MOSFET mirror to eliminate oxide encroachment effects.



**Figure 20.15** (a) Large device with a single contact and (b) its equivalent circuit. (c) Adding more contacts to reduce parasitic resistance.





**Figure 20.16** (a) A parallel device with dummy strips, (b) the equivalent circuit and (c) undercutting.

! 214 ob fuob

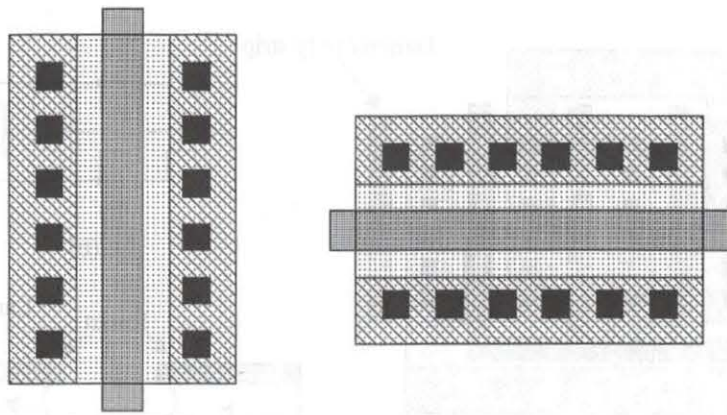
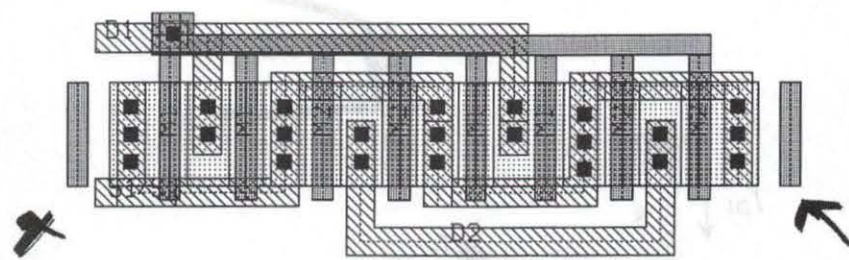
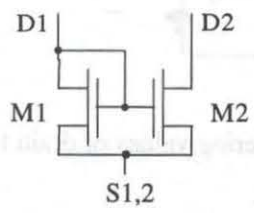


Figure 20.17 Devices with differing orientation.

don't do this!



(a)



(b)

**Figure 20.18** (a) Layout of a simple current mirror using interdigitation and (b) equivalent circuit.

$$\frac{I_2}{I_1} = 1 = \frac{I_2}{I_1} \leftarrow \text{Bias}$$

$$V_{GS} = V_{GS} - V_{TH}$$

$$\frac{I_o}{I_{D1}} = 1 - \frac{2\Delta V_{THN}}{(V_{GS} - V_{THN})}$$

↑  
BIAS

$$V_{OS} \geq V_{GS} - V_{THN}$$

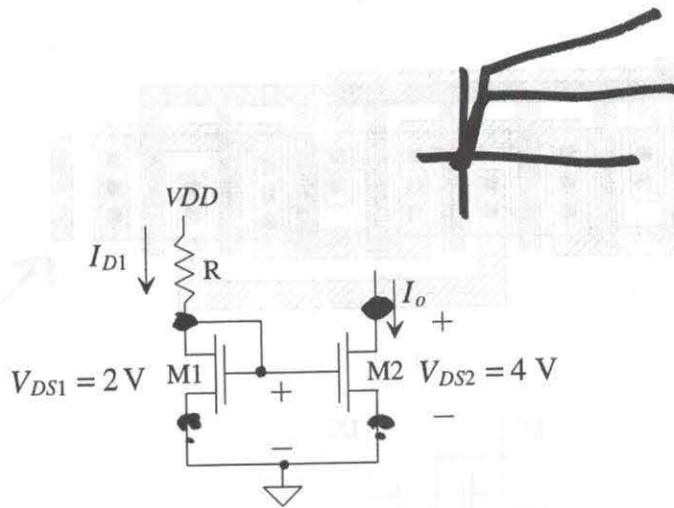


Figure 20.14 Basic current mirror with differing values of drain to source voltages.

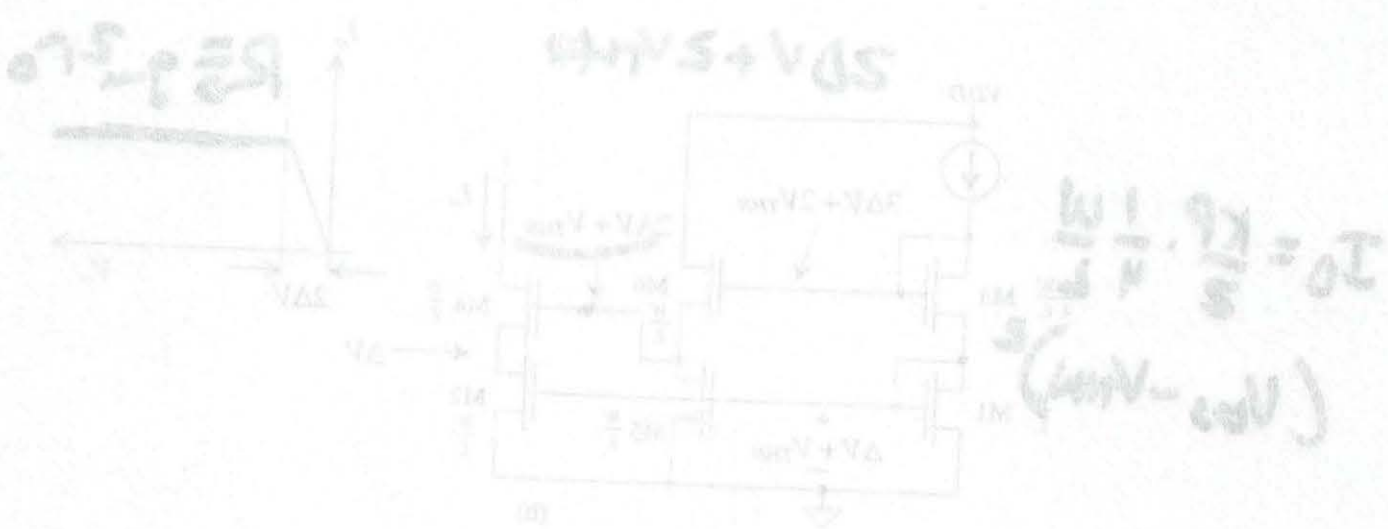
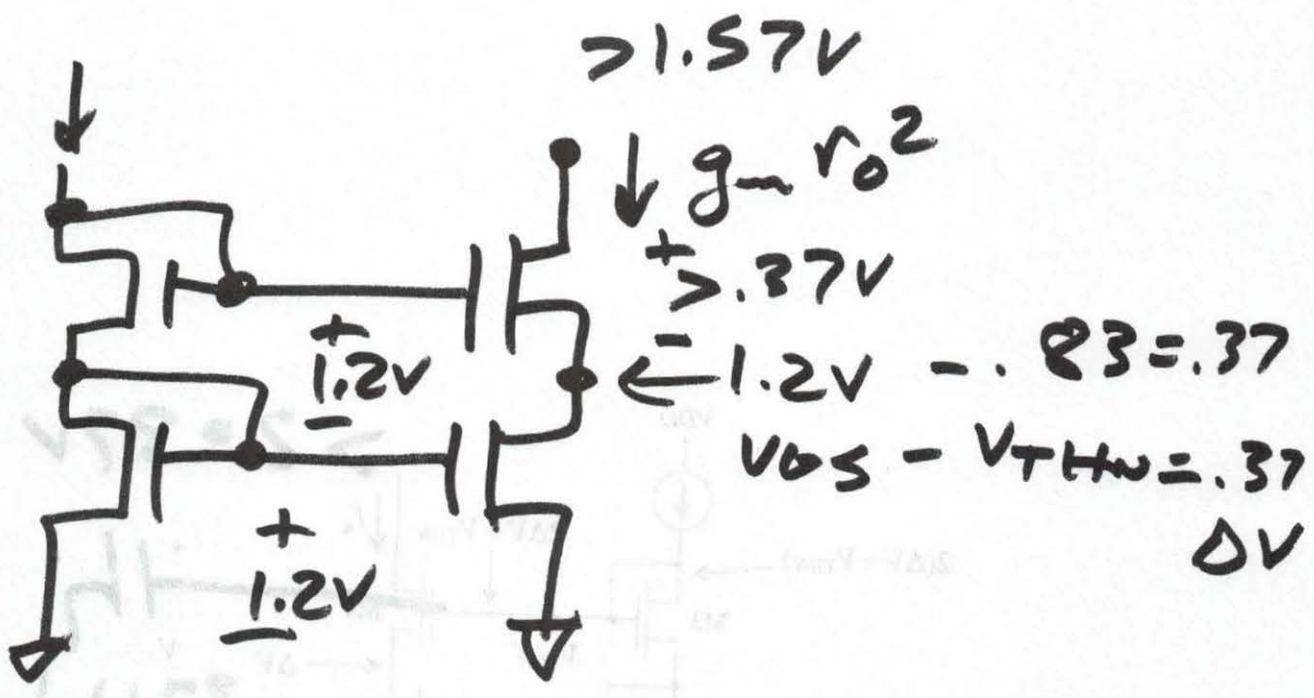


Figure 20.6. Finding of the load current source for lowest minimum voltage across the current source (best effects neglected).

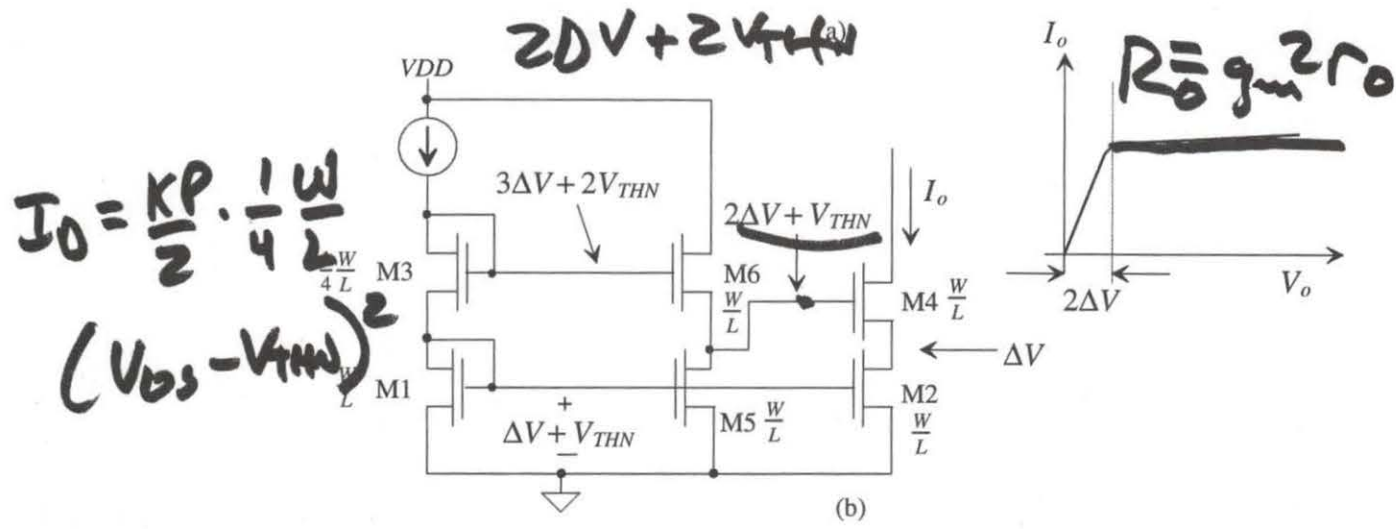
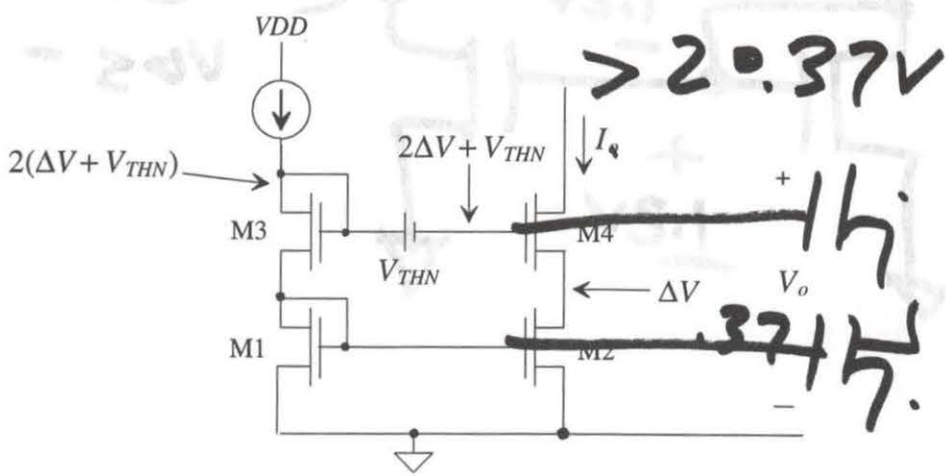
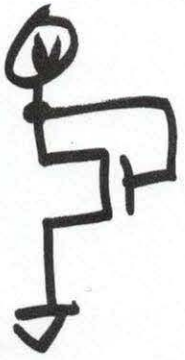


Figure 20.6 Biasing of the cascode current source for lower minimum voltage across the current source (body effects neglected).

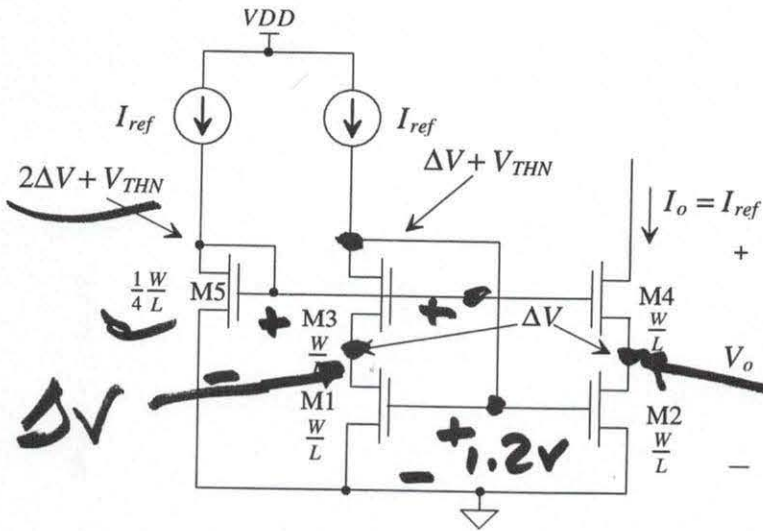


$$I_D = \frac{\beta}{2} (V_{GS} - V_{THN})^2$$

$$= \frac{K_P}{2} \cdot \frac{W}{L} (\Delta V)^2$$

$$I_D = \frac{K_P}{2} \cdot \frac{W}{L} (\Delta V)^2 = \frac{K_P}{2} \cdot \frac{1}{4} \cdot \frac{1}{4} (V_{GS} - V_{THN})^2$$

15/20



74V  
8V

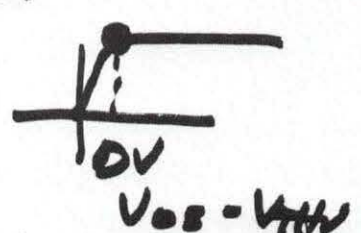


Figure 20.26 A high-swing cascode current mirror.

$$(\Delta V)^2 = \frac{1}{4} (V_{GS} - V_{THN})^2$$

$$\Delta V = \frac{1}{2} (V_{GS} - V_{THN})$$

$$V_{THN} + 2\Delta V = V_{GS}$$

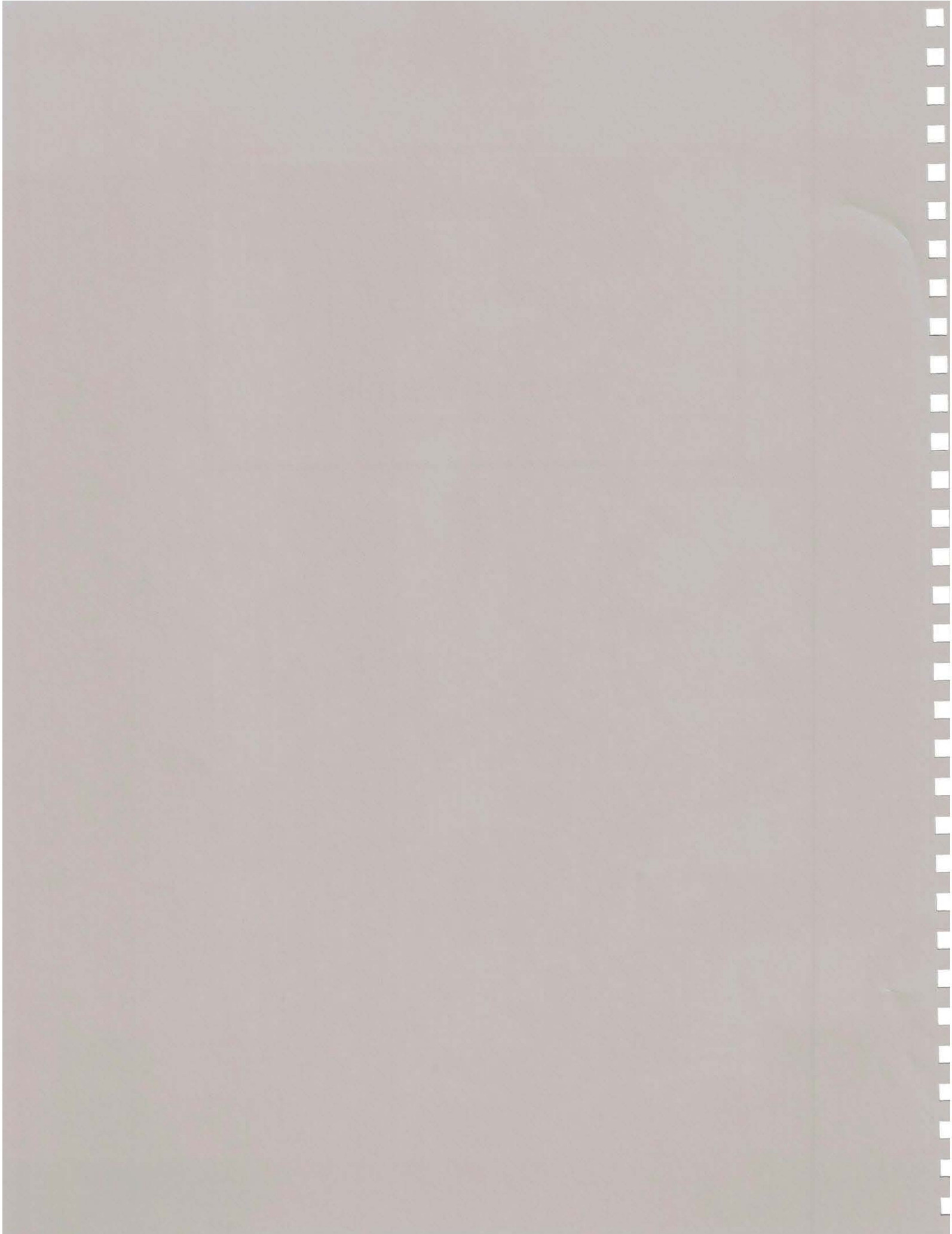




Lesson 4

References I

Tutorial Visuals



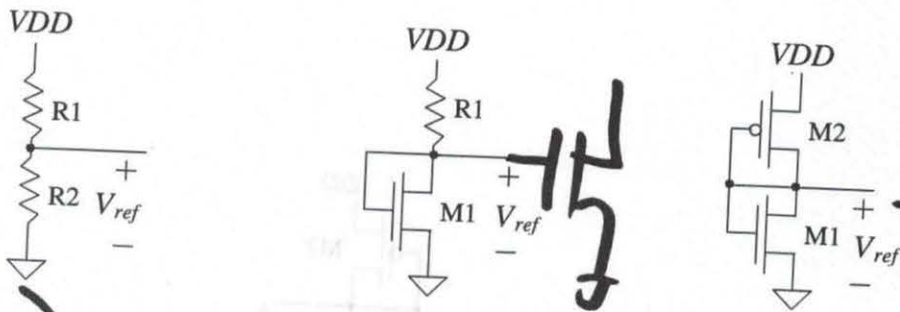
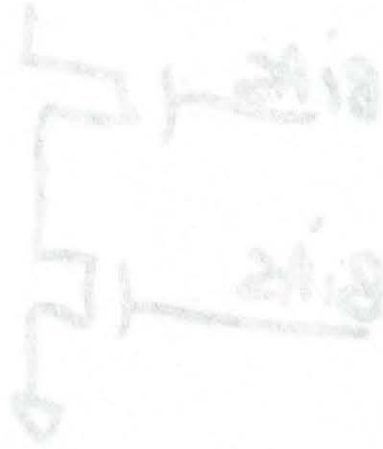


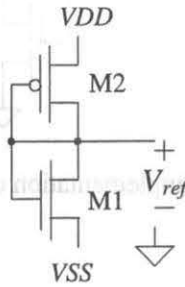
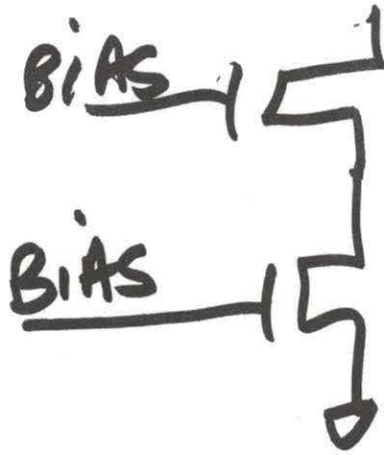
Figure 21.1 Implementation of voltage dividers in CMOS.

Ch. 7

CAN require large layout area.



MOSFET only  
PROCESS & TEMP  
INSENSITIVE

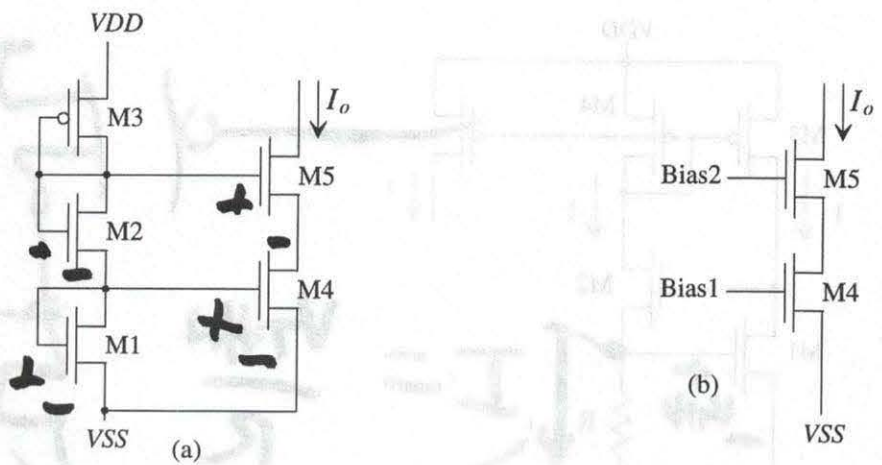


**Figure 21.3** MOSFET-only voltage divider used between VDD and VSS.

Can't require large layout area.

process & temp insensitive  
MOSFET only





**Figure 21.6** Use of the three-MOSFET voltage divider to bias the cascode current source: (a) full schematic and (b) simplified schematic.

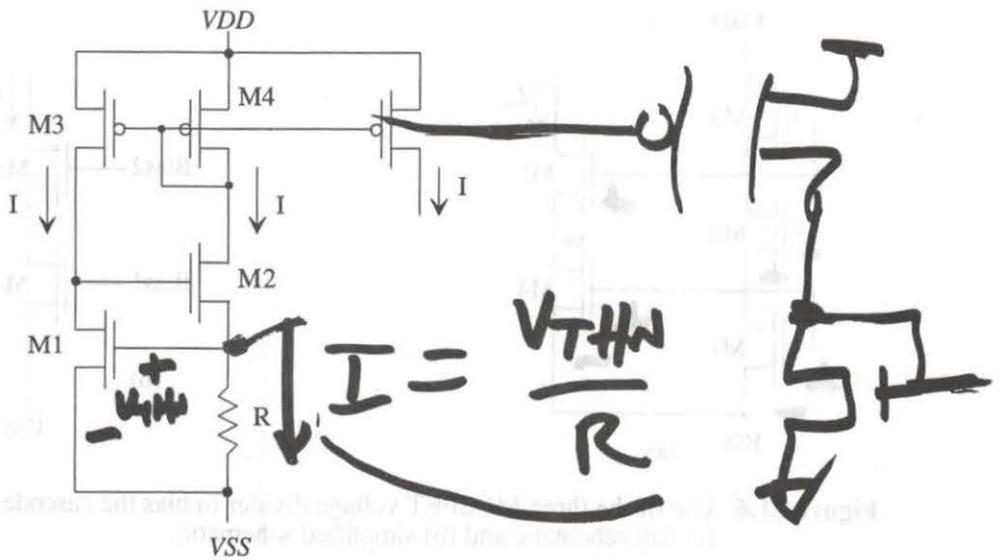
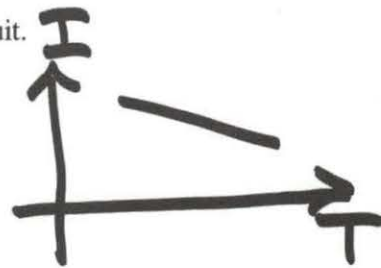
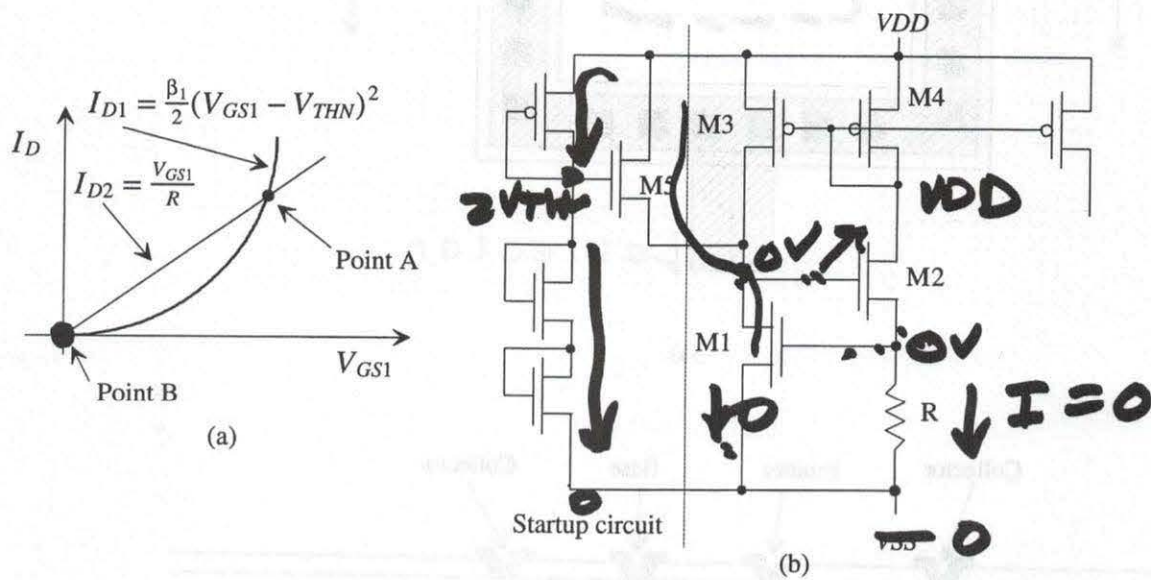


Figure 21.7 Threshold reference self-biasing circuit.

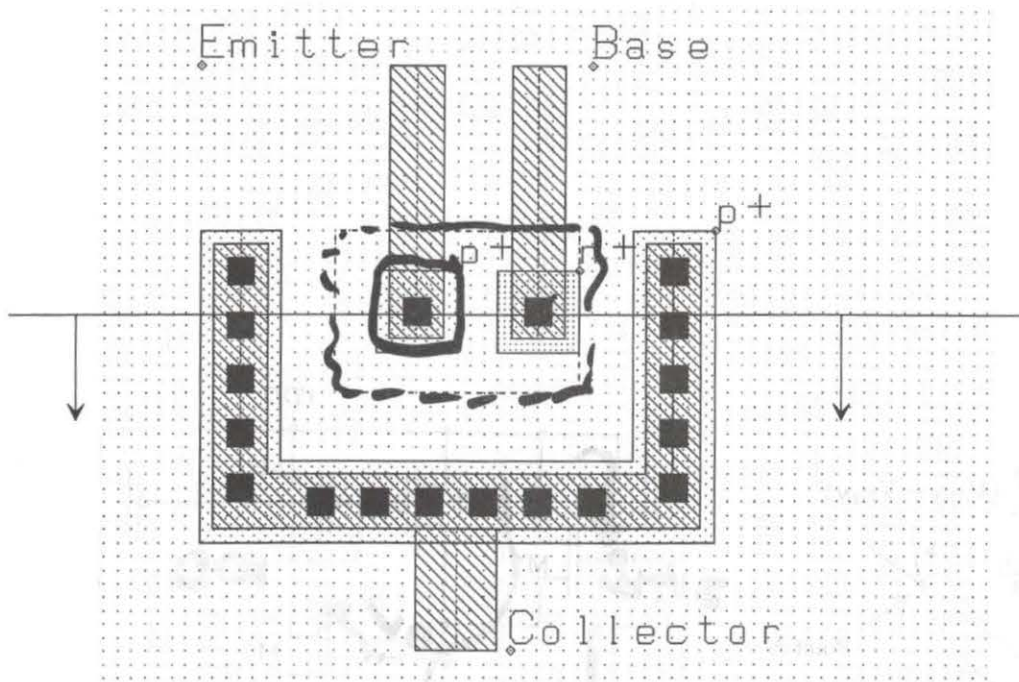
$T \nearrow$   $V_{THN} \searrow$   
 $T \nearrow$   $R \nearrow$



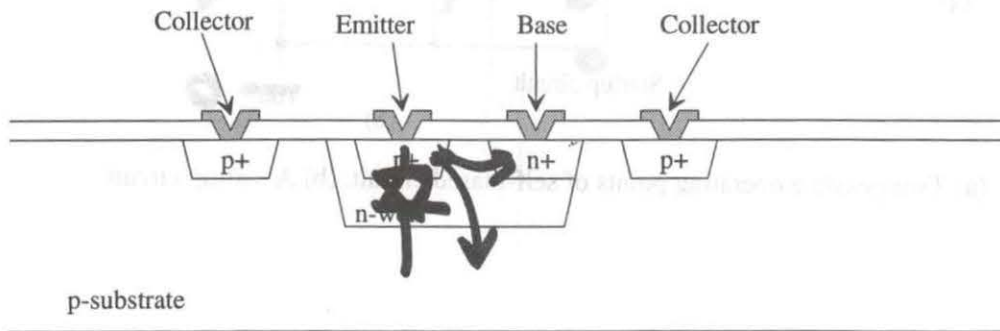


**Figure 21.8** (a) Two possible operating points of self-biased circuit. (b) A startup circuit.

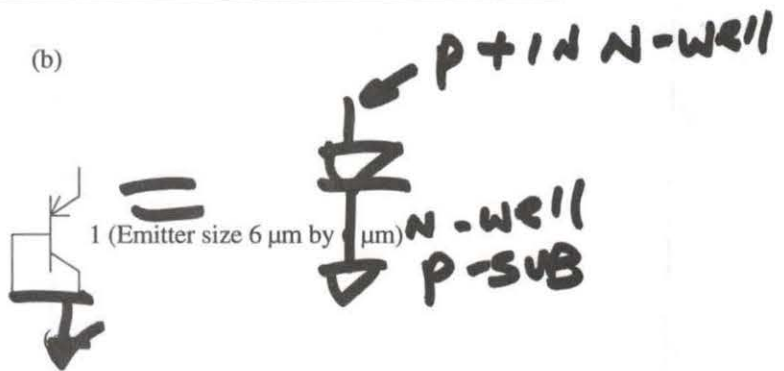
Figure 21.8 (a) and (b) are taken from the book "CMOS Analog Circuit Design" by Thomas L. Floyd, 2nd Edition, Prentice-Hall, 2003. The copyright notice for this book is: Copyright 2003 by Prentice-Hall, Inc. All rights reserved. No part of this book may be reproduced, stored in a retrieval system, or transmitted, in any form or by any means, electronic, mechanical, photocopying, recording, or by any information storage and retrieval system, without the prior written permission of Prentice-Hall, Inc.



(a)



(b)



**Figure 21.9** Layout (a) and cross-sectional view (b) of the parasitic pnp transistor available in an n-well CMOS process and (c) schematic representation of a minimum-size parasitic pnp, that is, emitter area of  $6 \mu\text{m}$  by  $6 \mu\text{m}$ .



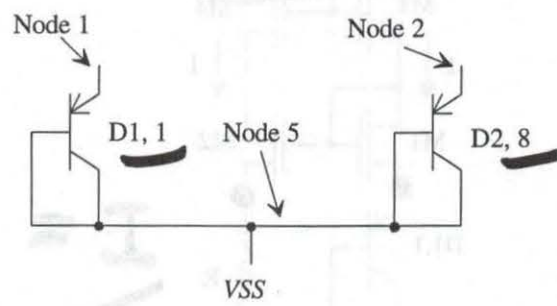
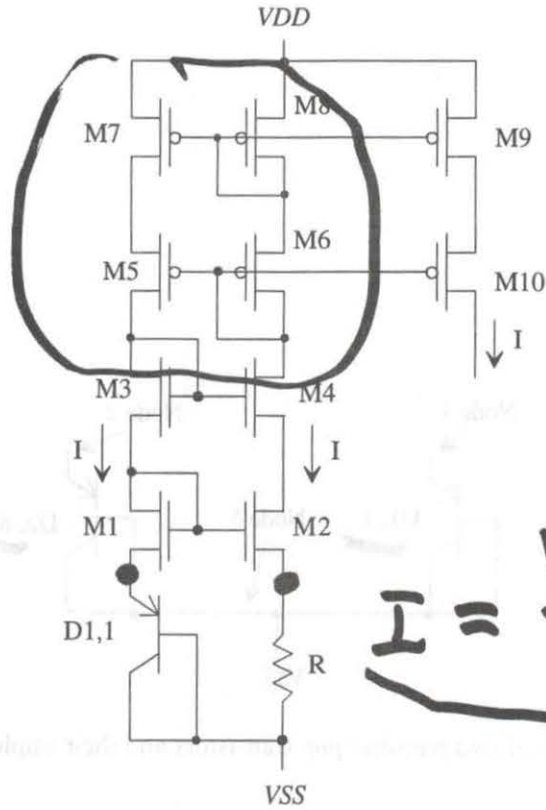


Figure 21.10 Diagram of two parasitic pnp transistors and their implementation in SPICE.



Requires startup circuit

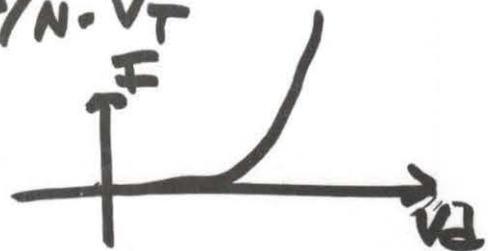
Figure 21.11 Diode referenced self-biasing circuit.

$$-2 \frac{mV}{C_0}$$



$$R \nearrow T \nearrow$$

$$I_d = I_s e^{V_d / (n \cdot V_T)}$$



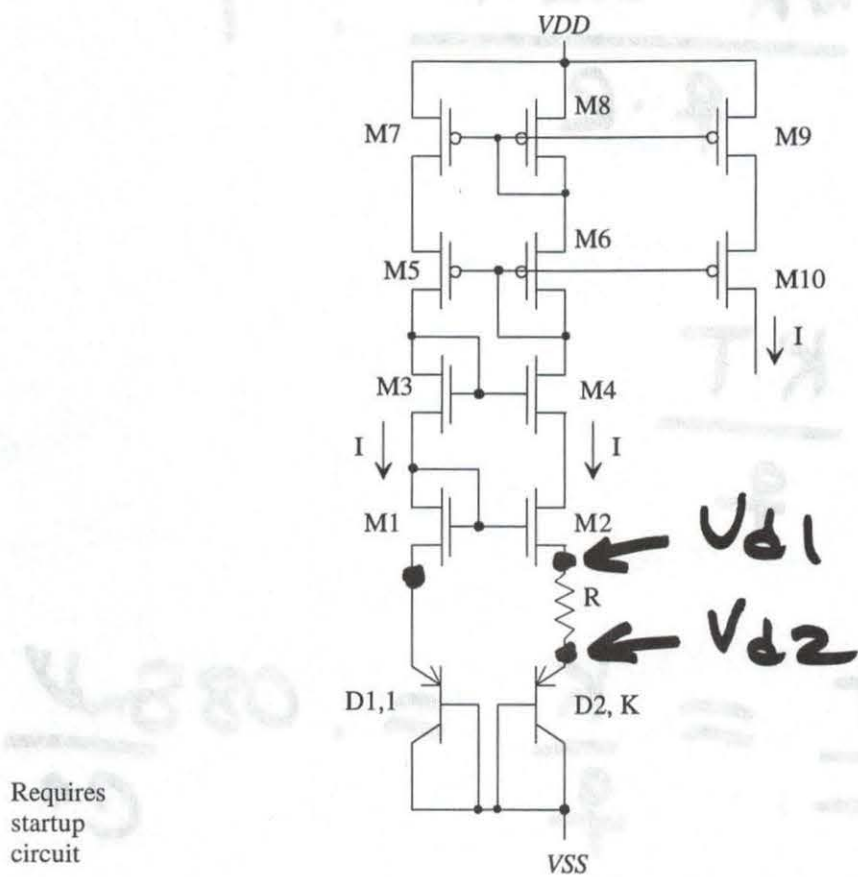


Figure 21.12 Thermal voltage referenced self-biasing circuit.

$$I = \frac{V_{d1} - V_{d2}}{R}$$

$$V_{d1} = NV_T \cdot \ln \frac{I_{d1}}{I_s}$$

$$V_{d2} = NV_T \cdot \ln \frac{I_{d2}}{I_s}$$

$$\ln \frac{a}{b} = \ln a - \ln b$$

$$R = \frac{N V_T \cdot \ln K}{I}$$

$$I = \frac{N K \cdot \ln K}{q \cdot R} \cdot T$$

$$V_T = \frac{kT}{q}$$

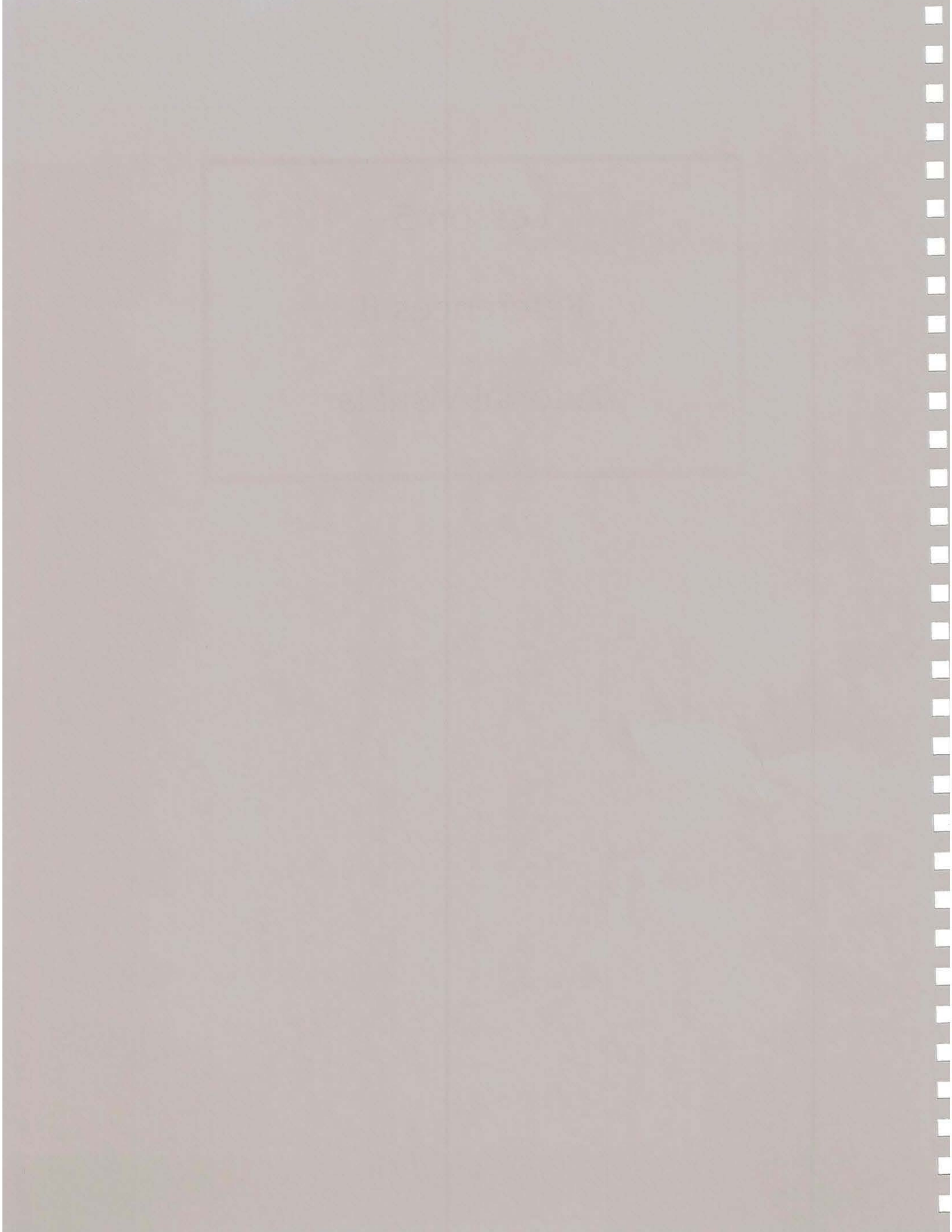
$$\frac{\delta V_T}{\delta T} = \frac{k}{q} = .085 \frac{\text{mV}}{\text{C}^\circ}$$

$$\text{TCV}_T \approx 7,000 \frac{\text{PPM}}{\text{C}^\circ}$$

Lesson 5

References II

Tutorial Visuals



$$I = \frac{N \cdot V_T \cdot \ln K}{R}$$

$$V_{REF} = I \cdot L \cdot R + V_{DS}$$

Requires  
startup  
circuit

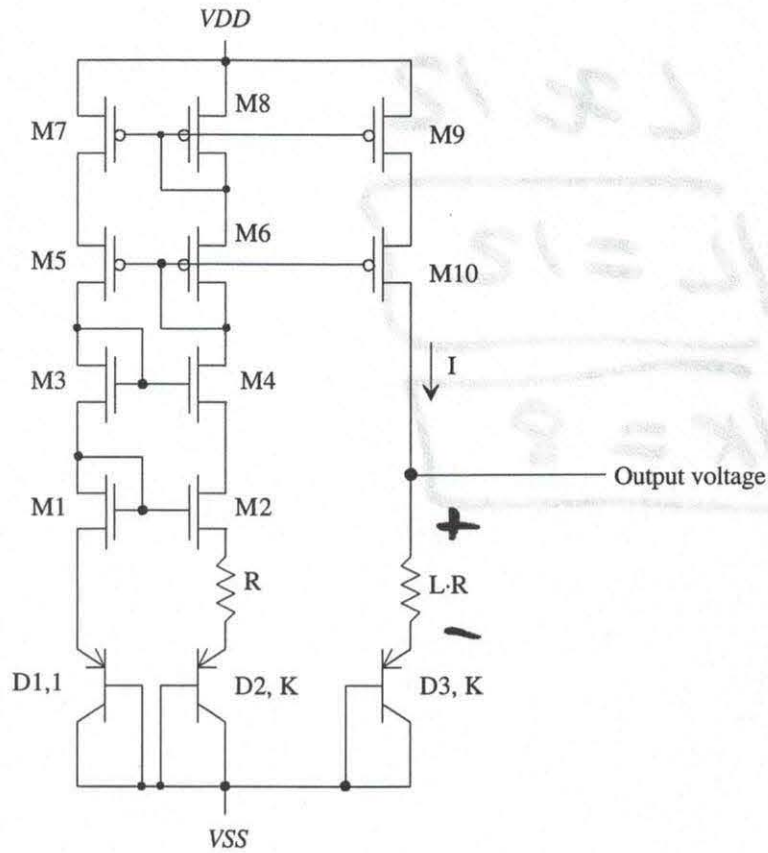


Figure 21.14 A bandgap voltage reference.

$$V_{REF} = (L \cdot N \cdot \ln K) V_T + V_{DS}$$

$$\frac{\delta V_{REF}}{\delta T} = L \cdot N \cdot \ln K \cdot \frac{\delta V_T}{\delta T} + \frac{dV_{DS}}{dT} \stackrel{?}{=} 0$$

$\frac{\delta V_T}{\delta T} = 0.85 \frac{mV}{^\circ C}$ 
 $\frac{dV_{DS}}{dT} = -2 \frac{mV}{^\circ C}$

$$L \cdot \frac{1}{k} \cdot L \cdot k = \frac{2}{.085} = 23.5$$

$$L \approx 12$$

$$L = 12$$

$$k = 8$$



Figure 2.14 A 2-bit ripple carry adder

$$V_{out} = (L \cdot k \cdot U) V_T + V_{ref}$$

$$\frac{V_{out}}{V_T} = L \cdot k \cdot U + \frac{V_{ref}}{V_T}$$

$$\frac{2.5}{1} = 12 \cdot 8 \cdot U + \frac{1.25}{1}$$

$$1.25 = 96U + 1.25$$

$$0 = 96U$$

$$U = 0$$



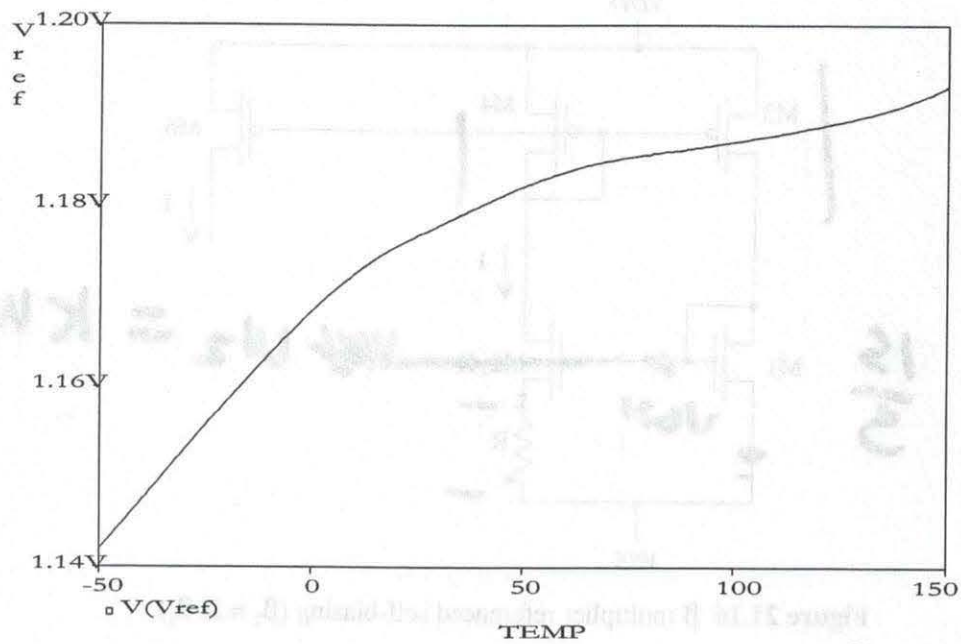


Figure 21.15 PSPICE simulation results of a bandgap voltage reference.

$$V_d \approx 0.7V$$

BUT depends on "I"

$$V_{REF} = \underline{\underline{1.25V}}$$

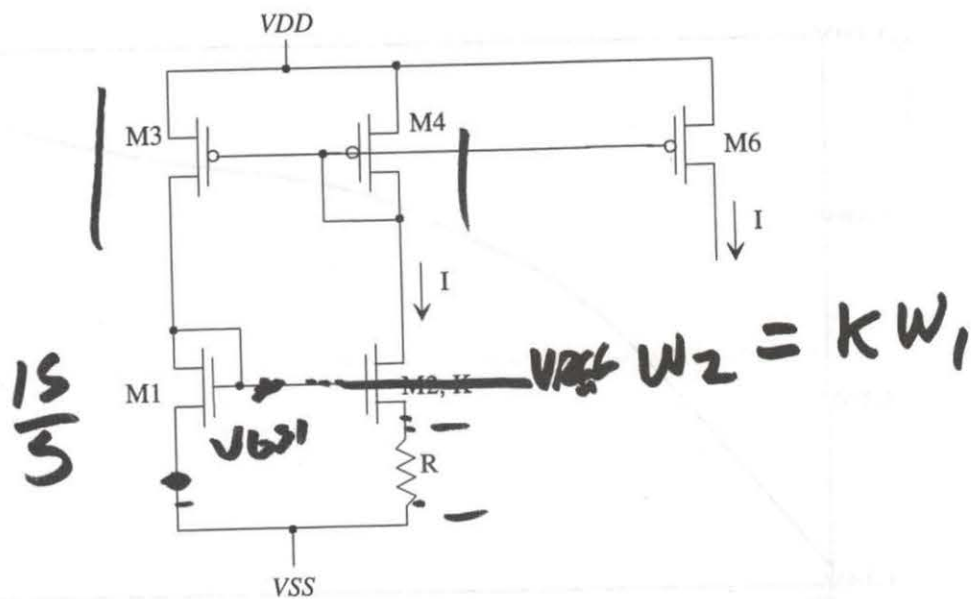
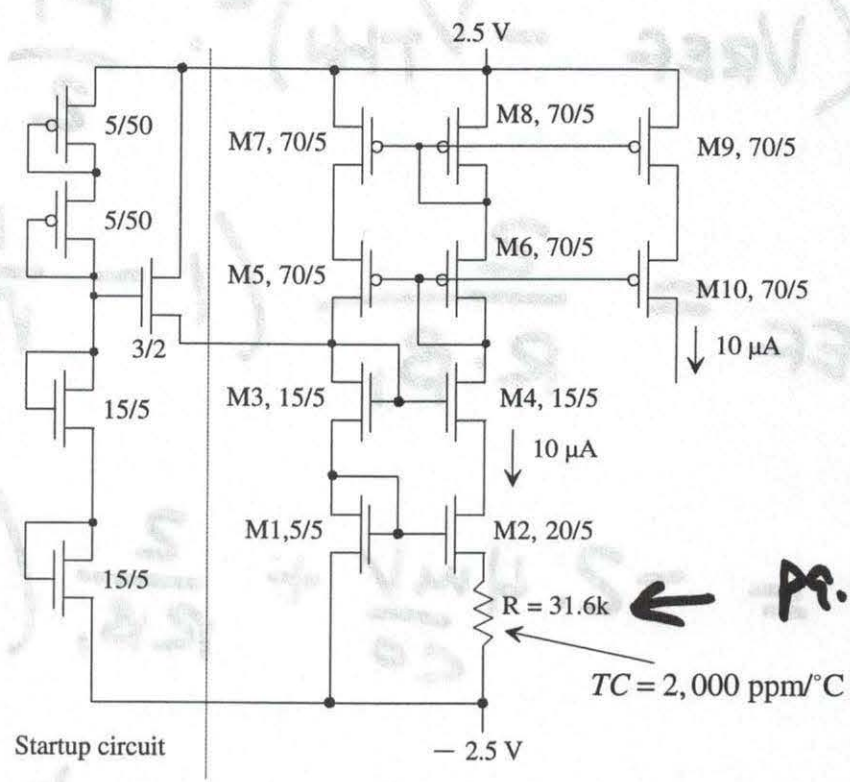


Figure 21.16  $\beta$  multiplier referenced self-biasing ( $\beta_2 = K \cdot \beta_1$ ).

$$I = \frac{V_{GS1} - V_{GS2}}{R}$$

$$I = \frac{2}{R^2 \cdot \beta_1} \left( 1 - \frac{1}{\sqrt{K}} \right)^2$$

$$TC_I = -4000 \text{ppm}/^\circ\text{C} + \frac{1.5}{T}$$



**Figure 21.17** A 10  $\mu\text{A}$  reference using a transconductance multiplier self-biased reference.

$$120V = \sqrt{2}V$$

$$= \left( \frac{1}{\sqrt{k}} - 1 \right) \cdot \frac{S}{R \cdot g} = I$$

pg. 481  
76

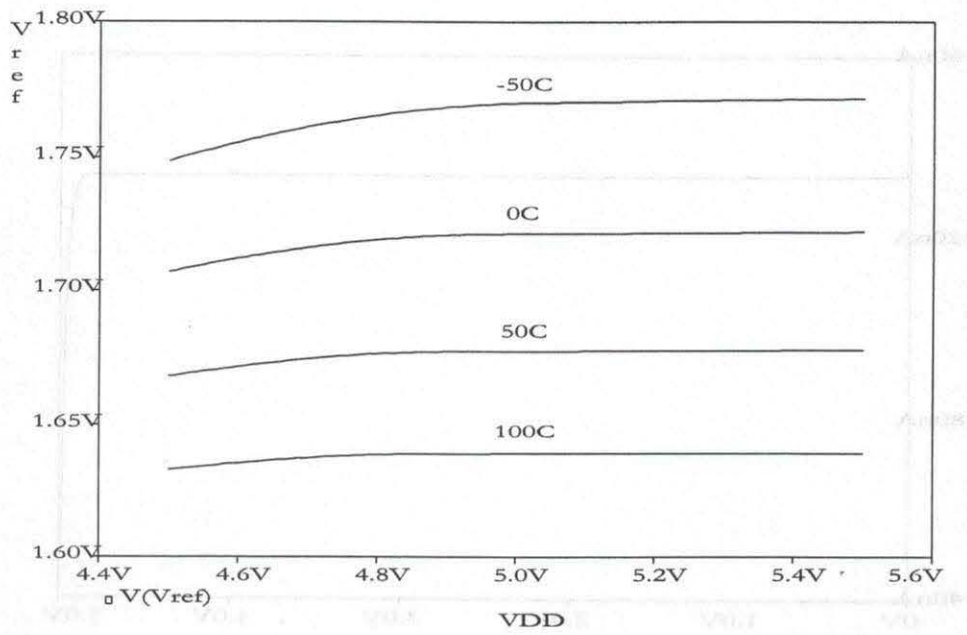
$$V_{REF} = V_{GS1}$$

$$I = \frac{2}{R^2 \beta_1} \cdot \left(1 - \sqrt{\frac{1}{K}}\right)^2 =$$

$$\frac{(V_{REF} - V_{THN})^2 \cdot \beta_1}{2}$$

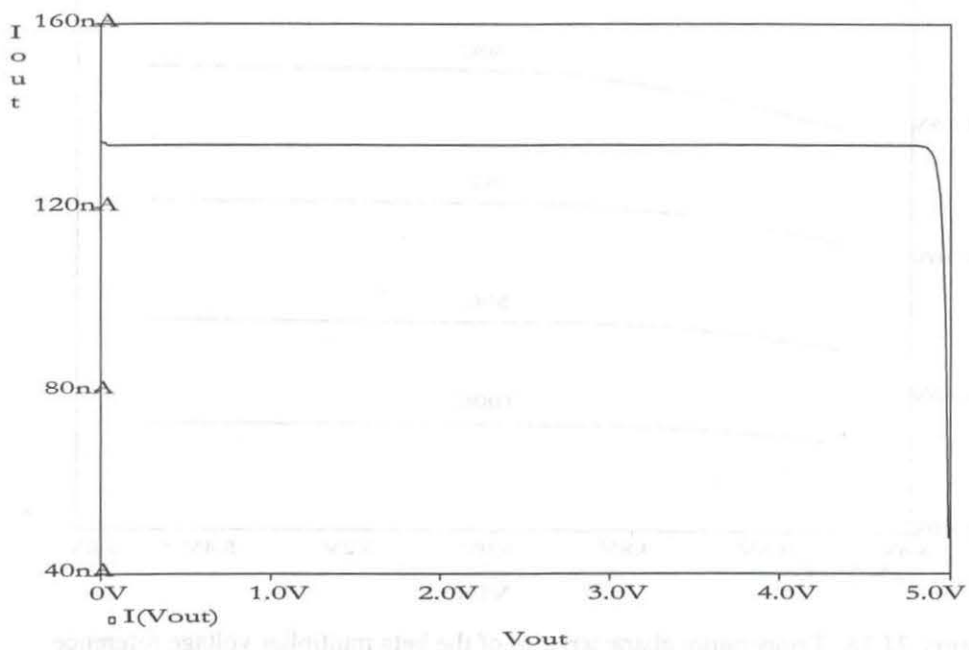
$$V_{REF} = \frac{2}{R \cdot \beta_1} \left(1 - \frac{1}{\sqrt{K}}\right) + \underbrace{V_{THN}}$$

$$\frac{dV_{REF}}{dT} = -2.4 \frac{\mu V}{^{\circ}C} + \frac{2}{R \beta_1} \left(1 - \frac{1}{\sqrt{K}}\right) \left(-2,000 \text{ ppm} + \frac{1.5}{T}\right)$$

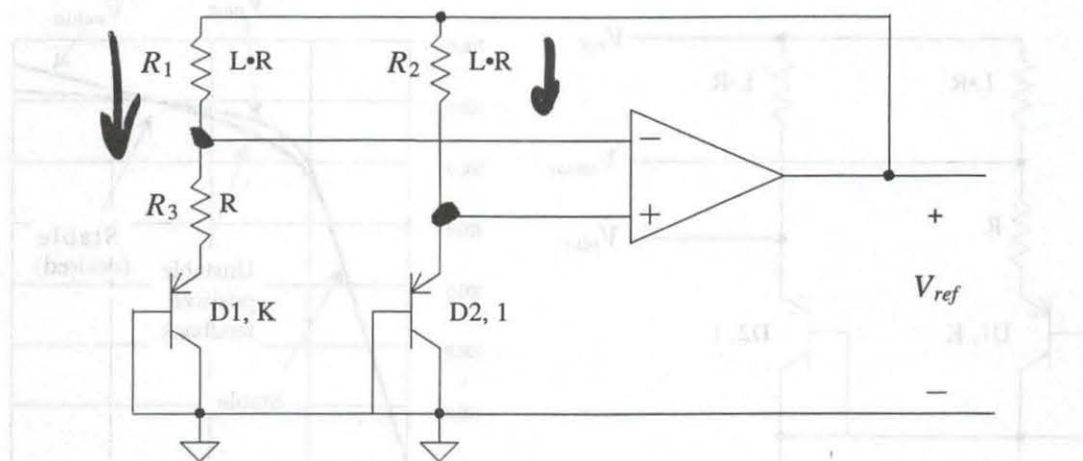


**Figure 21.18** Temperature characteristics of the beta multiplier voltage reference.

Figure 21.19 Simulation results of the beta multiplier voltage reference.



**Figure 21.19** Simulation results of Ex. 21.6, the design of a subthreshold current source.



A bandgap reference

Figure P21.13

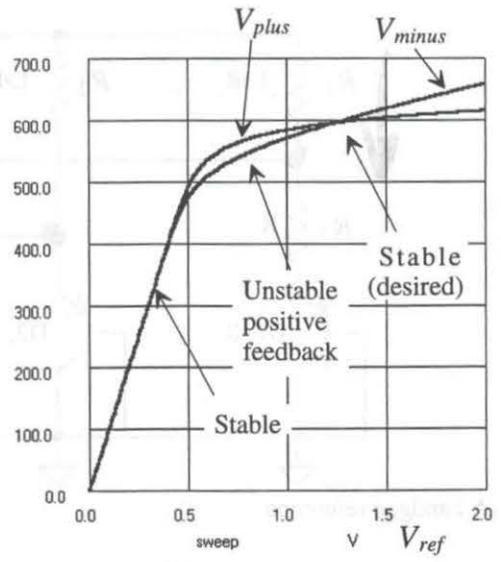
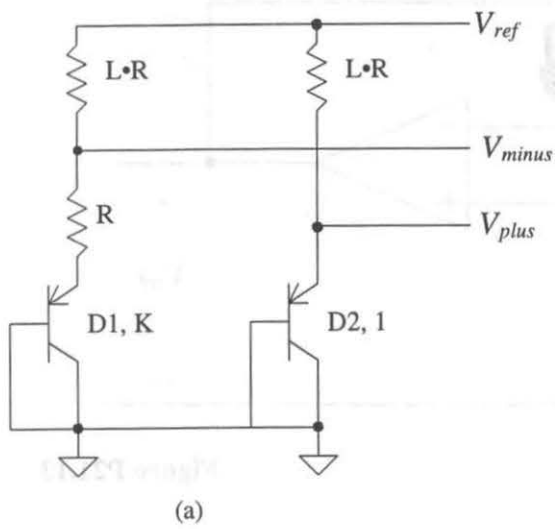


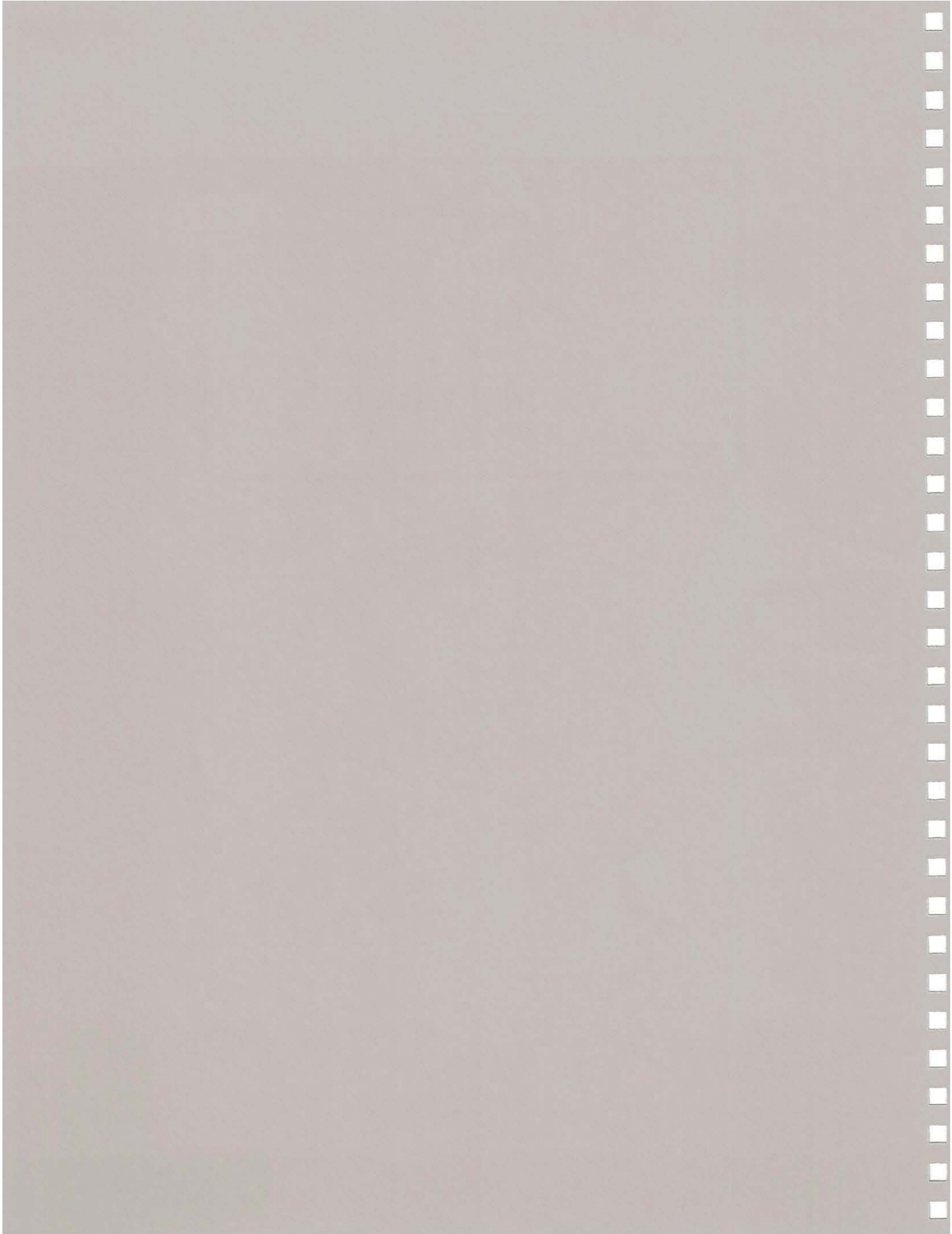
Figure P21.17



Lesson 6

Amplifiers

Tutorial Visuals



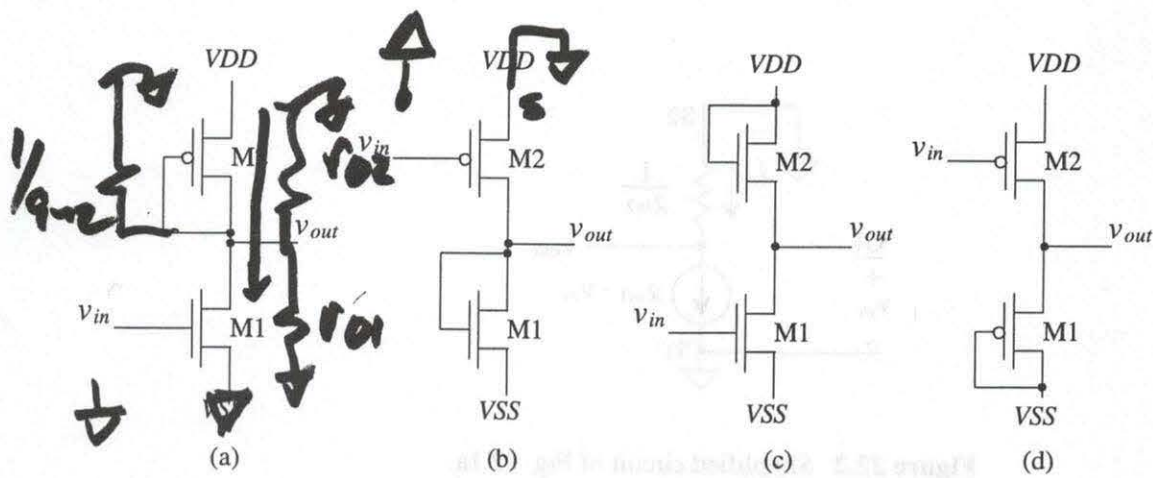
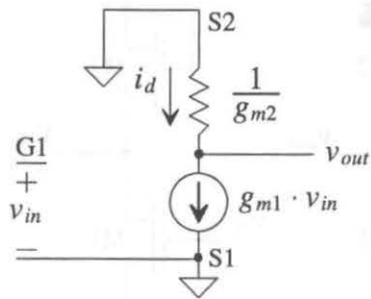


Figure 22.1 The four active load configurations available in CMOS.

$$i_d = g_{m1} \cdot v_{in}$$

$$v_{out} = -i_d \cdot \frac{1}{g_{m2}}$$

$$\frac{v_{out}}{v_{in}} = - \frac{\frac{1}{g_{m2}}}{\frac{1}{g_{m1}}} = \frac{\text{res. in dr}}{\text{res. in source}}$$



**Figure 22.2** Simplified circuit of Fig. 22.1a.

2. (10) The circuit shown in Fig. 22.1a is a simplified model of a two-stage CMOS amplifier. The input voltage  $V_{in}$  is the differential-mode input voltage, and the output voltage  $V_{out}$  is the differential-mode output voltage. The conductance  $G1$  is the conductance of the load resistor, and the conductance  $\frac{1}{g_{m2}}$  is the conductance of the load resistor of the second stage. The current  $i_d$  is the current through the load resistor of the second stage.

*Handwritten notes:*

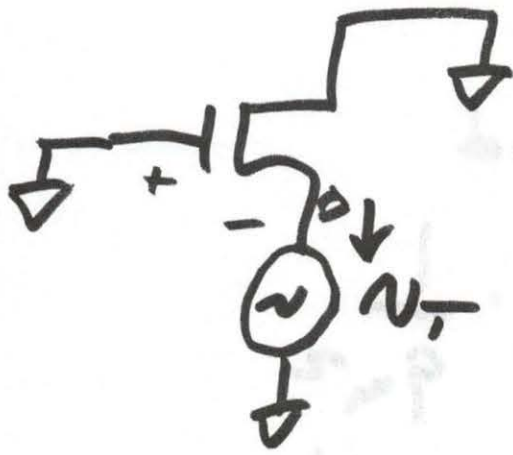
$i_d = g_{m2} \cdot V_{out}$

$\frac{1}{g_{m2}} \cdot i_d = V_{out}$

$\frac{1}{g_{m2}} \cdot g_{m2} \cdot V_{out} = V_{out}$

$\frac{1}{g_{m2}} \cdot g_{m2} \cdot V_{out} = V_{out}$

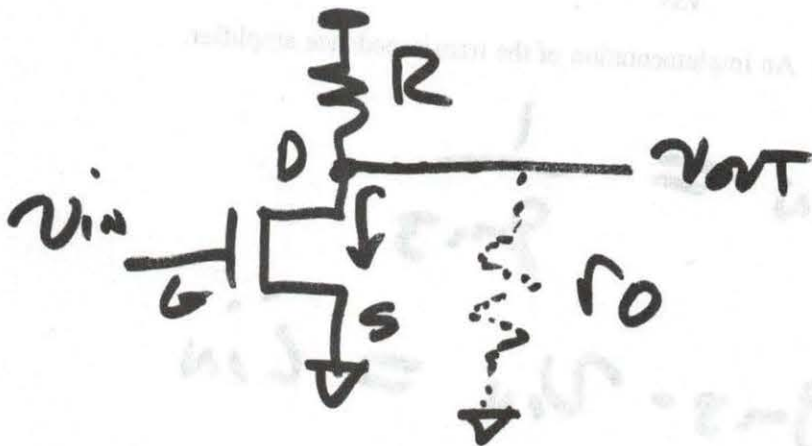
$\frac{1}{g_{m2}} \cdot g_{m2} \cdot V_{out} = V_{out}$



$$v_T = -v_{gs}$$

$$i_d = g_m v_{gs}$$

$$r_{\text{into source}} = -\frac{v_T}{i_T} = \frac{1}{g_m}$$



$$\frac{v_{OUT}}{v_{IN}} = -\frac{R \parallel r_o}{1/g_m}$$

$$v_{in} \cdot g_m = i_d$$

$$v_{out} = -i_d \cdot \frac{1}{g_{m2}}$$

$$\frac{v_{out}}{v_{in}} = \frac{-\frac{1}{g_{m2}}}{\frac{1}{g_{m1}}}$$

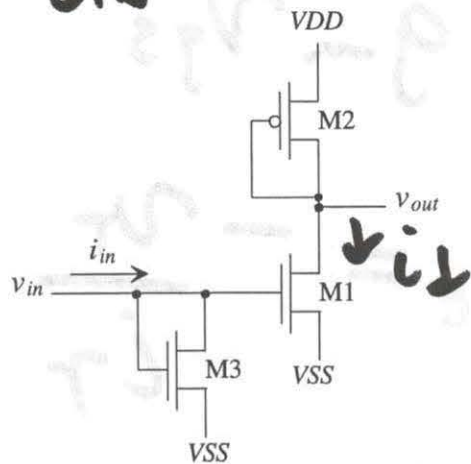
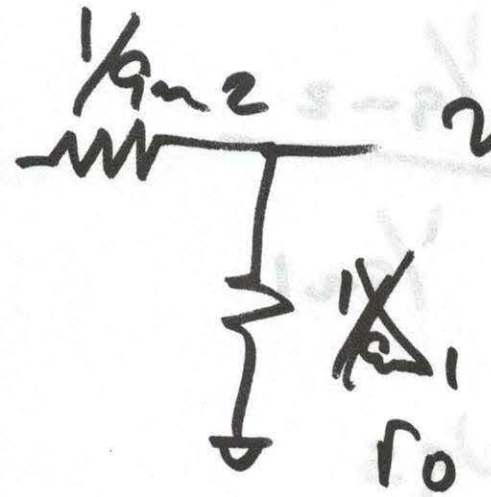


Figure 22.8 An implementation of the transimpedance amplifier.

$$R_{in} = \frac{1}{g_{m3}}$$

$$g_{m3} \cdot v_{in} = i_{in}$$

$$\frac{v_{out}}{i_{in}} = \frac{-\frac{1}{g_{m2}} \cdot \frac{1}{g_{m3}}}{\frac{1}{g_{m1}}}$$

$$v_{in} \cdot \frac{1}{k_{n2}} \quad v_{out} = \frac{v_{in} \cdot k_{n1}}{1/k_{n1} + 1/k_{n2}}$$


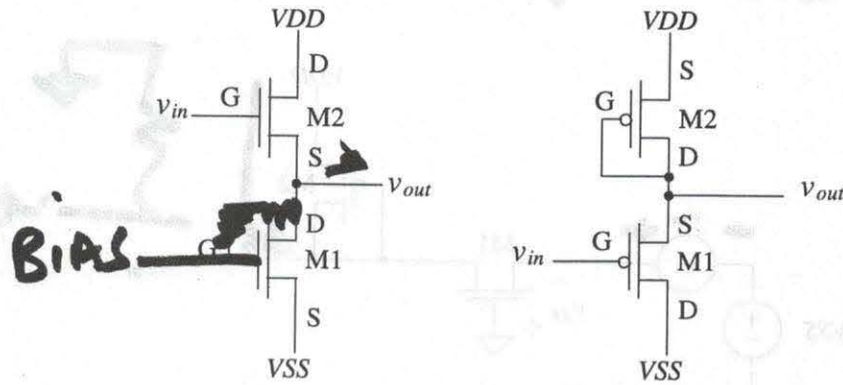


Figure 22.11 Source followers using active loads.

$$\frac{v_{out}}{v_{in}} = \frac{k_{n1}}{k_{n1} + k_{n2}}$$

$$\frac{v_o}{v_{in}} = \frac{1/g_{m2}}{1/g_{m1}}$$

$$v_{in} = -v_{gs}$$

$$i_d = g_m (-v_{in})$$

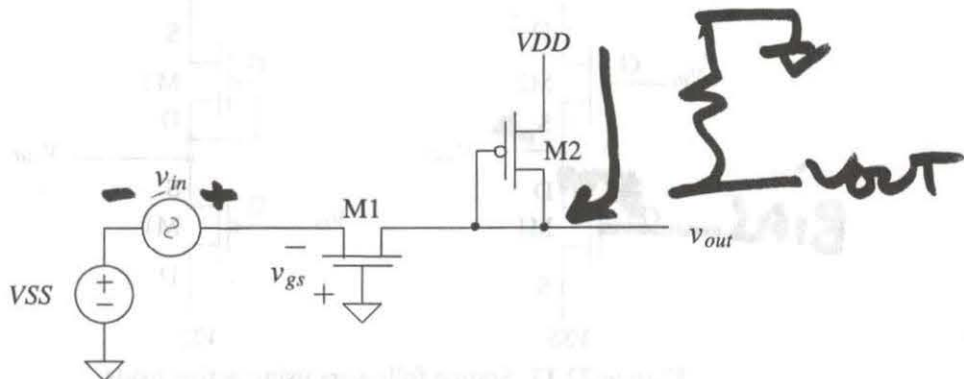


Figure 22.12 The common gate amplifier.

$$v_{out} = -i_d \cdot 1/g_{m2}$$

$$\frac{v_{out}}{v_{in}} = \frac{1/g_{m2}}{1/g_{m1}} = \frac{g_{m1}}{g_{m2}}$$



$$\frac{v_{out}}{v_{in}} = - \frac{r_{o1} \parallel r_{o2}}{1/g_{m1}} = -g_{m1}(r_{o1} \parallel r_{o2})$$

$$r_{o1} = \frac{1}{\lambda I}$$

$$= \frac{-\sqrt{2\beta_1 I_0}}{I_0(\lambda_1 + \lambda_2)} = \frac{\sqrt{2\beta_1}}{\sqrt{I_0}(\lambda_1 + \lambda_2)}$$

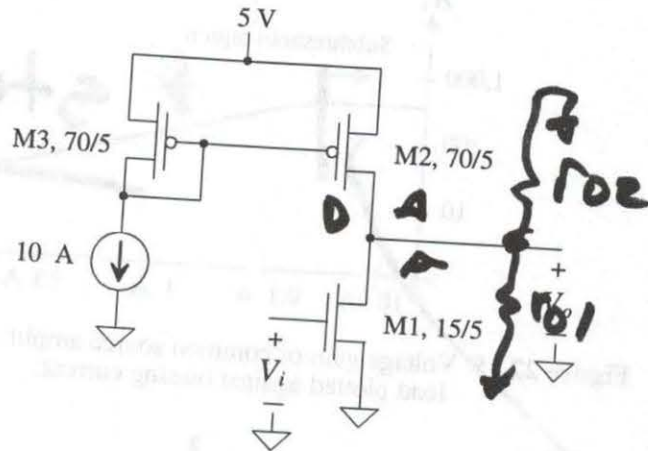


Figure 22.13 Common source amplifier with current source load.

Gain  $\uparrow$  Speed  $\downarrow$

$$f_T \propto \frac{(V_{GS} - V_T)}{L^2}$$

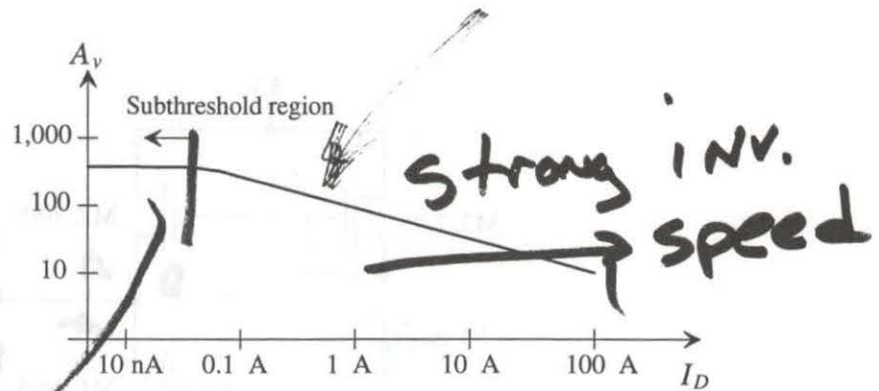


Figure 22.15 Voltage gain of common source amplifier with current source load plotted against biasing current.

$$r_o = \frac{1}{\lambda I}$$

$$g_m / \text{subthresh} = \left( \frac{V_T}{I} \right)^{-1}$$

$$g_m r_o$$

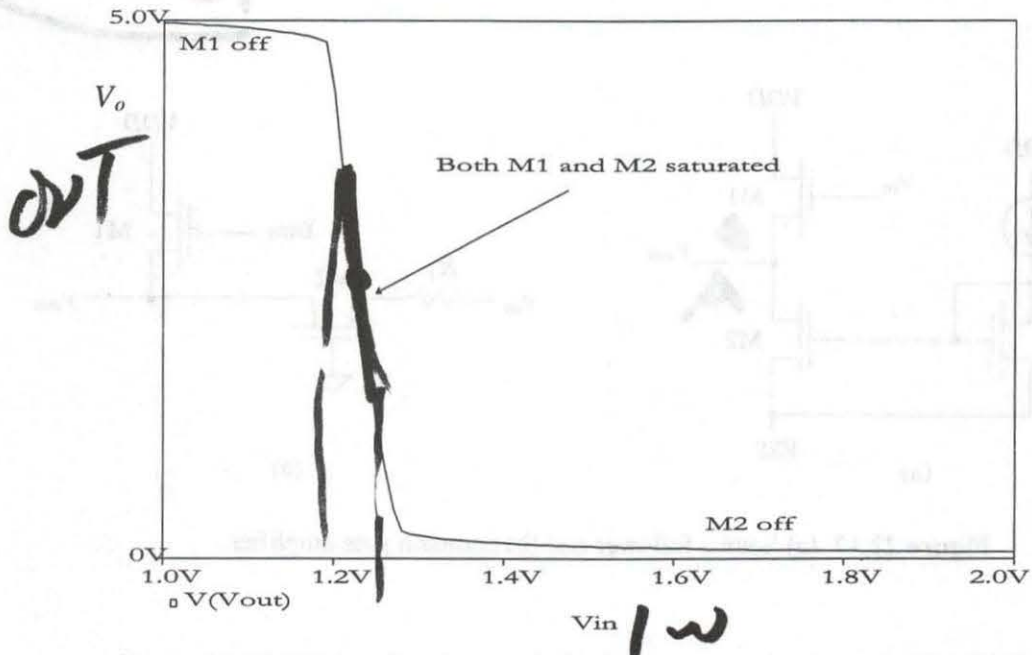
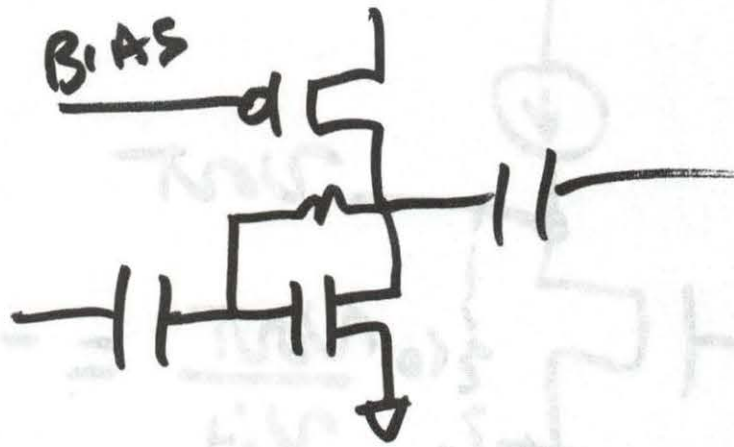


Figure 22.14 DC transfer characteristics for the amplifier shown in Fig. 22.11.

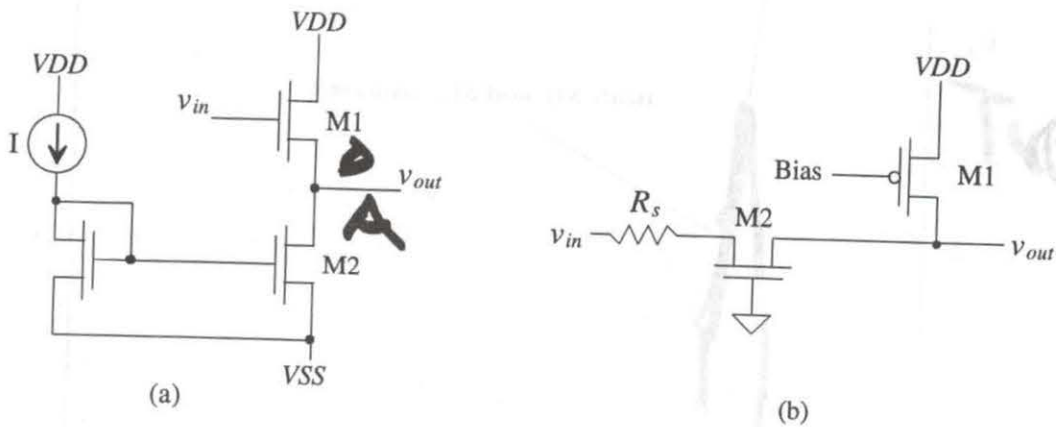
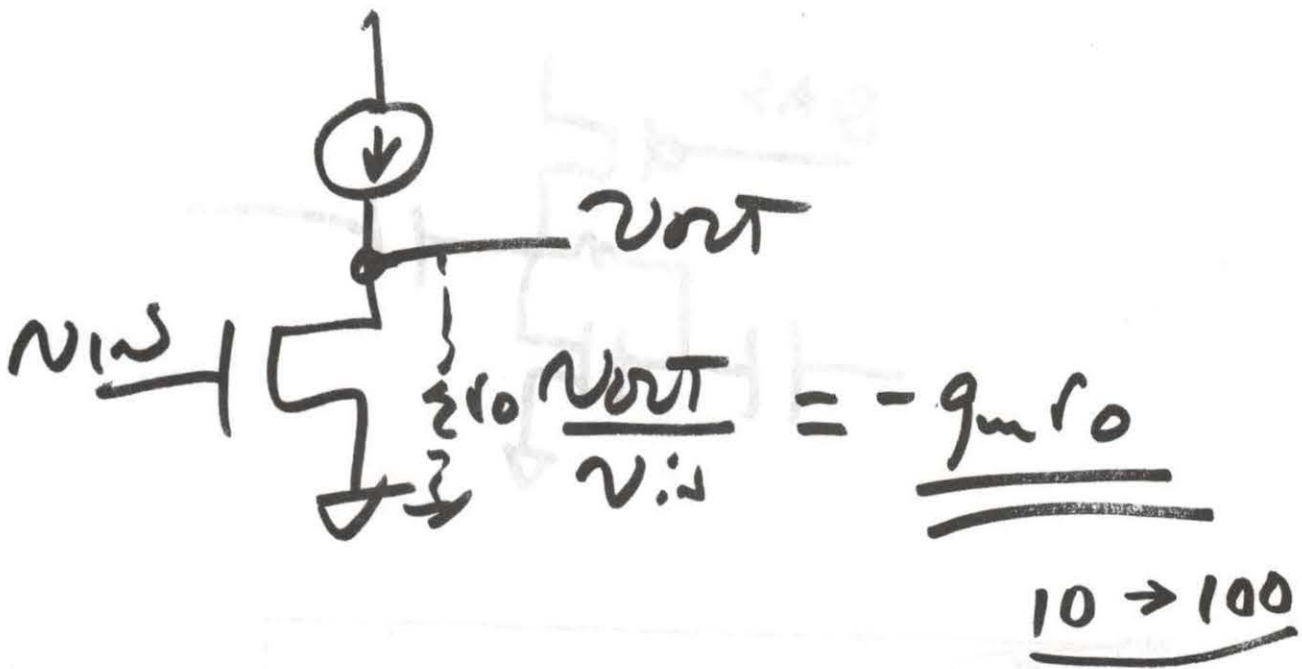


Figure 22.17 (a) Source follower and (b) common gate amplifier.

$\frac{1}{g_{m1}} \quad r_{o2}$

$$\frac{v_{out}}{v_{in}} = \frac{r_{o2}}{r_{o2} + \frac{1}{g_{m1}}} \approx 1$$

$r_{o2} \gg \frac{1}{g_{m1}}$

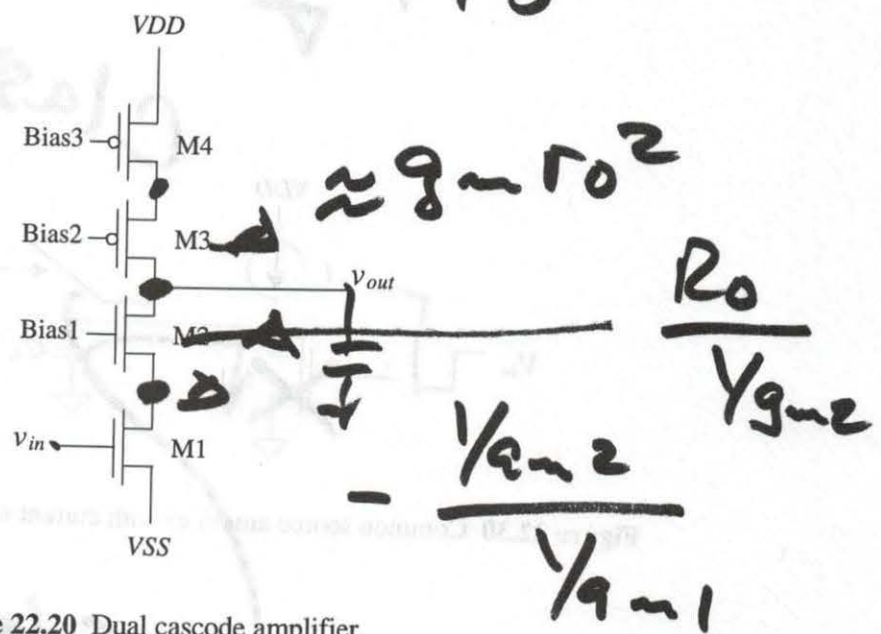
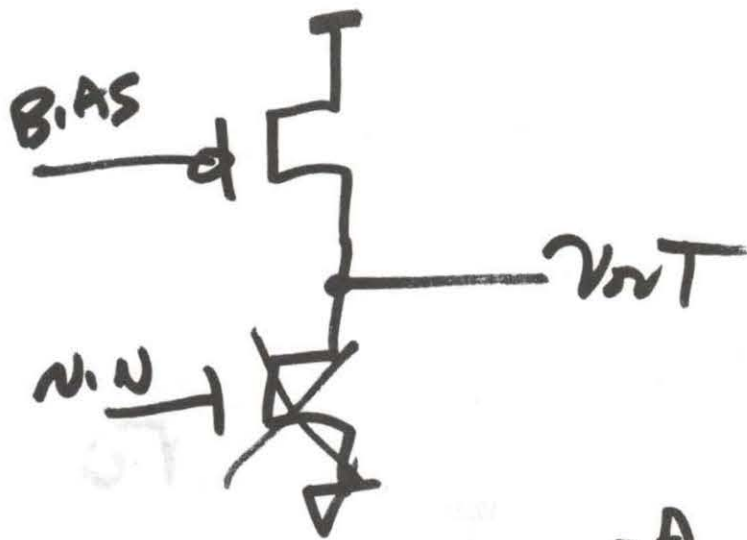


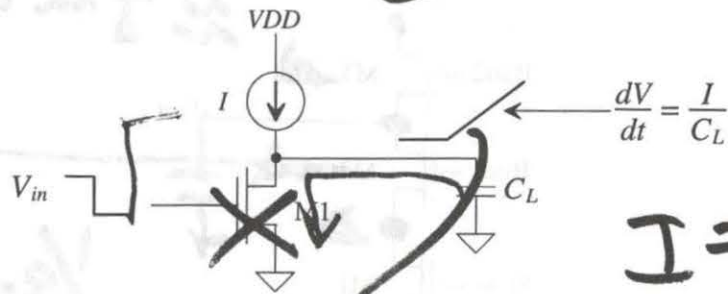
Figure 22.20 Dual cascode amplifier.

$$v_{out} = - \frac{R_o}{Y_{gm1}}$$

$$= -g_{m1} R_o$$



Class A



$$I = C_L \frac{dV}{dt}$$

Figure 22.30 Common source amplifier with current source load.

slew-rate limit

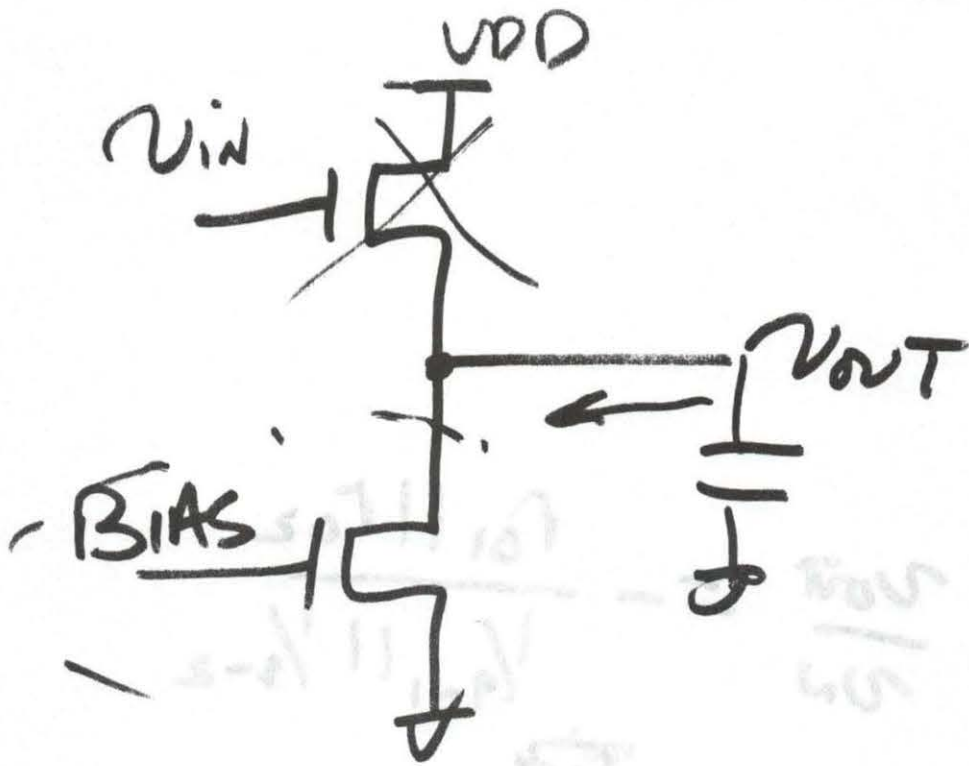


Figure 23.22 The differential amplifier

1) Biasing the DC  
 Bias flowing in  
 M1 M2

$$\frac{v_{out}}{v_{in}} = - \frac{r_{o1} \parallel r_{o2}}{1/g_{m1} \parallel 1/g_{m2}}$$

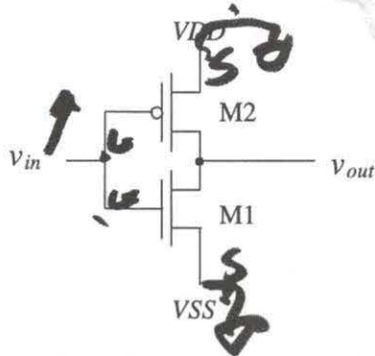


Figure 22.22 The push-pull amplifier.

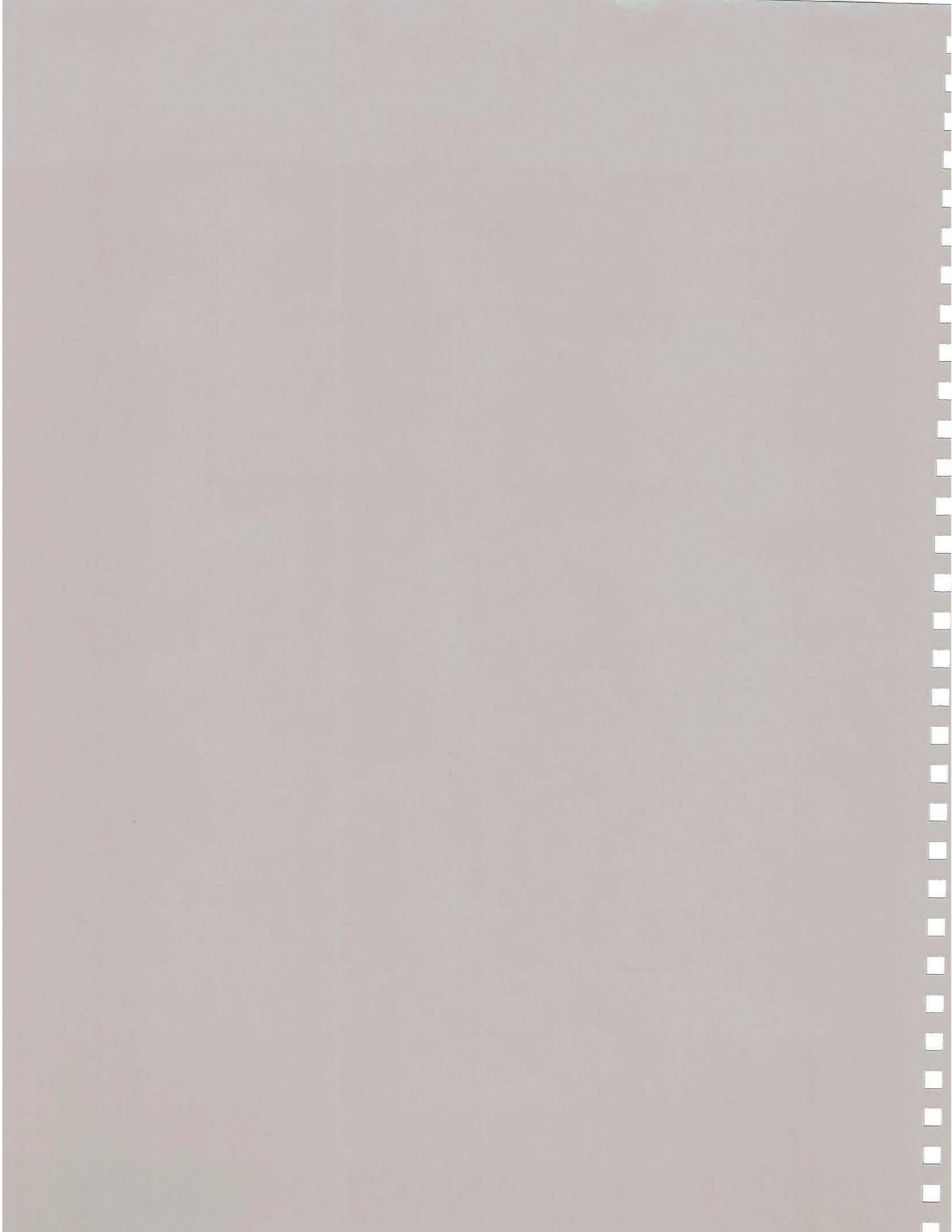
1) setting the DC  
BIAS flowing in ~~the~~  
~~the~~ M1 & M2



# Lesson 7

## Differential Amplifiers

### Tutorial Visuals



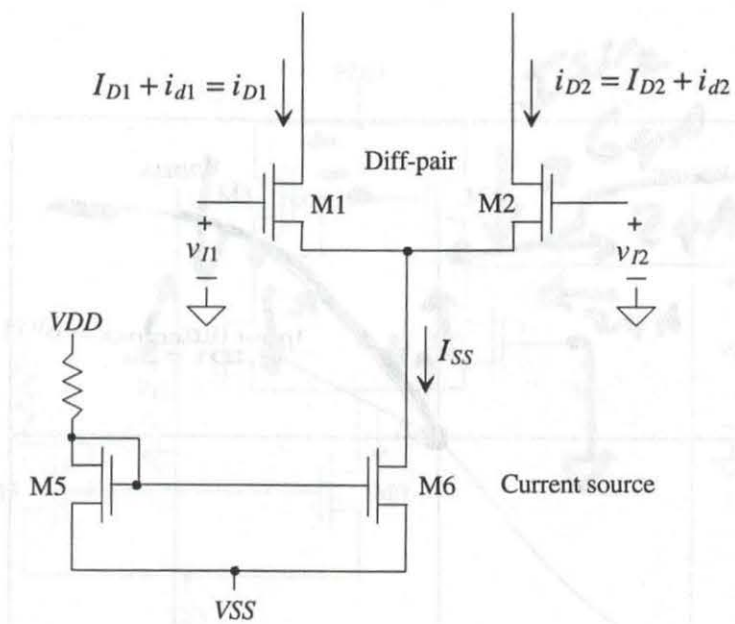
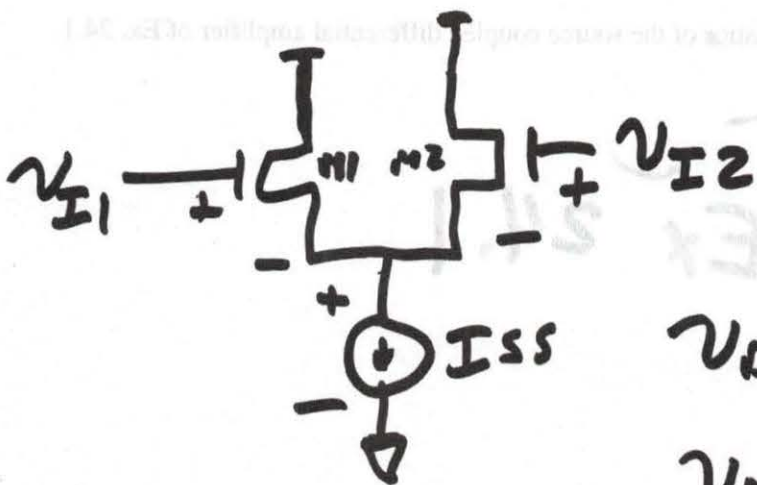


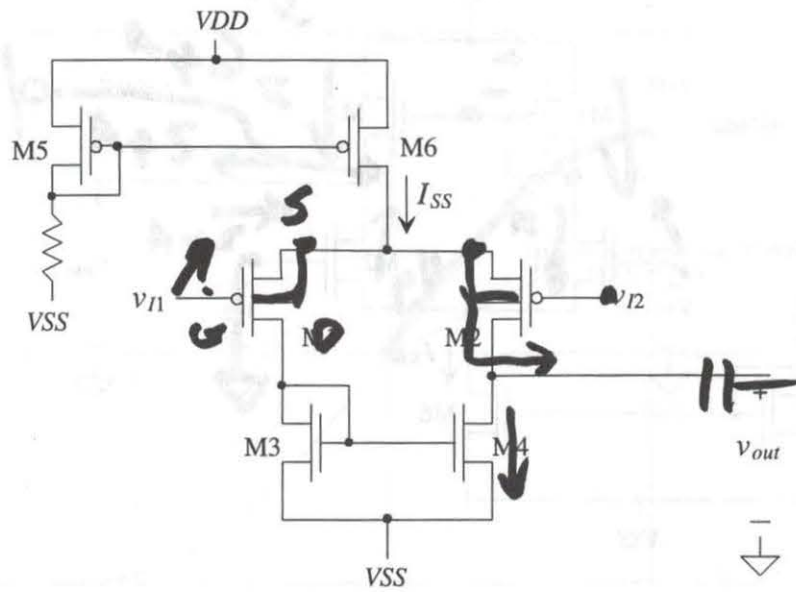
Figure 24.1 Differential amplifier.



$$v_{DI} = v_{I1} - v_{I2}$$

$$v_{DI} \times$$

EX. 24.1



**Figure 24.4** P-channel differential amplifier.

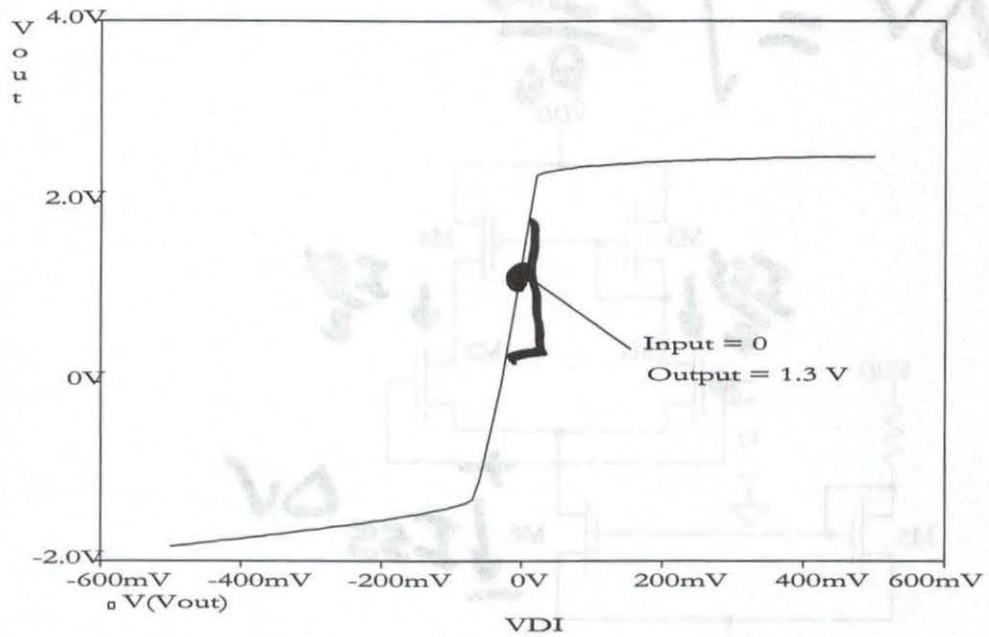
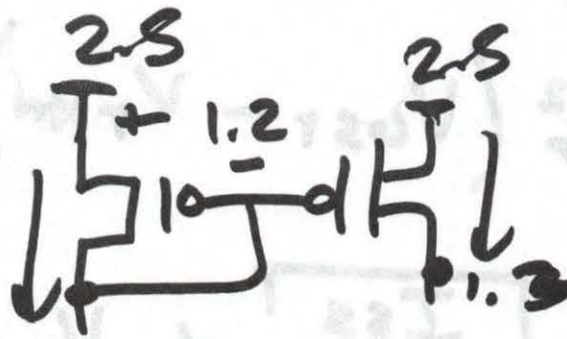


Figure 24.5 DC sweep of the differential amplifier of Ex. 24.2.

$$\frac{I_{SS}}{2} = \frac{\beta_{1,2}}{2} (V_{GS1} - V_{THN})^2$$

$$V_{GS1} = \sqrt{\frac{I_{SS}}{\beta_1}} + V_{THN}$$

$$\Delta V = \sqrt{\frac{2I_{SS}}{\beta_6}}$$

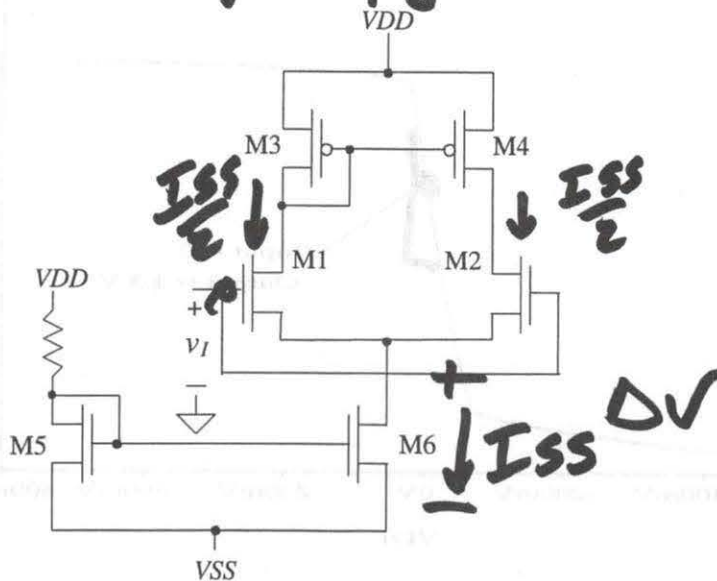


Figure 24.6 Differential amplifier configuration used to determine input common-mode range.

$$V_{Imin} = \sqrt{\frac{I_{SS}}{\beta_1}} + V_{THN} + \sqrt{\frac{2I_{SS}}{\beta_6}} + V_{SS}$$

$$V_{Imax} = VDD - \sqrt{\frac{I_{SS}}{\beta_3}}$$

$$v_{I1} = v_{gs1} - v_{gs2}$$

$$= \frac{i_{d1}}{g_{m1,2}} - \frac{i_{d2}}{g_{m1,2}}$$

$$= \frac{2i_d}{g_m}$$

$$i_d = i_{d1} = -i_{d2}$$

$$g_m = g_{m1,2} = g_{m1,2}$$

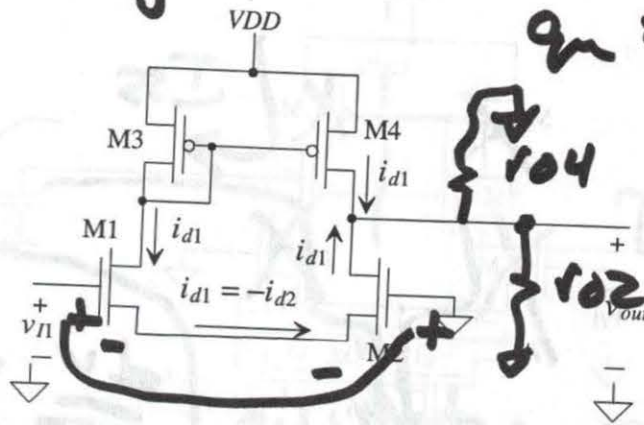


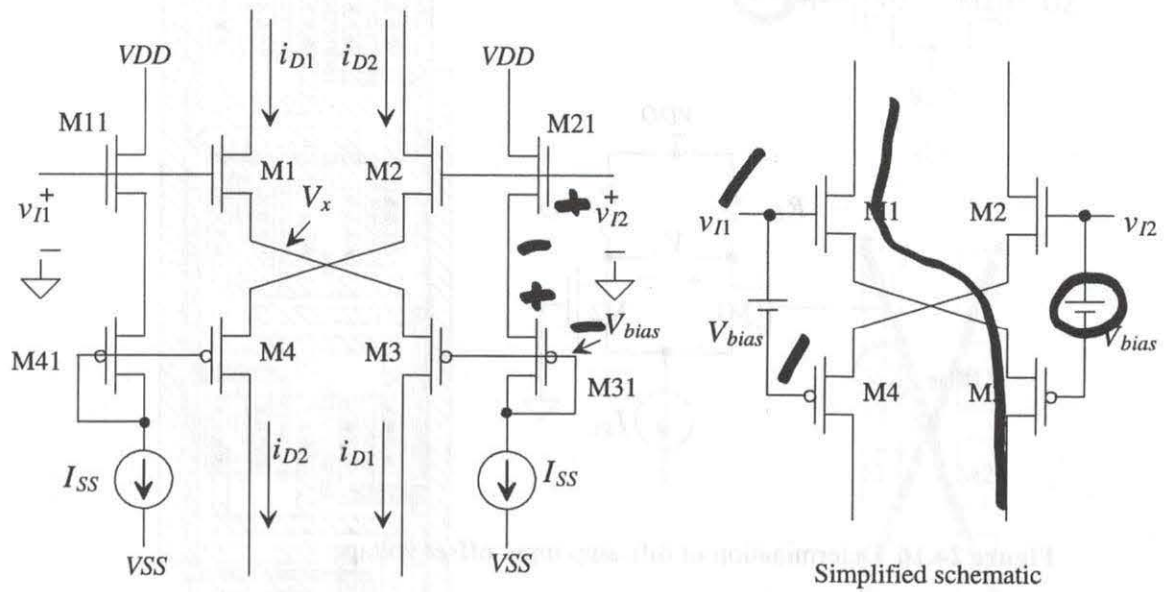
Figure 24.8 Differential amplifier with AC currents shown.

$$v_{OUT} = 2i_d \cdot (r_{o4} || r_{o2})$$

$$\frac{v_{OUT}}{v_{I1}} = g_m (r_{o4} || r_{o2})$$

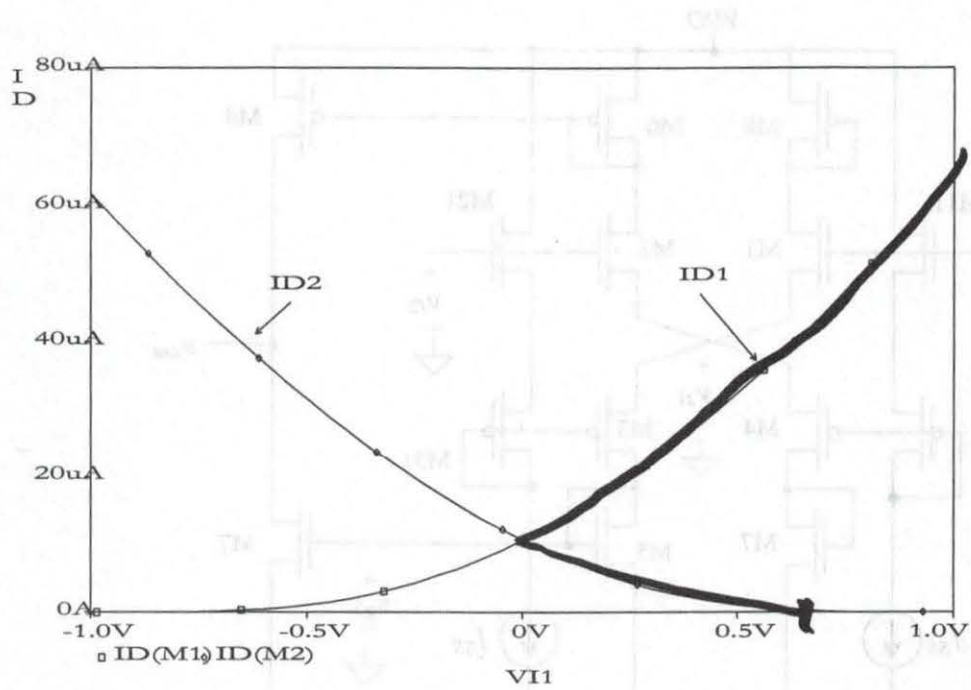
$$g_m = \sqrt{2 \cdot \beta_{1,2} \cdot \frac{I_{SS}}{2}}$$

$$= \sqrt{\beta_{1,2} \cdot I_{SS}}$$



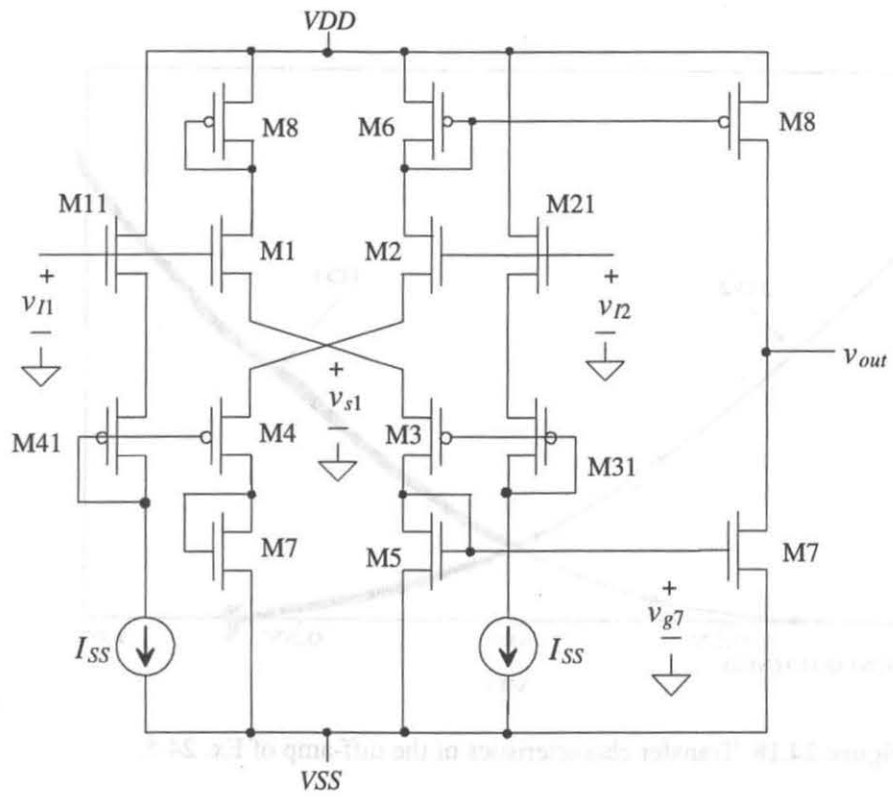
**Figure 24.17** Source cross-coupled differential amplifier, n-channel input devices.





**Figure 24.18** Transfer characteristics of the diff-amp of Ex. 24.5.

Figure 24.18 Source-coupled differential amplifier with current source load.



**Figure 24.20** Source cross-coupled differential amplifier, with current source loads.

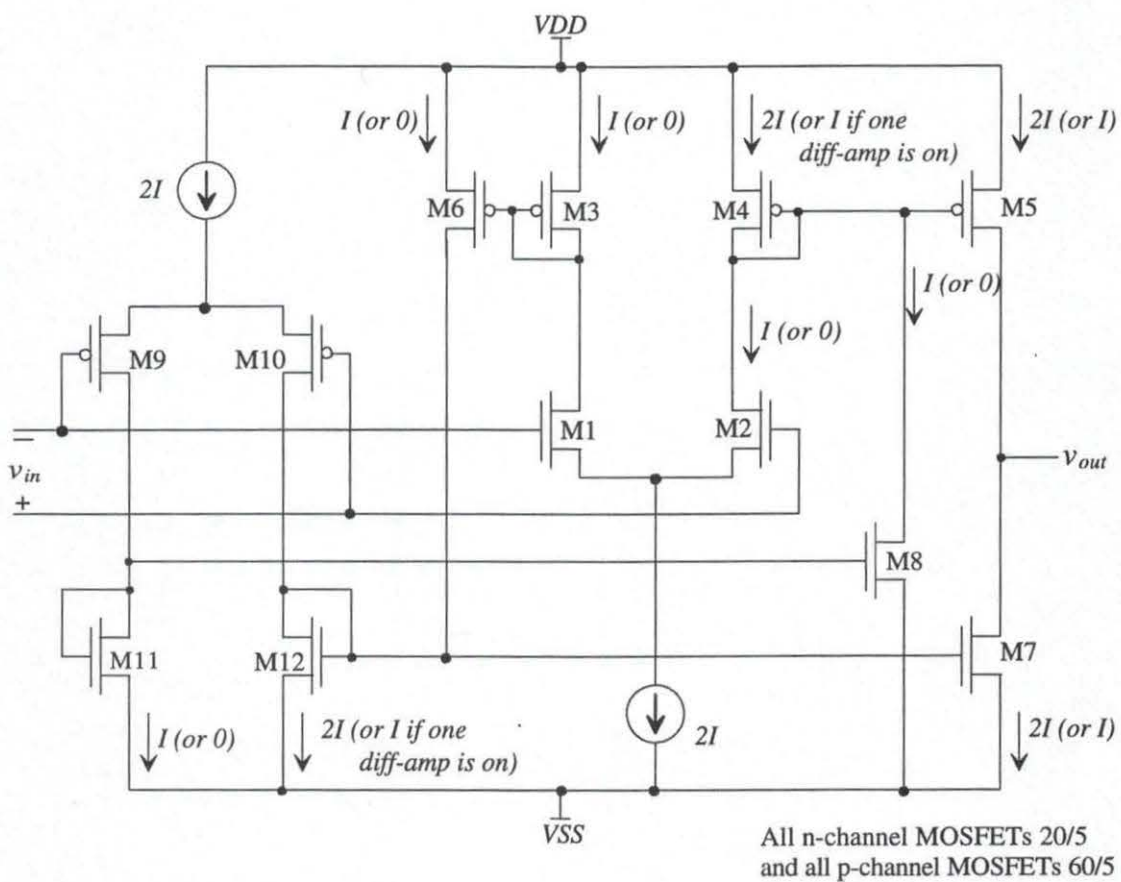


Figure 24.26 Two parallel differential amplifiers used to increase input swing.



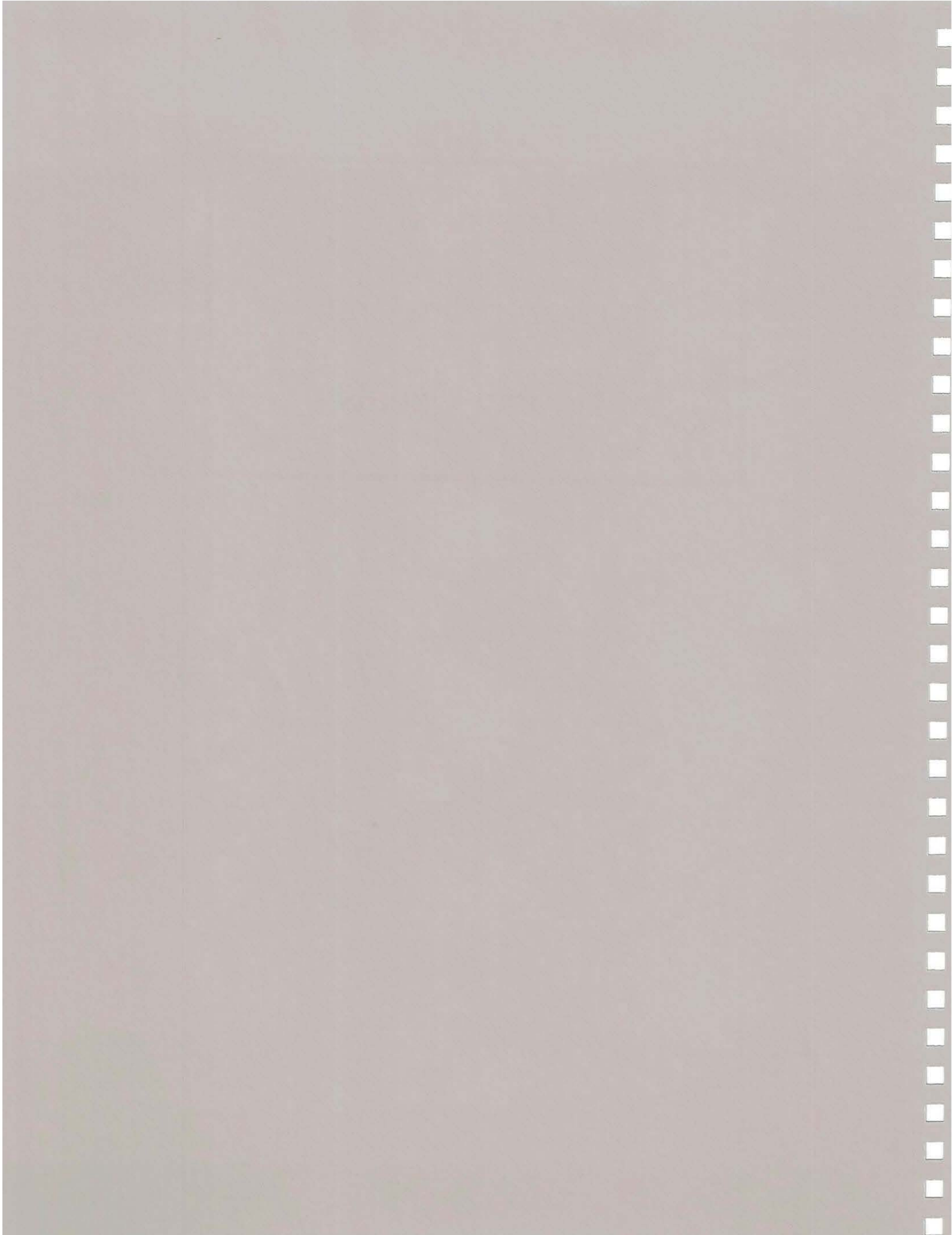
Figure 24.58 The pair of differential amplifiers used to increase input range

Figure 24.58 The pair of differential amplifiers used to increase input range

Lesson 8

Op-amp Design I

Tutorial Visuals



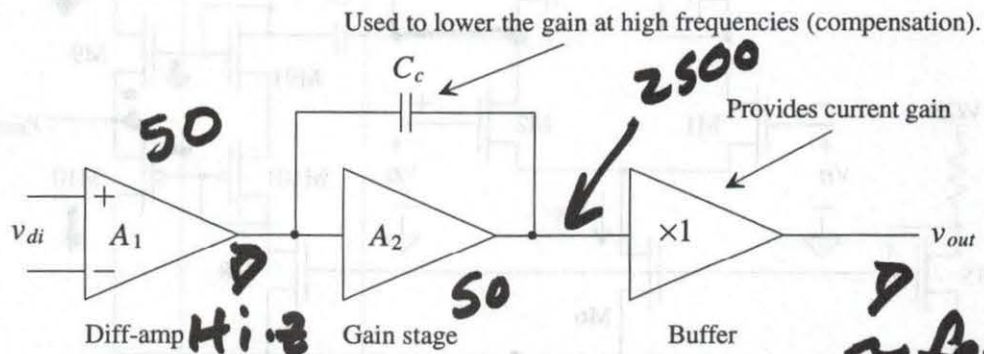
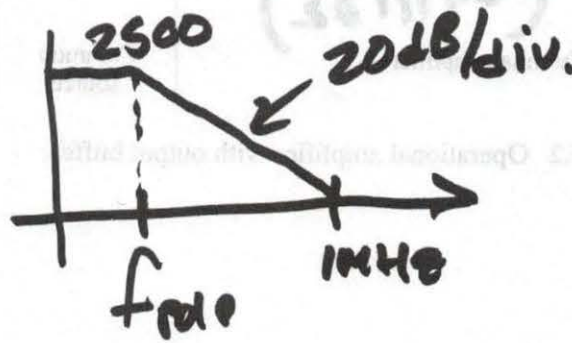


Figure 25.1 Block diagram of two-stage op-amp with output buffer.



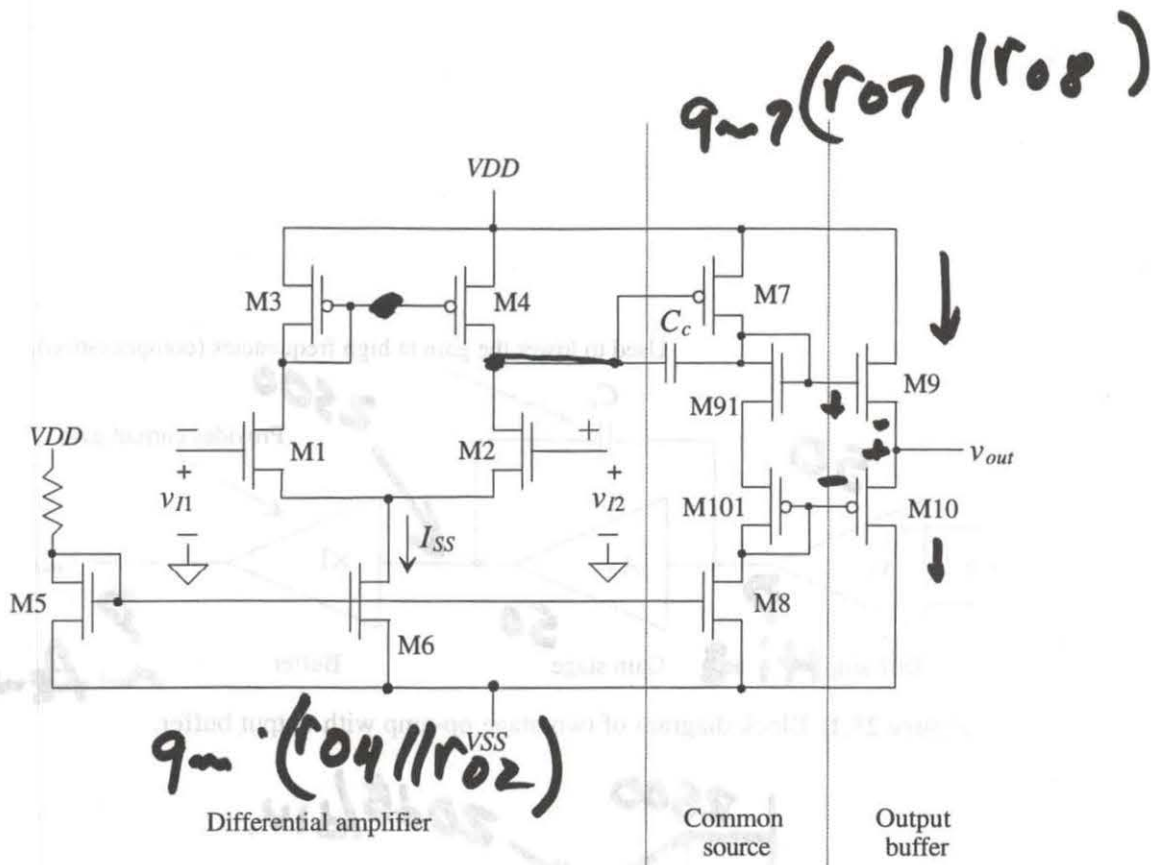


Figure 25.2 Operational amplifier with output buffer.



$$A_{OL} \Big|_{DC} = g_{m1} \cdot (r_{o2} \parallel r_{o4}) \cdot g_{m7} (r_{o7} \parallel r_{o8})$$

All device lengths are 5 m except output buffer, which uses L = 2 m since the output resistance is less important.

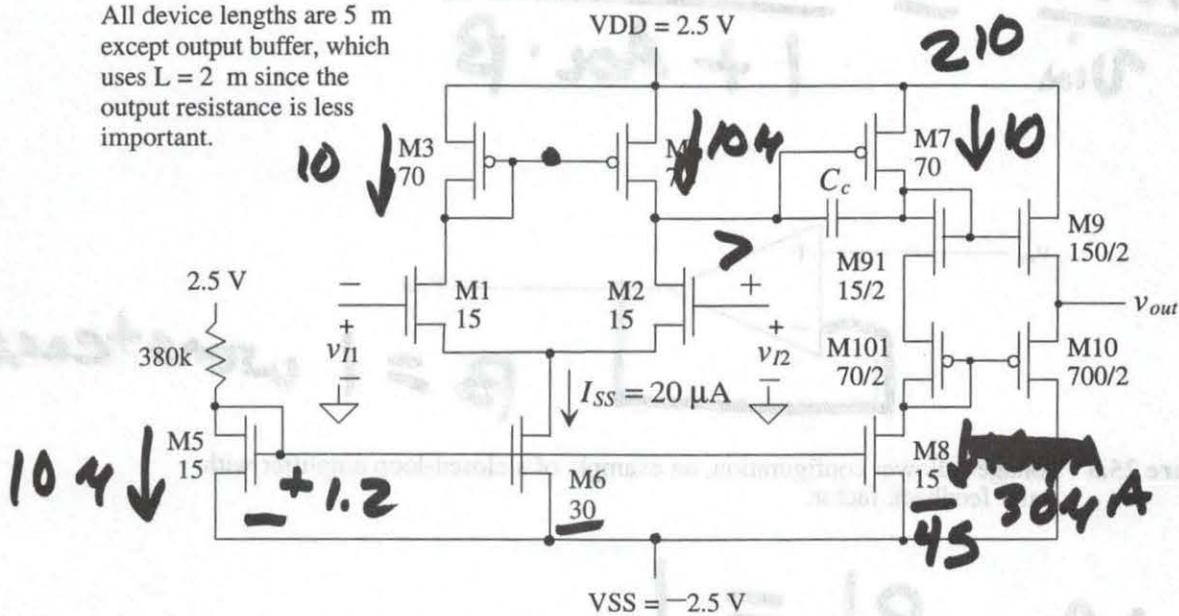
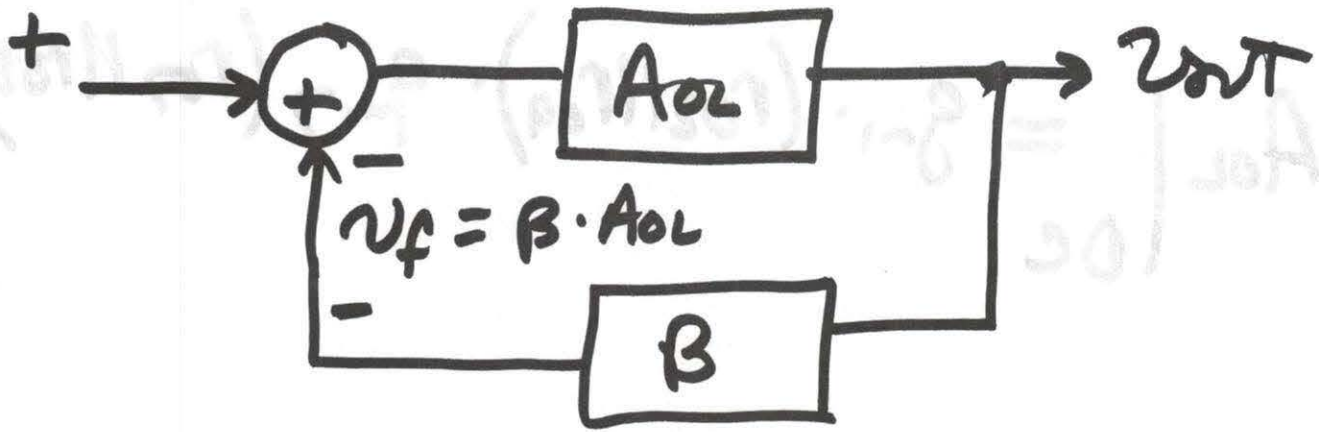


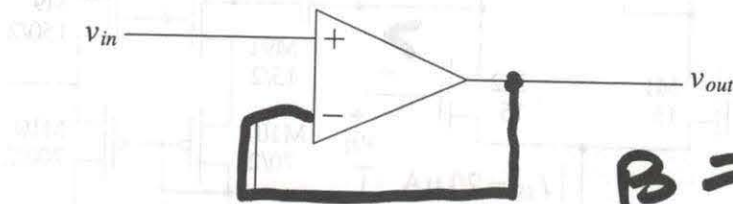
Figure 25.3 Operational amplifier with sizes.

$$f_{pole} = \frac{1}{2\pi (r_{o2} \parallel r_{o4}) \cdot C_c (1 + |A_{ol}|)}$$

$$C_c = \frac{g_{m1}}{2\pi f_u}$$



$$\frac{v_{out}}{v_{in}} = \frac{A_{OL}}{1 + A_{OL} \cdot \beta}$$



$\beta = 1$  worst case

Figure 25.5 Voltage follower configuration, an example of a closed-loop amplifier with unity feedback factor.

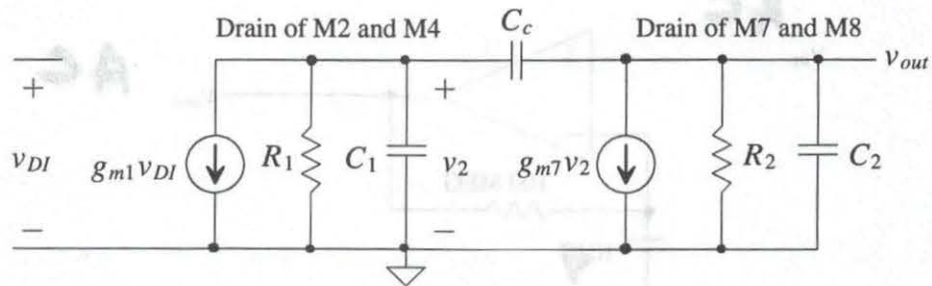
$$|A_{OL} \cdot \beta| = 1$$

$$\angle A_{OL} \cdot \beta = 180^\circ$$

$$A_{OL} \cdot \beta = -1$$

$$A_{OL} = 1$$

$$A_{OL} = 180^\circ$$



**Figure 25.6** Small-signal model of two-stage op-amp.

$$V_{OS} = 1\text{mV}$$

$$A_{OL}|_{AC} = 10,000$$

$$A_{OL} = \frac{v_{out}}{v_{in} - v_{E}} \circ$$

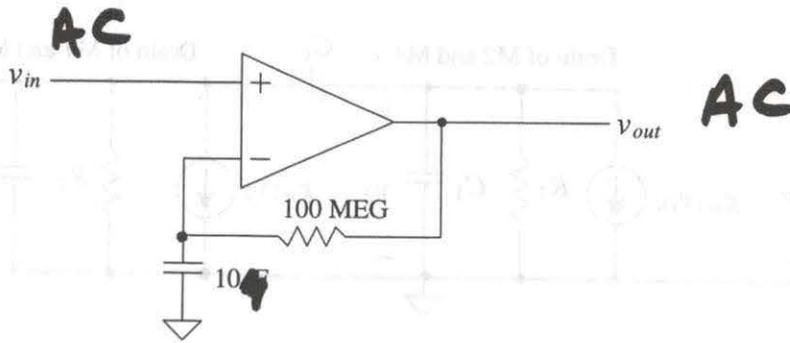
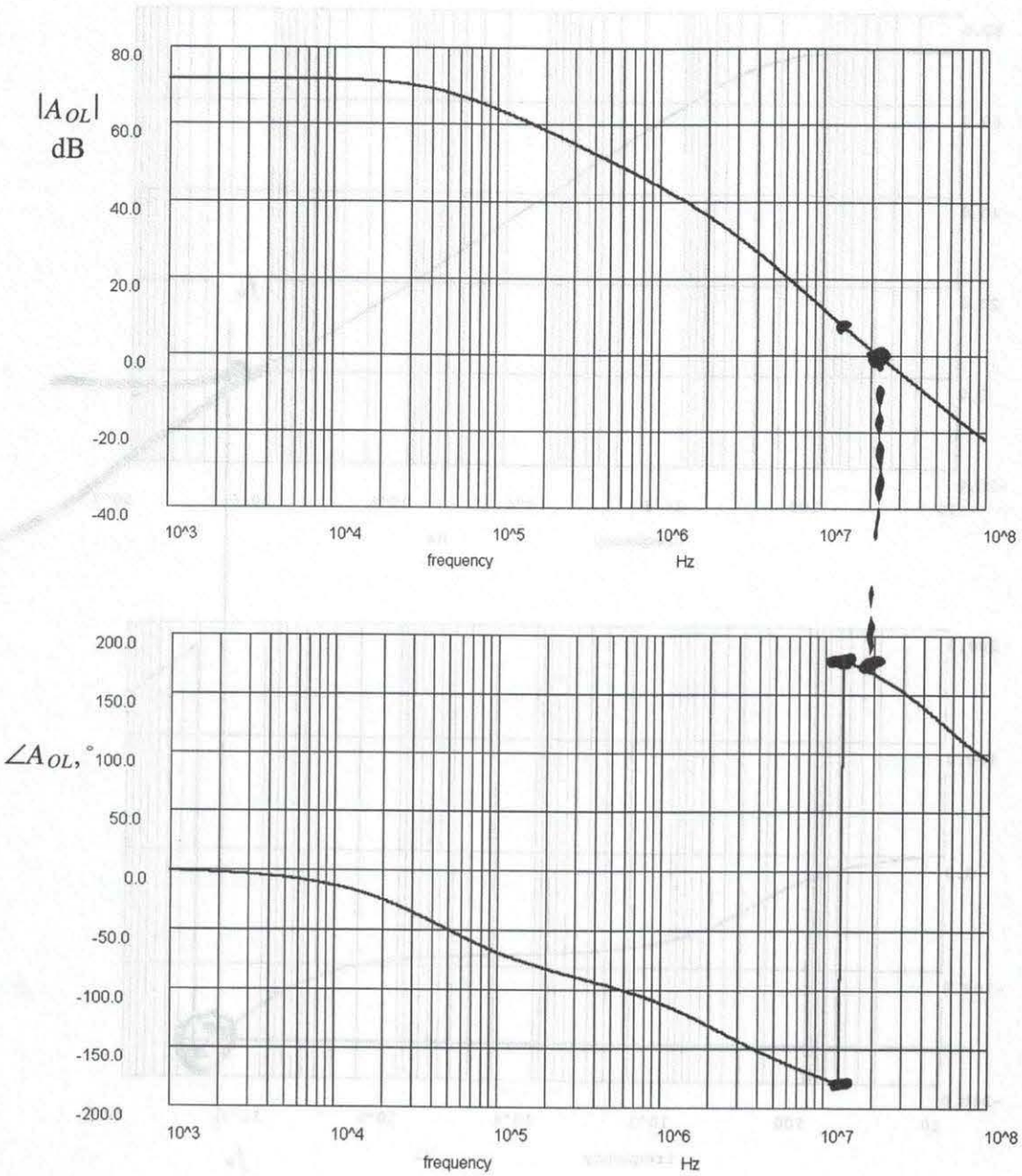
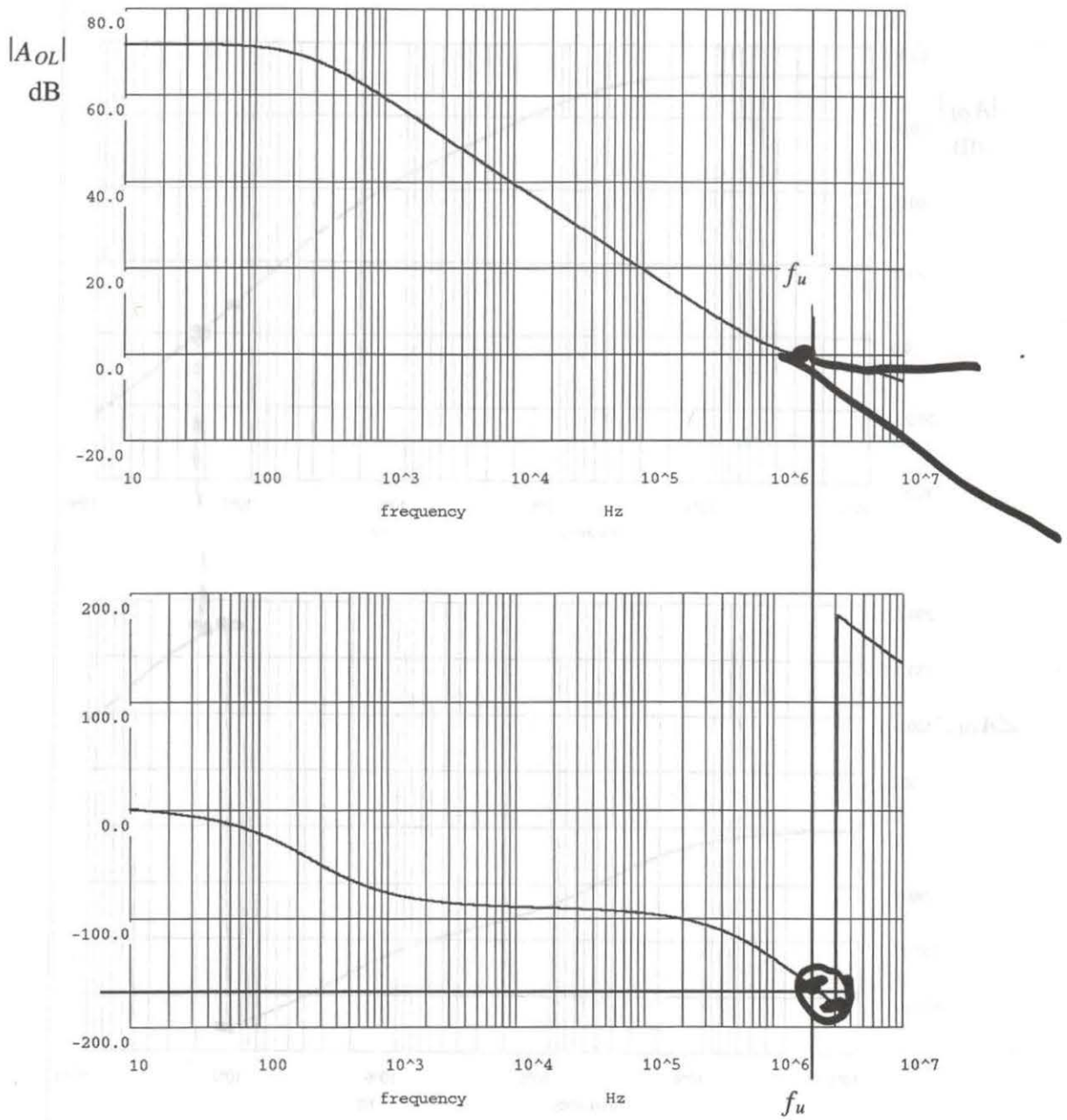


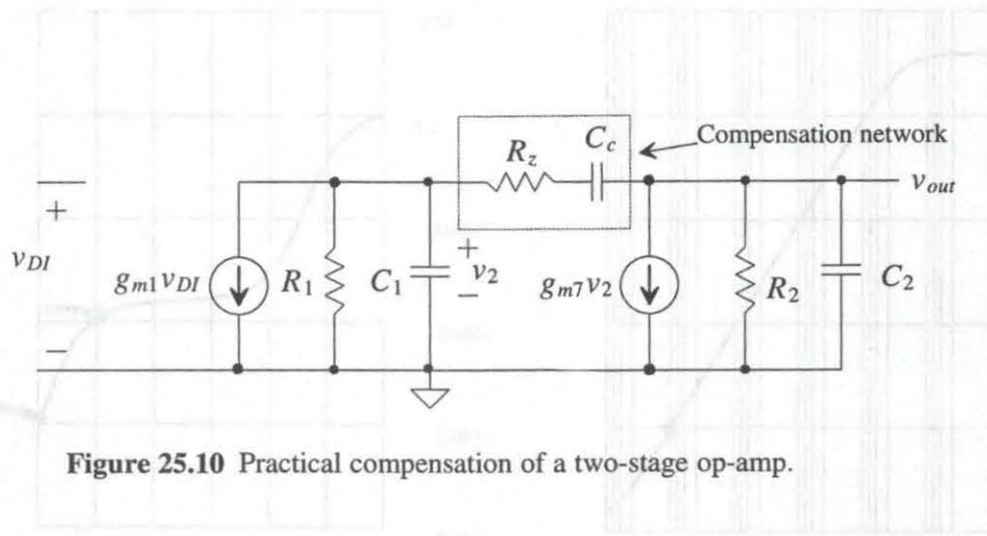
Figure 25.7 Circuit configuration used to measure open-loop gain and frequency response.



**Figure 25.8** Open-loop uncompensated frequency response of the amplifier of Fig. 25.3.

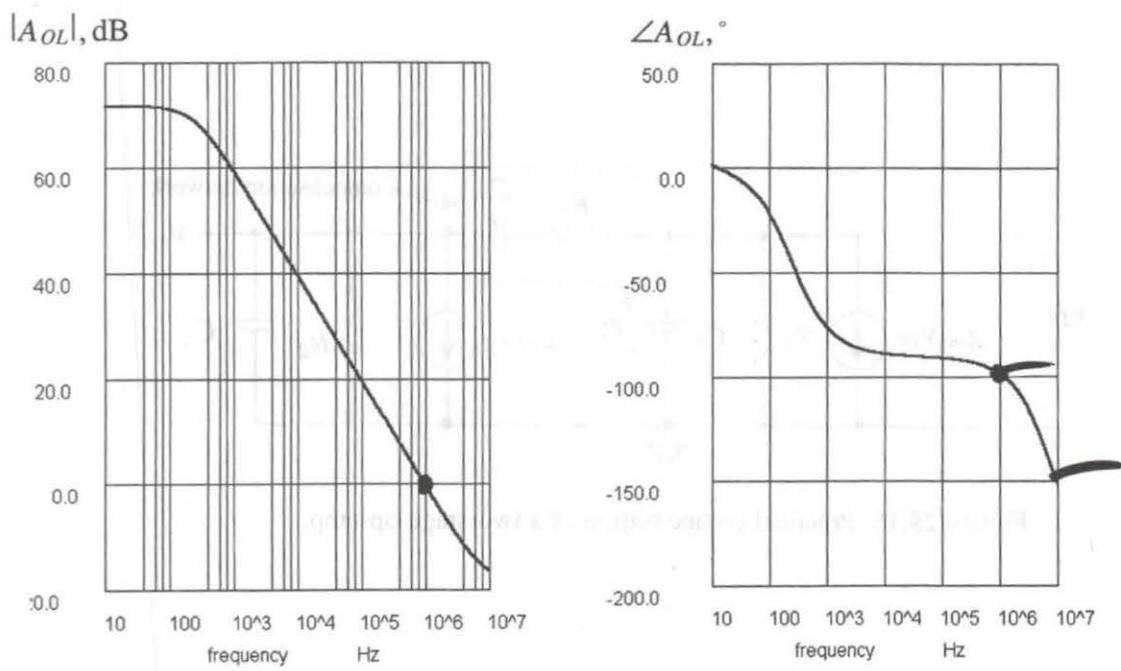


**Figure 25.9** Open-loop compensated op-amp of Fig. 25.3.



**Figure 25.10** Practical compensation of a two-stage op-amp.

Figure 25.13 Open-loop gain and phase response of the amplifier of Fig. 25.10 and zero-pole-pole-zero response of the amplifier of Fig. 25.10.



**Figure 25.12** Open-loop gain and phase response of the amplifier of Fig. 25.11 with zero nulling resistor. Phase margin is approximately 80 .



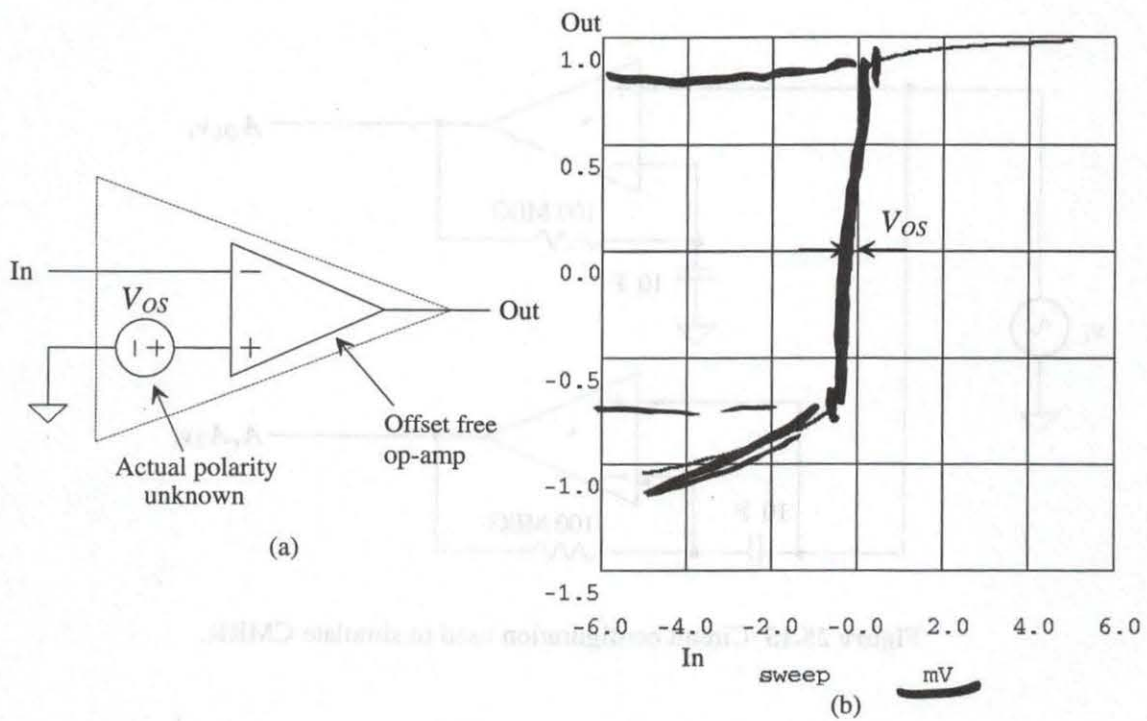
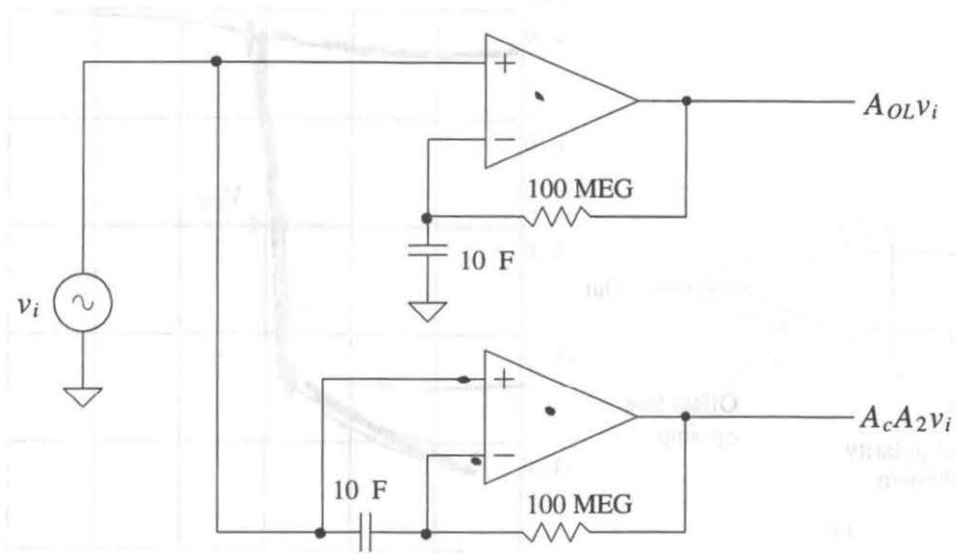
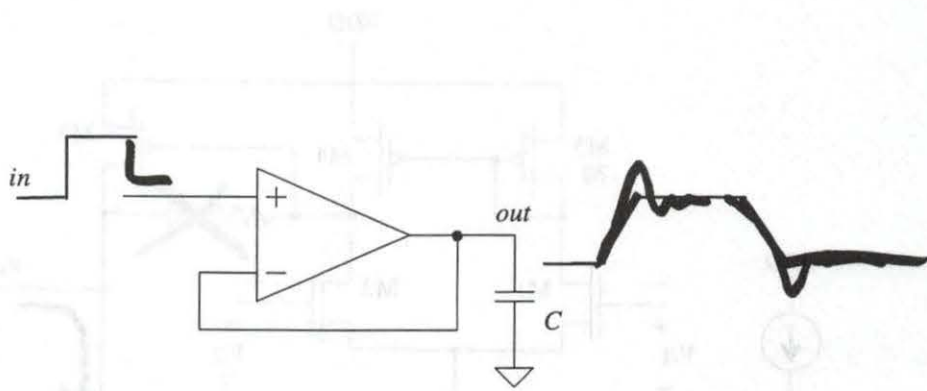


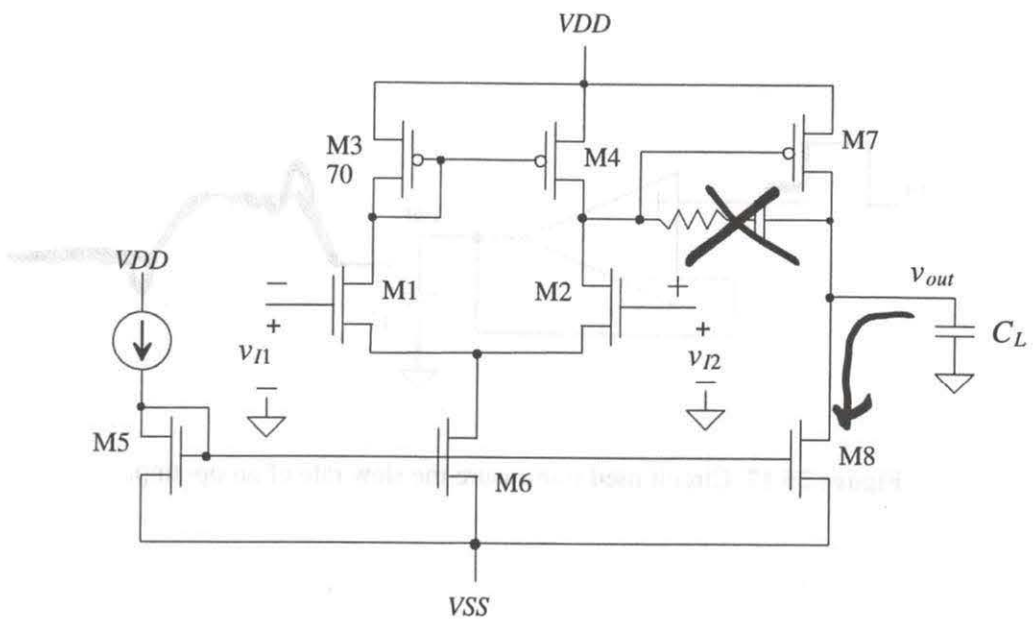
Figure 25.14 Simulation results of op-amp shown in Fig. 25.11 showing systematic offset.



**Figure 25.15** Circuit configuration used to simulate CMRR.



**Figure 25.17** Circuit used to measure the slew rate of an op-amp.



**Figure 25.20** Two-stage op-amp without buffer.

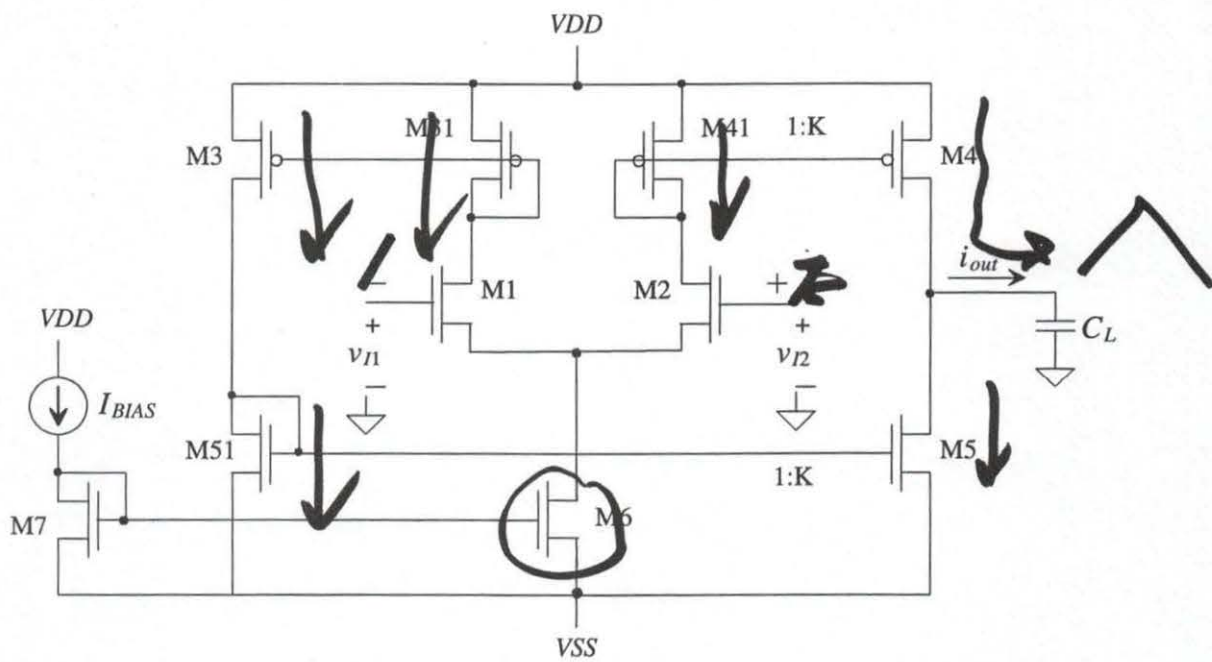


Figure 25.22 Basic configuration of an OTA.

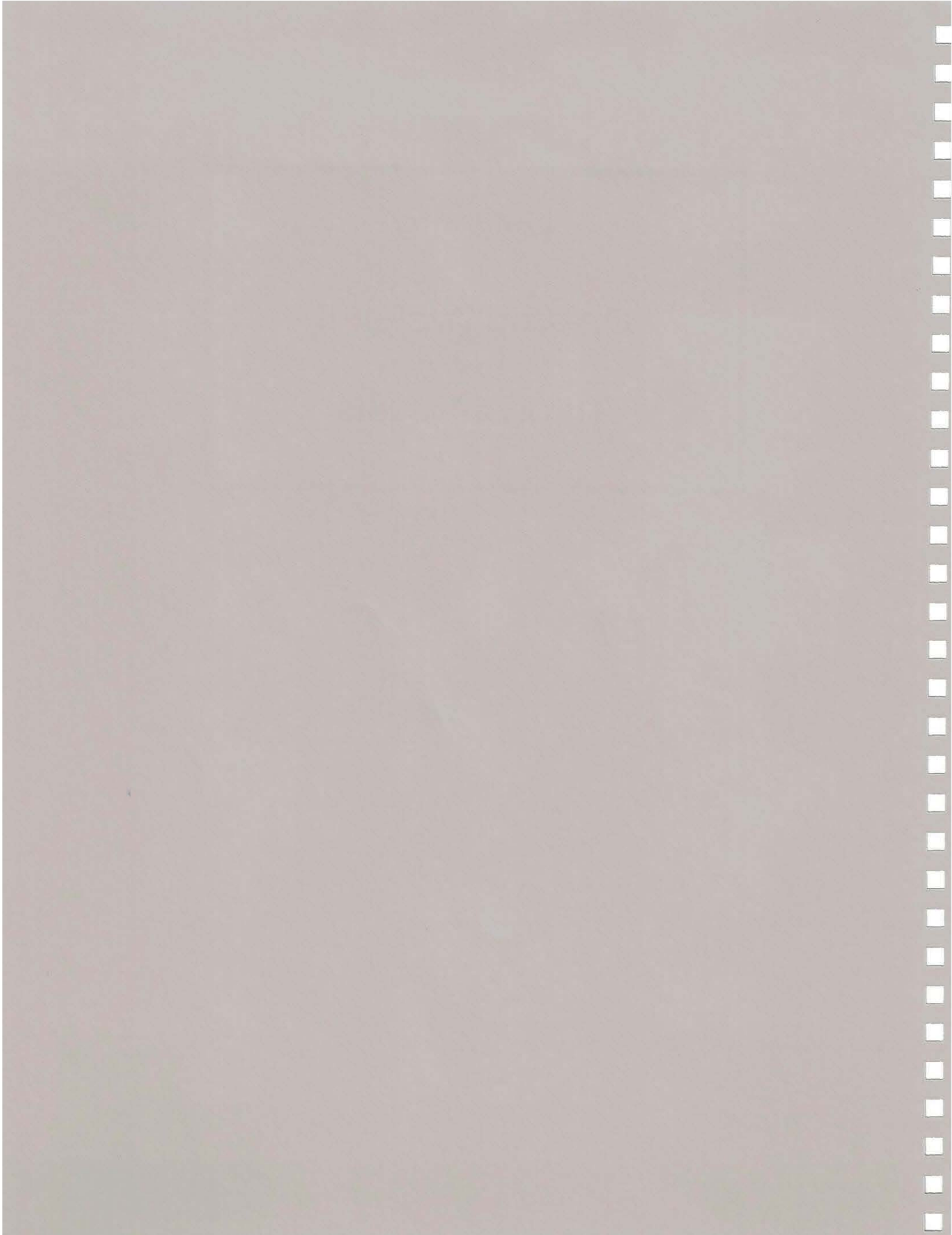


Figure 15.15 A Wheatstone bridge circuit.

Lesson 9

Op-amp Design II

Tutorial Visuals





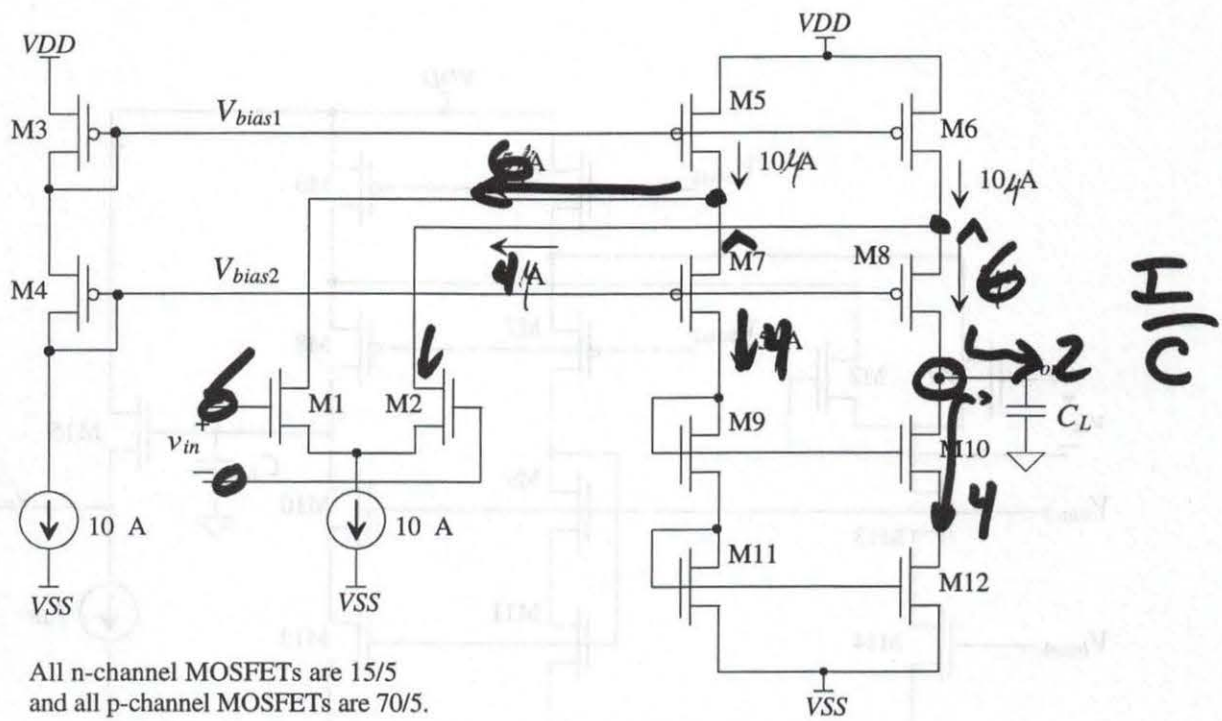
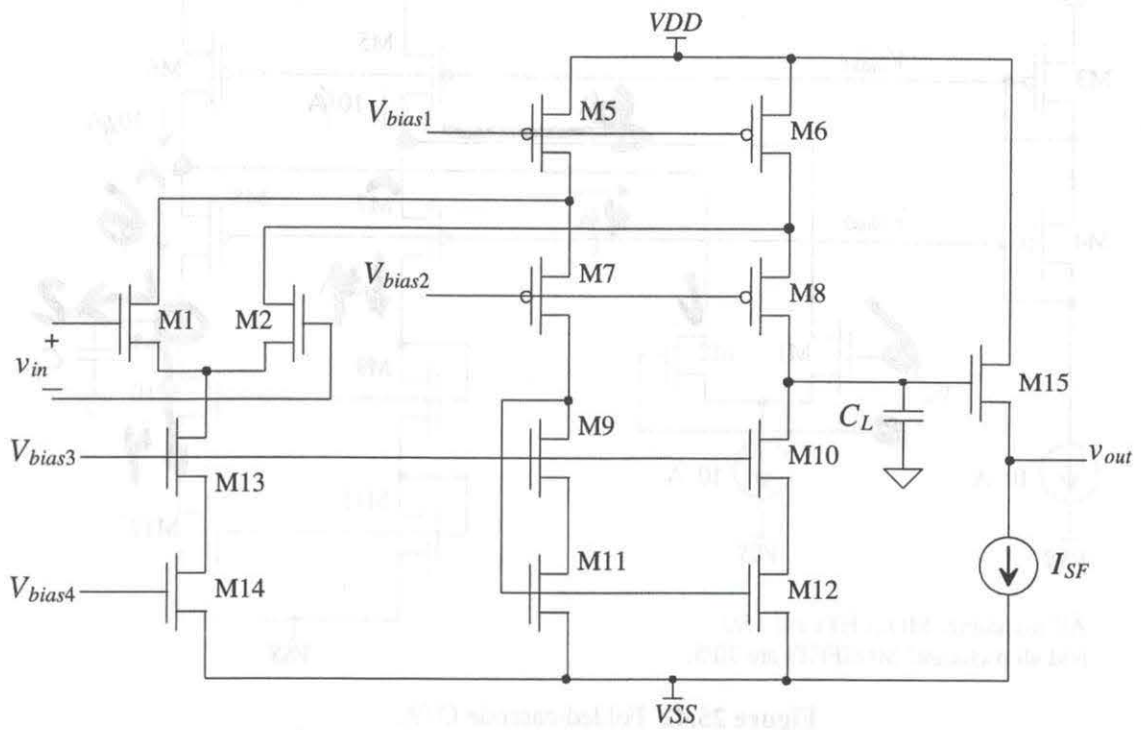


Figure 25.42 Folded-cascode OTA.



**Figure 25.43** Folded-cascode op-amp.

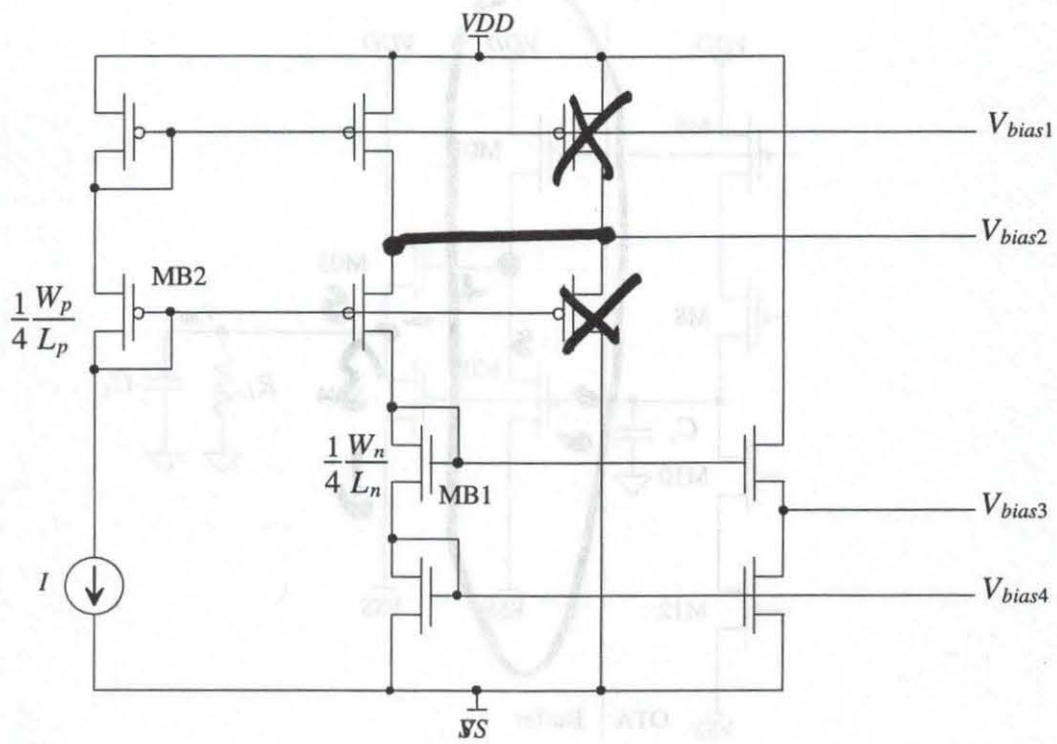
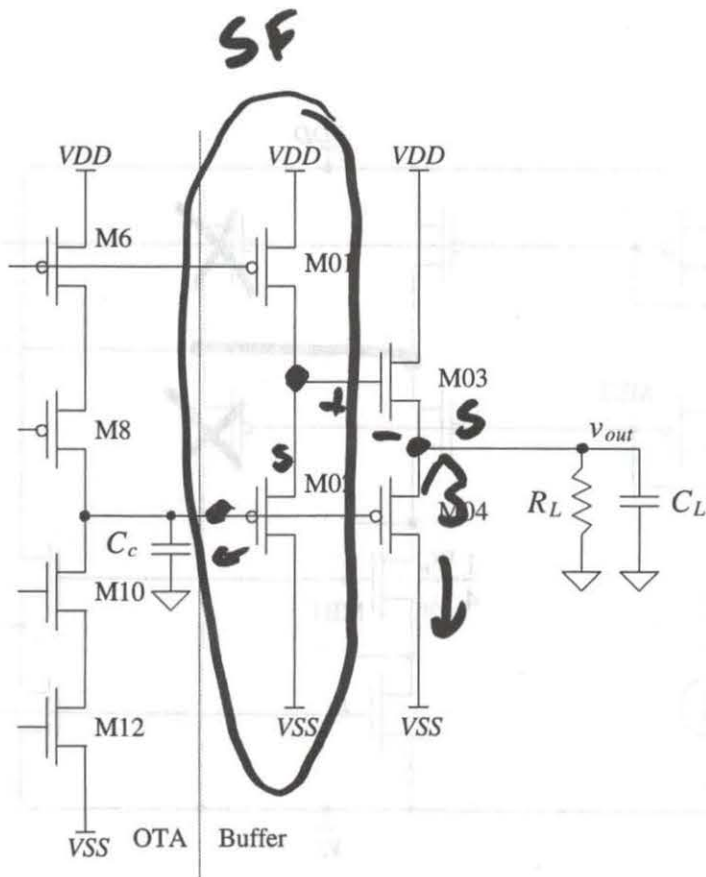


Figure 25.44 Biasing circuit for the op-amp of Fig. 25.43.



**Figure 25.47** Output buffer for use with a folded-cascode OTA (unity gain).



Appl  
Appl

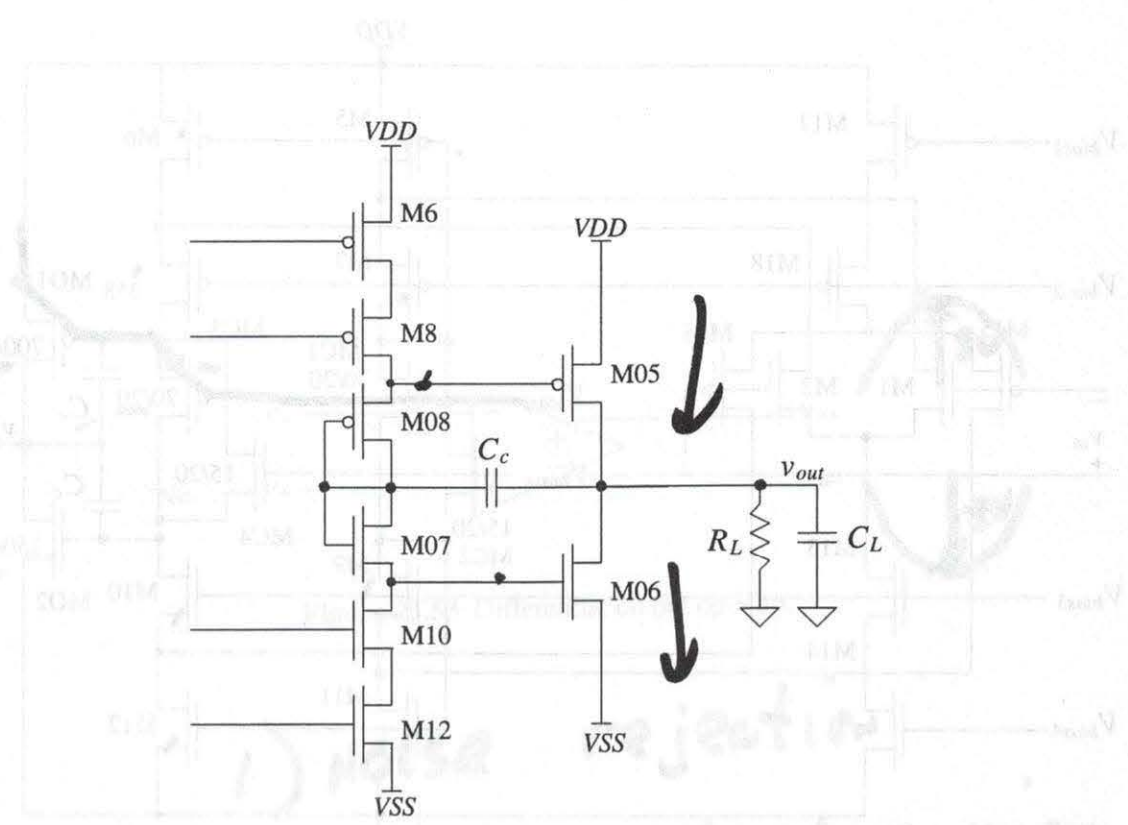
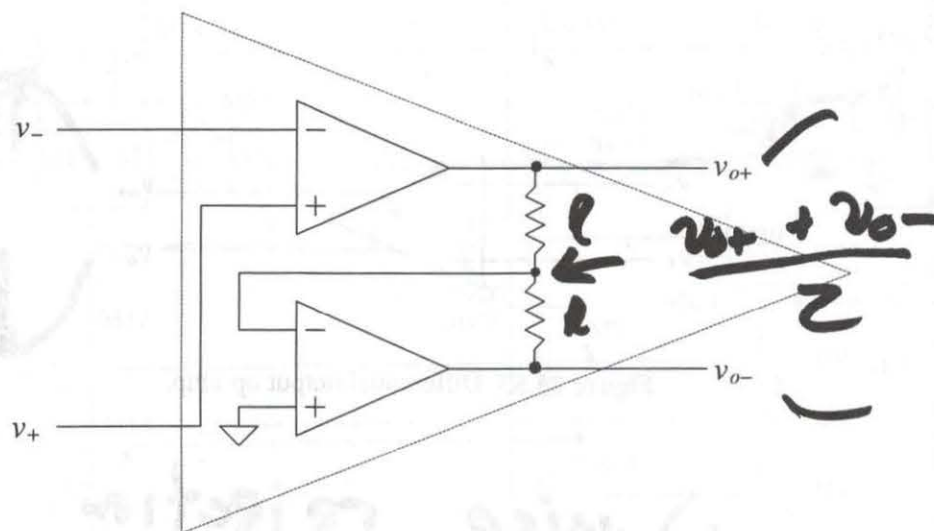


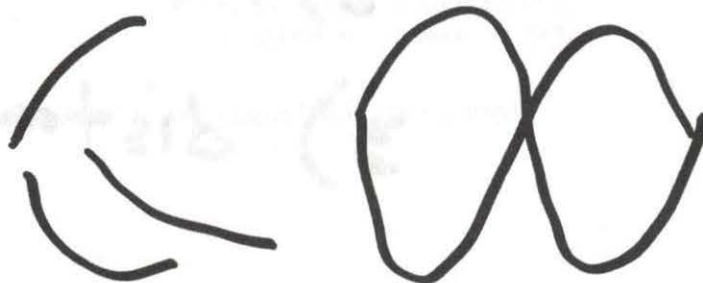
Figure 25.48 Output buffer for use with a folded-cascode OTA (with gain).

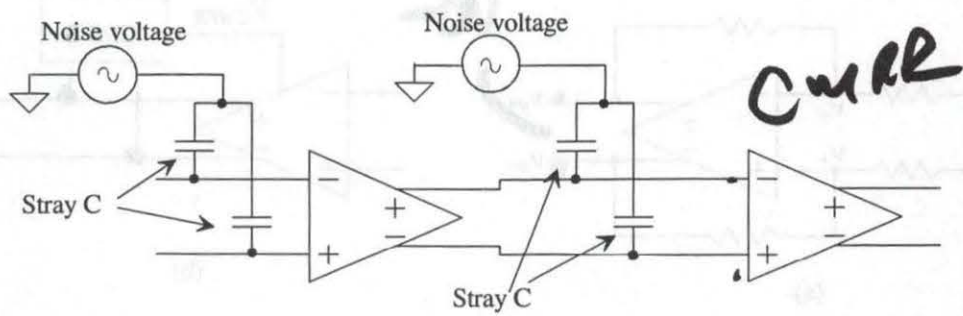
Figure 25.48 shows the output buffer for use with a folded-cascode OTA (with gain). The circuit consists of several MOSFETs: M6 (PMOS) and M8 (PMOS) are connected to VDD. M7 (NMOS) and M10 (NMOS) are connected to VSS. M5 (PMOS) and M06 (NMOS) are connected to VDD and VSS respectively. A compensation capacitor Cc is connected between the gates of M5 and M06. The output node vout is connected to the gates of M5 and M06, and is loaded with a resistor RL and a capacitor CL. Two large black arrows point downwards from the gates of M5 and M06, indicating the signal path.

Figure 25.48 shows the output buffer for use with a folded-cascode OTA (with gain). The circuit consists of several MOSFETs: M6 (PMOS) and M8 (PMOS) are connected to VDD. M7 (NMOS) and M10 (NMOS) are connected to VSS. M5 (PMOS) and M06 (NMOS) are connected to VDD and VSS respectively. A compensation capacitor Cc is connected between the gates of M5 and M06. The output node vout is connected to the gates of M5 and M06, and is loaded with a resistor RL and a capacitor CL. Two large black arrows point downwards from the gates of M5 and M06, indicating the signal path.

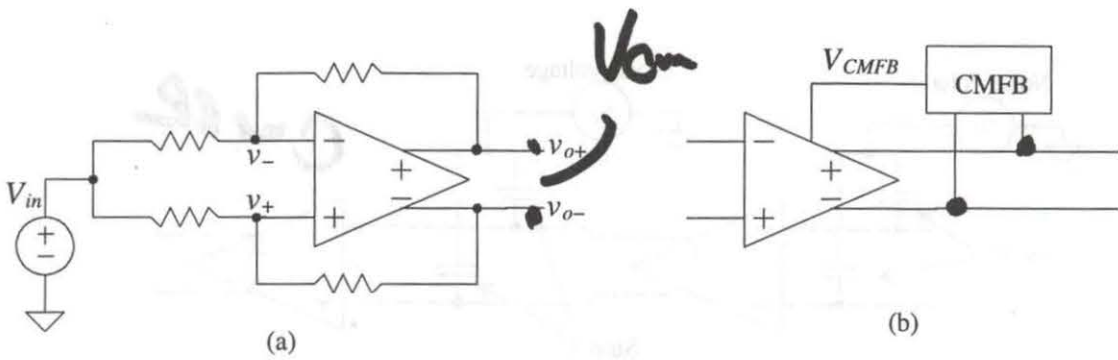


**Figure 25.54** Formation of a differential output op-amp using two single-ended op-amps.



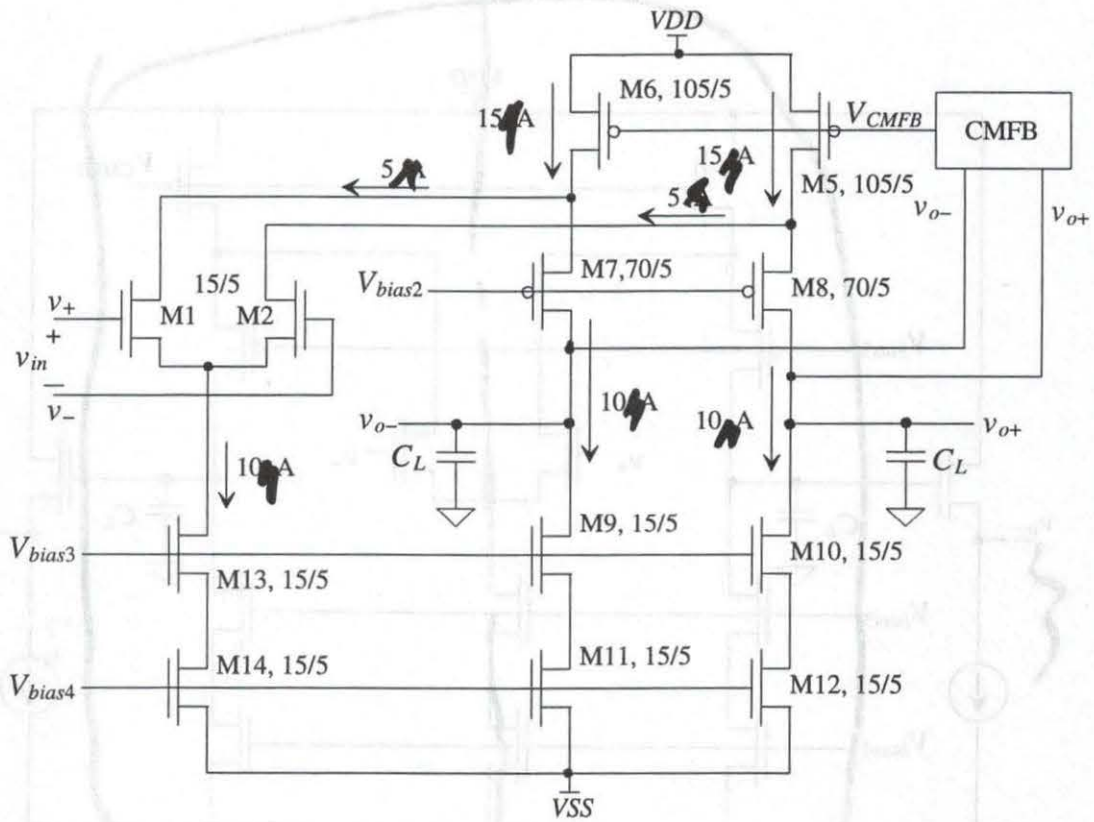


**Figure 25.55** Differential output op-amps showing parasitic capacitance and noise.



**Figure 25.56** (a) Simple gain configuration using differential output op-amp and (b) the use of a common mode feedback circuit to adjust the common-mode output voltage.





**Figure 25.57** Fully differential folded-cascode OTA.

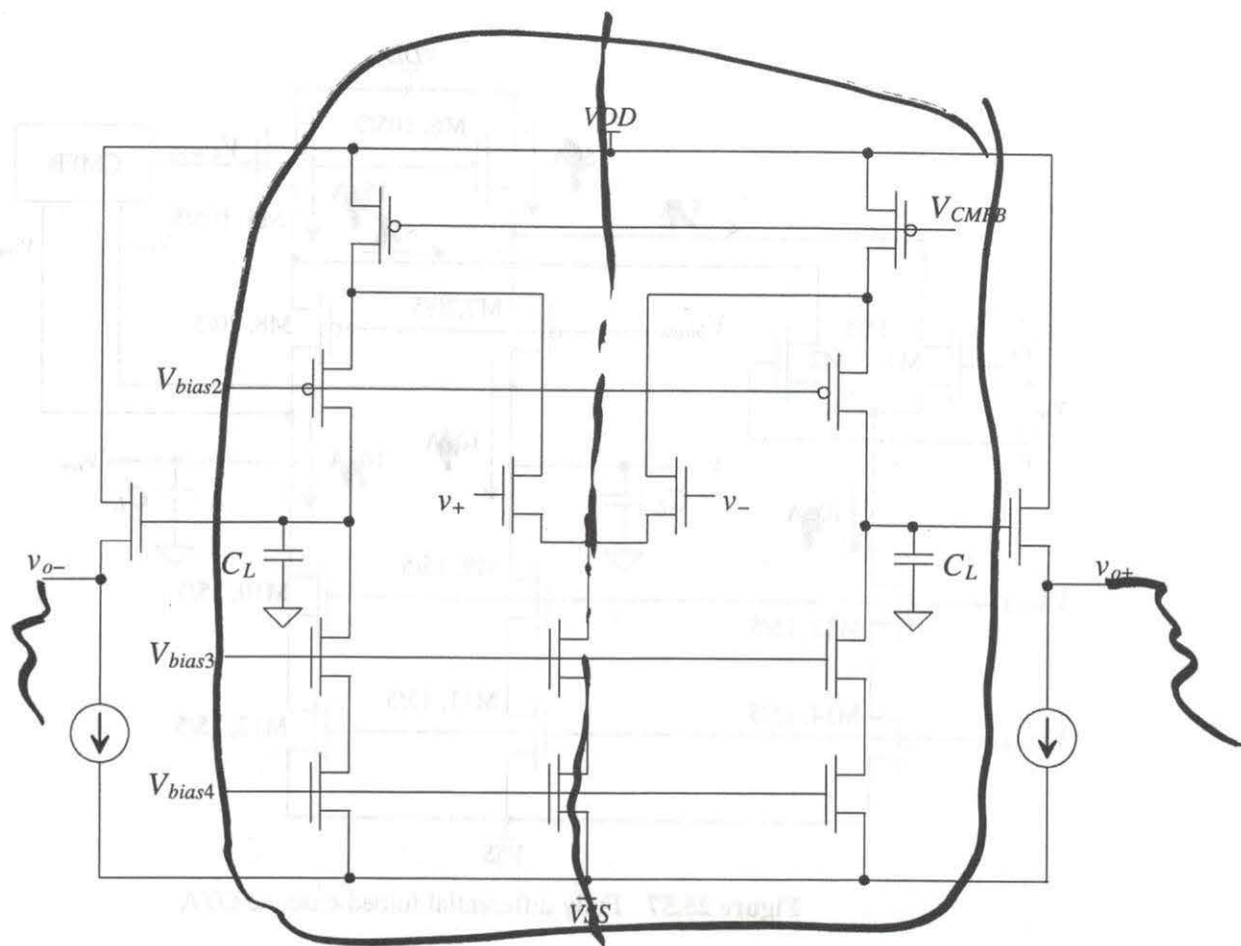


Figure 25.63 Fully differential folded-cascode op-amp.

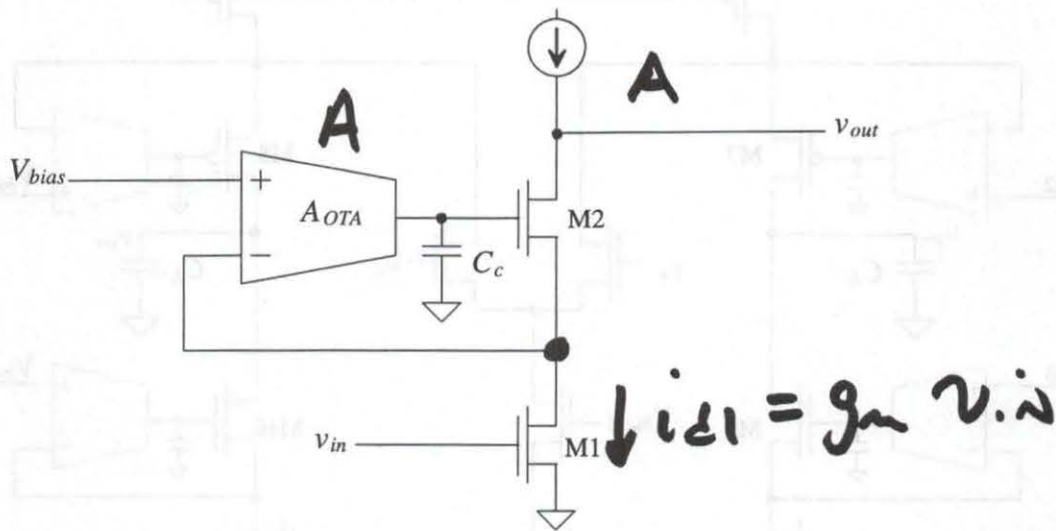


Figure 25.68 Use of gain enhancement to increase cascode open-circuit gain.

Normally,  $R_o = g_m r_o^2$

with Gain-Enhanc.  $R_o = g_m r_o^2 \cdot A$

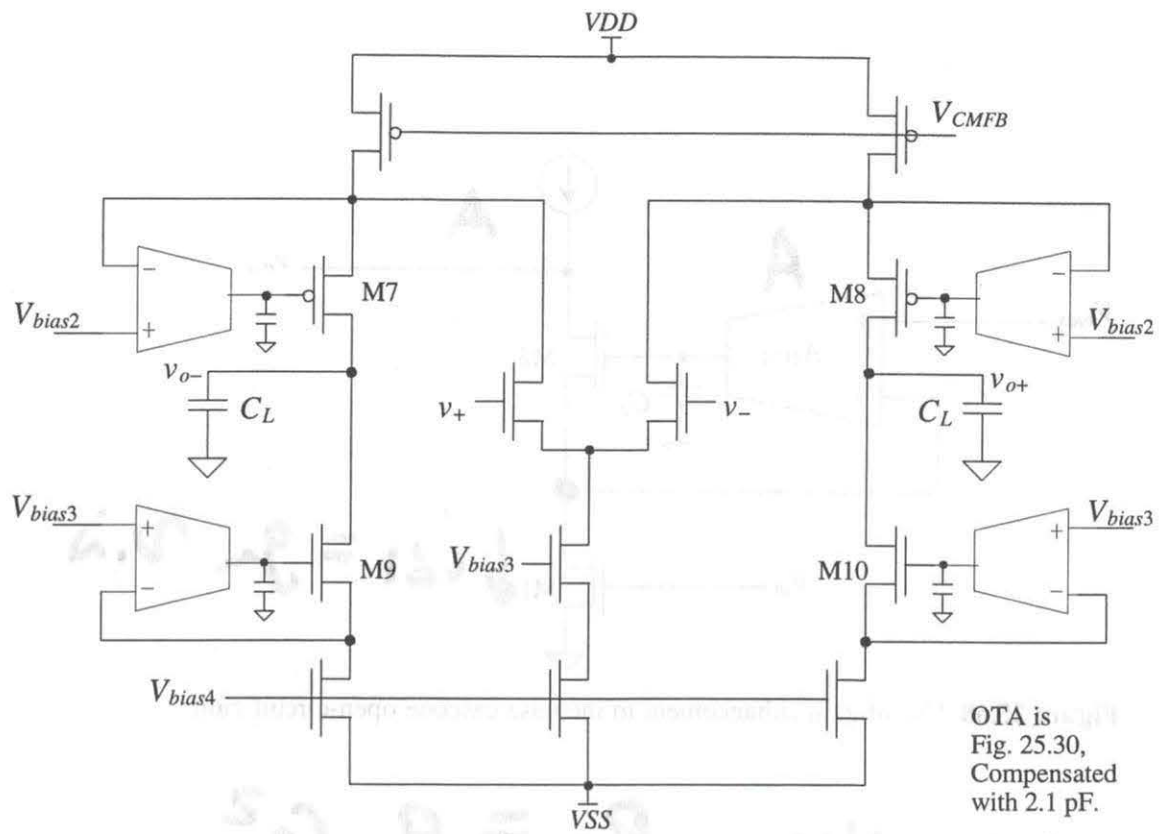
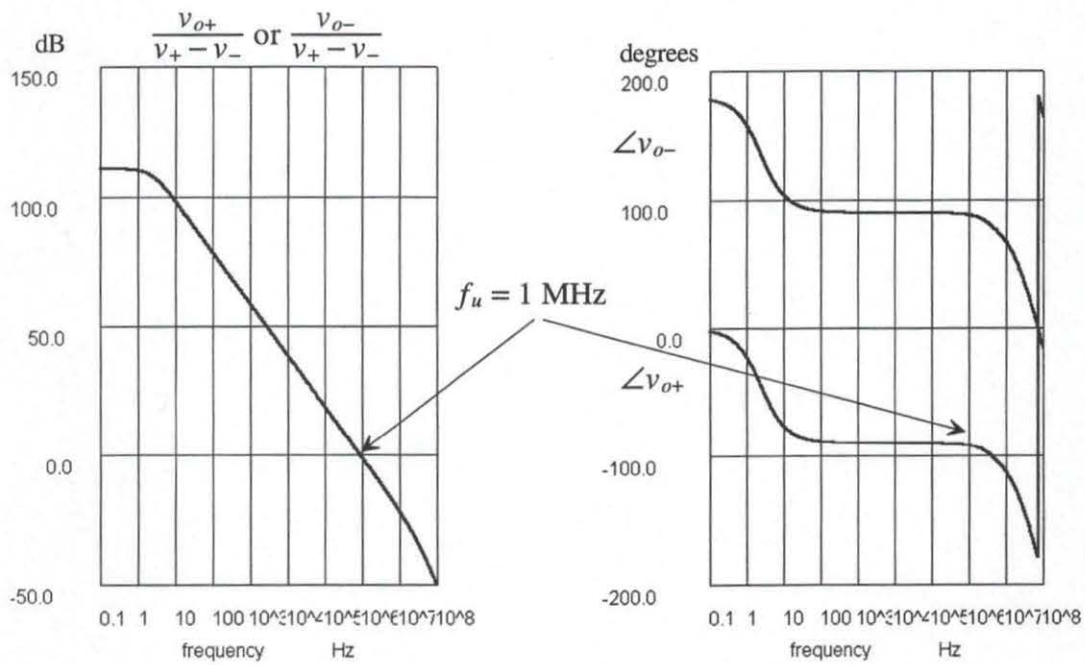


Figure 25.69 Fully differential folded-cascode OTA with gain enhancement.



**Figure 25.70** Simulation results for the op-amp of Fig. 25.69.

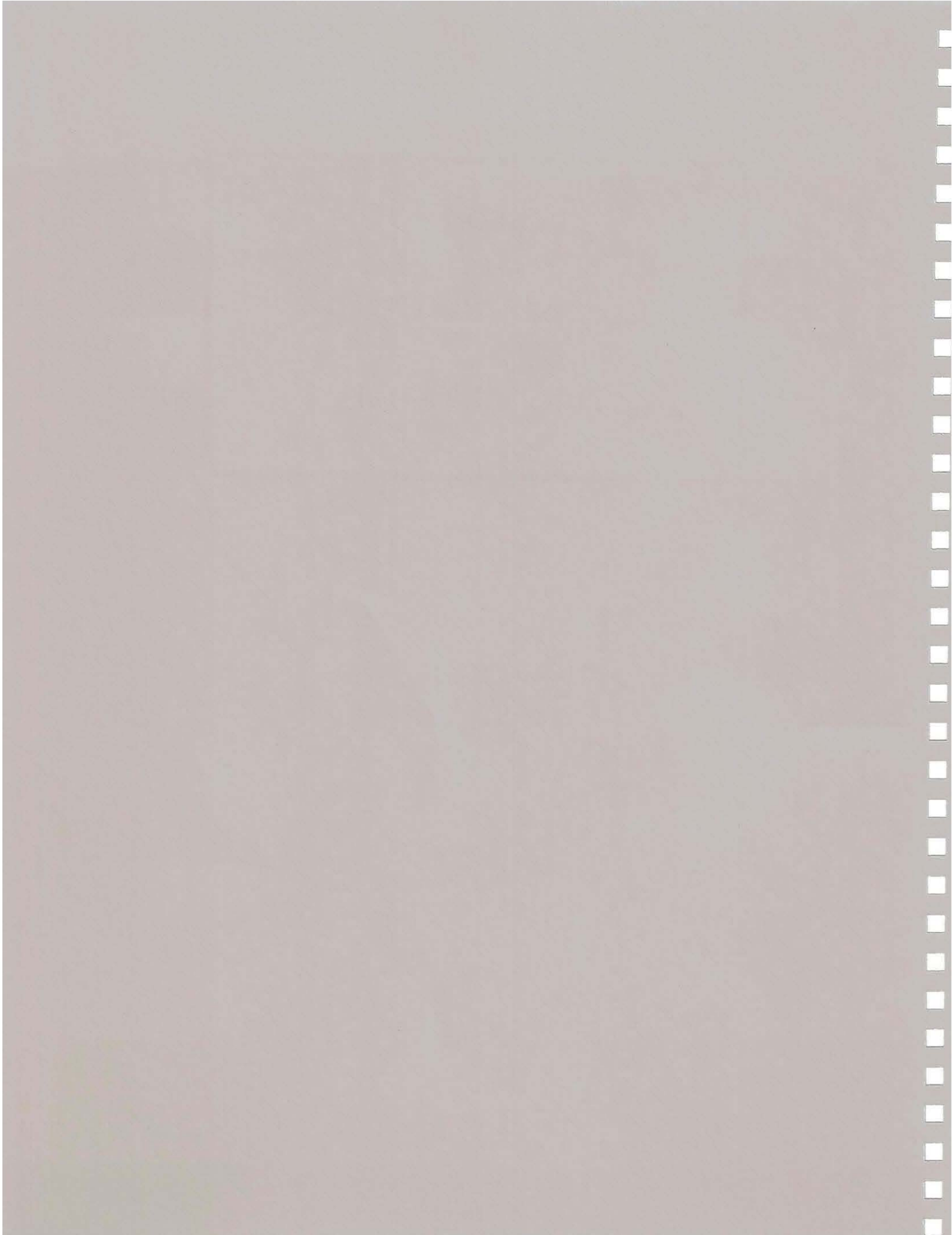


Figure 28.70: A graph showing the relationship between the rate of change of the function and the function itself.

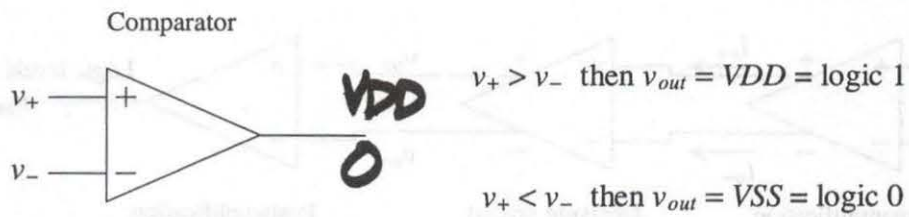
Lesson 10

Comparator Design

Tutorial Visuals

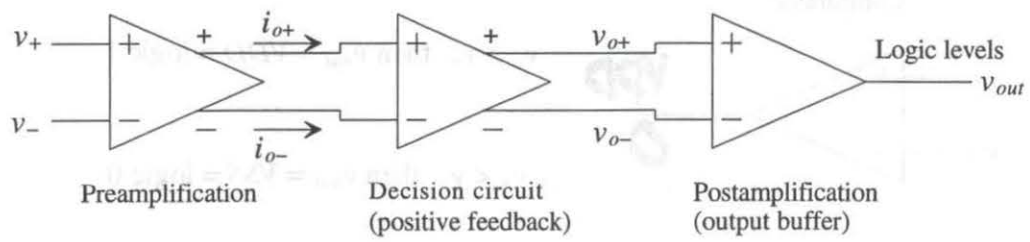




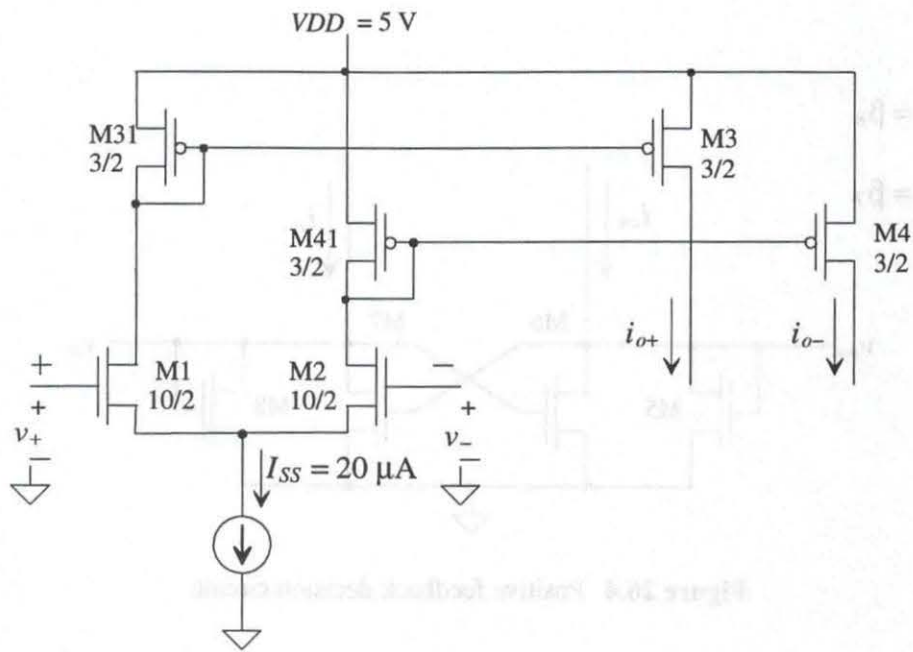


$v_+ - v_-$

Figure 26.1 Comparator operation.



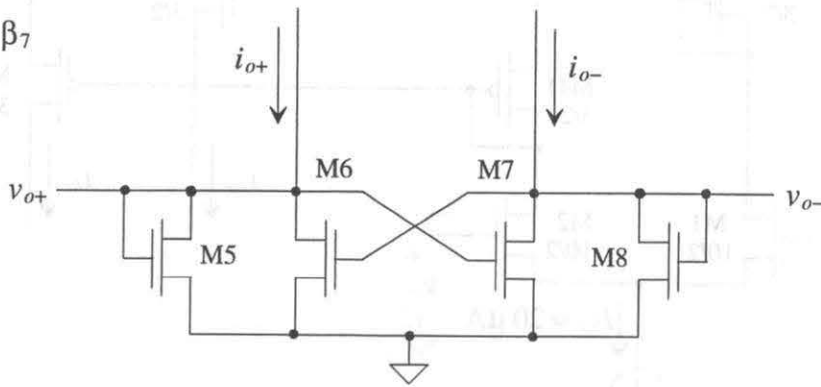
**Figure 26.2** Block diagram of a voltage comparator.



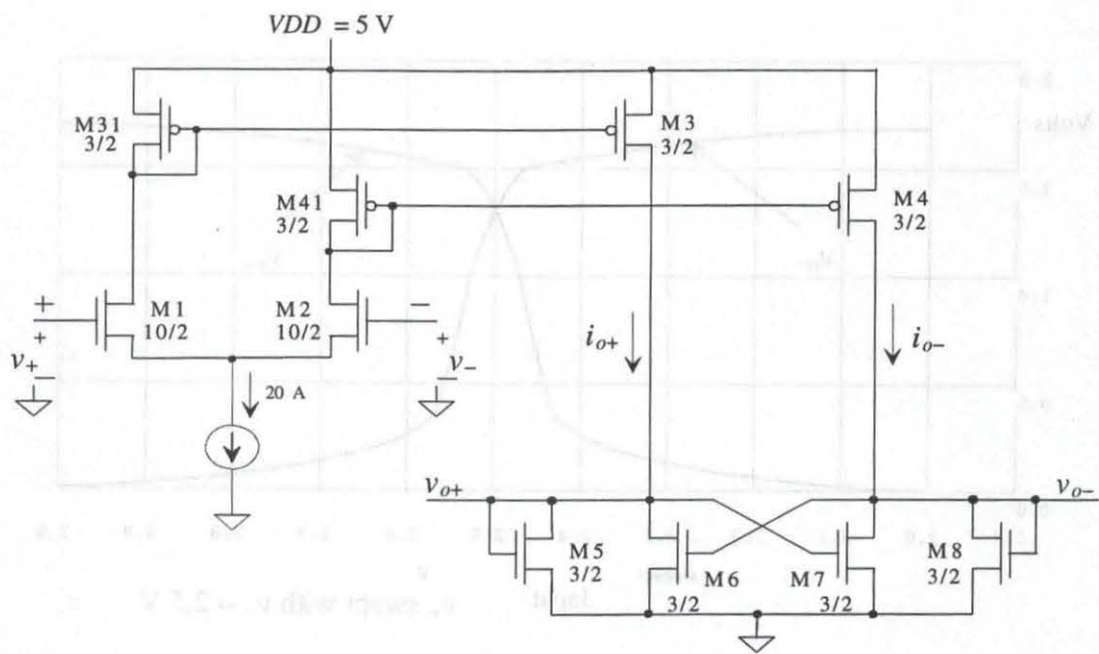
**Figure 26.3** Preamplification stage of comparator.

$$\beta_A = \beta_5 = \beta_8$$

$$\beta_B = \beta_6 = \beta_7$$



**Figure 26.4** Positive feedback decision circuit.



**Figure 26.5** Schematic of preamp and decision circuit.

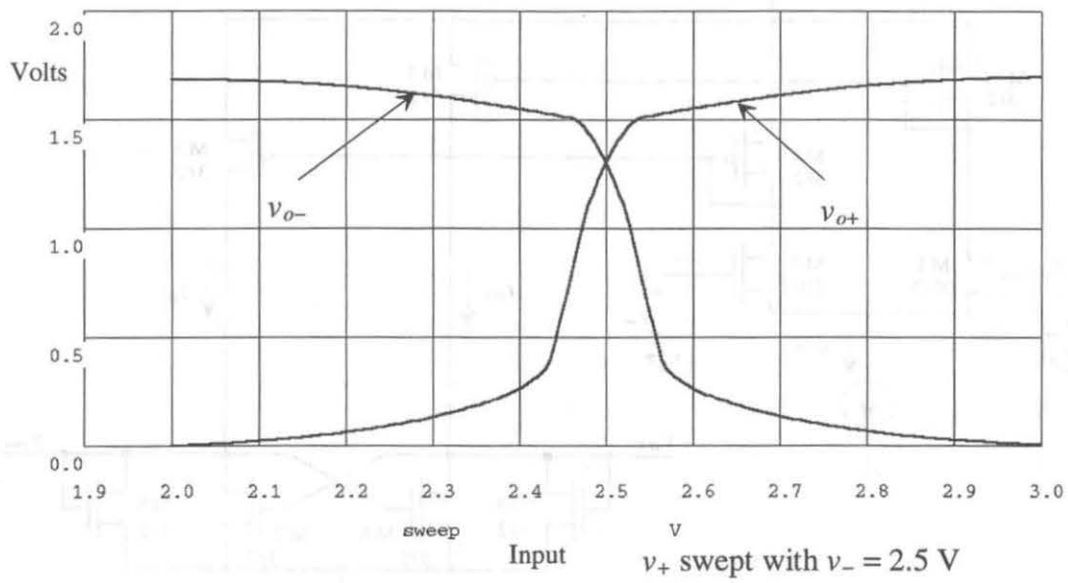
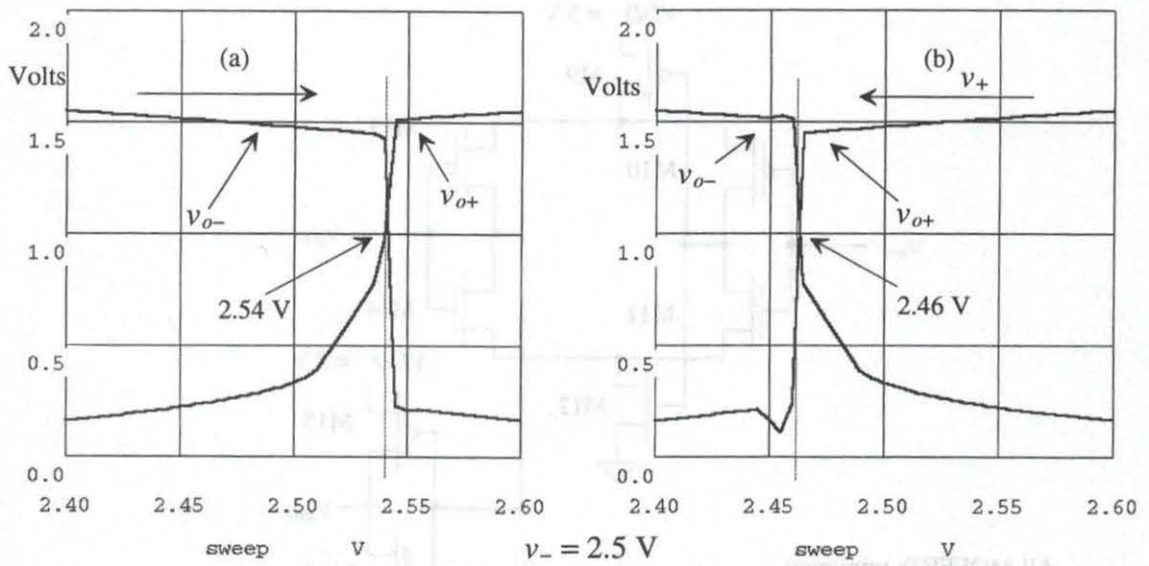
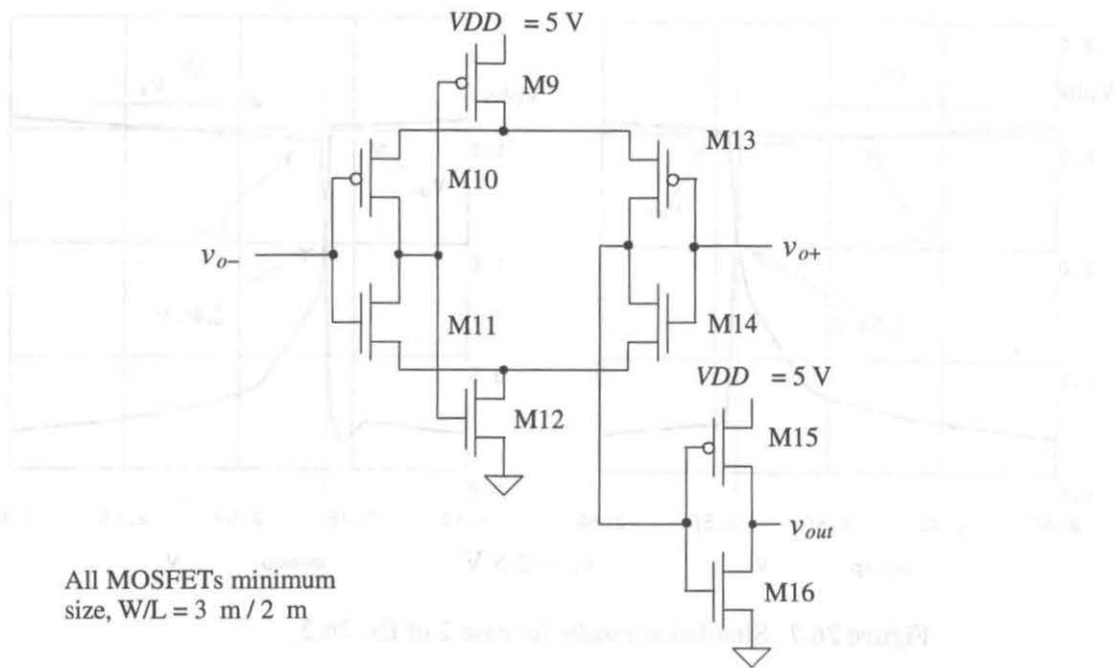


Figure 26.6 Simulation results for case 1 of Ex. 26.1.

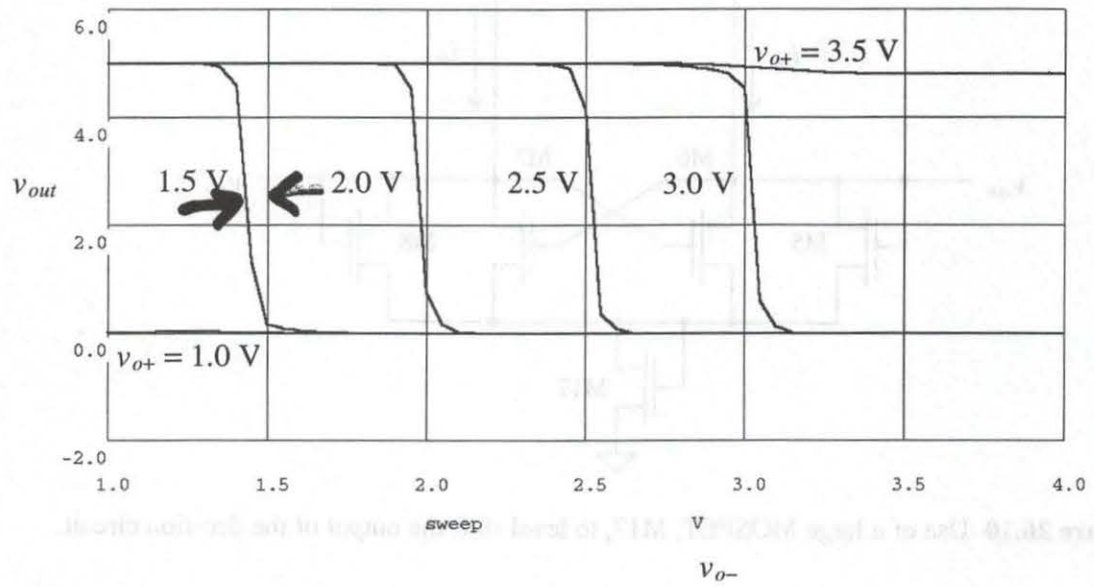


**Figure 26.7** Simulation results for case 2 of Ex. 26.2.

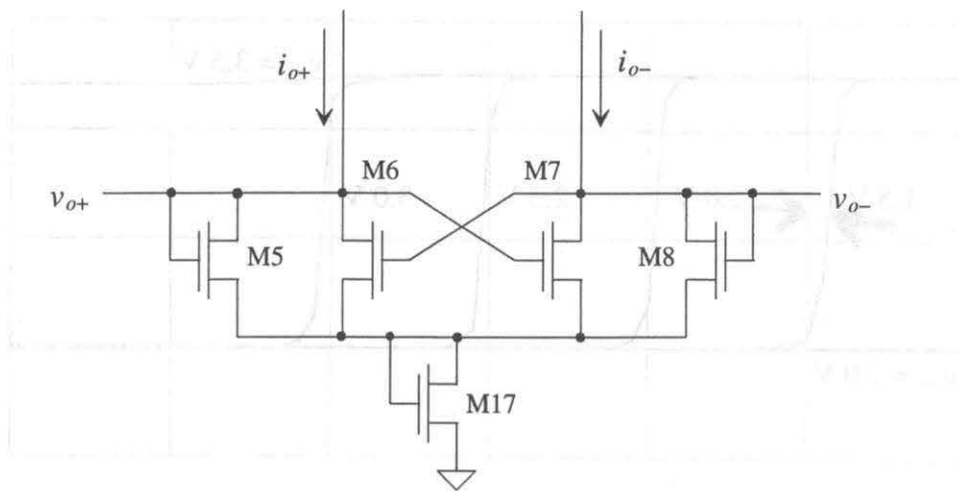


**Figure 26.8** A self-biasing differential amplifier used as the comparator output buffer.





**Figure 26.9** DC sweep of the self-biasing amplifier of Fig. 26.8.



**Figure 26.10** Use of a large MOSFET, M17, to level shift the output of the decision circuit.

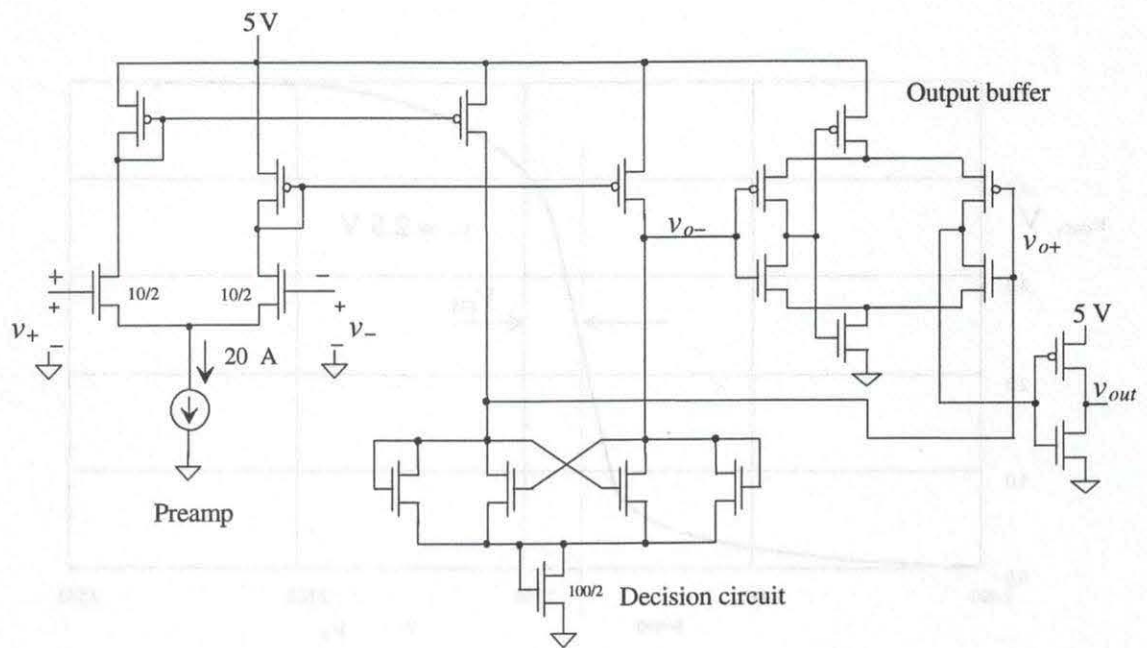
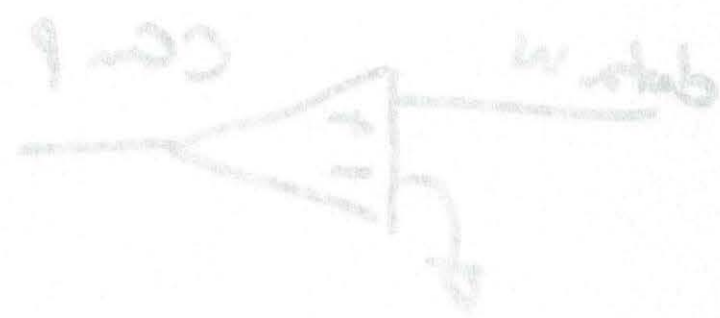


Figure 26.11 Complete schematic of comparator.



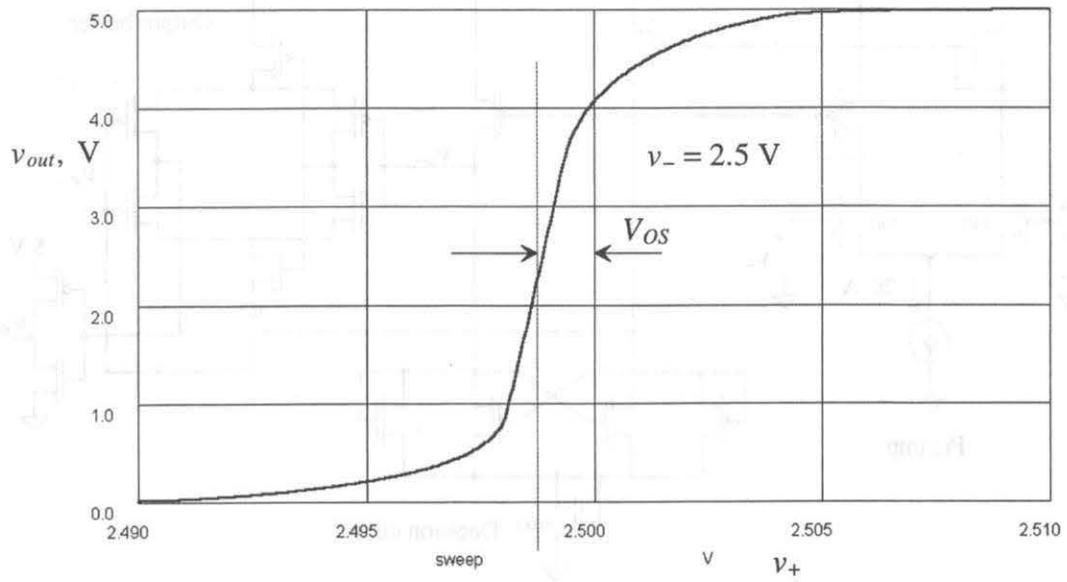
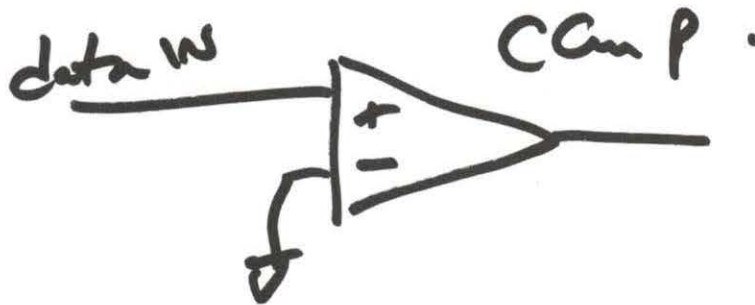


Figure 26.12 DC characteristics of the comparator of Fig. 26.11 with  $-$ input connected to 2.5 V.



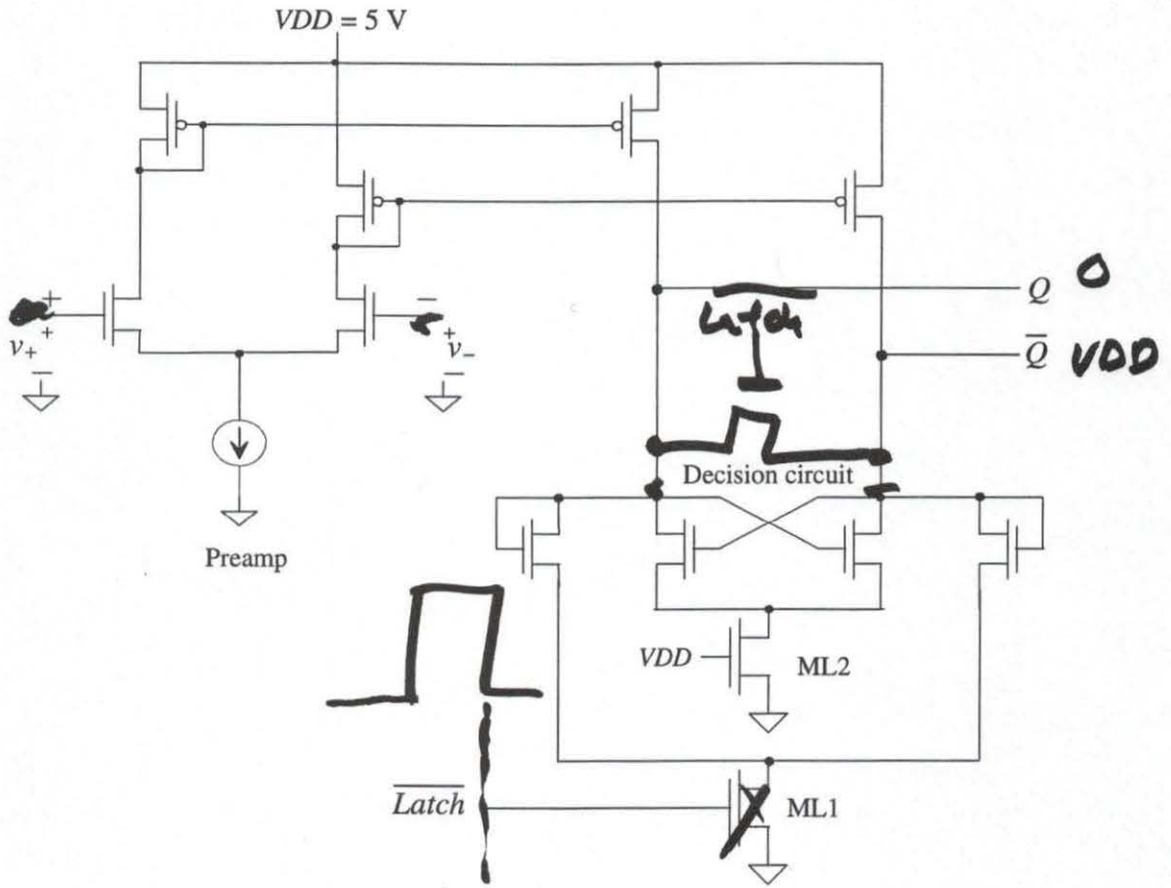


Figure 26.17 Clocked comparator.



Figure 6.11: Class-D audio amplifier

