CMOS
Analog Circuit Design

Developed by
R. Jacob Baker
University of Idaho

IEEE
Networking the World™

An IEEE/EAB
Self-Study Course

Prepared for the Educational
Activities Board of the
Institute of Electrical and

Study Guide & Final Examination

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CONTENTS

CMOS Analog Circuit Design

A Self-Study Course

This course was designed around Chapters 9, 20, 21, 22, 24, 25, and 26 of *CMOS: Circuit Design, Layout, and Simulation*, by Baker, Li and Boyce, IEEE Press, 1998. The goal of this self-study course is to provide tutorial information on custom CMOS (Complimentary Metal Oxide Semiconductor) analog circuit design with an emphasis on the practical implementation of analog CMOS integrated circuits (ICs).

Prerequisites

This course assumes the student has an electrical engineering background with fundamental knowledge in the areas of MOSFET operation, linear circuits, and engineering electronics. No knowledge of integrated circuit design is assumed beyond the junior engineering electronics sequence in a typical electrical engineering curriculum.

Goals

After finishing this course the student should be able to:

- understand biasing in analog CMOS integrated circuits (ICs).
- discuss basic layout concerns for high-performance analog ICs.
- design voltage and current references.
- understand the operation and use of CMOS differential amplifiers.
- design basic CMOS op-amps.
- understand compensation and gain enhancement in CMOS op-amps.
- design clocked and non-clocked high-speed CMOS comparators.

Features of this course

This course includes:

- a study guide including learning objectives, reading assignments, and practice problems.
- a CD-ROM providing solutions to the practice problems in Adobe Portable Document Format (PDF) files.
- a final exam which, upon completion, will lead to a certificate of achievement from the IEEE and 8 continuing education units (CEUs).
- a video tutorial for each lesson to help reinforce the concepts presented in the book and study guide.
- the course textbook.

How to use this course

This course was developed assuming the reader would complete the lessons sequentially, that is, Lesson 1 followed by Lesson 2, etc. Similarly the lessons should be completed sequentially in the following order:

1. read the objectives of the lesson, designated by the  icon.
2. read the assigned sections of the text, designated by the  icon.
3. watch the video taped tutorial corresponding to the lesson number, designated by the  icon.
4. review the key points of the chapter, designated by the  icon.
5. solve the practice problems, designated by the  icon.
6. review the solutions to the practice problems, designated by the  icon.
7. review the objectives of the lesson and determine if they have been met. If so proceed to the next lesson. If not review 2 through 5 above until the objectives are met.

After finishing lesson 10 review the final exam instructions given in the final exam booklet. Information on taking and submitting the exam for grading/credit is given in this booklet.

Acknowledgments

I would like to take this opportunity to thank Jill Bagley and Barbara Stoler of the Educational Activities Department of the IEEE for their time, effort and encouragement in developing this course. Also, special thanks go to my wife Julie and children Kyri and Josh for their patience and encouragement while this course was being developed.

Lesson 1 - CMOS Analog modeling

Learning Objectives

After completing this lesson you will be able to:

- Demonstrate an understanding of the course and its goals.
- Lay out an n-channel MOSFET (NMOS) and a p-channel (PMOS).
- Discuss large-signal operation of MOSFETs.
- Explain small-signal models and their uses in circuit design.
- Recognize the CN20 process used throughout the book and this self-study course.

Reading Assignment

Read Chapter 9 and Appendix A of the book.

Video Assignment

Watch the Lesson 1 tutorial on the video tape. These short tutorials are an important part of the course. Many of the final exam questions are based on the material presented in these tutorials.

Key Points

- Small-signal models are used to represent the operation of a MOSFET.

- By adjusting the width and length of a MOSFET we can change the electrical characteristics of the device.
- The output resistance of a MOSFET is an important design parameter in analog design.

Practice Problems

Do problems 9.1, 9.4, 9.8, 9.11, and 9.13

Answers to Practice Problems

The answers to the practice problems are given on the accompanying CD-ROM. To use this CD you must have Adobe Acrobat Reader (version 3.0 or later) installed on your computer. This reader is available on the CD-ROM itself in the */data/acroread/* directory or on the Internet at:

http://www.adobe.com/prodindex/acrobat/readstep.html

Lesson 2 - Current sources and sinks I

Learning Objectives

After completing this lesson you will be able to:

- Analyze the simple current mirror's operation.
- Size the width and length of the MOSFET's used in a basic current mirror.
- Discuss the cascode connection.
- Determine the output resistance of various current mirror configurations.

Reading Assignment

Read Section 20.1 of the textbook.

Video Assignment

Watch the Lesson 2 tutorial on the video tape. Again, these videos are an important portion of the course and will cover material that will be on the final exam.

Key Points

- The current mirror is a basic building block in analog integrated circuit design.

- Generally, the gate to source voltage of a MOSFET is biased to a few hundred mV above the MOSFETs threshold voltage.
- When the same current is forced through two identically sized MOSFETs with the same gate to source voltage the MOSFETs drain to source voltages are identical. This property is used for biasing other MOSFETs in more complicated CMOS analog circuits.
- The cascode connection of MOSFETs is used to increase the output resistance of a current mirror at the cost of reduced output swing (the minimum voltage require across the current mirror increases.)

Practice Problems

Do problems 20.1, 20.2, 20.3, 20.5, 20.6, and 20.7.

Answers to Practice Problems

See the accompanying CD-ROM for practice problem solutions.

Lesson 3 - Current sources and sinks II

Learning Objectives

After completing this lesson you will be able to:

- Perform matching in current mirrors.
- Determine temperature behavior in current mirrors.
- Recognize transient properties of current mirrors.
- Demonstrate an understanding of wide-swing, low-voltage current mirrors.

Reading Assignment

Review Section 20.1 and read Section 20.2.

Video Assignment

Watch the Lesson 3 tutorial on the video tape.

Key Points

- Matching is an important concern when designing a current mirror.

- Designing a current mirror with a small gate-source voltage results in a large current mismatch due to variations in the threshold voltage.
- Using vastly different size current mirrors can result in transient response problems.
- Oxide encroachment effects can be avoided by laying larger MOSFETs out as parallel connection of smaller, or unit size, MOSFETs.
- Temperature effects can cause matching problems in current mirrors. To avoid large fluctuations in the currents, over a given operating temperature range, current references (circuits designed to provide currents that are independent of temperature) can be used. These are discussed in the next section.

Practice Problems

Do problems 20.8 (without SPICE), 20.14, 20.20, 20.21

Answers to Practice Problems

See the accompanying CD-ROM for practice problem solutions.

Lesson 4 - References I

Learning Objectives

After completing this lesson you will be able to:

- Discuss the types and merits of various voltage dividers available in a CMOS process.
- Understand why self-biasing is needed in current and voltage references.
- Recognize the temperature behavior of a self-biased reference.
- Determine why a start-up circuit is needed and how to design a start-up circuit.

Reading Assignment

Read Sections 21.1 and 21.2.

Video Assignment

Watch the lesson 4 tutorial.

Key Points

- A resistive voltage divider provides division that is process insensitive at the cost of large area for low-power.
- MOSFET voltage dividers can be for current sink biasing and lower power dissipation.

- Self-biasing reduces a current references sensitivity to power supply variations.
- A start-up circuit is required to make sure a self-biased reference is operating in the active region (make sure the reference isn't off.)

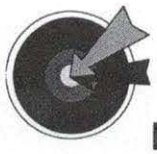
Practice Problems

Do problems 21.1, 21.3, 21.6, and 21.7

Answers to Practice Problems

See the accompanying CD-ROM for practice problem solutions.

Lesson 5 - References II



Learning Objectives

After completing this lesson you will be able to:

- Discuss the operation of a bandgap reference.
- Determine the operation of a beta-multiplier reference.
- Recognize the benefits of the bandgap beta-multiplier references.

Reading Assignment

Read Sections 21.3 and 21.4.

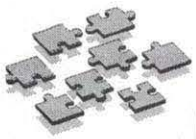
Video Assignment

Watch the Lesson 5 tutorial.

Key Points

- Bandgap references combine the positive temperature coefficient of the thermal voltage with the negative temperature coefficient of the diode forward voltage.

- The Beta-multiplier combines the positive temperature coefficient of a resistor with the decrease in threshold voltage with increasing temperature or the increase in drain current with temperature (dependent on the point of operation, see Fig. 9.11) to provide a reference with a settable temperature coefficient.
- The Beta-multiplier can also be used for biasing current mirrors in the subthreshold region.



Practice Problems

Do problems 21.13, 21.15, 21.16, and 21.18

Answers to Practice Problems

See the accompanying CD-ROM for practice problem solutions.

Lesson 6 - Amplifiers

Learning Objectives

After completing this lesson you will be able to:

- Illustrate the basic configurations for CMOS amplifiers.
- Determine the differences between gate-drain connected loads and current source/sink loads.
- Explain how biasing current affects the gain of a CMOS amplifier.
- Understand why the cascode configuration is used to increase the gain of a CMOS amplifier.
- Discuss class AB output buffer stages and their use.

Reading Assignment

Read Chapter 22.

Video Assignment

Watch the Lesson 6 tutorial.

Key Points

- we can think of a gate-drain connected MOSFET as a resistor with a value of $1/g_m$. The resistance looking into the source of a MOSFET is also $1/g_m$. If we do this we can intuitively analyze the gain of MOSFET amplifiers.
- current source loads provide large gain at the cost of bandwidth while gate-drain connected loads provide speed at the cost of gain.
- amplifiers using current source/sink loads are limited to sourcing or sinking a current limited by the load.
- class AB amplifier stages are used to reduce the power dissipated in the amplifier when a large load (small resistance or large capacitance) is driven.

Practice Problems

Do problems 22.1, 22.5, 22.6, 22.7, 22.10, 22.14, and 22.15

Answers to Practice Problems

See the accompanying CD-ROM for practice problem solutions.

Lesson 7 - Differential amplifiers

Learning Objectives

After completing this lesson you will be able to:

- Discuss the operation of a differential amplifier (diff-amp).
- Expain why a diff-amps are used.
- Determine matching considerations in diff-amps.
- Demonstrate an understanding of class AB diff-amps.
- Analyze the operation of wide-swing diff-amps.

Reading Assignment

Read Chapter 24.

Video Assignment

Watch the Lesson 7 tutorial.

Key Points

- The diff-amp is a fundamental building block in CMOS analog circuit design.

- The diff-amp, ideally, amplifies the difference in its inputs while rejecting any common signal on its inputs. The ability of a diff-amp to amplify differences in the input signal while rejecting common signals is measured using the common mode rejection ratio (CMRR).
- The source coupled diff-amp can source and sink a current limited by the source bias current. To avoid these current sourcing/sinking limitations the source cross-coupled pair can be used since it can be operated as a class AB amplifier.
- Wide swing diff-amps can be used to amplify signals that extend from the positive power supply (VDD) to the negative power supply (VSS).

Practice Problems

Do problems 24.2, 24.7, 24.10, 24.14, and 24.15.

Answers to Practice Problems

See the accompanying CD-ROM for practice problem solutions.

Lesson 8 - Op-amp design I

Learning Objectives

After completing this lesson you will be able to:

- Determine the basic topology for a two-stage CMOS op-amp with output buffer.
- Examine sources of the parasitic poles present in a two-stage CMOS op-amp.
- Demonstrate an understanding of compensation of the two-stage CMOS op-amp.
- Characterize the CMOS op-amp.
- Discuss and introduction to operational transconductance amplifiers (OTAs).

Reading Assignment

Read Section 25.1 and the first several pages of Section 25.2.

Video Assignment

Watch the Lesson 8 video tutorial.

Key Points

- The basic operational amplifier (op-amp) is made up of two stages so that the gain of the resulting circuit is reasonably large (in the thousands.)

- The compensation capacitor is added to an op-amp so that at high frequencies the gain of the op-amp drops. This is necessary in order to keep the op-amp stable.
- The op-amp is characterized to determine: stability, input common-mode range, CMRR, PSRR, and output voltage swing.
- An operational transconductance amplifier is a single stage amplifier that only has two high impedance nodes; the input node and the output node.

Practice Problems

Do problems 25.1, 25.2, 25.3, 25.8, and 25.11.

Answers to Practice Problems

See the accompanying CD-ROM for practice problem solutions.

Lesson 9 - Op-amp design II

Learning Objectives

After completing this lesson you will be able to:

- Discuss the topology and operation of a folded-cascode OTA.
- Examine op-amp design using a folded-cascode OTA and output buffer.
- Understand the use of floating current sources in output buffer design.
- Demonstrate an understanding of a brief introduction to fully-differential op-amps.
- Recognize the use of gain-enhancement.

Reading Assignment

Read Sections 25.2 and 25.3.

Video Assignment

Watch the lesson 9 video tutorial.

Key Points

- The folded-cascode OTA has good power supply rejection characteristics and can be compensated with a load capacitance.

- An output buffer can be added to a folded-cascode OTA to make a folded-cascode op-amp.
- Floating current sources can be used to set the bias current in a push-pull output stage used in a folded-cascode op-amp.
- Gain enhancement can be used to overcome fundamental gain/bandwidth limitations in CMOS op-amps.

Practice Problems

Do problems 25.19, 25.20, 25.21, 25.25, and 25.26.

Answers to Practice Problems

See the accompanying CD-ROM for practice problem solutions.

Lesson 10 - Comparator design

Learning Objectives

After completing this lesson you will be able to:

- Describe the basic topology of a CMOS comparator.
- Recognize requirements for high speed comparators.
- Design a comparator with hysteresis.
- Recognize the design of clocked comparators.

Reading Assignment

Read Section 26.1.

Video Assignment

Watch the lesson 10 video tutorial.

Key Points

- A comparator must use a pre-amplifier to isolate the inputs from the decision circuit and to provide gain.
- The decision circuit can be designed with hysteresis for avoiding comparator metastability.

- Use of a clock signal can enhance the performance of a comparator.

Practice Problems

Do problems 26.1 (by sketching by hand the resulting output), 26.2, and 26.6.

Answers to Practice Problems

See the accompanying CD-ROM for practice problem solutions.

CMOS

Analog Circuit Design

Final Examination

FINAL EXAM DIRECTIONS

This examination covers the material presented in the Study Guide for "CMOS Analog Circuit Design." This exam is divided into sections, which correspond to the Study Guide lessons. It consists of 100 multiple choice questions, each worth 1 point.

A passing grade of 70% is required to receive a Certificate of Achievement from the IEEE. Please take your time, read the questions carefully and then review your answers when you are finished. Record your answers on the perforated answer sheet at the end of the final exam.

This exam is open book, notes, and Study Guide (meaning you can use these as references while taking the exam). Complete and submit the Answer Sheet.

Completed answer sheets may be returned to the IEEE in one of the following ways:

By Mail - send to:

IEEE Education Department
445 Hoes Lane, PO Box 1331
Piscataway, NJ 08855-1331

By Fax - send to "Education" at 732-981-1686

or

By E-mail - send your list of answers along with the appropriate contact information to:
ssc-exam@ieee.org

GOOD LUCK!

This exam requires the use of the course textbook *CMOS: Circuit Design, Layout, and Simulation*, by Baker, Li and Boyce, IEEE Press, 1998. Unless otherwise stated use the CN20 process parameters given in Appendix A of the text for the problems in this exam.

Lesson 1 - CMOS analog modeling

1. A p-channel MOSFET (PMOS) has a body made using the:

A. p-well

B. p+

C. n+

D. n-well

2. Absolutely zero drain current flows in an n-channel MOSFET when the gate-source voltage is less than the threshold voltage.

A. True

B. False

3. Referring to Fig. 9.1 on page 166; if the DC drain voltage is equal to the DC gate voltage the MOSFET is

A. operating in the saturation region.

B. operating in the triode region.

C. operating in the saturation region as long as the drain voltage is greater than the threshold voltage of the MOSFET.

D. off.

4. If a PMOS device has a V_{SD} of 2.5V and a $V_{SG} = 2$ V the device is operating

A. in the saturation region.

B. in the triode region.

C. in the saturation region as long as the drain voltage is less than the threshold voltage.

D. in the cutoff region.

5. The body effect occurs when the source and substrate (or body) of a MOSFET are electrically shorted together.

A. True.

B. False

6. The body effect causes

A. the gate voltage of the MOSFET to vary.

B. the drain voltage of the MOSFET to vary.

C. the body potential of the substrate to vary.

D. the threshold voltage of the MOSFET to vary.

7. When a MOSFET is operated in the triode region we think of the resistance between the drain and source of the MOSFET

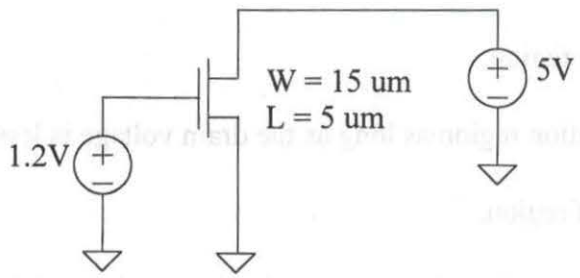
A. as a channel resistance.

B. as a resistance set by channel length modulation.

C. as a resistance set by mobility modulation.

D. as an off MOSFET.

For problems 8 - 10 refer to the MOSFET circuit shown below.



8. What is the, approximate, DC current flowing in the MOSFET (again use the CN20 process parameters given on the front cover of the book.)

A. 1 μA

B. 10 μA

C. 100 μA

D. 1 mA

9. What is the small-signal resistance looking into the drain of the NMOS device?

A. 0.06 V^{-1}

B. 1 MΩ

C. 1.667 MΩ

D. infinite, the device is off.

10. If a 10 mV AC voltage is applied to the gate of the MOSFET how much AC current will flow in the MOSFET.

A. 550 nA

B. 55 μA/V

C. 10 mA.

D. None, the MOSFET doesn't have a load.

Lesson 2 - Current sources and sinks I

11. What happens, when designing a simple current mirror, if we design assuming the MOSFET V_{GS} is close to the threshold voltage?

A. The device sizes become very large.

B. Threshold voltage variations have a large affect on the matching between the device currents.

C. The current mirror functions properly.

D. All of the above.

12. The output resistance of a current mirror has a small bearing on the matching between the two currents flowing in the devices comprising the mirror.

A. True

B. False

13. What happens, in Example 20.1 on pages 429 and 430, if we increase the width of M2 (in Fig. Ex20.1) so that it is 150 μm?

A. M2's V_{GS} gets smaller.

B. M2's V_{GS} gets larger.

C. M2's current becomes 1 μA

D. M2's current becomes 100 μA.

14. If two identically sized MOSFETs have exactly the same drain currents and gate to source voltages how are their drain to source voltages related?

A. They are the same too.

B. They are equal to the gate to source voltage of the MOSFETs.

C. It can't be determined by the information given.

D. The voltages are the product of the drain current and the gate to source voltages.

15. The small-signal output resistance of a simple current mirror increases with:

A. an increase in operating current.

B. a decrease in operating current.

C. the output resistance of the mirror is not a function of the operating current.

D. it doesn't make sense to talk about output resistance of a current mirror since it is not an amplifier.

16. The cascode connection of MOSFET used in a current mirror is used to increase the output resistance of the current mirror.

A. True

B. False

17. Why don't we use minimum channel lengths when designing CMOS current mirrors?

A. Because the resulting circuit takes up smaller area.

B. The output resistance can get really large causing biasing problems.

C. We want to keep the MOSFET output resistance as large as possible and using minimum channel length results in lower output resistance.

D. None of the above.

18. In Ex. 20.4 on page 437 what is the value of R needed in the current mirror if we want the MOSFETs to conduct 100 μA assuming the MOSFET V_{GS} remain 1.2V?

A. 260 Ω

B. 2.6 kΩ

C. 26 kΩ

D. 260 kΩ

19. How do the MOSFET's widths change in problem 18?

A. They don't, they remain 15 μm

B. Since the MOSFETs are conducting ten times more current the widths, for a V_{GS} of 1.2 V, become 150 μm.

C. The widths become, approximately, 33 μm.

D. The widths become, approximately, 73 μm.

20. The cost for using the cascode mirror configuration over the simple current mirror is:

A. increased layout area.

B. higher minimum voltage across the current source/sink.

C. more complicated circuit.

D. all of the above.

Lesson 3 - Current sources and sinks II

21. The drain current of a MOSFET with a fixed gate-source voltage and operating in the saturation region

A. decreases with increasing temperature under all situations.

B. increases with increasing temperature under all situations.

C. doesn't change with temperature under all situations.

D. may increase or decrease depending on the region of operation.

22. If a current mirror is made using a 15/5 NMOS and a 150/5 MOSFET care should be used when laying out the devices to ensure oxide encroachment doesn't affect the MOSFETs' lengths.

A. True.

B. False.

23. If a current sink is made with a pair of NMOS devices is it possible the change in voltage across the output device will drastically affect the current? Can it cause and error in the output current in excess of 100% of the typical output current value?

A. Yes

B. No

24. If we want to design a current mirror that is insensitive to variations, from one device to another, in threshold voltage we would

A. bias the current mirror with a large V_{GS}.

B. bias the current mirror with a V_{GS} a few hundred mV above the threshold voltage.

C. bias the current mirror with a small V_{GS}.

D. None of the above.

25. The oxide thickness variation from one device to another will not affect how well the devices match.

A. True

B. False

26. The Wilson current mirror results in what improvement in performance over the basic cascode current mirror?

A. Improved output resistance.

B. Improved minimum voltage across the current mirror.

C. Both A and B.

D. Neither A or B.

27. The regulated cascode current mirror results in what improvement in performance over the basic cascode current mirror?

A. Improved output resistance.

B. Improved stability.

C. Both A and B.

D. Neither A or B.

28. In Fig. 20.27 on page 456 what happens to the output current if M4 and M2s width is increased to 150 μm?

A. Nothing because the devices gate-source voltages do not change.

B. The current goes up by a factor of ten.

C. The current goes down by a factor of ten.

D. The current increases by the root of 10.

29. The output resistance of the wide-swing, low-voltage cascode circuit shown in Fig. 20.27 is the same as the cascode circuit shown in Fig. Ex20.4 when all devices are operating in the saturation region.

A. True

B. False.

30. In Fig. 20.27 M2 and M4 don't suffer from the body effect.

A. True

B. False.

Lesson 4 - References I

31. The operation of the resistive voltage divider is very dependent on process variations in the sheet resistance of the material used for the resistors.

A. True

B. False

32. What is the major benefit of the MOSFET divider over the resistive divider?

A. Better process tolerance.

B. Smaller layout for a given power dissipation.

C. More immune to ESD.

D. None of the above are true.

33. Voltage dividers made using resistors and MOSFETs have outputs that are very dependent on the power supply voltages.

A. True

B. False

34. Self-biasing circuits use positive feedback to reduce the circuits output current or voltage sensitivity to power supply variations.

A. True

B. False

35. The threshold voltage reference biasing circuit uses

A. a threshold voltage as a reference voltage because the threshold voltage of a MOSFET doesn't change with temperature.

B. a resistor, whose value increases with increasing temperature, together with the threshold voltage of a MOSFET, whose value also increases with increasing temperature to make a current that is independent of temperature variations.

C. a resistor, whose value increases with increasing temperature, together with the threshold voltage of a MOSFET, whose value also decreases with increasing temperature to make a current that is dependent of temperature variations.

D. none of the above.

36. A start-up circuit is required in self-biased reference circuits because

A. the possibility that zero current will flow in the circuit exists.

B. the possibility that the circuit will oscillate is a real concern.

C. it increases the complexity of the circuit and thus makes the reference appear more complicated then it really is.

D. it generates a voltage for the reference when the power supplies are not applied to the circuit.

37. In a diode referenced self-biasing circuit the diode voltage is

A. dropped across the substrate to generate a reference current.

B. can be zero if a start-up circuit isn't used.

C. is dropped across a resistor to generate a reference current.

D. both B and C.

38. The diode referenced biasing circuit has a large negative temperature coefficient because the resistor value increases with temperature while the voltage across the diode, with a constant current flowing through the diode, decreases with increasing temperature.

A. True

B. False

39. The thermal voltage reference biasing circuit requires a known temperature be applied to the reference circuit to generate a known current.

A. True

B. False

40. The change in the thermal voltage, with temperature, is constant.

A. True

B. False

Lesson 5 - References II

41. Bandgap references rely on that fact that the bandgap of silicon is a constant. This can be used to design voltage references that are independent of temperature.

A. True

B. False

42. A bandgap reference can be made by adding a multiple of the thermal voltage with a diode forward voltage. This causes

A. the positive temperature coefficient of the thermal voltage to cancel with the negative temperature coefficient of the forward diode voltage.

B. the positive temperature coefficient of the thermal voltage to cancel with the positive temperature coefficient of the forward diode voltage.

C. the bandgap voltage of silicon to stay at a fixed value over changes in temperature.

D. none of the above.

43. A bandgap can only be made in CMOS if

A. a diode is used external to the chip.

B. a MOSFET is used as a diode.

C. the parasitics present in the CMOS process are used to make the diode.

D. none of the above.

44. Why won't the variation in the sheet resistance affect the output voltage of the bandgap reference?

A. It will. There is no way to keep the sheet resistance from changing in a CMOS process.

B. The change is too small to matter.

C. We are interested in the ratio of the resistors and not the actual resistor values, within reason.

D. The resistor we use will be part of the diode so that as the diode characteristics change so will the resistors.

45. The Beta-muliplier reference is used in CMOS since it doesn't use parasitics.

A. True

B. False

46. The Beta-multiplier's temperature performance is determined by

A. the variations in the fabrication of resistors.

B. the parasitic diodes present in the circuit.

C. the sum of the voltage dropped across the resistor and a MOSFET gate-source voltage.

D. none of the above.

47. The Beta-multiplier can be used as both a voltage and a current reference.

A. True

B. False

48. The Beta-multiplier reference can be used to bias circuits in the subthreshold region.

A. True

B. False

49. If the resistor, in Fig. 21.17 on page 481, is made really large the voltage between the gate and source of M2 will be essentially a threshold voltage. This will cause the temperature coefficient of the output current to be negative at room temperature.

A. True

B. False

50. Power supply variations should have a small effect on a properly designed self-biased bandgap or beta-multiplier reference.

A. True

B. False

Lesson 6 - Amplifiers

Assume, for the remainder of the exam, that all MOSFETs are operating in the saturation region (unless otherwise indicated.)

51. A gate-drain connected MOSFET load can be thought of as

A. very small capacitance.

B. a current sink/source.

C. a resistor of value r_o.

D. a resistor with a value of $1/g_m$.

52. The amplifier in Fig. 22.7 on page 495 is a

A. common drain amplifier.

B. common gate amplifier.

C. common source amplifier.

D. source follower amplifier.

53. The common source amplifier with gate-drain connected load has the benefit of

A. wide bandwidth.

B. high gain.

C. process intolerance.

D. A and B.

54. A common source amplifier with current source load can increase its gain by reducing its biasing current.

A. True

B. False

55. The amplifier in problem 54 can also increase its speed by decreasing its biasing current.

A. True

B. False

56. The cascode connection is used to increase the gain of an amplifier by

A. increasing the number of MOSFETs used in the circuit.

B. decreasing the Miller effect.

C. increasing the effective output resistance of an amplifier.

D. none of the above.

57. The common source amplifier with current source load is limited in drive by

A. the available current from the common source MOSFET.

B. the load current source/sink.

C. the speed of the circuit driving the amplifier.

D. it isn't limited in drive.

58. The source-follower has a low output impedance and good drive even though it's load may be a current source/sink.

A. True

B. False

59. By increasing the widths of the MOSFETs used in a source follower it is possible to get a reasonably large gain, in general, at least a gain of ten.

A. True

B. False

60. The speed of an amplifier can be increased by increasing the gate-source voltages of the MOSFETs used in the amplifier while holding the MOSFET lengths used constant.

A. True, if the inherent speed of the MOSFETs is limiting the amplifier speed.

B. True, if the load is limiting the speed of the amplifier.

C. False, the speed of an amplifier has nothing to do with the V_{GS} of the MOSFETs used.

D. False, the length of the MOSFETs used in an amplifier has nothing to do with the speed.

Lesson 7 - Differential amplifiers

61. The maximum input differential voltage, v_{DIMAX},

A. increases with increasing diff-pair bias current.

B. decreases with decreasing diff-pair bias current.

C. increases with increasing diff-pair length.

D. all of the above.

62. The common mode range of a diff-amp is defined as the input voltage, common to both inputs, that the MOSFETs in a diff-amp will stay in the saturation region.

A. True

B. False

63. The gain of a diff-amp increases with increasing I_{SS}.

A. True

B. False

64. Suppose the gate of MOSFET M1, in Fig. 24.11 on page 590, is grounded (just as is the gate of M2.)

A. The current through M3 and M4 is equal.

B. The current through M6 is equal to the sum of the currents through M3 and M4.

C. The voltage on the drain of M4 is the same as the voltage on the gate of M3.

D. All of the above.

65. Suppose, in problem 64, a 140/5 PMOS device has its source connected to VDD, its gate connected to the drain of M4 and its drain connected to ground. Neglecting the finite MOSFET output resistance and oxide encroachment what is the current that flows in this device?

A. The same as the current that flows in M2.

B. The same as the current that flows in M4.

C. Twice the current that flows in M4.

D. Twice the current that flows in M6.

66. The offset voltage associated with a diff-amp can be reduced by

A. layout techniques.

B. attempting to minimize the mismatch in the load.

C. designing with small V_{GS}.

D. all of the above.

67. The basic diff-amp can source or sink a maximum current of I_{SS}.

A. True

B. False

68. The source cross-coupled diff-amp doesn't have slew-rate limitations because

A. it is a more complicated circuit.

B. there isn't a current source in series with the diff-amp.

C. it uses two regular diff-amps and adds the output currents.

D. all of the above.

69. The bias batteries shown on the right side of Fig. 24.17 on page 596 are generated by

A. passing a constant current through a resistor.

B. passing a constant current through two MOSFETs.

C. external batteries supplied outside of the chip.

D. additional diff-amps that will automatically adjust the bias potential.

70. Wide swing diff-amps

A. have rail to rail input common-mode range.

B. have rail to rail output voltage swing.

C. don't have slew-rate limitations.

D. are less complicated then regular diff-amps.

Lesson 8 - Op-amp design I

71. A compensation capacitor is used to lower the gain of an op-amp at high frequencies so the op-amp doesn't become unstable when used with feedback.

A. True

B. False

72. For the op-amp shown in Fig. 25.2, for biasing purposes, we treat the gate of M7 as if

A. it were tied to the drain of M4.

B. it were tied to the gate of M4.

C. it were tied to an external bias voltage.

D. none of the above.

73. We can determine if an op-amp is stable by looking at the op-amps

A. open-loop magnitude frequency response.

B. open-loop magnitude phase response.

C. open-loop magnitude and phase frequency responses.

D. none of the above.

74. Referring to Fig. 25.11 on page 628 the node common to the drains of M1 and M3 is a low impedance node with an approximate small-signal resistance to ground of $1/g_{m3}$.

A. True

B. False

75, An op-amps common mode rejection ratio is determined by

A. the characteristics of the input diff-amp.

B. the open-loop gain of the op-amp.

C. the gain of the second stage used in the op-amp

D. all of the above.

76. The dominant pole in a two stage compensated op-amp should come from the combination of the compensation capacitance and the output resistance of the first stage.

A. True

B. False

77. The two stage op-amp shown in Fig. 25.11 without output buffer can be considered an operational transconductance amplifier.

A. True

B. False

78. An OTA is useful because

A. it can be used as part of an op-amp.

B. it can be compensated with a load capacitance.

C. it can be used in a filter.

D. all of the above.

79. In Fig. 25.22 on page 637 the drain of M6 is a high-impedance node.

A. True

B. False

80. OTAs don't have slew-rate limitations.

A. True

B. False

Lesson 9 - Op-amp design II

81. Referring to the schematic of the folded cascode OTA shown in Fig. 25.42 why aren't the drains of M1 and M2 considered high-impedance?

A. Because it is a high impedance looking into the drains of M5 and M6.

B. Because it is a low impedance looking into the drains of M7 and M8.

C. Because it is a low impedance looking into the sources of M5 and M6.

D. Because it is a low impedance looking into the sources of M7 and M8.

82. Referring again to Fig. 25.42 if the power supply, VDD, contains a ripple this ripple will affect each side of the folded cascode section equally.

A. True

B. False

83. An op-amp can be formed with a folded cascode OTA and a source follower. The resultant op-amp can be compensated by

A. the same methods used to compensate any two-stage op-amp design.

B. the input capacitance of the source follower.

C. a load capacitance to ground on the output of the OTA.

D. all of the above.

84. A wide swing folded cascode OTA is designed so the output of the OTAs common mode voltage extends to the supply rails.

A. True

B. False

85. Referring to Fig. 25.49 the sum of the source-gate voltages MC3 and MO1 are set by V_{biasp}. This is used to set the bias current in the output p-channel MOSFET.

A. True

B. False

86. The purpose of a common-mode feedback circuit is to

A. increase a fully-differential op-amps gain.

B. double the output swing of a fully-differential op-amp.

C. hold the average of the op-amps inputs at a known value.

D. hold the average of the op-amps outputs at a known value.

87. Gain enhancement is used

A. to increase the gain of an op-amp.

B. to speed up the settling time of an op-amp.

C. to increase the bandwidth of an op-amp.

D. all of the above.

88. The intrinsic speed of a MOSFET is not a function of the MOSFETs gate to source voltage but rather is simple a function of the MOSFETs drain current.

A. True

B. False

89. An op-amp that uses gain-enhancement doesn't possess slew-rate limitations.

A. True

B. False

90. Fully-differential op-amps are used because:

A. they have better noise rejection characteristics.

B. they take up more layout area.

C. they dissipate less power than a single-ended output op-amp.

D. all of the above.

Lesson 10 - Comparator design

91. A comparator utilizes feedback to reduce propagation delays and to increase gain.

A. True

B. False

92. The pre-amp is used in a comparator to

A. isolate the switching noise in the decision circuit from the input of the comparator.

B. to amplify the input signal so the comparator is more sensitive.

C. to change the input voltage signal into a current.

D. all of the above.

93. A comparator may use hysteresis to when the inputs to the comparator vary at a slow rate. This may be necessary to keep the comparator from oscillating.

A. True

B. False

94. The two-stage op-amp can be used as a comparator, without compensation capacitance, and has good symmetrical high to low and low to high propagation times.

A. True

B. False

95. The offset voltage of a comparator is mainly determined by the input pre-amp.

A. True

B. False

96. Improvements in comparator sensitivity come directly from increasing the speed of the decision circuit.

A. True

B. False

97. A clocked comparator can be used to sample, at a particular instant in time, the inputs to the comparator.

A. True

B. False

98. The transconductance of a diff-amp used in a comparator doesn't affect the speed of the comparator.

A. True

B. False

99. The comparator of Fig. 26.11 can be used as an op-amp provided feedback is used around the circuit.

A. True

B. False

100. The high to low propagation delay of a comparator should match the low to high propagation delay in many applications.

A. True

B. False, the high to low delay is always irrelevant.

Answer Sheet

CMOS ANALOG CIRCUIT DESIGN

NAME_____
ADDRESS_____
CITY_____ STATE/PROV_____ POSTAL CODE_____
DATE_____

INSTRUCTIONS

1. Read each question in the Final Examination and select the correct answer. Place a check adjacent to your answer.
2. Using a pencil, circle the letter corresponding to your answer choice. Be careful in transferring your answer. If you should circle the wrong choice, erase your mark completely. Double check this answer sheet against your choices on the Final Examination.
3. Fill in the remainder of this answer sheet. Write your complete name and address in the spaces provided. Sign the exam in the space provided at the end of the Examination Answer Sheet.
4. Make a copy of this answer sheet for your records.
5. Return this answer sheet to IEEE by Mail, Fax or Internet (ssc-exam@ieee.org). If submitting by internet, please remember to provide your full name and mailing address.

1.	A	B	C	D	26.	A	B	C	D	51.	A	B	C	D	76.	A	B		
2.	A	B			27.	A	B	C	D	52.	A	B	C	D	77.	A	B		
3.	A	B	C	D	28.	A	B	C	D	53.	A	B	C	D	78.	A	B	C	D
4.	A	B	C	D	29.	A	B			54.	A	B			79.	A	B		
5.	A	B			30.	A	B			55.	A	B			80.	A	B		
6.	A	B	C	D	31.	A	B			56.	A	B	C	D	81.	A	B	C	D
7.	A	B	C	D	32.	A	B	C	D	57.	A	B	C	D	82.	A	B		
8.	A	B	C	D	33.	A	B			58.	A	B			83.	A	B	C	D
9.	A	B	C	D	34.	A	B			59.	A	B			84.	A	B		
10.	A	B	C	D	35.	A	B	C	D	60.	A	B	C	D	85.	A	B		
11.	A	B	C	D	36.	A	B	C	D	61.	A	B	C	D	86.	A	B	C	D
12.	A	B			37.	A	B	C	D	62.	A	B			87.	A	B	C	D
13.	A	B	C	D	38.	A	B			63.	A	B			88.	A	B		
14.	A	B	C	D	39.	A	B			64.	A	B	C	D	89.	A	B		
15.	A	B	C	D	40.	A	B			65.	A	B	C	D	90.	A	B	C	D
16.	A	B			41.	A	B			66.	A	B	C	D	91.	A	B		
17.	A	B	C	D	42.	A	B	C	D	67.	A	B			92.	A	B	C	D
18.	A	B	C	D	43.	A	B	C	D	68.	A	B	C	D	93.	A	B		
19.	A	B	C	D	44.	A	B	C	D	69.	A	B	C	D	94.	A	B		
20.	A	B	C	D	45.	A	B			70.	A	B	C	D	95.	A	B		
21.	A	B	C	D	46.	A	B	C	D	71.	A	B			96.	A	B		
22.	A	B			47.	A	B			72.	A	B	C	D	97.	A	B		
23.	A	B			48.	A	B			73.	A	B	C	D	98.	A	B		
24.	A	B	C	D	49.	A	B			74.	A	B			99.	A	B		
25.	A	B			50.	A	B			75.	A	B	C	D	100.	A	B		

SIGNATURE_____