Ch. 9 Mixed-Signal

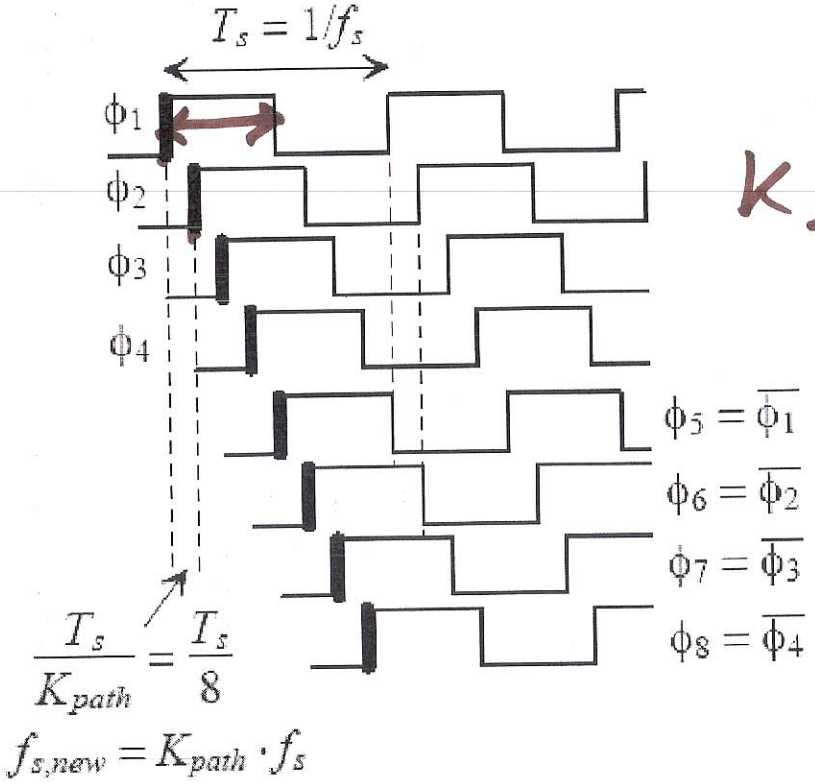


Figure 9.1 Showing the clock signals used for time-interleaved sampling and the high-speed topologies discussed in this chapter.

$f_s \cdot K = f_{s,new}$

K_{path} OSR

$K_{path} \cdot K = OSR$

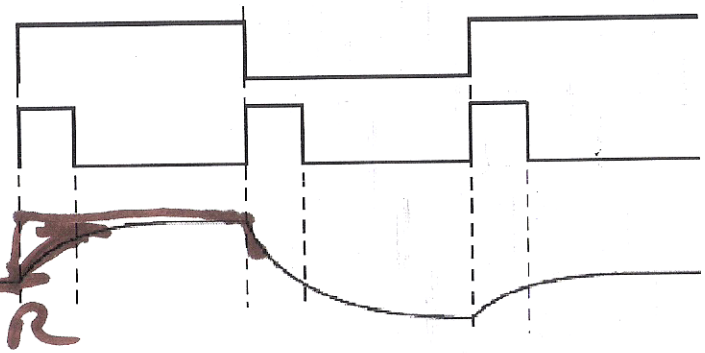


Fig. 2.37

Fig. 9.1

Figure 9.2 Charging discharging a switched-capacitor.

slewing is bad

$x(t)$ → $y(t) = K \cdot x(t - t_0)$

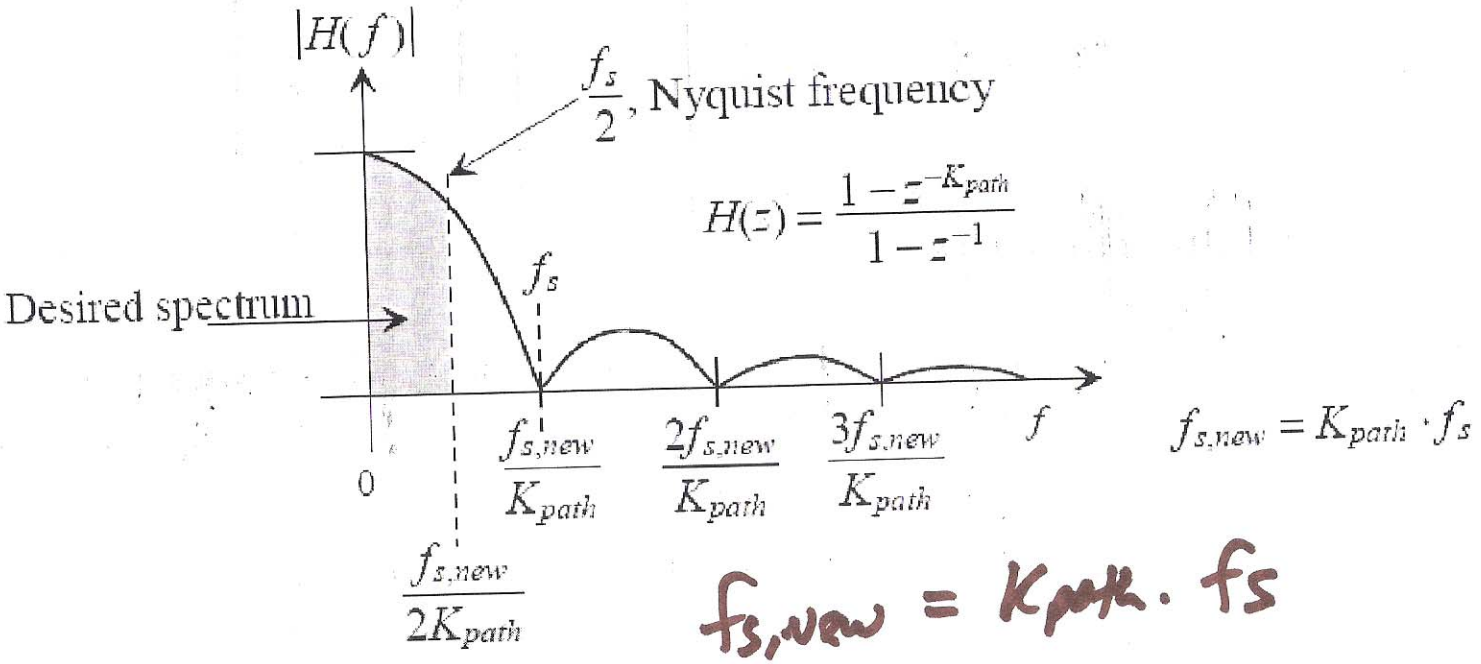


Figure 9.3 Frequency response of the summing circuit (path filter) seen in Fig. 9.4.

3)

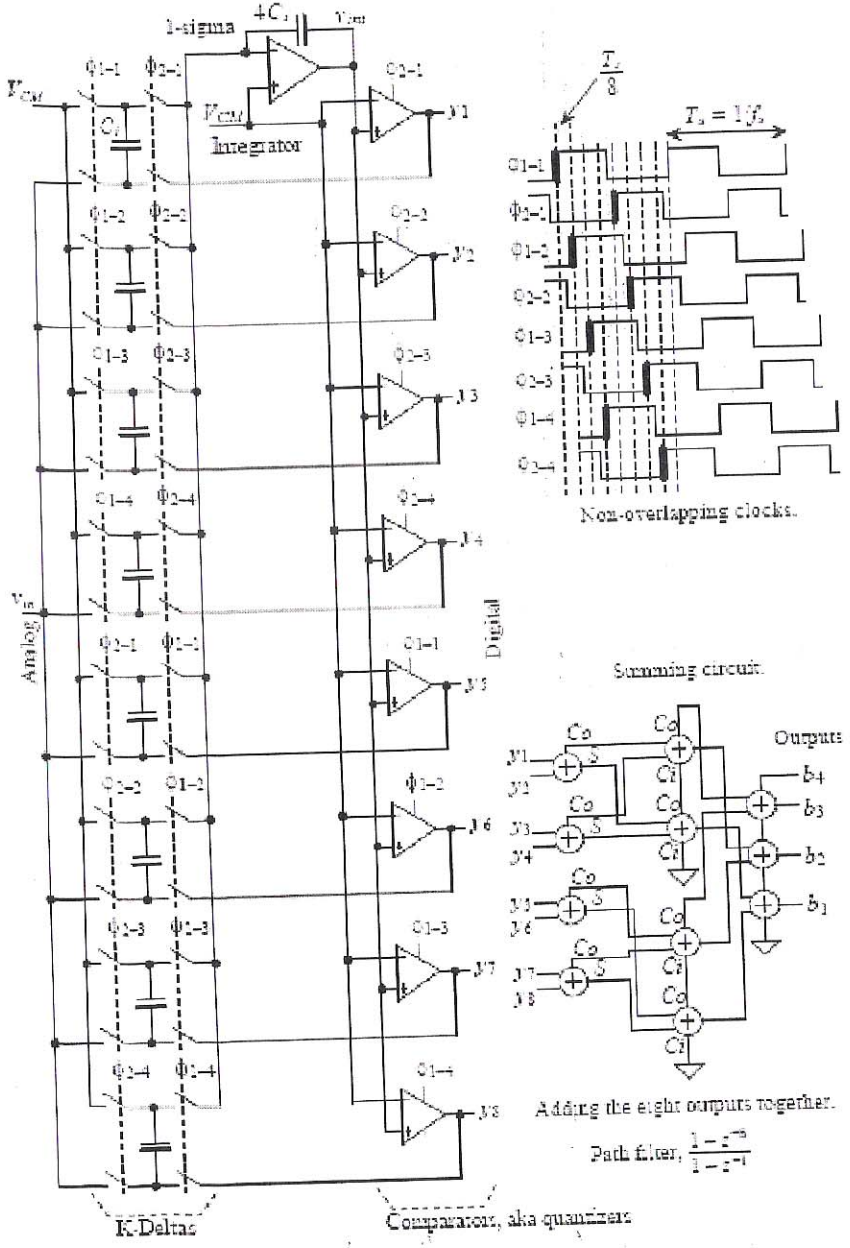
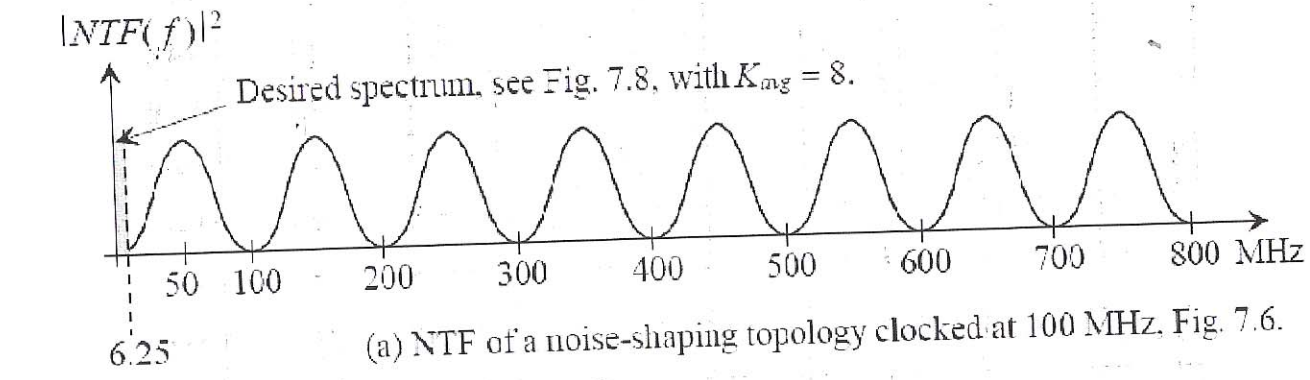


Figure 9.4 A topology for high-speed data conversion using mixed-signal techniques, the K-delta-1-sigma topology.

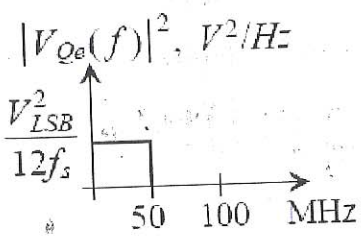
1111 0000 ←

1010 1010 ←

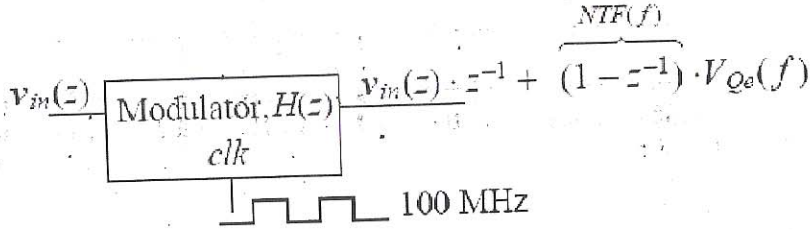
4)



(a) NTF of a noise-shaping topology clocked at 100 MHz, Fig. 7.6.

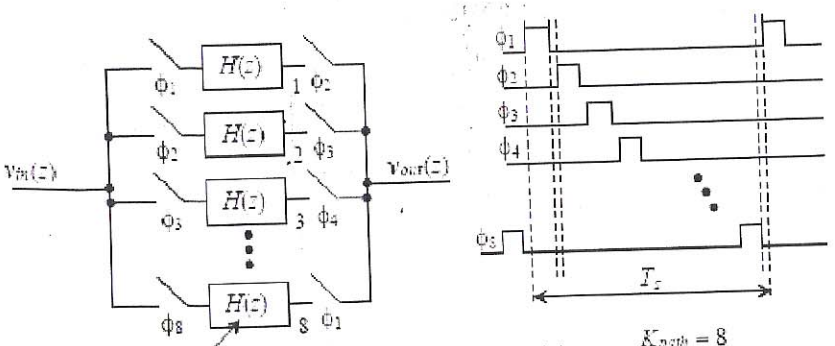


(b) Quantization noise PSD, Fig. 5.12.



(c) Modulator clocked at 100 MHz.

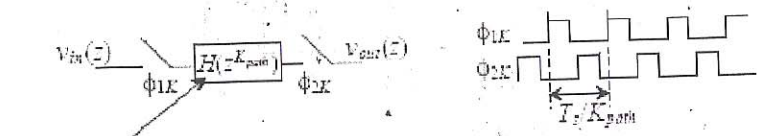
Figure 9.19 NTF and quantization noise spectrums of a first-order NS modulator clocked at 100 MHz with $K_{avg} = 8$.



(a) 8 modulators in parallel

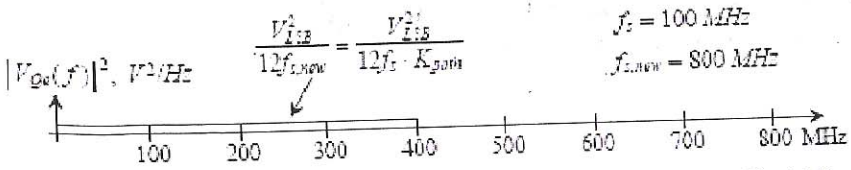
$K_{path} = 8$

$$H(z) = V_{in}(z) \cdot z^{-1} + (1 - z^{-1}) \cdot V_{Qe}(f)$$

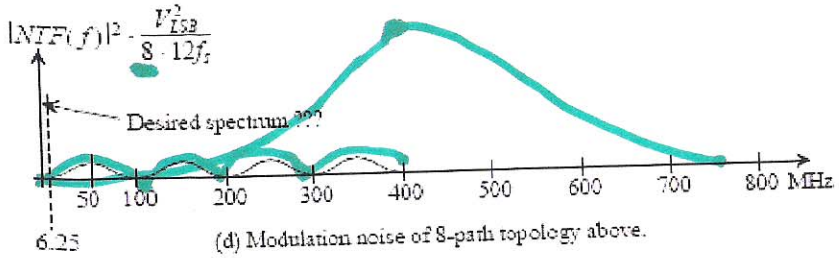


(b) Equivalent circuit

$$H(z^{K_{path}}) = V_{in}(z) \cdot z^{-K_{path}} + (1 - z^{-K_{path}}) \cdot V_{Qe}(f)$$



(c) Quantization noise for an 8-path topology clocked 100 MHz, compare to Fig. 9.19b.

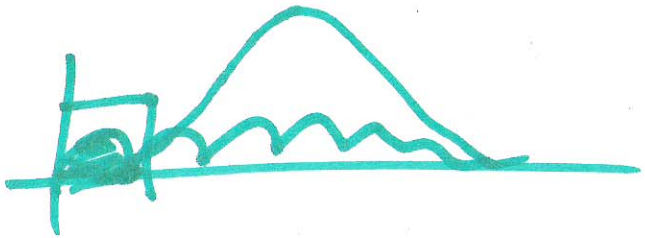


(d) Modulation noise of 8-path topology above.

Figure 9.20 Eight modulators in parallel (a time-interleaved topology).

$z \rightarrow z^8$

poly graph



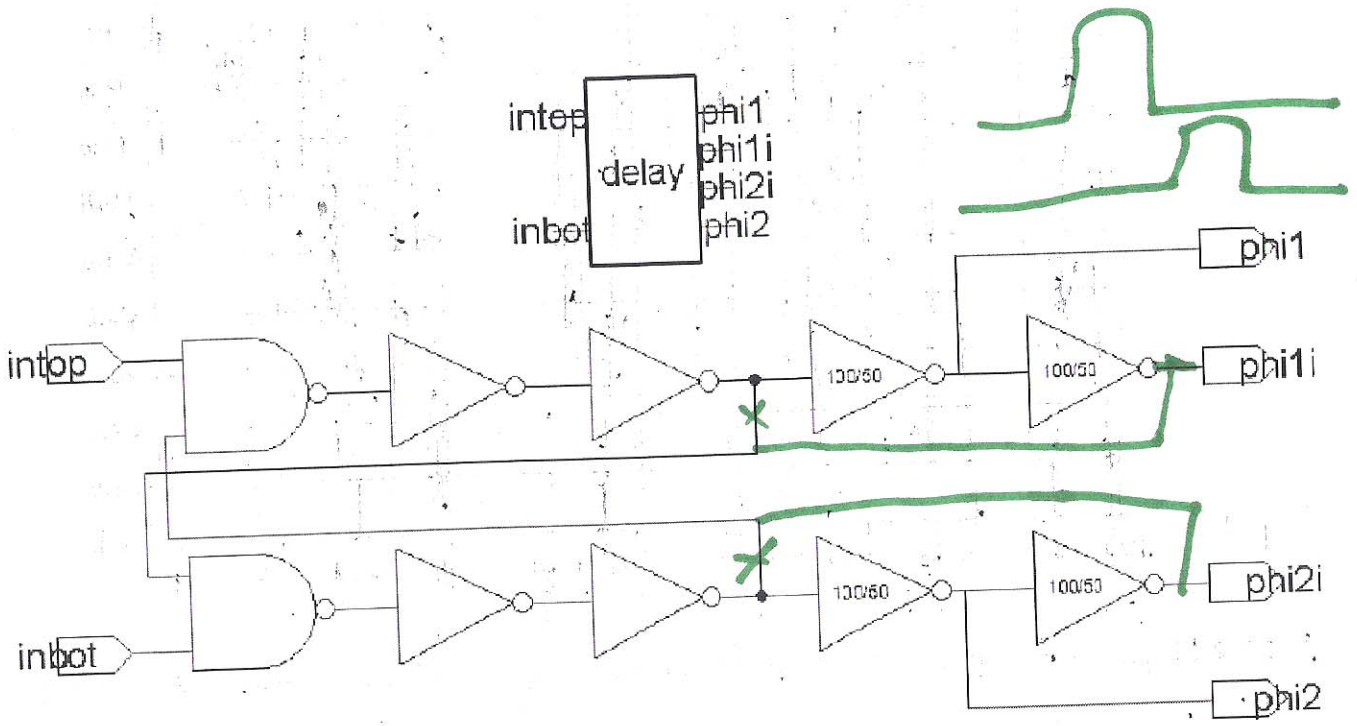
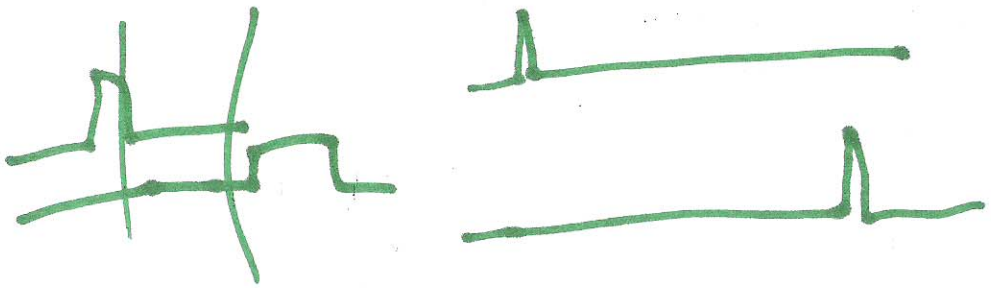


Figure 9.23 Delay stage used in the ring oscillator, schematic and icon.



7)

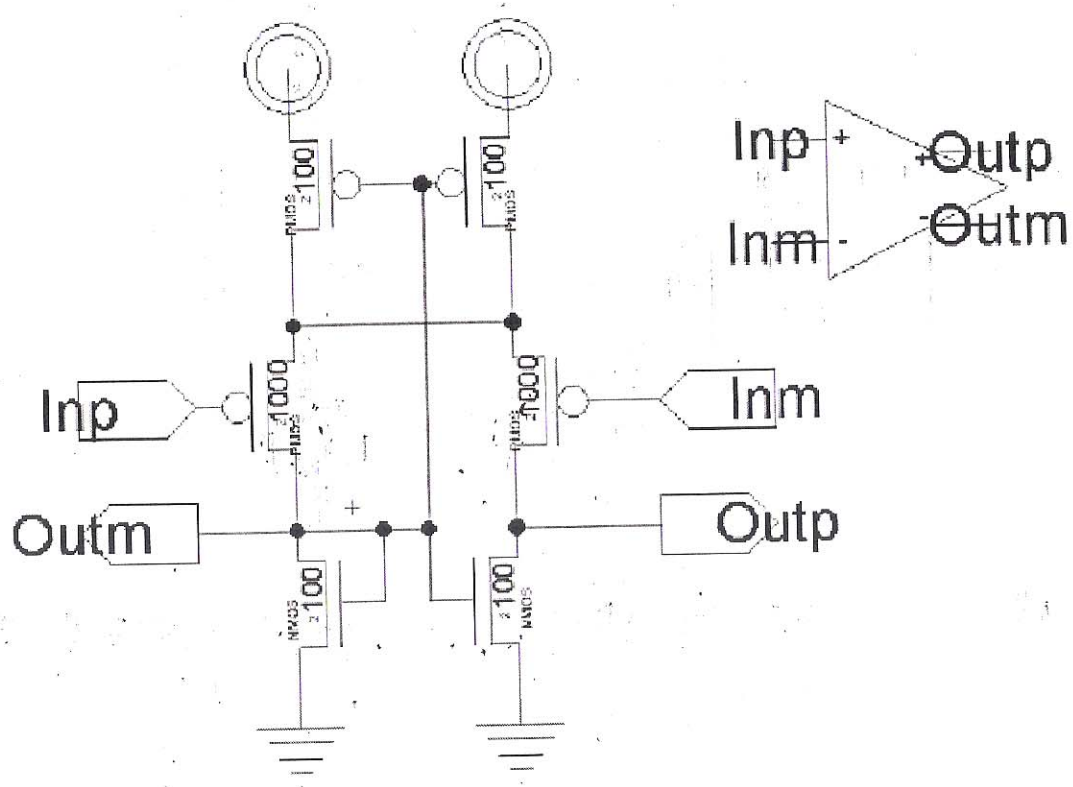


Figure 9.28 Self-biased amplifier and icon.

8)