Ch. 4 – Digital filters

Friday make-up

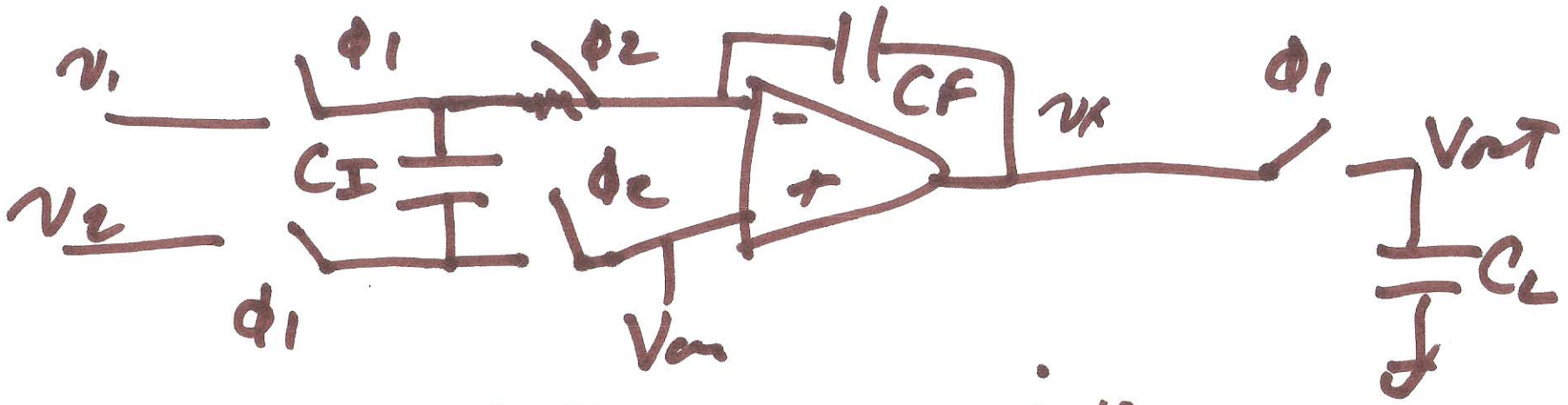
4–5:15 pm

TBE B178

NO H.W due

NO Quiz

if you can't make it watch the video before Monday 9/29



ϕ_1 ↓ ϕ_1 switches one opening

$$C_I\left(v_1[(N-1)T]^{+V_{cm}} - v_2[(N-1)T]^{+V_{cm}}\right) = Q_I$$

$$\left(v_{out}(NT) - v_{out}((N-1)T)\right).C_F =$$

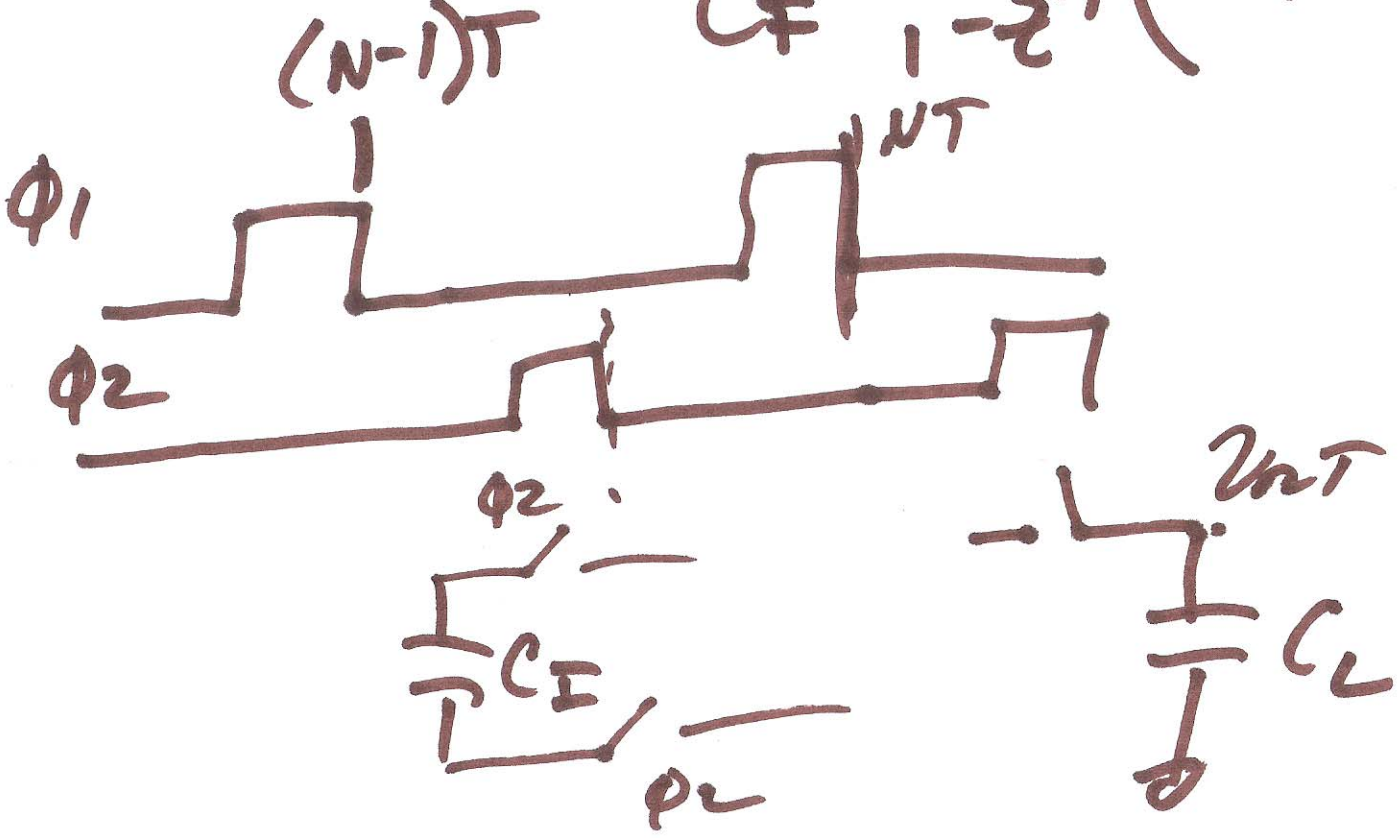
$$V_{out}(z)(1-z^{-1}).C_F$$

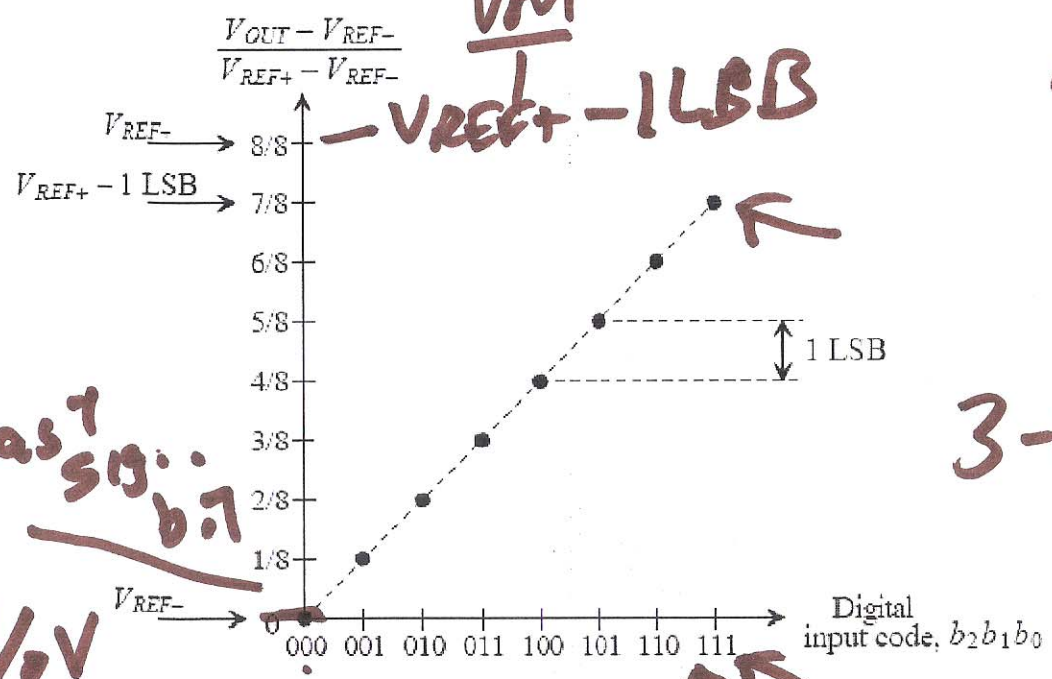
$$= C_I.V_1(z)z^{-1} - V_2(z).C_I.z^{-1}$$

$$C_I\left(v_1([(N-1)T]\right.$$

$$\left. - v_2[(N-1)T]\right)$$

$$V_{OUT}(z) = \frac{C_I}{C_F} \frac{z^{-1}}{1-z^{-1}} \left(V_1(z) - V_2(z) \right)$$





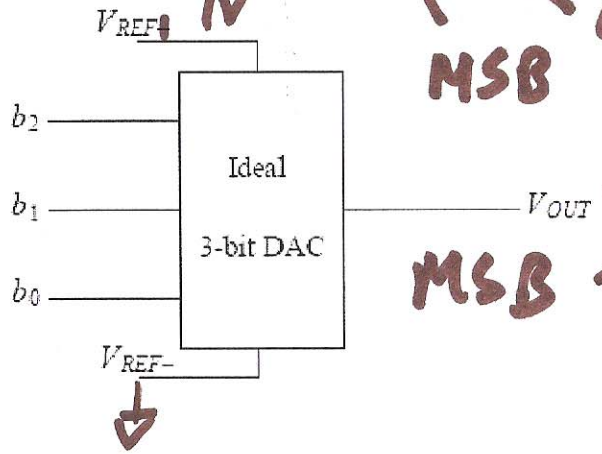


Figure 4.1 An ideal 3-bit DAC.

VFS

$= V_{REF+} - 1LSB$

$LSB = \frac{V_{REF+} - V_{REF-}}{2^N}$

Least Sig.. b.1

$\frac{1}{8}V$

3-bits $2^3 = 8$

$2^8 = 256$

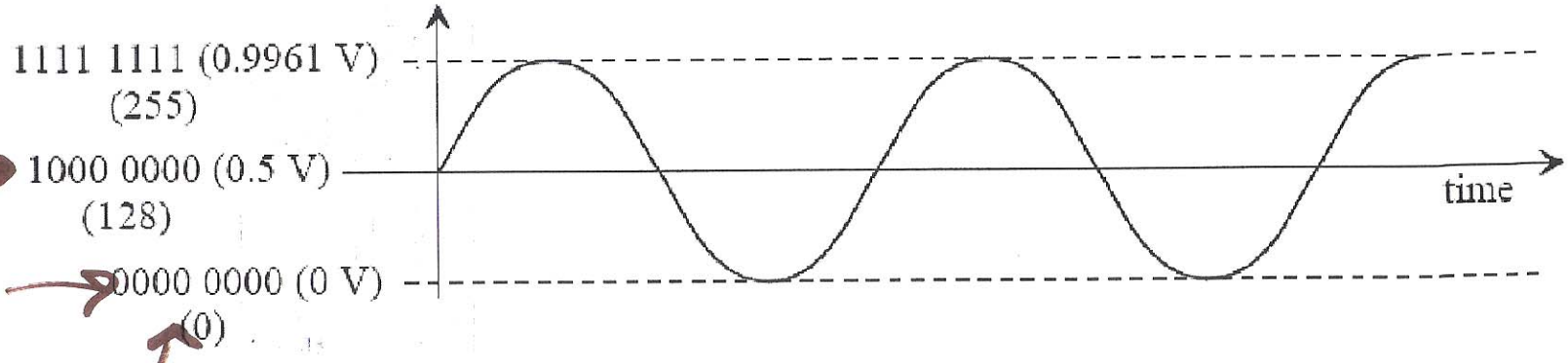
V_{REF+} 1V

MSB LSB

$V_{OUT} = (V_{REF+} - V_{REF-}) \cdot$

MSB $\left(\frac{b_{N-1}}{2^1} + \frac{b_{N-2}}{2^2} + \cdots \frac{b_0}{2^N} \right) + V_{REF-}$

$\frac{1}{2^8} \approx 4mV$



V_{cm}

Figure 4.4 Representing a sinusoid in binary offset format.

offset binary → complement the MSB → two's completion

1000 0000

V_{cm} V_{cm} V_{cm}

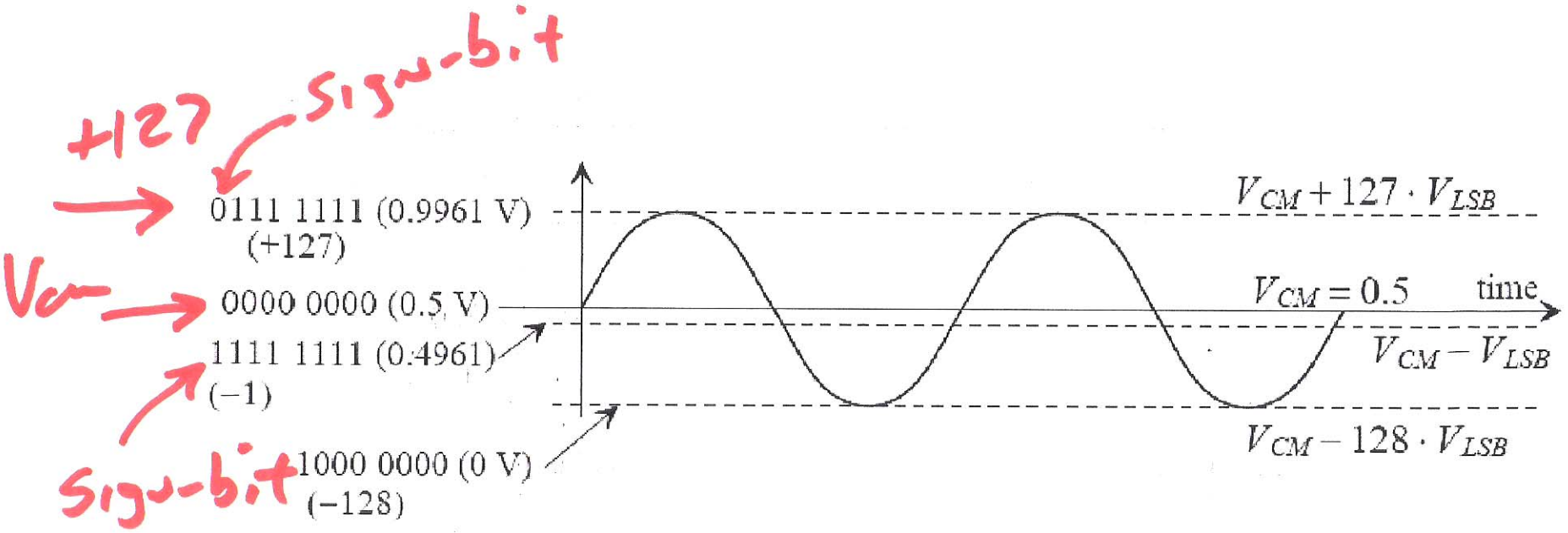
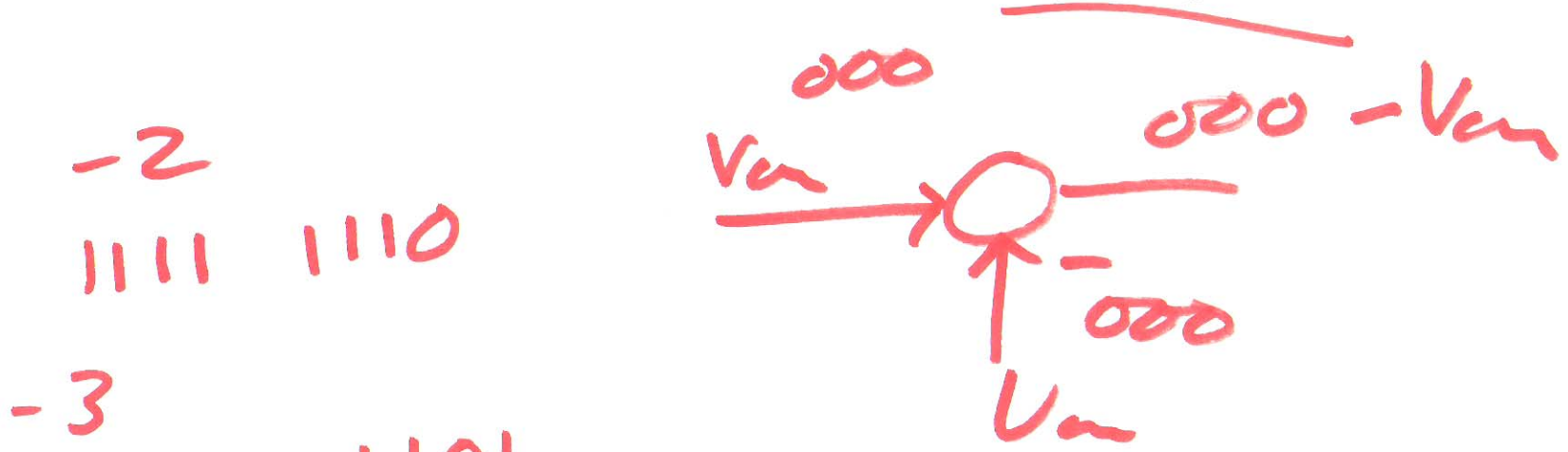
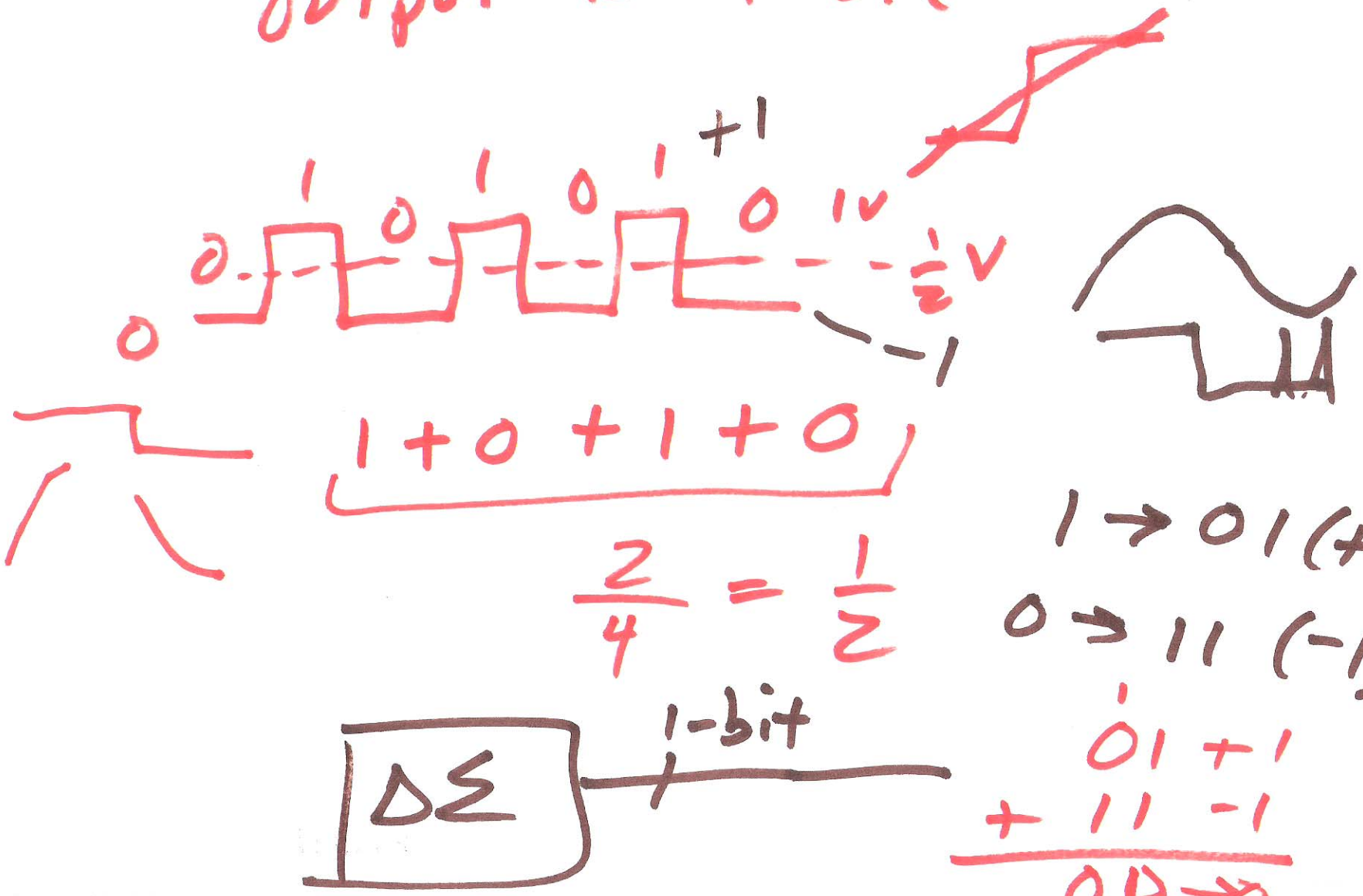


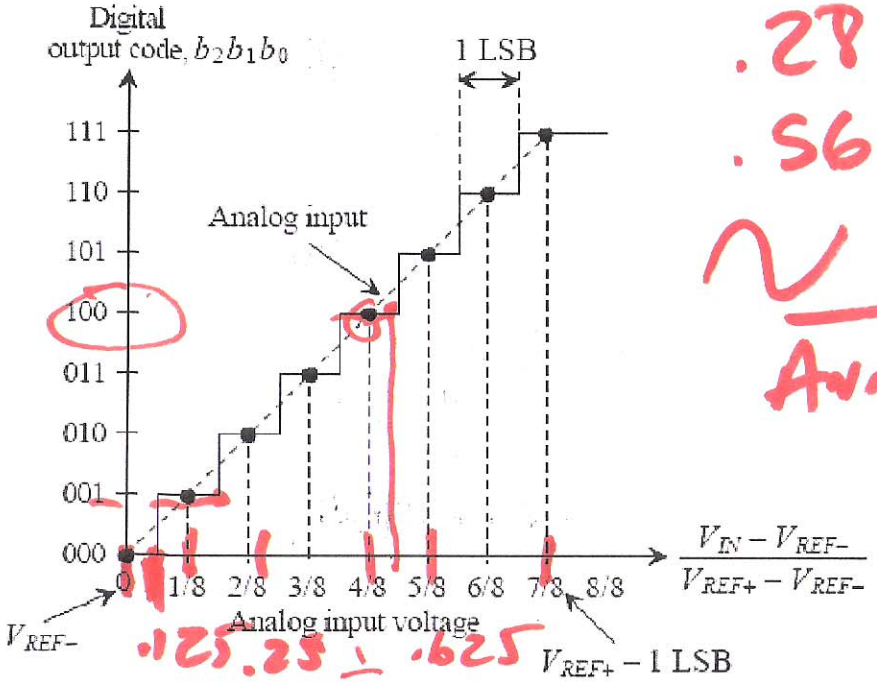
Figure 4.5 Representing a sinusoid in two's complement format.



Delta-Sigma ADC

output is 1-bit





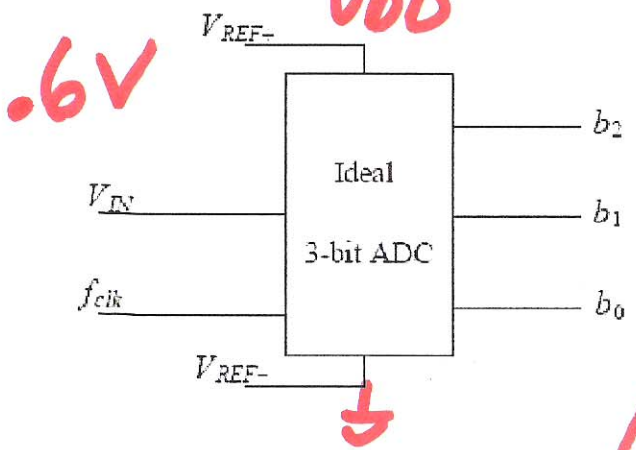


Figure 4.3 An ideal 3-bit ADC.

.14 $b_2 = 0$

.28 $b_1 = 0$

.56 $b_0 = 1$

.125 .25 .625

$\frac{1}{2}$ VDD

.6V

$$V_{in} = \frac{VREF+ + VREF-}{2}$$

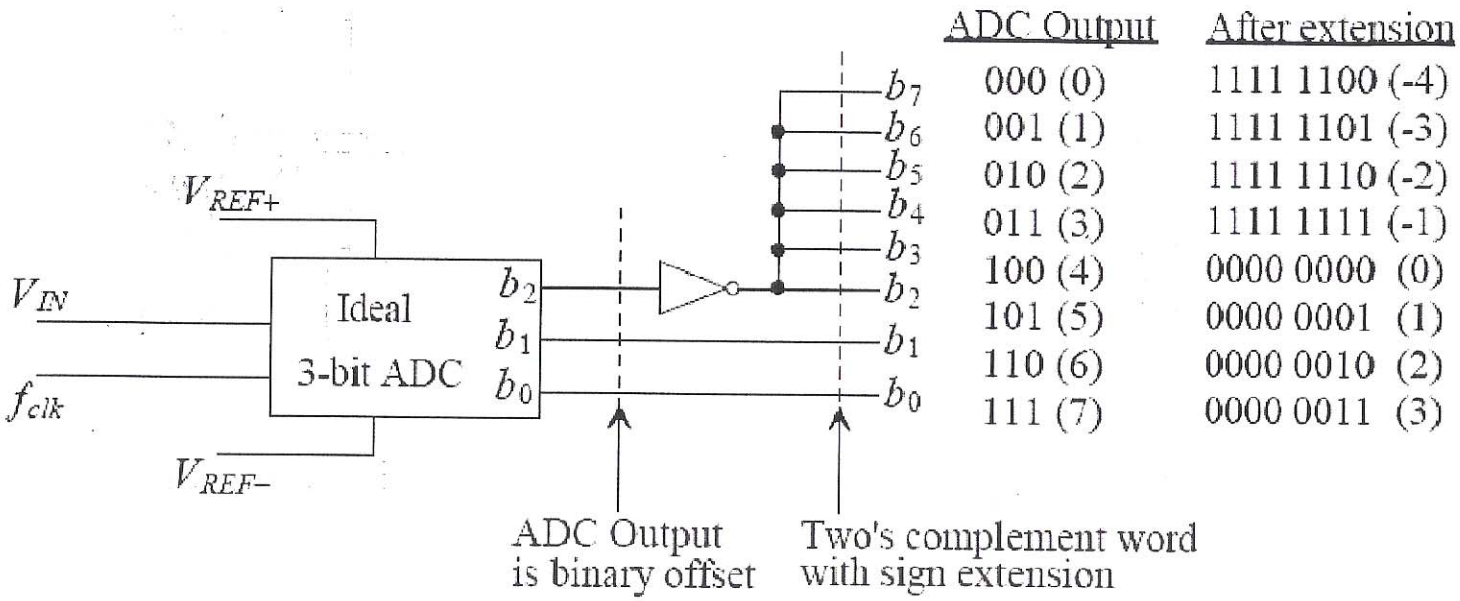
$\frac{1}{2}$ $b_2 \to 1$

$b_1 - 0$ $b_0 \to 0$

$(.6 - \frac{1}{2}) \times 2 = 200mV$

400mV

8)



ADC Output	After extension
000 (0)	1111 1100 (-4)
001 (1)	1111 1101 (-3)
010 (2)	1111 1110 (-2)
011 (3)	1111 1111 (-1)
100 (4)	0000 0000 (0)
101 (5)	0000 0001 (1)
110 (6)	0000 0010 (2)
111 (7)	0000 0011 (3)

Figure 4.6 Showing how to change the output of an ADC to two's complement and how to extend the sign bit.

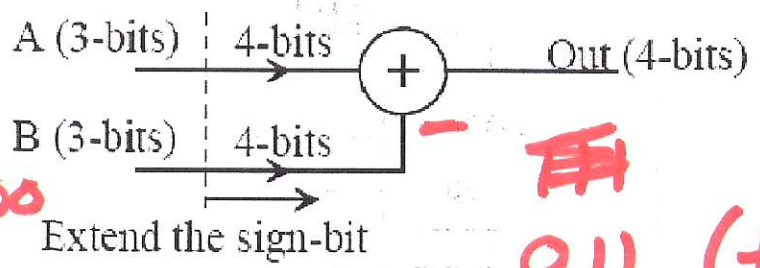
1 → 01 → 0000 0001 (+1)

0 → 11 → 1111 1111 (-1)

offset binary

2-bit two's complement

9)

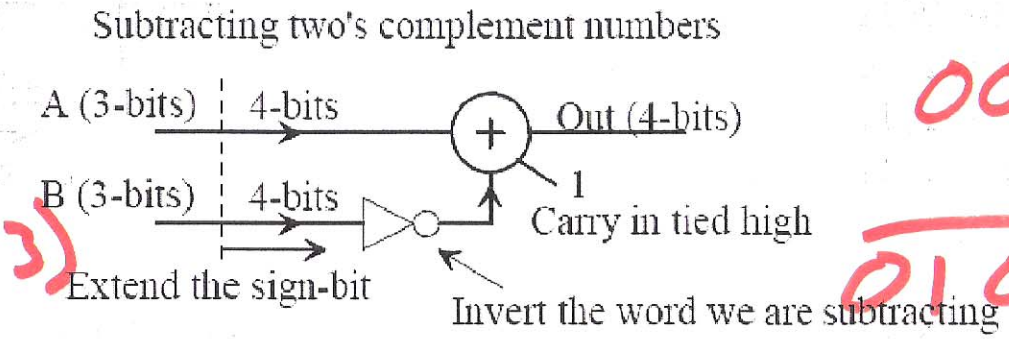


A	B	Out (A+B)
0011 (+3)	0011 (+3)	0110 (+6)
1100 (-4)	1100 (-4)	1000 (-8) OF!
1111 (-1)	0001 (+1)	0000 (0) OF!
0011 (+3)	1111 (-1)	0110 (+2) OF!
0001 (+1)	1100 (-4)	1101 (-3)

```
  1100 (-4)          1111 (-1)
+ 1100 (-4)        + 0001 (+1)
-----------        -----------
1 1000 (-8)        1 0000 (0)
```

Overflow (OF!), toss into the bit bucket (ignore).

Figure 4.7 Showing how two's complement numbers are added.



A	B	$\overline{B}+1$	Out (A-B)
0011 (+3)	1100 (-4)	0100 (+4)	0111 (+7)
1100 (-4)	1100 (-4)	0100 (+4)	0000 (0) OF!
1111 (-1)	0001 (+1)	1111 (-1)	1110 (-2) OF!
0011 (+3)	1111 (-1)	0001 (+1)	0100 (+4)
0010 (+2)	0001 (+1)	1111 (-1)	0001 (+1) OF!

Figure 4.8 Showing how two's complement numbers are subtracted.

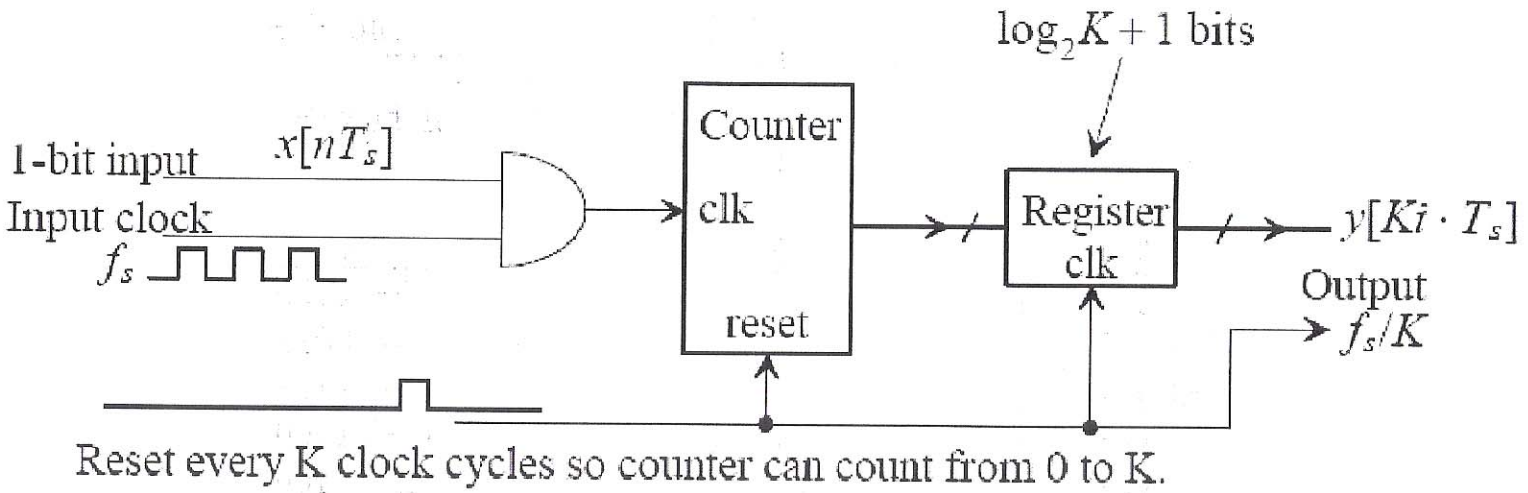


Figure 4.9 Using the counter as a digital filter.

$$Y = \frac{X_1 + X_2 + X_3 + X_4 + \cdots X_N}{N}$$

$$V(z) = \frac{V(z)}{N}\left(1 + z^{-1} + z^{-2} + z^{-3} + \cdots z^{-(N-1)}\right)$$

$$\frac{V(z)}{X(z)} = \frac{1}{N}\,\frac{1 - z^{-N}}{1 - z^{-1}}$$

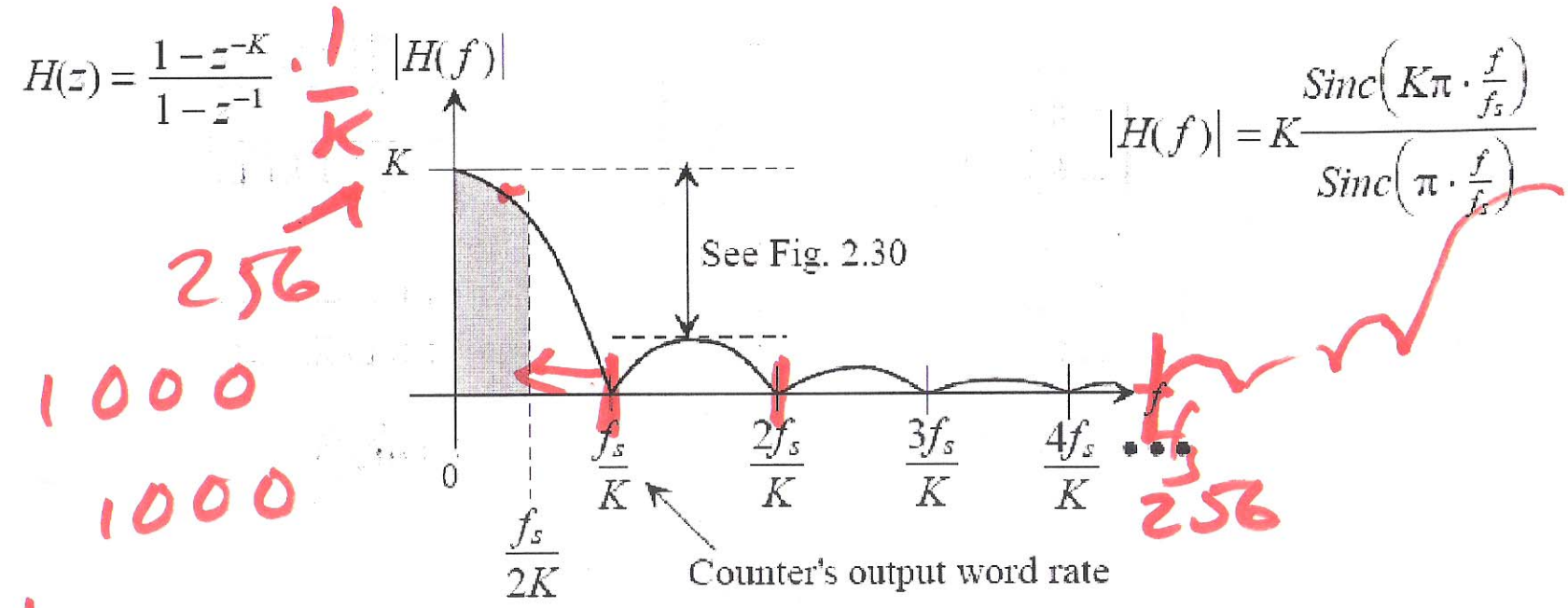


Figure 4.10 Frequency response of a Sinc-shaped digital filter.

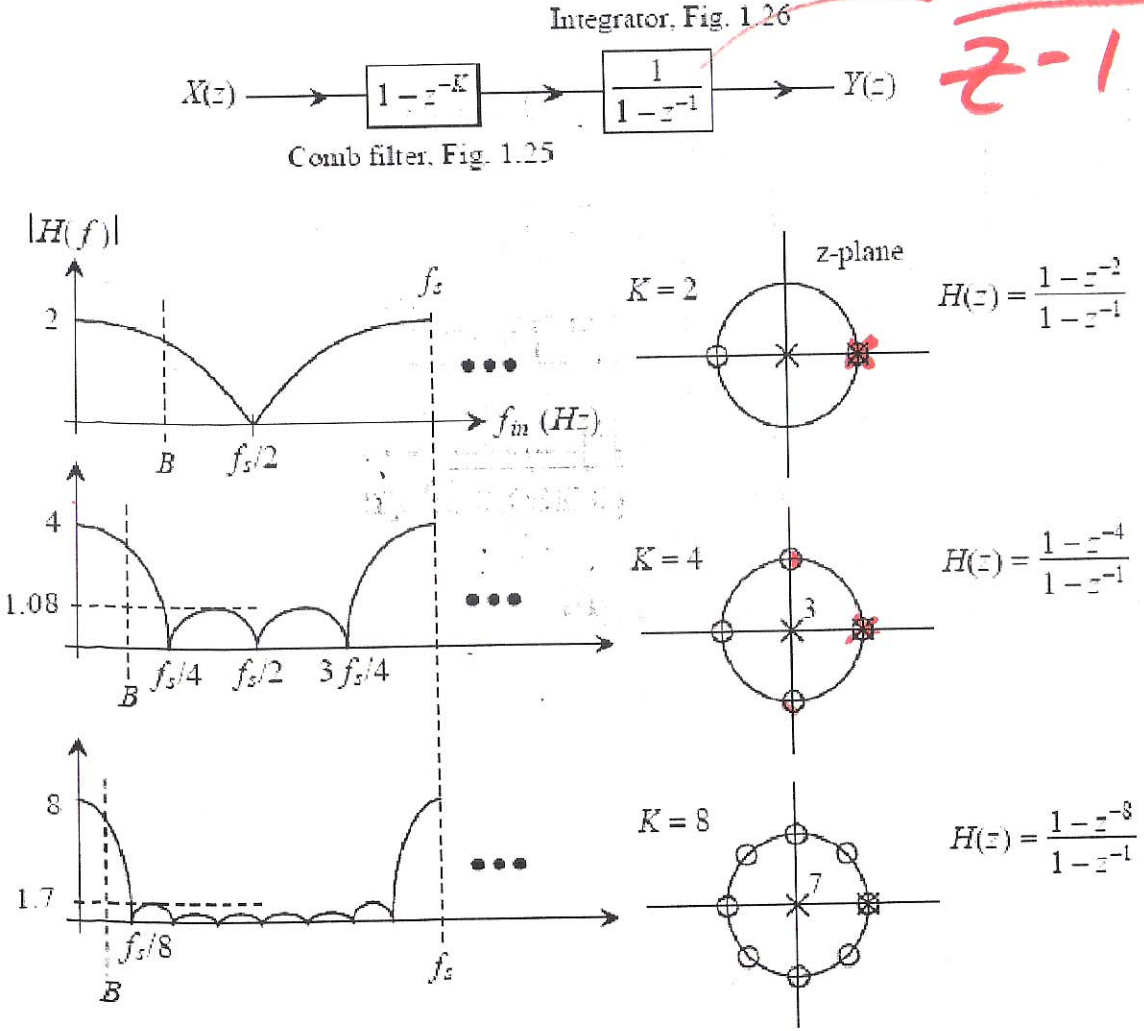


Figure 4.13 Lowpass Sinc-response filters with varying values of K.