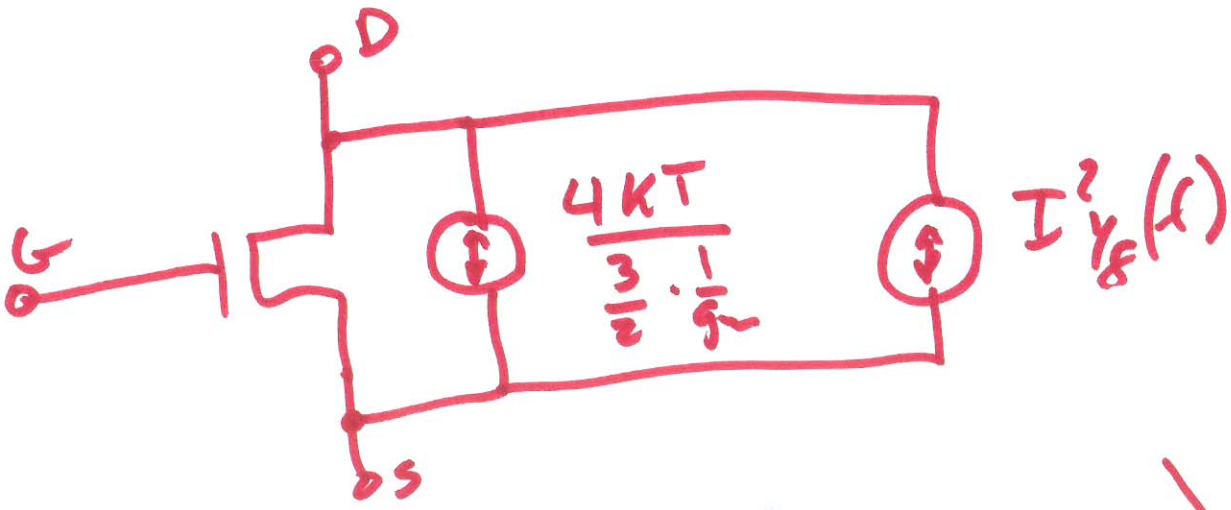
MOSFET Noise Modeling



(6.46) $$Q_I' = \frac{2}{3} C_{ox}' \left(V_{GS} - V_{THN}\right)$$

6.27 $$dR = \frac{1}{\mu_N Q_I'(Y)} \cdot \frac{dY}{W}$$

$$R = \int_0^L \frac{1}{\mu_N \cdot \frac{2}{3} C_{ox}' \left(V_{GS} - V_{THN}\right) \cdot W} \cdot dY$$

1)

$$R = \frac{1}{\frac{2}{3}\underbrace{\mu_N C'_{ox}}_{KP_N}(V_{GS}-V_{THN})\cdot W} \cdot L$$

$$g = KP_N \cdot \frac{W}{L}(V_{GS} - V_{THN})$$

$$R = \frac{3}{2}\cdot\frac{1}{g_m}$$

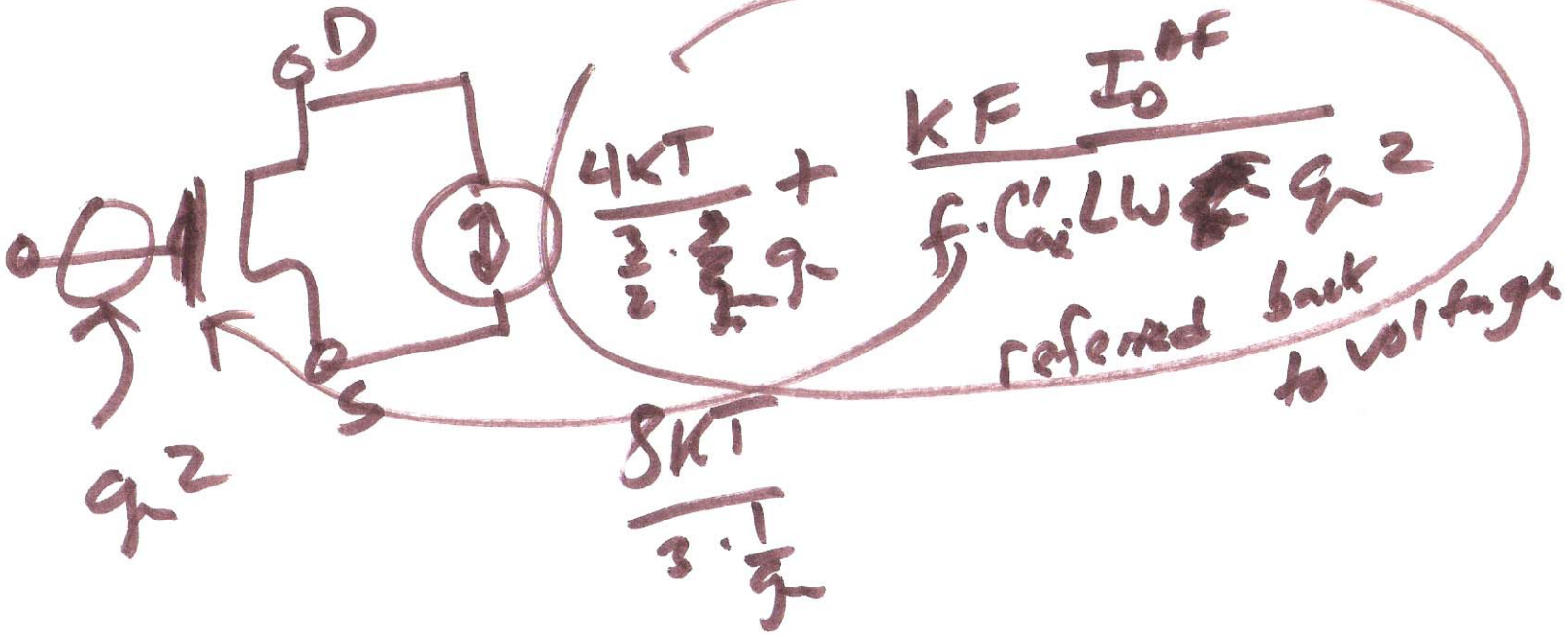
NLEV = 0

$$I^2_{1/f}(f) = \frac{KF \cdot I_D^{AF}}{f(C'_{ox}\cdot L)^2}$$

NLEV = 1

$$I^2_{1/f}(f) = \frac{KF \cdot I_D^{AF}}{f \cdot C'_{ox} \cdot L \cdot W}$$

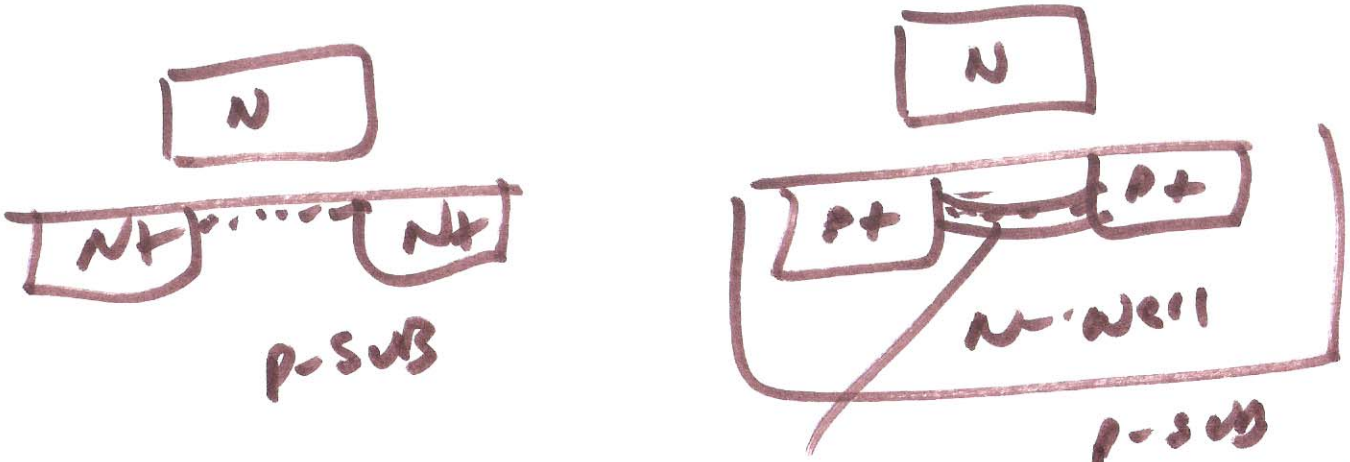
Bigger Area
less 1/f NOISE



3)

Low Noise pmos or NMOS

IN 0.35 μm And older technologies



buried channel

pmos is better in older CMOS

Newer CMOS
0.25μm And newer
dual work function gates
So both devices, NMOS
&
PMOS,
Are surface devices
So it depends on technology
but generally NMOS is
better
because
bigger!

16:06