Backend of the line (BEOL)

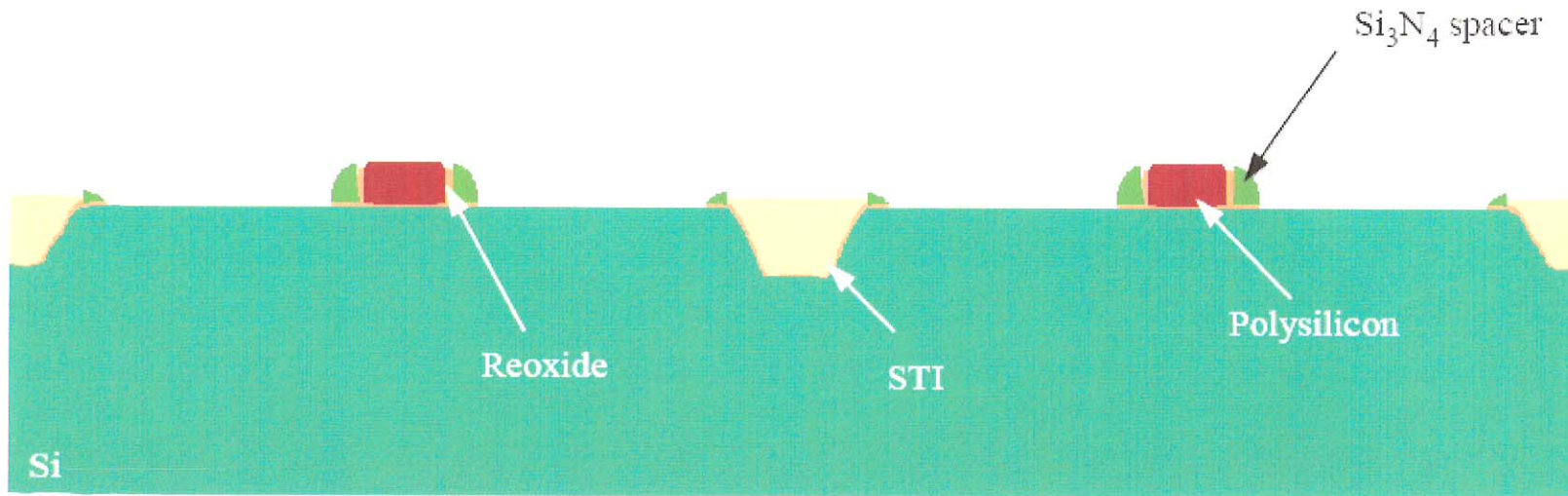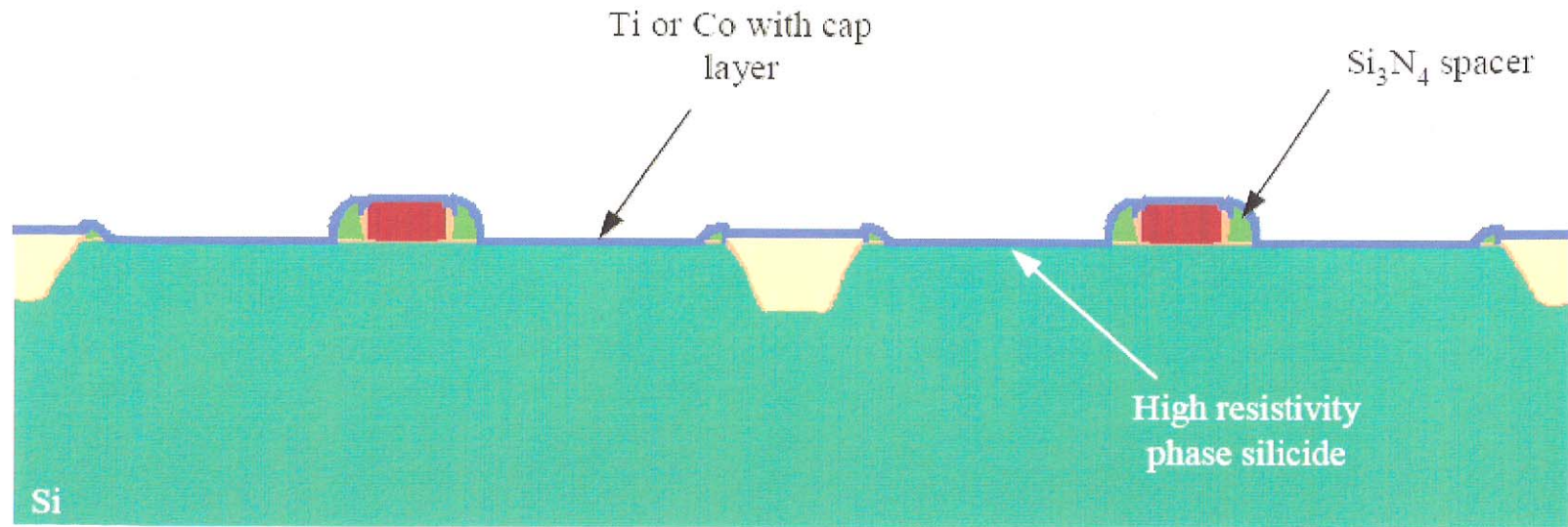
Si₃N₄ spacer

Reoxide

STI

Polysilicon

Si

Figure 7.61 Removal of the exposed reoxide (present from the FEOL) using buffered-*HF*.

Ti or Co with cap layer

Si$_3$N$_4$ spacer

High resistivity phase silicide

Si

Figure 7.62 Titanium or cobalt deposited by PVD followed by the first salicide rapid thermal anneal.

Unreacted Ti or
Co and cap layer

Polycide

Si₃N₄ spacer

Low resistivity
phase silicide

Si
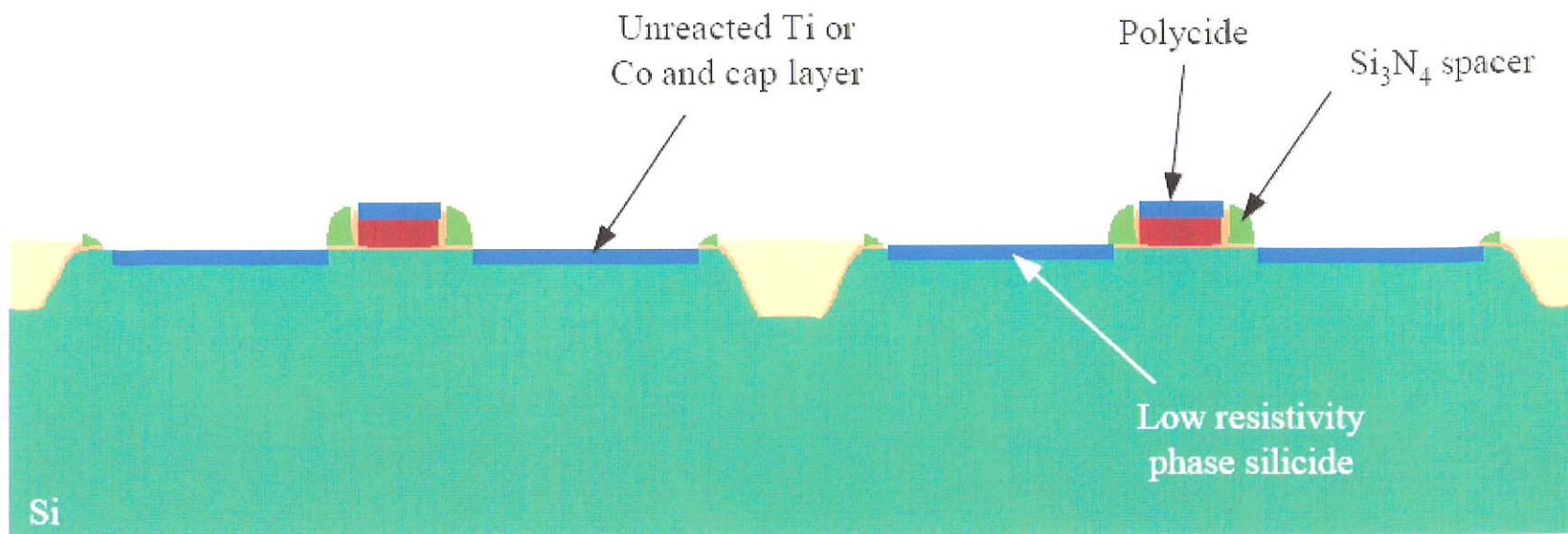
Figure 7.63 Wet chemical etch of the unreacted titanium or cobalt followed by the second salicide rapid thermal anneal.

PMD

STI

Etch stop layer

Si
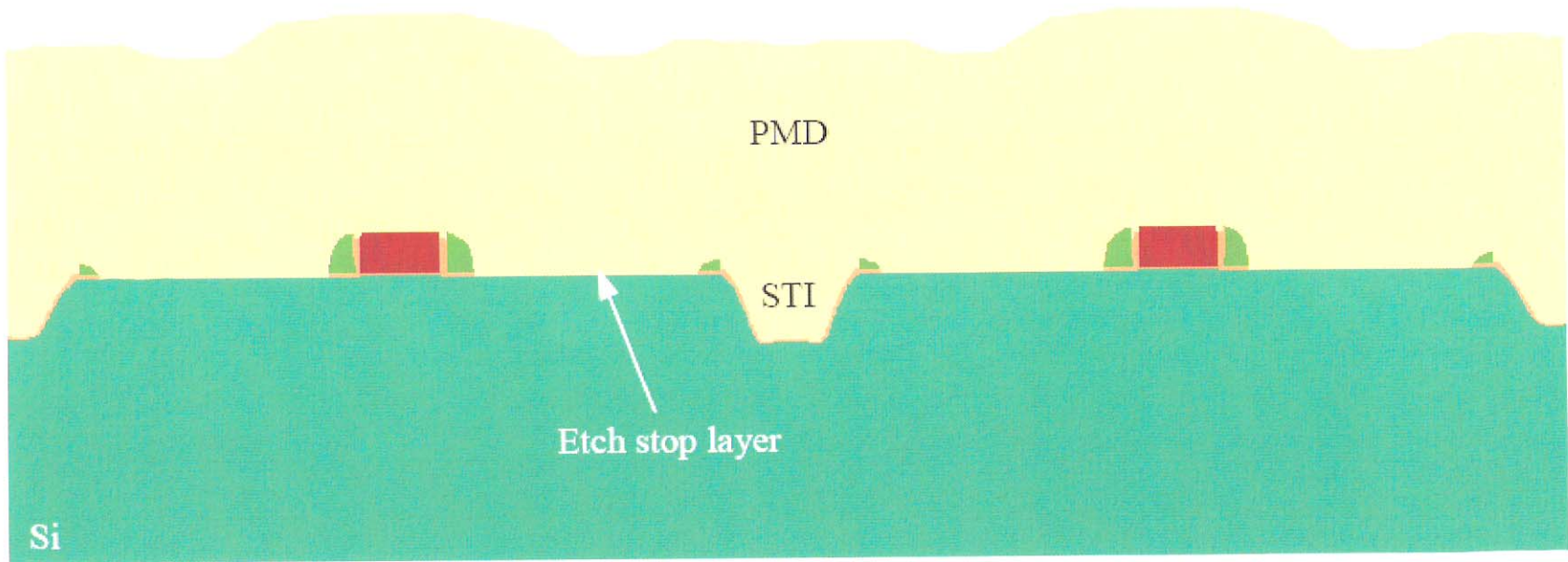
Figure 7.64 Pre-metal dielectric (PMD) deposition using high density plasma
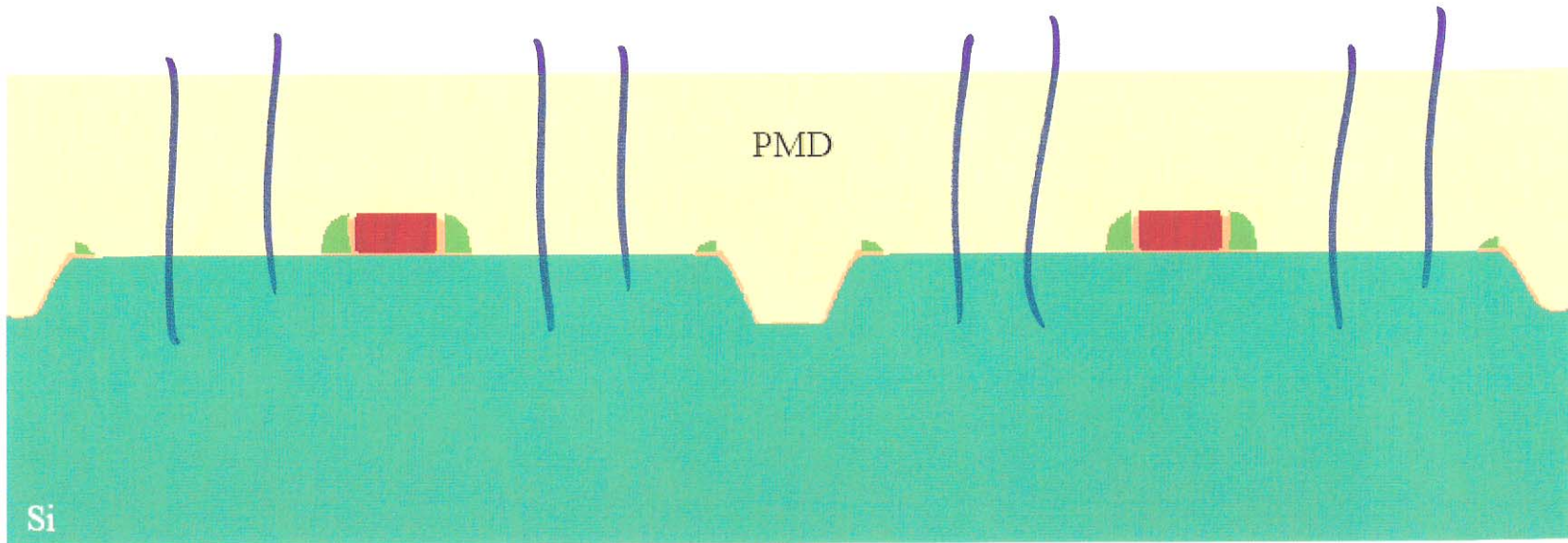
Figure 7.65 Planarizing of the PMD using CMP.

Layout view (mask layer 7)

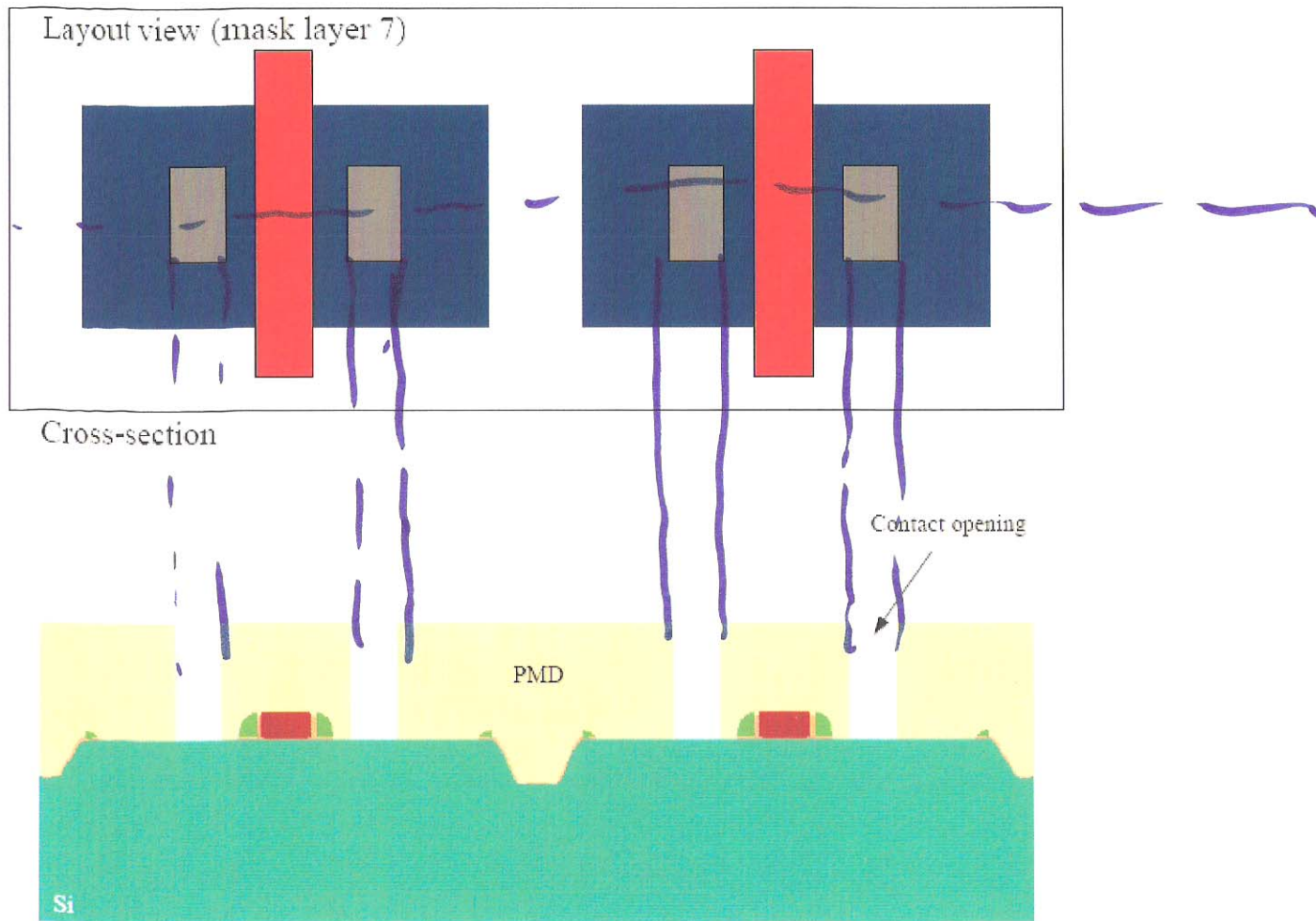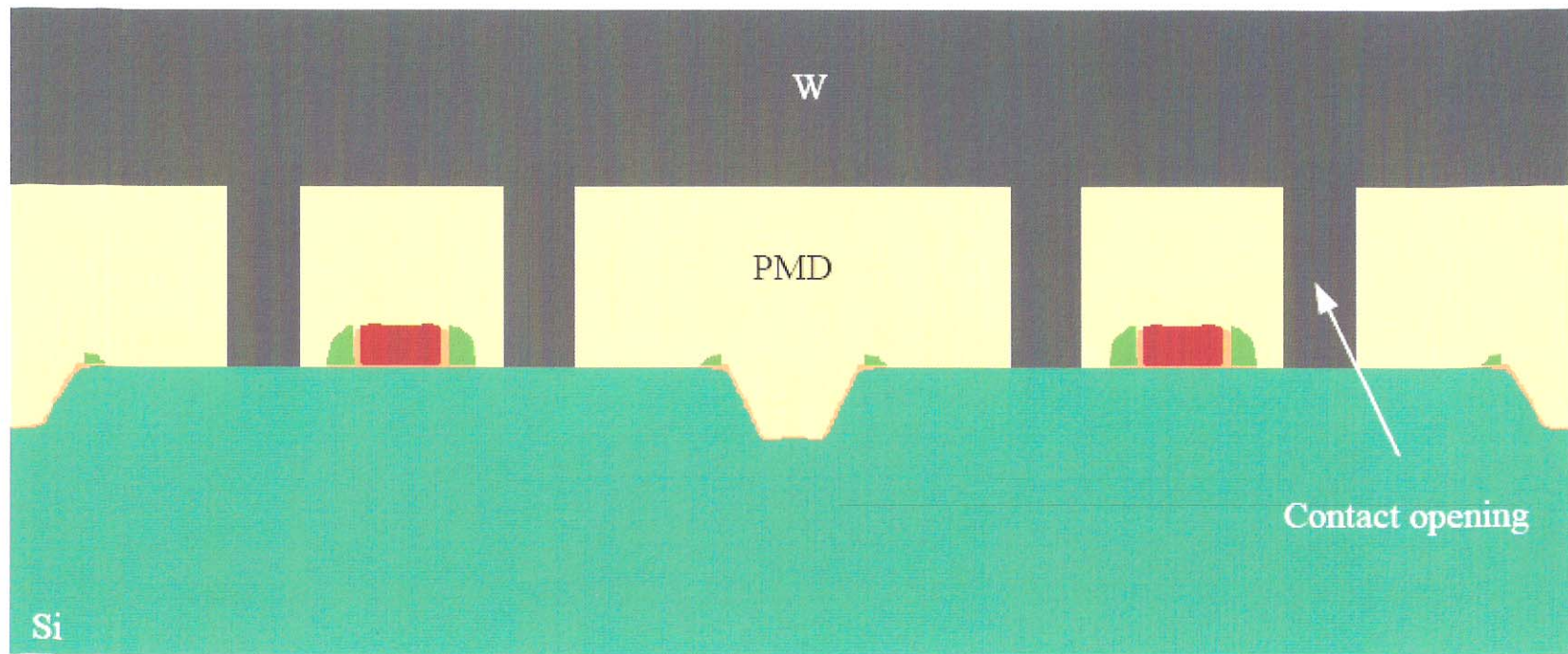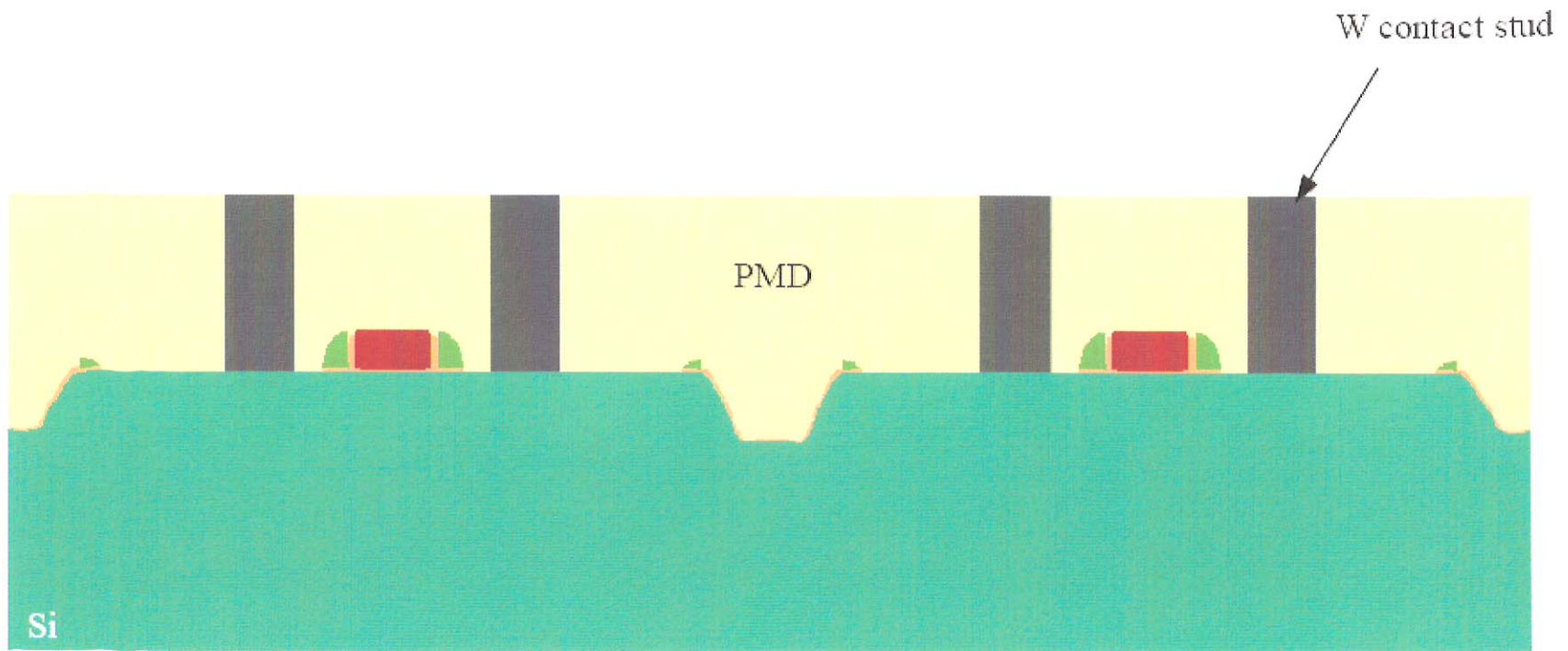Cross-section

Contact opening

PMD

Si

Figure 7.66 Contact definition using photolithography and reactive ion etching of the PMD. Notice the contacts to the poly are formed at the same time but not shown.

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Figure 7.67 *Ti/TiN* liner deposition using IMP and CVD. respectively. *W* contact fill deposition using WF_6 CVD.

W contact stud

PMD

Si

Figure 7.68 *W* CMP to form defined contacts.

Recess

Contact to
polysilicon

PMD

Contact to silicon

Recessed W
contact stud

PMD

Si
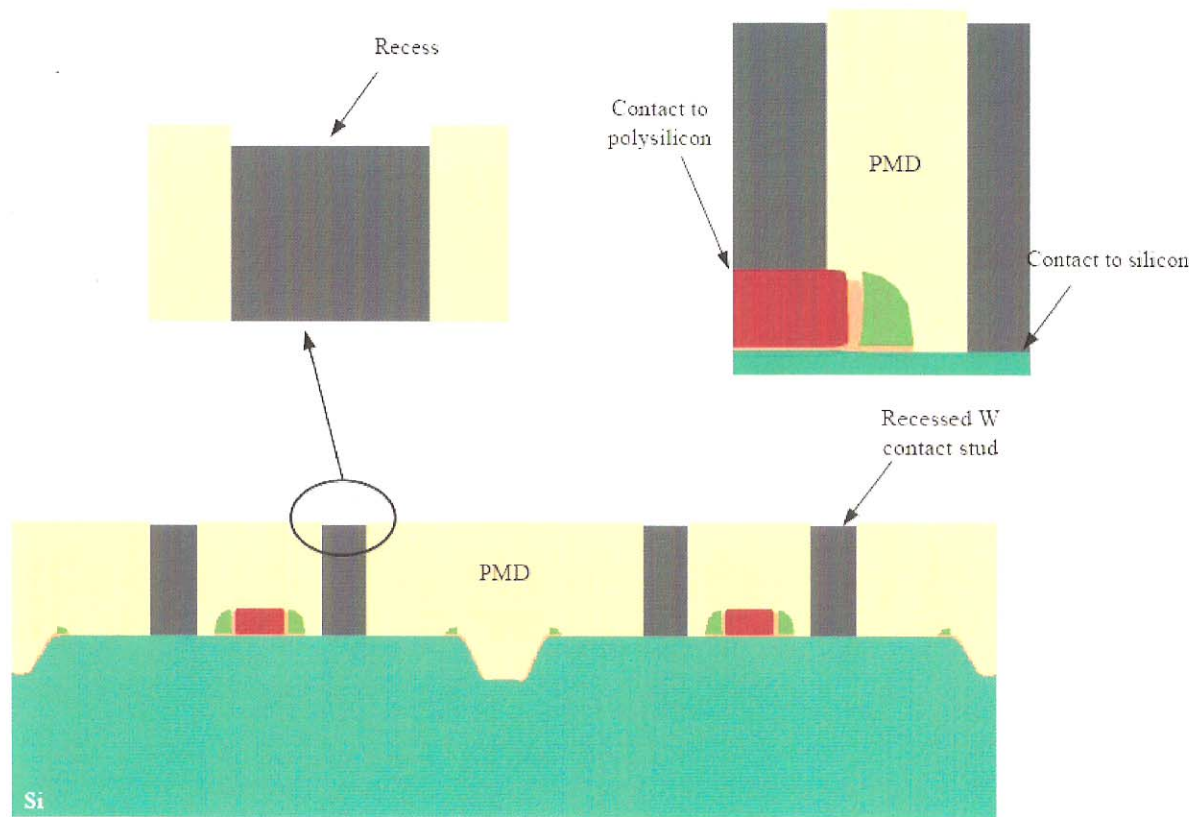
Figure 7.69 W recess etch using "buff" polish or dry W etch.

Ti/TiN/AlCu/TiN
(metal1)

PMD

Recessed W
contact stud

Si
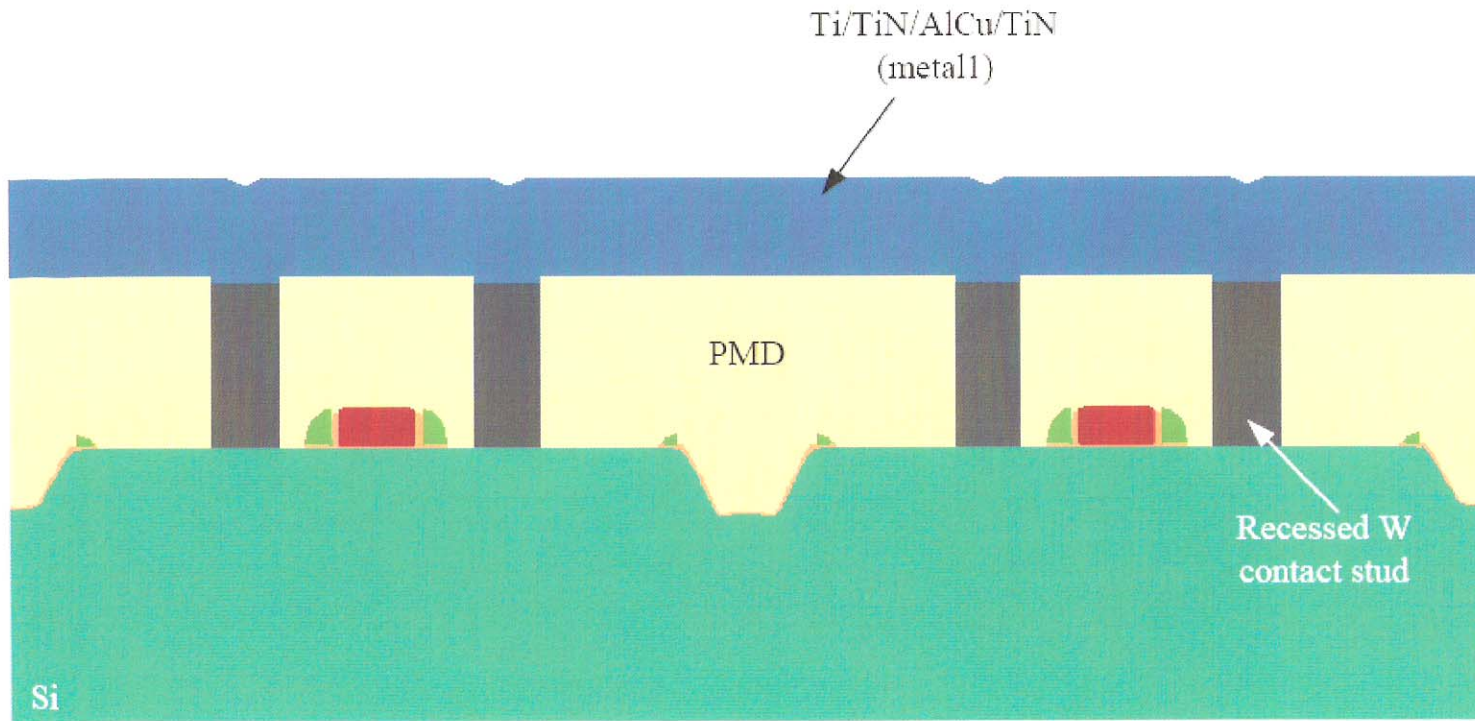
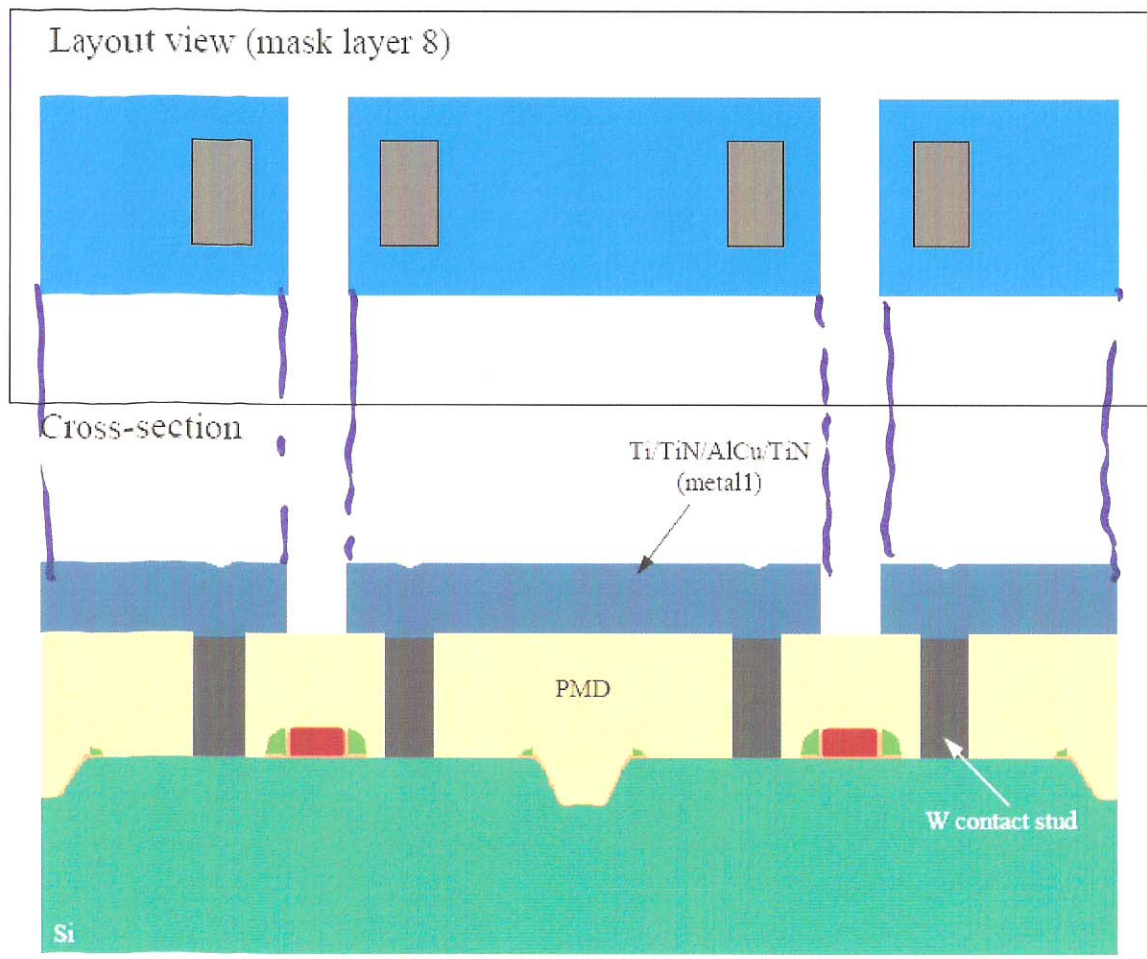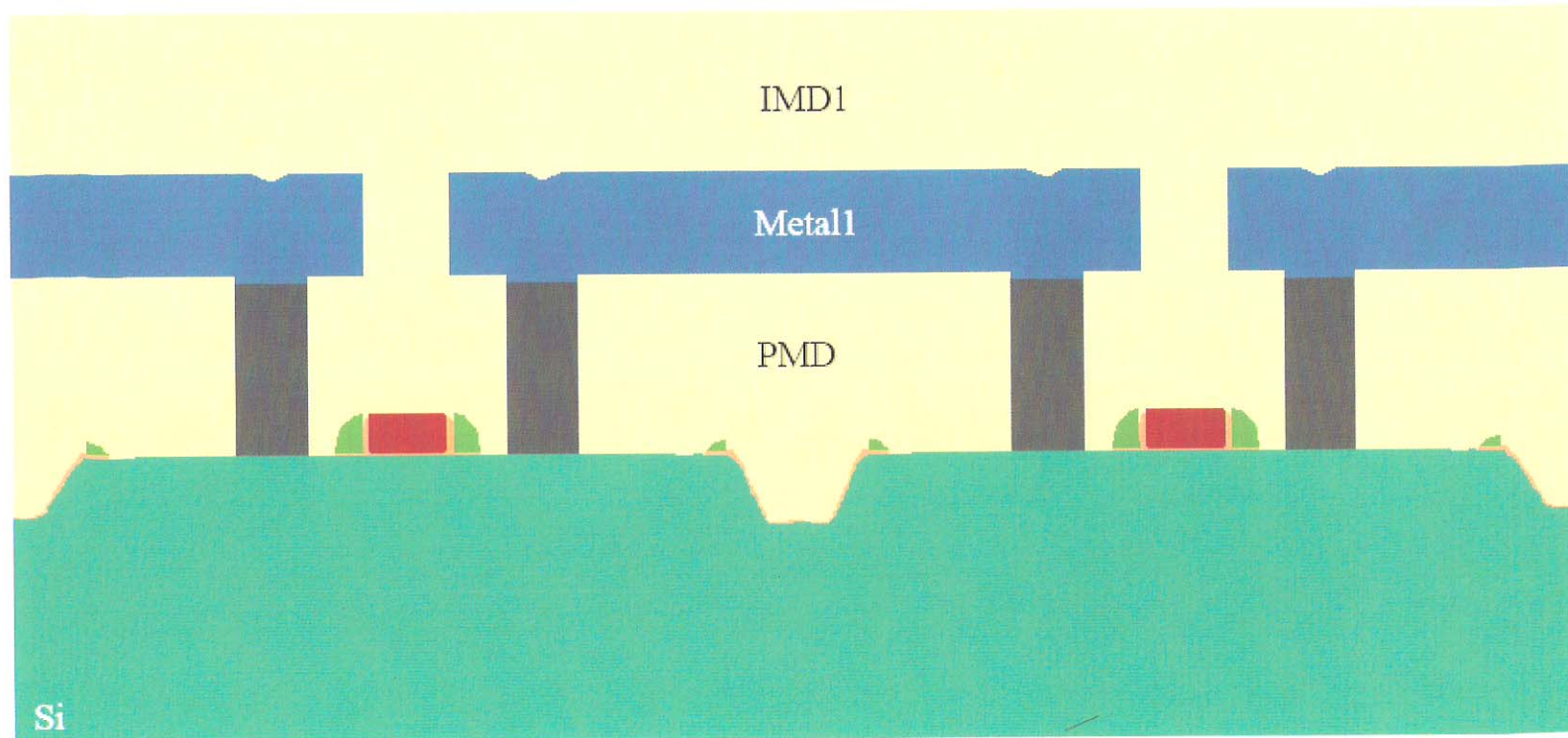**Figure 7.70** Metal1 stack deposition using
PVD.

Figure 7.71 Metal1 definition using photolithography and dry metal etch.

Figure 7.72 Intra-metal dielectric 1 (IMD1) deposition using HDP CVD. This is followed by IMD1 planarization using CMP.
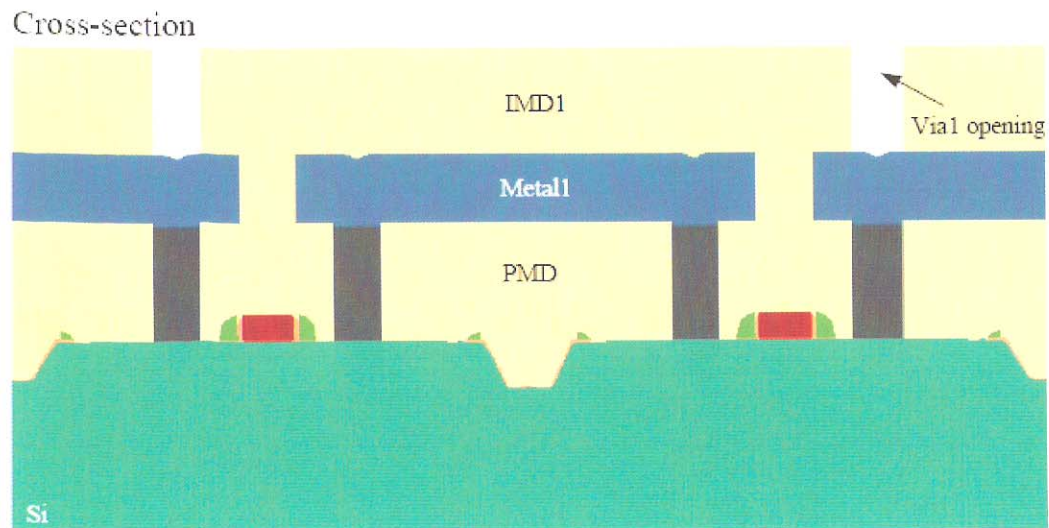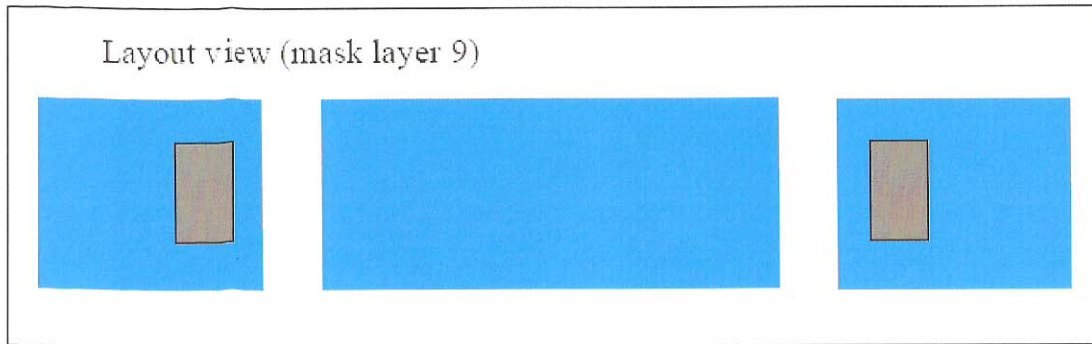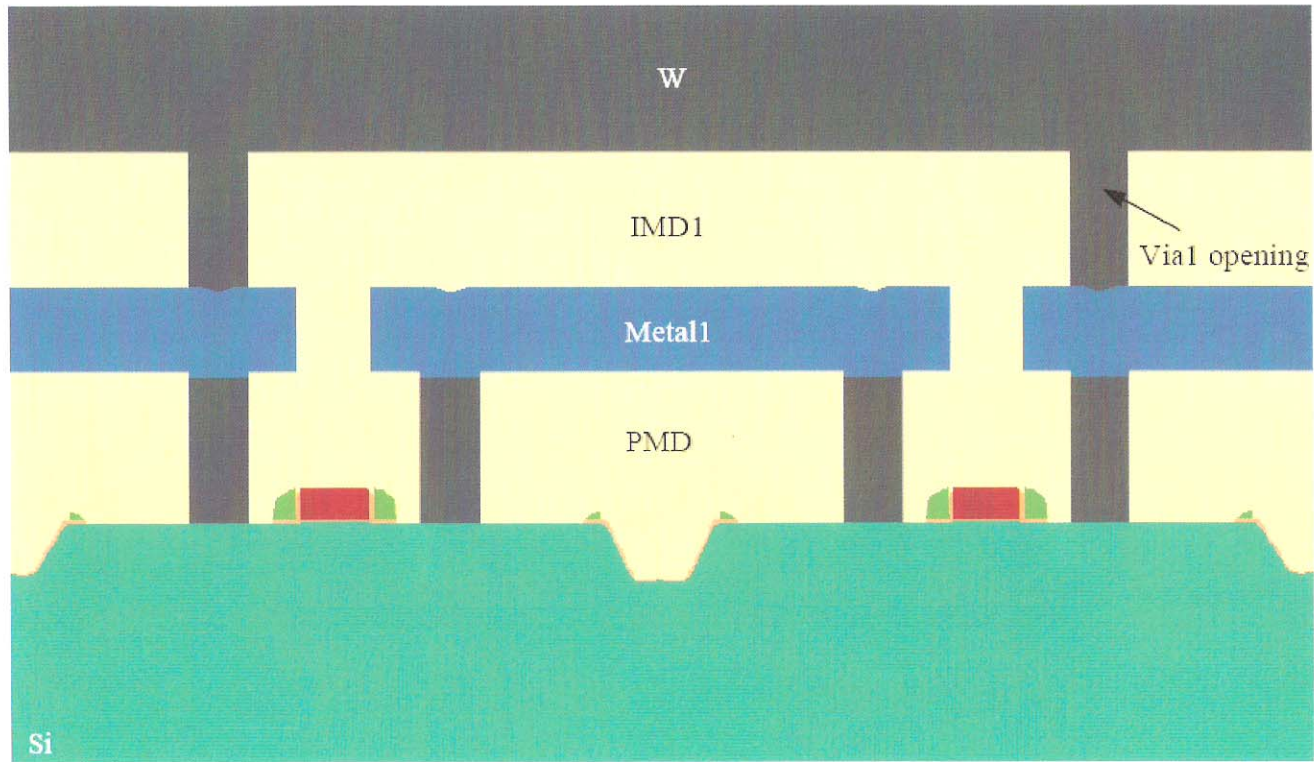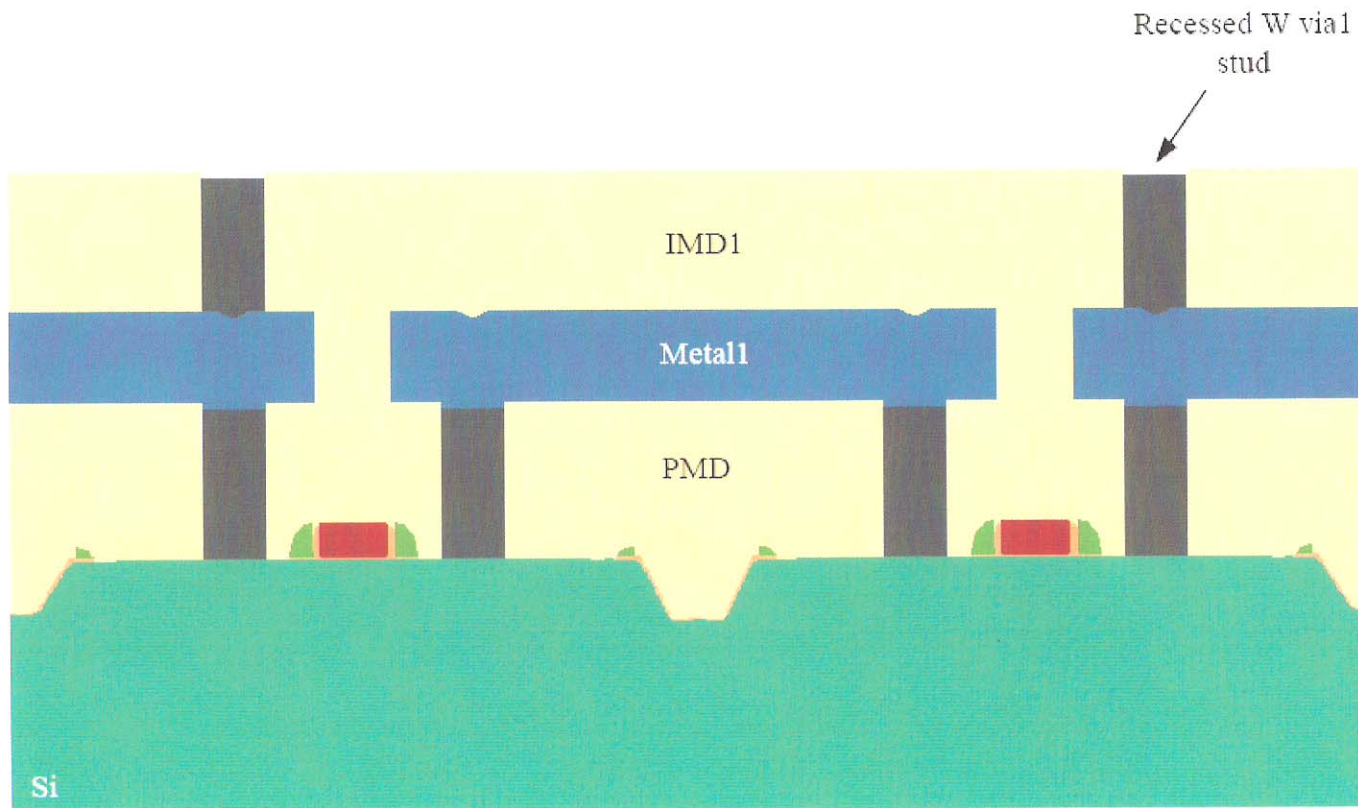
Layout view (mask layer 9)

Cross-section

IMD1

Metal1

Via1 opening

PMD

Si

Figure 7.73 Via1 definition using photolithography and dry IMD1 etch.

Figure 7.74 *Ti/TiN* liner deposition using IMP and CVD. respectively. *W* via1 fill deposition using WF_6 CVD.

14)

Figure 7.75 *W* CMP to form defined vias. This is followed by *W* recess etch using "buff" polish or dry *W* etch.
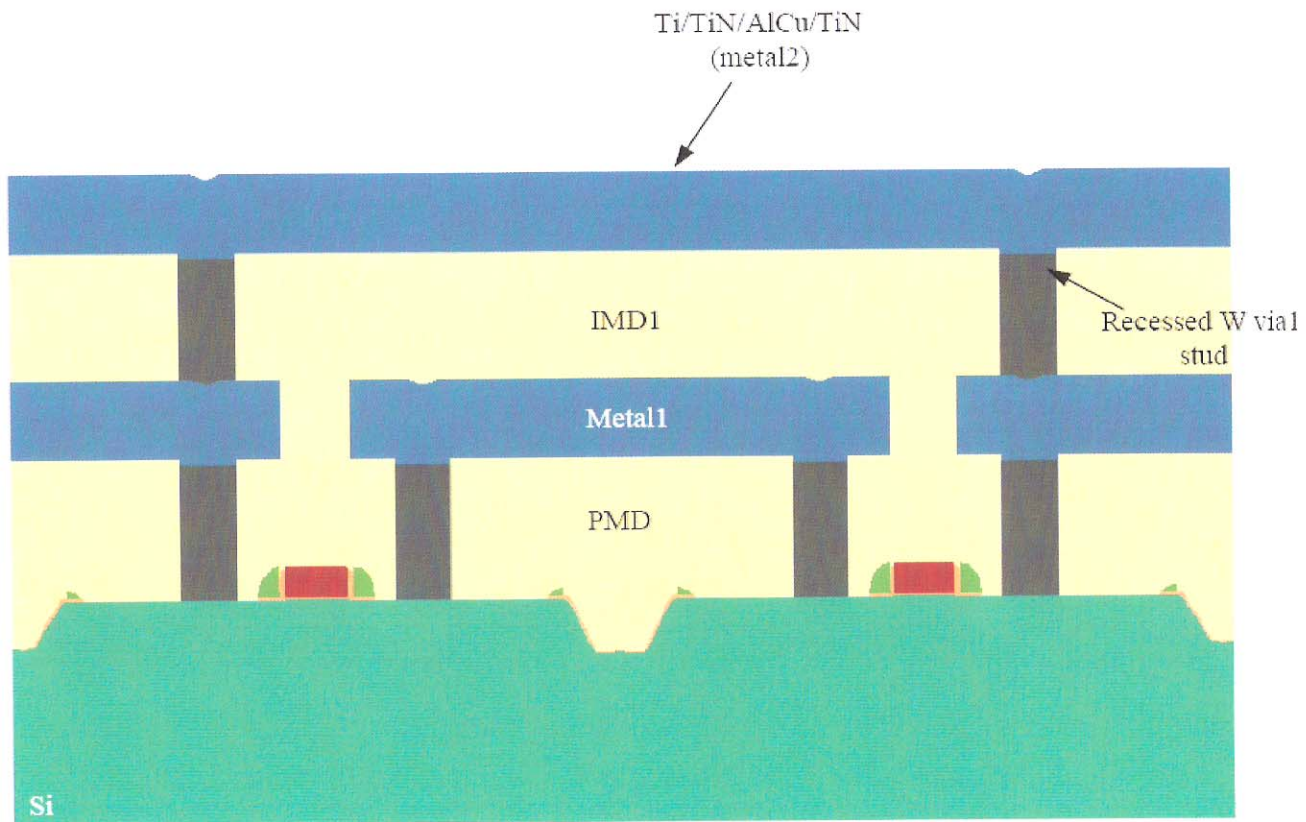
Ti/TiN/AlCu/TiN
(metal2)

IMD1

Recessed W via1
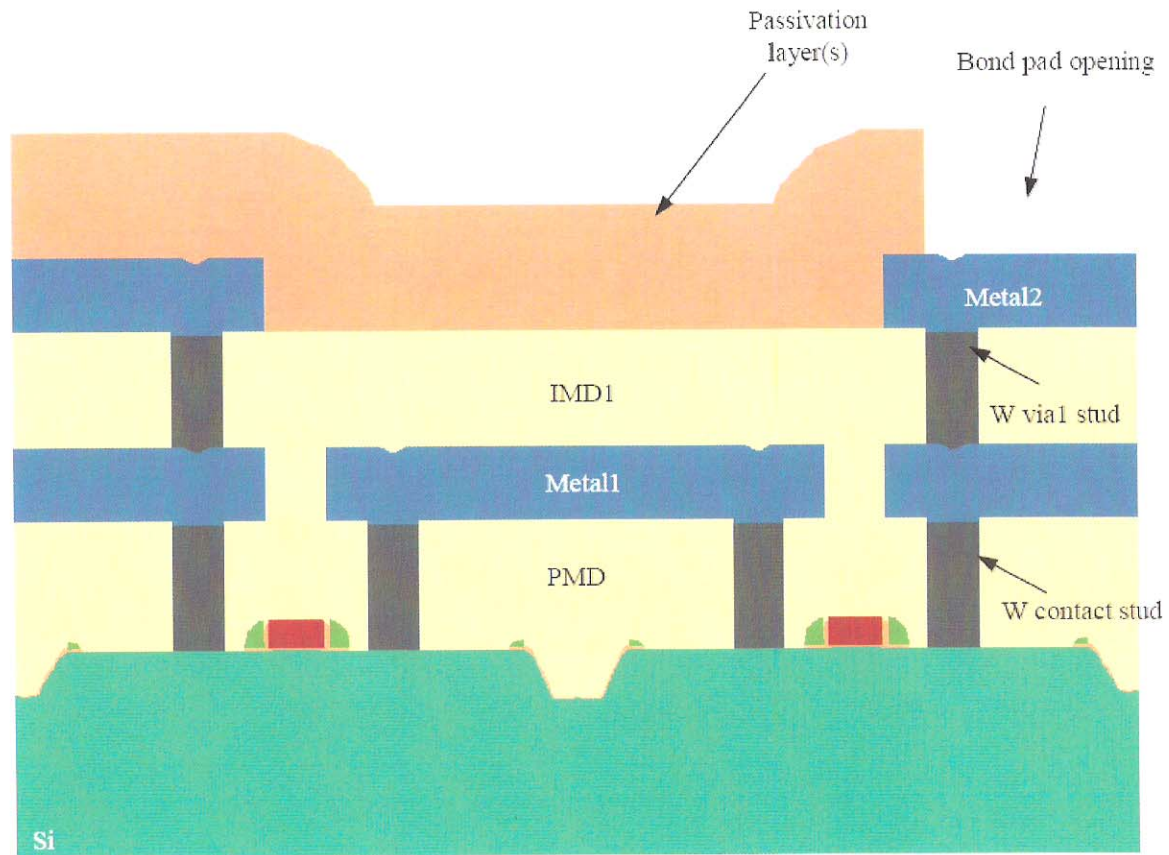stud

Metal1

PMD

Si

Figure 7.76 Metal2 stack deposition using PVD.

Layout view (mask layer 10)

Ti/TiN/AlCu/TiN
(metal2)

IMD1

W via1 stud

Metal1

PMD

W contact stud

Si
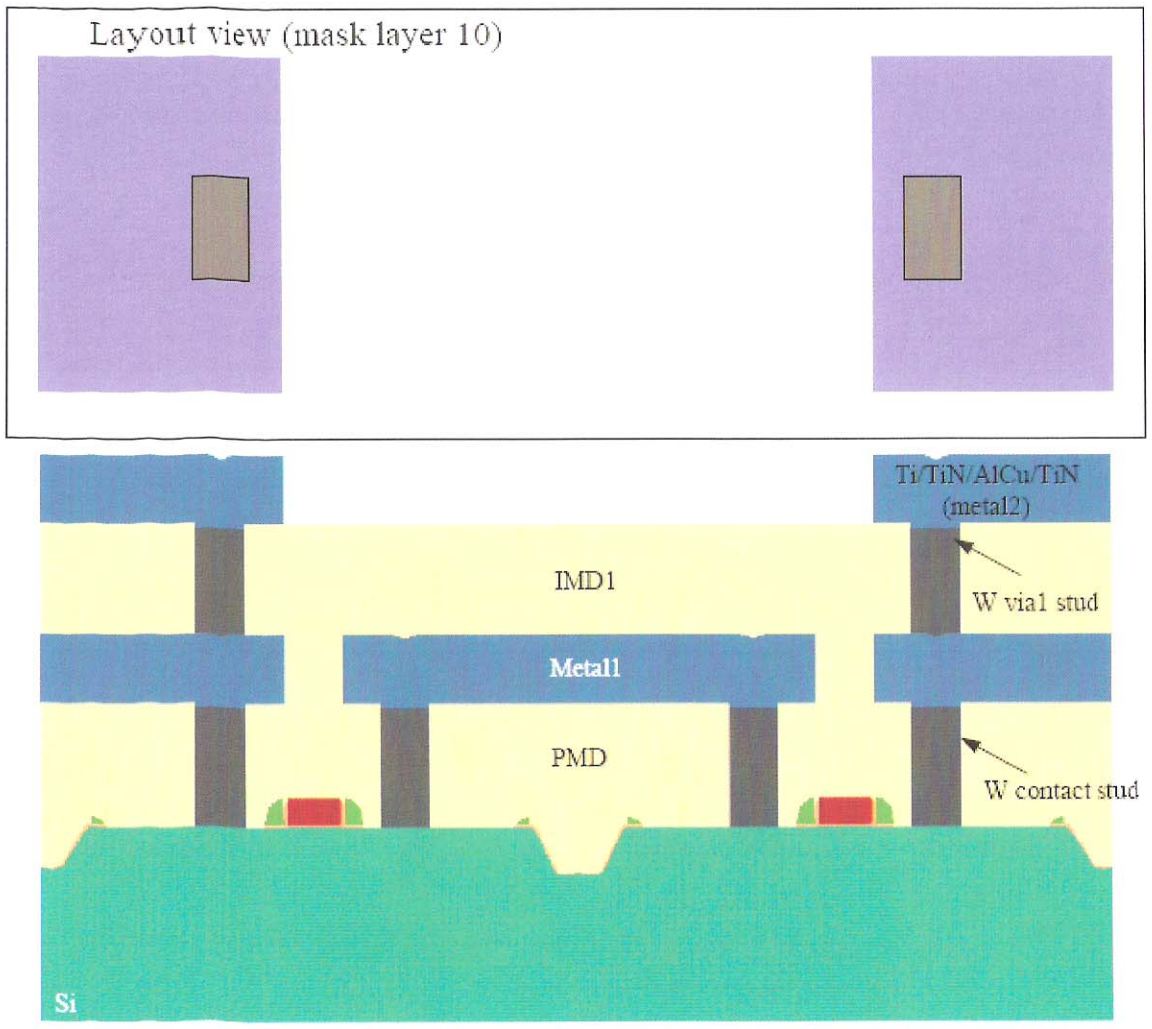
Figure 7.77 Metal2 definition using photolithography and dry metal

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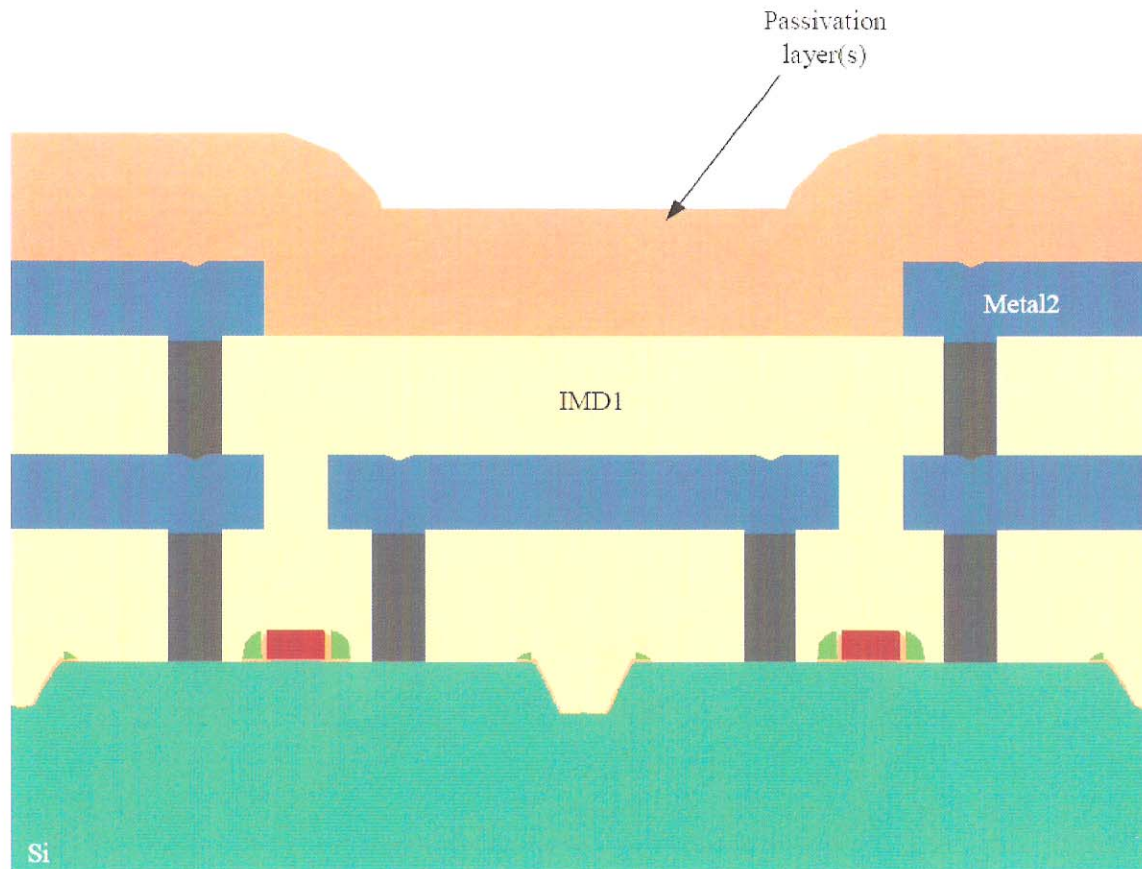
Figure 7.78 Deposition of final passivation.

Figure 7.79 Bond pad definition using photolithography and dry etch of passivation.