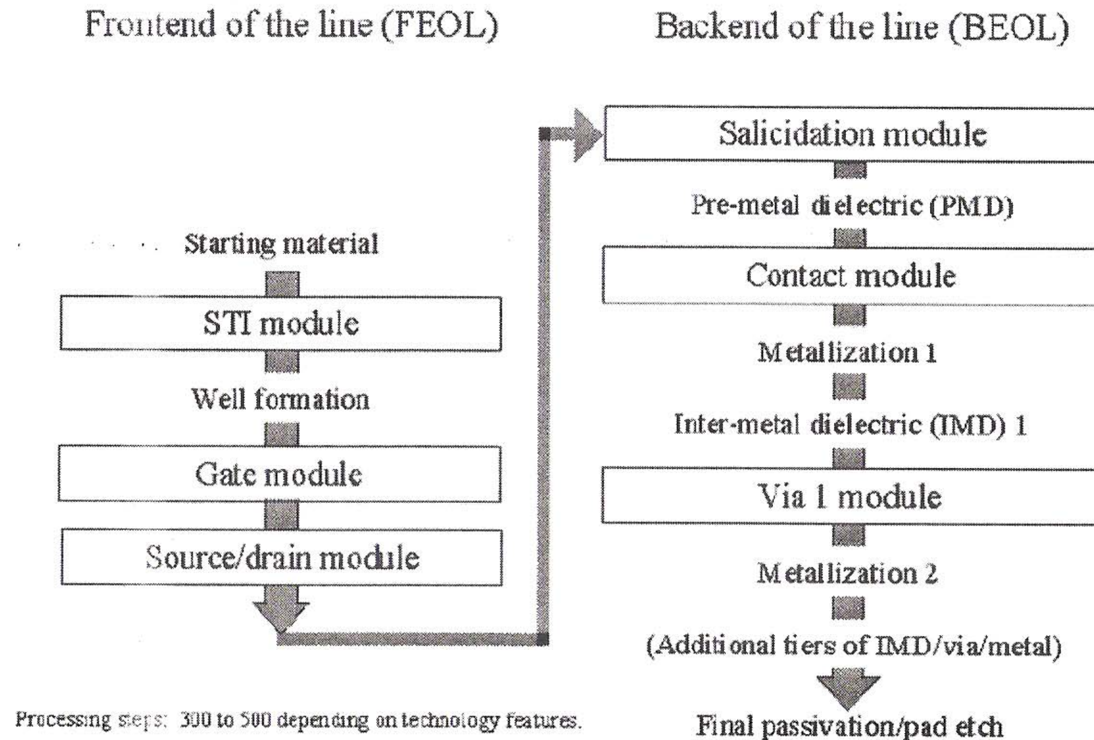

Figure 7.25 A typical CMOS process flow illustrating the difference between FEOL and BEOL processes.

FRONT END of the Line (FEOL)

* shallow trench Isolation (STI)
* Twin-tubs (twin wells)
* single level poly silicon
* Low-doped drain extensions

1)

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Backend of the line (BEOL)

* fully planarized dielectrics
* planarized tungsten contacts and via plugs
* Aluminum metallization

In the following we want describe

* wafer cleaning
* individual photolithographic steps
* Back side film removal after CVD
* metrology to measure thickness, critical dimensions, etc.

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Table 7.1 Masks used in our generic CMOS process.

Layer name	Mask	Aligns to level	Times used	Purpose
1 (active)	Clear	aligns to notch	1	Defines active areas
2 (p-well)	Clear	1	2	Defines NMOS sidewall implants and p-well
3 (n-well)	Dark	1	2	Defines PMOS sidewall implants and n-well
4 (poly1)	Clear	1	1	Defines polysilicon
5 (n-select)	Dark	1	2	Defines nLDD and n+
6 (p-select)	Dark	1	2	Defines pLDD and P+
7 (contact)	Dark	4	1	Defines contact to poly and actives areas
8 (metal1)	Clear	7	1	Defines metal1
9 (via1)	Dark	8	1	Defines via1 (connects M1 to M2)
10 (metal2)	Clear	9	1	Defines metal2
passivation	Dark	Top-level metal	1	Defines bond pad opening in passivation

3)

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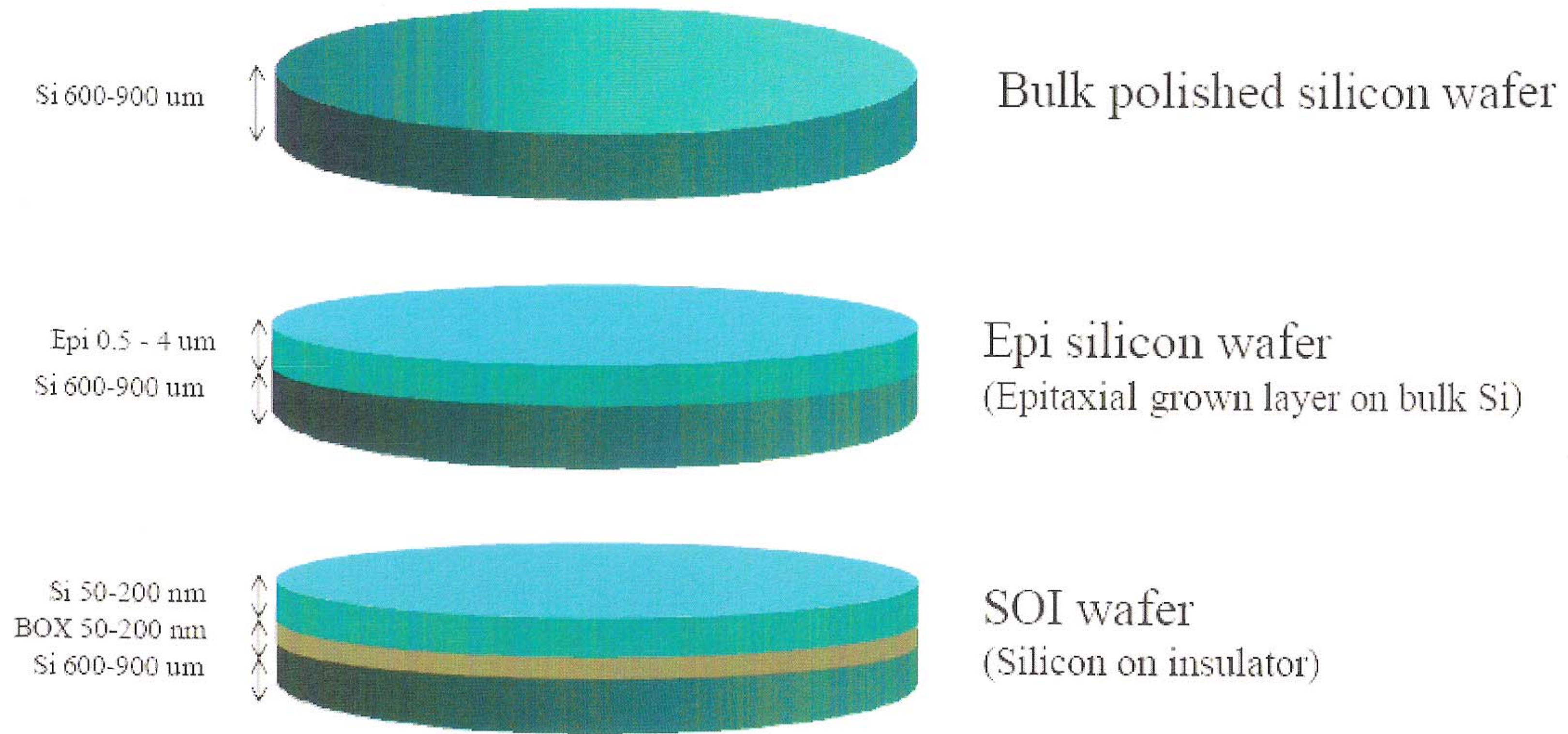

Figure 7.26 The three general types of silicon wafers used for CMOS fabrication.

4)

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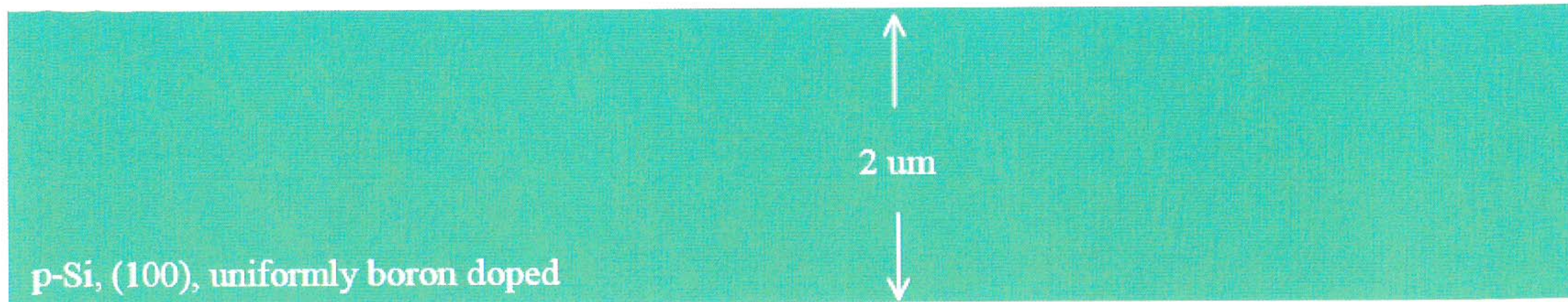

Figure 7.27 Simulated cross-sectional view (the top 2 μm) of the bulk wafer in Fig. 7.26.

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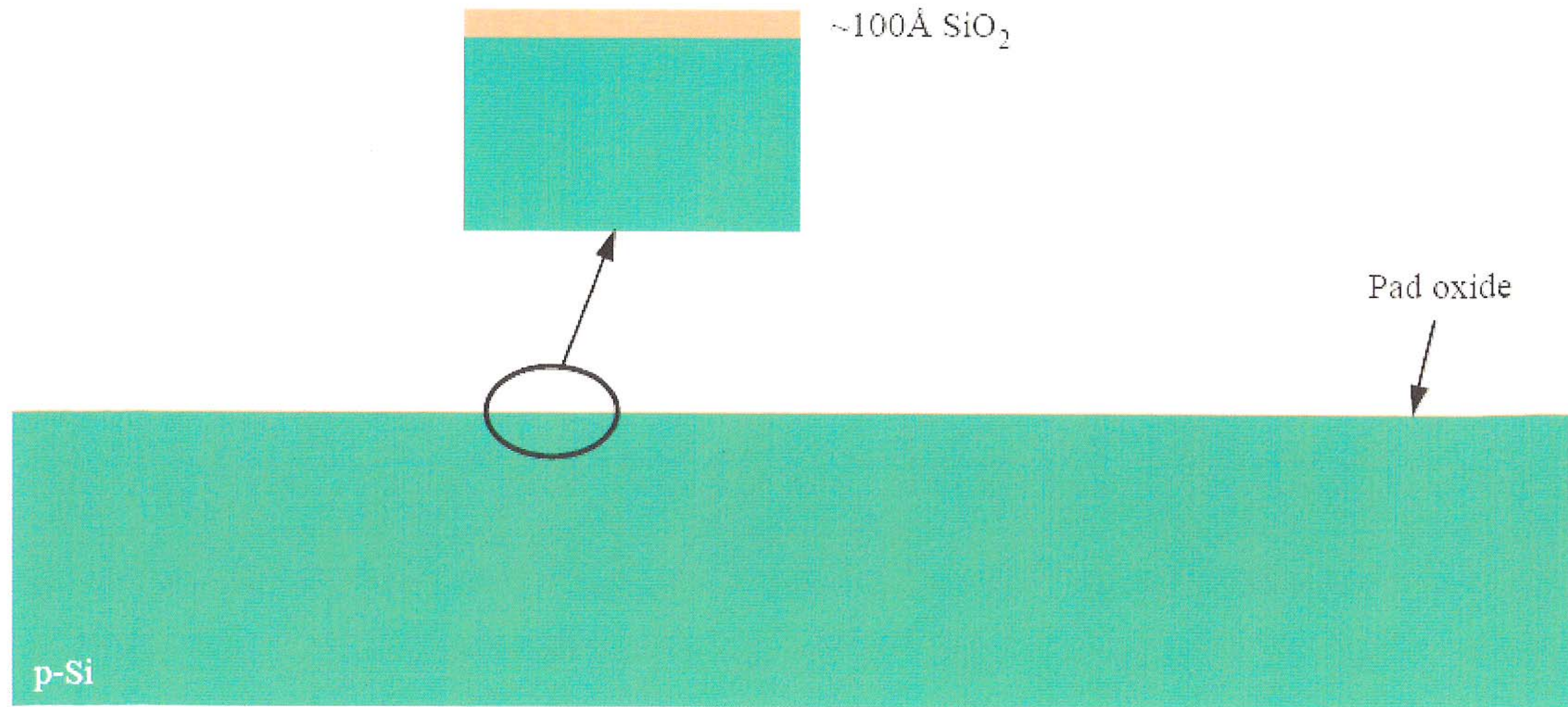
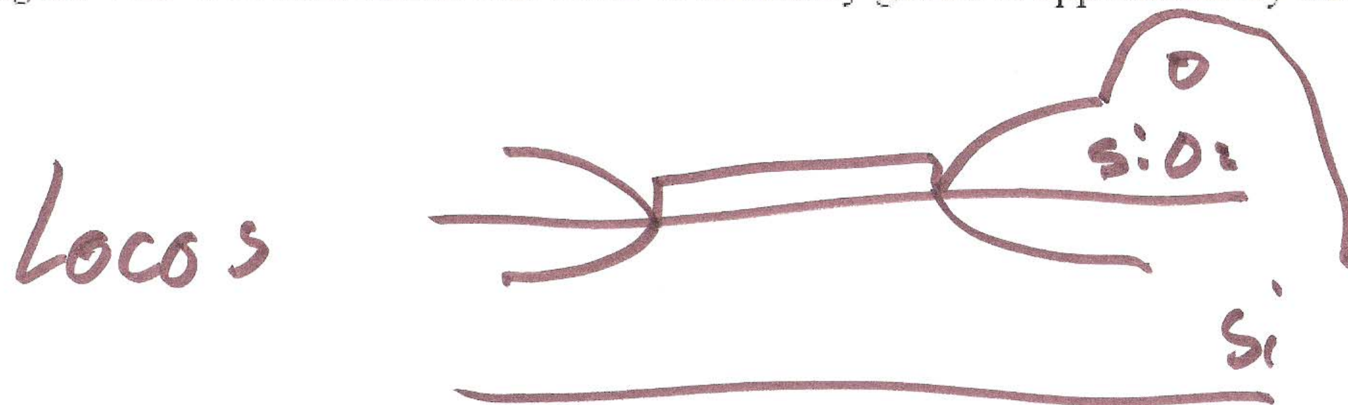


Figure 7.28 STI film stack. The oxide is thermally grown at approximately 900 °C with dry



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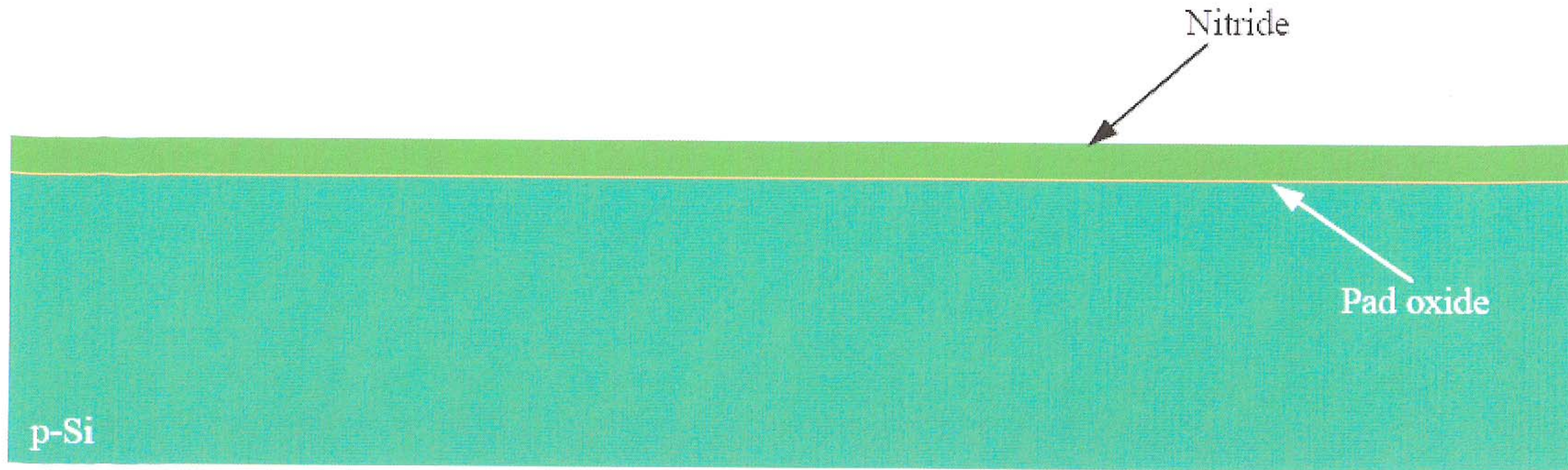
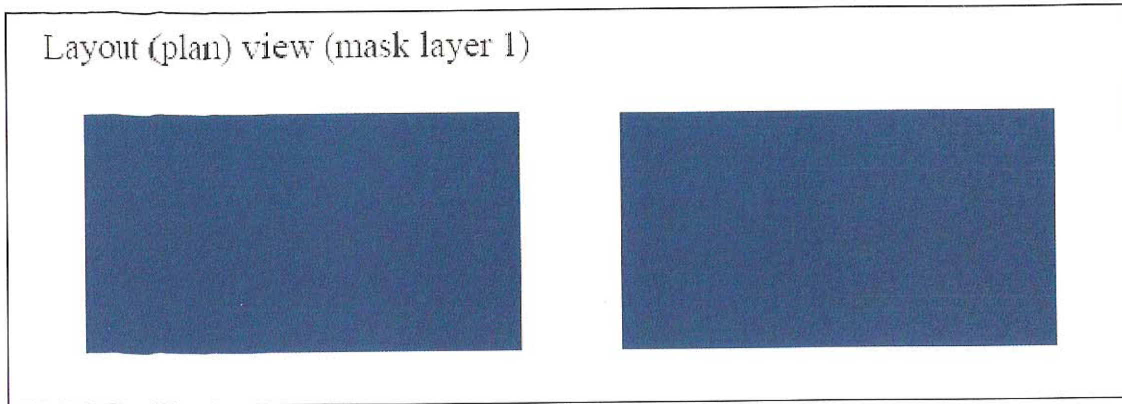


Figure 7.29 STI film stack. Silicon nitride deposited by LPCVD at approximately 800 °C.



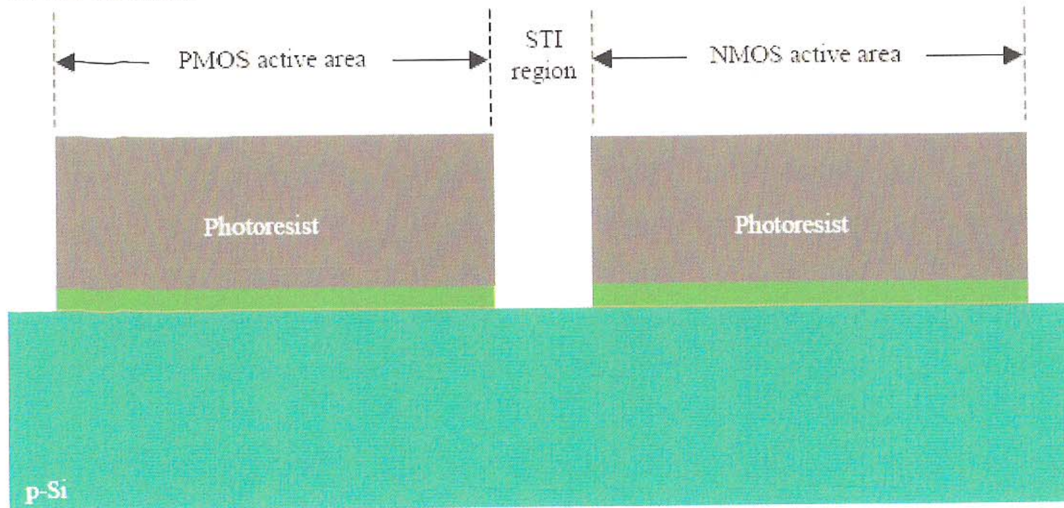


Figure 7.30 STI definition, photolithography and nitride/pad oxide etch with fluorocarbon- based RIE.

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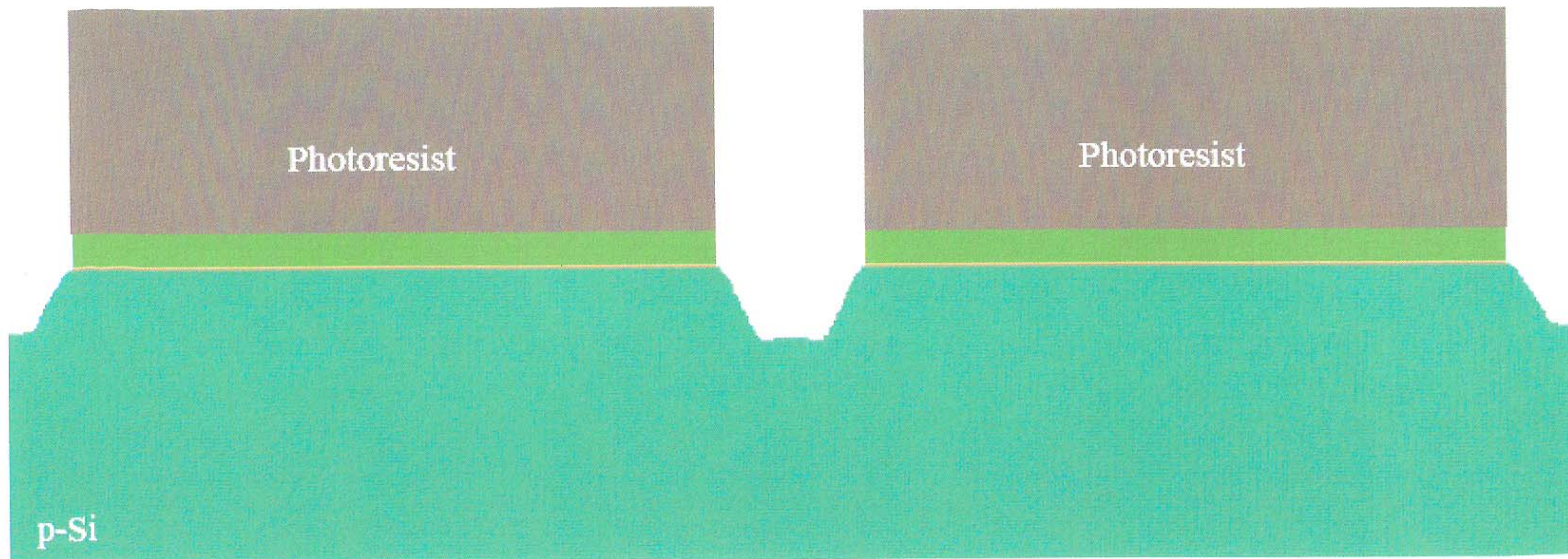

Figure 7.31 Timed silicon trench reactive ion etch.

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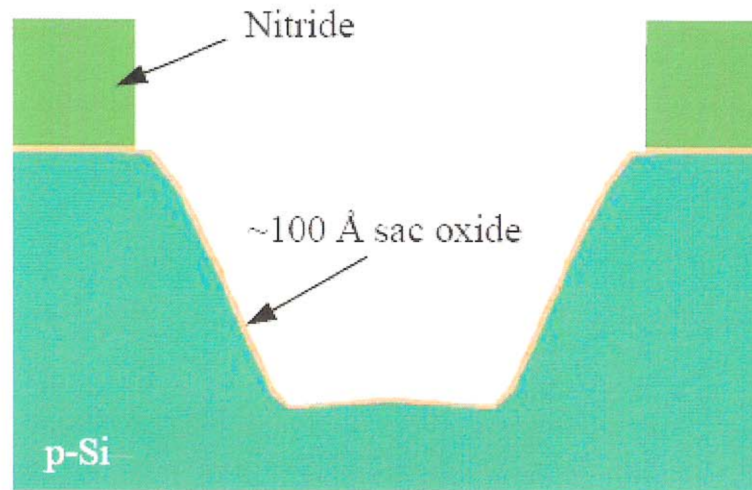

Figure 7.32 Cross section showing post STI resist strip followed by the dry thermal oxidation (at 900 °C) of a sacrificial (sac) oxide in the trench.

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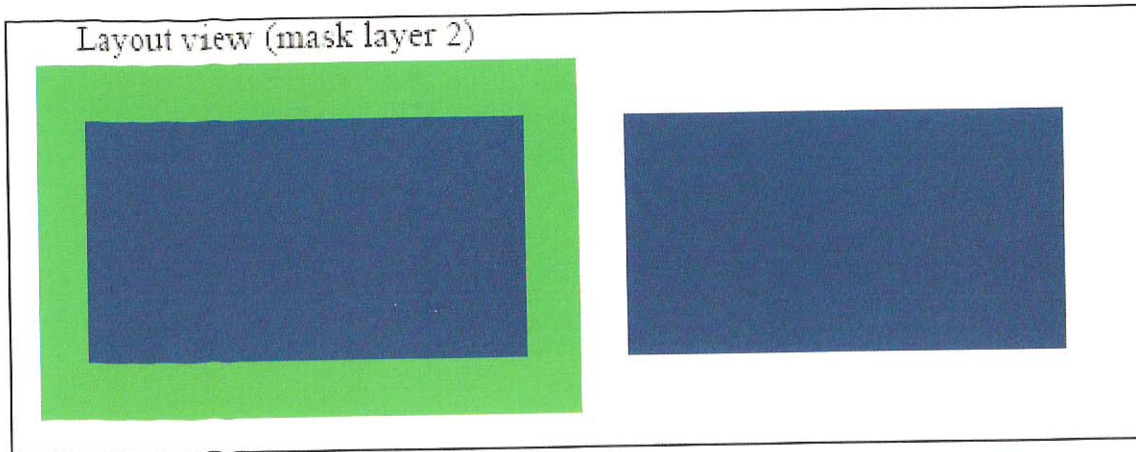
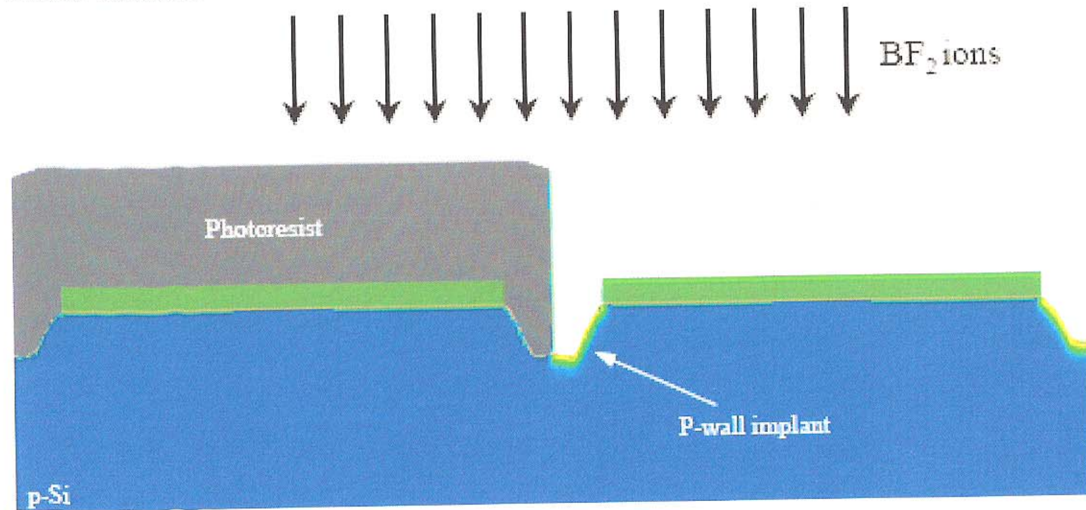


Cross-section



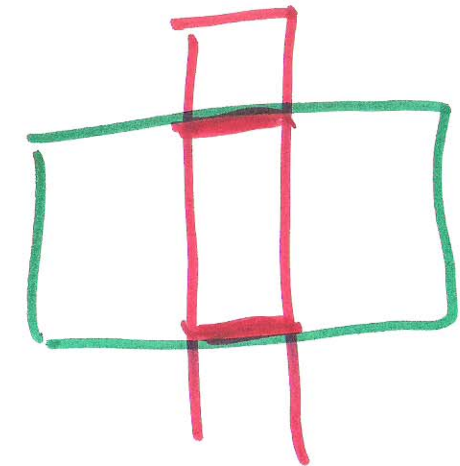


Figure 7.33 P-wall sidewall formation via photolithography and BF_2 implantation.

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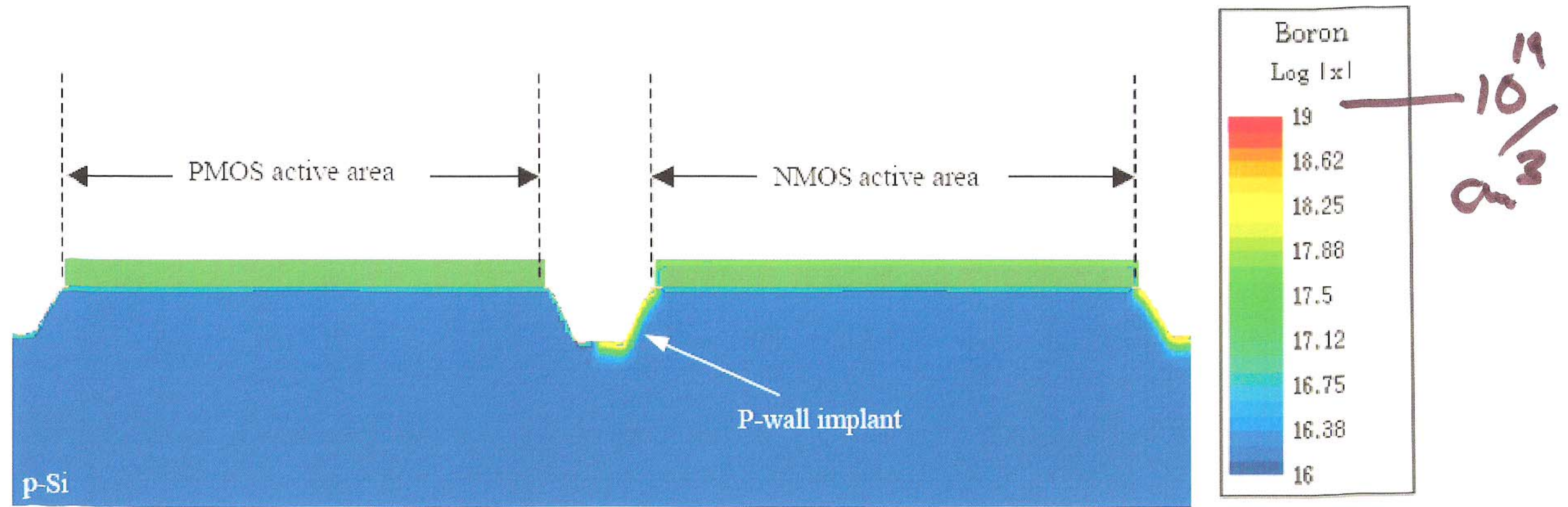

Figure 7.34 Post p-wall photoresist strip using O_2 plasma and wet processing.

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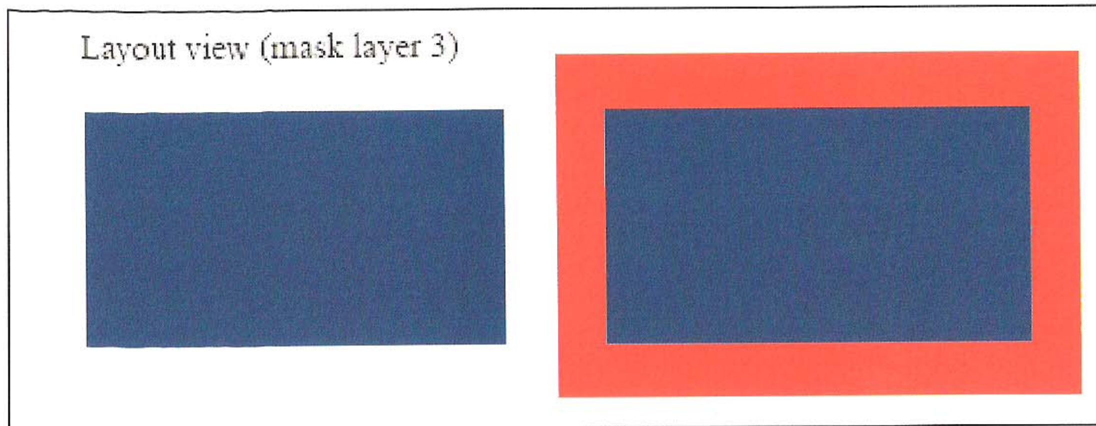

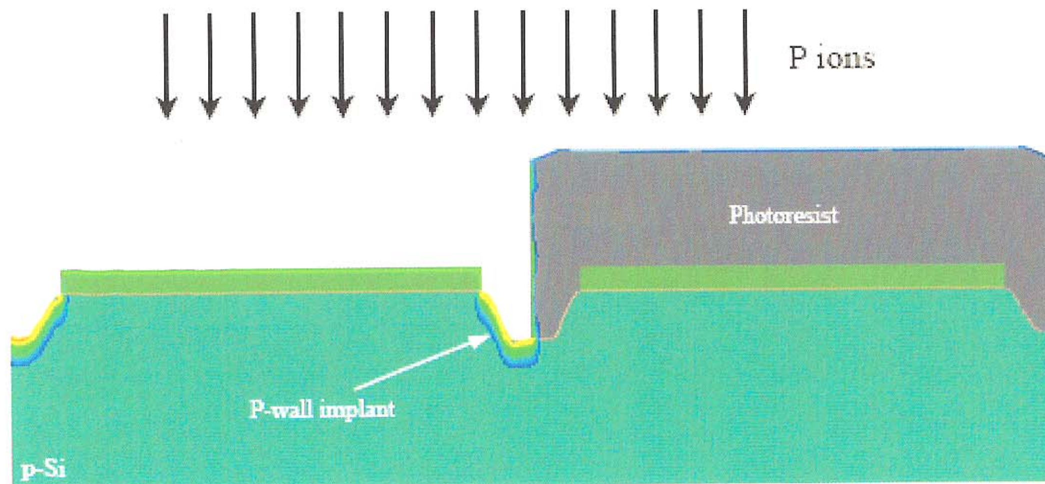

Figure 7.35 N-wall sidewall formation via photolithography and *P* implantation.

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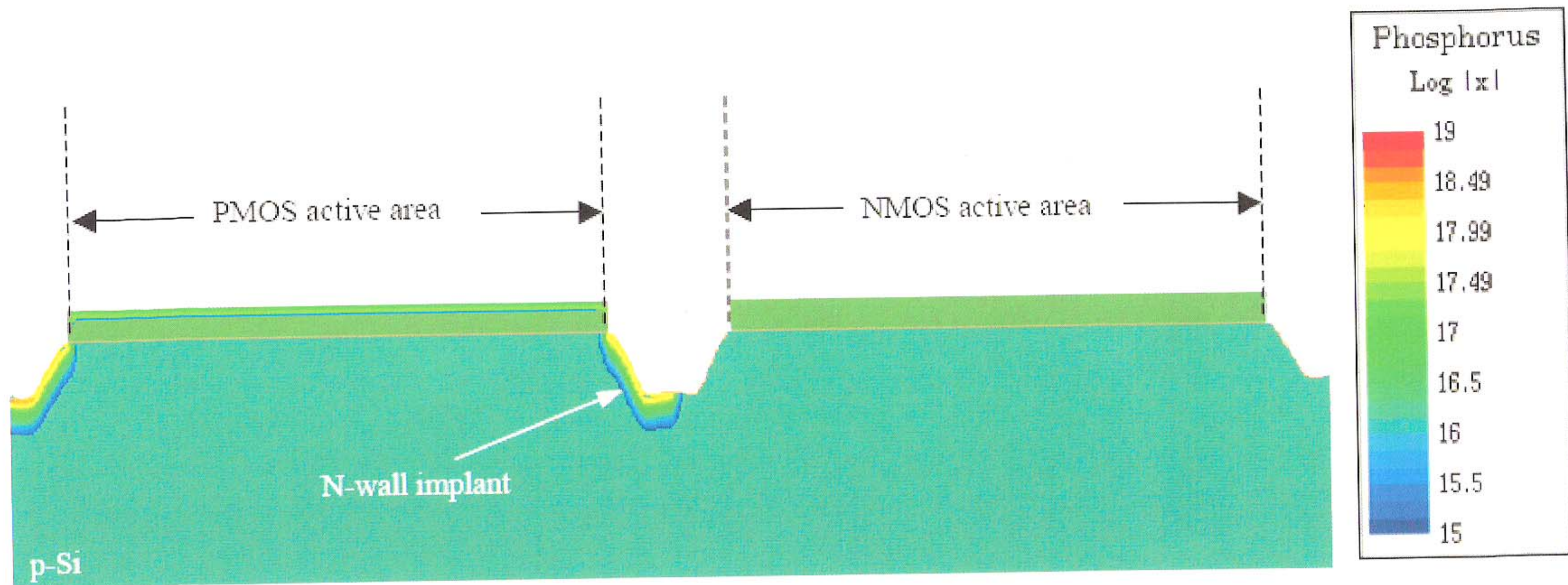

Figure 7.36 Post n-wall photoresist strip using O_2 plasma and wet processing.

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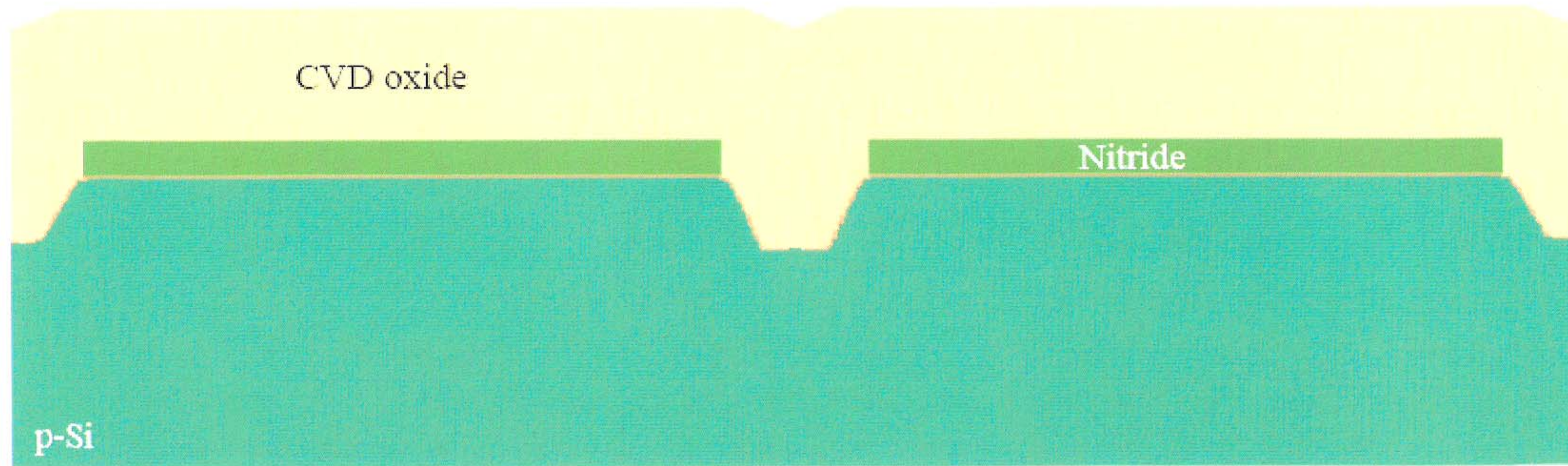

Figure 7.37 High-quality, 100 Å thick liner oxide, is thermally grown at 900 °C. High-density plasma (HDP) CVD trench fill at room temperature. Notice the trenches are overfilled.

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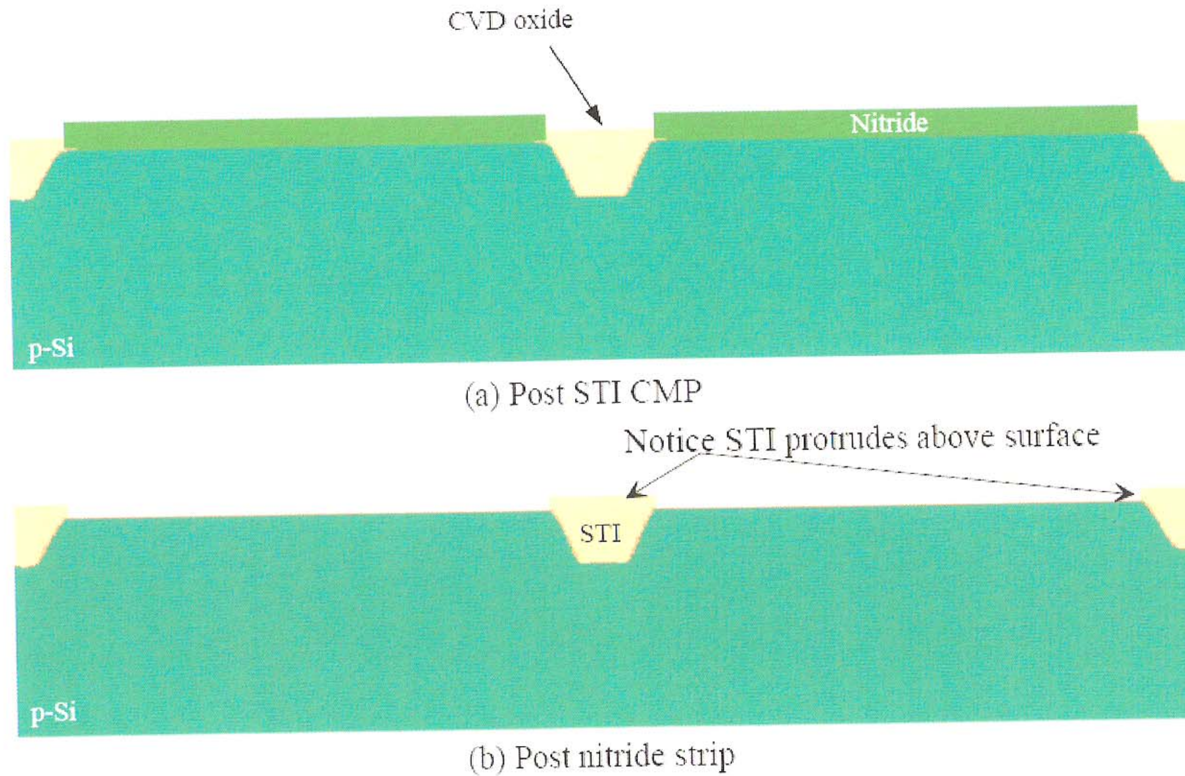
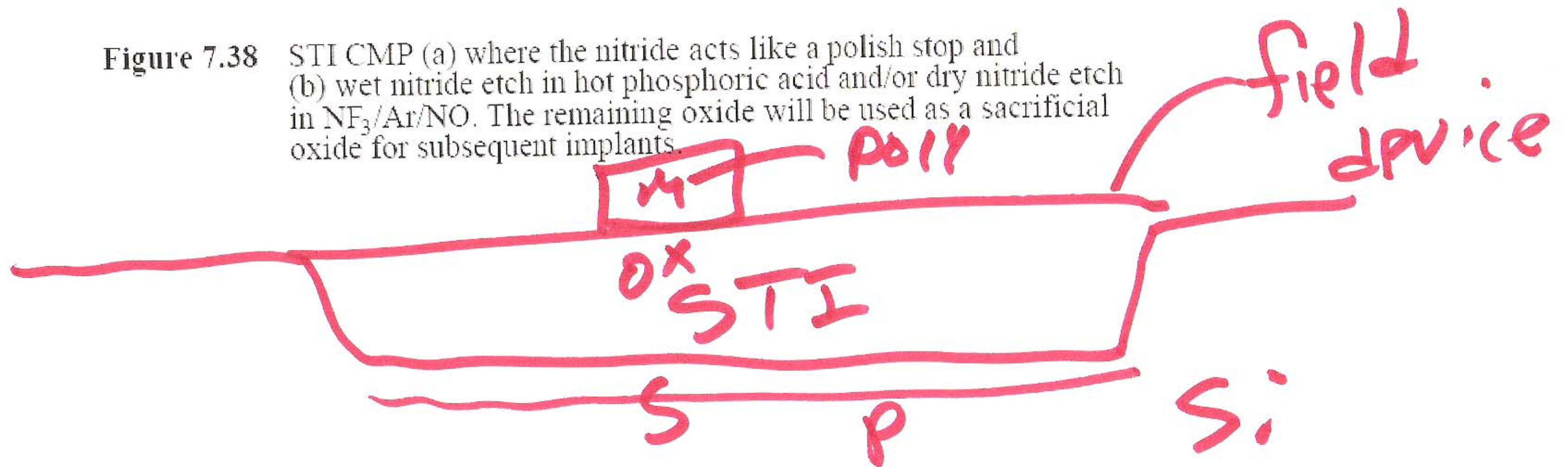


Figure 7.38 STI CMP (a) where the nitride acts like a polish stop and (b) wet nitride etch in hot phosphoric acid and/or dry nitride etch in NF_3/Ar/NO. The remaining oxide will be used as a sacrificial oxide for subsequent implants.



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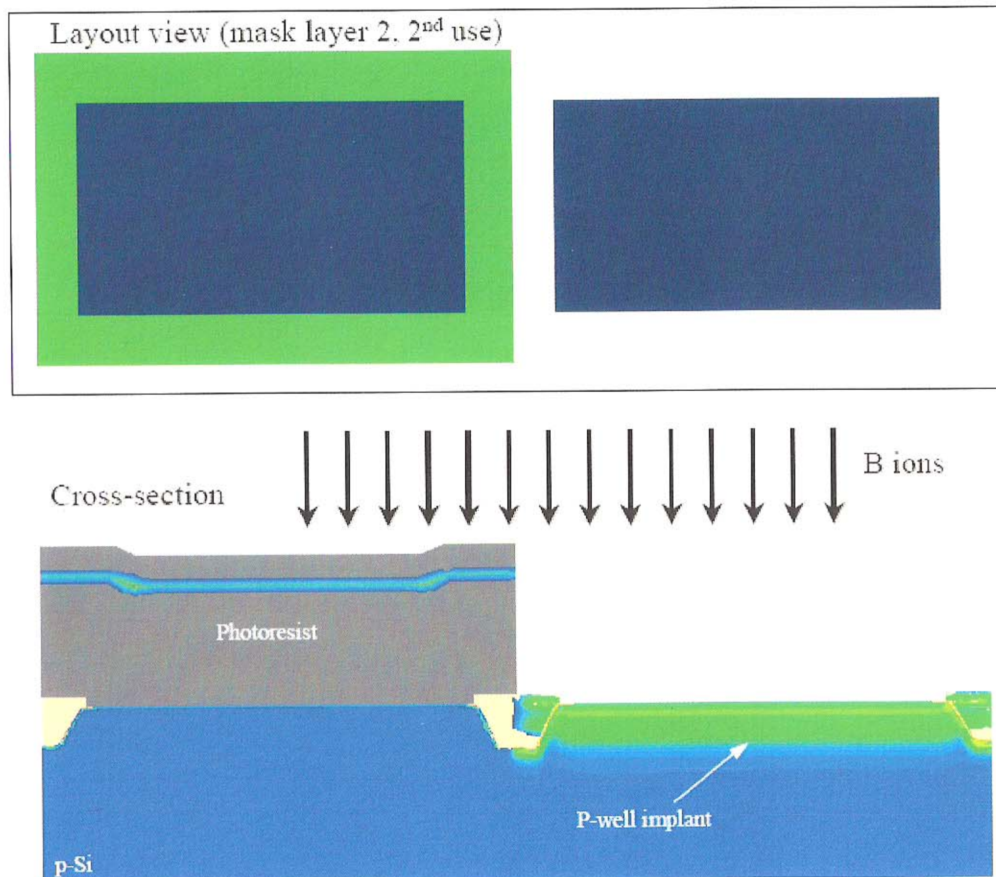

Figure 7.39 P-well formation via photolithography and *B* implantation.

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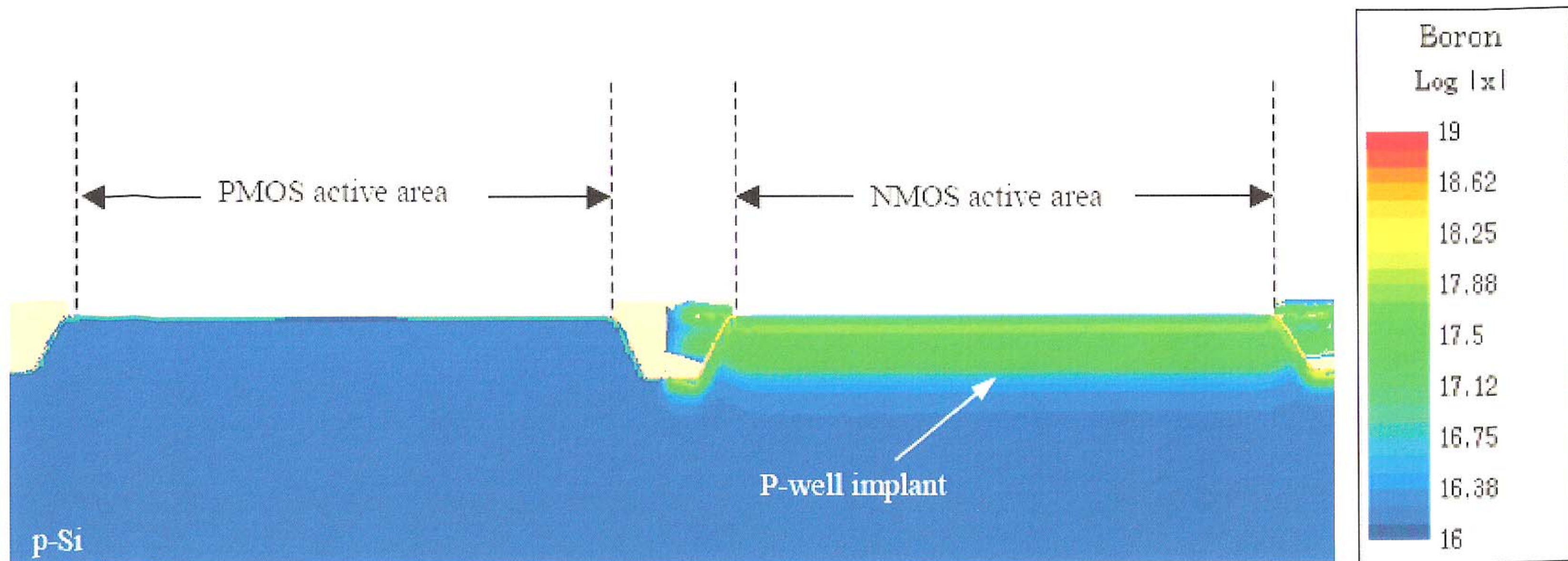

Figure 7.40 Post p-well photoresist strip using O_2 plasma and wet processing.

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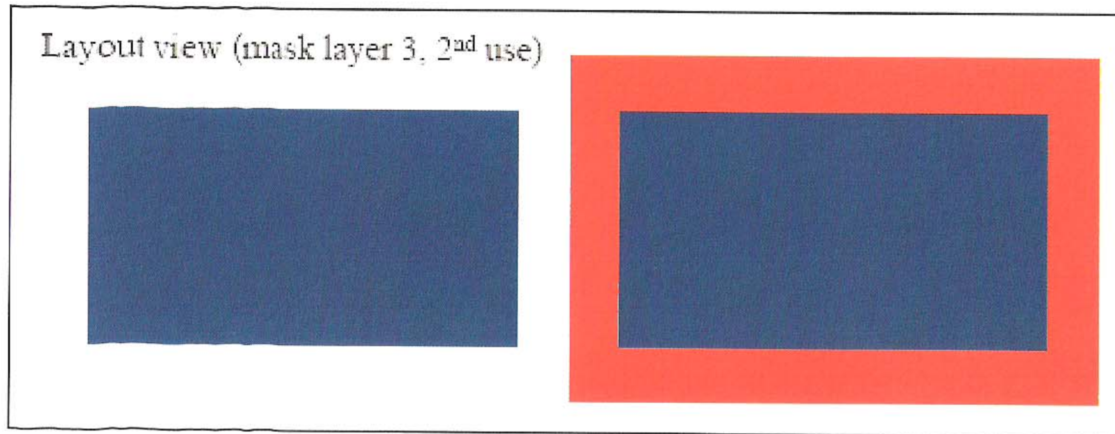

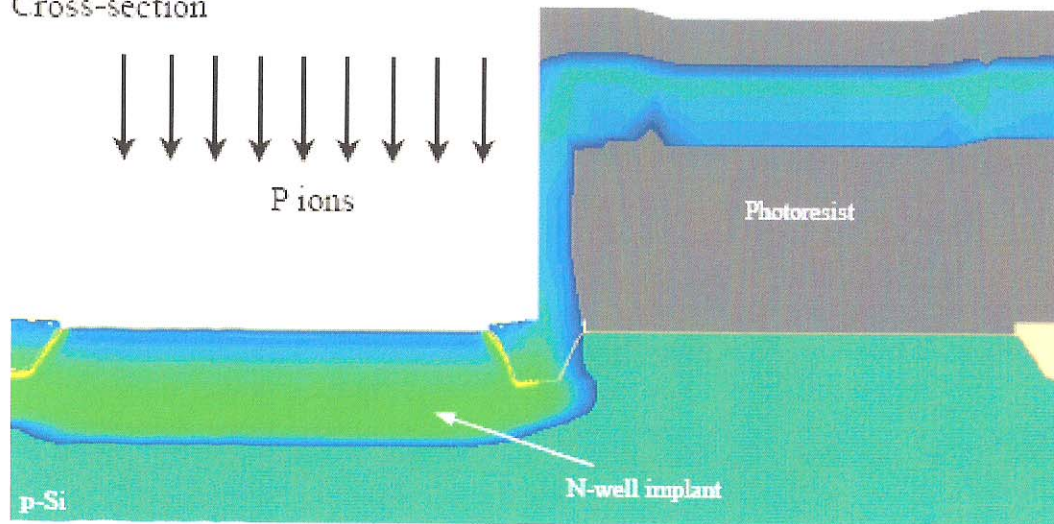

Figure 7.41 N-well formation via photolithography and *P* implantation.

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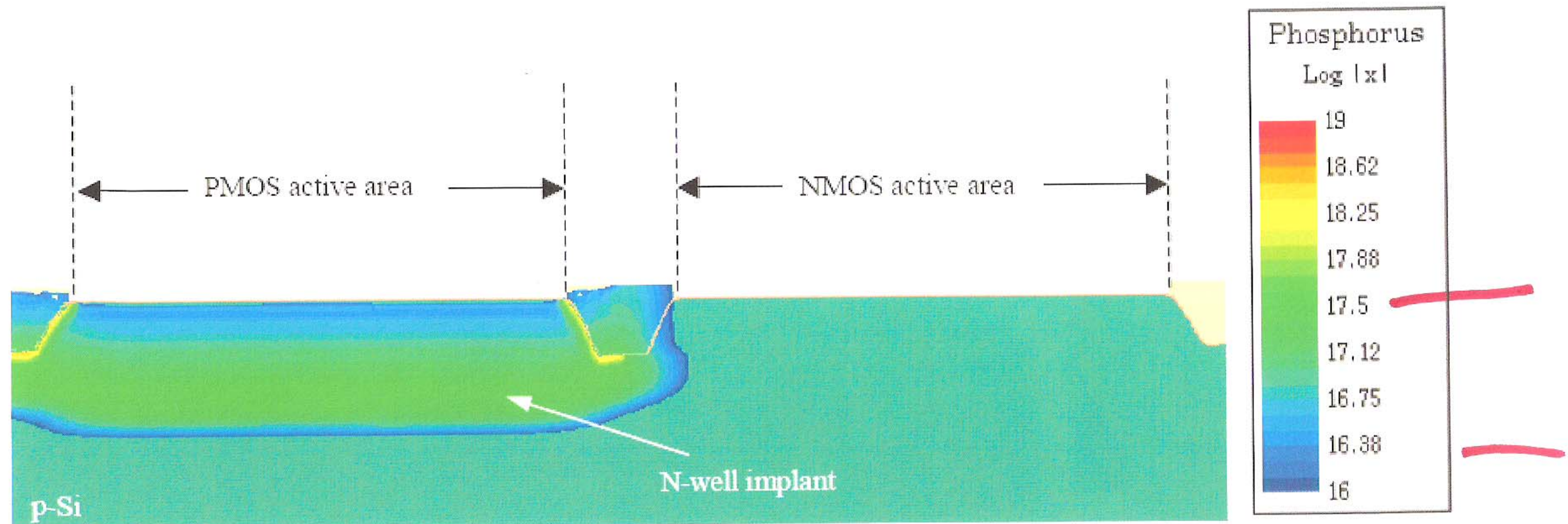


Figure 7.42 Post n-well photoresist strip using O_2 plasma and wet processing.

retrograde profile

20)

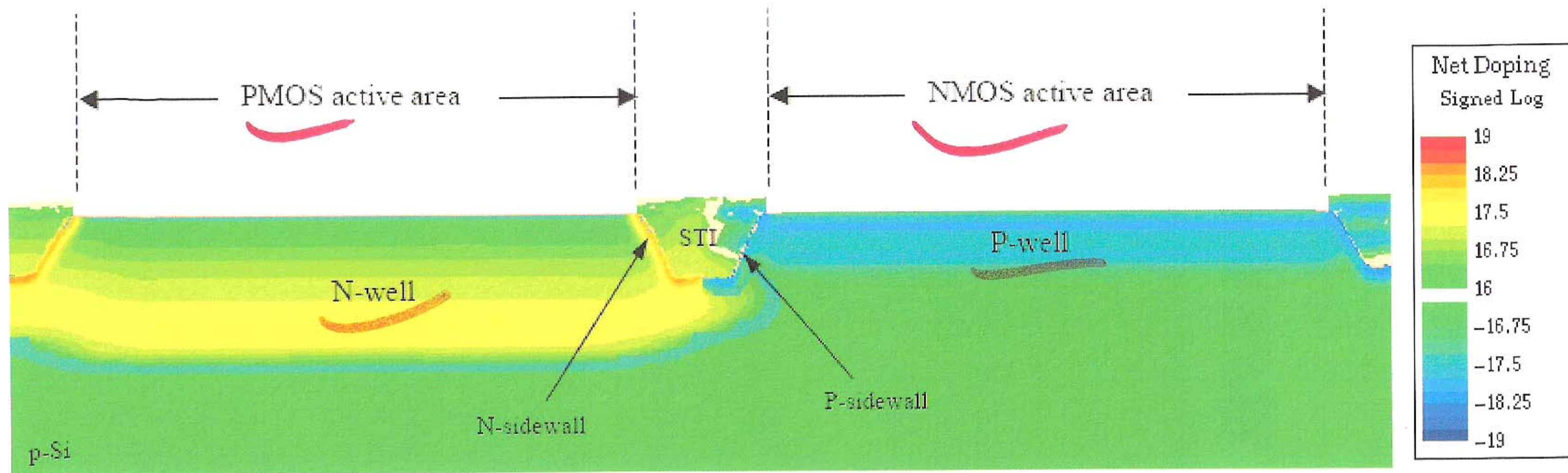
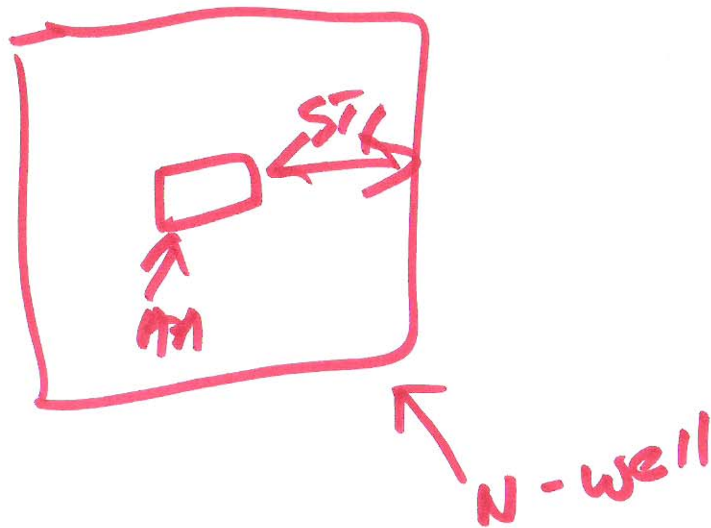


Figure 7.43 Net doping profile of both the n-well and the p-well.



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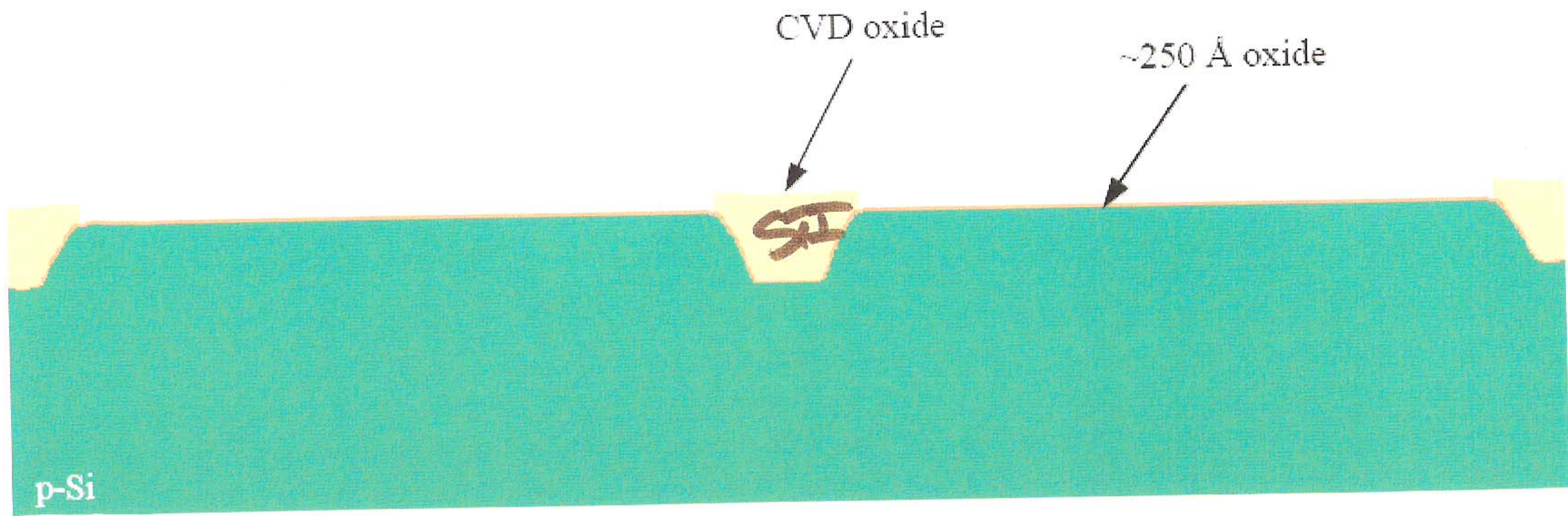

Figure 7.44 Wet etch the remaining trench stack oxide using buffered *HF*. Sacrificial oxide formation using dry thermal oxidation at approximately 900 °C.

N-well
p-well not shown

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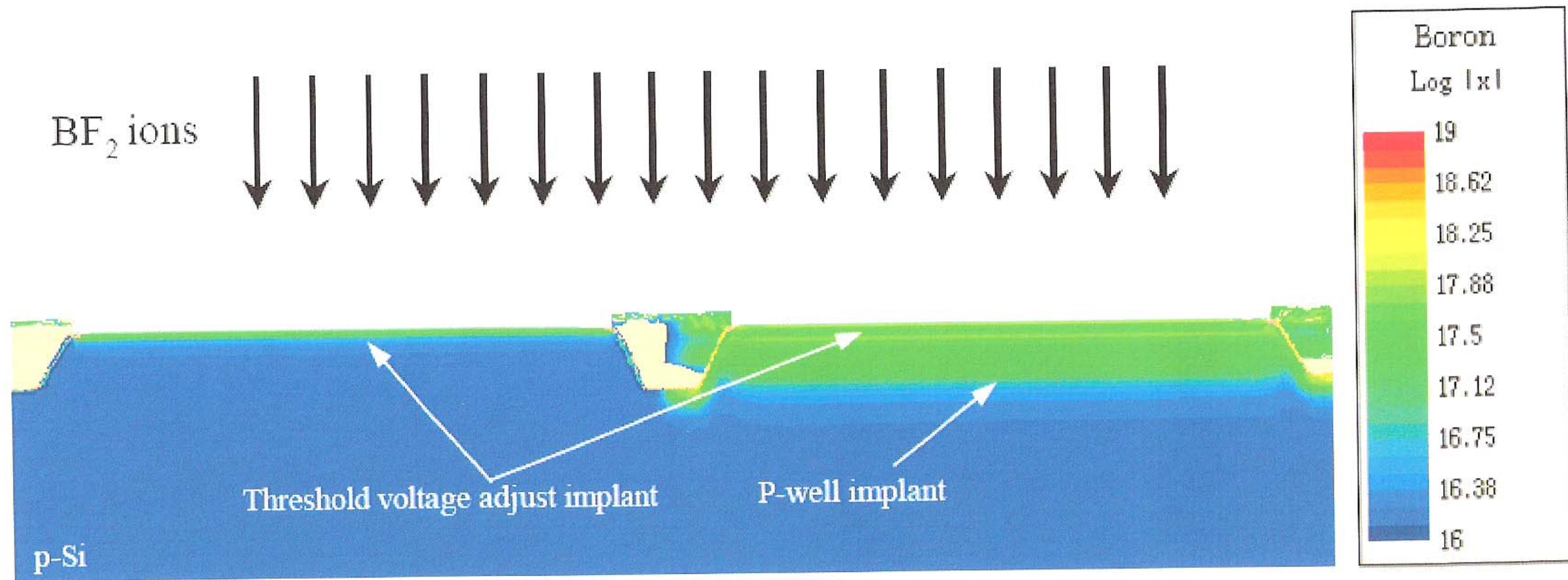

Figure 7.45 Blanket low-energy BF_2 implant for NMOS and PMOS threshold voltage adjust.

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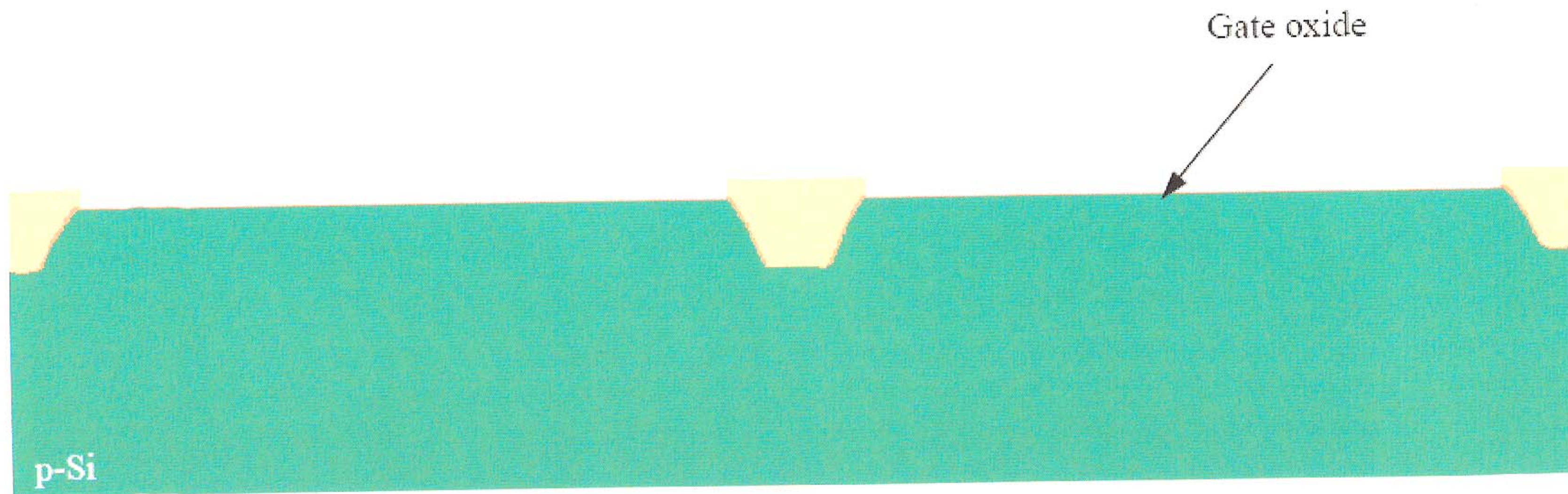

Figure 7.46 Removal of sacrificial oxide using buffered *HF* followed by gate dielectric formation using dry oxidation in an ambient of O_2 . *NO* and/or N_2O.

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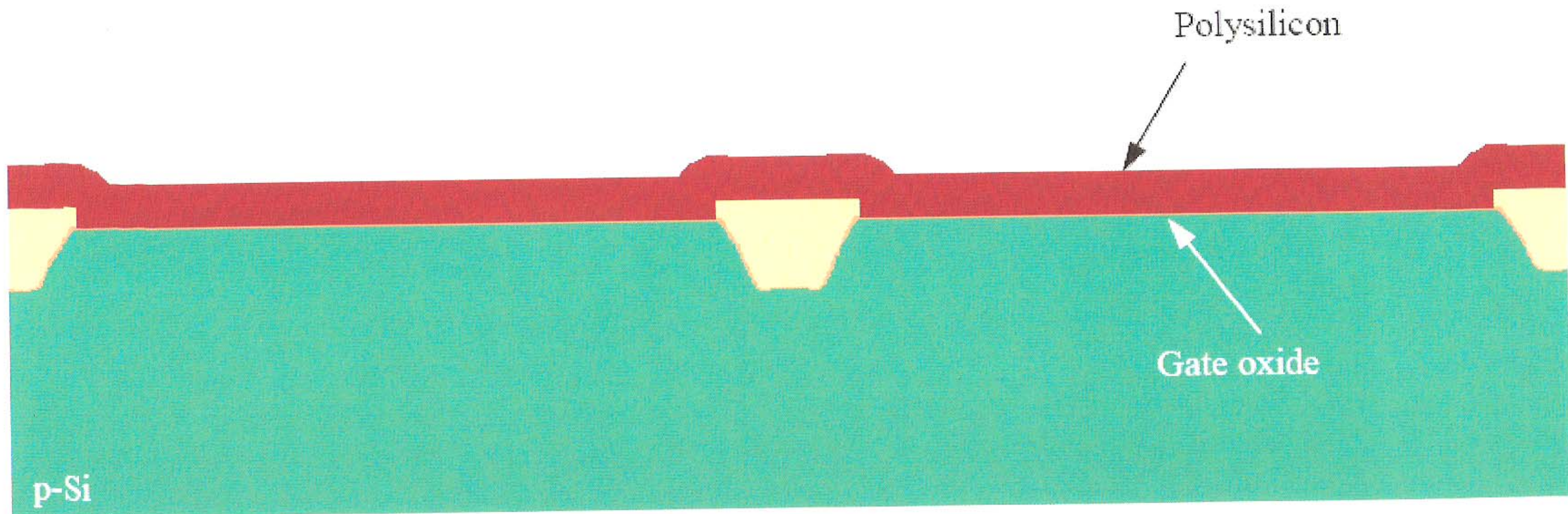

Figure 7.47 Polysilicon deposition via LPCVD at approximately 550 °C. Note the polysilicon deposition must occur immediately following gate oxidation.

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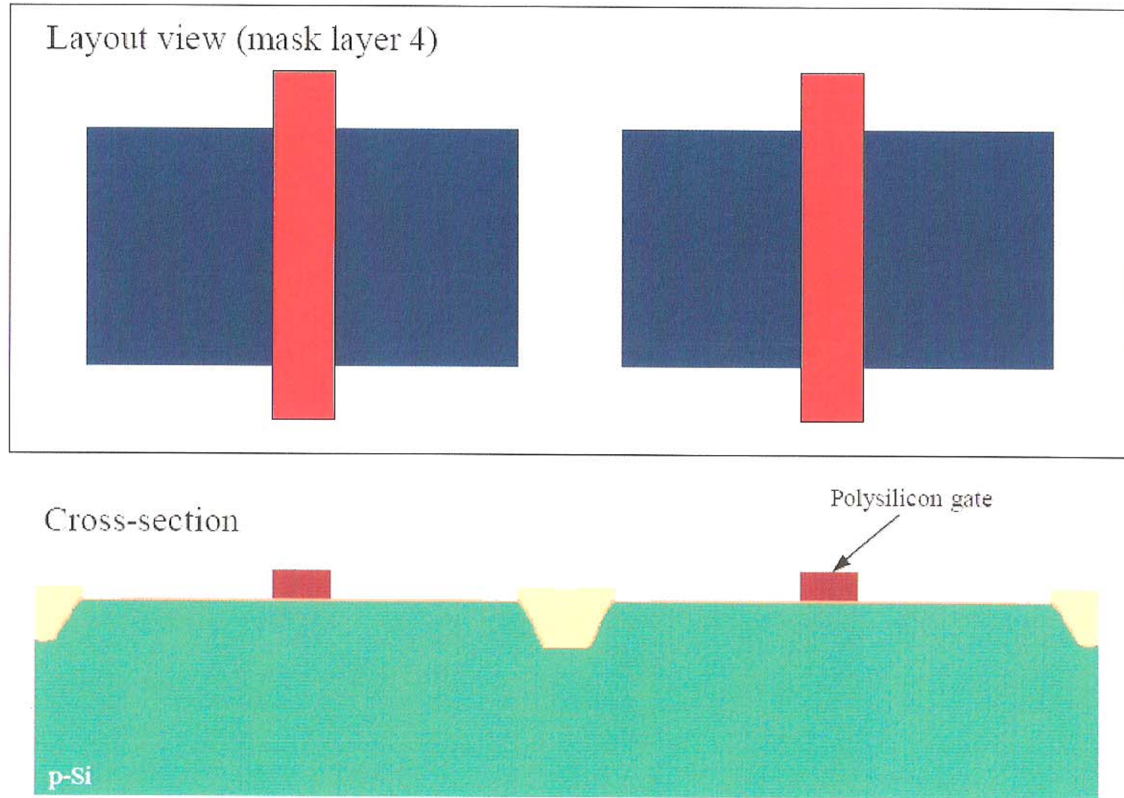

Figure 7.48 Gate electrode and local interconnect photolithography and polysilicon reactive ion etching.

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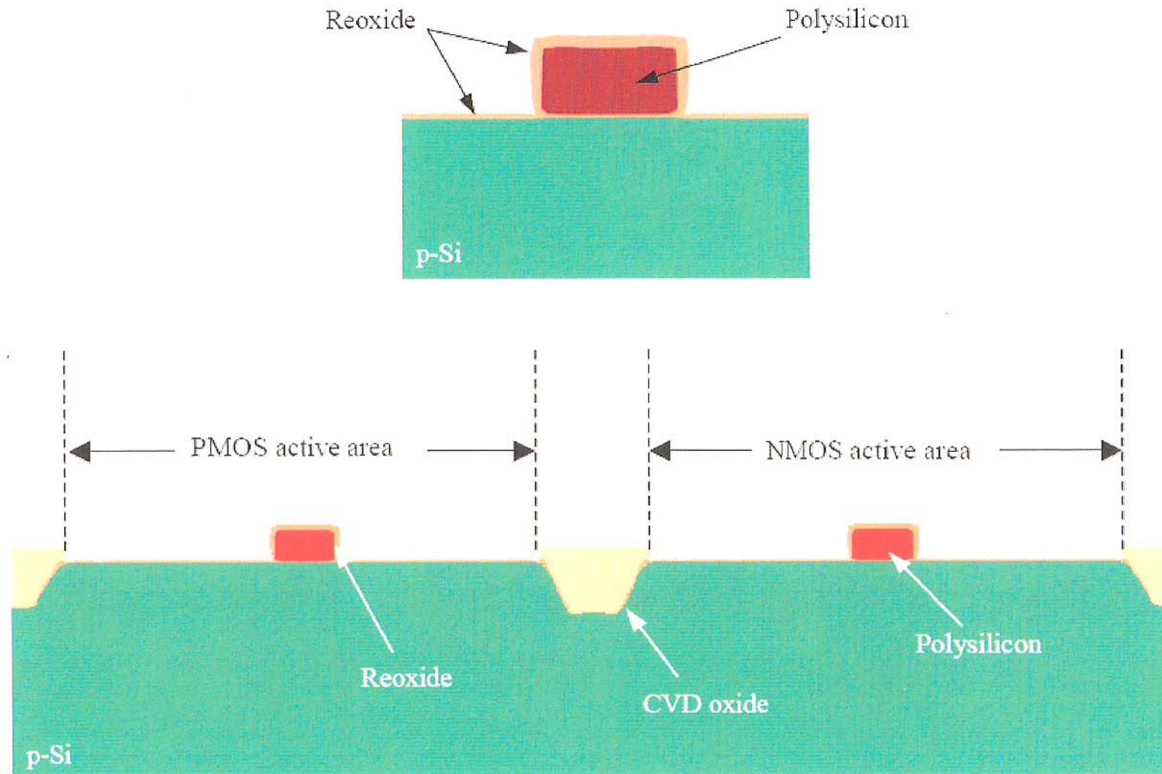

Figure 7.49 Polysilcion reoxidation using dry O_2 at approximately 900 °C. Notice the resulting oxide is thicker on the polysilicon then on the active silicon.

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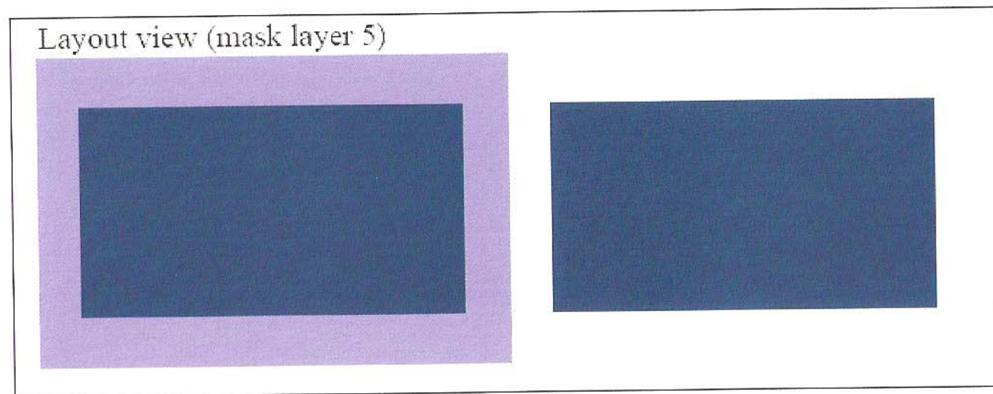


Cross-section

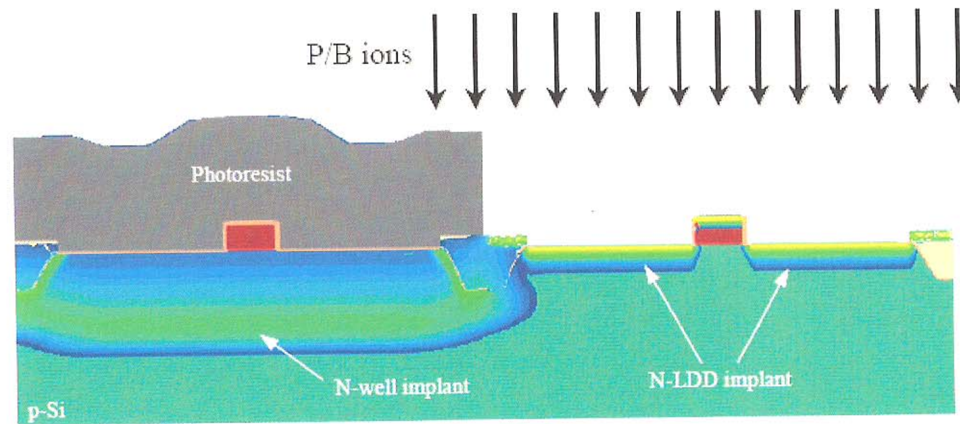
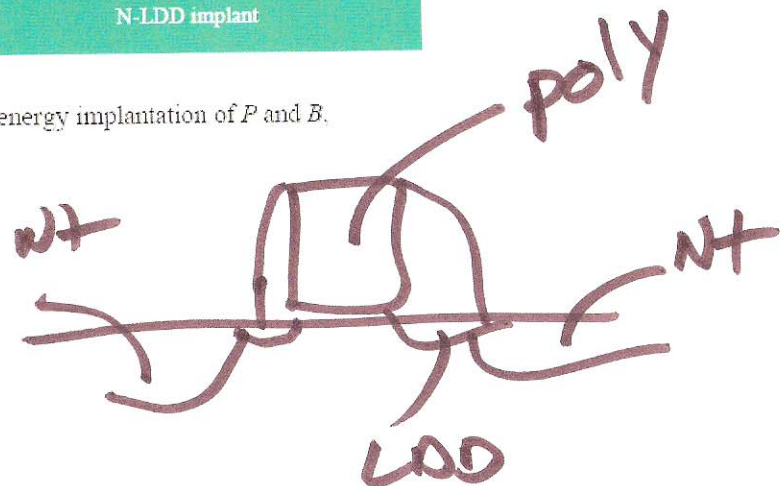


Figure 7.50 N-LDD/n-pocket formation using low energy implantation of *P* and *B*.



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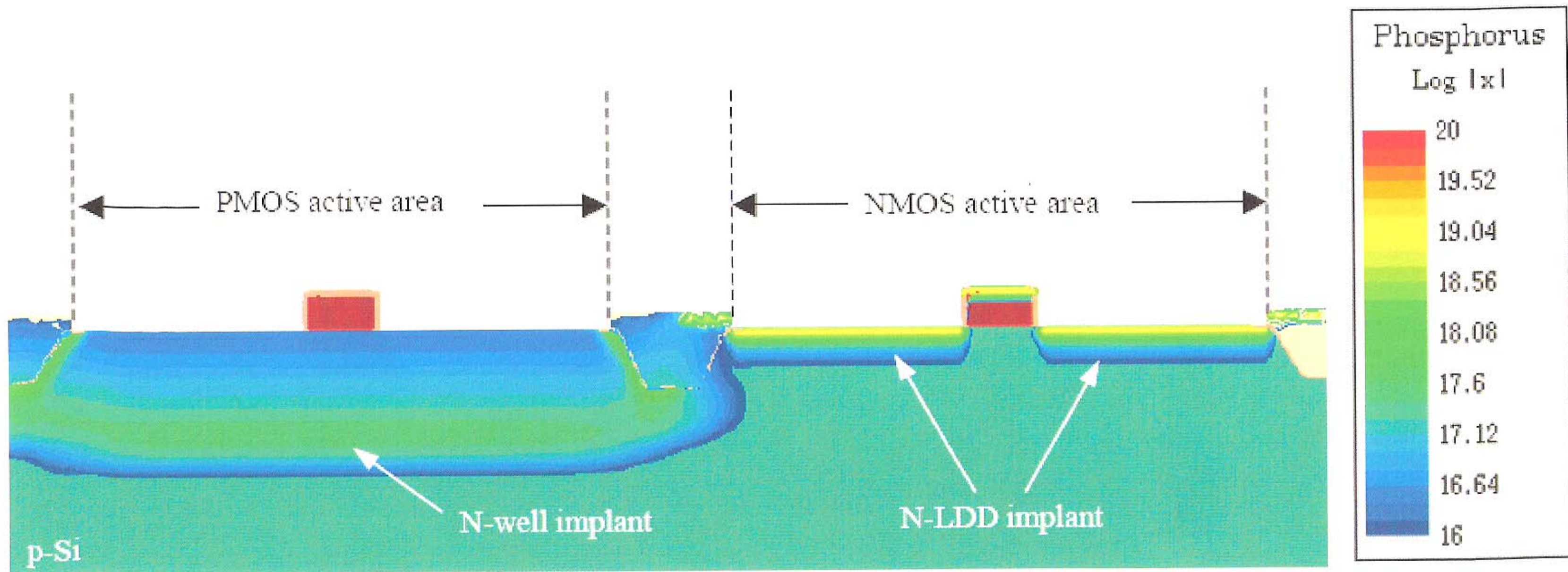

Figure 7.51 Post N-LDD resist strip using O_2 plasma and wet processing.

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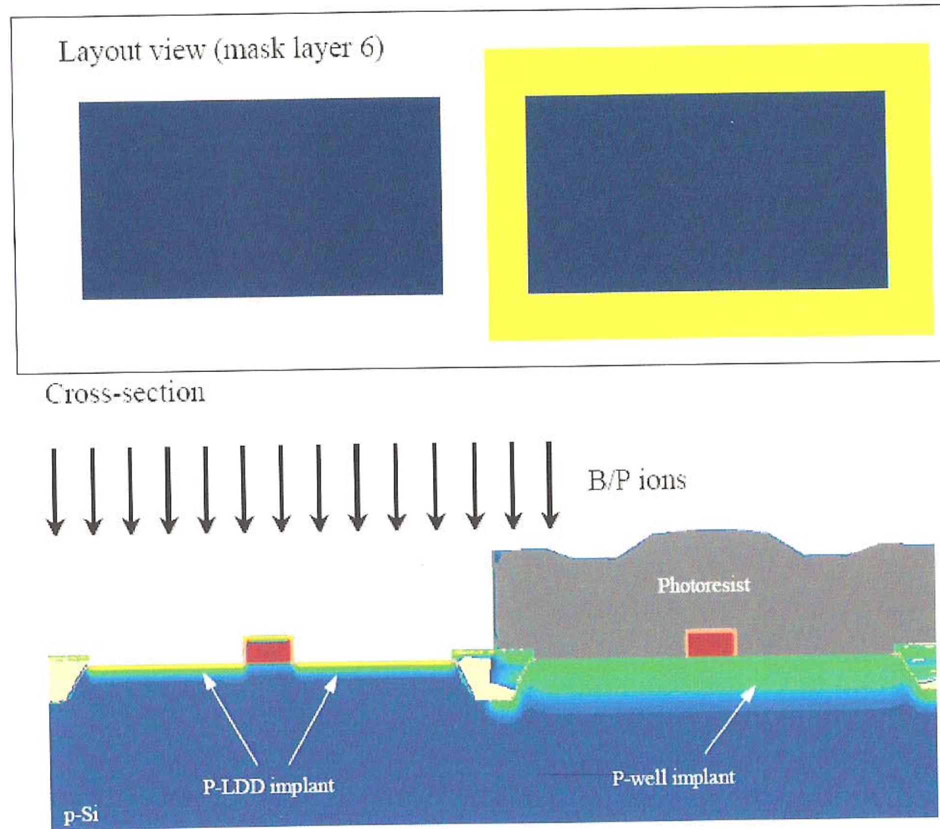

Figure 7.52 P-LDD/p-pocket formation using low energy implantation of *B* and *P*, respectively.

30)

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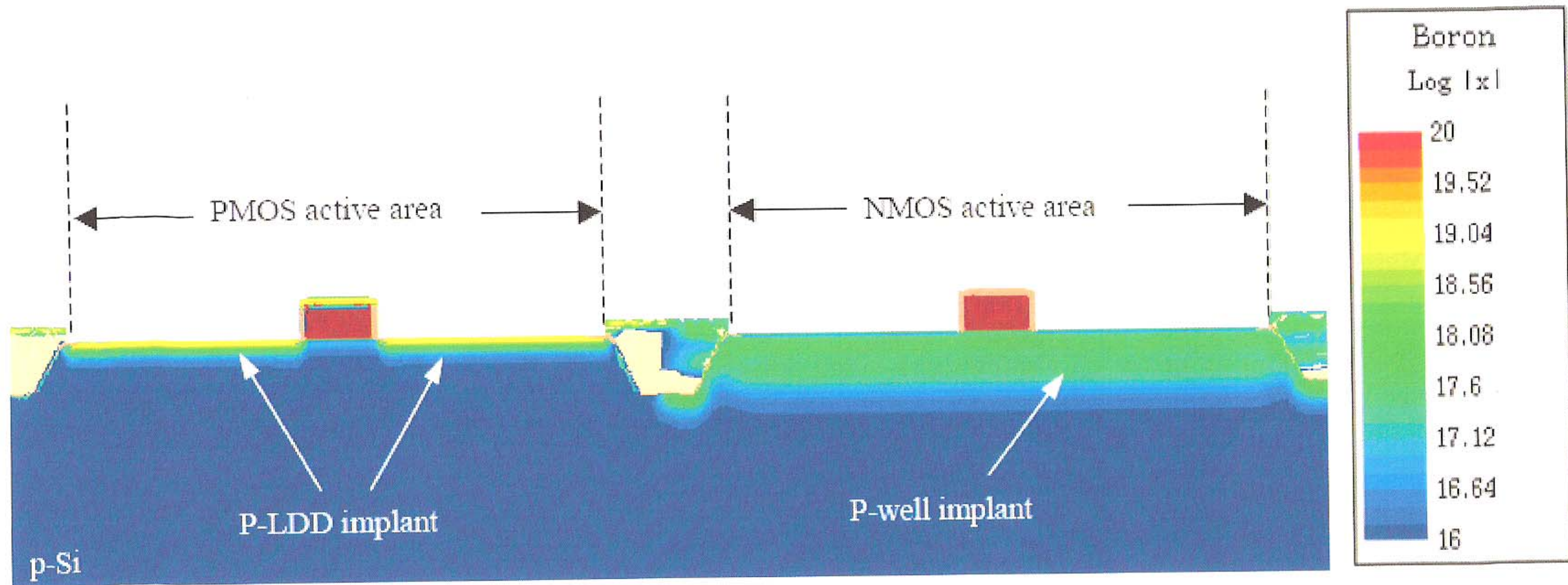

Figure 7.53 Post P-LDD resist strip using O_2 plasma and wet processing.

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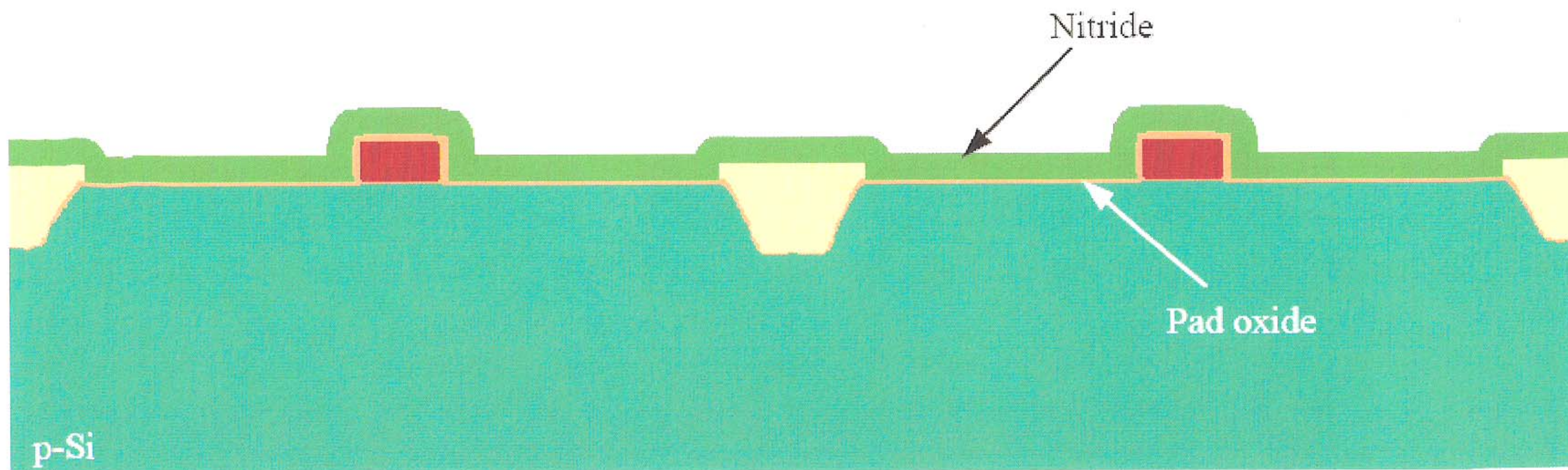

Figure 7.54 Sidewall spacer nitride deposition using LPCVD at approximately 800 °C.

32)

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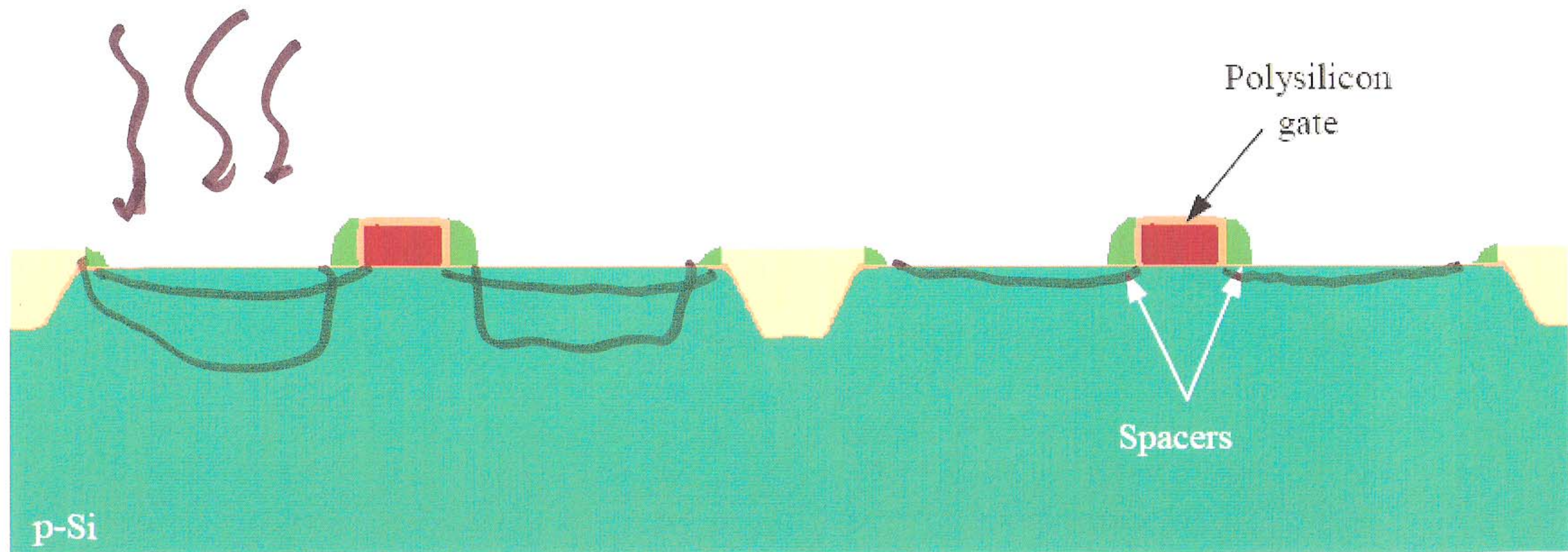

Figure 7.55 Dry, anisotropic, end-pointed reactive ion etch of spacer nitrate yielding gate sidewall spacers.

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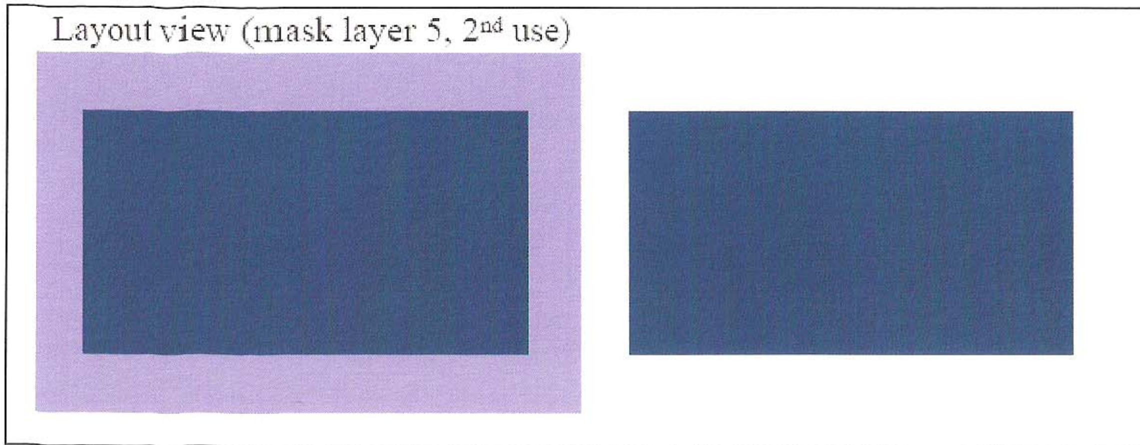

Cross-section

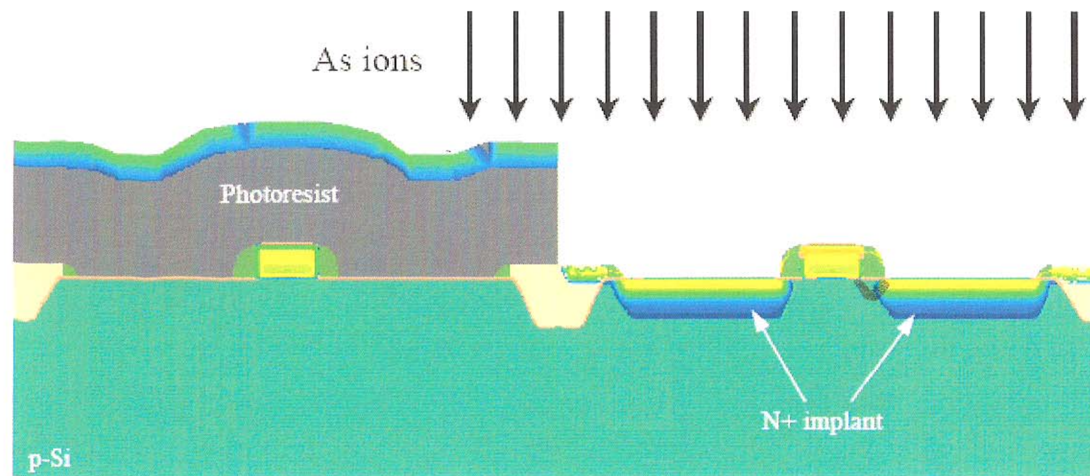

Figure 7.56 N+ source/drain formation using a low energy, high dose implantation of *As*.

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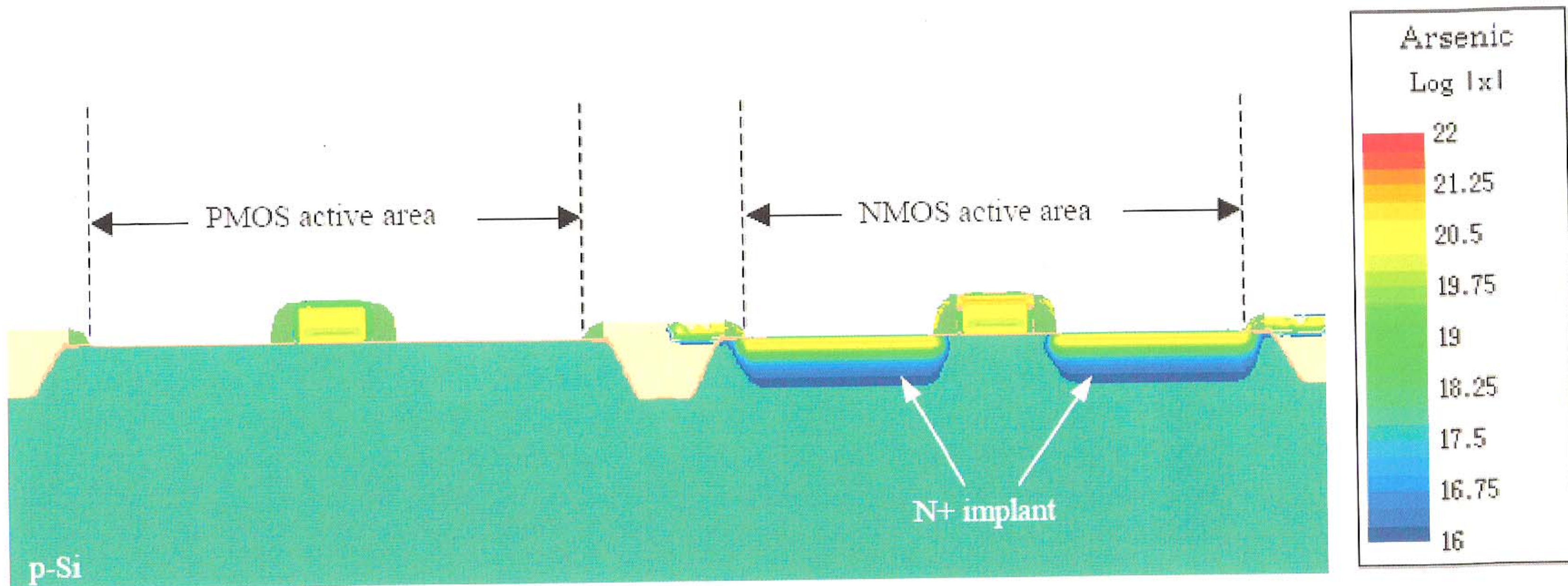

Figure 7.57 Post n+ resist strip using O_2 plasma and wet processing.

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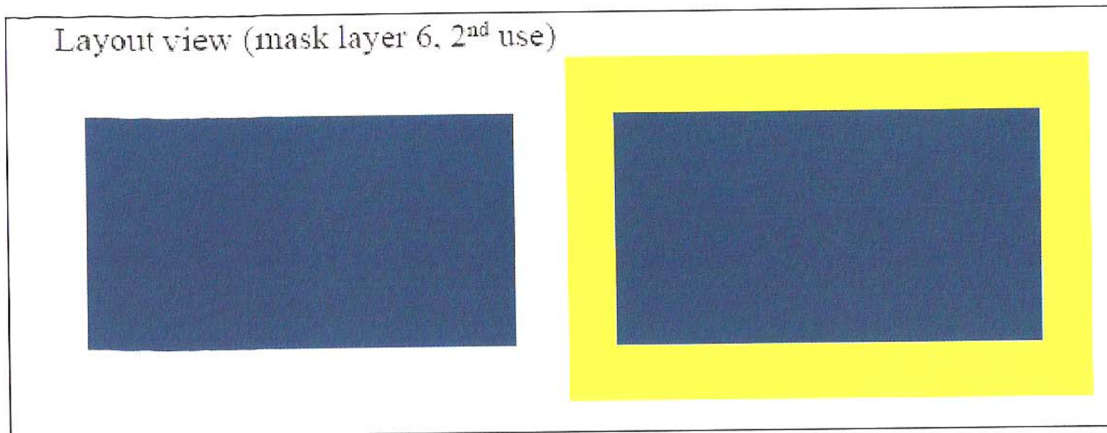

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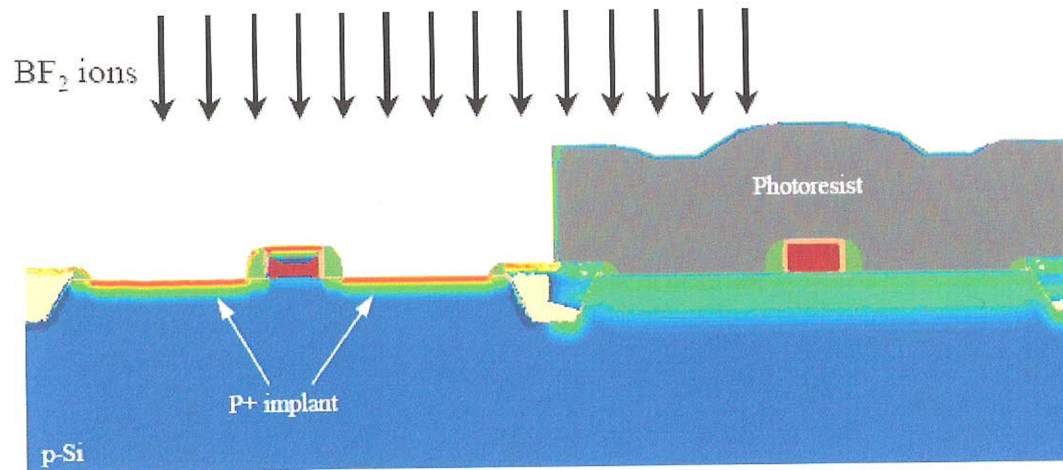

Figure 7.58 P+ source/drain formation using a low energy, high dose implantation of BF_2.

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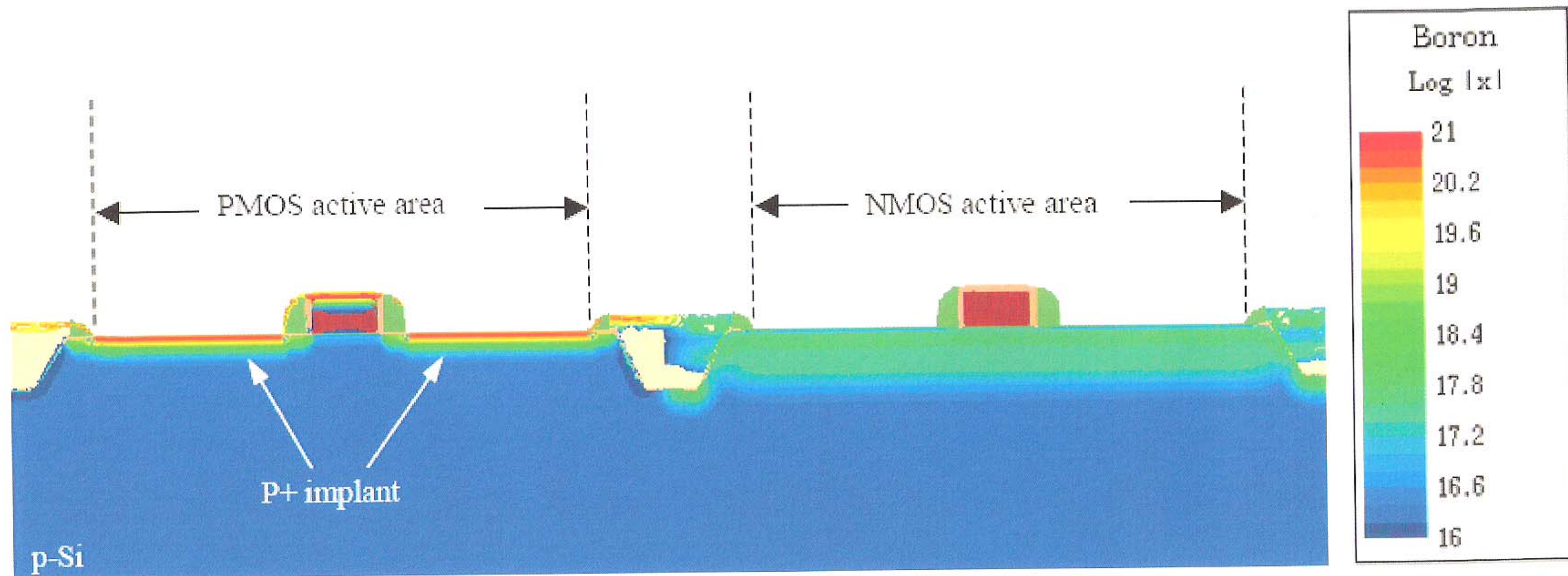

Figure 7.59 Post p+ resist strip using O_2 plasma and wet processing.

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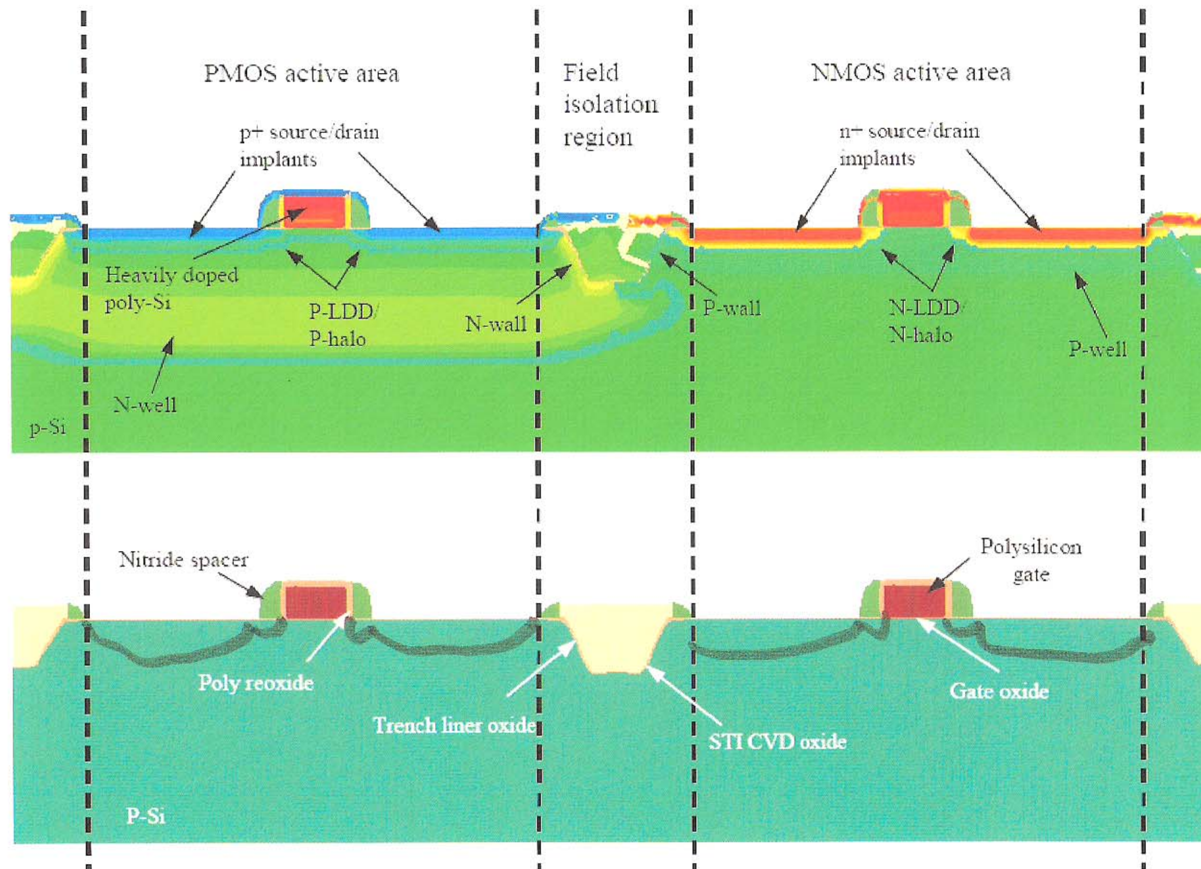

Figure 7.60 Summary of the FEOL features.

35:36

38)

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