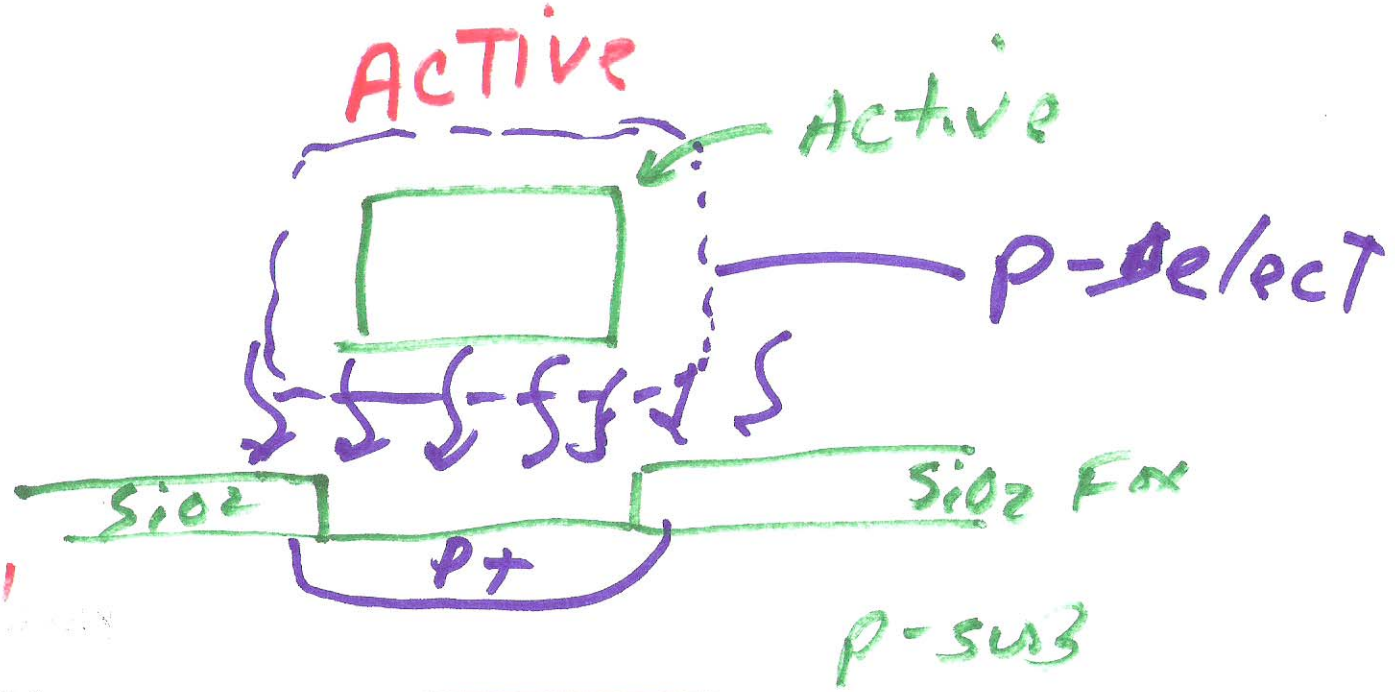
EE 421 / ECG 621

Digital IC Design

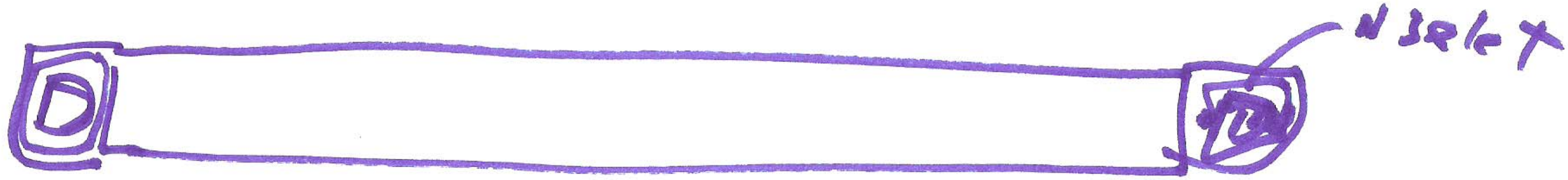
Sept. 22, 2014

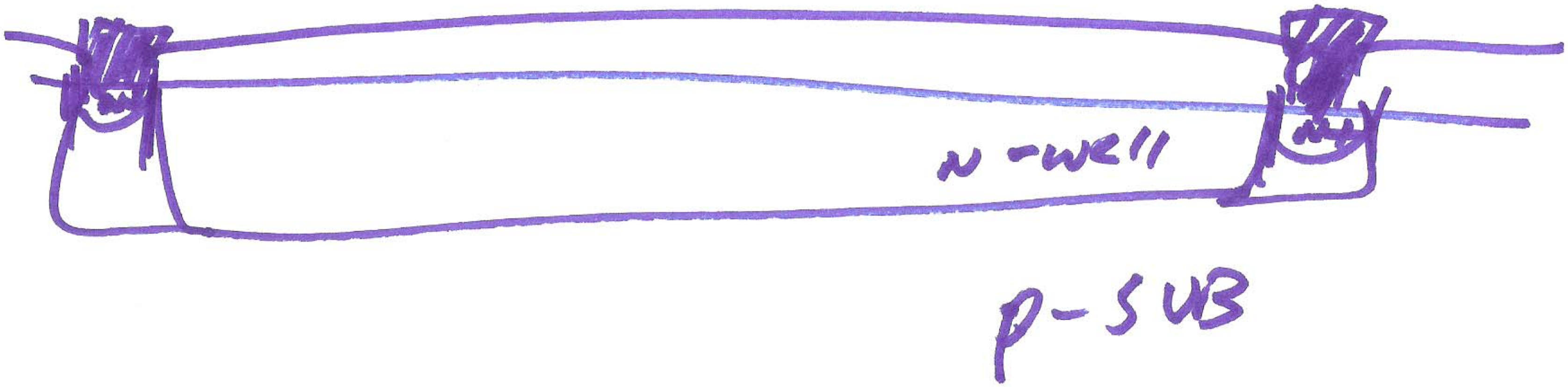
Lecture 8

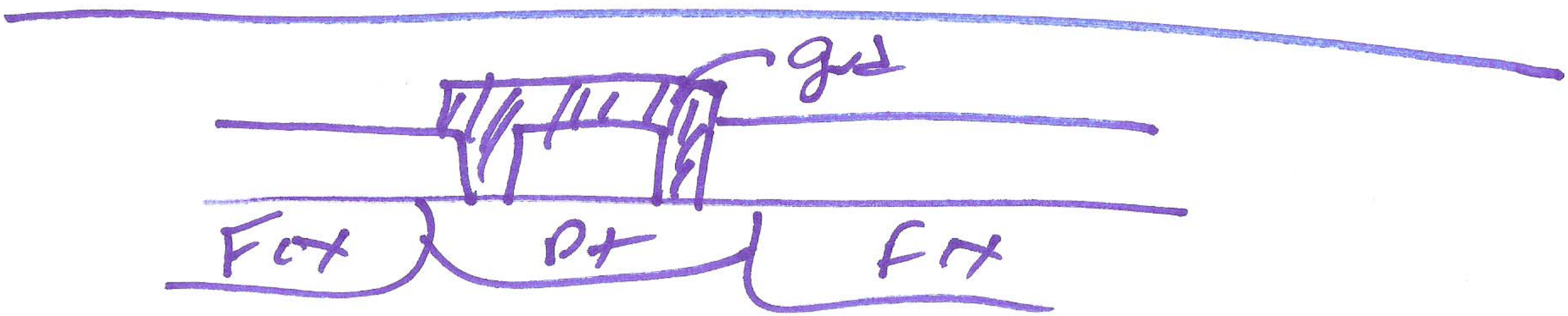
N-well
M1
M2
M3
OVGL
PAD
VIA2
VIA = VIA1

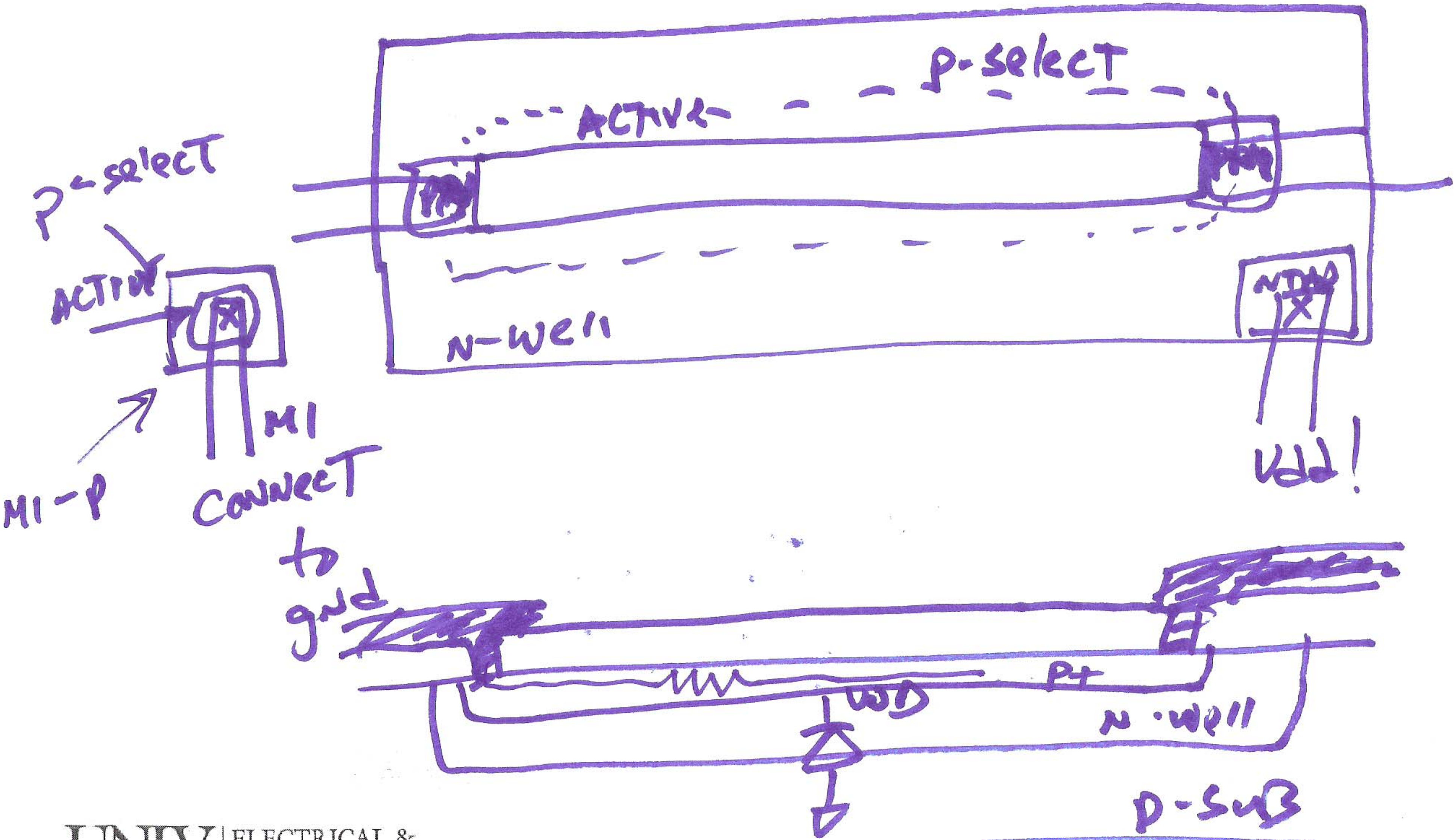


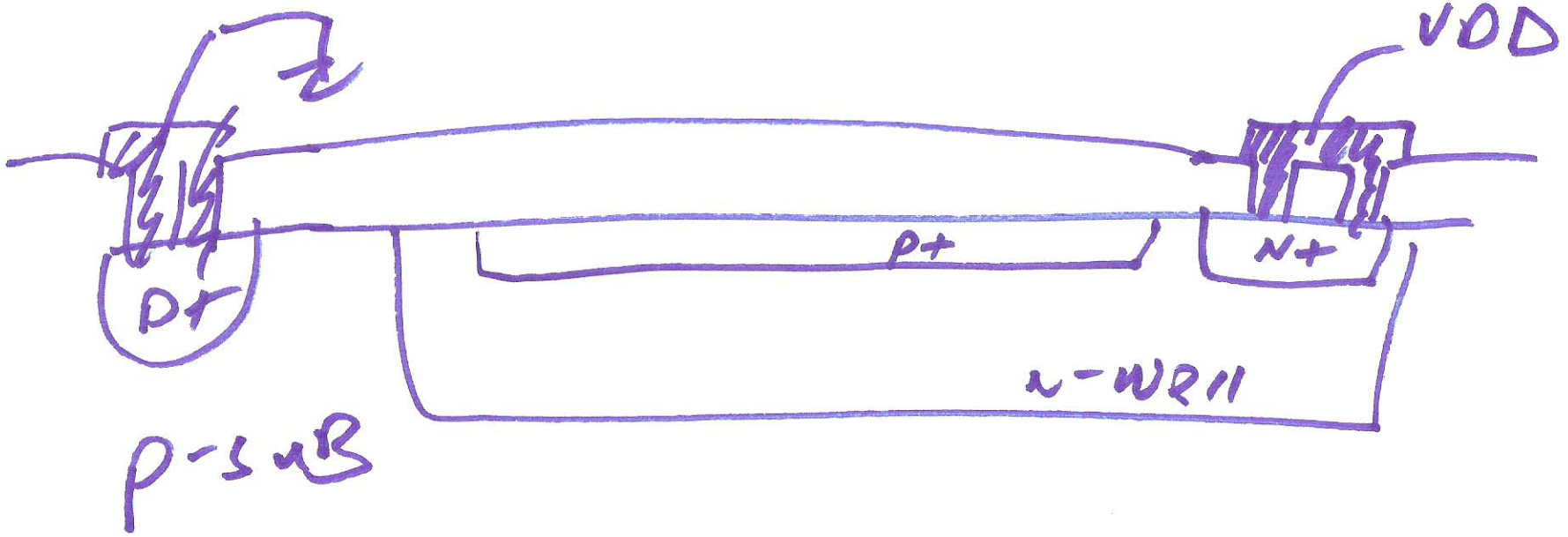
Grounding the substrate


N select


n-well
p-SUB


gnd
Fox
p+
Fox


p-select
ACTIVE
p-select
ACTIVE
N-well
Vdd!
M1-p
M1
connect to gnd
P+
VDD
n-well
p-sub


VDD
P+
N+
n-well
p-sub

Polysilicon is chunks of crystalline Si