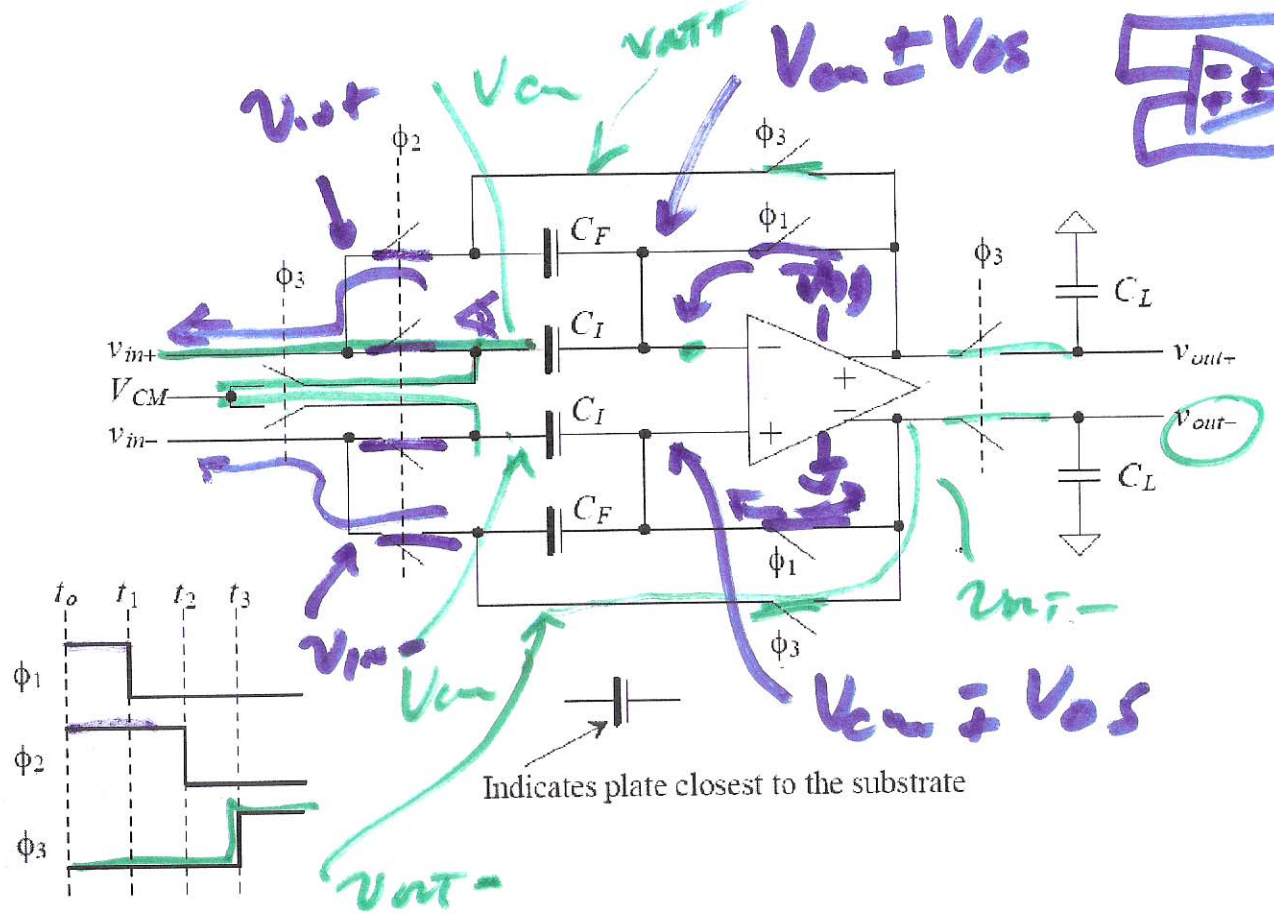

Figure 30.30 Data converter S/H building block.

- To be added

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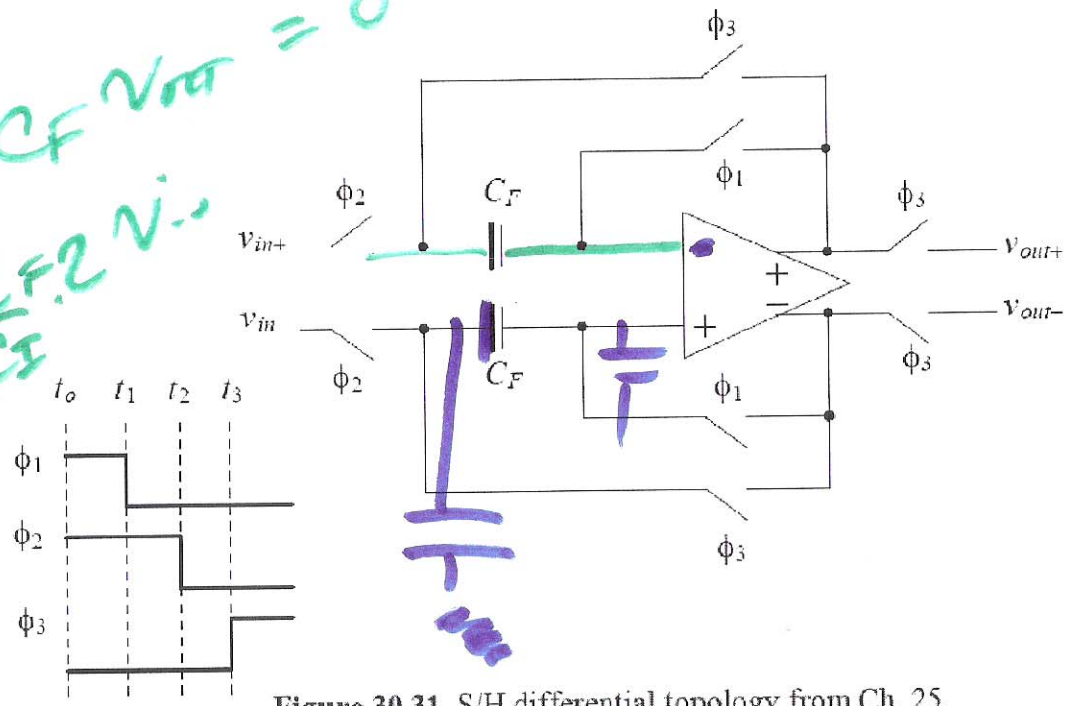

Figure 30.31 S/H differential topology from Ch. 25.

- To be added

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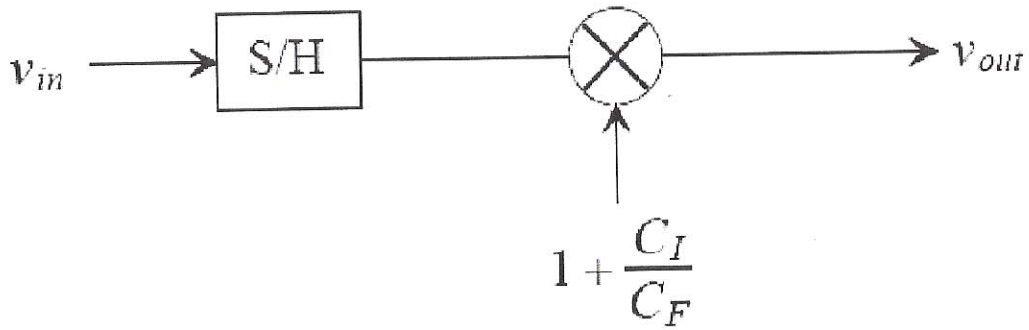

Figure 30.32 Block diagram for the S/H of Fig. 30.30.

- To be added

$$C_I(v_{in}) - C_F v_{out} + C_F v_{in} = 0$$

$$(C_I + C_F)v_{in} = C_F \cdot v_{out}$$

$$\frac{v_{out}}{v_{in}} = \left(1 + \frac{C_I}{C_F}\right)$$

EQ. 30.50

3)

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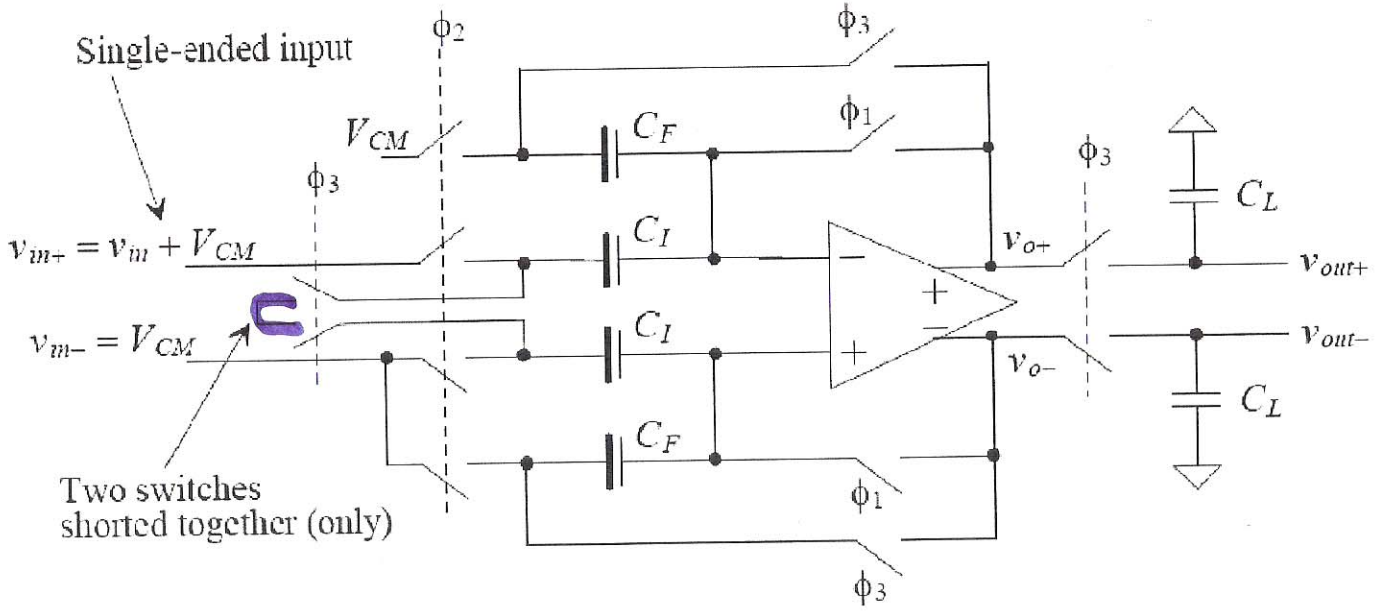

Figure 30.34 Single-ended to differential S/H.

- To be added

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4)

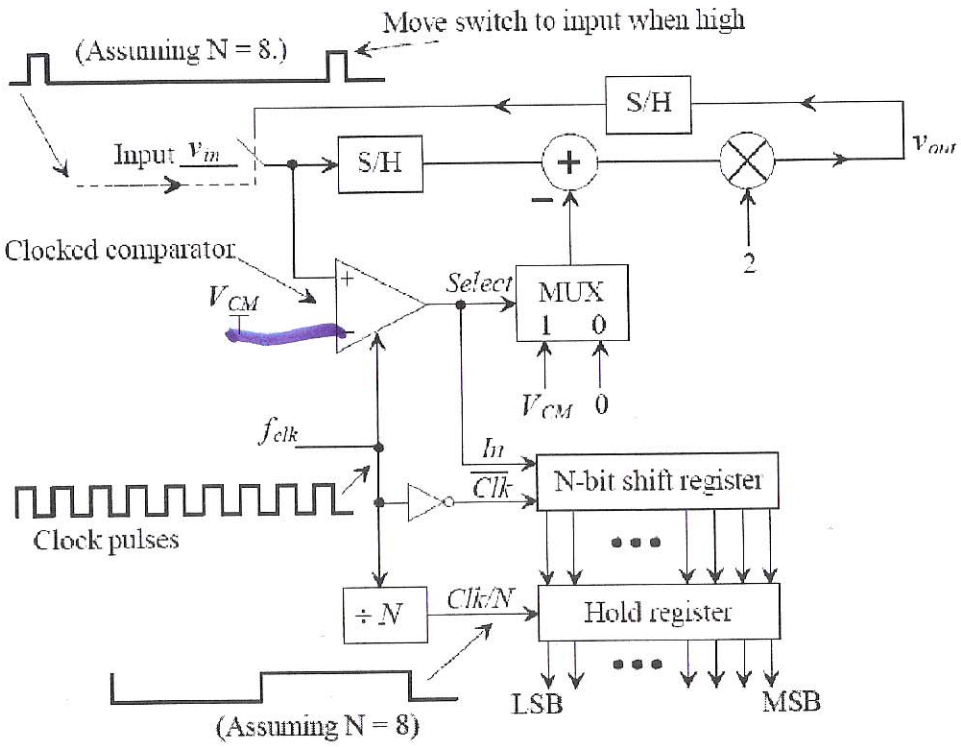

Figure 30.38 Block diagram of a cyclic ADC.

- To be added

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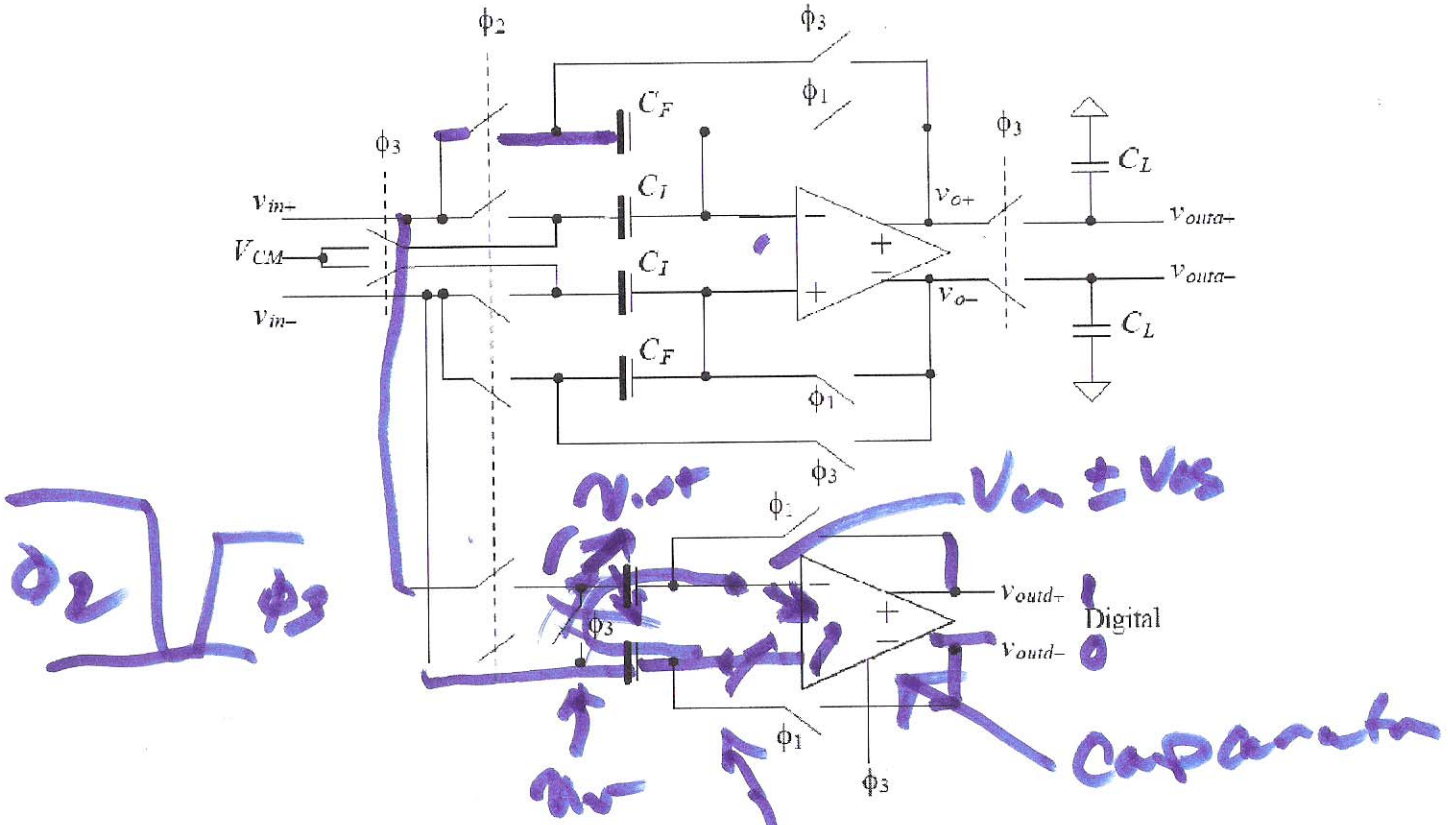

Figure 30.39 Implementation of the comparator with an S/H for use in a cyclic ADC.

- To be added

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VDD = 1V
Vm = ½ V

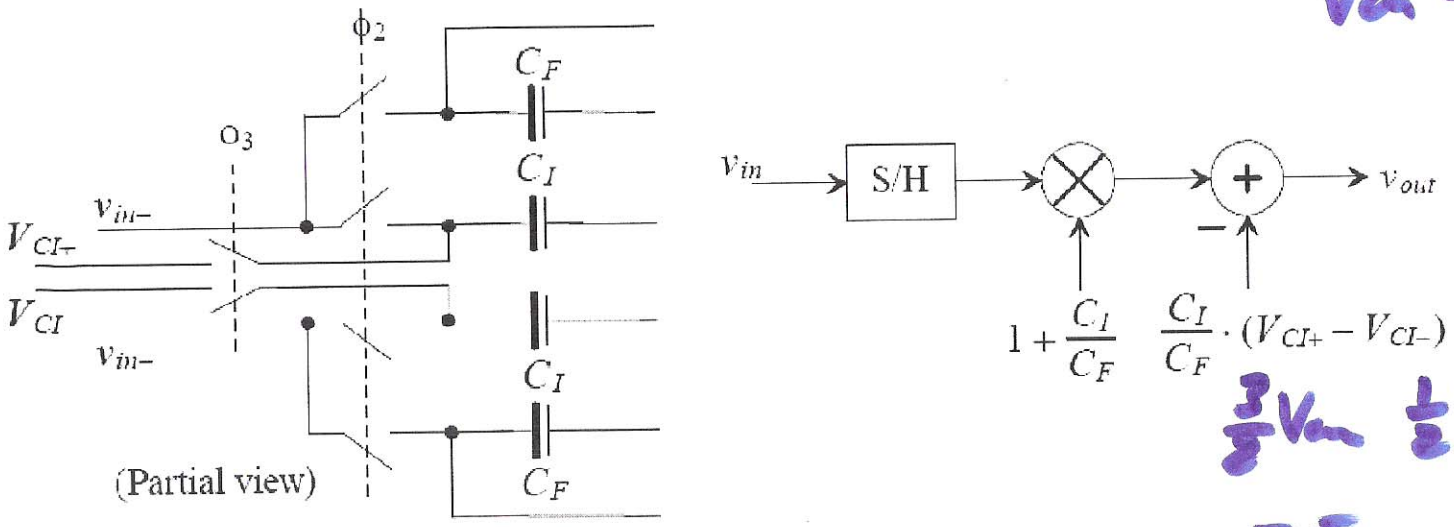

Figure 30.40 Implementing subtraction in the S/H.

¾Vm ½Vm
.75 .25
.5 = Vm

- To be added

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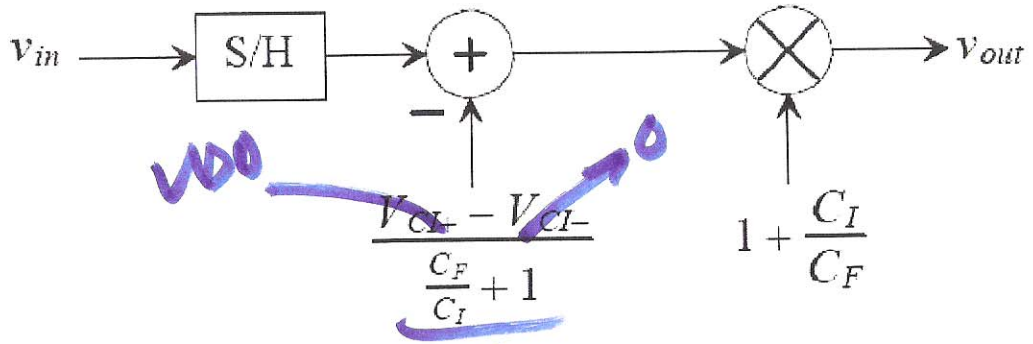

Figure 30.41 Block diagram of Fig. 30.30 with bottom plates of C_I tied to V_{CI}.

- To be added

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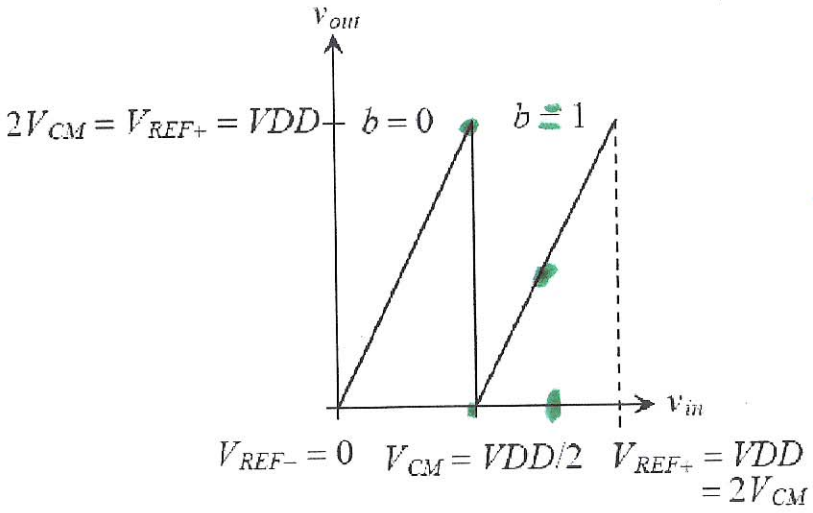

Single-ended

Figure 30.45 Transfer curve for the cyclic ADC (single-ended case).

- To be added

3-bit

VDD = 1

$V_{in} = \frac{1}{2}$

.4V $\frac{b_2}{0}$ $\frac{b_1}{1}$ $\frac{b_0}{1}$

1LSB = $\frac{VDD}{23}$ = .125V

.8
−.5
.3 x2 .6

→ 0.375V

9)

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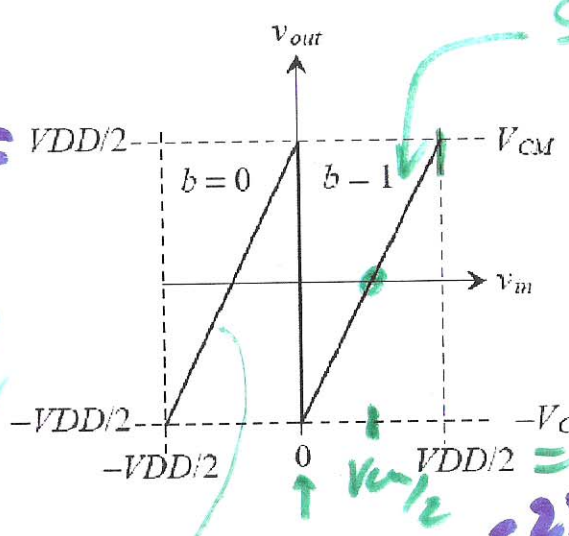

Figure 30.46 Transfer curve for the cyclic ADC when using fully-differential signals.

- To be added

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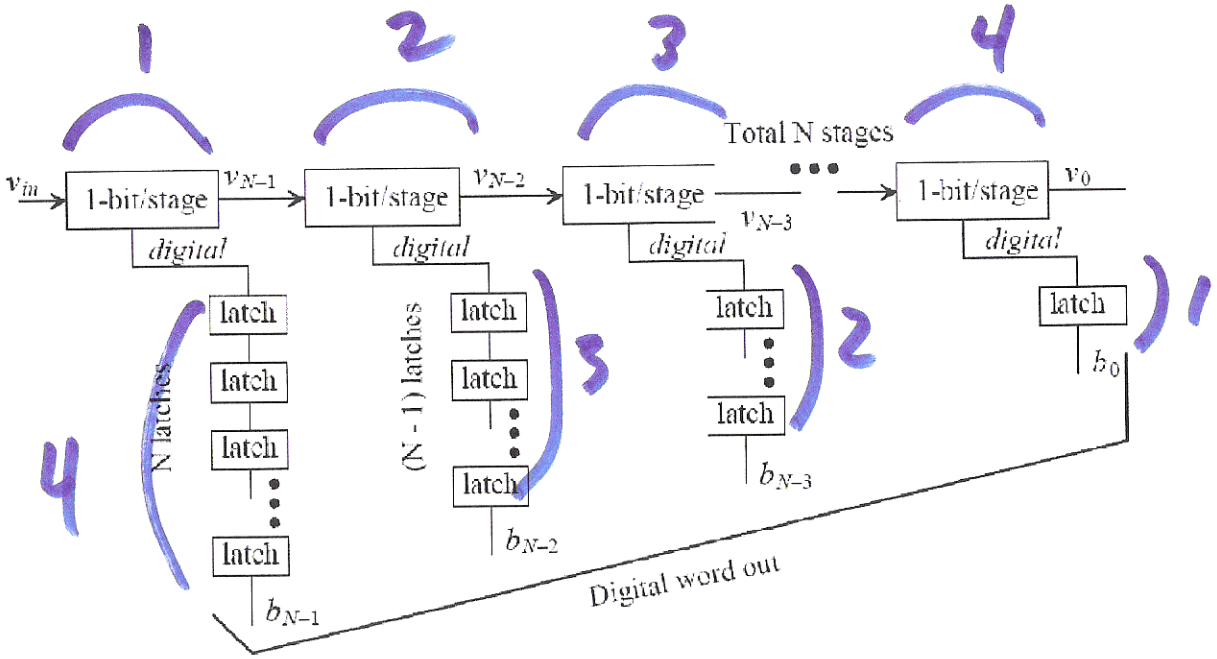

Figure 30.49 Pipelined ADC based on the cyclic stages discussed in the last section.

- To be added

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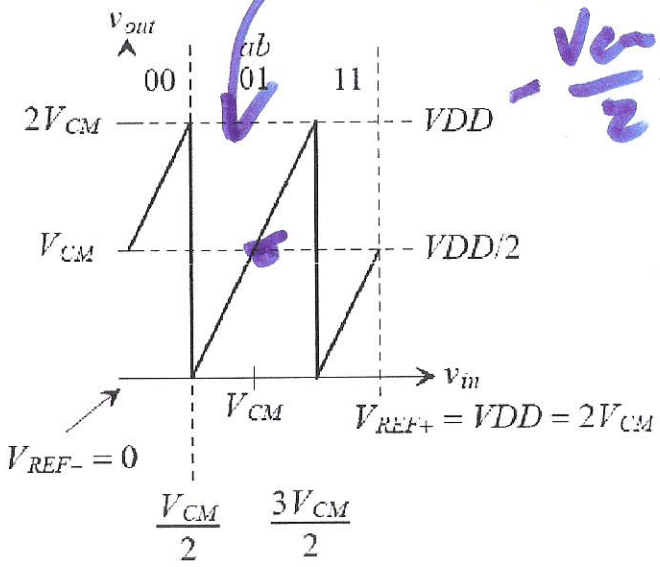
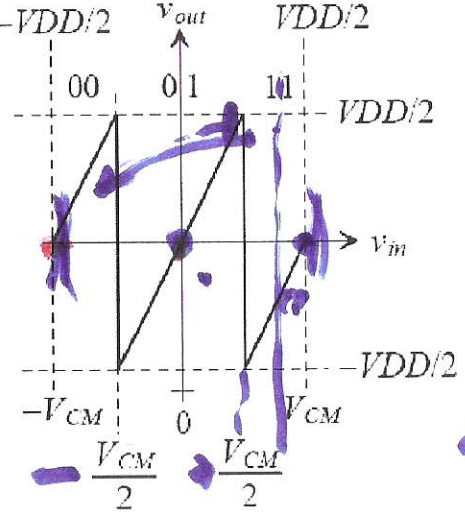


Single-ended input and output



Double-ended input and output

Figure 30.50 Transfer curves for using 1.5-bits per clock cycle.

- To be added

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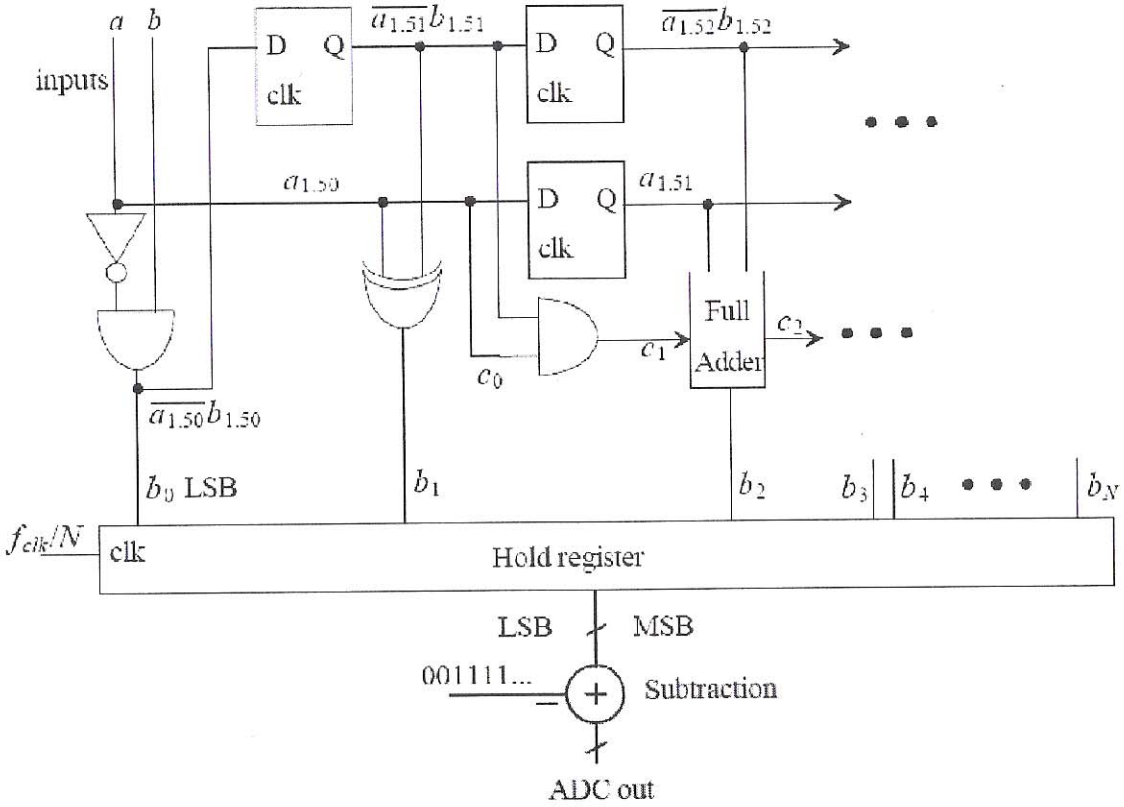

Figure 30.53 Combining the outputs of the cyclic ADC when 1.5 bits/stage is used.

- To be added

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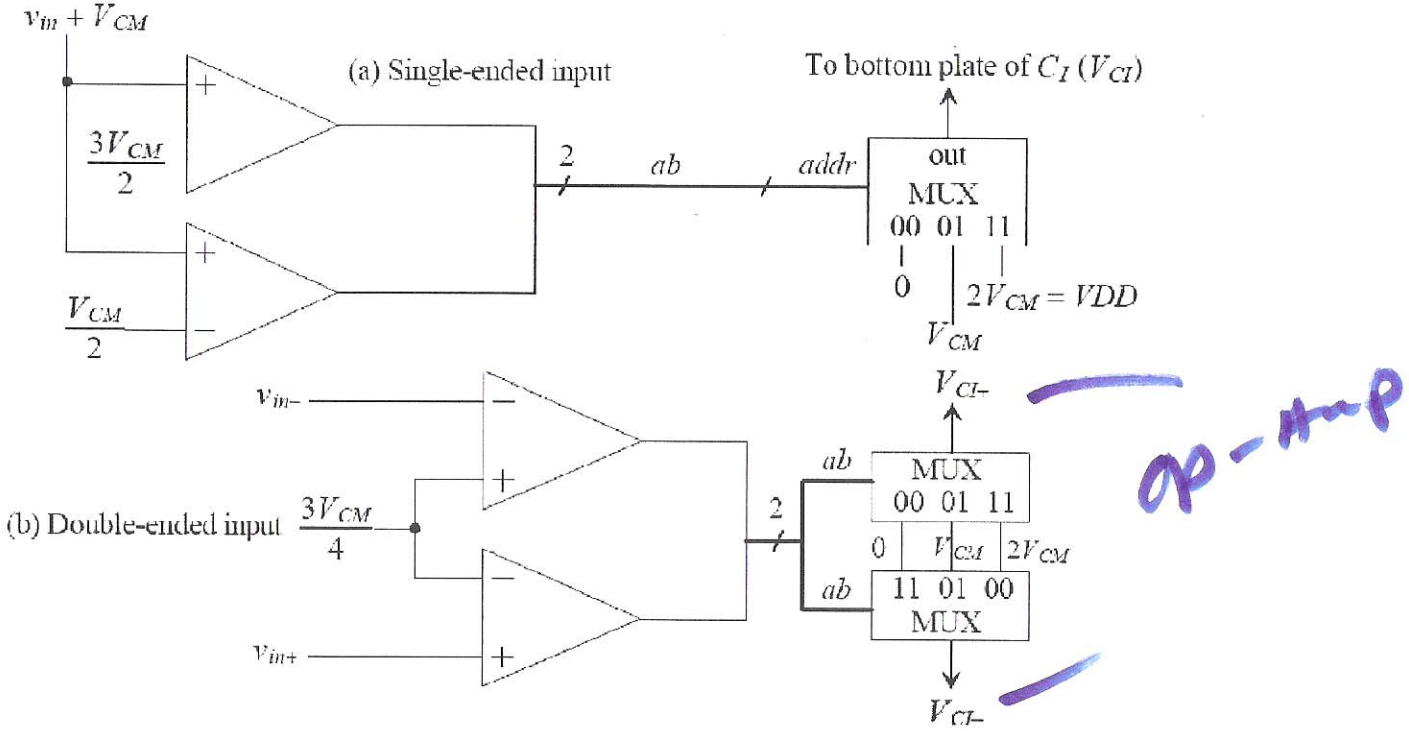

Figure 30.51 Implementing comparators and MUX for 1.5 bits.

- To be added

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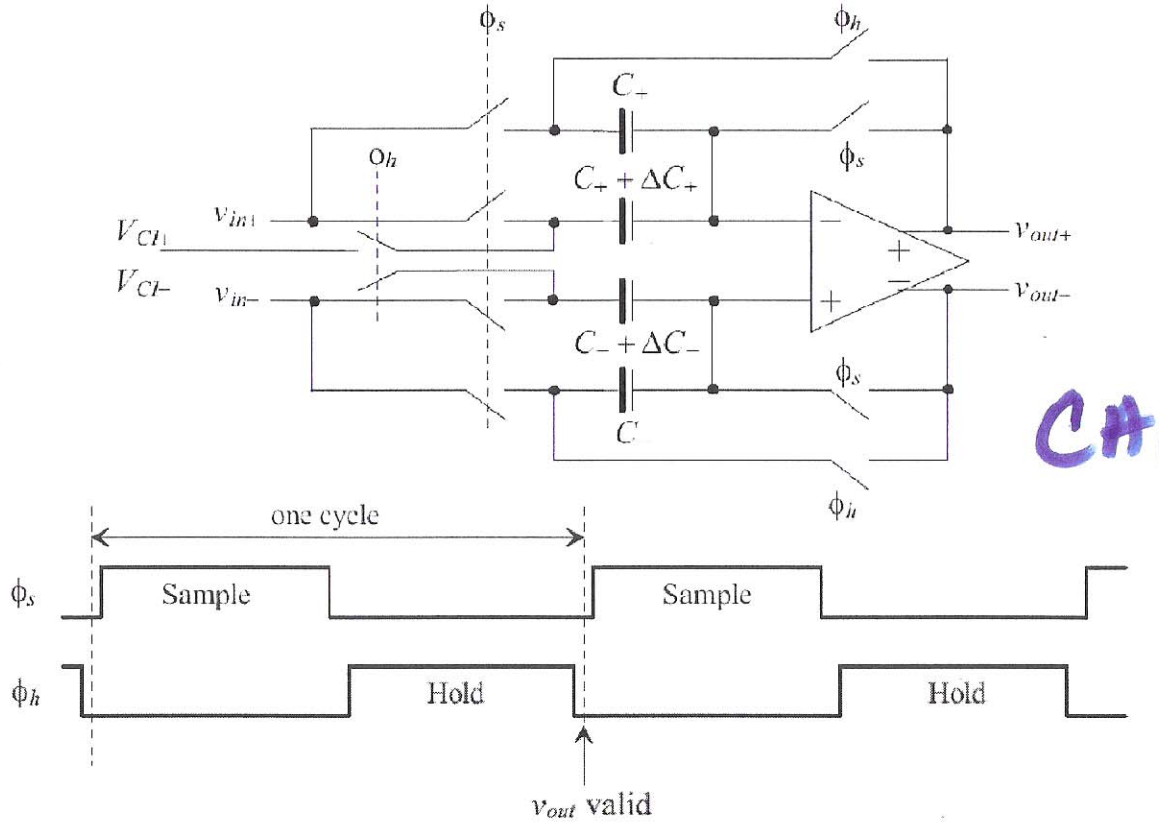

Figure 30.54 S/H of Fig. 30.42 with mismatched capacitors.

Capacitor error averaging

- To be added

15)

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