

Figure 30.30 Data converter S/H building block.

- To be added

$$Q_{I,F_{\pm}}^{\phi_1} = C_{I,F_{\pm}} (V_{in} - V_{cm} \pm V_{os})$$

$$C_I (V_{cm} - V_{cm} \pm V_{os}) + C_F (V_{INT} - V_{cm} \pm V_{os})$$

$$= C_I (V_{in} - V_{cm} \pm V_{os}) + C_F (V_{in} - V_{cm} \pm V_{os})$$

$$2C_I v_{in} - C_F v_{out} = 0$$

$$v_{out} = \frac{C_F}{C_I} v_{in}$$

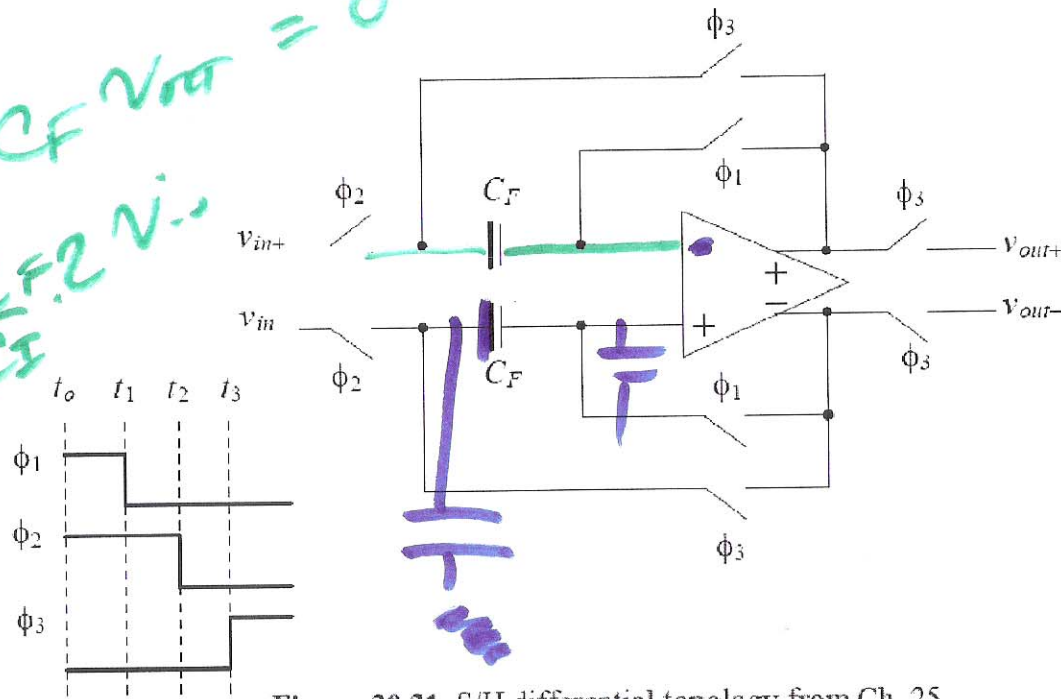


Figure 30.31 S/H differential topology from Ch. 25.

• To be added

$$v_{out} = v_{out+} - v_{out-}$$

$$v_{in} = v_{in+} - v_{in-}$$

$$C_I (v_{in+} - v_{in-}) - C_F (v_{out+} - v_{out-}) = 0$$

$$C_I \cdot v_{in} + C_F \cdot v_{out} - C_I v_{in+} - C_F \cdot v_{out+} = 0$$

$$C_I (-v_{in+} + v_{in}) + C_F (v_{out+} - v_{out}) = 0$$

$$C_I (-v_{in-} + v_{in}) + C_F (v_{out-} - v_{out}) = 0$$

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$$C_F (v_{out+} - v_{out-}) = (v_{in+} - v_{in-}) C_F$$

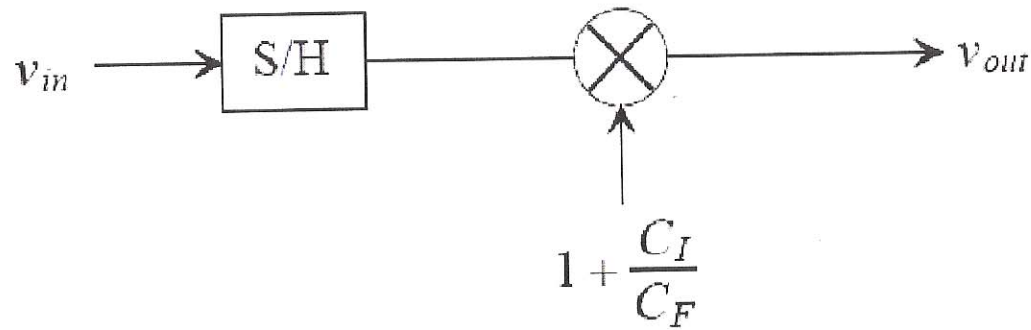


Figure 30.32 Block diagram for the S/H of Fig. 30.30.

- To be added

$$C_I(v_{in}) - C_F v_{out} + C_F v_{in} = 0$$

$$(C_I + C_F)v_{in} = C_F \cdot v_{out}$$

$$\frac{v_{out}}{v_{in}} = \left(1 + \frac{C_I}{C_F}\right)$$

EQ. 30.50

3)

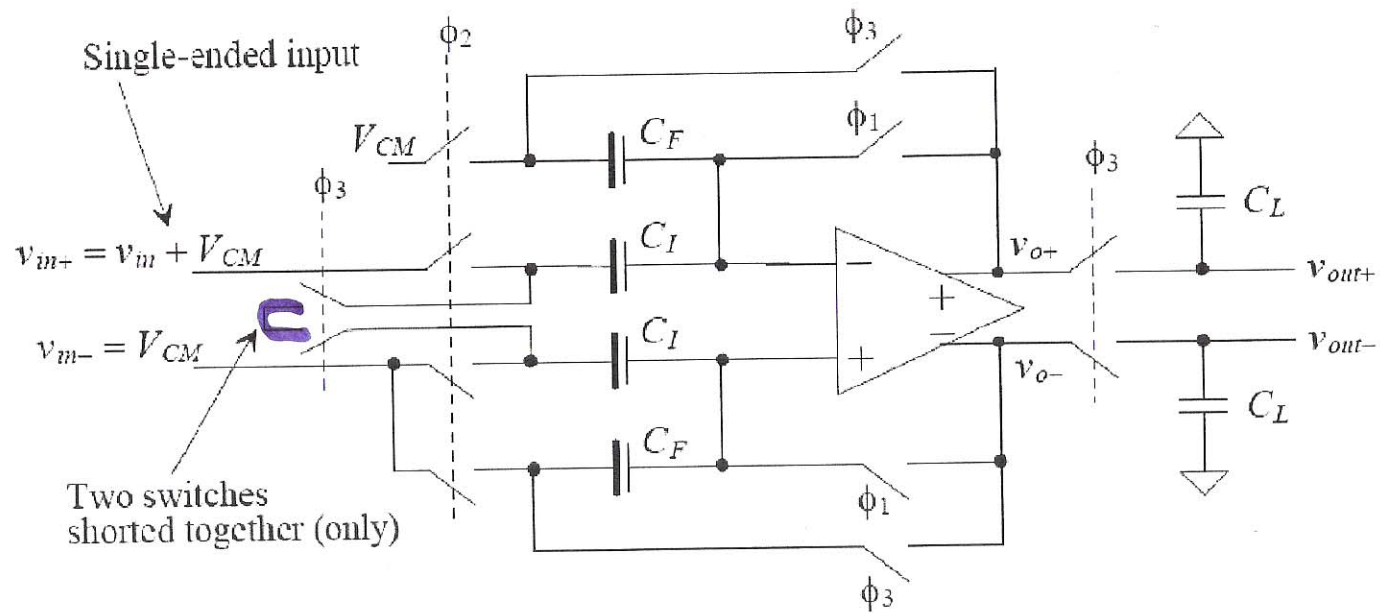


Figure 30.34 Single-ended to differential S/H.

- To be added

4)

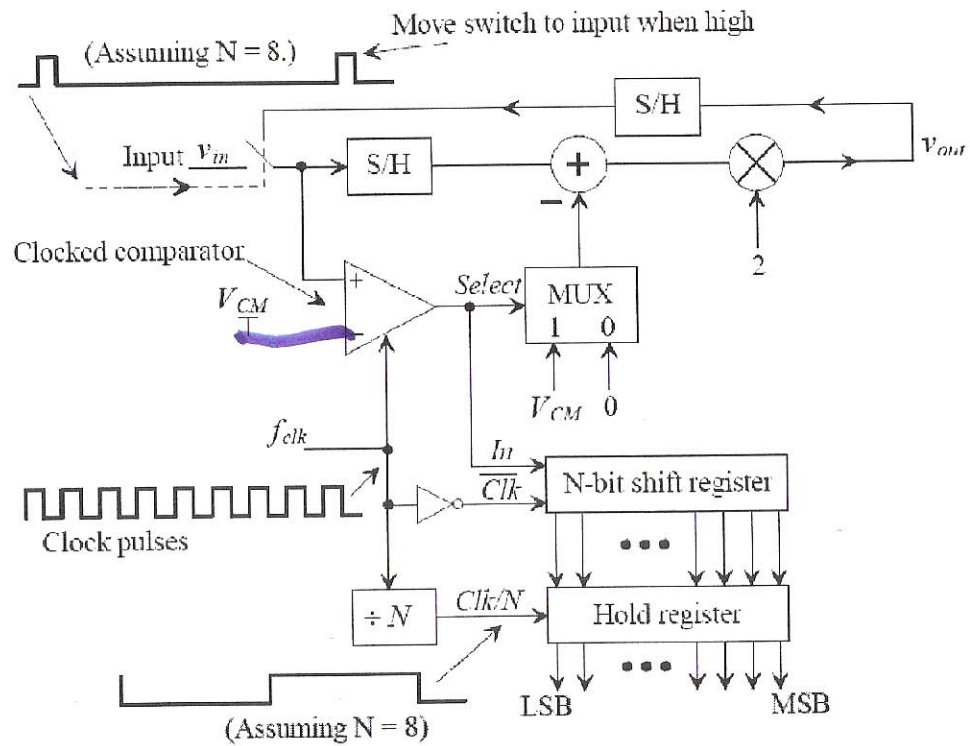


Figure 30.38 Block diagram of a cyclic ADC.

- To be added



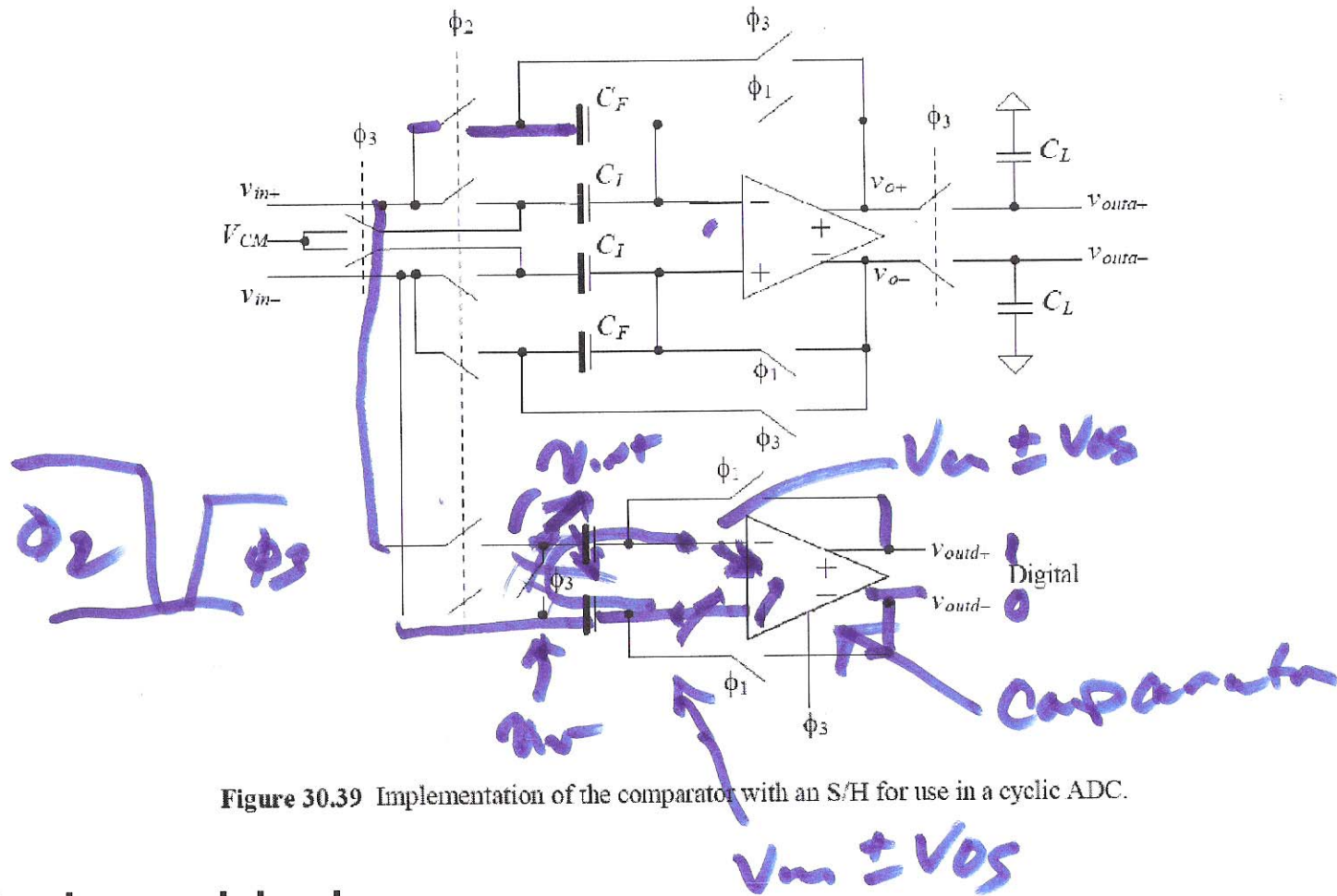
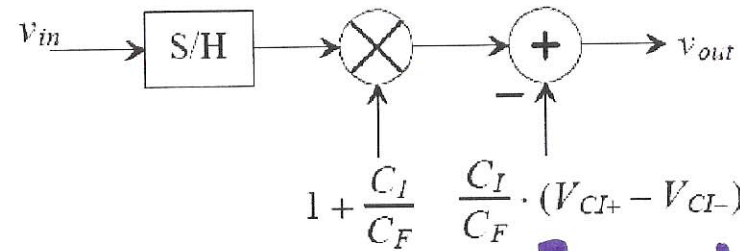
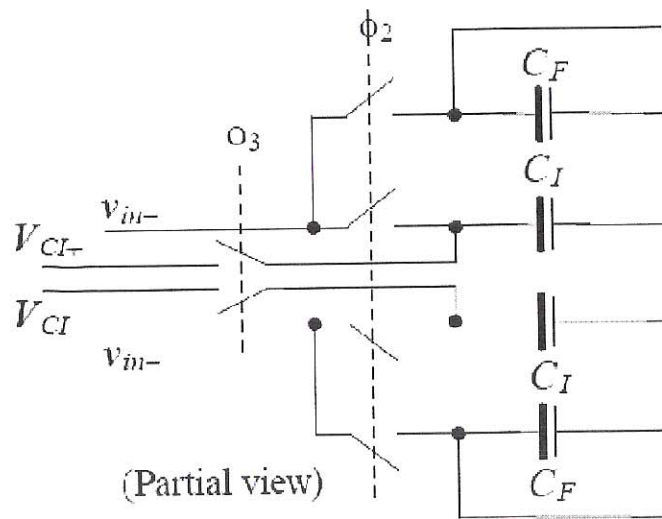


Figure 30.39 Implementation of the comparator with an S/H for use in a cyclic ADC.

- To be added



$V_{DD} = 1V$
 $V_{in} = \frac{1}{2}V$

$1 + \frac{C_I}{C_F}$
 $\frac{C_I}{C_F} \cdot (V_{CI+} - V_{CI-})$
 $\frac{3}{8}V_{in} \quad \frac{1}{8}V_{in}$
 $.75 \quad .25$
 $.5 = V_{in}$

Figure 30.40 Implementing subtraction in the S/H.

- To be added



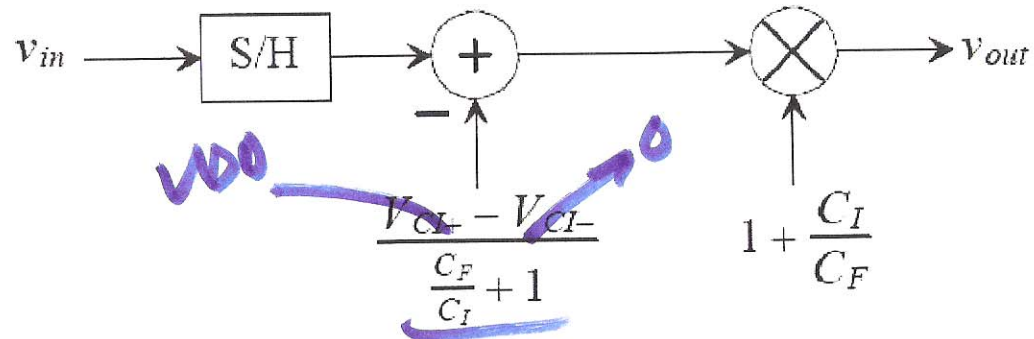
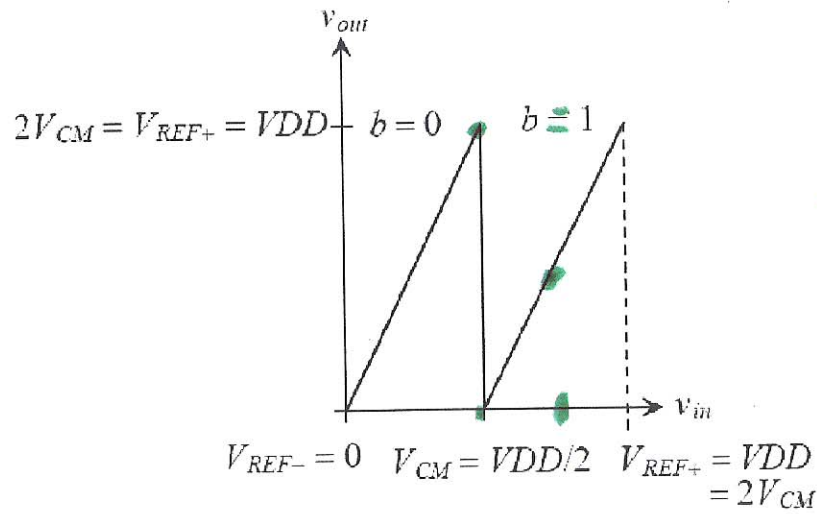


Figure 30.41 Block diagram of Fig. 30.30 with bottom plates of C_I tied to V_{CI} .

- To be added

8)



Single-ended

Figure 30.45 Transfer curve for the cyclic ADC (single-ended case).

• To be added

3-bit

$V_{DD} = 1$

$V_{CM} = \frac{1}{2}$

$.4V$ $\frac{b_2}{0}$ $\frac{b_1}{1}$ $\frac{b_0}{1}$

$1LSB = \frac{V_{DD}}{2^3} = .125V$

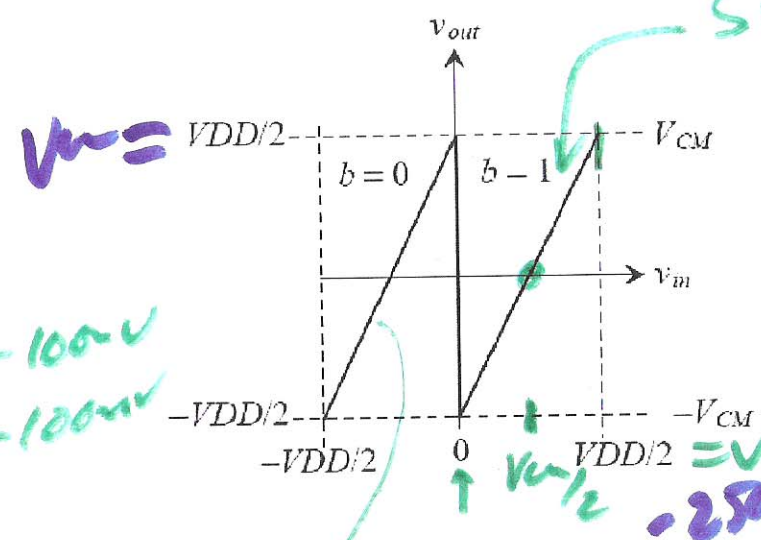
$\begin{array}{r} .8 \\ -.5 \\ \hline .3 \times 2 \end{array} .6$

0.375V

a)

$V_{in} = -0.1V$
 $v_{out+} = 0.45$
 $v_{out-} = 0.55$

$v_{in} = .2$
 $v_{out+} = 0.6 = v_{in} + 100\mu V$
 $v_{out-} = 0.4 = v_{in} - 100\mu V$



$V_{CM} = 250\mu V$
 $\frac{V_{CM}}{2} = 625\mu V$
 $v_{out+} = 375\mu V$
 $v_{out-} = 375\mu V$
 $v_{out+} = 625\mu V$
 $v_{out-} = 625\mu V$

Figure 30.46 Transfer curve for the cyclic ADC when using fully-differential signals.

- To be added

$v_{in} = -1$
 $v_{out+} = 0$
 $v_{out-} = VDD$
 $v_{in} = +1$
 $v_{out+} = VDD$
 $v_{out-} = 0$

$250\mu V - 250\mu V = 0$
 $v_{out+} = v_{in} = V_{in}$
 $(625 - 375) + (375 - 625) - 250 = 0$
 250

10)

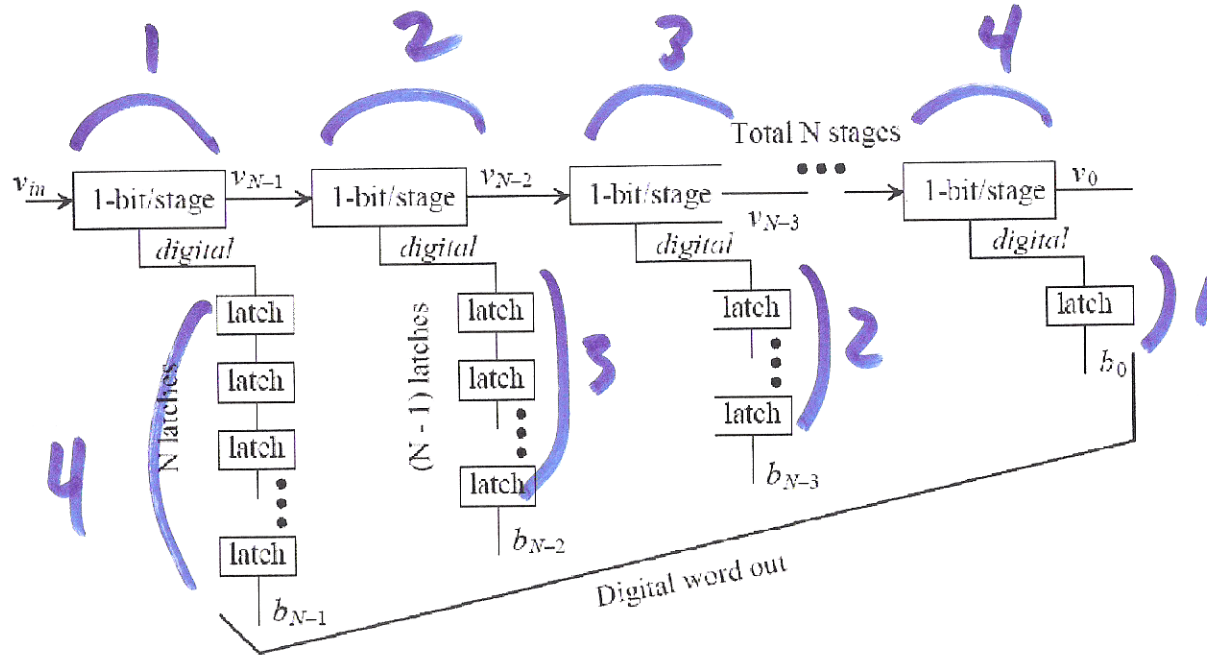
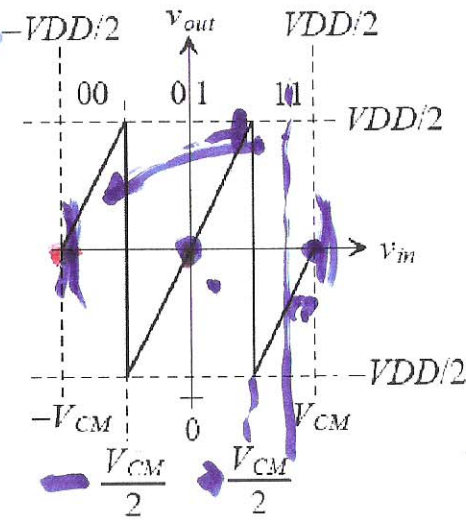
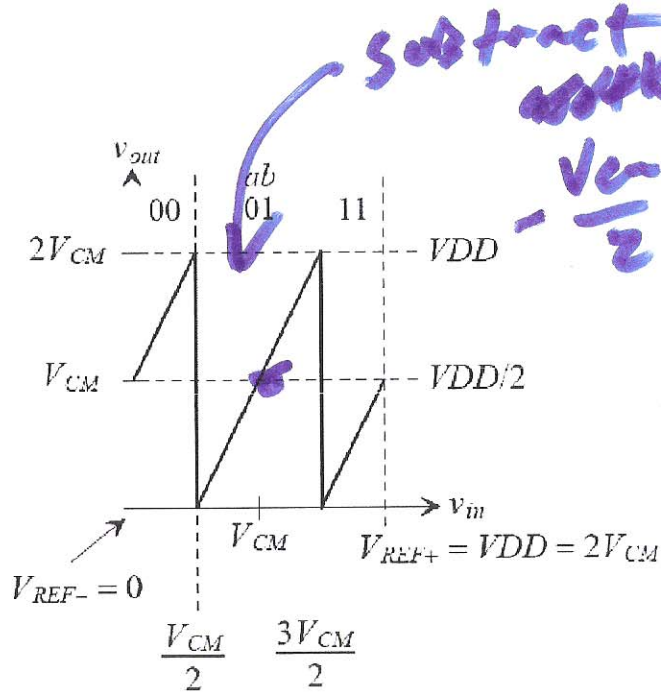


Figure 30.49 Pipelined ADC based on the cyclic stages discussed in the last section.

- To be added

11)



Single-ended input and output

Double-ended input and output

Figure 30.50 Transfer curves for using 1.5-bits per clock cycle.

00000 → 0
 01111 → V_CM
 11111 → V_DD - 1LSB

- To be added

11
 01
 01
 01
 01

1111

01
 01
 01

0111

1100
 1100
 1100

0101

00000
 $V_{int} = 750\mu V$
 $V_{w-} = 250\mu V$
 $V_{in} = V_{CM} = 0.5V$

12)

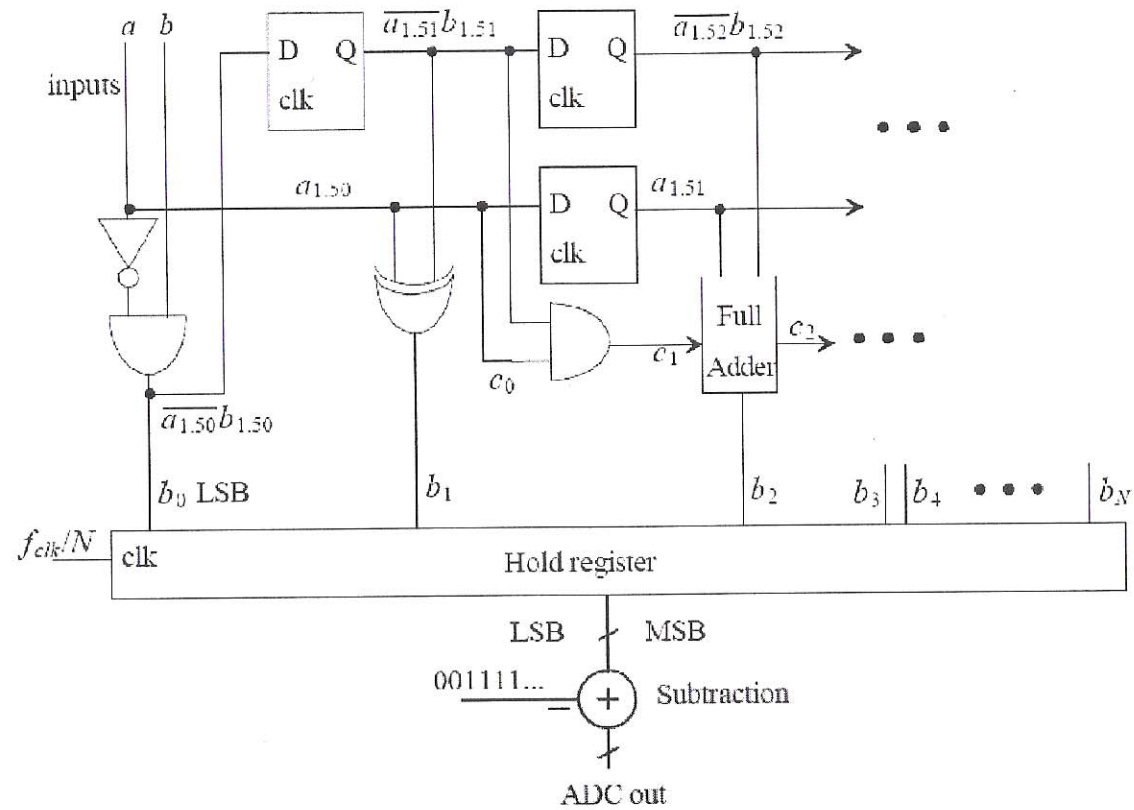


Figure 30.53 Combining the outputs of the cyclic ADC when 1.5 bits/stage is used.

- To be added

13)

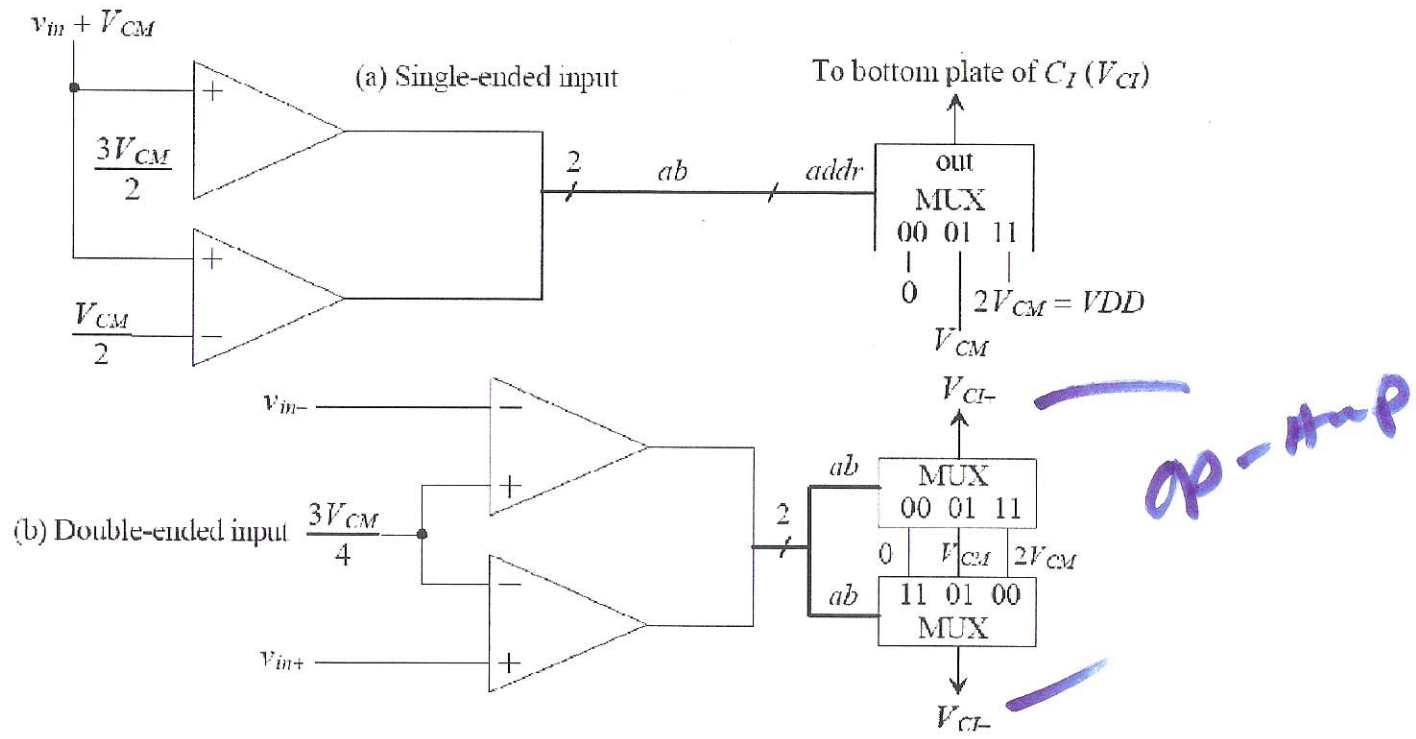
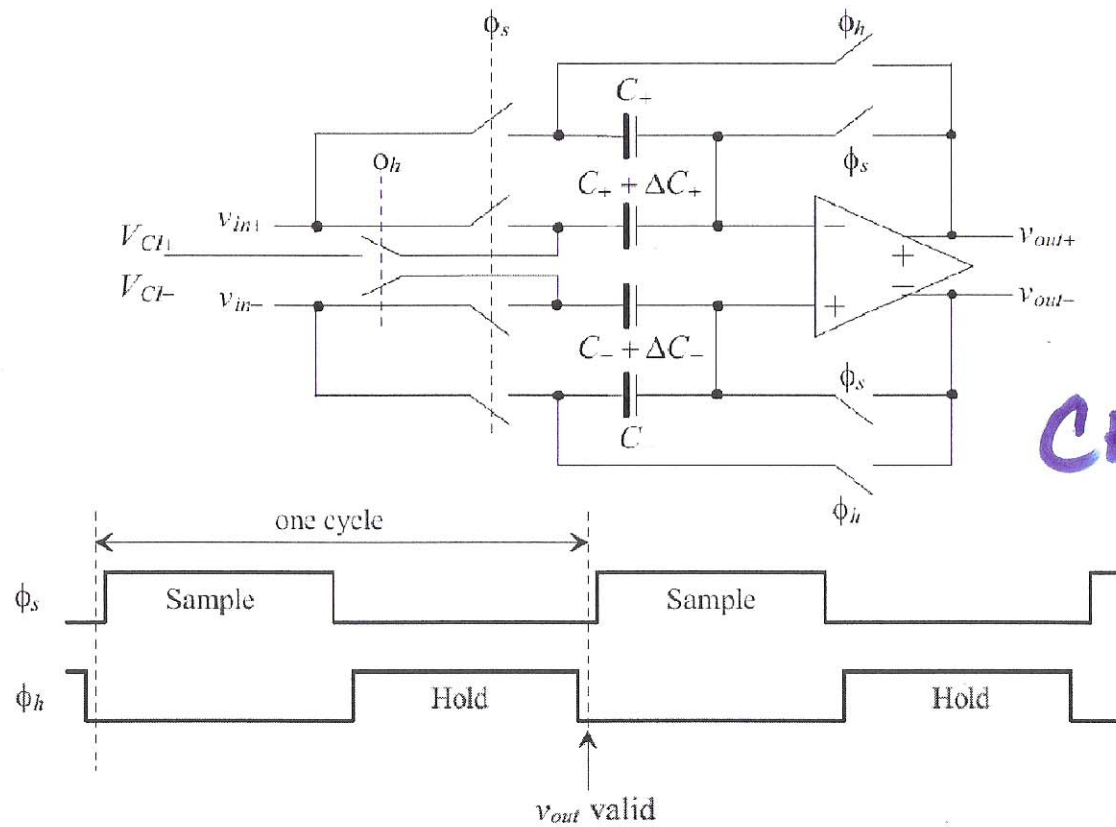


Figure 30.51 Implementing comparators and MUX for 1.5 bits.

- To be added

14)



Capacitor error averaging

Figure 30.54 S/H of Fig. 30.42 with mismatched capacitors.

- To be added

15)