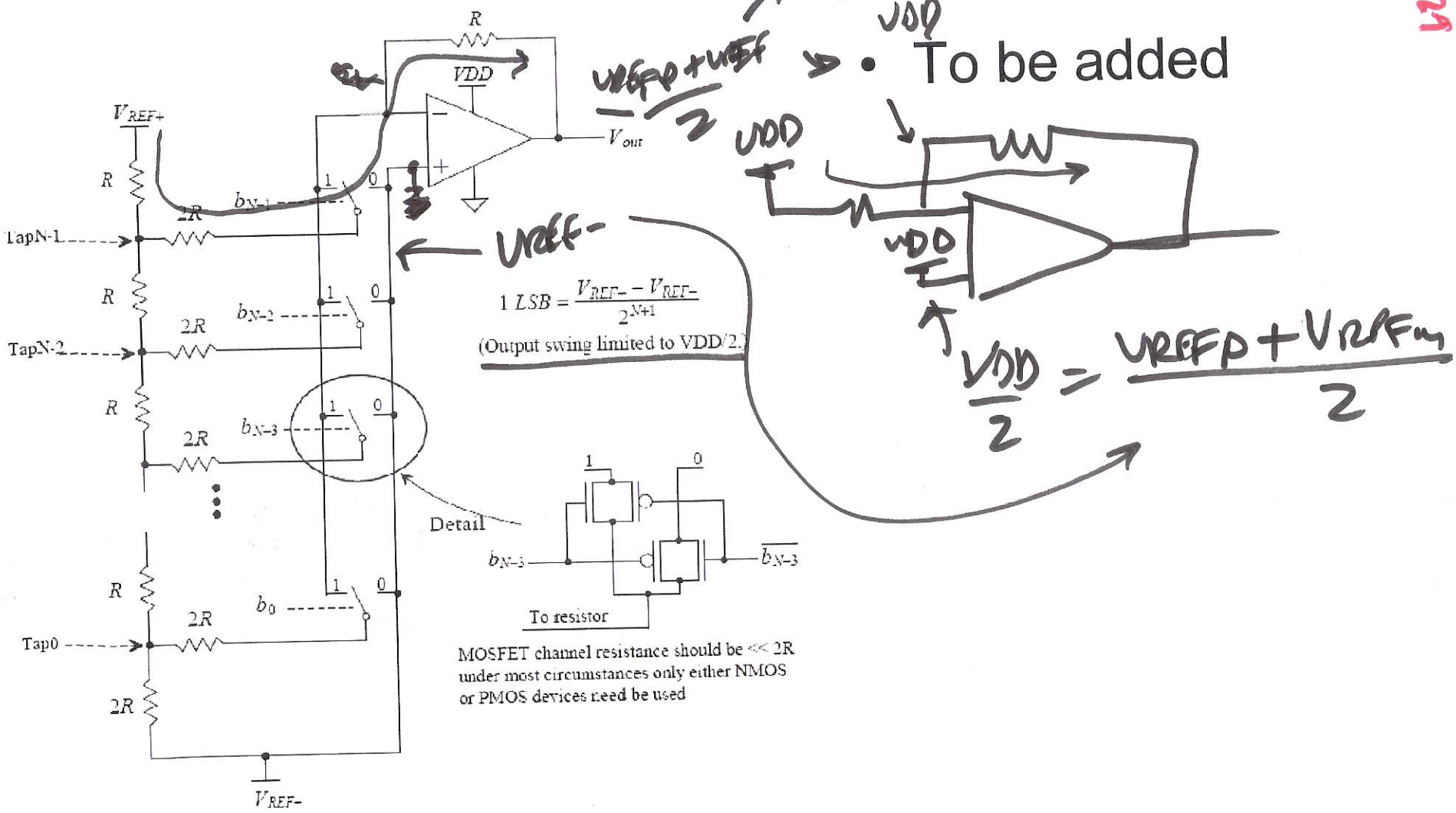


Figure 30.1 Traditional current-mode R-2R DAC.

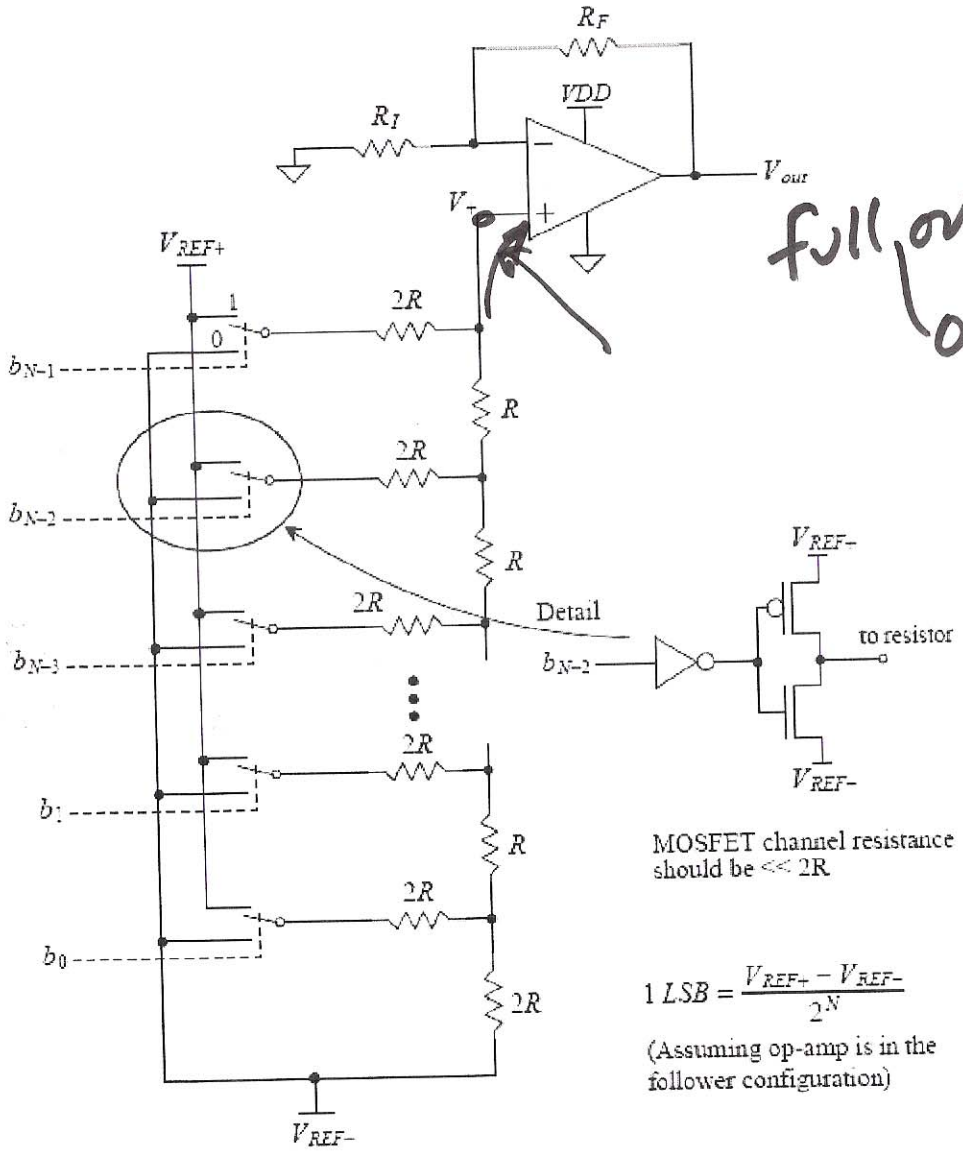


Figure 30.2 Traditional voltage-mode R-2R DAC.

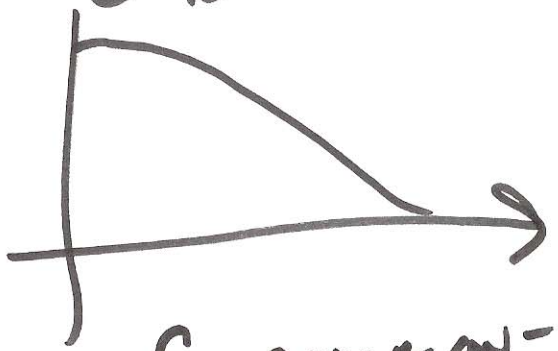
- To be added

full output swing
0 → VDD

common mode voltage

$V_{OS} = \frac{\Delta V_c}{CMRR}$

CMRR



Bad if common-mode voltage on op-amp inputs varies

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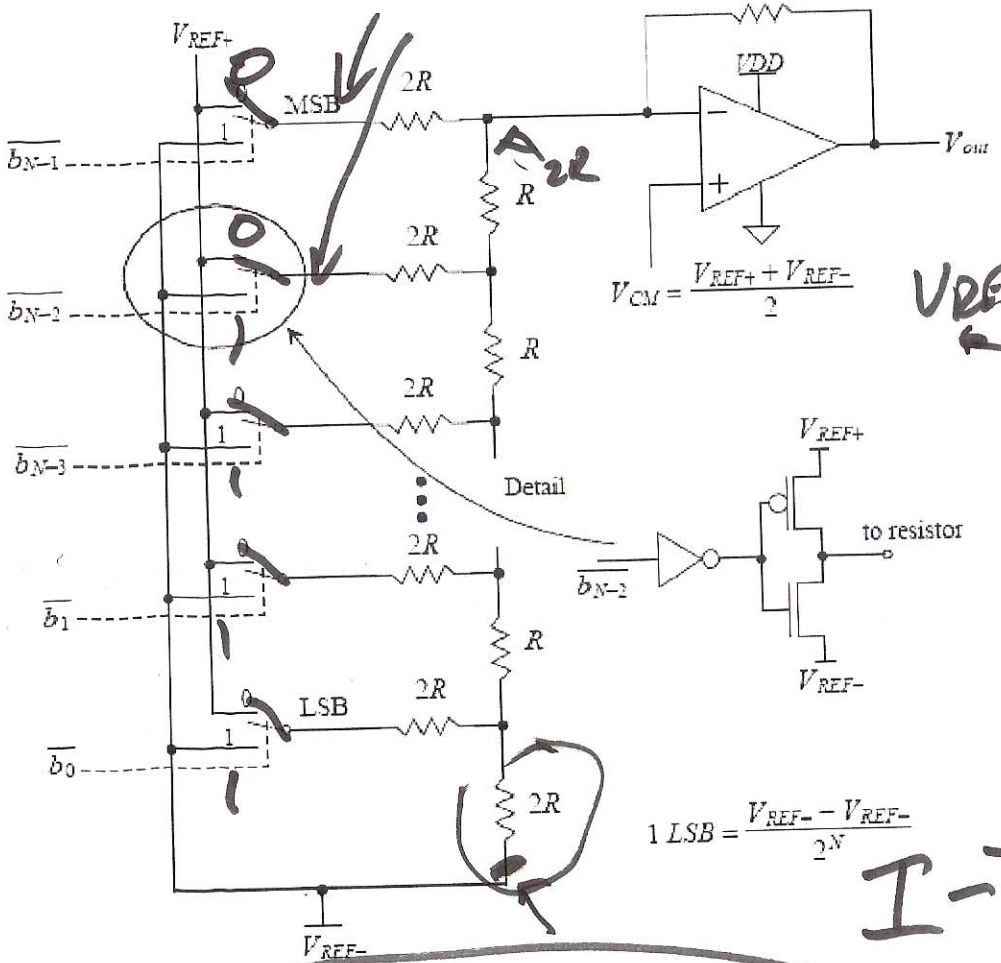


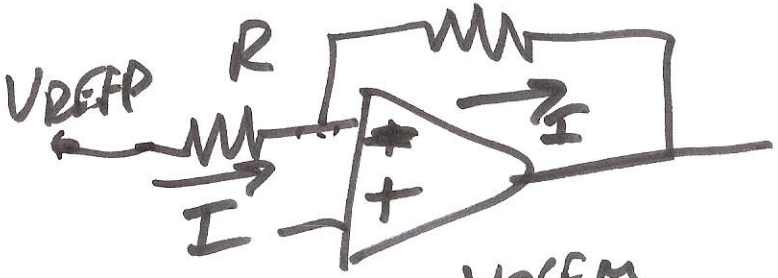
Figure 30.3 Wide-swing current-mode R-2R DAC.

VREFP

VREFm + 1LSB

- To be added

VREFP − 1LSB



$\frac{VREFP + VREFm}{2}$

$I = \frac{VREFP - \frac{VREFP}{2} - \frac{VREFm}{2}}{R}$

$-I \cdot R + \frac{VREFP + VREFm}{2}$

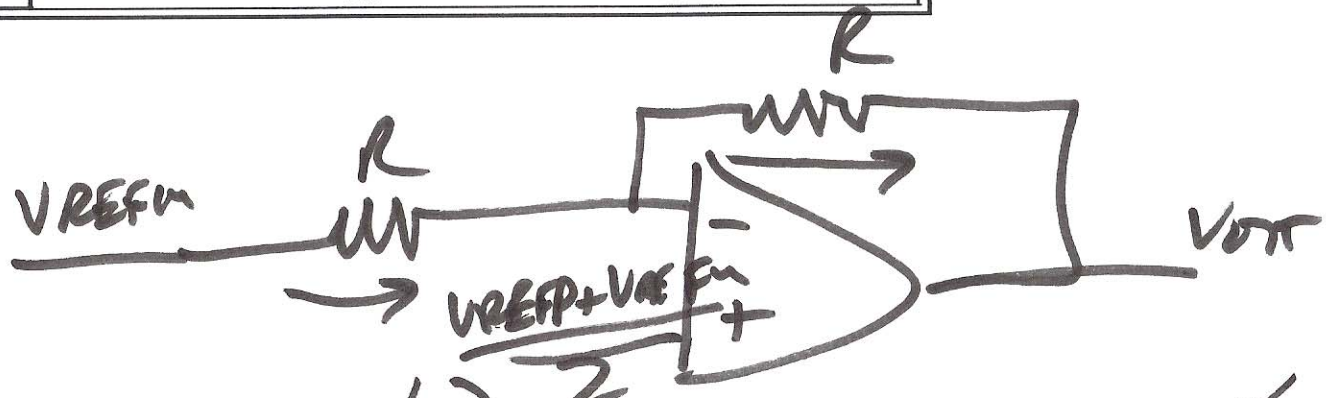
$I = \frac{VREFP - VREFm}{-\frac{VREFP}{2} + \frac{VREFm}{2} + \frac{2R}{2} + \frac{VREFP}{2} + \frac{VREFm}{2}}$

3)

Table 30.1 Summary of experimental results.

	8-bit	10-bit	12-bit
DNL (LSB)	0.150	0.450	2.000
INL (LSB)	0.200	1.000	3.000
Settling time	200 ns		
Power	3.88 mW (driving a 1k load)		
Area (mm^2)	0.045		
$f_{clk,max}$	4 MHz		
Output swing	$0 < V_{out} < VDD\ (= 1.8\ V)$		

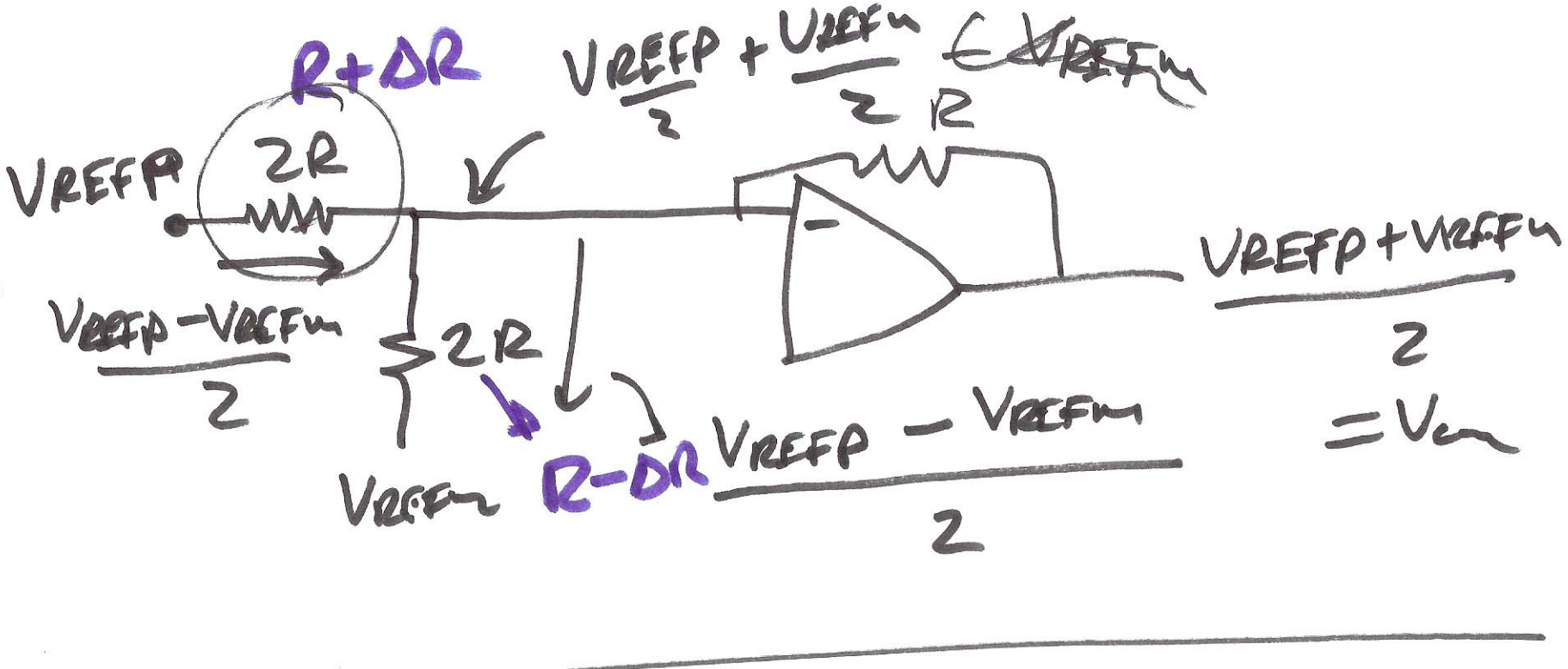
- To be added



$$V_{OUT} = -\left(V_{REFm} - \frac{V_{REFP} - V_{REFm}}{2}\right)\cdot\frac{R}{R} + \frac{V_{REFP} + V_{REFm}}{2}$$

$$V_{OUT} = V_{REFP}$$

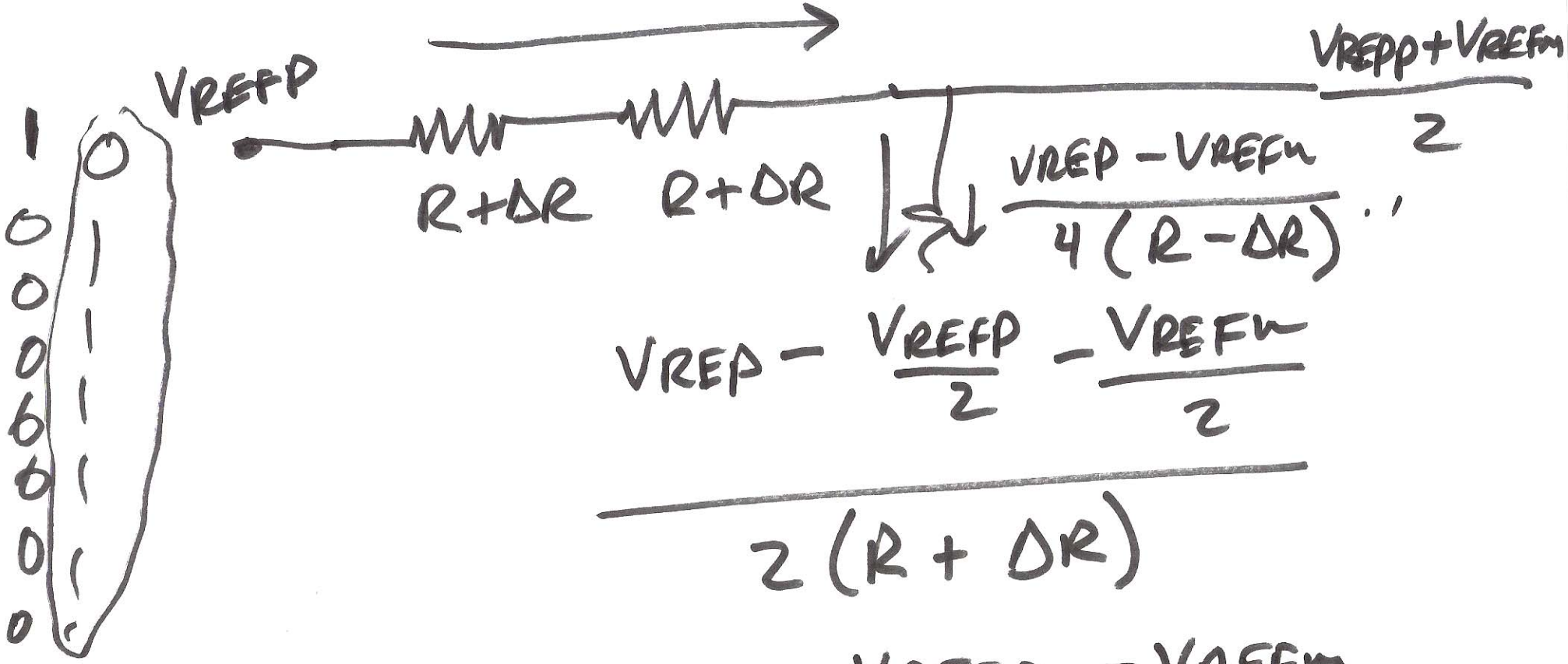
4)



6

D.N.L Analysis:

$$\frac{V_{REFP} - V_{REF}}{2(R+\Delta R)}$$



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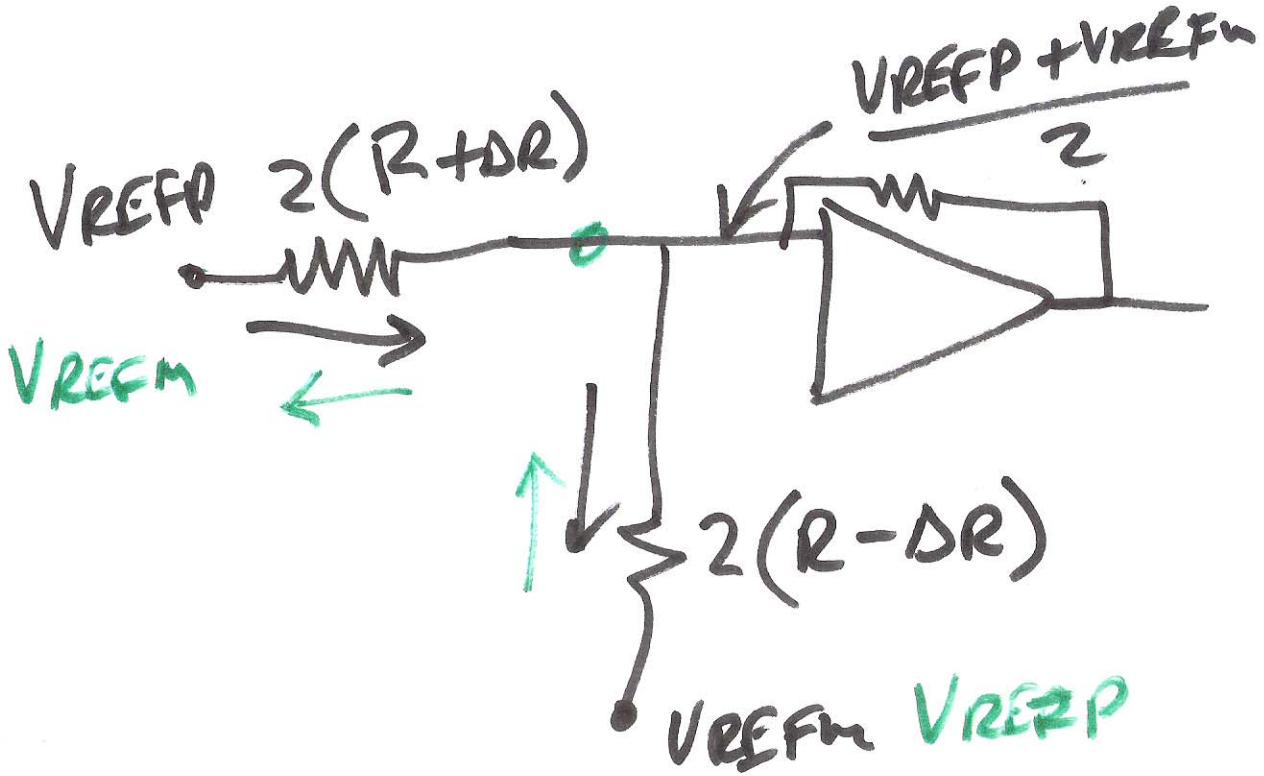
$$\Delta I = \frac{V_{REF+} - V_{REF-}}{4(R-\Delta R)} - \frac{V_{REF+} - V_{REF-}}{4(R+\Delta R)}$$



$$\Delta I$$

$$\frac{V_{REFP} - V_{REFm}}{2(2(R+\Delta R))} \mp \frac{V_{REFP} - V_{REFm}}{2(2(R \mp \Delta R))} +$$

$$+ \frac{V_{REFP} - V_{REFm}}{2(2(R+\Delta R))} \mp \frac{V_{REFP} - V_{REFm}}{2(2(R-\Delta R))}$$

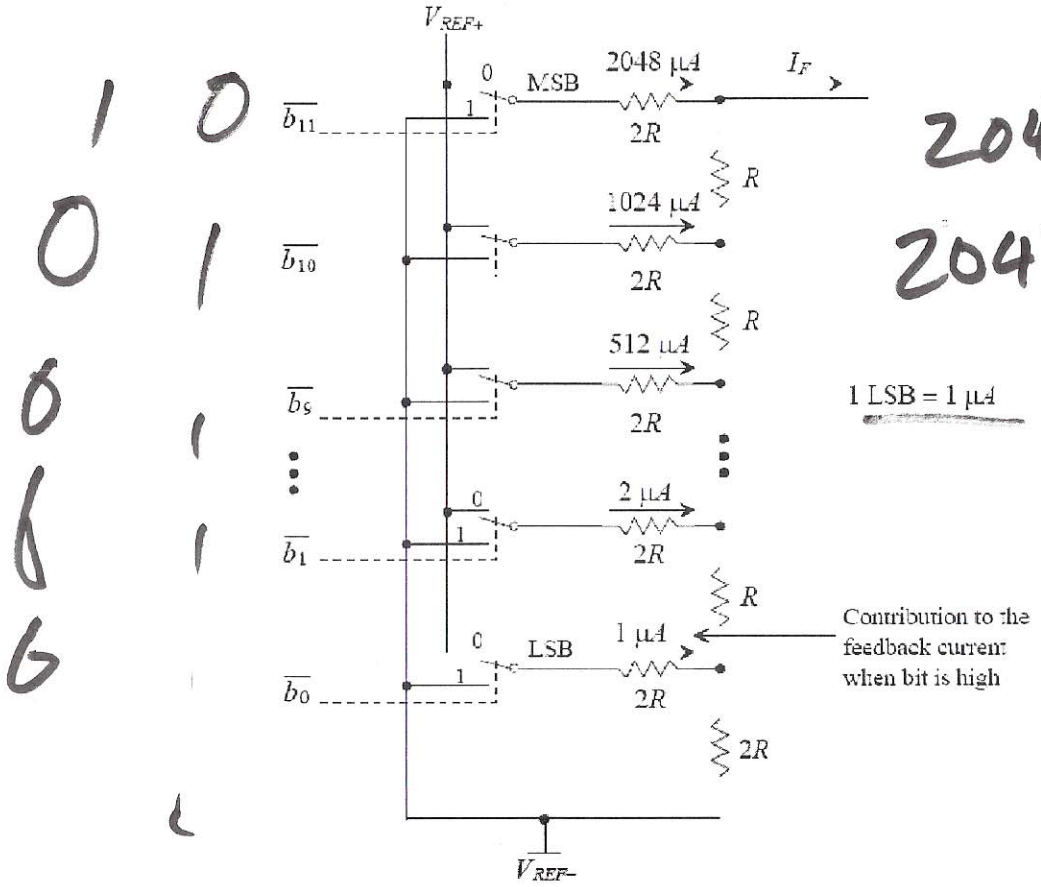


Figure 30.5 Showing how currents sum into the feedback current.

- To be added

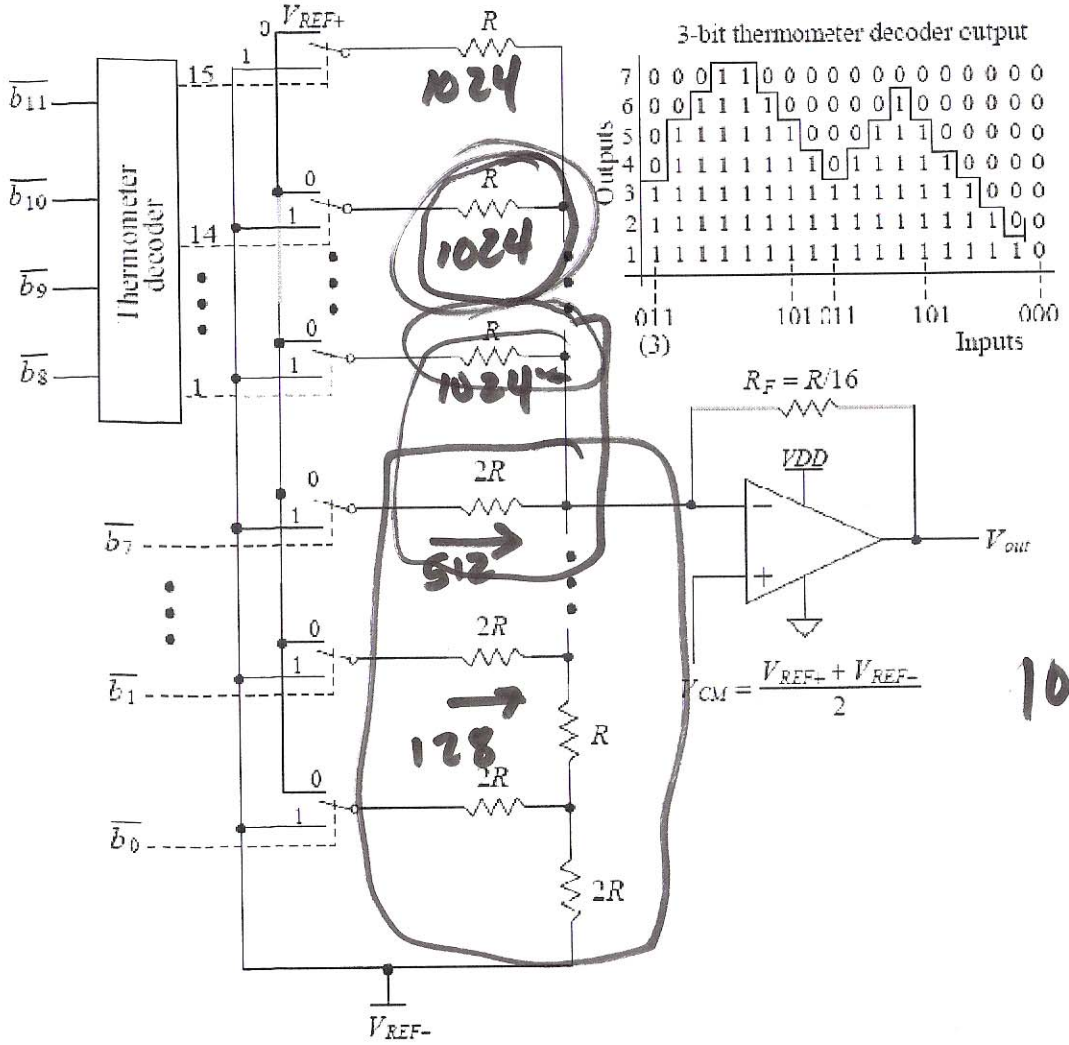


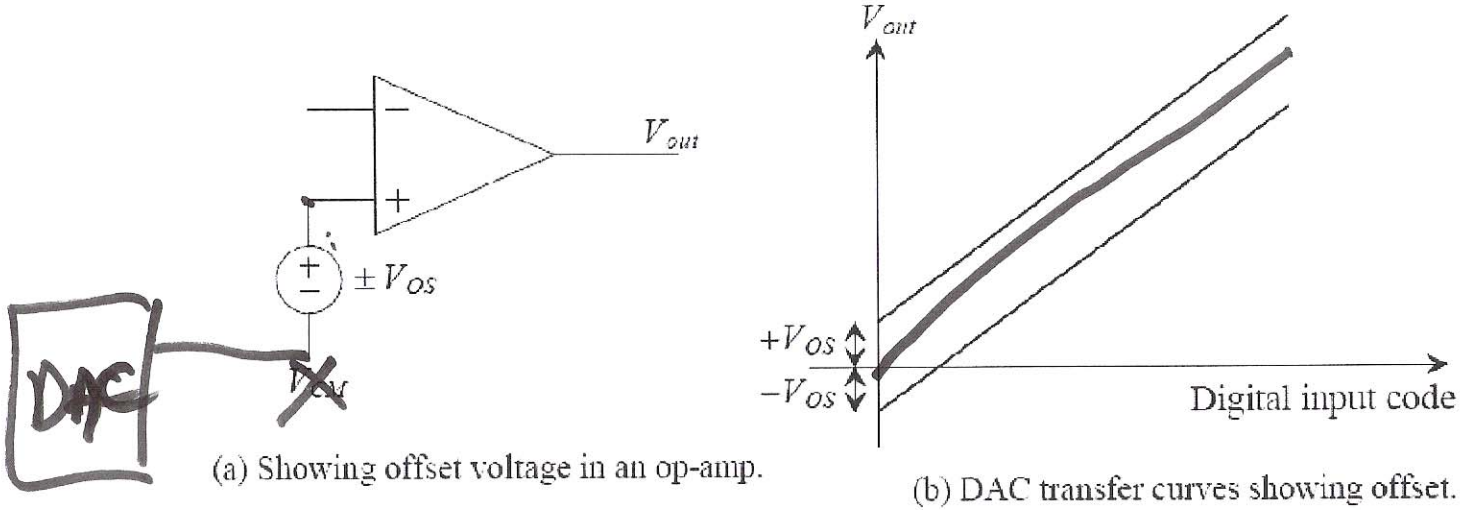
Figure 30.6 Segmentation in a wide-swing R-2R DAC.

- To be added

1023 → 1024

2047 → 2048

helps DNL but no help for INL

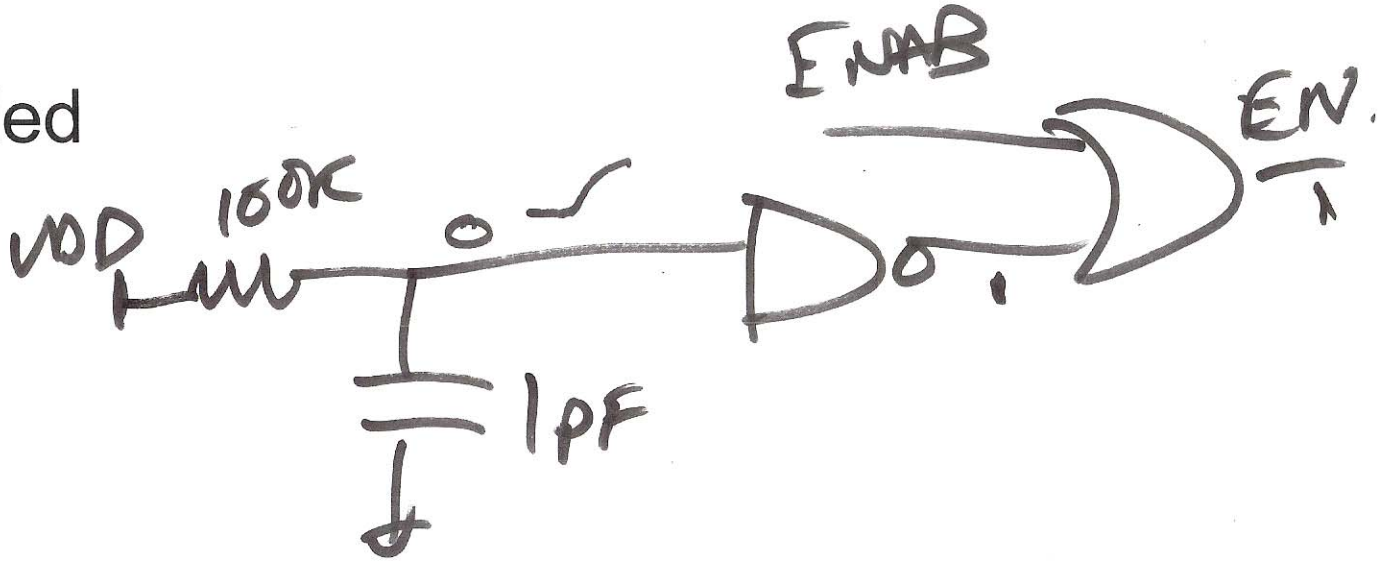


(a) Showing offset voltage in an op-amp.

(b) DAC transfer curves showing offset.

Figure 30.7 Showing how an op-amp offset affects the DACs transfer curves.

- To be added



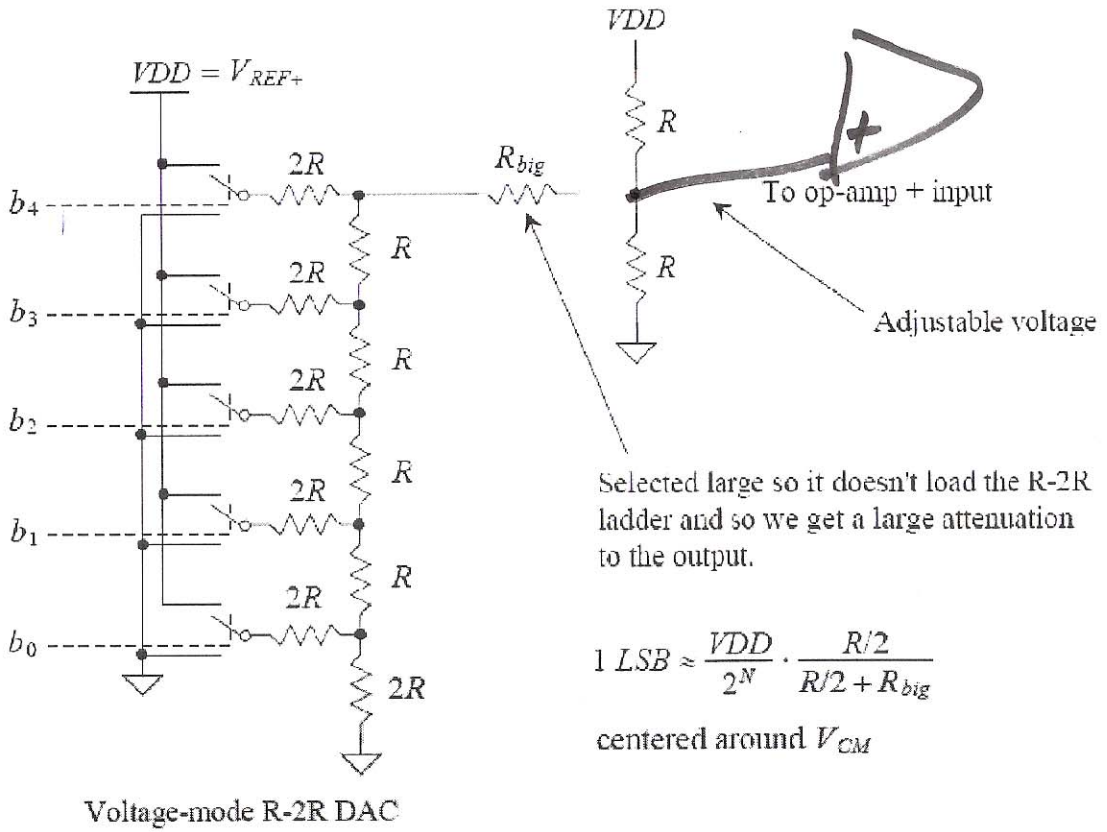
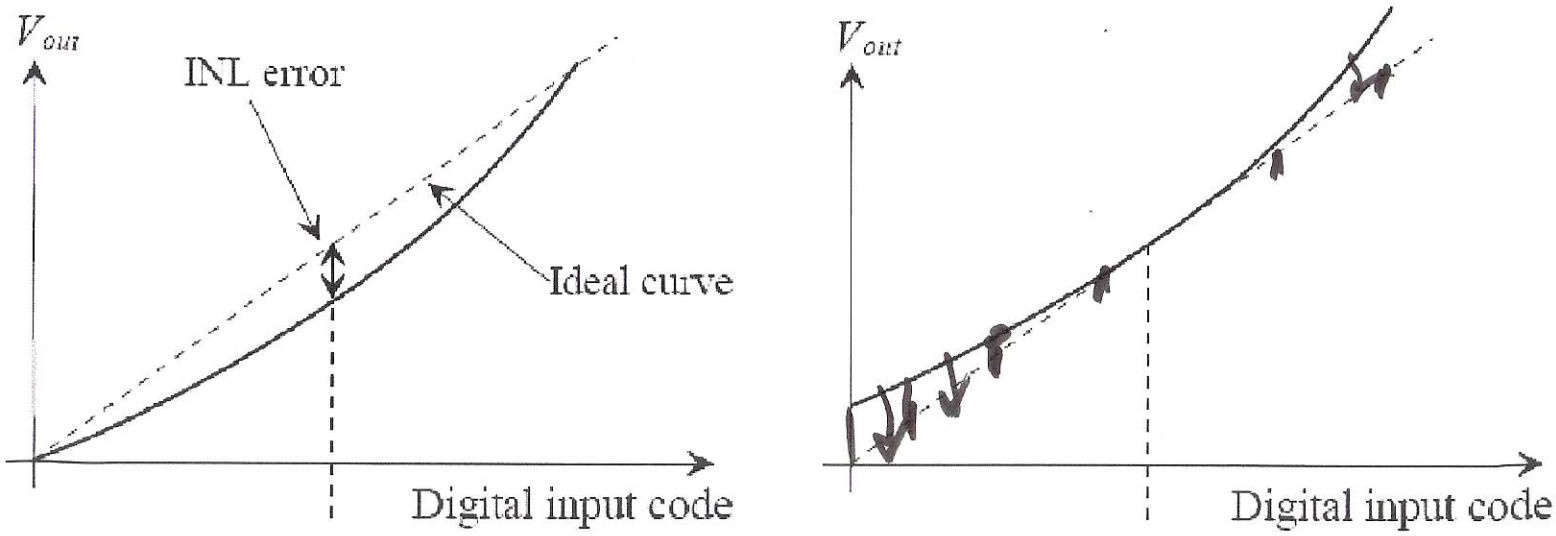


Figure 30.8 Trimming circuit for DAC offset.

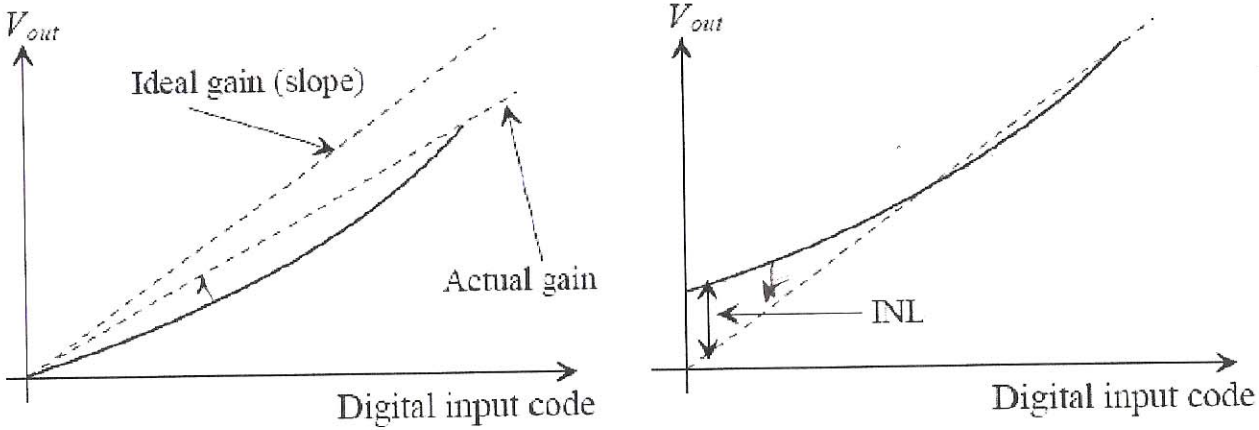
- To be added



(a) DAC transfer curves before calibration. (b) DAC transfer curves after offset calibration

Figure 30.10 Showing how INL can be seen as an offset error.

- To be added



(a) DAC transfer curves with gain error.

(b) DAC transfer curves after offset calibration with gain error.

Figure 30.11 Showing gain error and how it can cause problems in an offset calibration.

- To be added

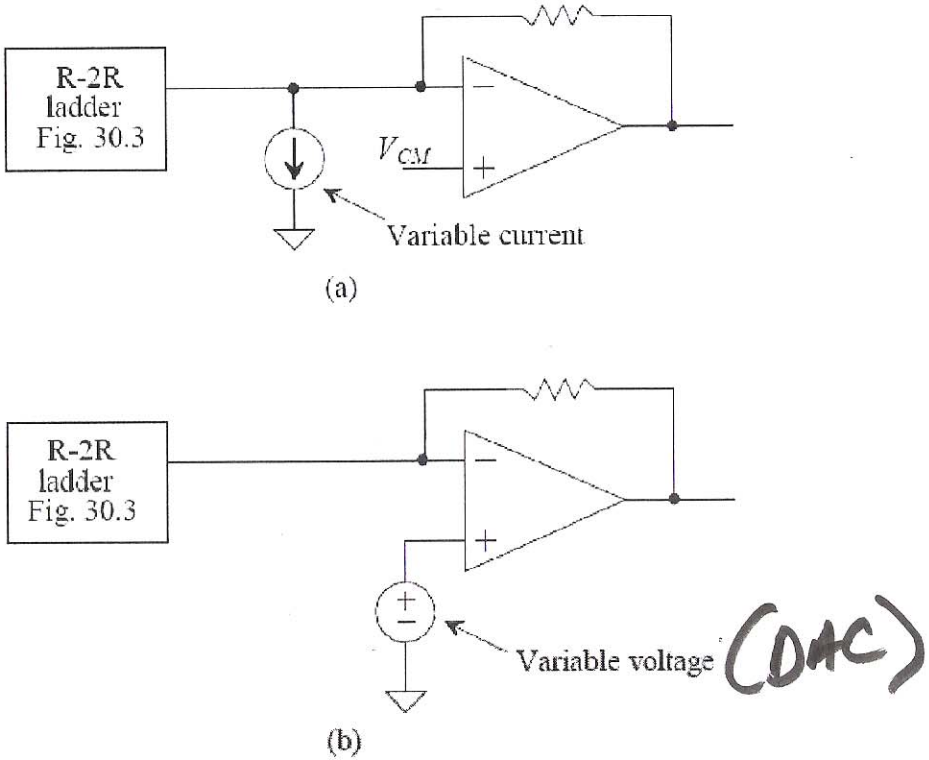
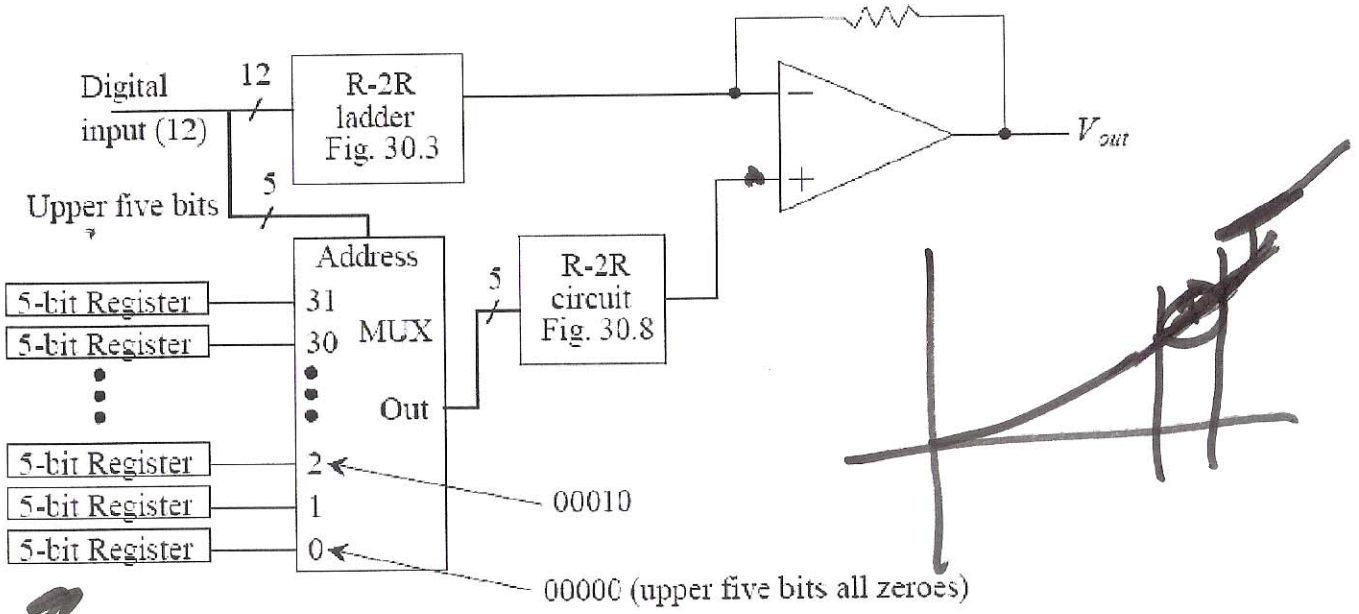


Figure 30.12 Trimming the output of the DAC using (a) current and (b) voltage.

- To be added



Calibration code

Figure 30.13 Calibration scheme for 12-bit DAC.

- To be added

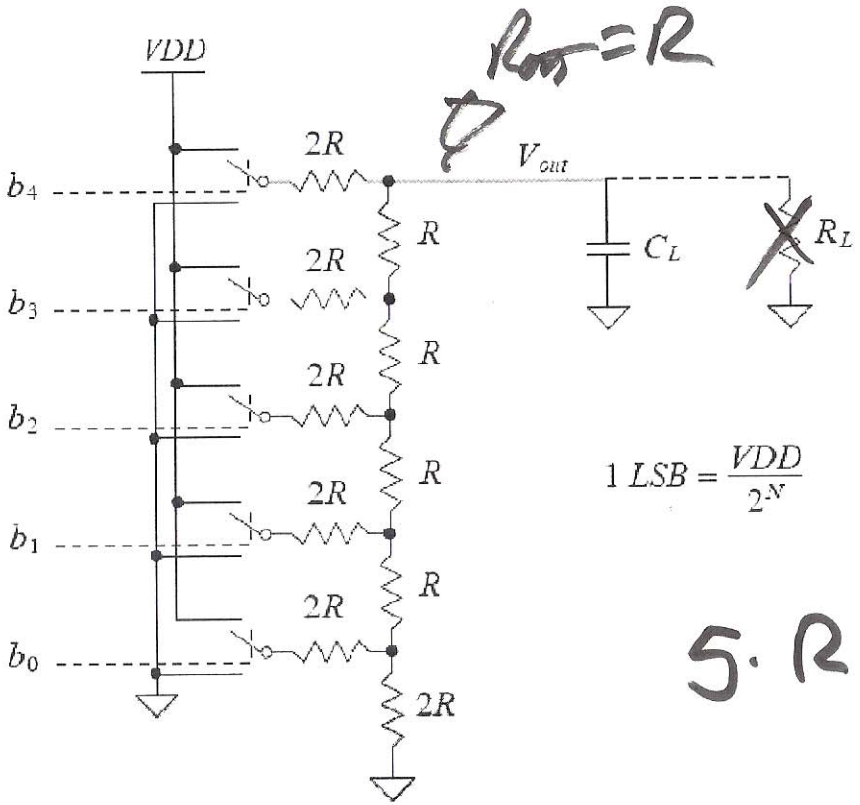


Figure 30.14 Voltage-mode (5-bit) DAC without an op-amp.

- To be added

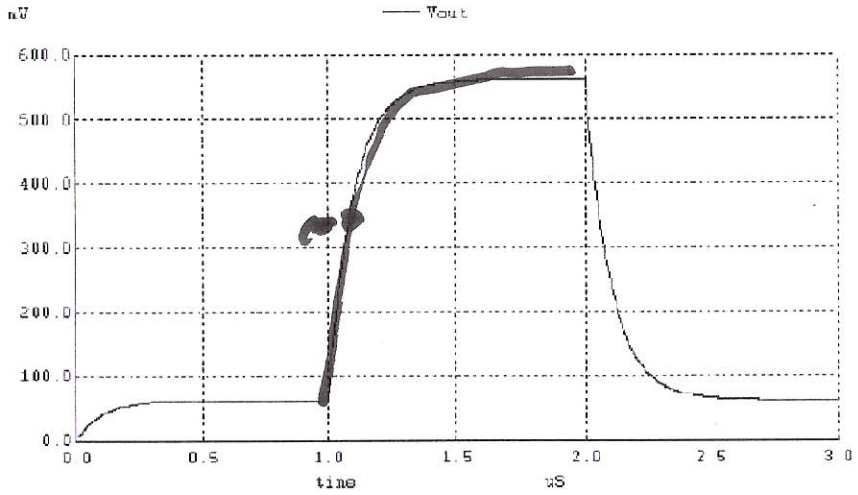
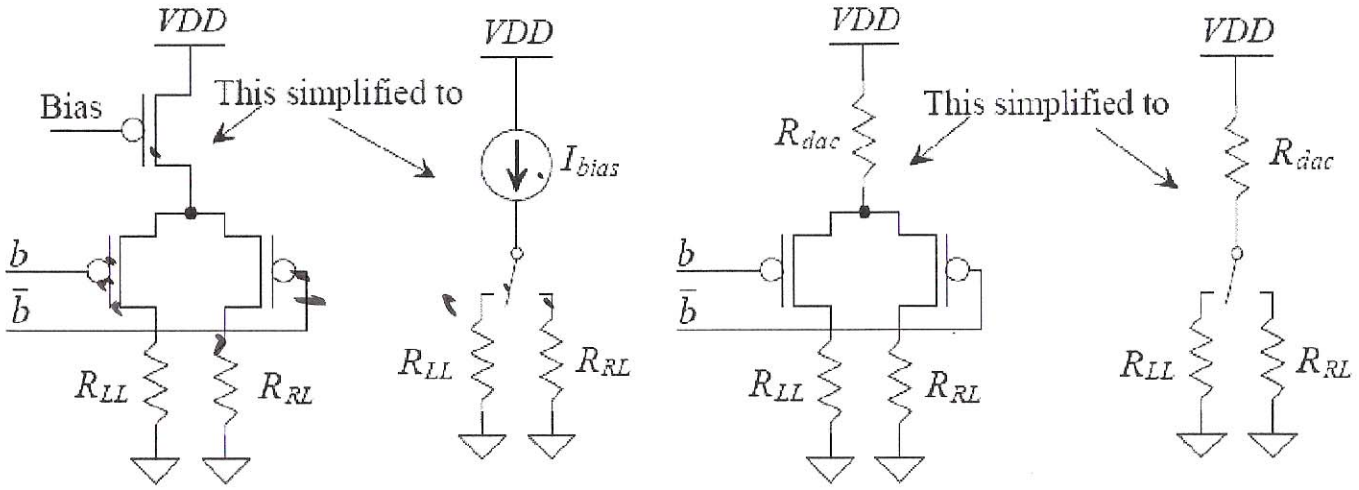


Figure 30.15 Example output for the 10-bit DAC in Ex. 30.1 showing settling time limitations.

- To be added



Current-source-based cell. Resistor-based cell.

Figure 30.18 Basic cell used in a current-mode DAC.

- To be added

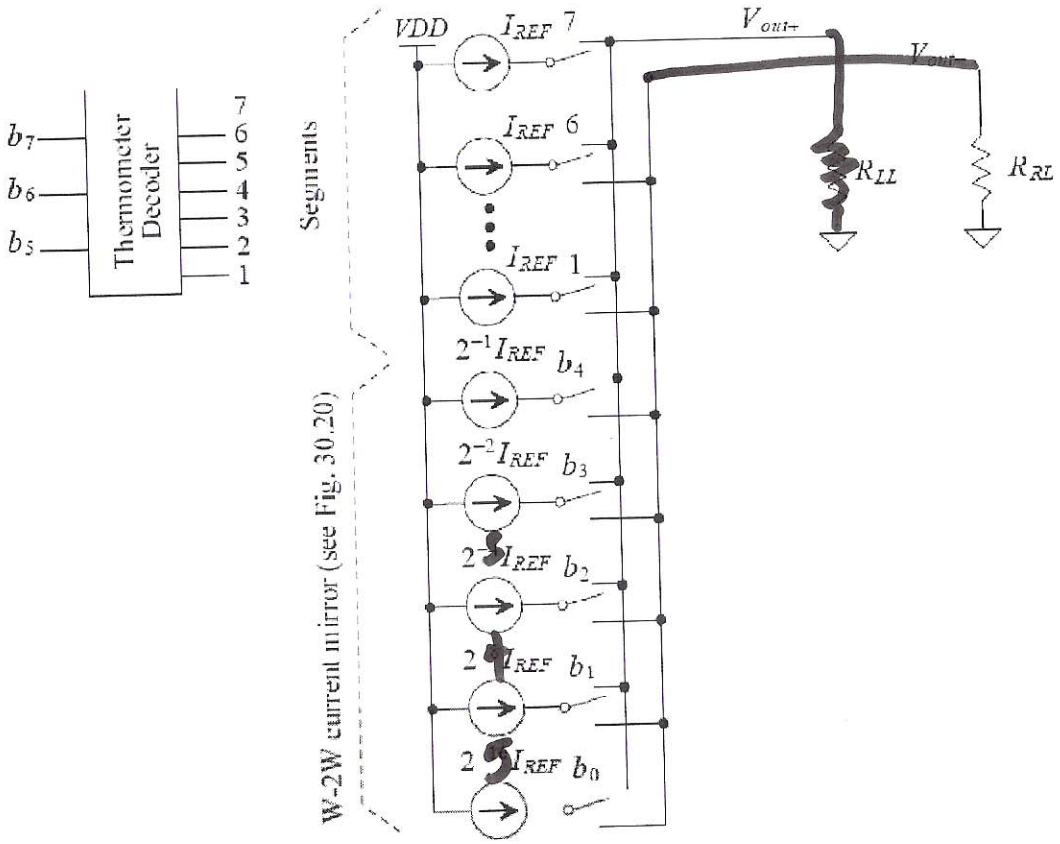


Figure 30.19 Implementation of a current-mode DAC.

- To be added

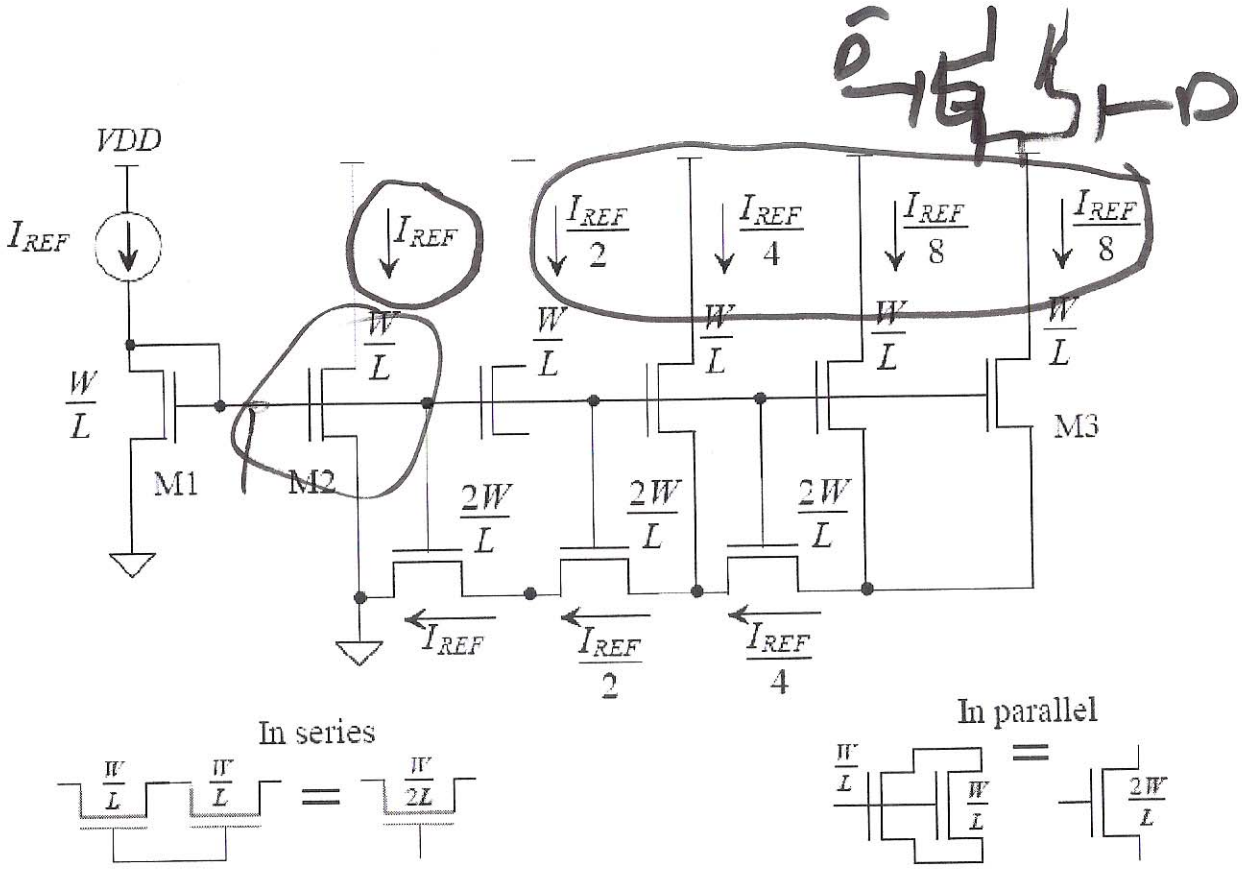


Figure 30.20 W-2W current mirror.

- To be added