29.2 part 2

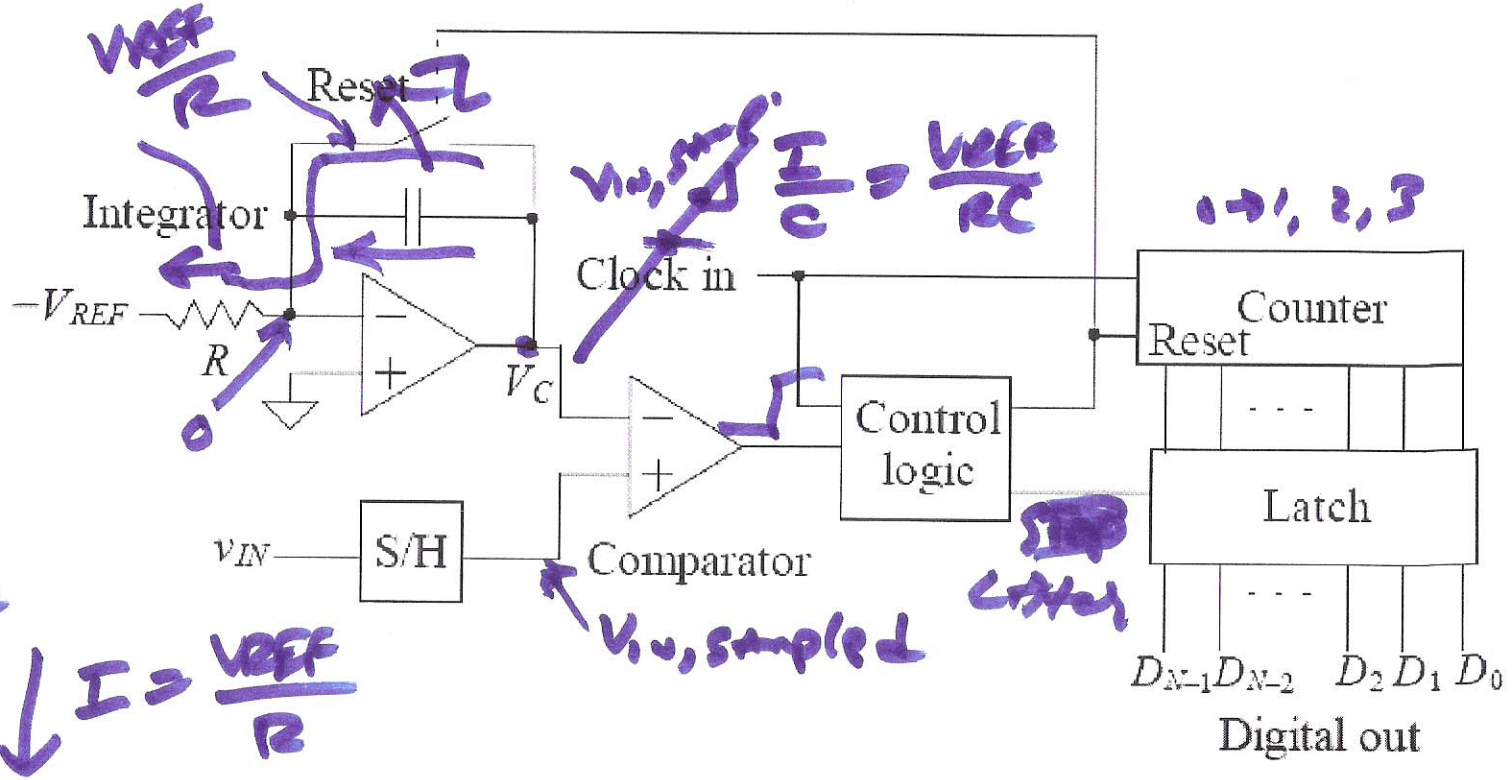


Figure 29.32 Block diagram of a single-slope ADC.

$I = C\frac{dv}{dt}$ $\frac{dv}{dt} = \frac{I}{C} = \text{const}$

$\frac{dv}{dt} = \text{const}$ $v \cdot t$

1)

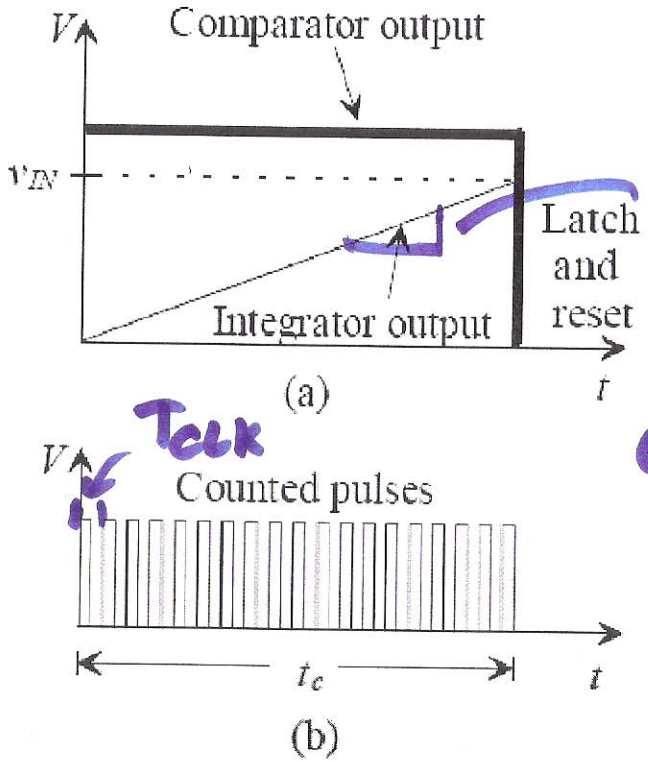


Figure 29.33 Single-slope ADC timing diagrams for (a) the comparator inputs and outputs and (b) the resulting counted pulses.

$f_{CLK} = \frac{1}{T_{CLK}}$

$\frac{I}{C} = \frac{V_{REF}}{RC}$

T_{CLK}

$0 \rightarrow 1023$ $N = 10$

total time for conversion

$1023 \cdot T_{CLK}$

$2^N \cdot T_{CLK}$

$LSB = \frac{V_{REF}}{2^N} = 1mV$ — $1mV$

1 ms

2)

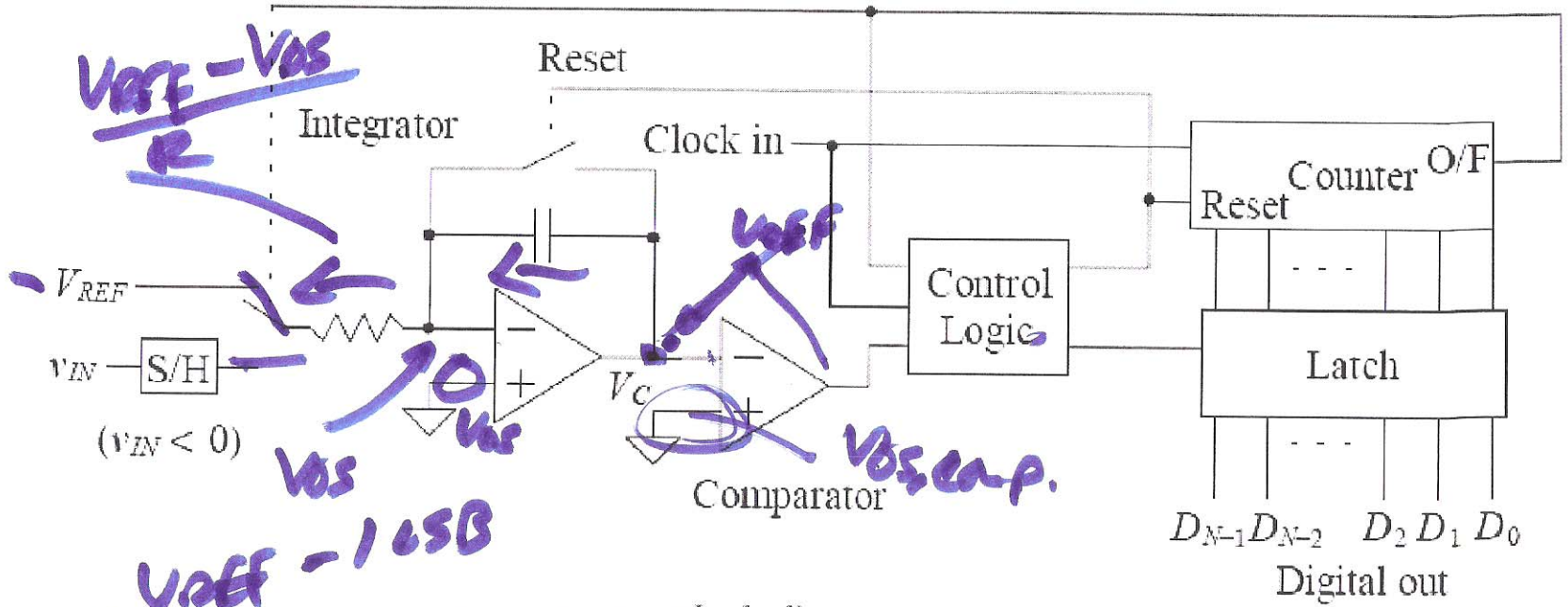


Figure 29.34 Block diagram of a dual-slope ADC.

$$\frac{\frac{V_{REF} - V_{OS}}{R}}{C} \cdot t_1 = \frac{\frac{V_{in} - V_{OS}}{R}}{C} \cdot t_2$$

$$\frac{V_{REF}}{V_{in}} = \frac{t_2}{t_1} = \#\text{ of clock diff}$$

3)

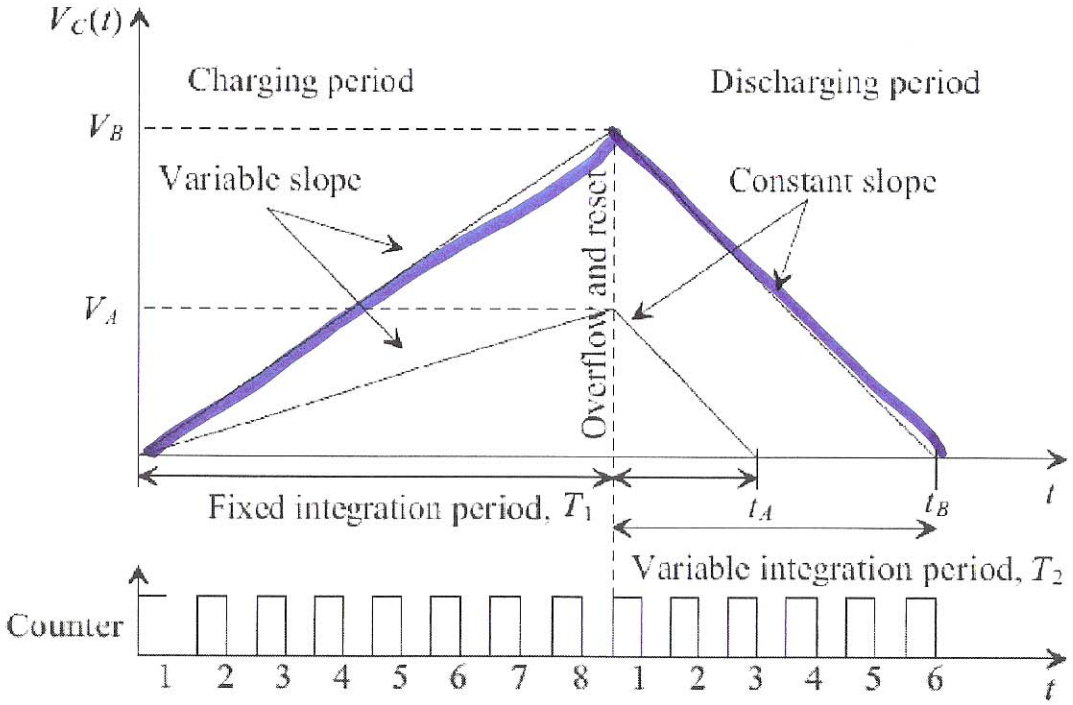


Figure 29.35 Integration periods and counter output for two separate samples of a 3-bit dual-slope ADC.

4)

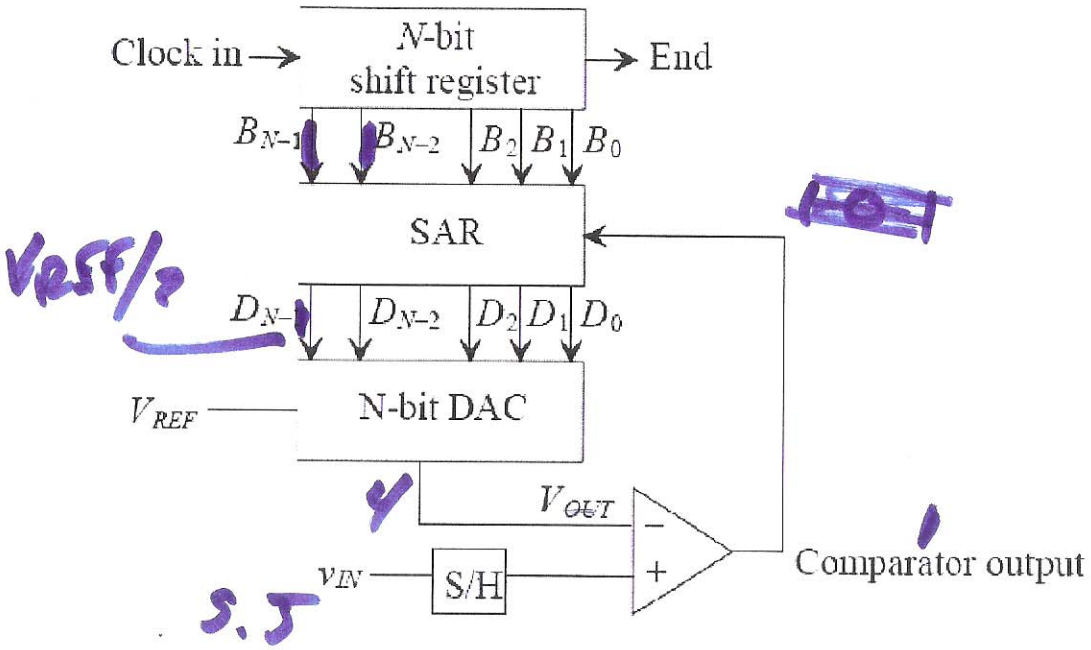


Figure 29.36 Block diagram of the successive approximation ADC.

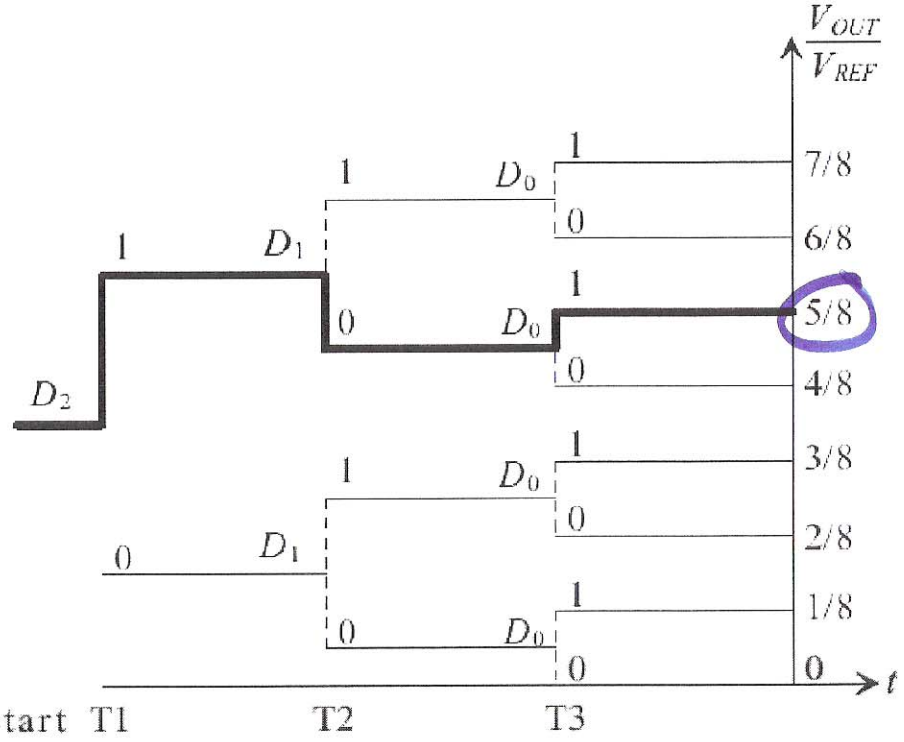


Figure 29.37 Binary search performed by a 3-bit successive approximation ADC for D=101.

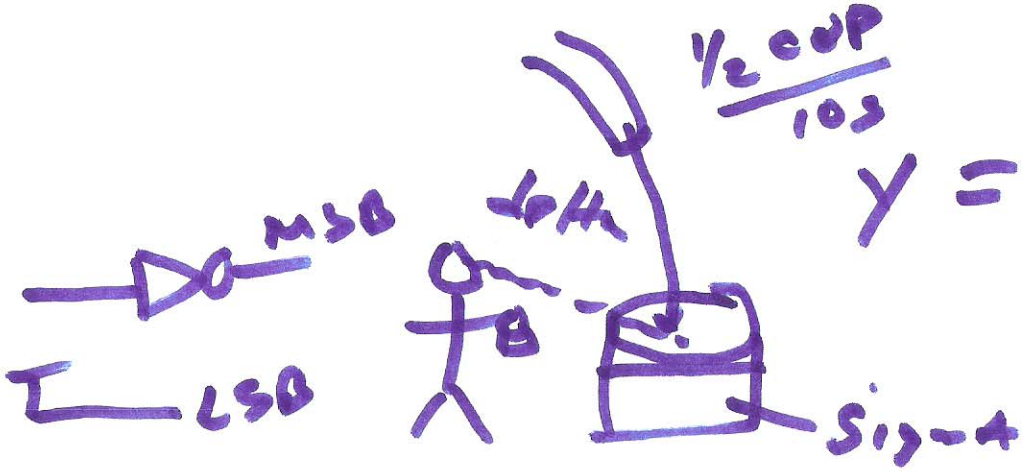
Step	v_{IN}	$B_2B_1B_0$	$D_2D_1D_0$	V_{OUT}	Comp Out	$D_2D_1D_0$
T1	5.5	100	100	$1/2\ V_{REF} = 4$ V	0	100
T2	5.5	010	110	$(1/2+1/4)V_{REF} = 6$ V	1	100
T3	5.5	001	101	$(1/2+1/8)V_{REF} = 5$ V	0	101

(a)

Step	v_{IN}	$B_2B_1B_0$	$D'_2D'_1D'_0$	V_{OUT}	Comp Out	$D_2D_1D_0$
T1	2.5	100	100	$1/2\ V_{REF} = 4$ V	1	000
T2	2.5	010	010	$1/4\ V_{REF} = 2$ V	0	010
T3	2.5	001	011	$(1/4+1/8)V_{REF} = 3$ V	1	010

(b)

Figure 29.38 Results from the 3-bit successive approximation ADC using (a) $v_{IN} = 5.5$ and (b) 2.5 V.



$$y = \frac{1}{N}(x_1 + x_2 + x_3 \cdots + x_N)$$

$$y(z) = \frac{1}{N} x(z)\left(1 + z^{-1} + z^{-2} + z^{-N}\right)$$

$$\frac{y(z)}{x(z)} = \frac{1}{N}\left(1 + z^{-1} + z^{-2} + \cdots z^{-N}\right)$$

0 → −1 (11) 10 sec

1 → +1 (01)

	10
10	0
20	1
30	0
40	1
50	0
60	1

− 1 cup
− ½ cup
− 0 cup

Avg = ½ cup/10s

$x_1 + x_2 + x_3 + x_4 + x_5$

$$\frac{0+1+1+0+1+1}{6} = \frac{4}{6} = \frac{2}{3}$$

8)

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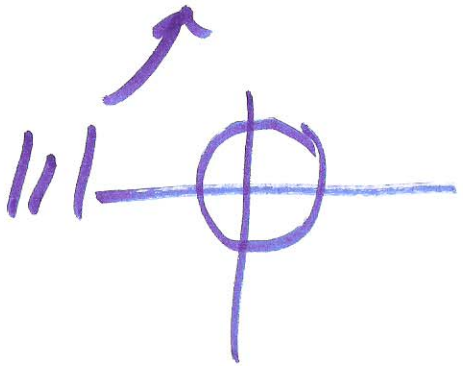
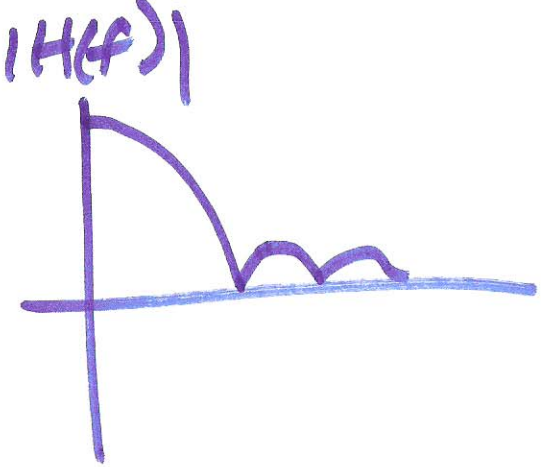
$$H(z) = \frac{Y(z)}{X(z)} = \frac{1}{N}\left(1 + z^{-1} + z^{-2} + \dots z^{-N}\right)$$

$$1 - z^{-1} + z^{-1} - z^{-2} + z^{-2} - z^{-3}$$



$$\cdot \frac{(1 - z^{-1})}{(1 - z^{-1})}$$

$$H(z) = \frac{1}{N} \frac{1 - z^{-N}}{1 - z^{-1}}$$



$$z \to e^{j2\pi f/f_s}$$

sample freq.

$f_s = 0.1$ Hz

9)

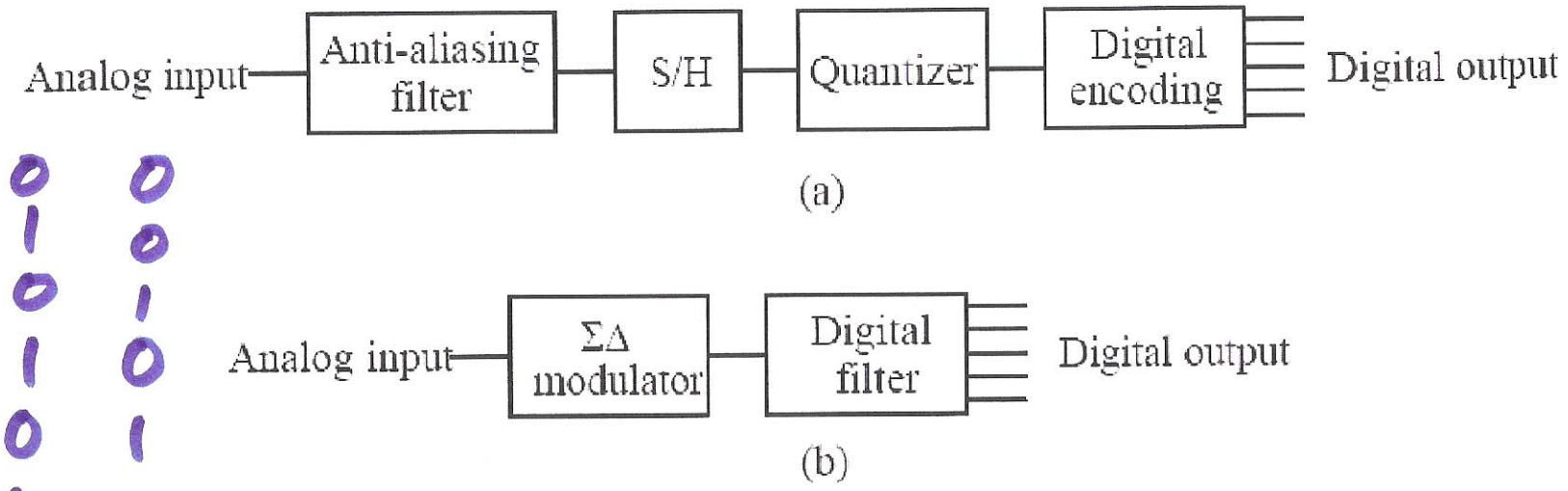
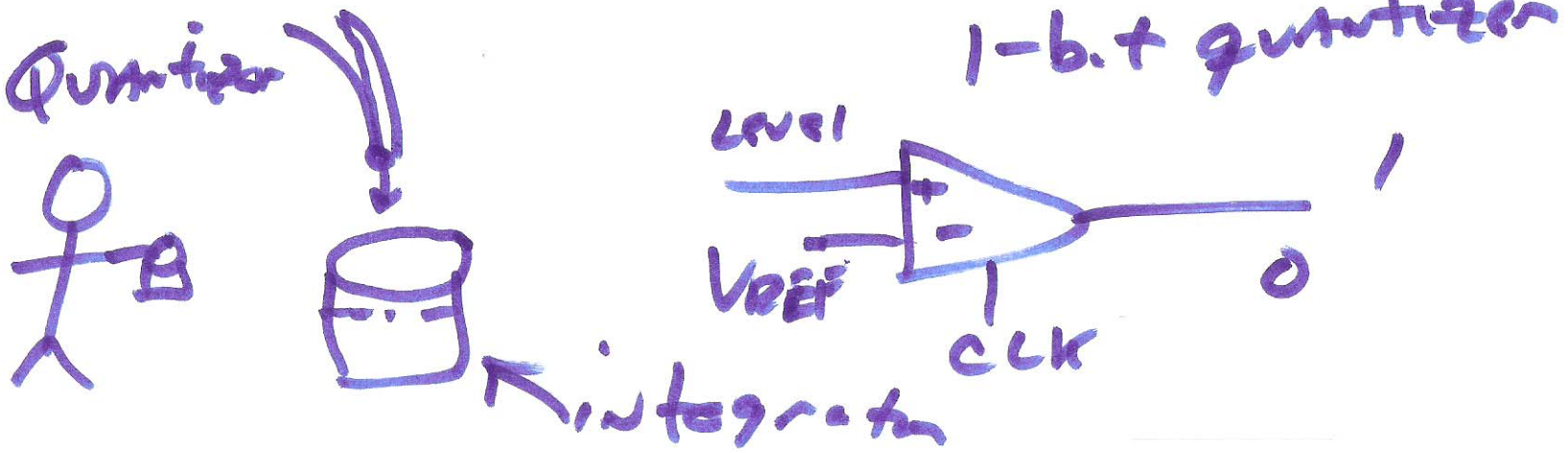
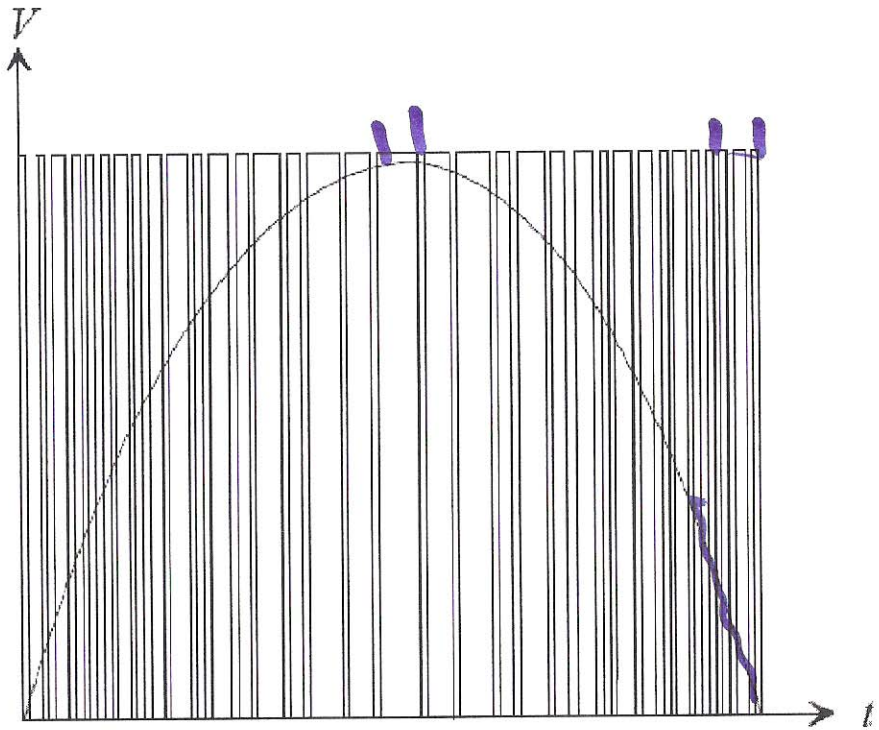


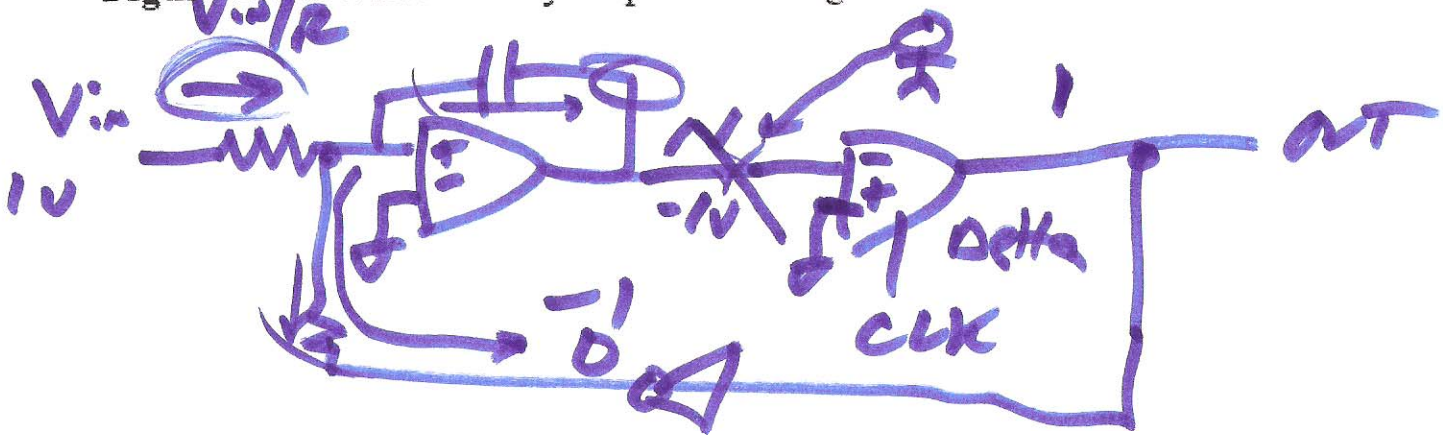
Figure 29.41 Typical block diagram for (a) Nyquist rate converters and (b) oversampling ADCs.





Sigma Delta

Figure 29.43 Pulse-density output from a sigma-delta modulator for a sine wave input.



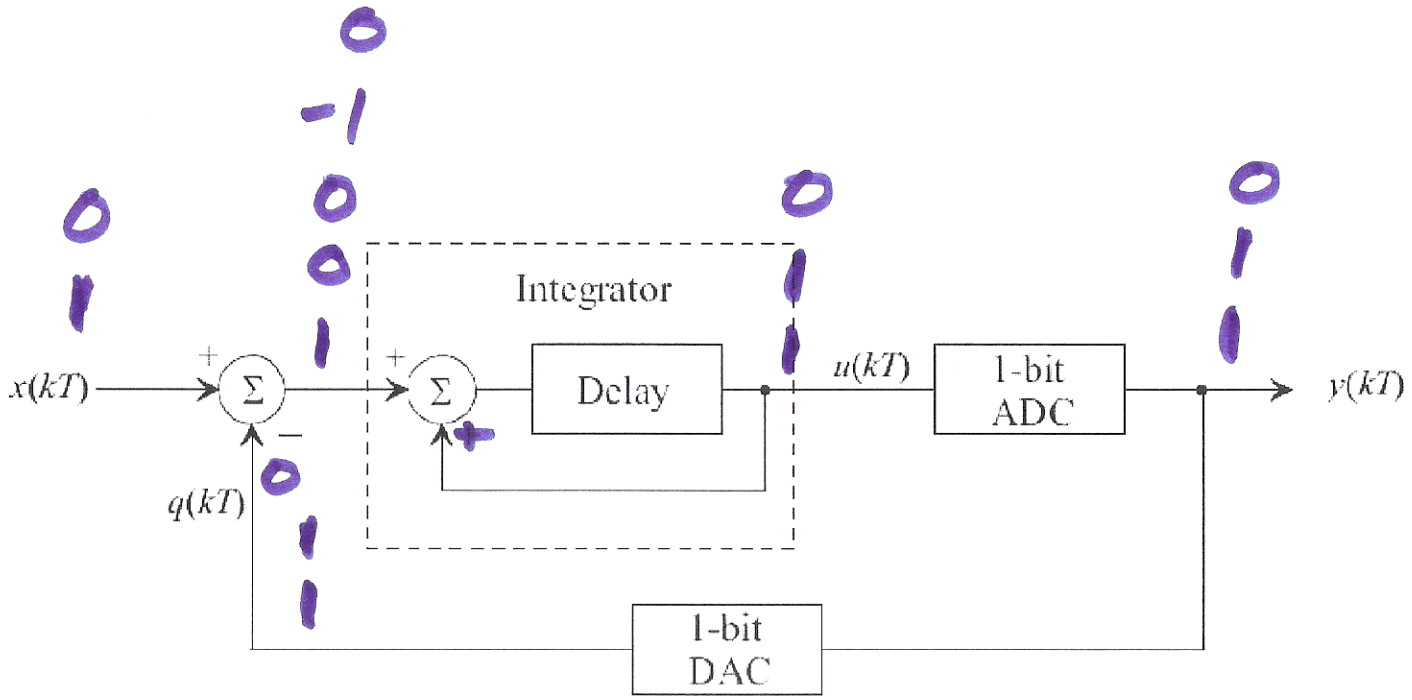
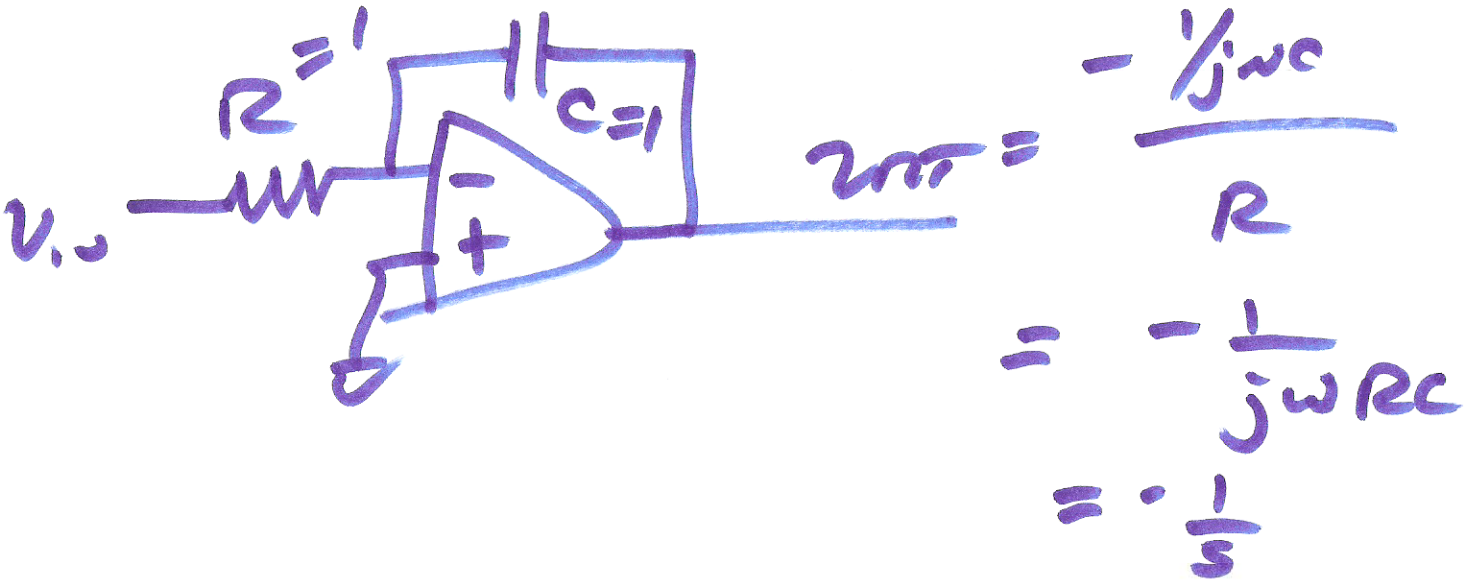


Figure 29.44 A first-order sigma-delta modulator.



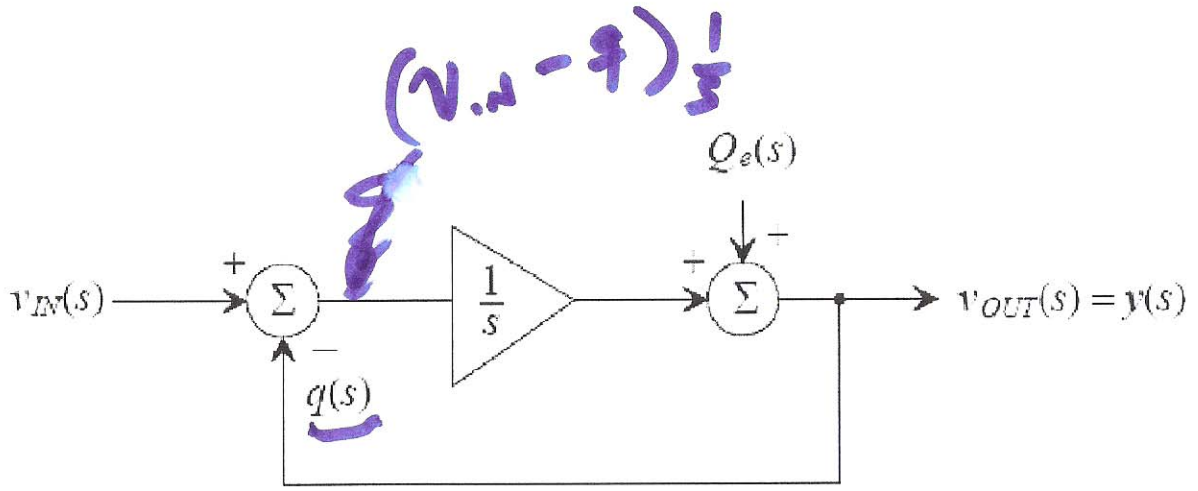
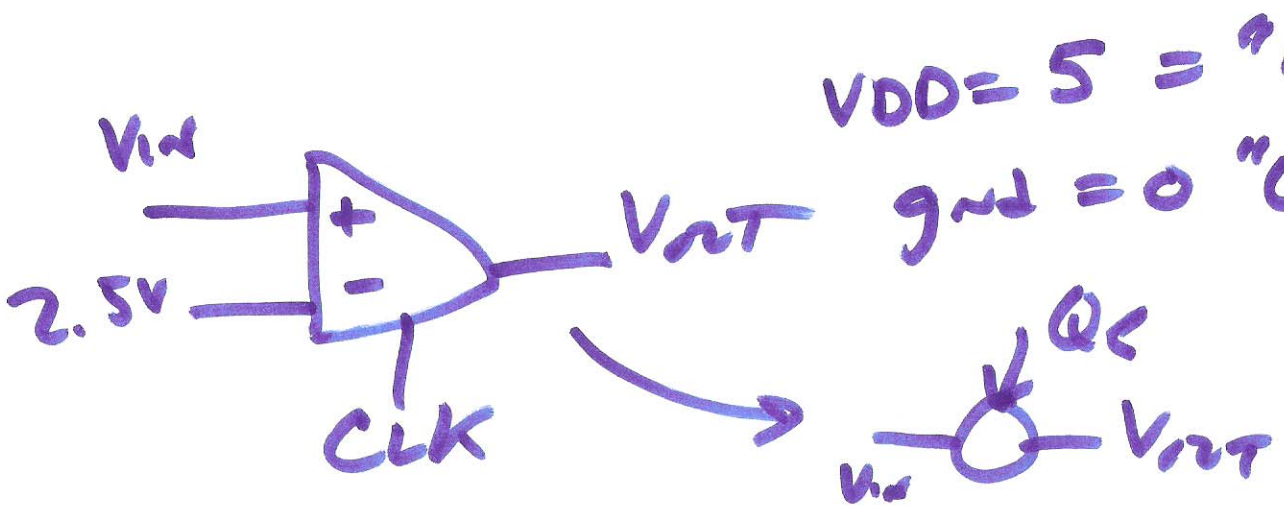


Figure 29.45 A frequency domain model for the first-order sigma-delta modulator.

$$v_{out} = Q_e + \frac{1}{s}(v_{in} - q) \quad v_{out}$$

$$v_{out}\left(1+\frac{1}{s}\right) = Q_e + \frac{1}{s}v_{in}$$

$$v_{out} = v_{in}\cdot\underbrace{\frac{1}{1+s}}_{STF} + Q_e\cdot\underbrace{\frac{s}{1+s}}_{NTF}$$



Vin	Vout	Qe
2	0	-2
1	0	-1
0	0	0
3	5	+2
3.42	5	1.58V

$$V_{LSB} = \frac{q}{\sqrt{12}\,C_s} = Q_e^2$$

14)

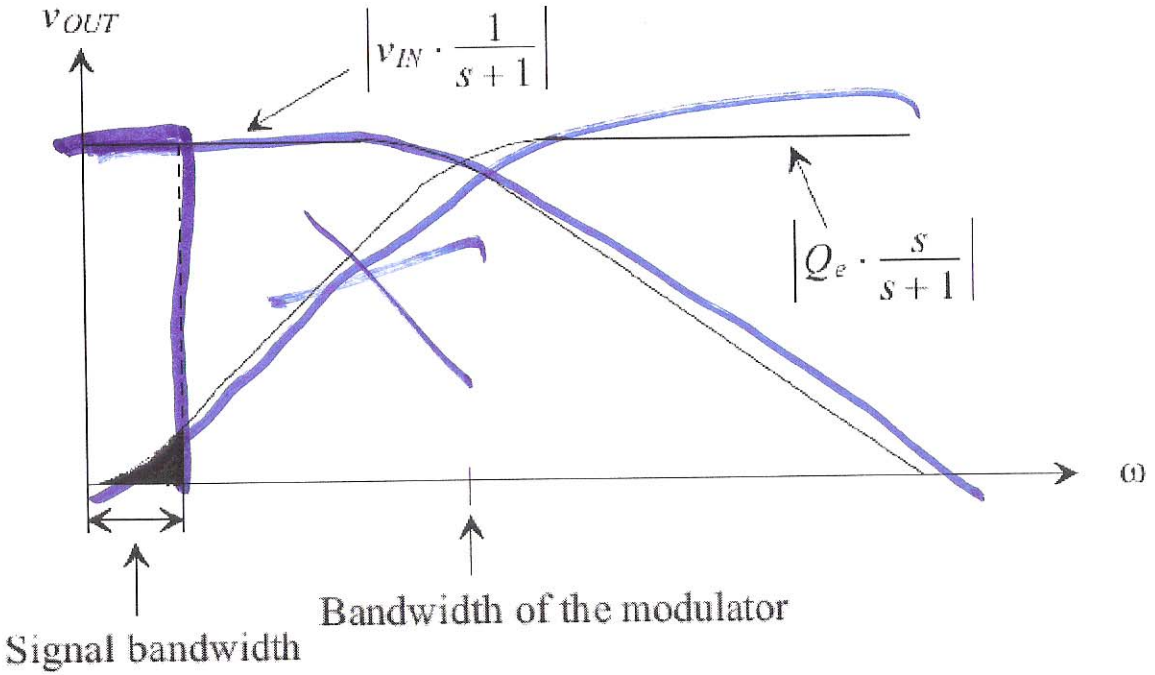


Figure 29.46 Frequency response of the first-order sigma-delta modulator.

15)

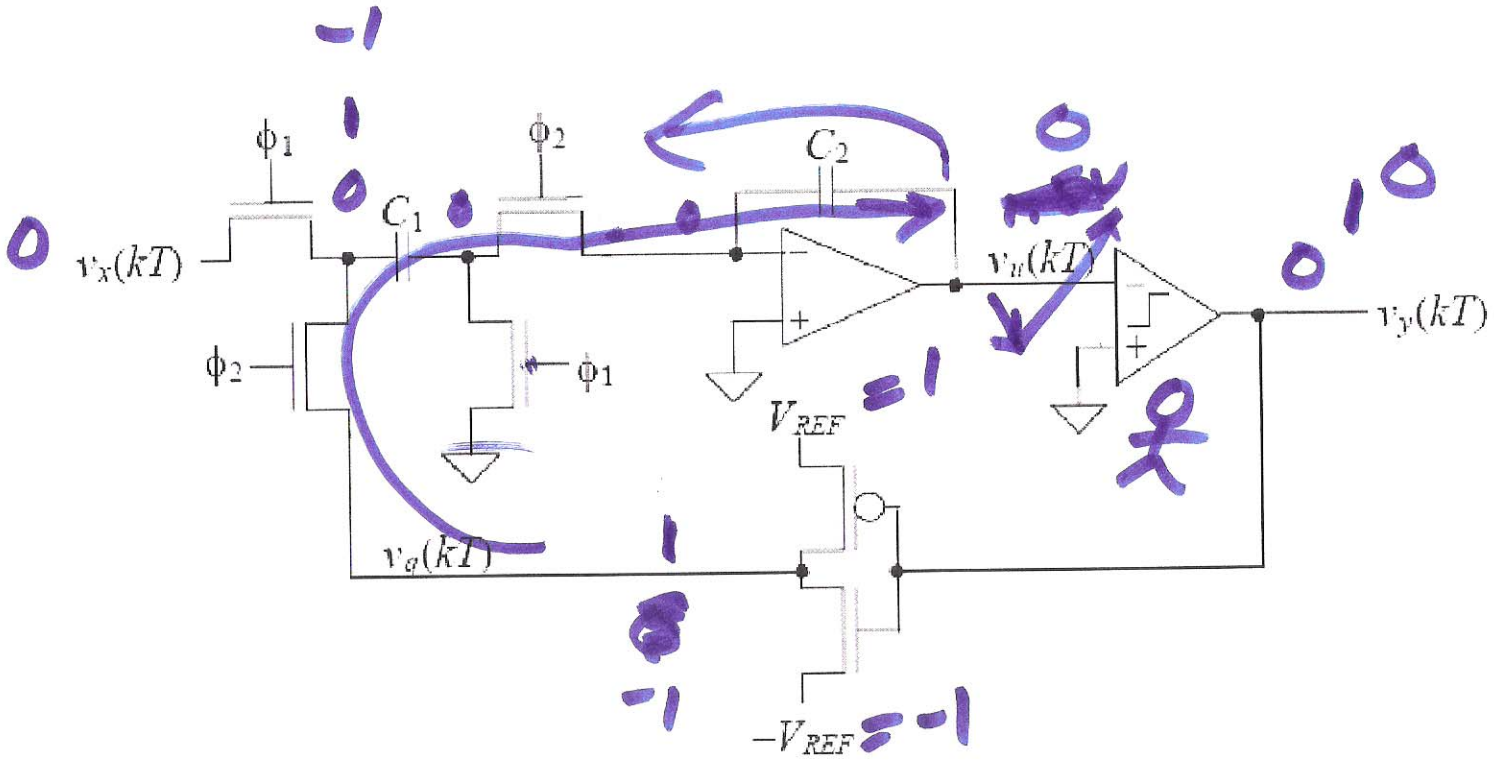


Figure 29.47 Implementation of a first-order sigma-delta modulator using a switched capacitor integrator.

k	$v_a(kT)$	$v_u(kT)$	$v_q(kT) = v_y(kT)$	$Q_e(kT)$	$\overline{v_q(kT)}$
0	–0.6	0.1	1.0	0.9	1.0
1	1.4	–0.5	–1.0	–0.5	0
2	–0.6	0.9	1.0	0.1	0.333
3	–0.6	0.3	1.0	0.7	0.50
4	1.4	–0.3	–1.0	–0.7	0.20
5	–0.6	1.1	1.0	–0.1	0.333
6	–0.6	0.5	1.0	0.5	0.429
7	1.4	–0.1	–1.0	–0.9	0.25
8	–0.6	1.3	1.0	–0.3	0.333
9	–0.6	0.7	1.0	0.3	0.40

Figure 29.48 Data from the first-order ΣΔ modulator.