Sec. 26.4

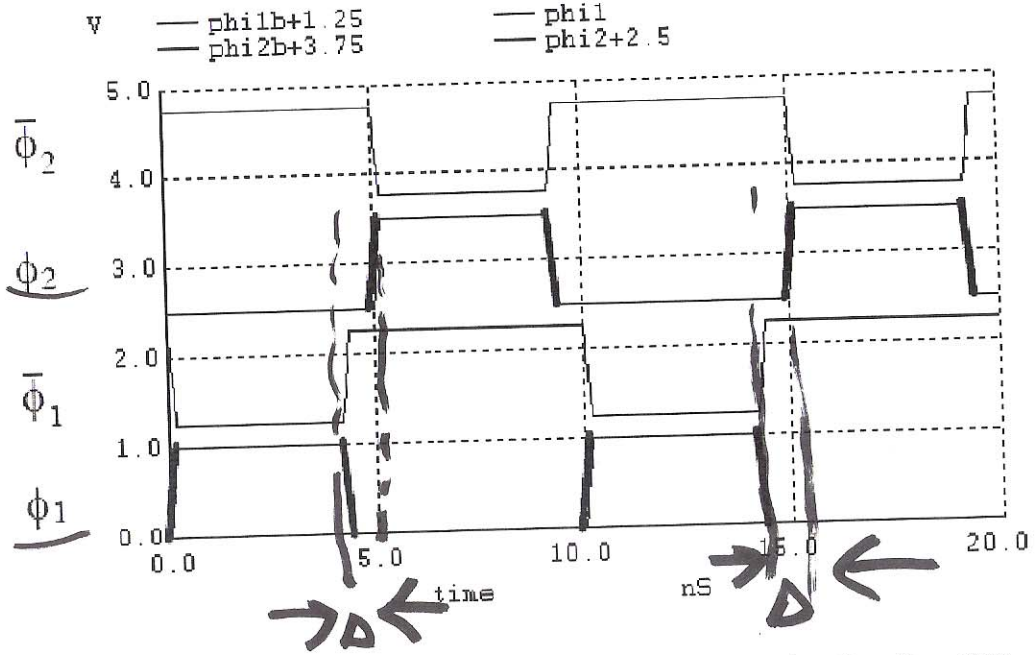


Figure 26.49 Generating nonoverlapping clocks for SC circuits.

30:07

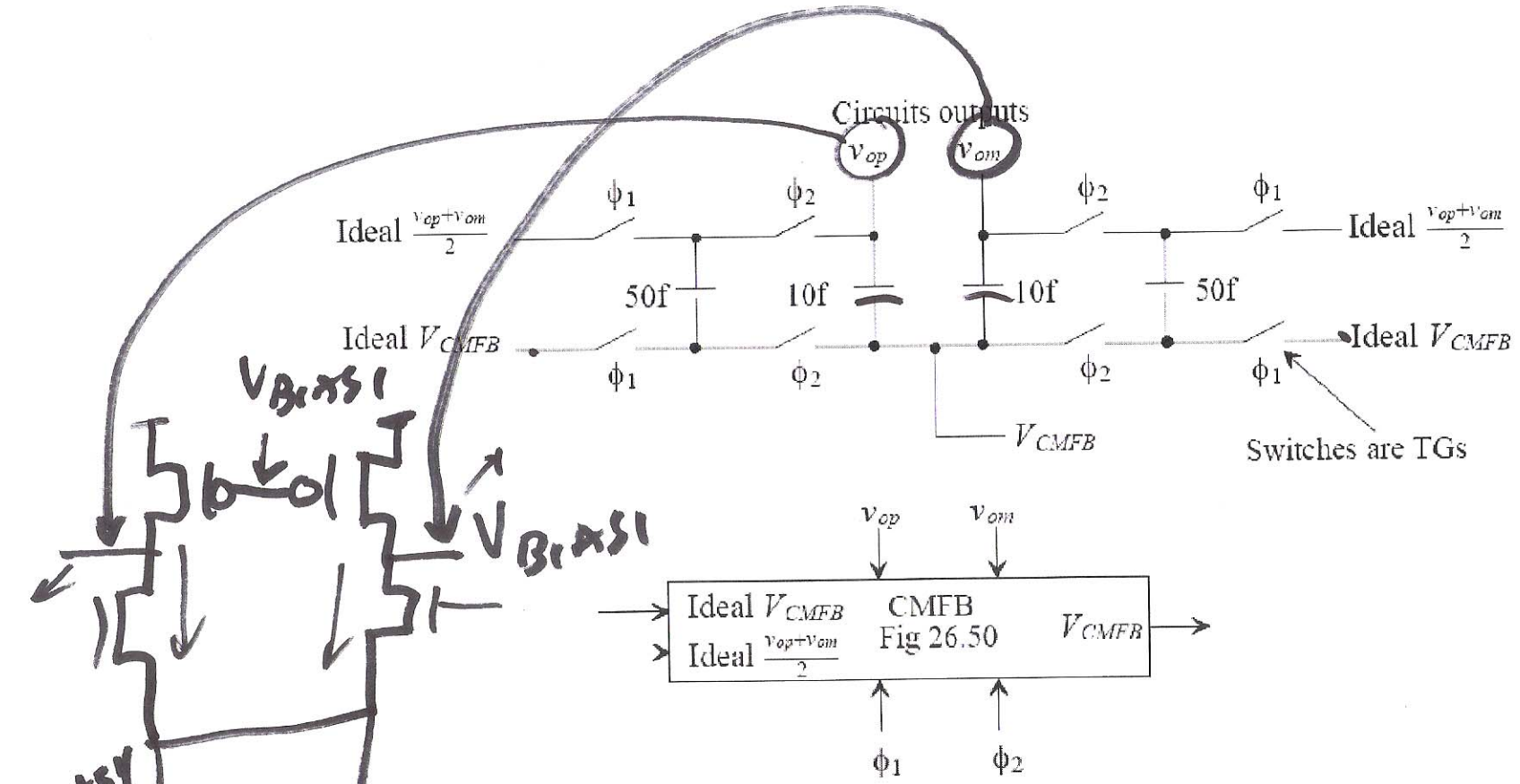


Figure 26.50 A switched-capacitor CMFB circuit (see Fig. 26.16). Switches implemented with transmission gates.

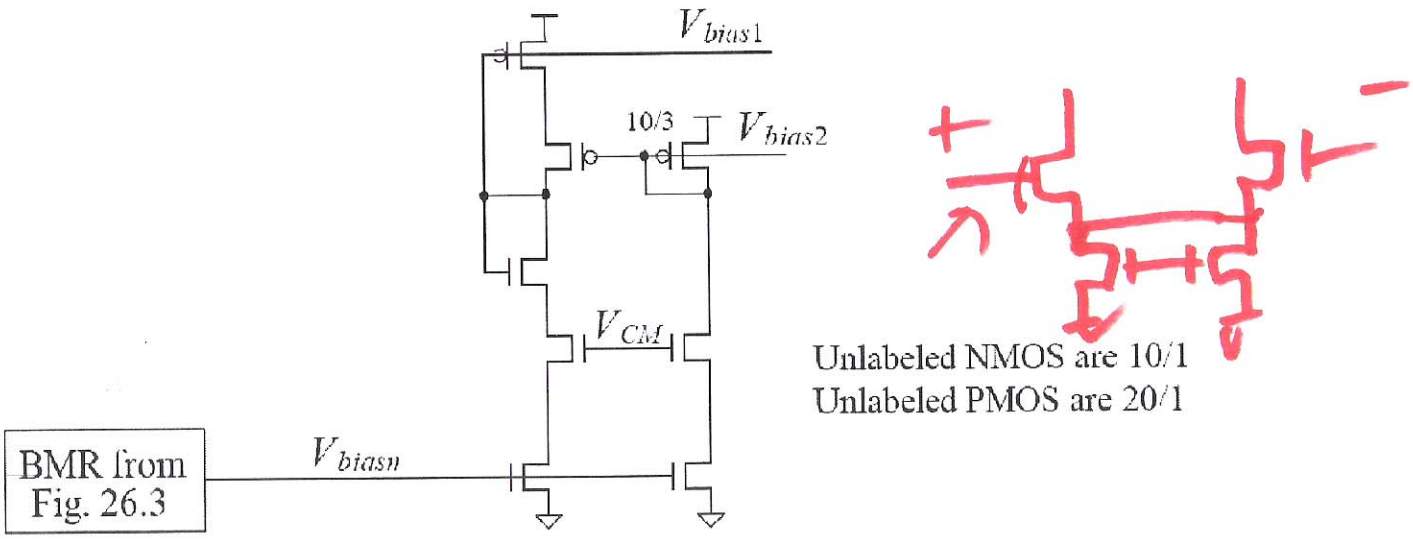
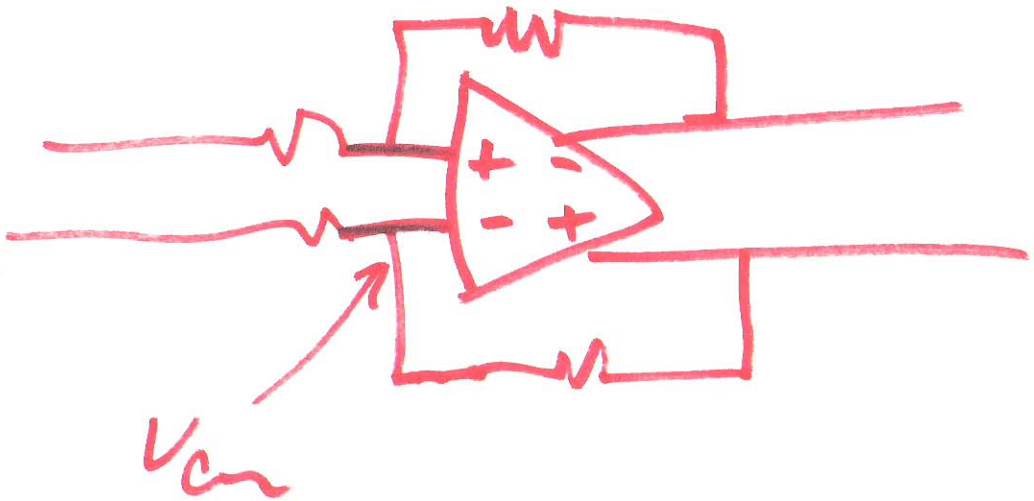


Figure 26.52 Biasing circuit for the op-amp developed in this section.



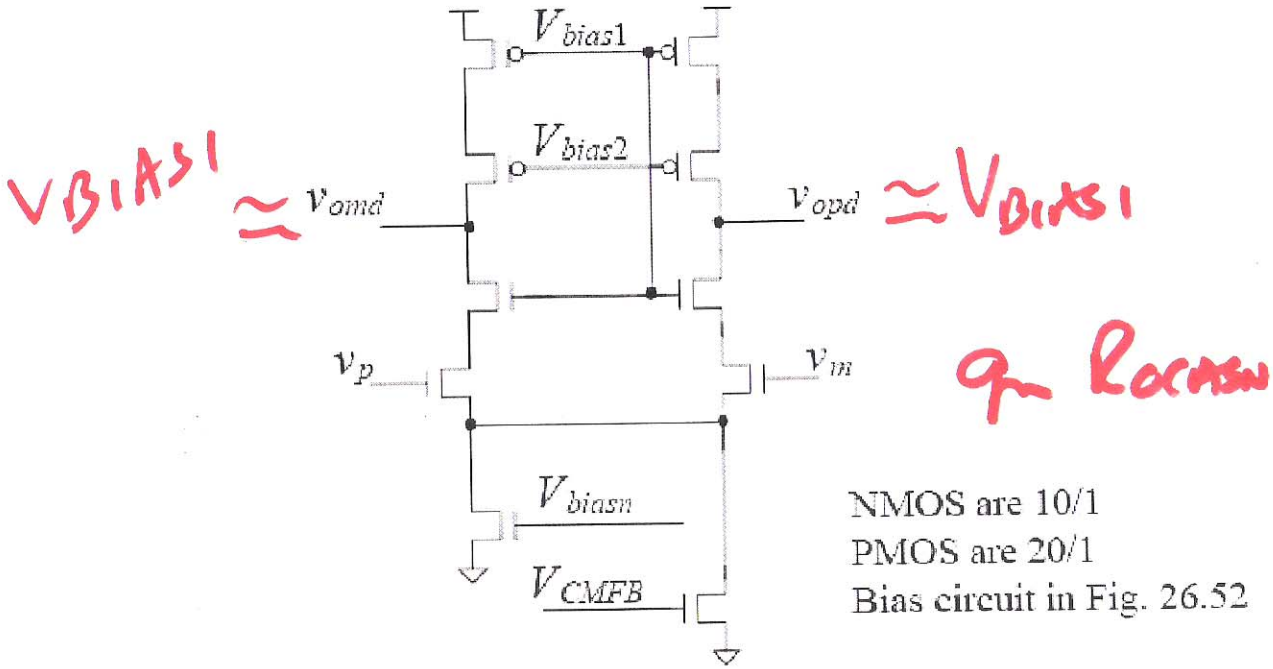


Figure 26.53 Diff-amp used with the bias circuit of Fig. 26.52.

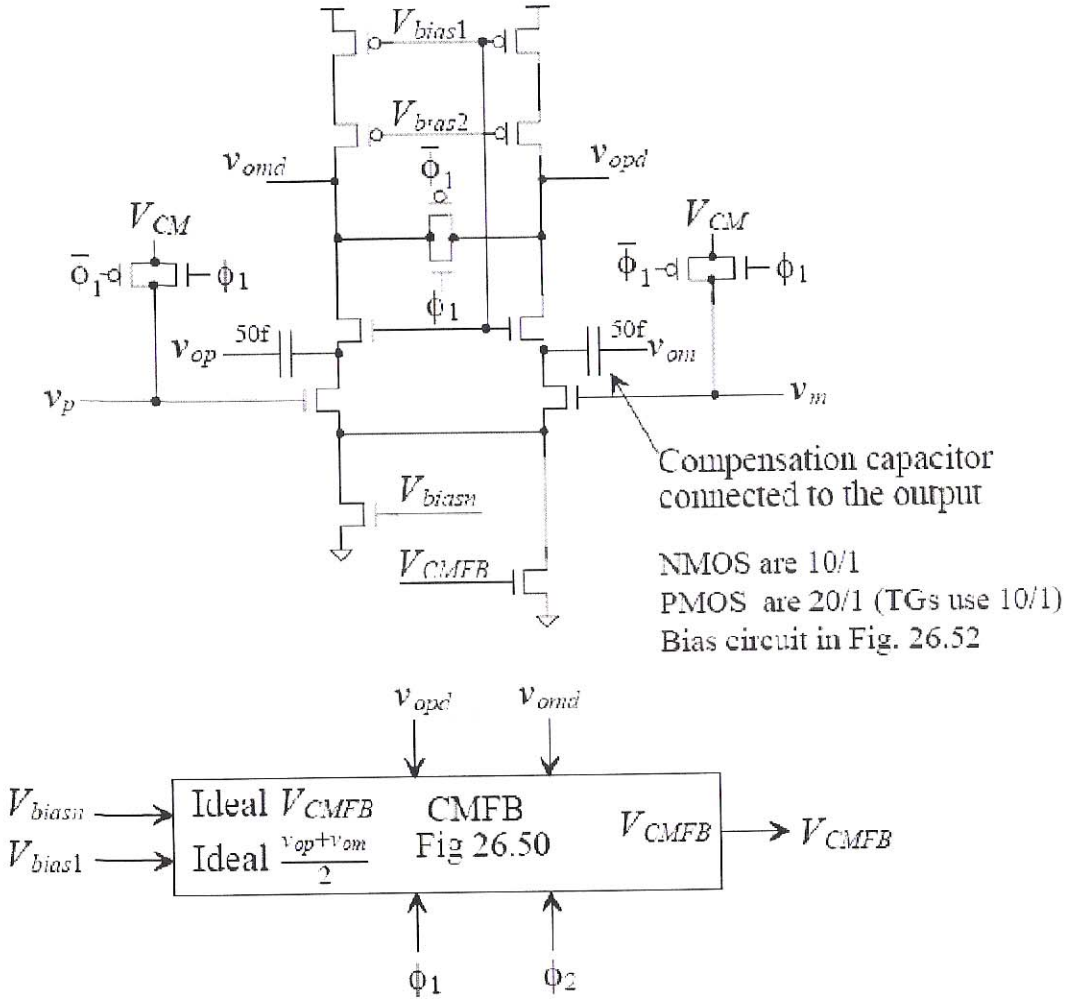
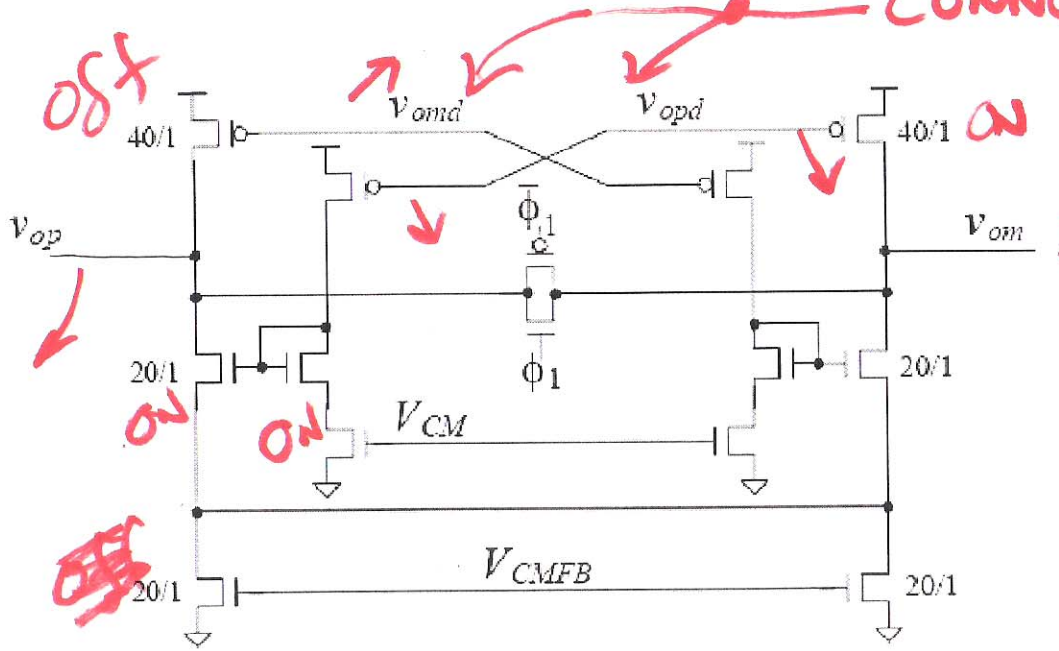


Figure 26.54 First-stage diff-amp with SC CMFB.



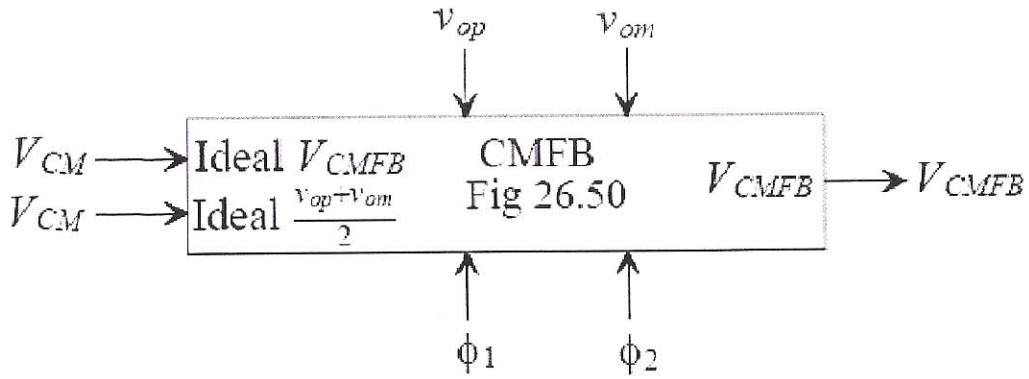
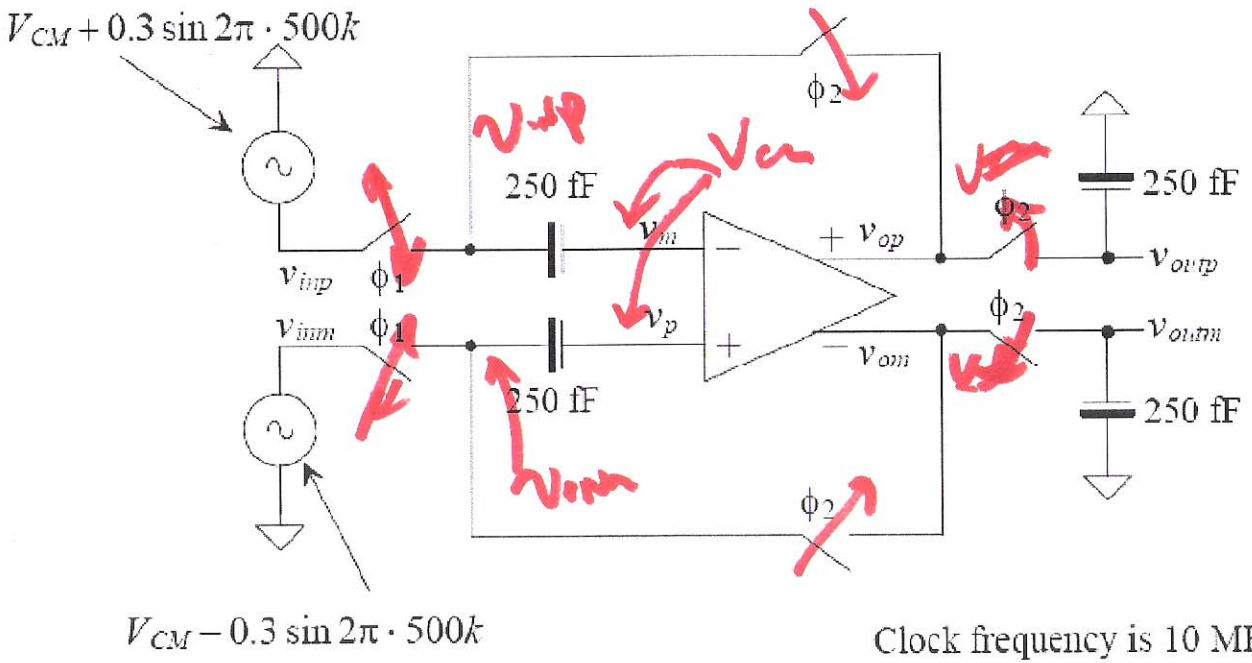


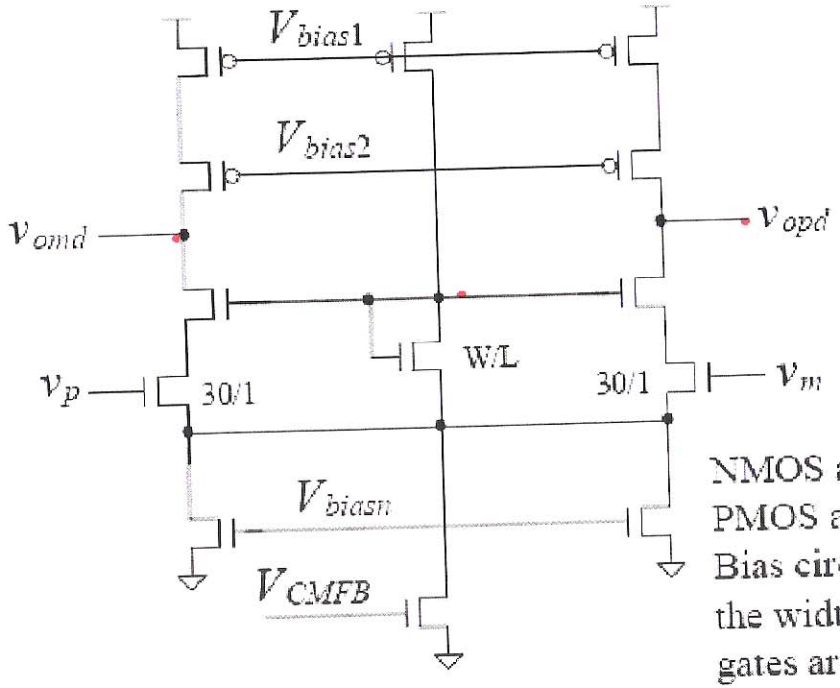
Figure 26.56 Output buffer and CMFB.



Clock frequency is 10 MHz.

Figure 26.58 Simulating the operation of the op-amp formed with the diff-amp in Fig. 26.54 and buffer in Fig. 26.56.

Sample & Hold



NMOS are 10/1
PMOS are 20/1
Bias circuit in Fig. 26.52 with the widths of the NMOS whose gates are tied to Vcm increased to 30.

Figure 26.63 Modifying the diff-amp seen in Fig. 26.53 for wider swing operation.