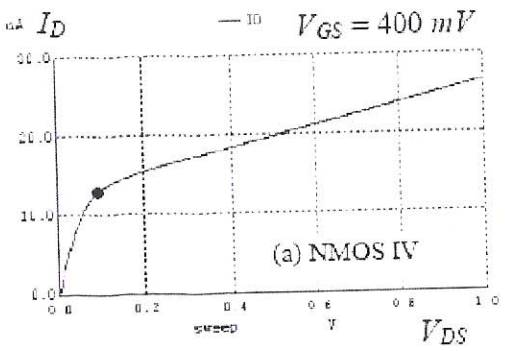
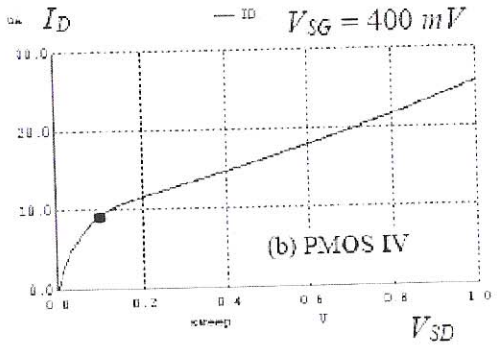
26.3

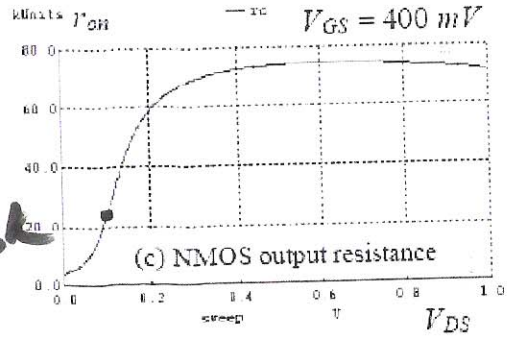
TABLE 9.2

$g_m r_o \sim 25$

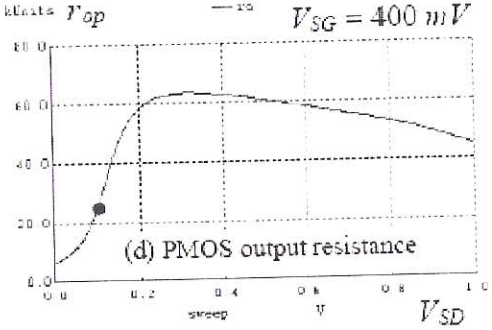




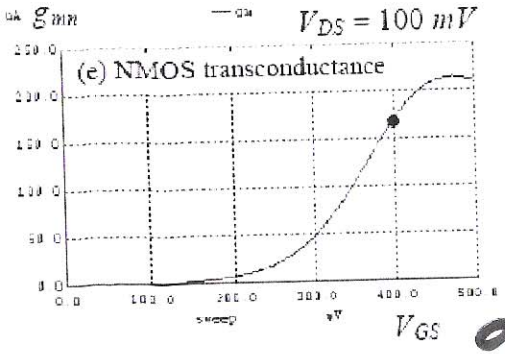
$L = 1 \quad g_m r_o < 5$

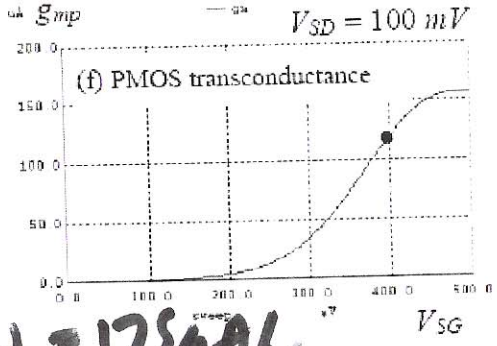


$r_{ON} \simeq 25k$



$r_{op} \simeq 25k$





$g_p \simeq 125\mu A$

$g_N = 175\mu A/V$

Figure 26.18 Characteristics of NMOS (10/1) and PMOS (20/1) devices.

1)

NMOS are 10/1
PMOS are 20/1
Bias circuit in Fig. 26.3

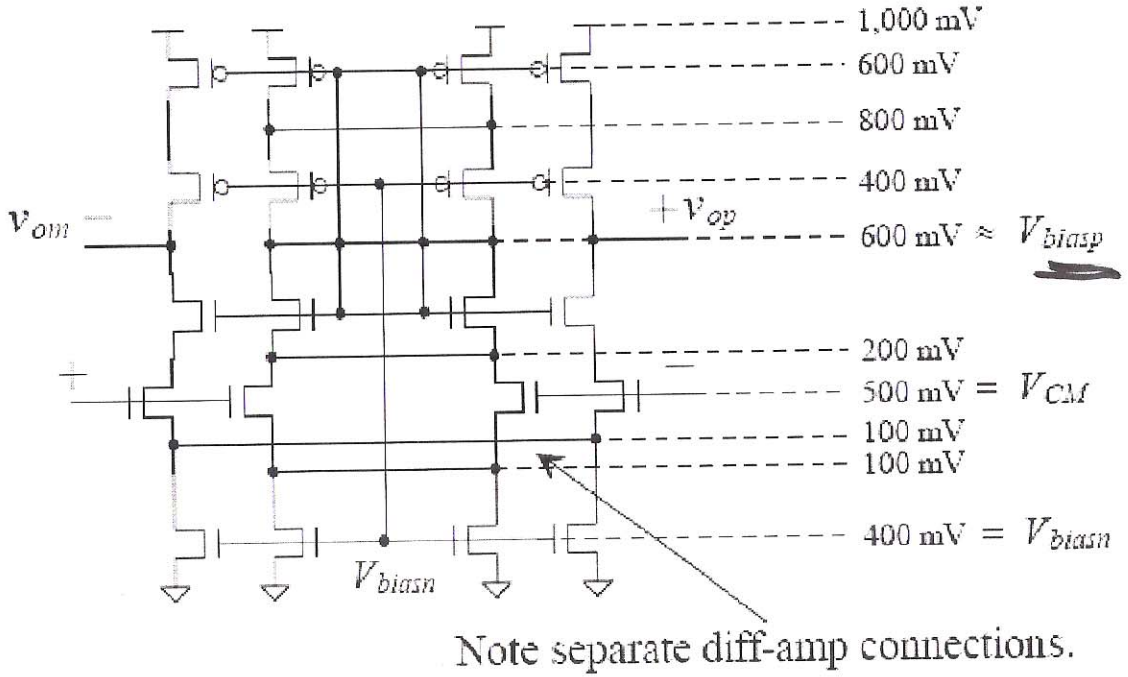
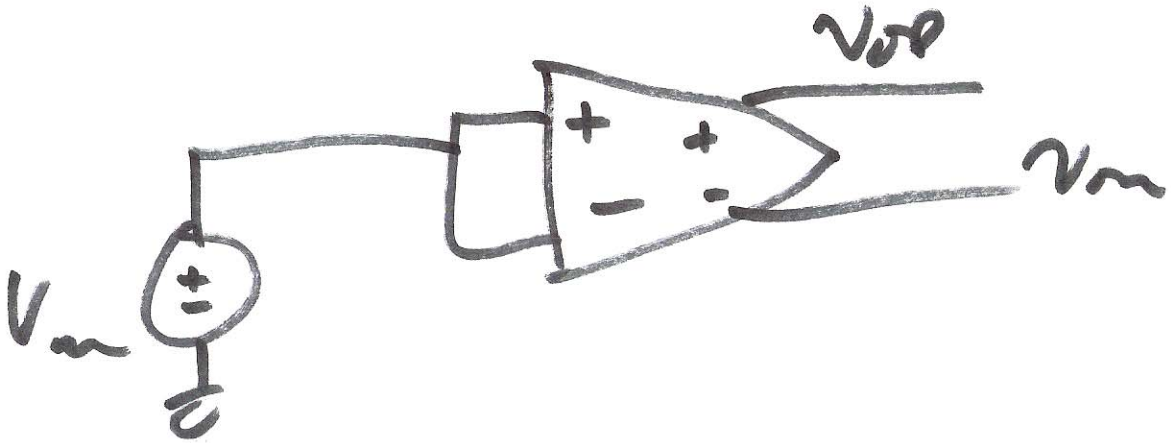


Figure 26.19 Fully-differential cascode diff-amp.



2)

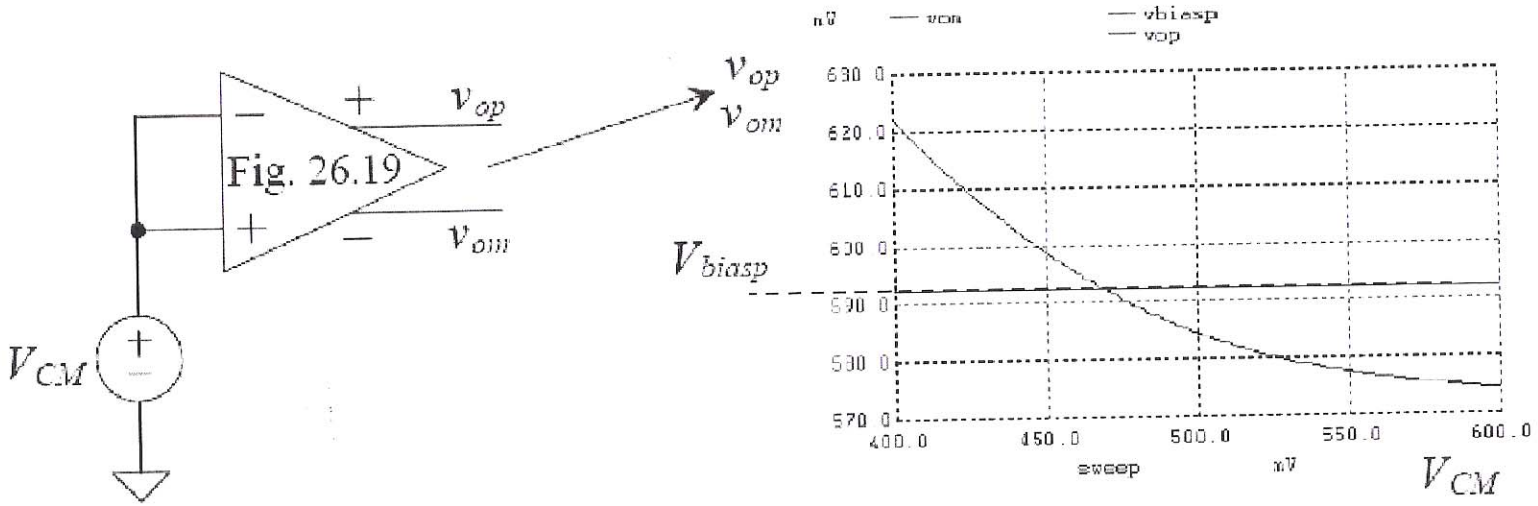


Figure 26.20 Varying the common-mode voltage and looking at the output.

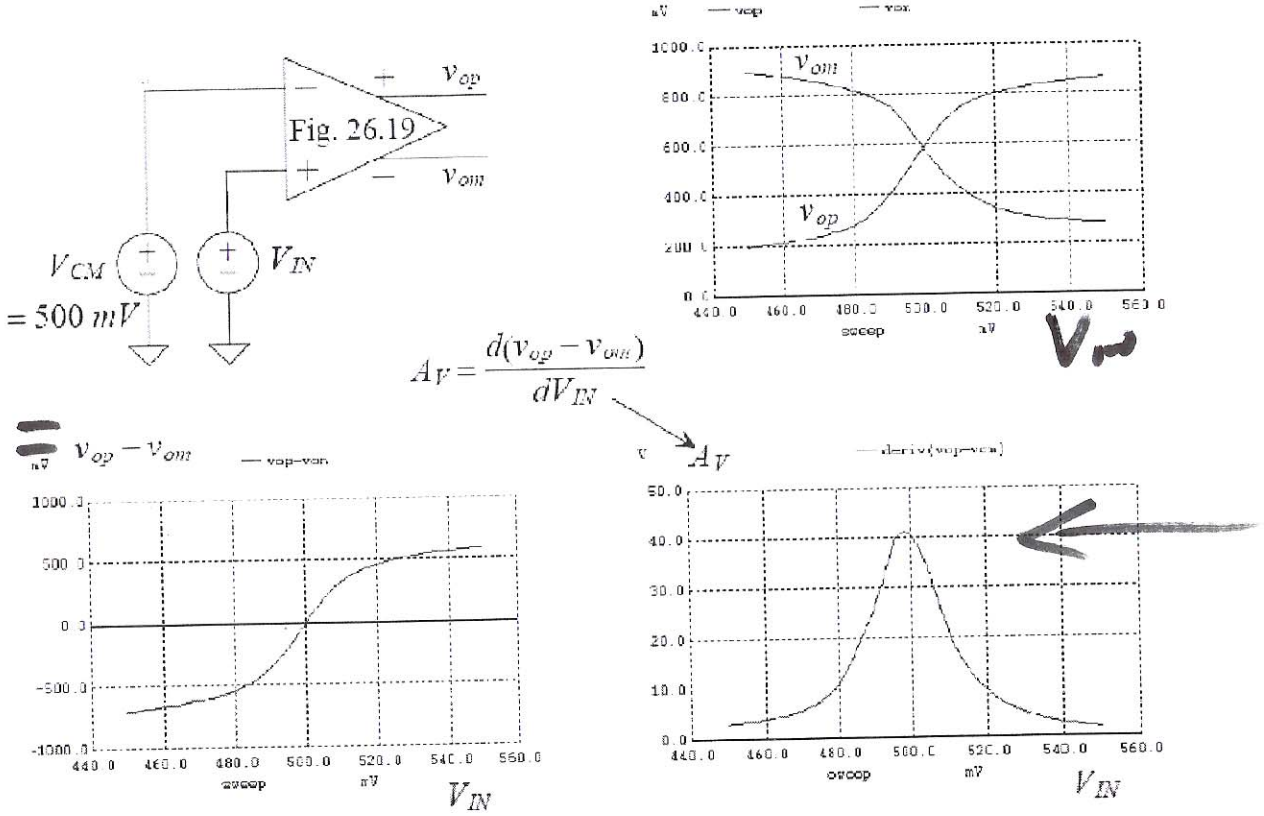
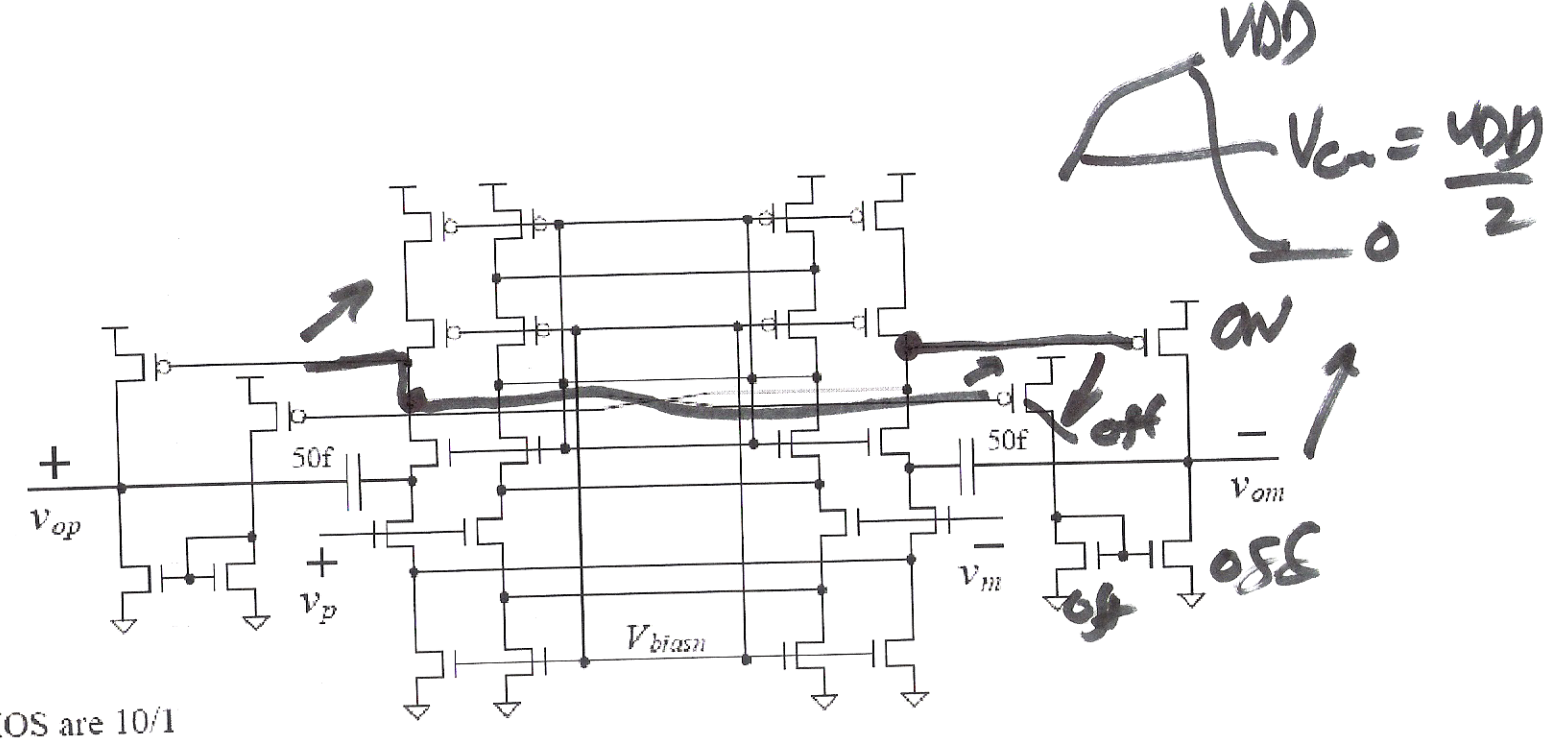
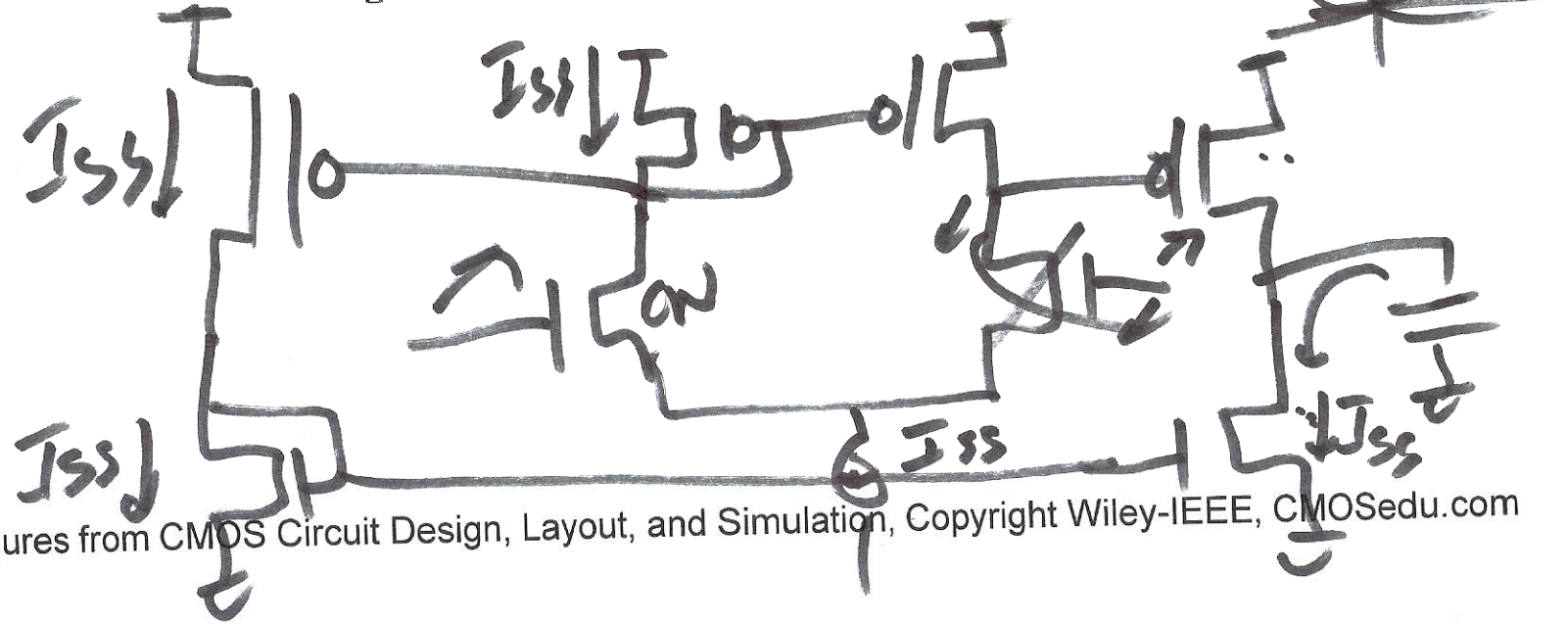


Figure 26.21 DC behavior and gain of the diff-amp in Fig. 26.19.



NMOS are 10/1
PMOS are 20/1
Bias circuit in Fig. 26.3

Figure 26.22 Basic two-stage op-amp without CMFB.



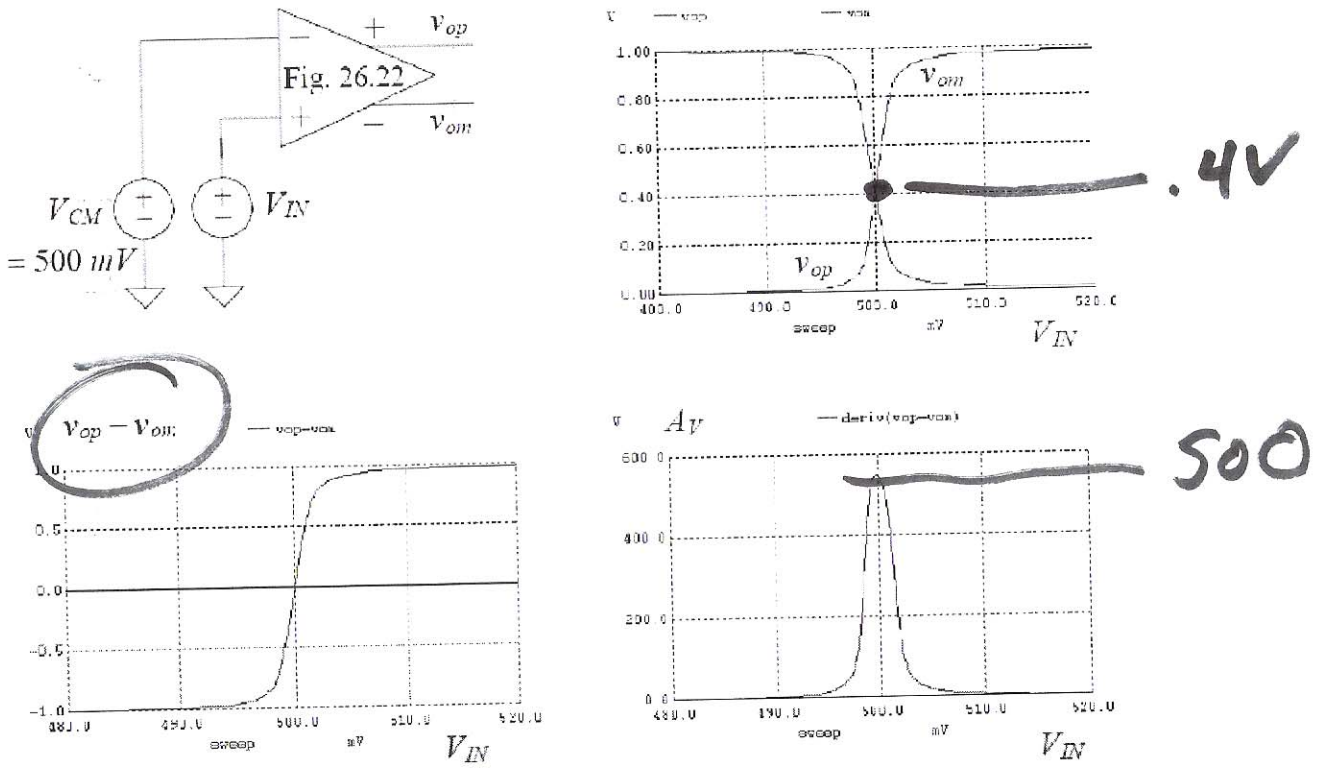


Figure 26.23 DC behavior and gain of the op-amp in Fig. 26.22.

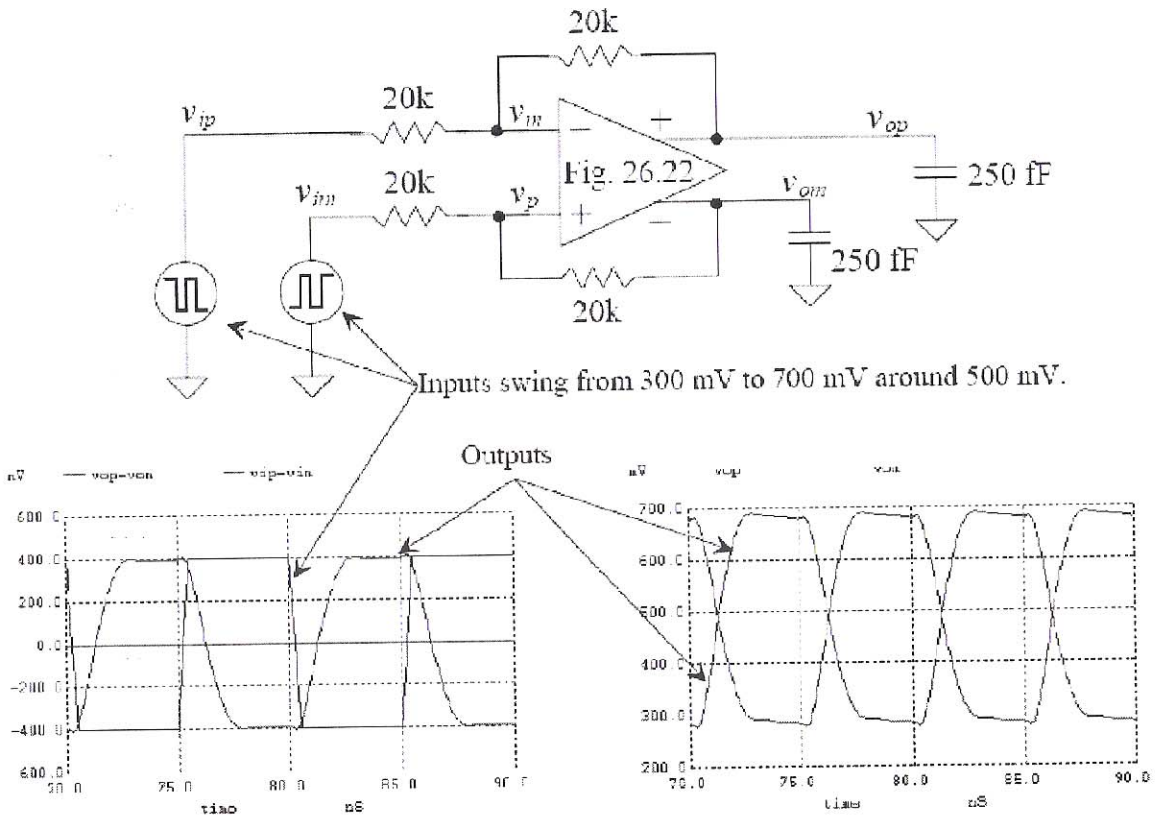


Figure 26.24 Step response of the op-amp in Fig. 26.22 driving 250 fF load capacitors and 20k feedback resistors.

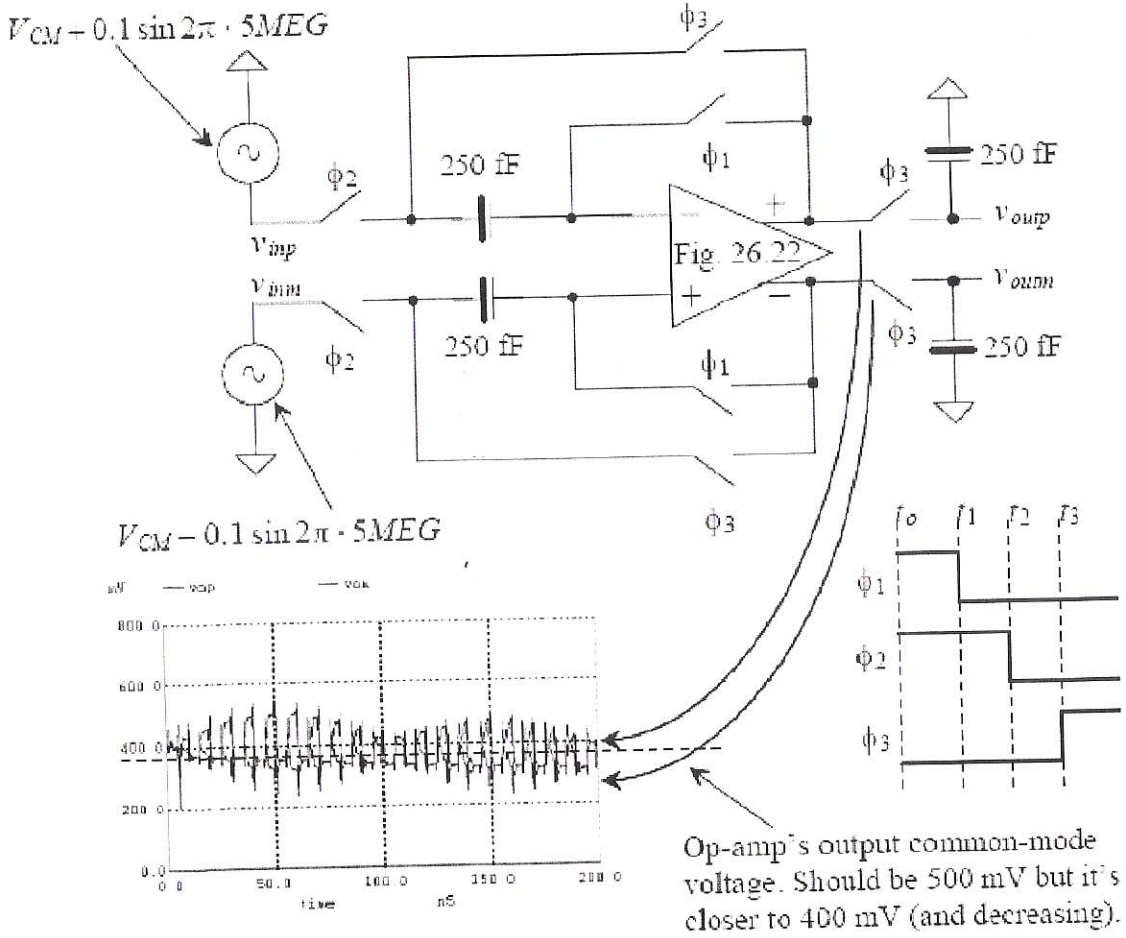


Figure 26.25 A sample-and-hold circuit. Notice how the output common-mode voltage is wandering.

8)

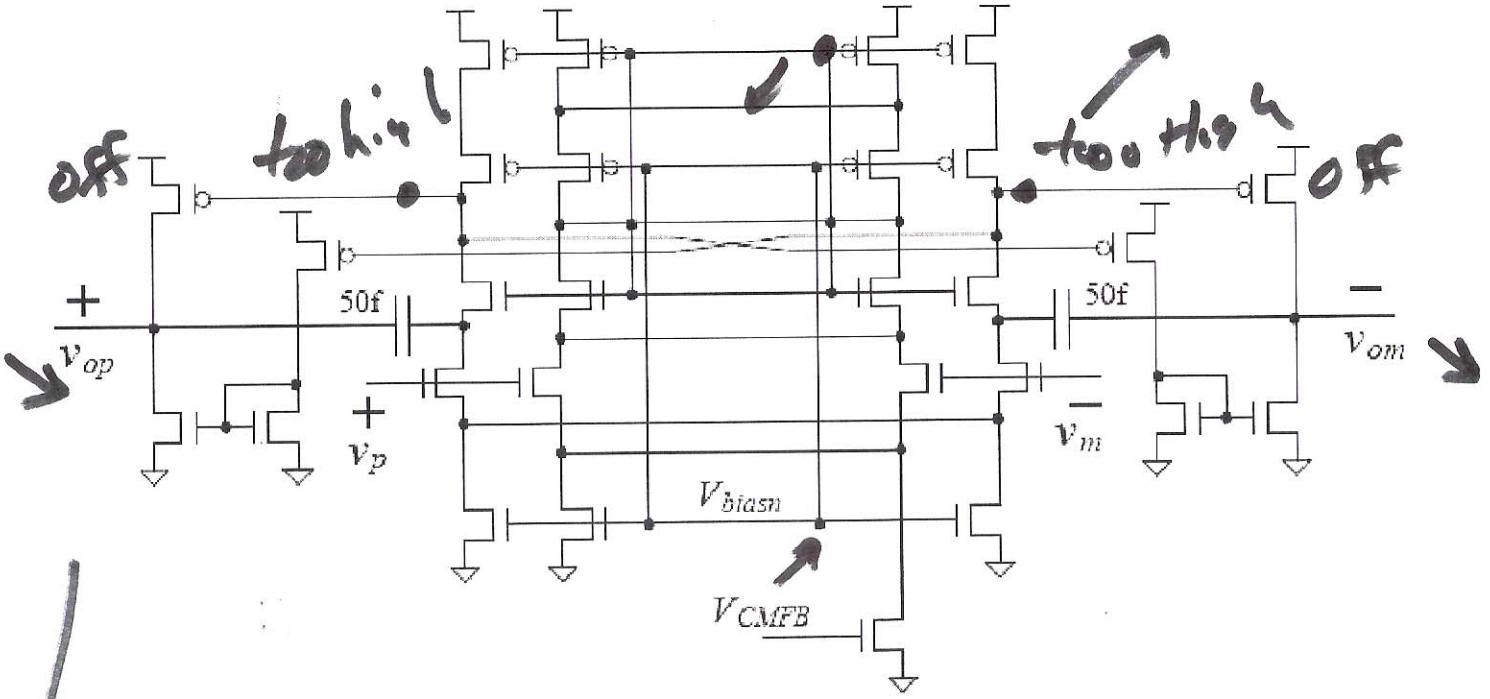
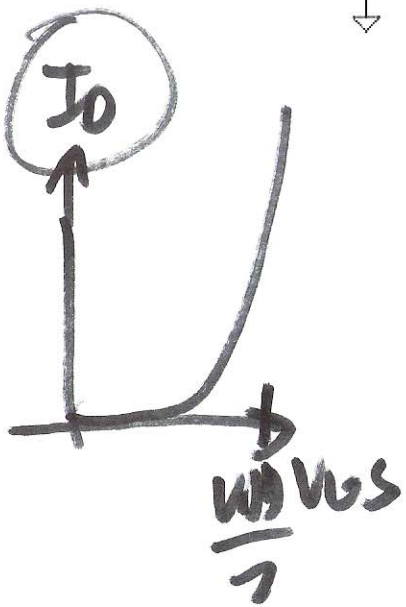
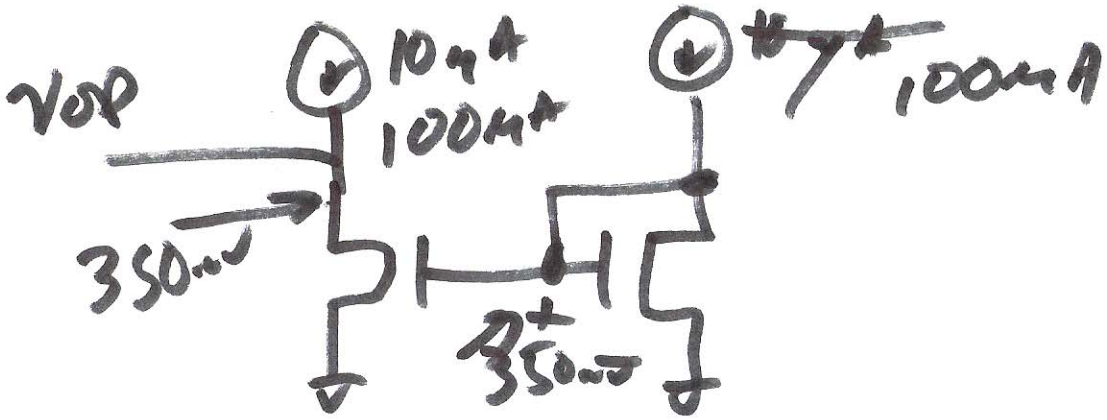


Figure 26.26 Modifying the op-amp for a CMFB input signal.





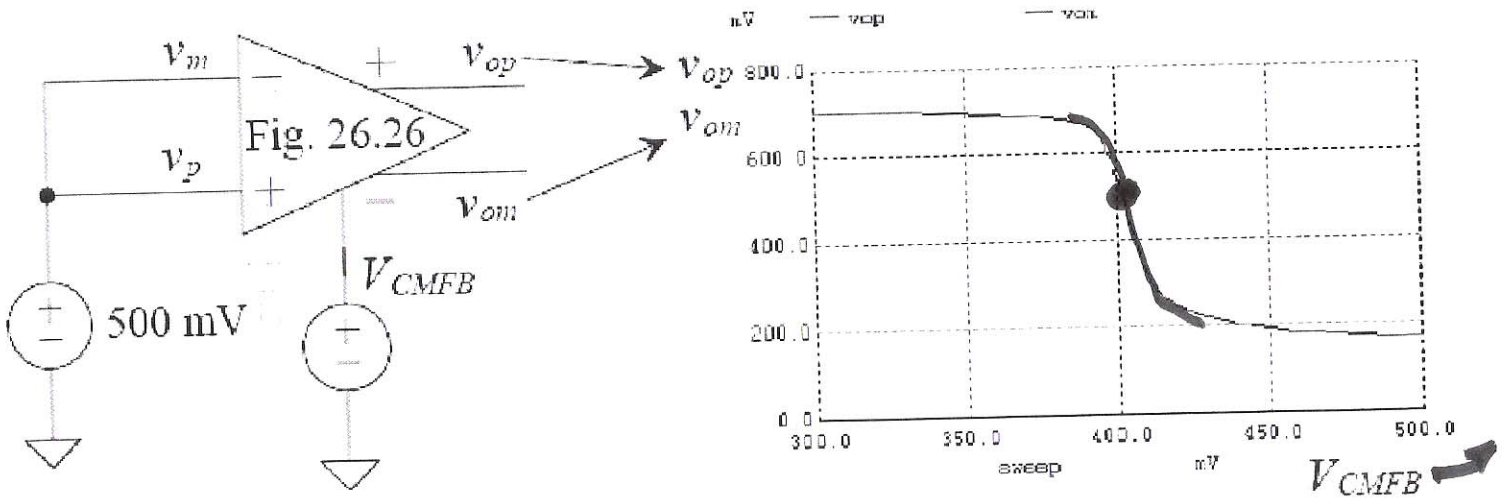


Figure 26.27 The CMFB input to output relationship. The gain is approximately 25 (considerably less than the forward differential gain).

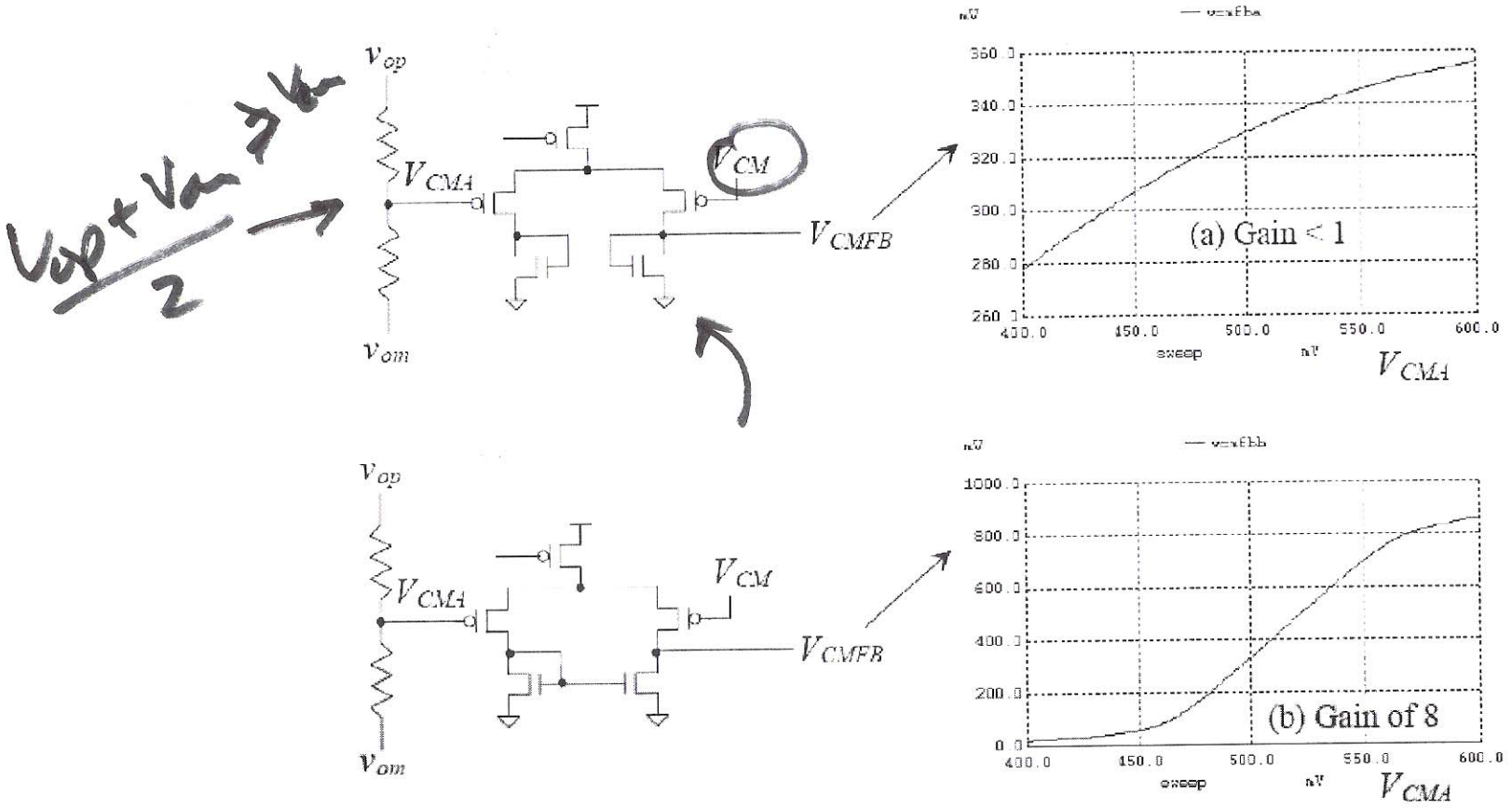


Figure 26.28 Gains of CMFB amplifiers.

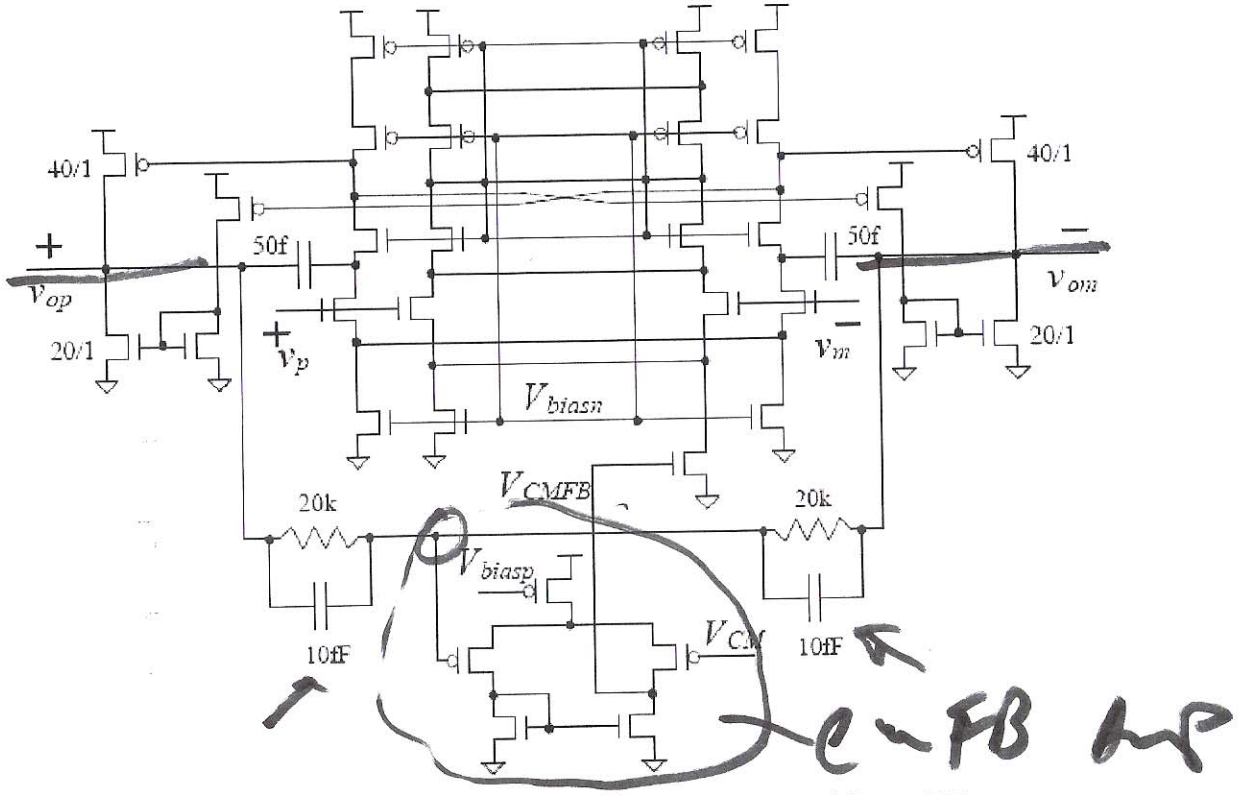


Figure 26.29 Complete schematic of op-amp with CMFB.

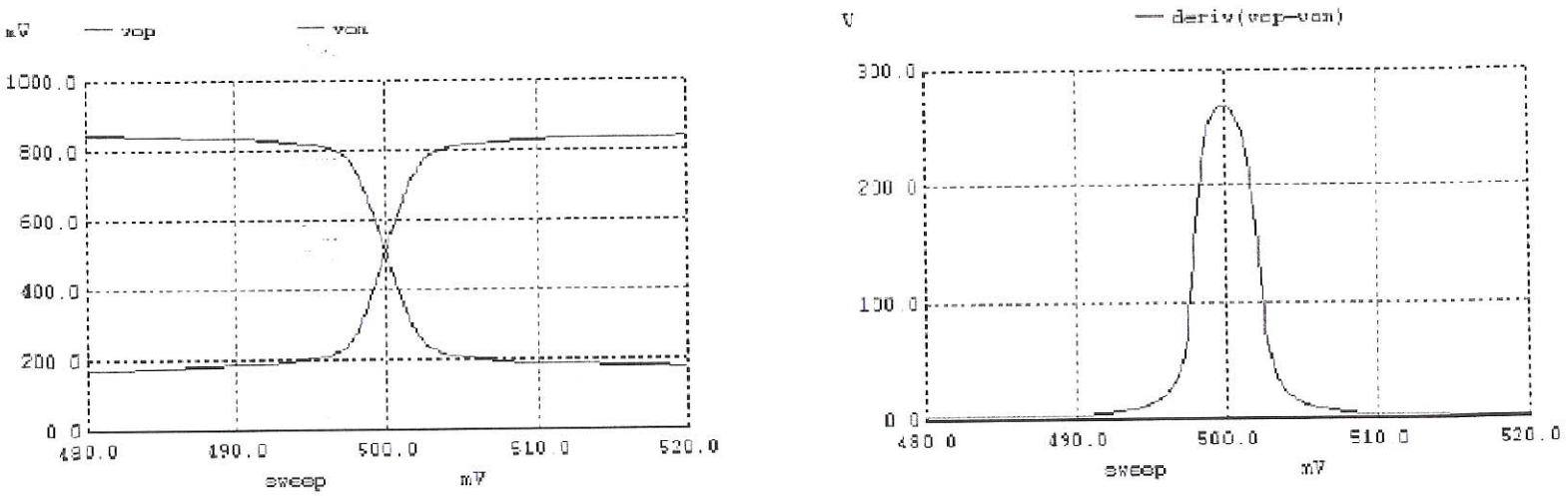


Figure 26.30 Simulating the operation of the op-amp in Fig. 26.29.

See Sim

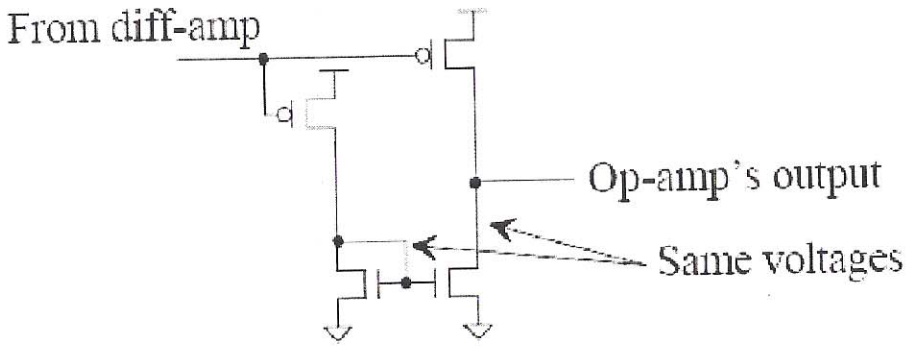


Figure 26.31 Output buffer used in the op-amp of Fig. 26.29.

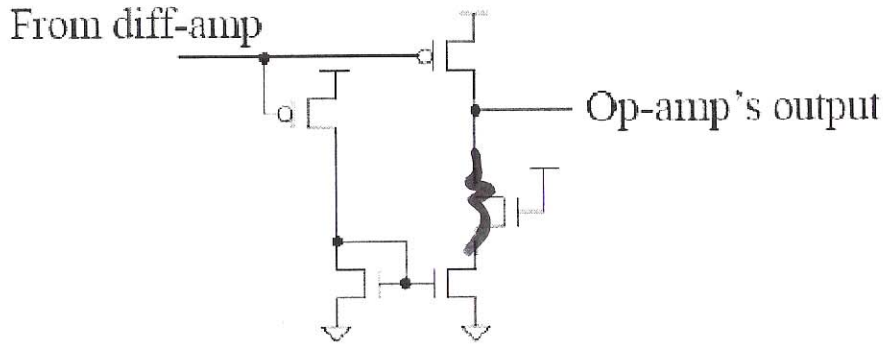


Figure 26.32 Adding a device to allow the output voltage to swing.

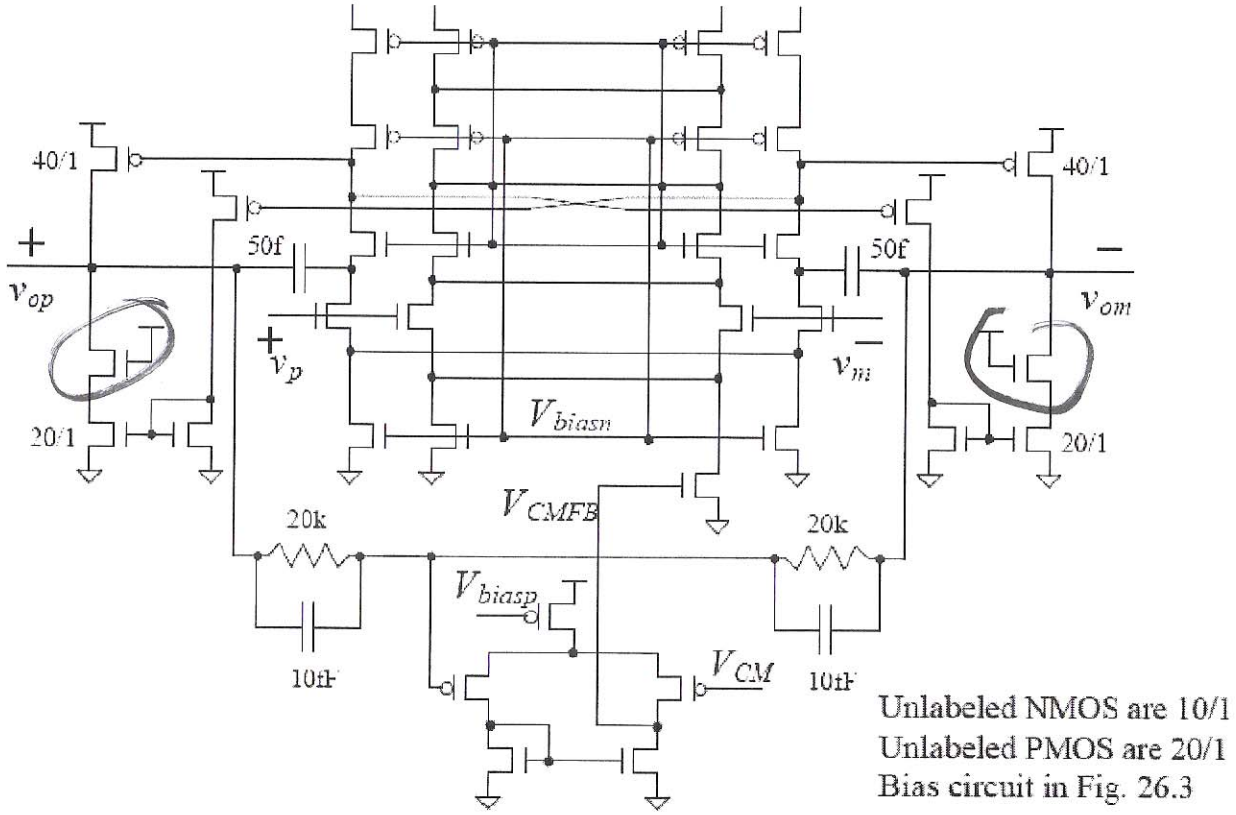
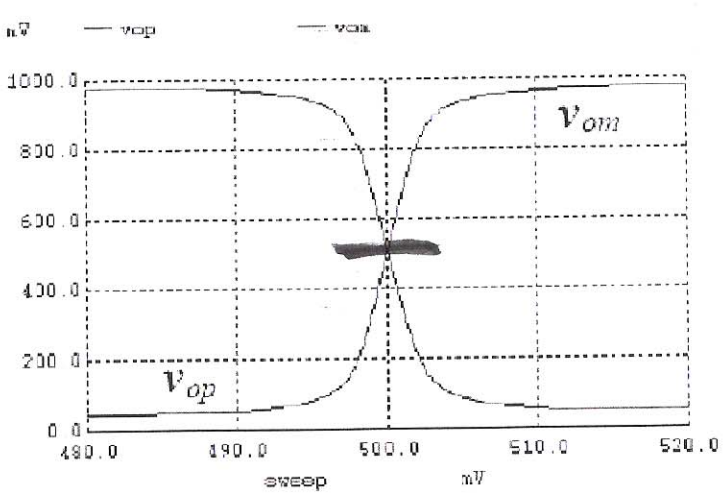


Figure 26.33 Op-amp with modified output buffer.

not the best solution

16)



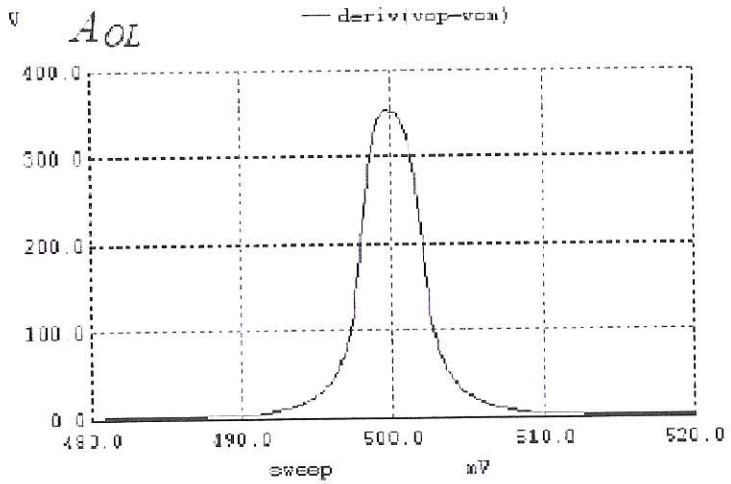


Figure 26.34 Resimulating the op-amp in Fig. 26.33 in the configuration seen in Fig. 26.23.

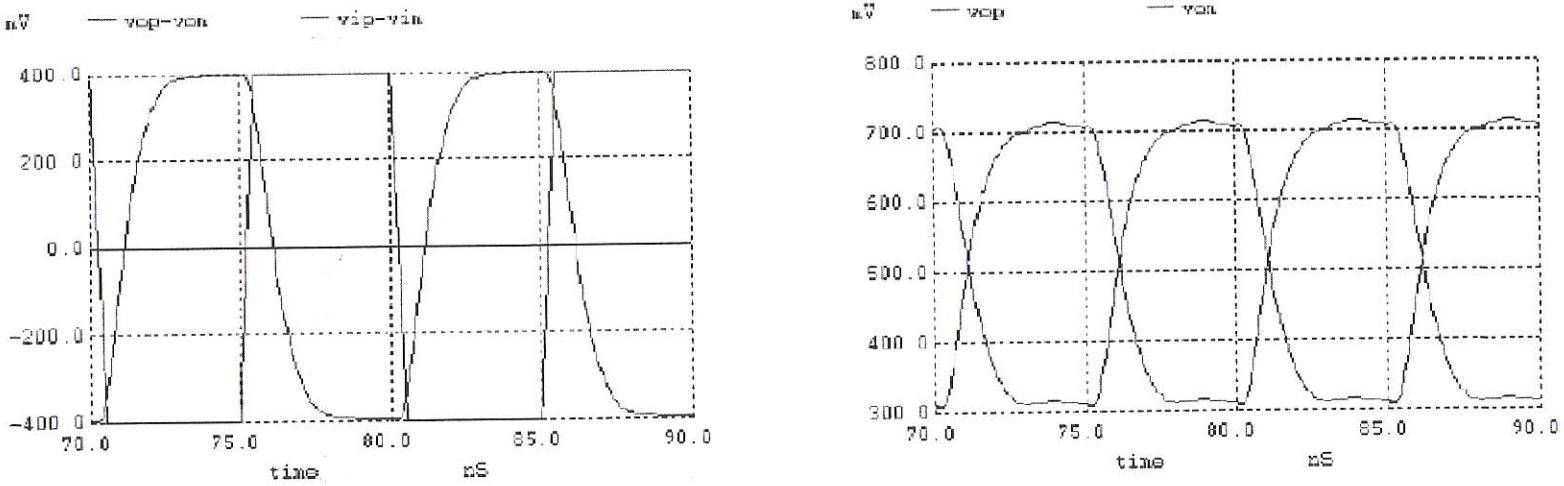


Figure 26.35 Regenerating the simulation results using the topology in Fig. 26.24 with the op-amp in Fig. 26.33.

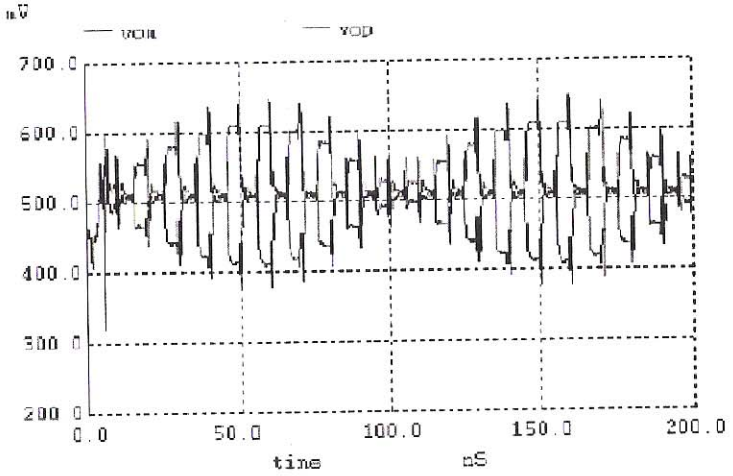


Figure 26.36 Using the op-amp in Fig. 26.33 in the sample-and-hold circuit of Fig. 26.25. Figure shows the outputs of the op-amp.

no drift

A portion of the output buffer.

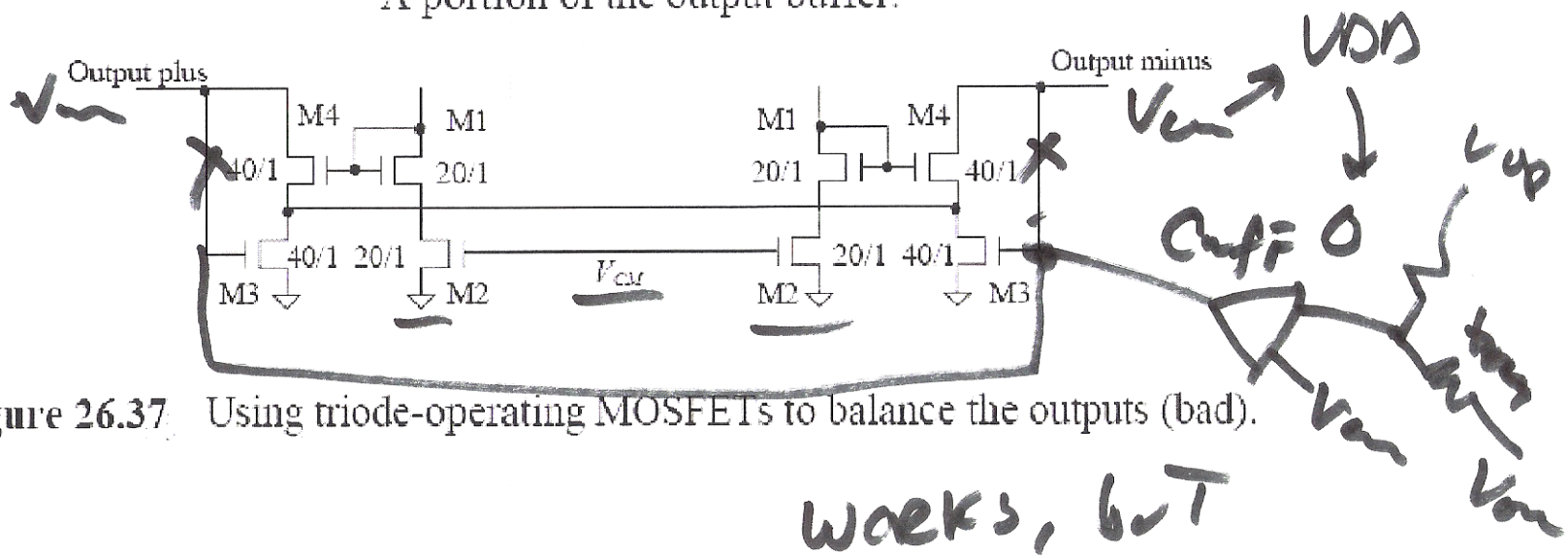


Figure 26.37 Using triode-operating MOSFETs to balance the outputs (bad).

works, but not great

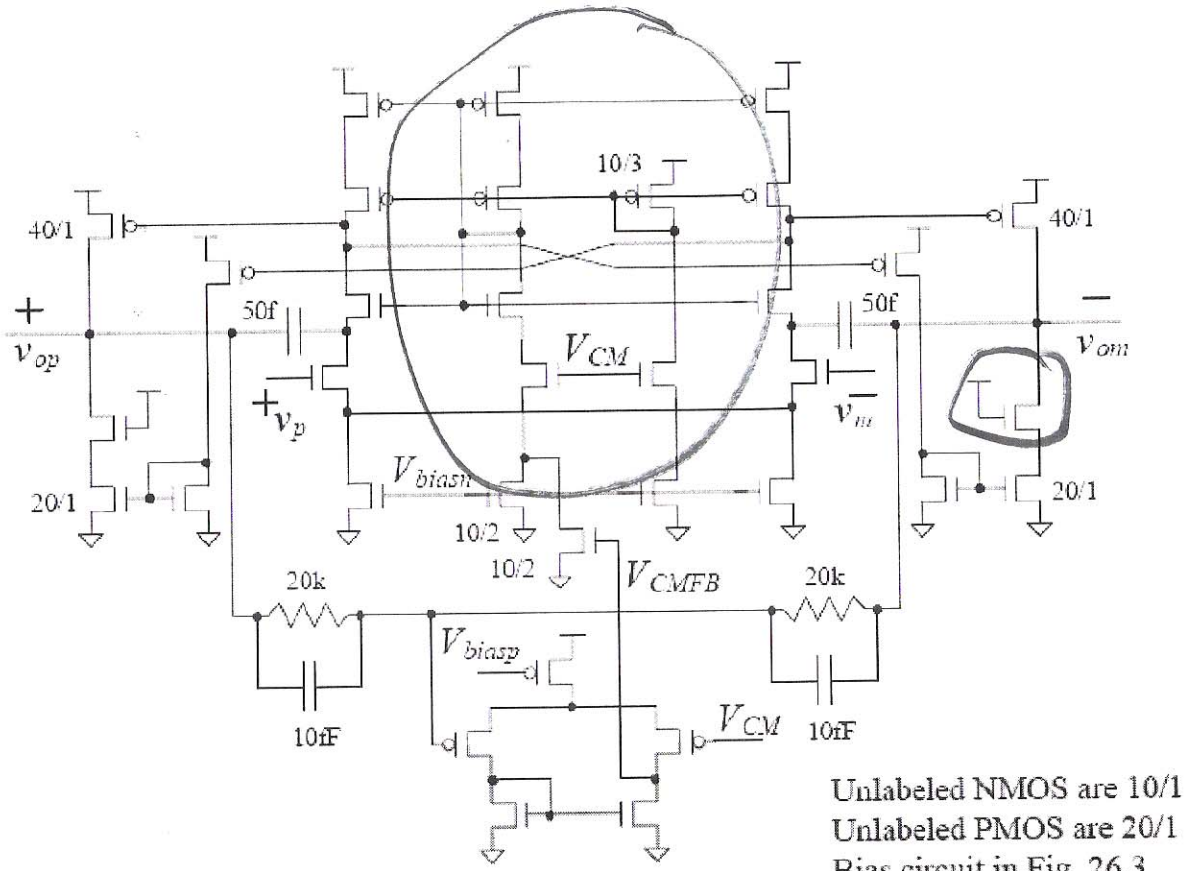


Figure 26.40 Making the op-amp more practical.

21)

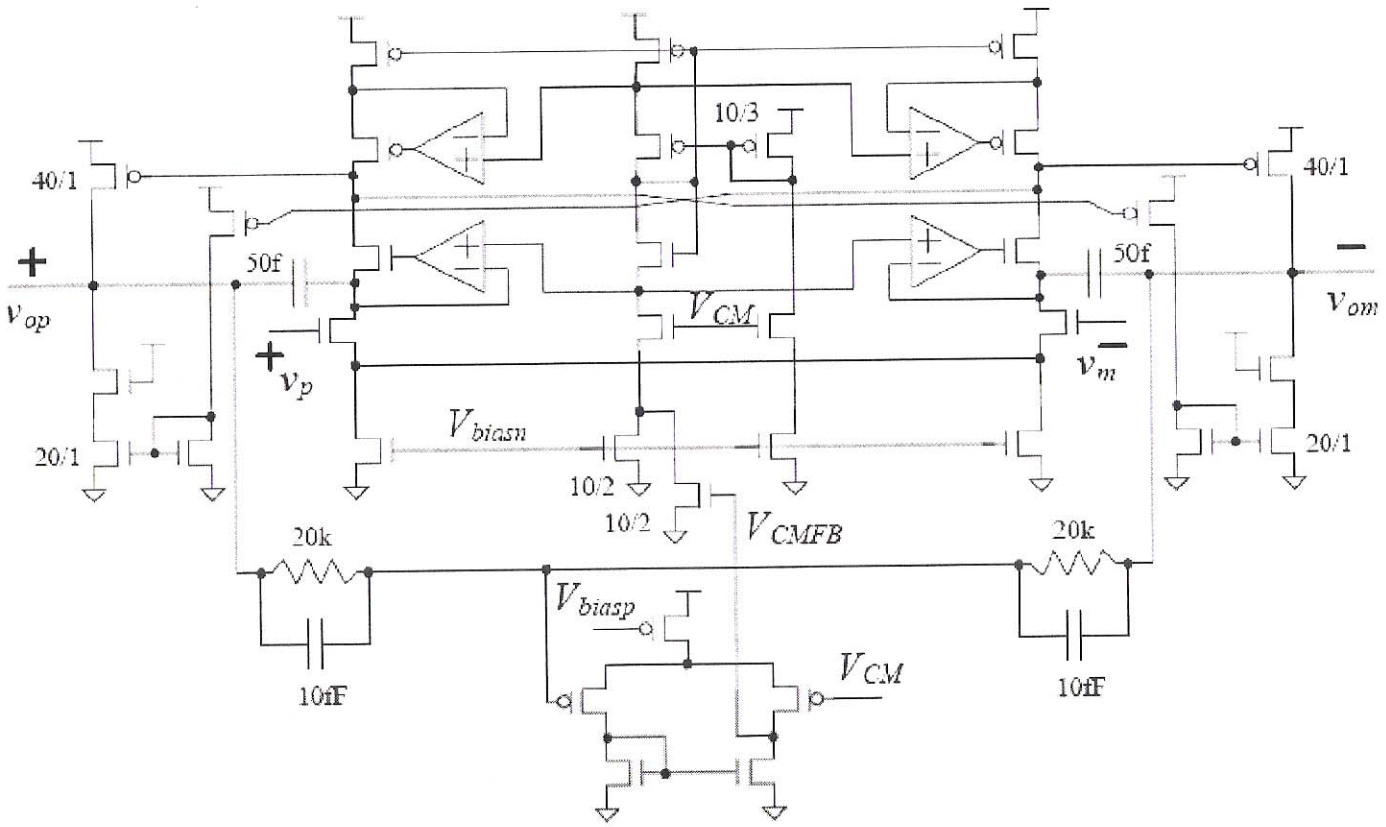


Figure 26.42 Adding gain-enhancement to the op-amp.

GAIN ENHANCEMENT

BOOST ENHANCEMENT

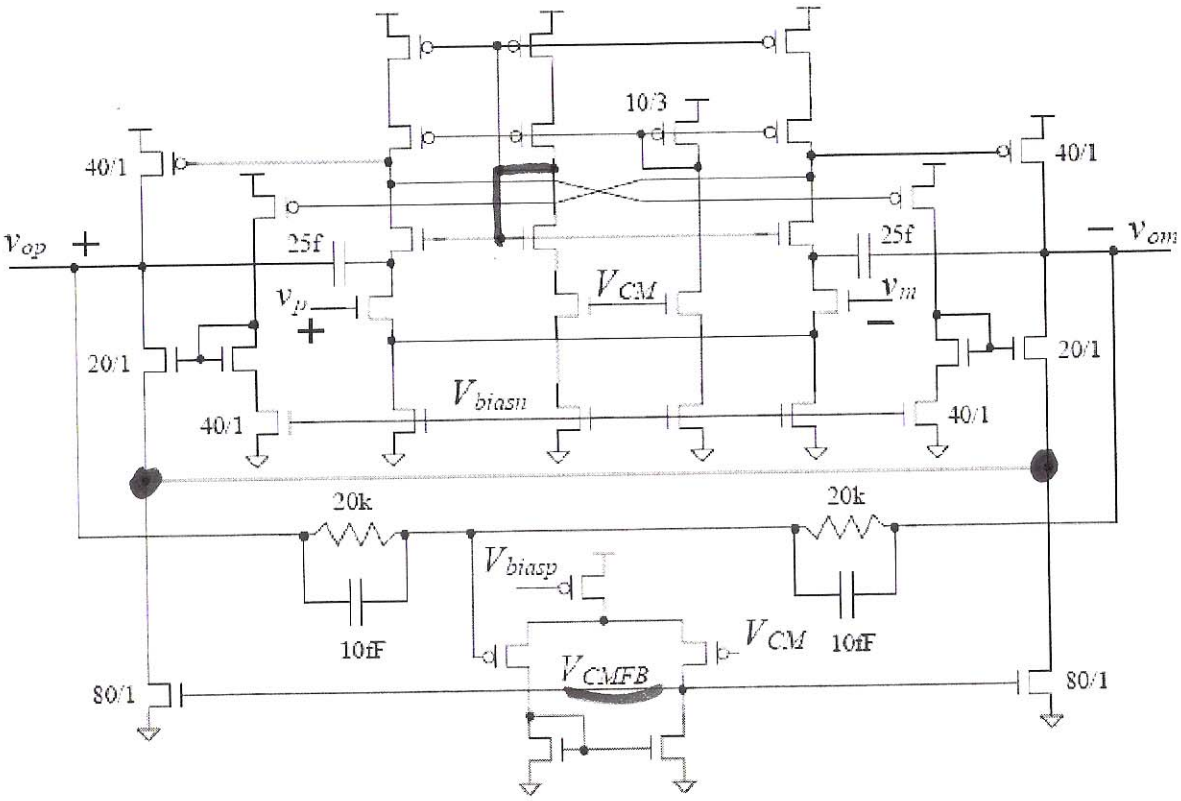


Figure 26.43 Providing CMFB through just the output buffer. Using an amplifier with triode-operating MOSFETs for CMFB (good).