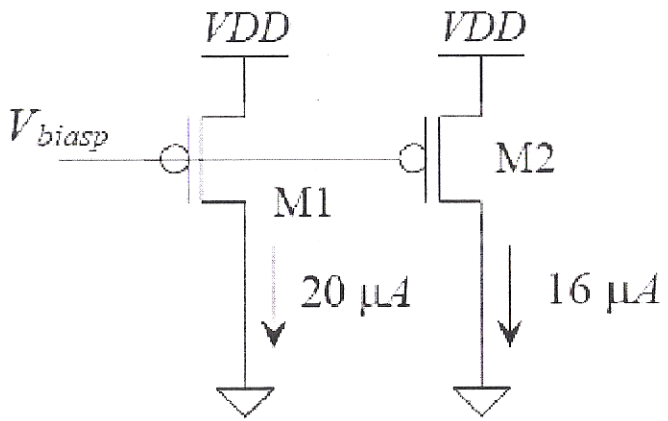
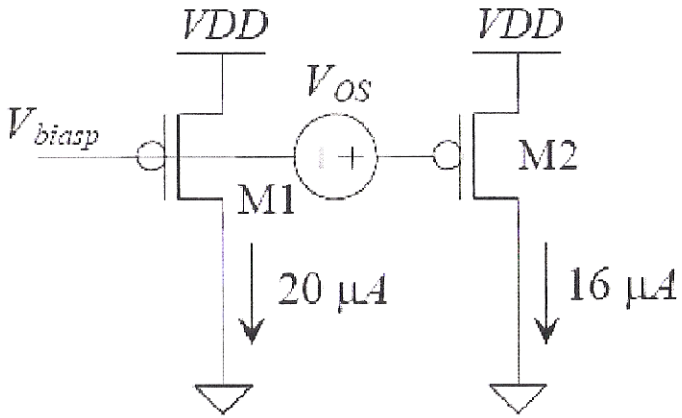
26.2



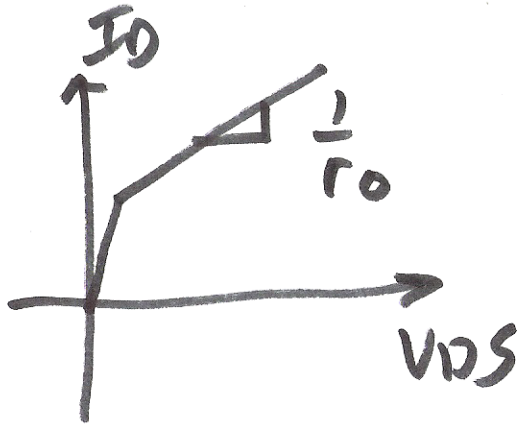
(a) M1 and M2 are mismatched.

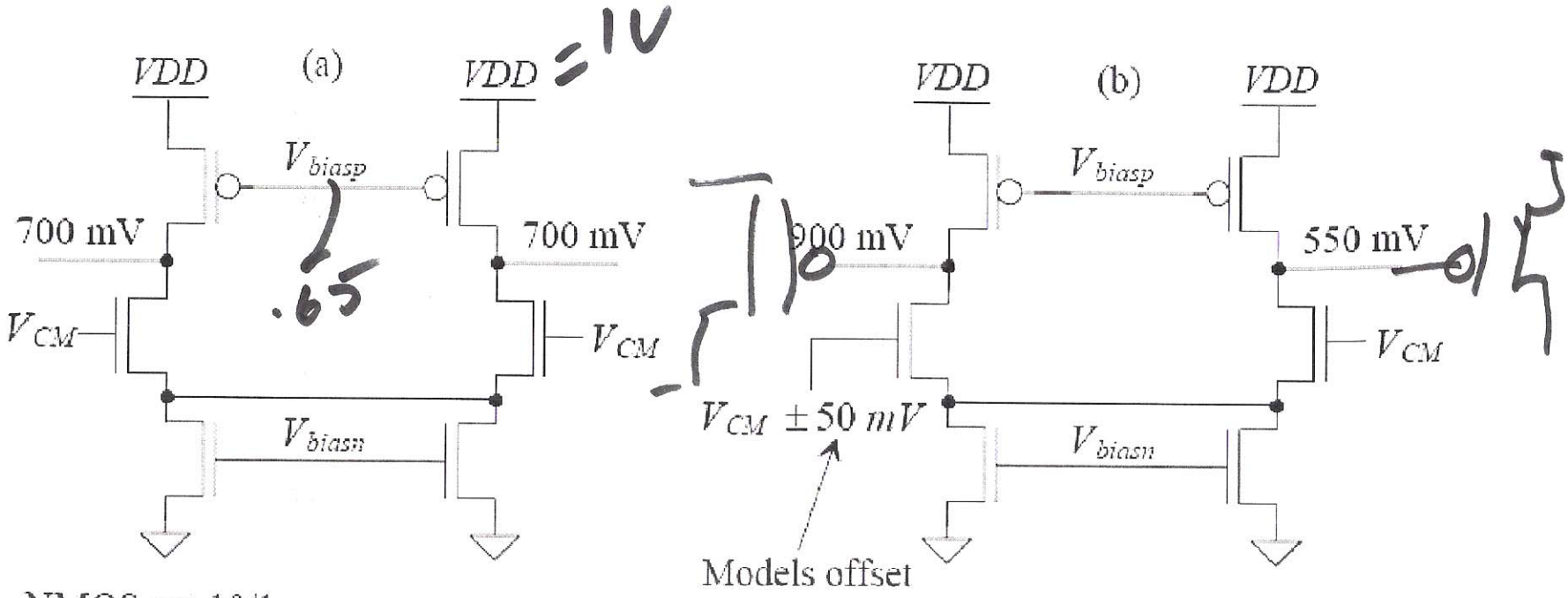


(b) M1 and M2 are perfectly matched (as in a SPICE simulation).

Figure 26.5 How we add an offset into the circuit to model mismatch.

26.20





NMOS are 10/1
PMOS are 20/1
Bias circuit seen in Fig. 26.3

$V_{CM} = VDD/2 = 500\ mV$

Figure 26.6 Comparing the diff-amp's output voltages with and without an offset.

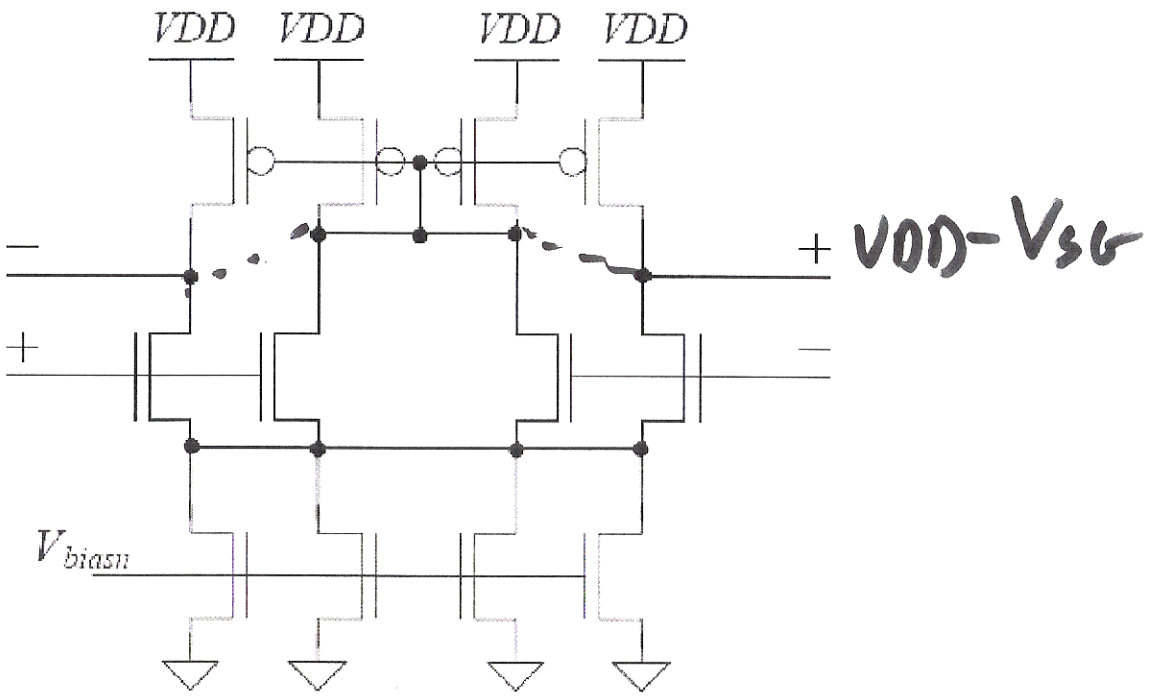


Figure 26.7 A fully-differential diff-amp that generates its own bias for the PMOS.

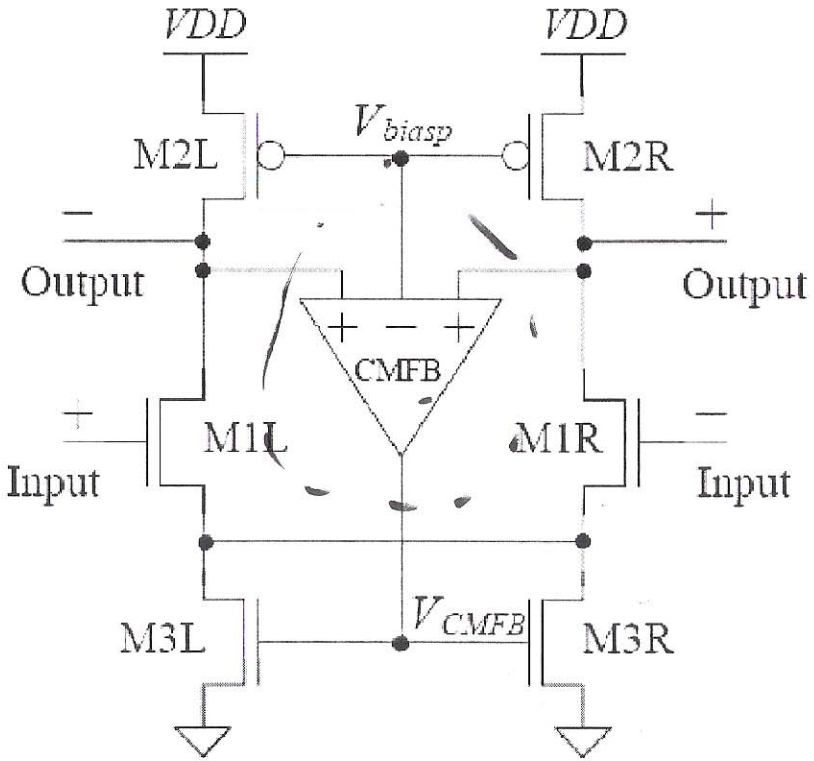
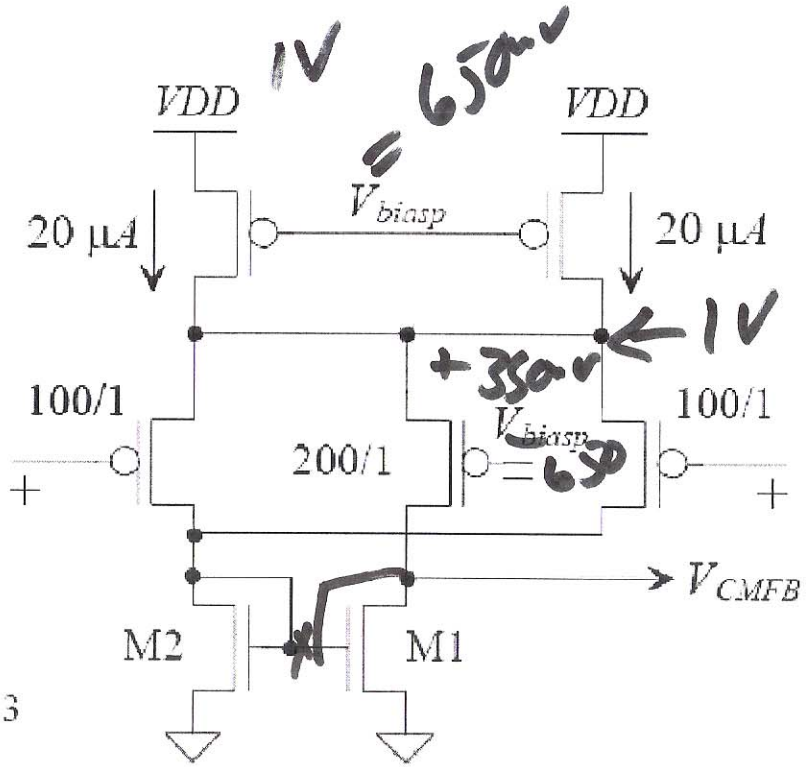
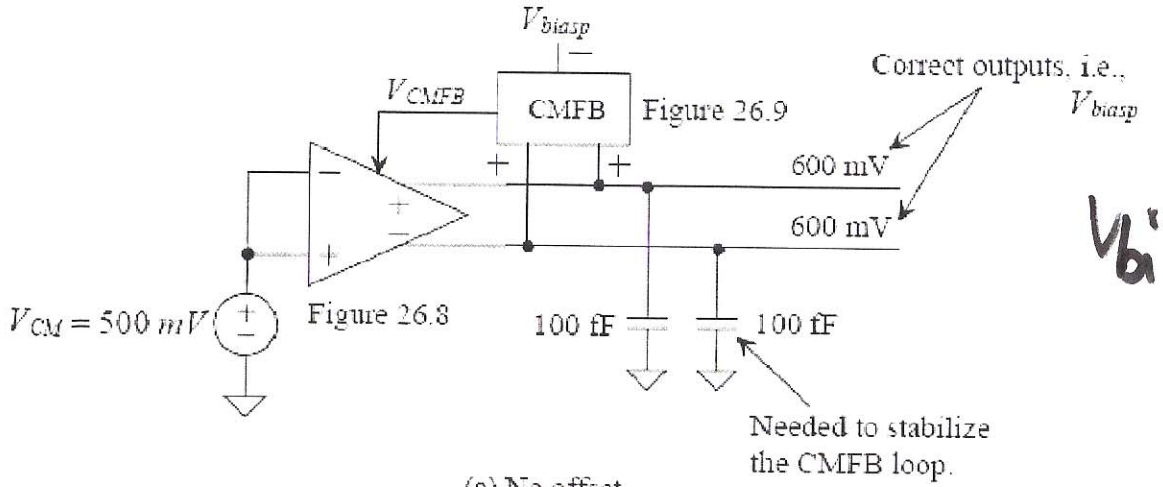


Figure 26.8 Using a common-mode feedback (CMFB) amplifier to set the output voltages.

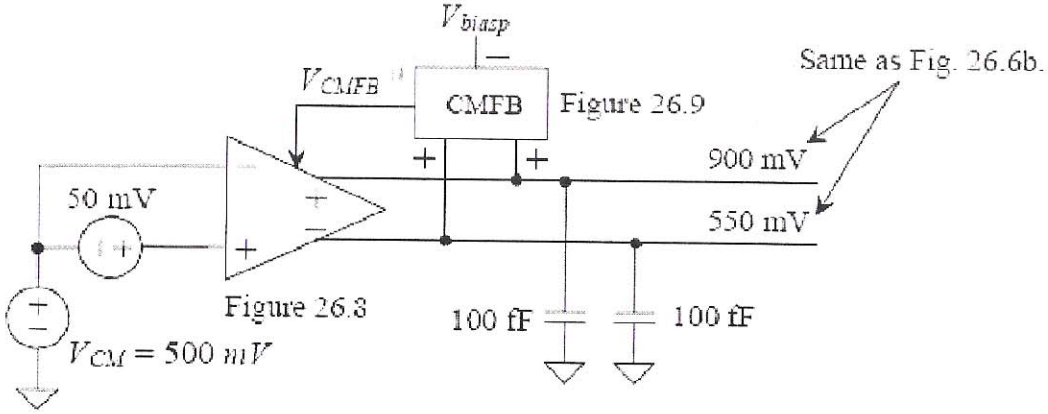


NMOS are 10/1
Unlabeled PMOS are 20/1
Bias circuit seen in Fig. 26.3

Figure 26.9 Implementation of the CMFB amplifier in Fig. 26.8.



(a) No offset



(b) With a 50 mV offset. Note how the CMFB isn't doing anything.

Figure 26.10 Simulating the operation of the CMFB circuit in Fig. 26.9.

$V_{GS} = 400mV$

$V_{biasp} = 600mV$

b)

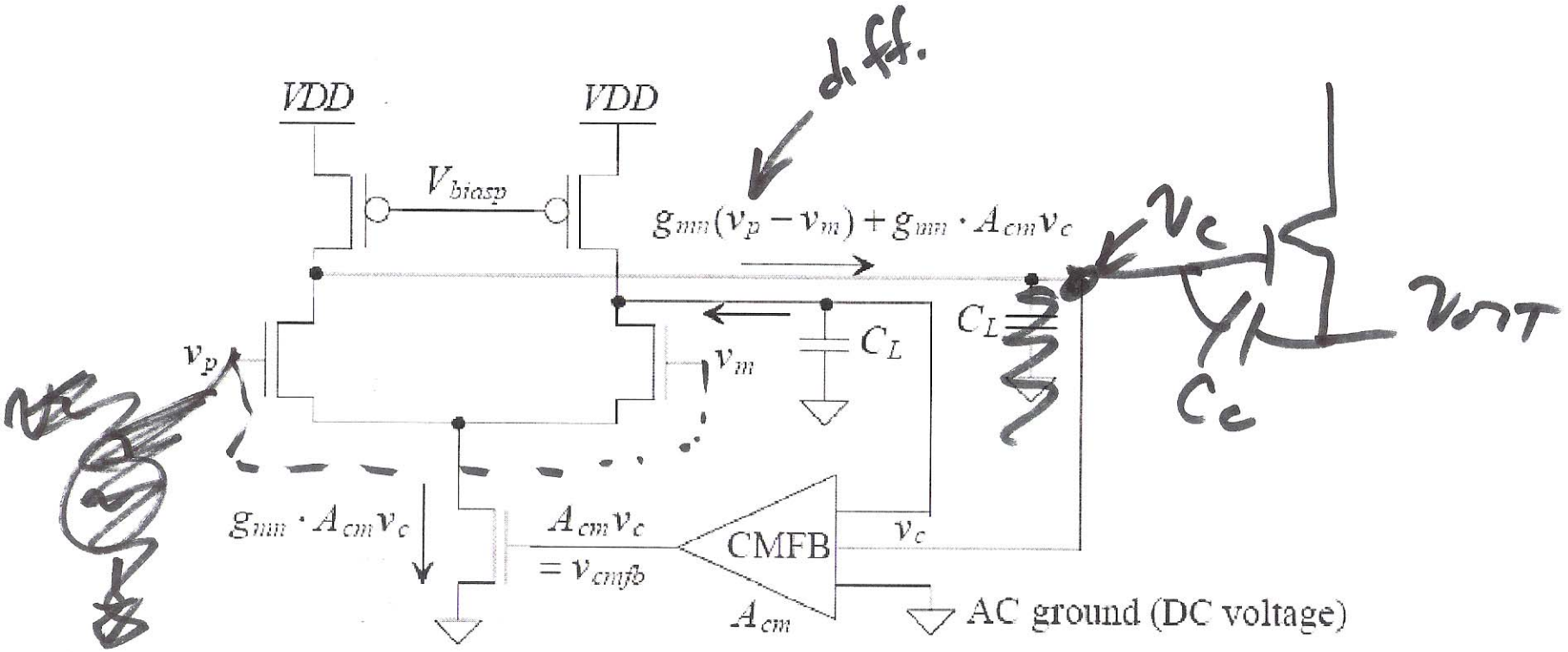


Figure 26.11 Schematic view of differential and CM feedback.

$$\frac{v_c}{v_{CI}} = \left| g_m \cdot A_{cm} \cdot \frac{1}{j\omega C_L} \right| = 1$$

$$f_{u,cm} = \frac{g_m A_{cm}}{2\pi \cdot C_L} \quad (26.2)$$

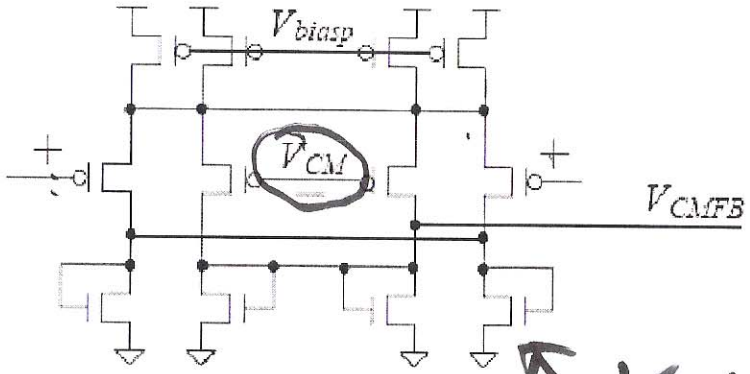


Figure 26.12 A CMFB amplifier with a gain of nominally unity.

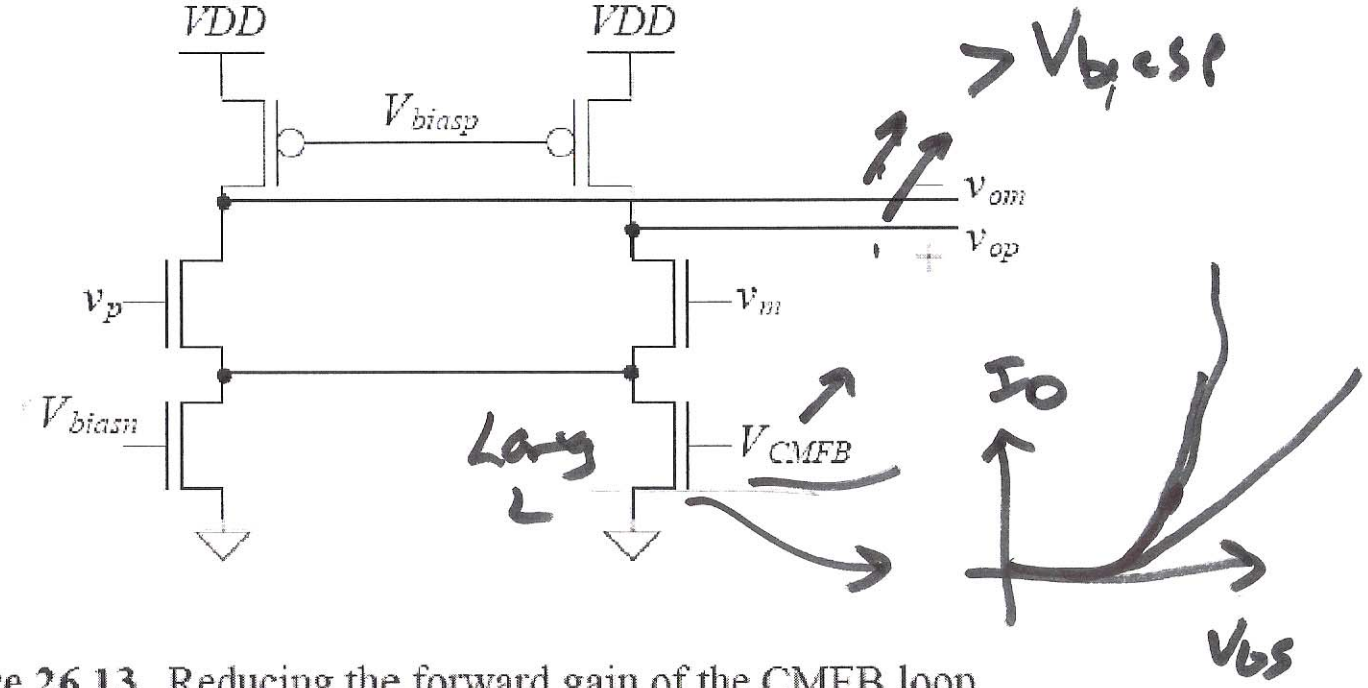
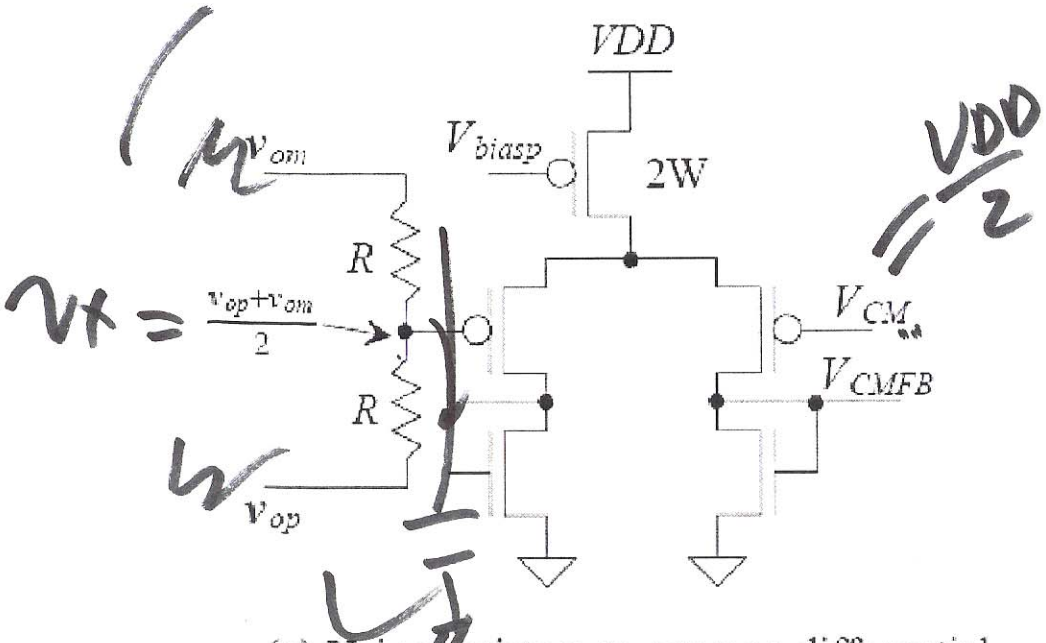


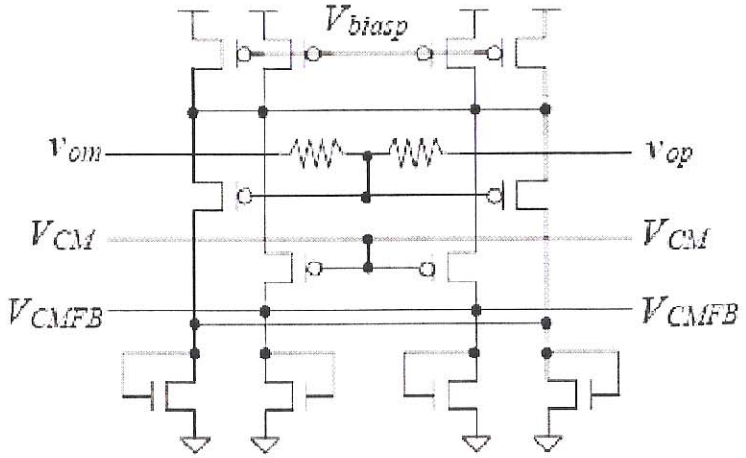
Figure 26.13 Reducing the forward gain of the CMFB loop.

NMOS - diff-Amp

9)



(a) Using resistors to average differential output signals.



(b) Symmetrical implementation of the CMFB circuit in (a).

Figure 26.14 Increasing CMFB amplifier input range.

$$\frac{v_{op}+v_{om}}{2} = \left(\frac{v_{om}-v_{op}}{2R}\right)R + \frac{2V_{DP}}{2} = v_x$$

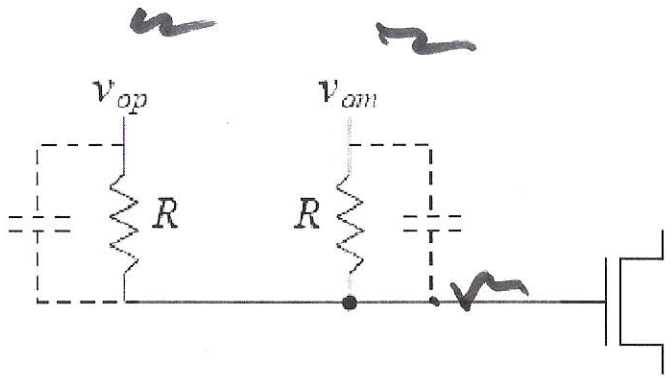


Figure 26.15 Adding parasitic capacitances across the resistors to compensate for the input capacitance of the MOSFET.

ideal output of diff-amp

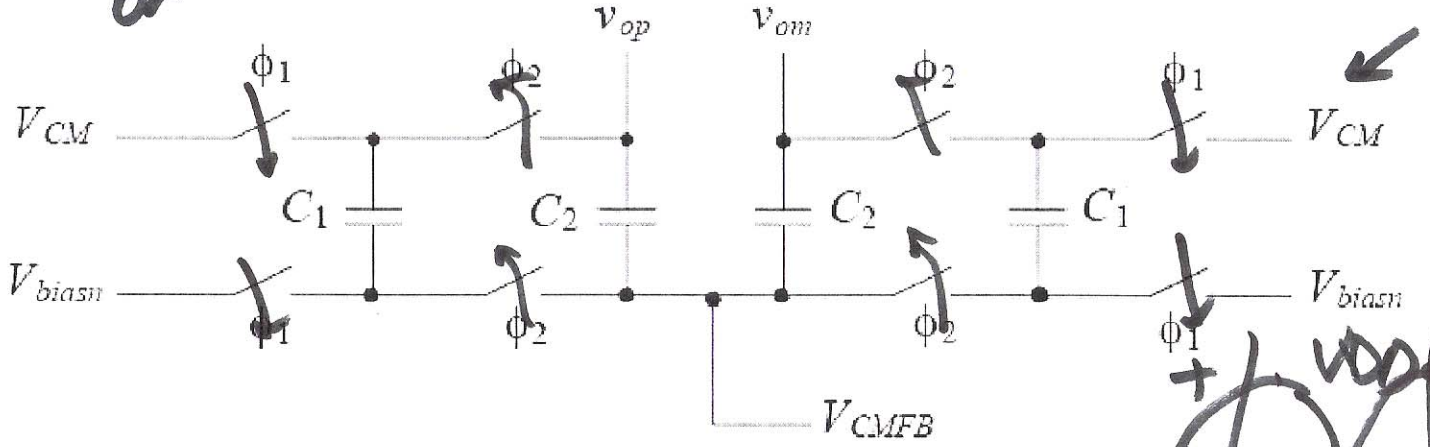
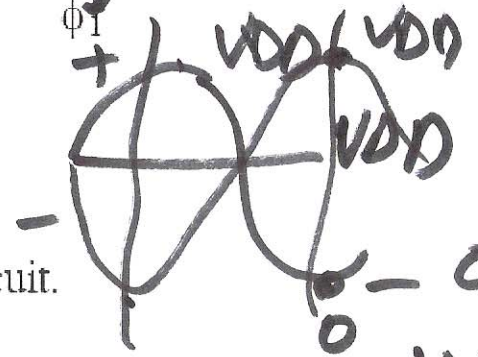


Figure 26.16 A switched-capacitor CMFB circuit.

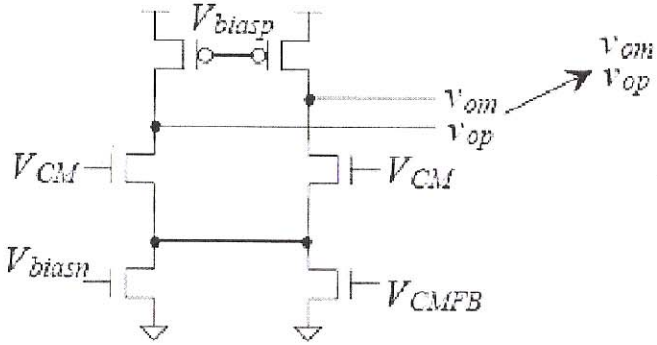


$V_+ - V_- = VDD$

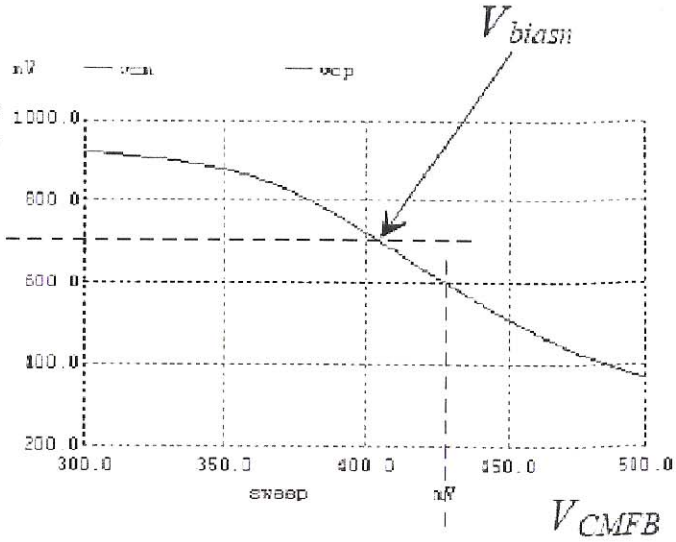
$V_+ - V_- = 0 - VDD$

$= -VDD$

12)



NMOS 10/1
PMOS 20/1
Bias circuit from Fig. 26.3



Value of CM feedback voltage when the outputs are 600 mV.

Figure 26.17 Plotting the output voltages as a function of the CM feedback voltage.