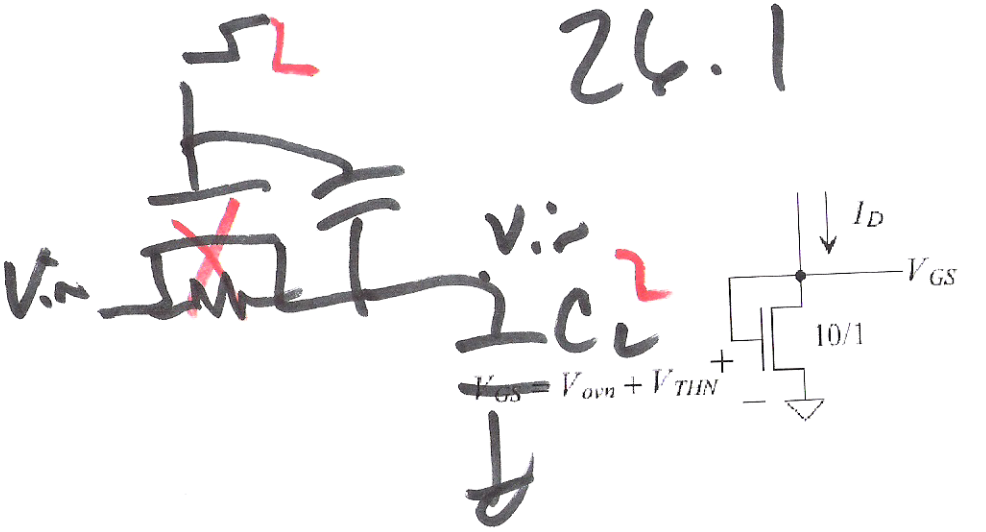
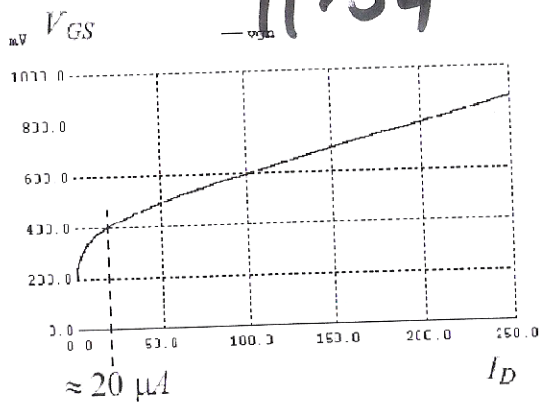
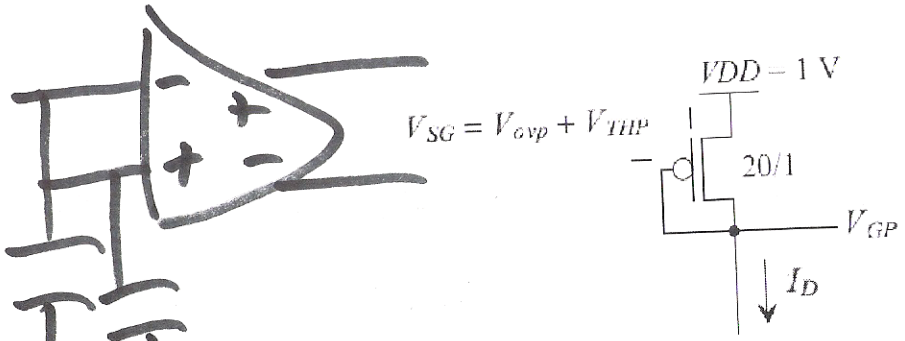
26.1 Basic Biasing for power & speed

11:54







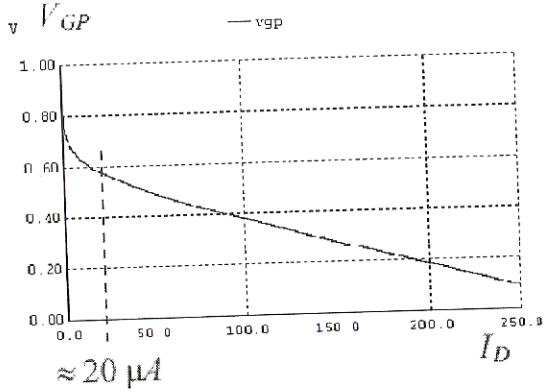
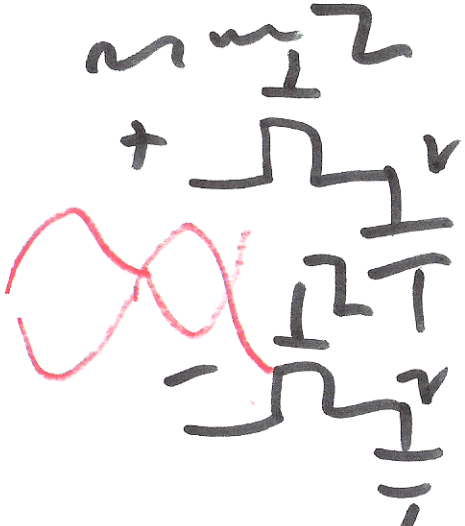


Figure 26.1 Gate-source voltages plotted against drain currents.

1) f_T
2) overdrive
3) current



quiescent current $\frac{I}{C_{load}} = \frac{dV}{dT}$

1)

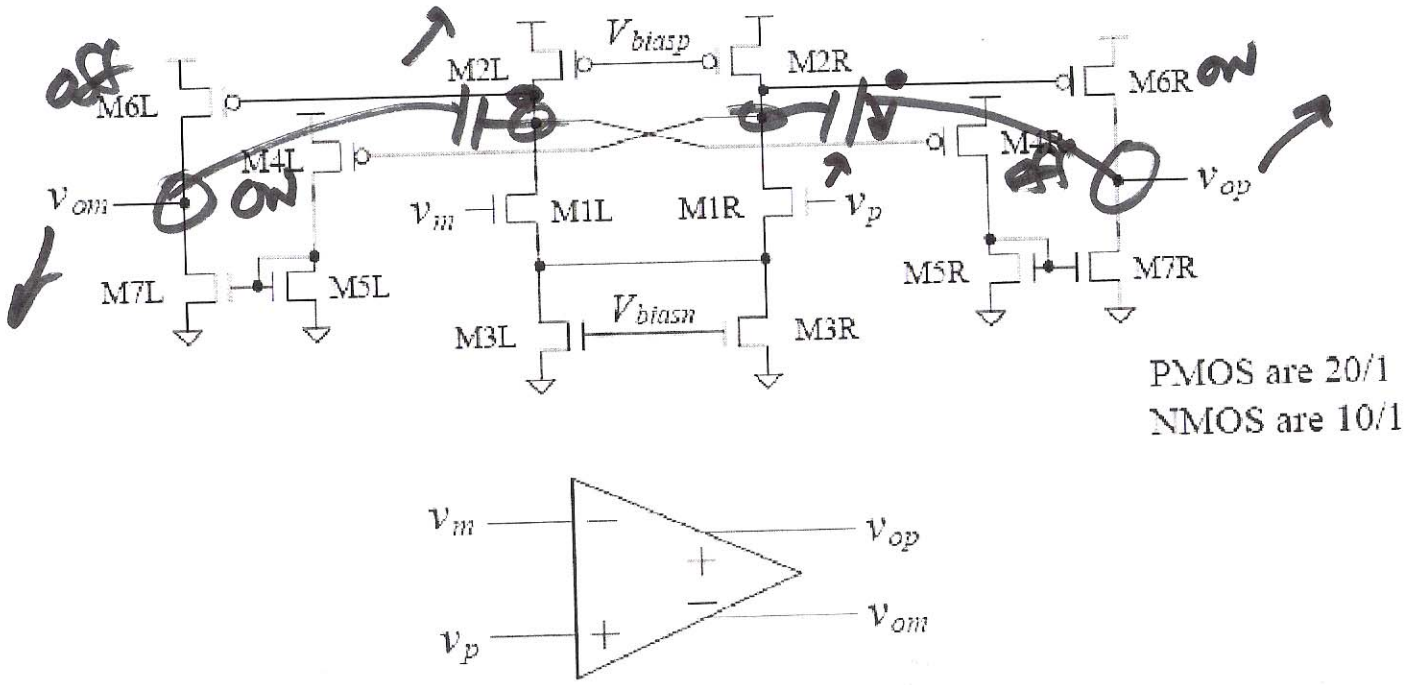


Figure 26.2 A two-stage fully-differential op-amp. Compensation and CMFB are not shown. Output stage operates class AB. See discussion in the next section concerning the output voltage of the diff-amp.

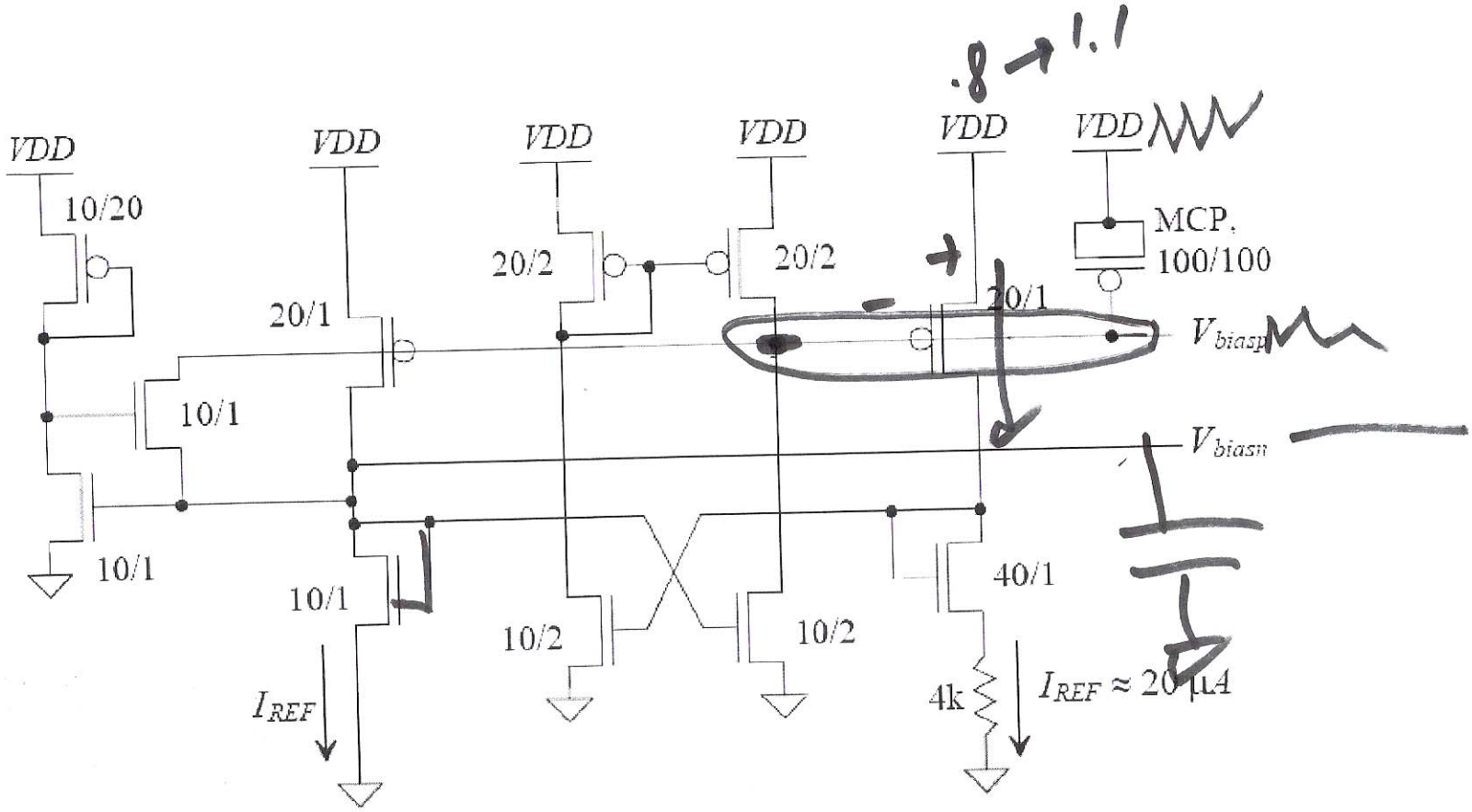
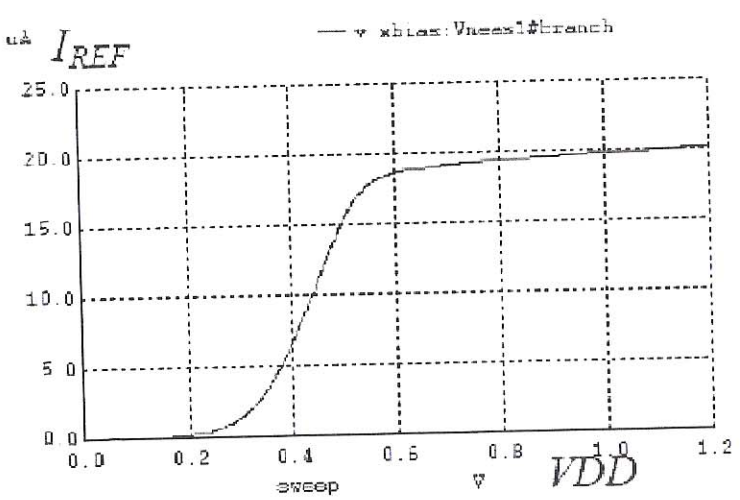


Figure 26.3 Biasing circuit used in this chapter. This bias circuit pulls approximately 50 microamps.



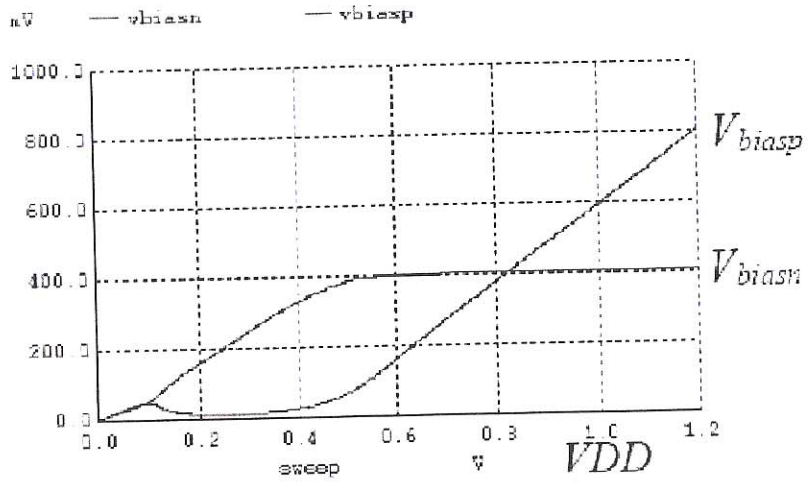


Figure 26.4 Simulating how the reference current changes with VDD.