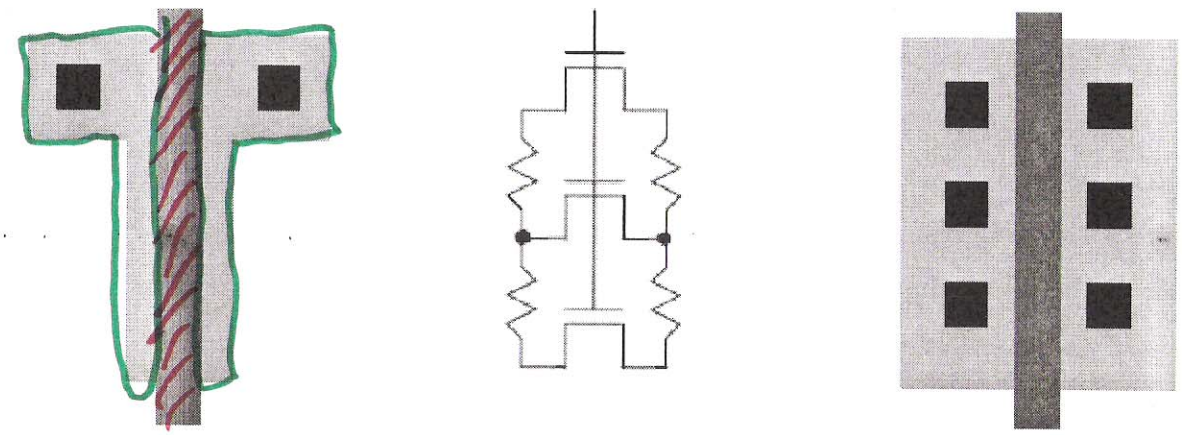


(a) (b) (c)

Figure 20.5 (a) Large device with a single contact and (b) its equivalent circuit. (c) Adding more contacts to reduce parasitic resistance.

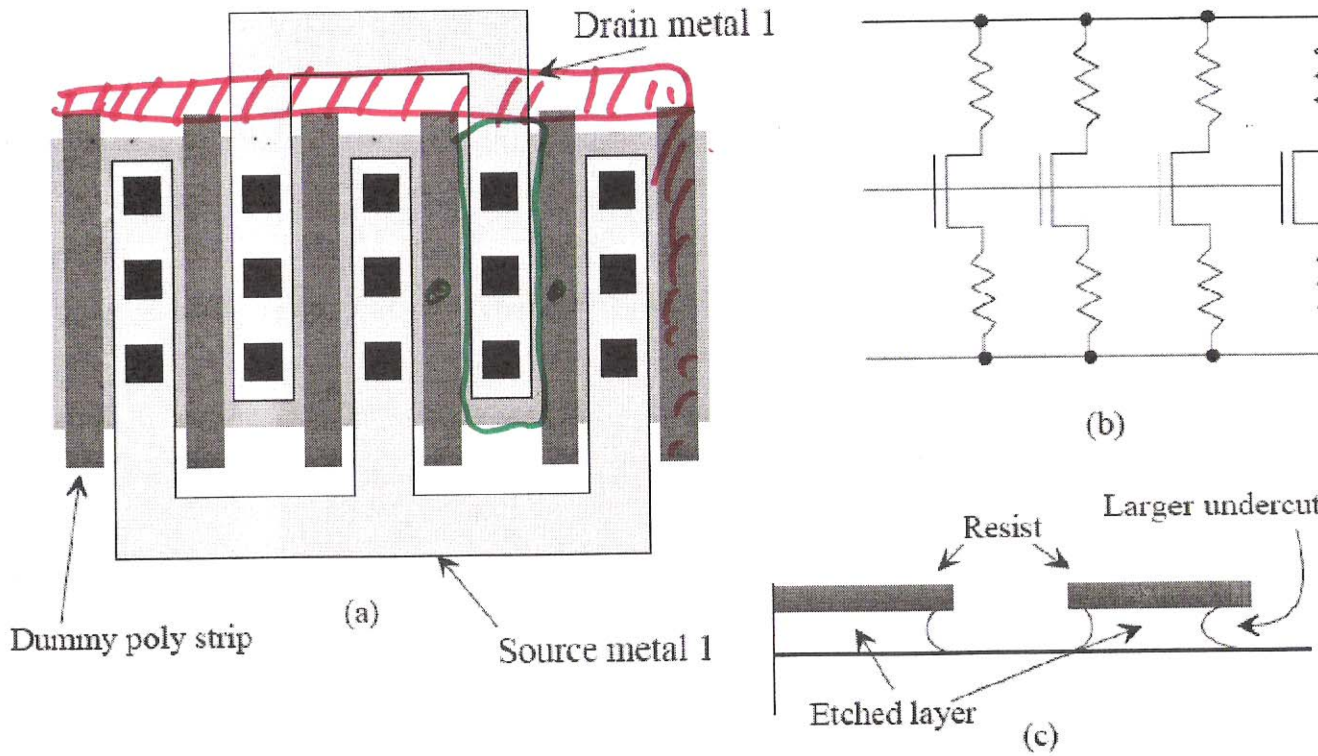


Figure 20.6 (a) A parallel device with dummy strips, (b) the equivalent circuit, and (c) undercutting.

2)

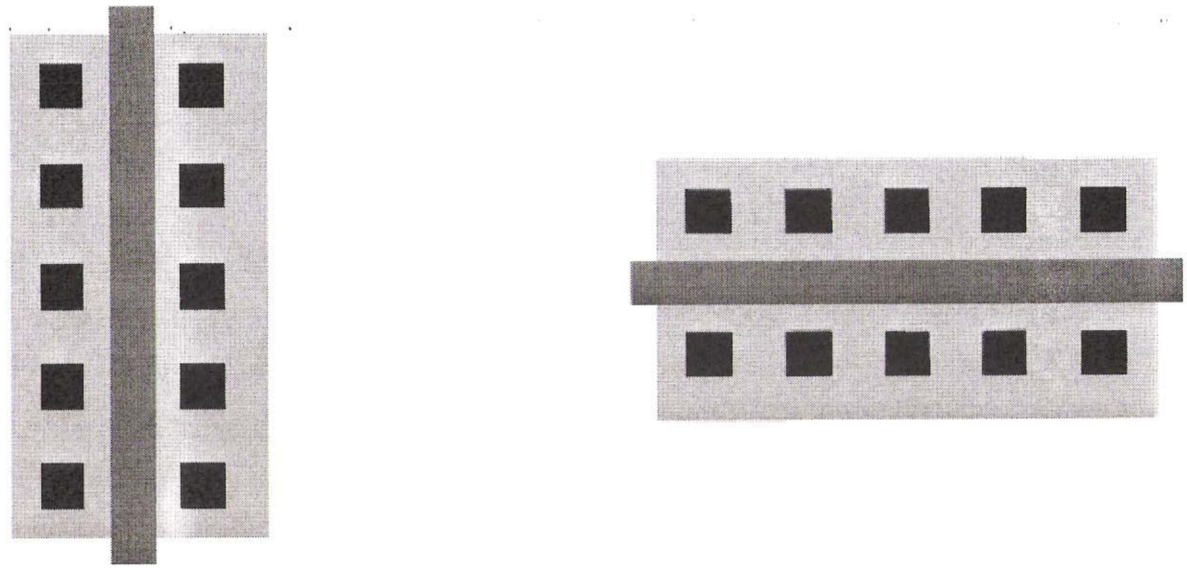
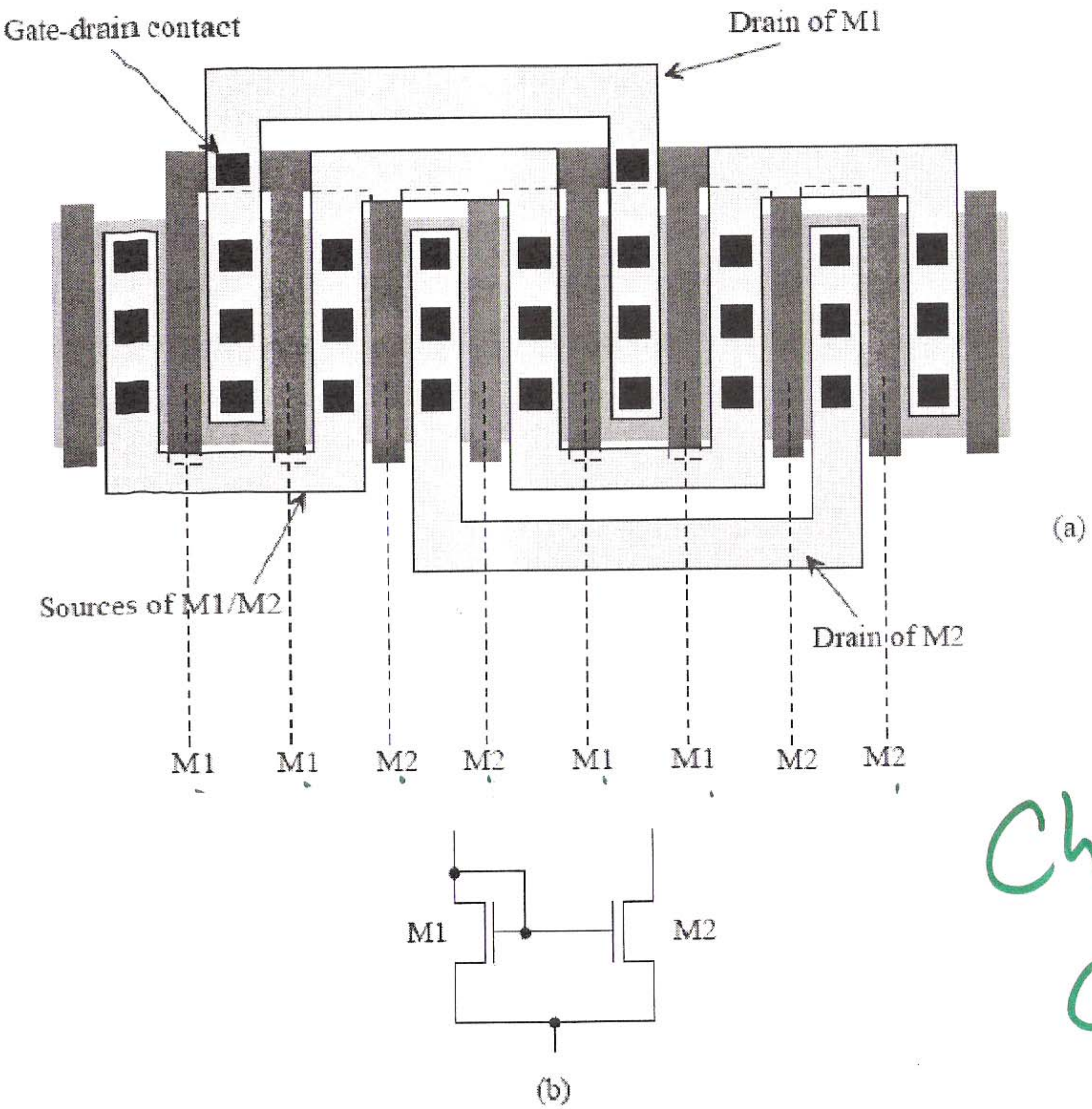


Figure 20.7 Devices with differing orientation (bad).

WANT, for good matching, devices to have same orientation.

you also WANT devices to be close



Ch. 5
Common-centroid
layout

Figure 20.8 (a) Layout of a simple current mirror using interdigitation and (b) equivalent circuit.

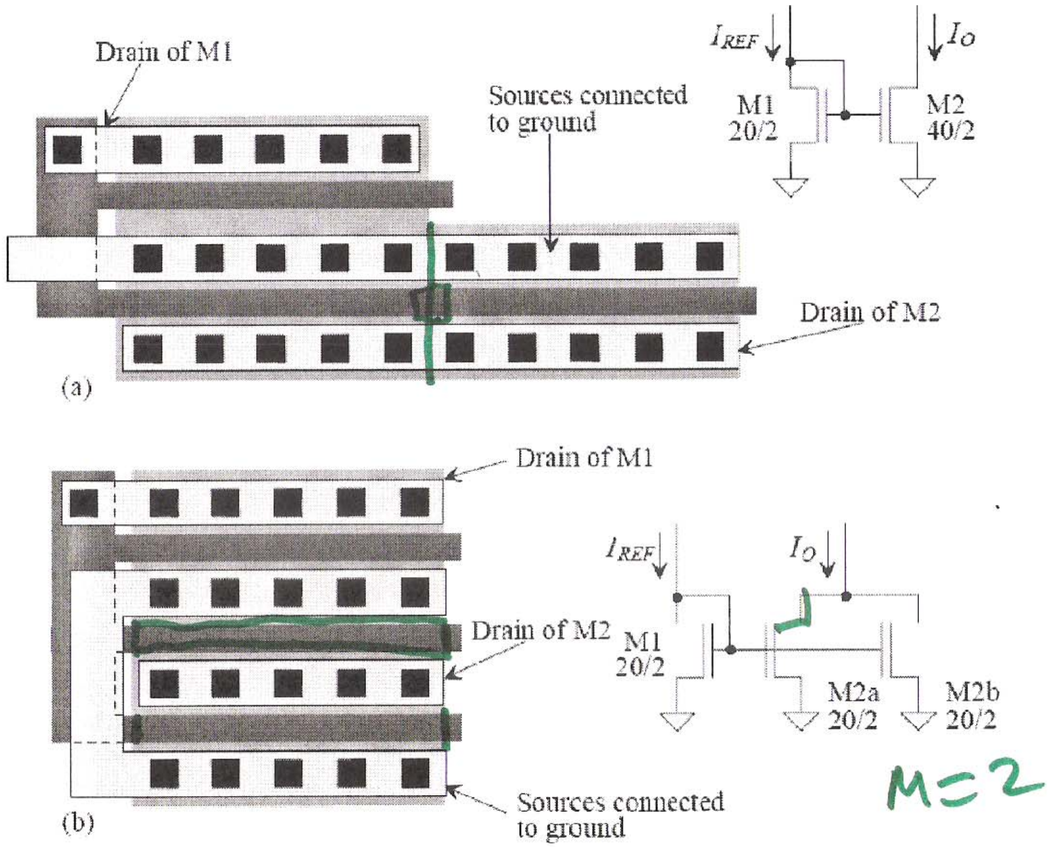
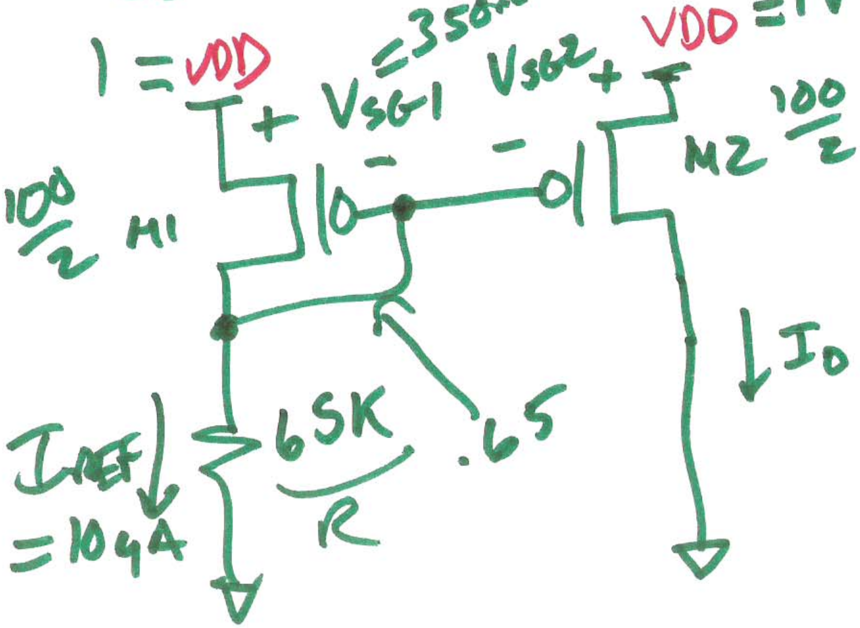


Figure 20.9 Layout of a current mirror (a) without width correction and (b) with width correction.

5)

Figures from CMOS Circuit Design, Layout, and Simulation, Copyright Wiley-IEEE, CMOSedu.com

Sec. 20.1.3



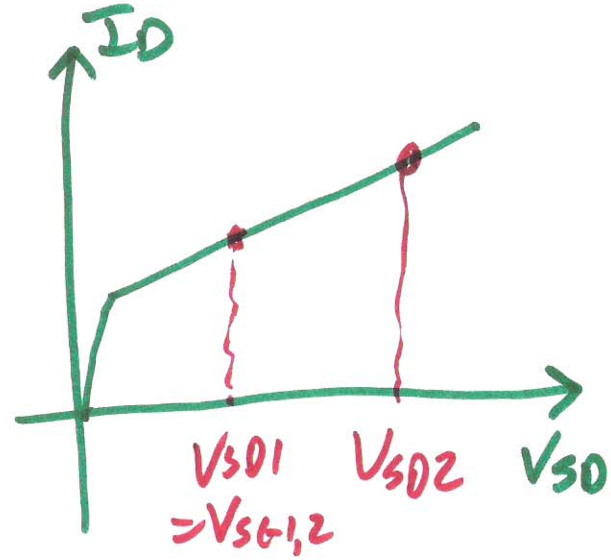
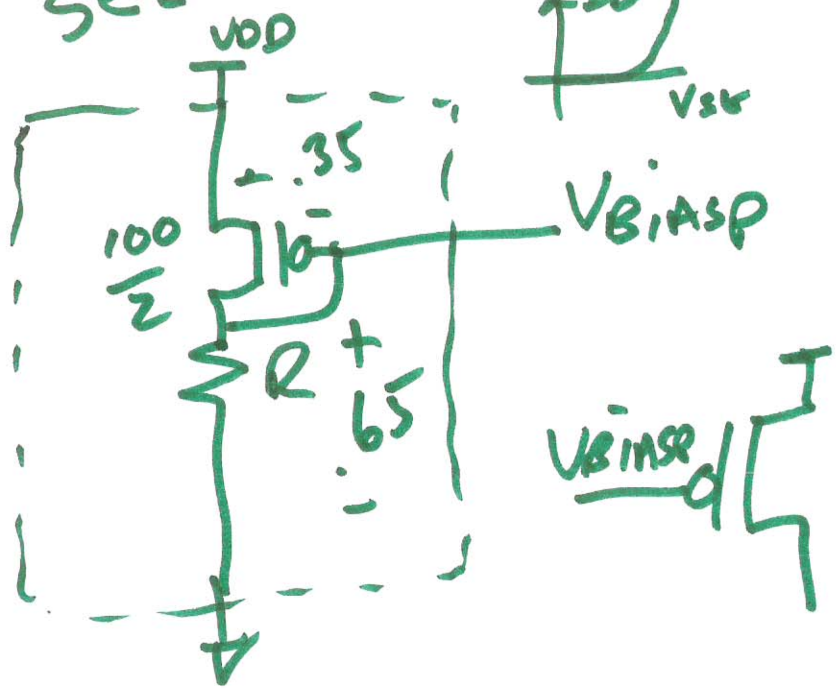


TABLE 9.2
scale = 50n
5μ/100nm

$$\frac{1 - .35}{65K} = 10\mu A$$

see Ex. 20.2



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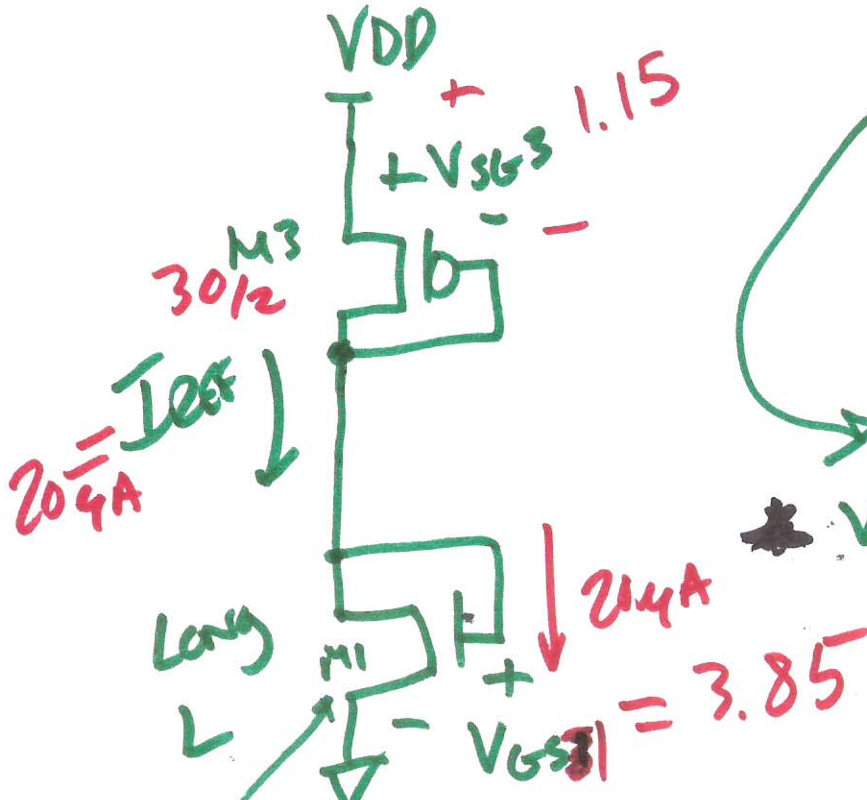
b)



think of as a resistor

$V_{GS1} > V_{SG3}$

$$VDD = V_{SG3} + V_{GS1}$$

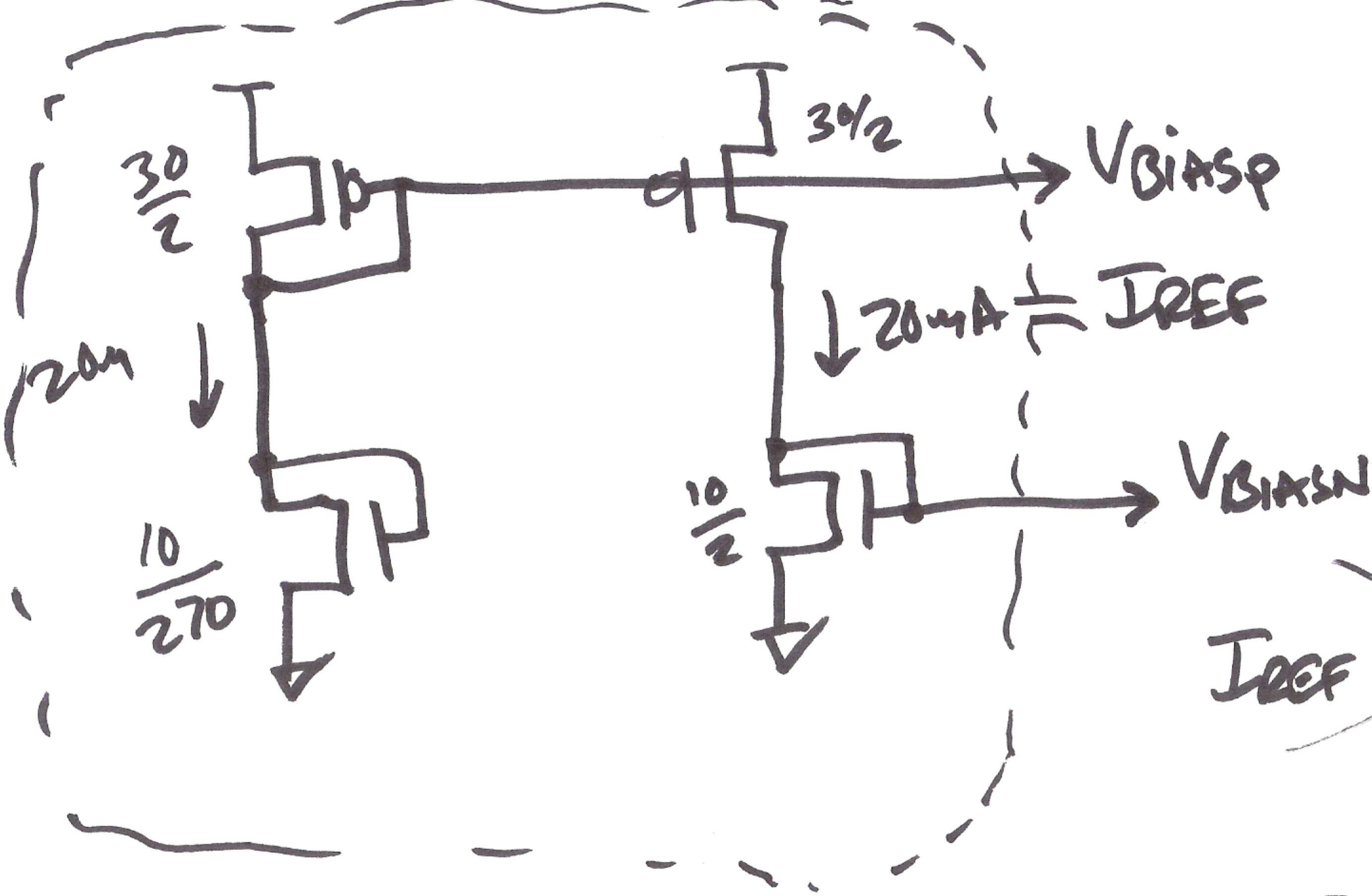
$$V_{GS} = \sqrt{\frac{2 I_D}{KP_N \cdot \frac{W}{L}}} + V_{THN}$$

$$VDD = \underbrace{\sqrt{\frac{2 I_{REF}}{KP_N \cdot \frac{W_1}{L_1}}} + V_{THN}}_{3.85} + \underbrace{\sqrt{\frac{2 I_{REF}}{KP_P \cdot \frac{W_3}{L_3}}} + V_{THP}}_{1.15}$$

$V_{THN} \rightarrow .8$, $\frac{W_3}{L_3} \rightarrow 30/2$

$$\sqrt{\frac{2 \cdot 20\mu}{120\mu \cdot \frac{W_1}{L_1}}} + .8 = 3.85$$

$$\frac{W_1}{L_1} \approx \frac{10}{270}$$

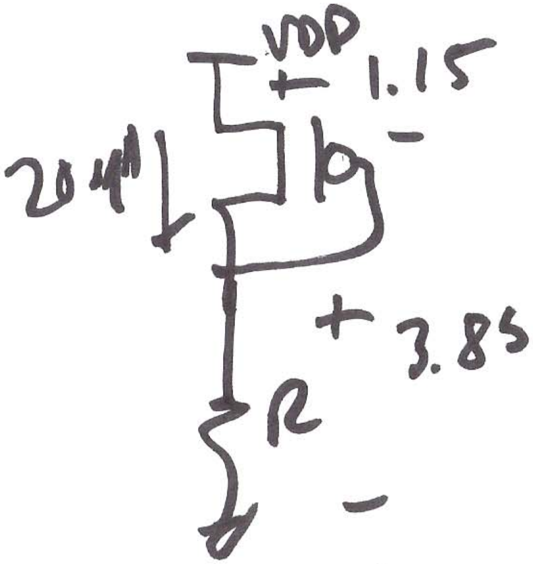


~~$I_{REF} = \frac{\beta_P}{2}(VDD - I_{REF}\cdot$~~

How sensitive is IREF to changes in VDD?

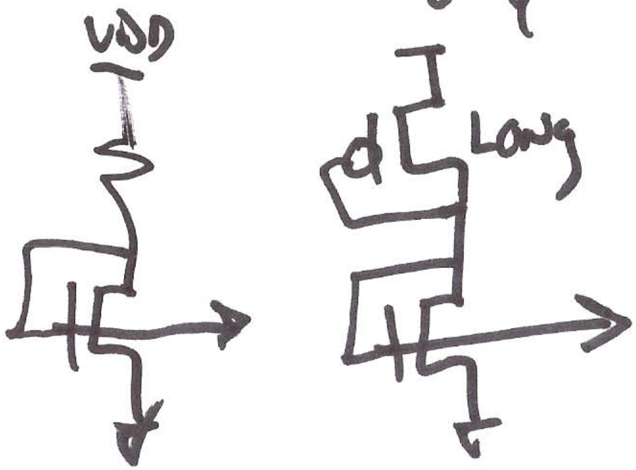
$$\frac{\delta I_{REF}}{\delta VDD} = \frac{\delta \;*}{VDD} = \frac{2VDD}{K} - \frac{2(V_{THN} + |V_{THP}|)}{K}$$

$$\frac{\delta I_{REF}}{\delta VDD} = \frac{12nA}{mV}$$



Long channel

$$R = \frac{3.85}{20\mu} \approx 192K$$



$$I_{REF} = \frac{VDD - V_{SG}}{R}$$

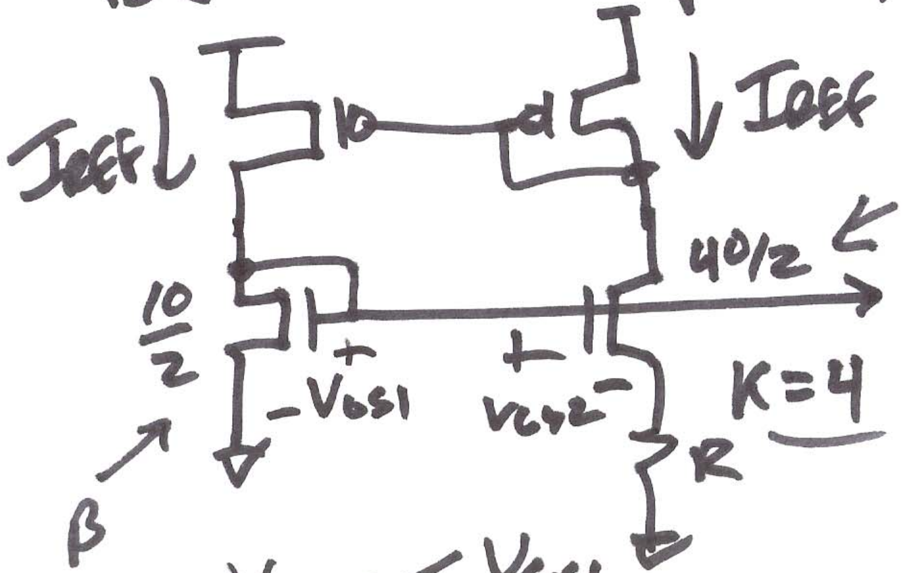
$$I_{REF} \approx \frac{VDD}{R}$$

$$\frac{\delta I_{REF}}{\delta VDD} = \frac{1}{R}$$

5 nA/mV

Beta-Multiplier, self-biased reference

Start-up CKT Not shown



$K \cdot \beta = 4 \cdot \beta$

BMR

$V_{GS2} < V_{GS1}$

$$V_{GS1} = V_{GS2} + I_{REF} \cdot R$$

$$V_{GS} = \sqrt{\frac{2I_D}{\beta}} + V_{THN}$$

$$\sqrt{\frac{2I_{REF}}{\beta}} + \cancel{V_{THN}} = \sqrt{\frac{2I_{REF}}{K \cdot \beta}} + \cancel{V_{THN}} + I_{REF} \cdot R$$

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$$I_{REF} \cdot R = \sqrt{\frac{I_{REF} \cdot 2}{\beta}} \left(1 - \frac{1}{\sqrt{K}}\right)$$

$$I_{REF} \cdot R^2 = \frac{2}{KP \cdot \frac{W_1}{L_1}} \cdot \left(1 - \frac{1}{\sqrt{K}}\right)^2$$

$$\boxed{I_{REF} = \frac{2}{KP \cdot \frac{W_1}{L_1} \cdot R^2} \left(1 - \frac{1}{\sqrt{K}}\right)^2}$$

independent of VDD!

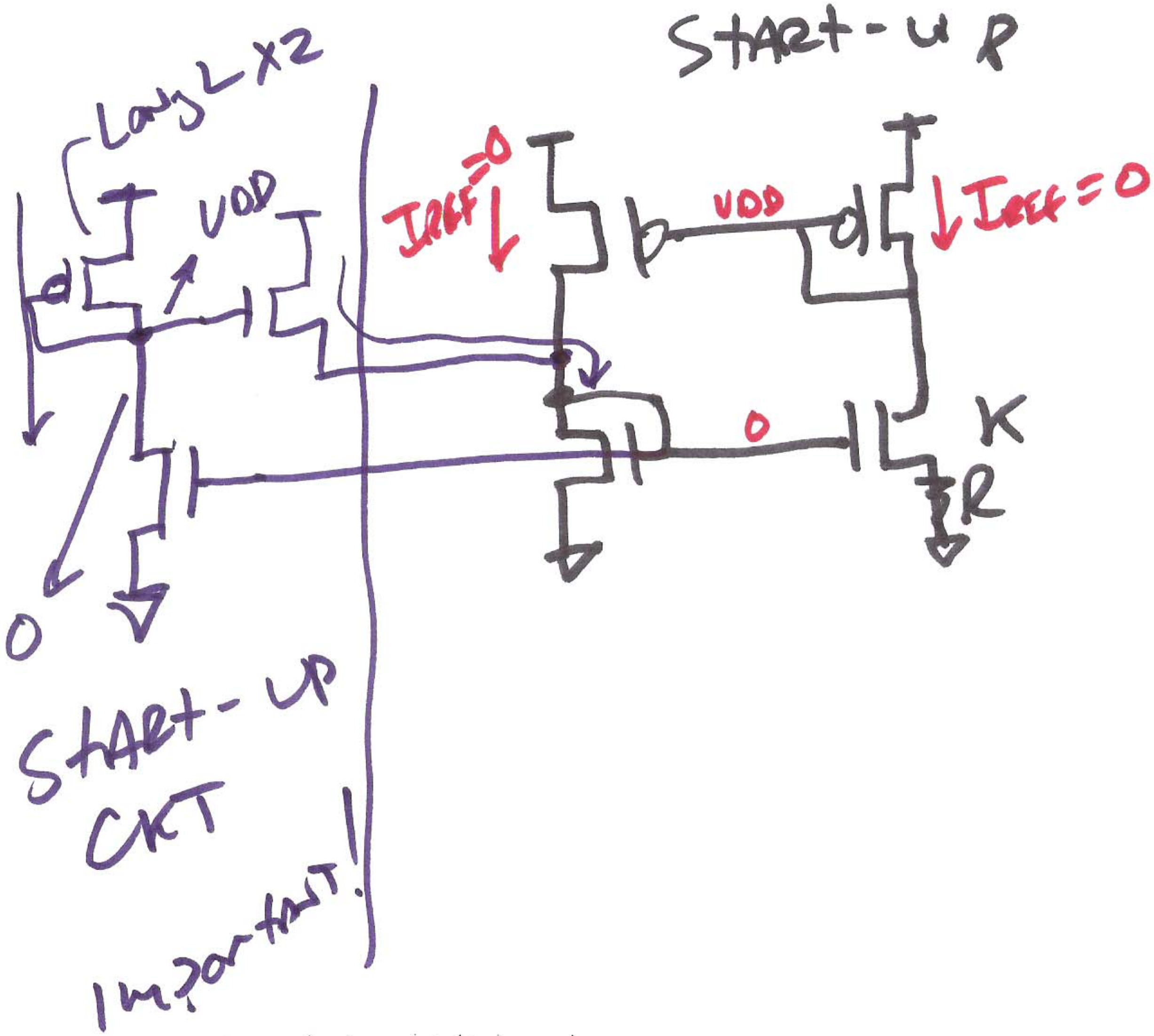
if $K = 4$

$$I_{REF} = \frac{1}{2KP \cdot \frac{W_1}{L_1} \cdot R^2}$$

$$g_m = \sqrt{2 \cdot KP \cdot \frac{W}{L} \cdot I_{REF}} = \frac{1}{R} \quad (k = 4)$$

.8pA/mV

CMOSedu.com use BMR



START-UP
Long L x2
VDD
0
START-UP CKT
important!
IREF=0
VDD
IREF=0
0
K
R

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