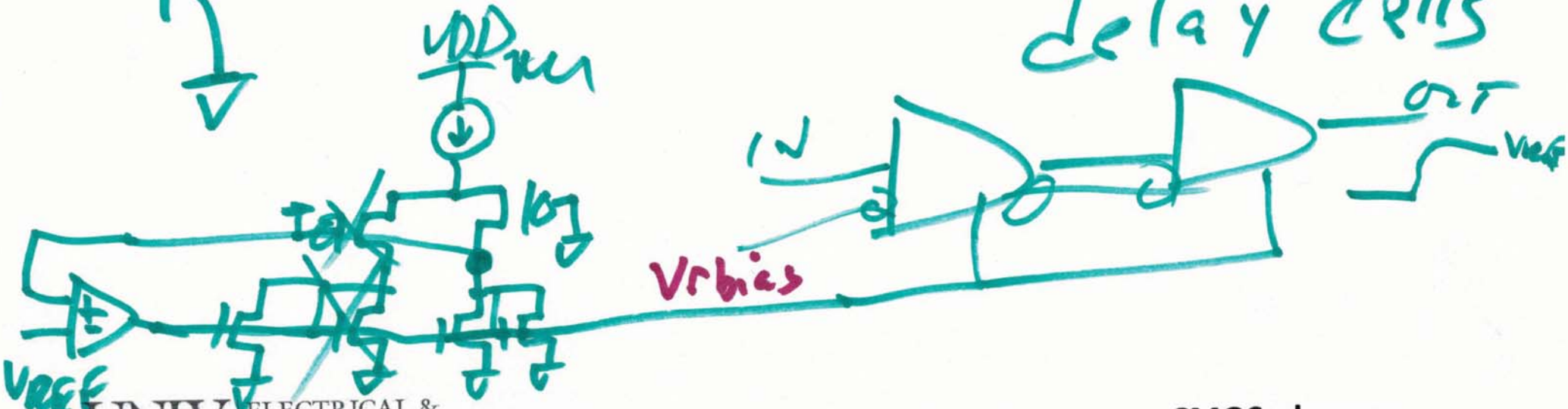
Lecture 21

November 9, 2015

ELG 721 MEMORY circuit design

Sec. 19.6

delay cells



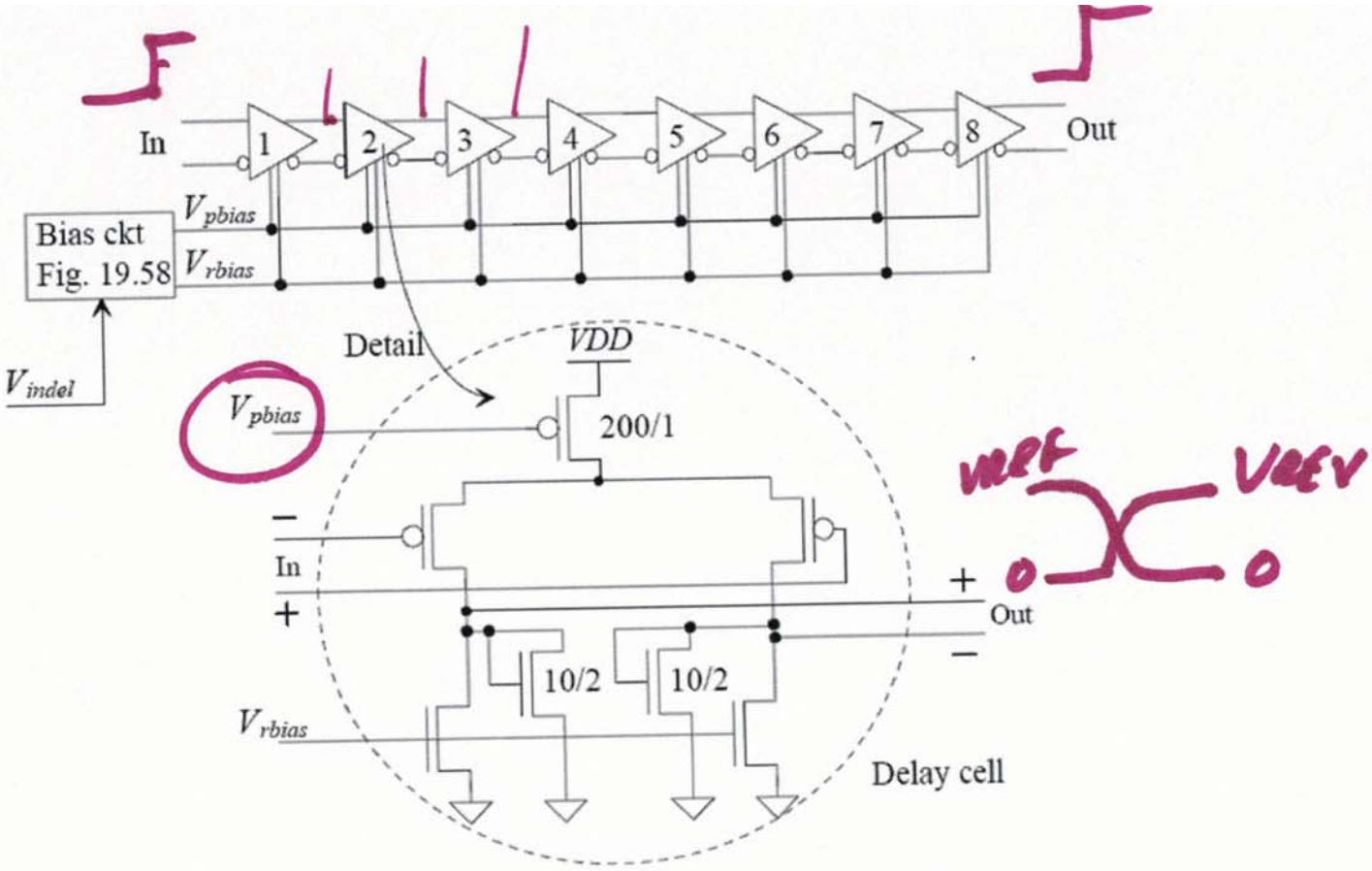
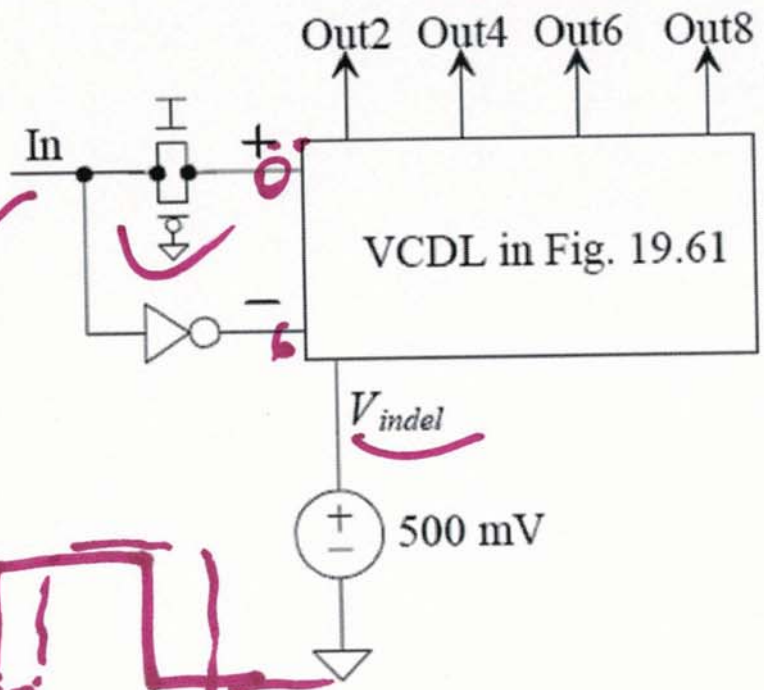


Figure 19.61 An eight-stage VCDL.

2)



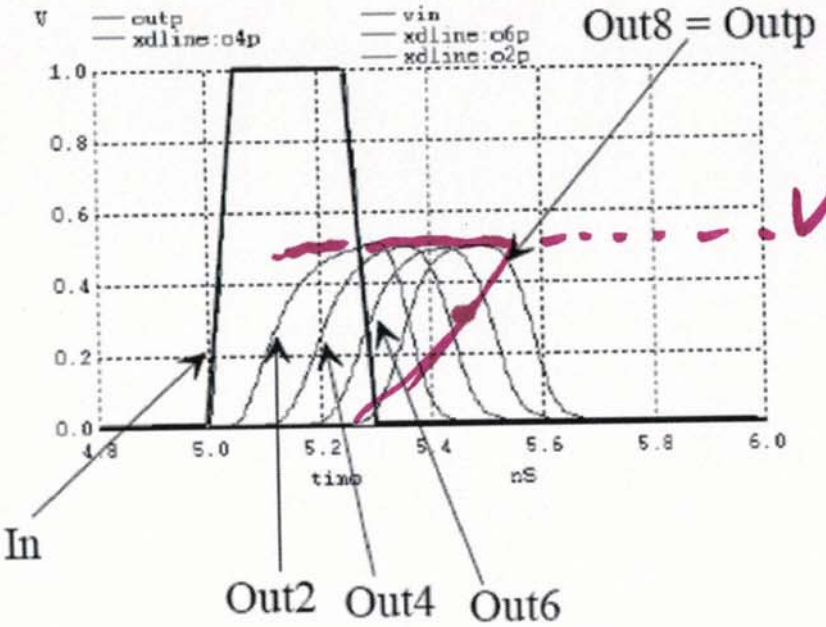


Figure 19.62 Simulating the VCDL in Fig. 19.61.

3)

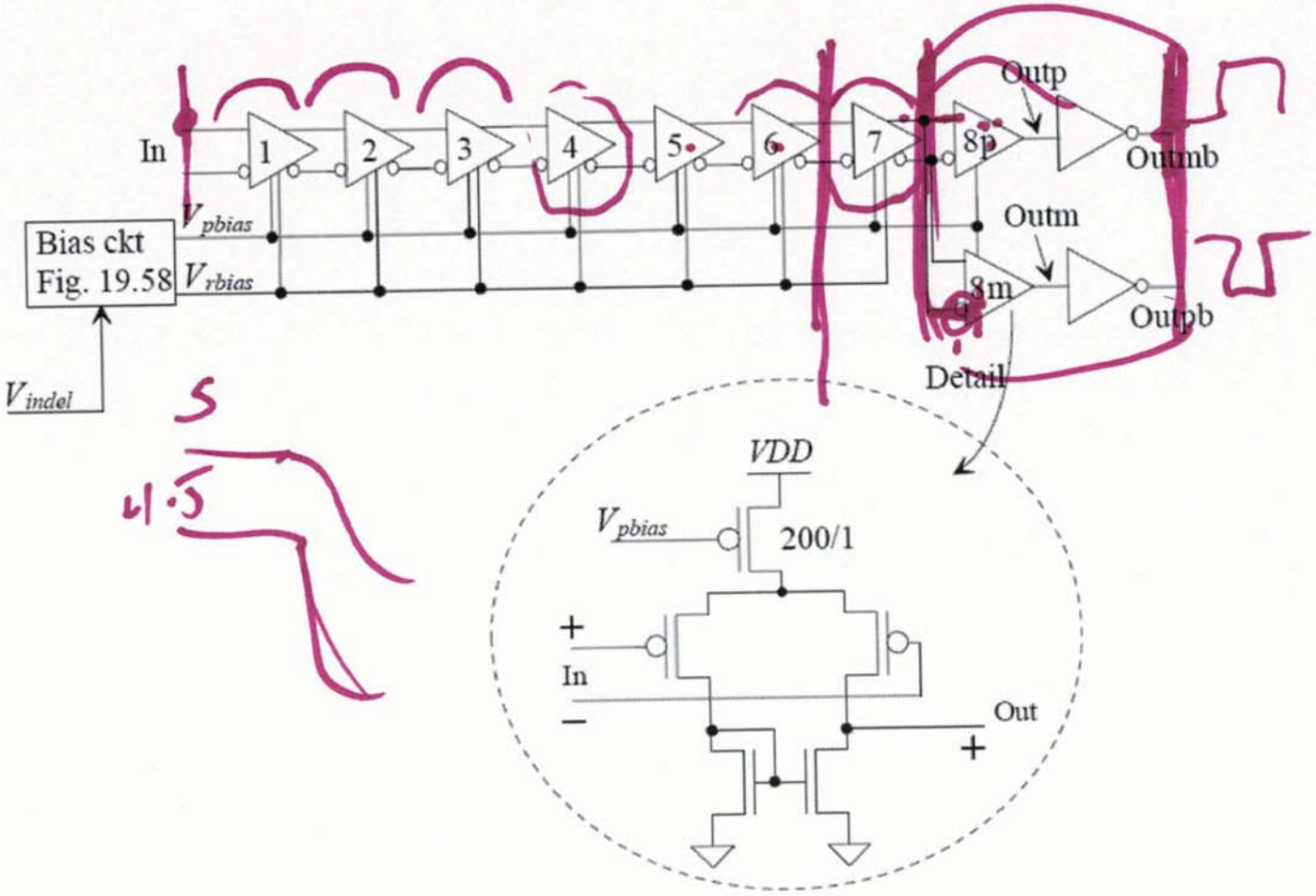


Figure 19.63 Modifying the VCDL to generate full output logic levels.

4)

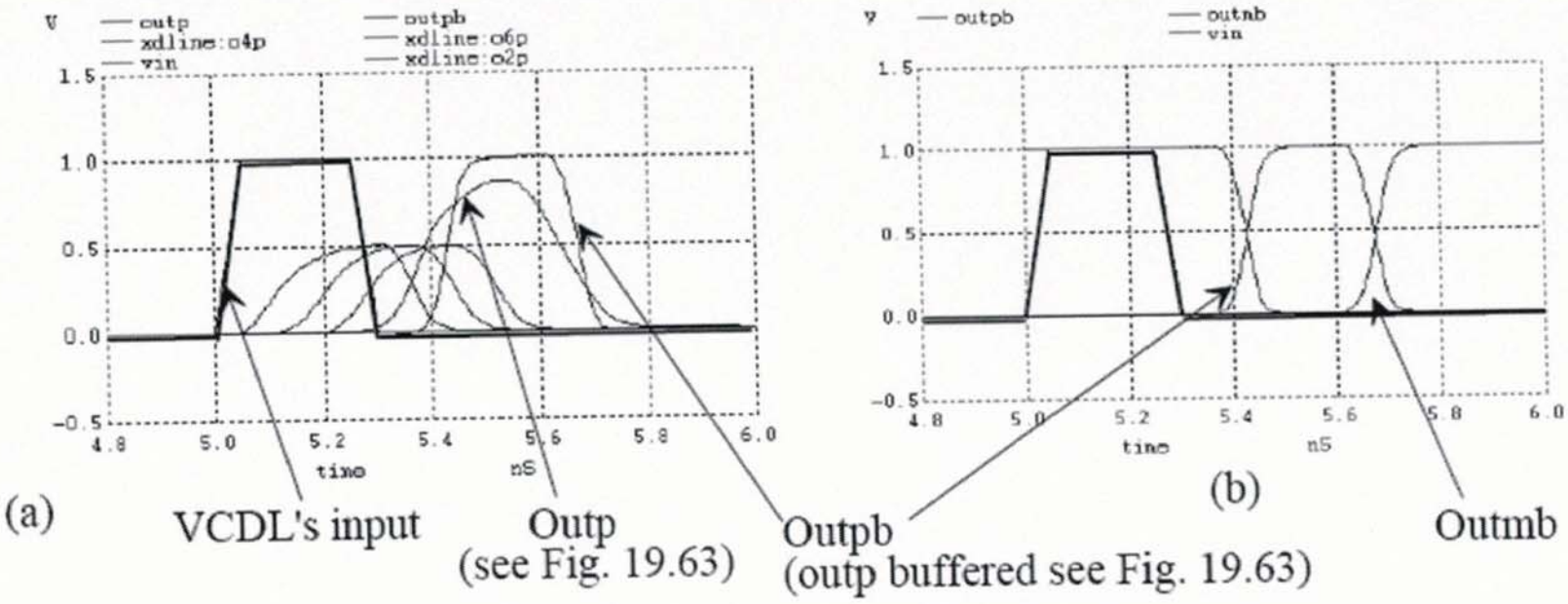


Figure 19.64 The operation of the VCDL in Fig. 19.63.

6)

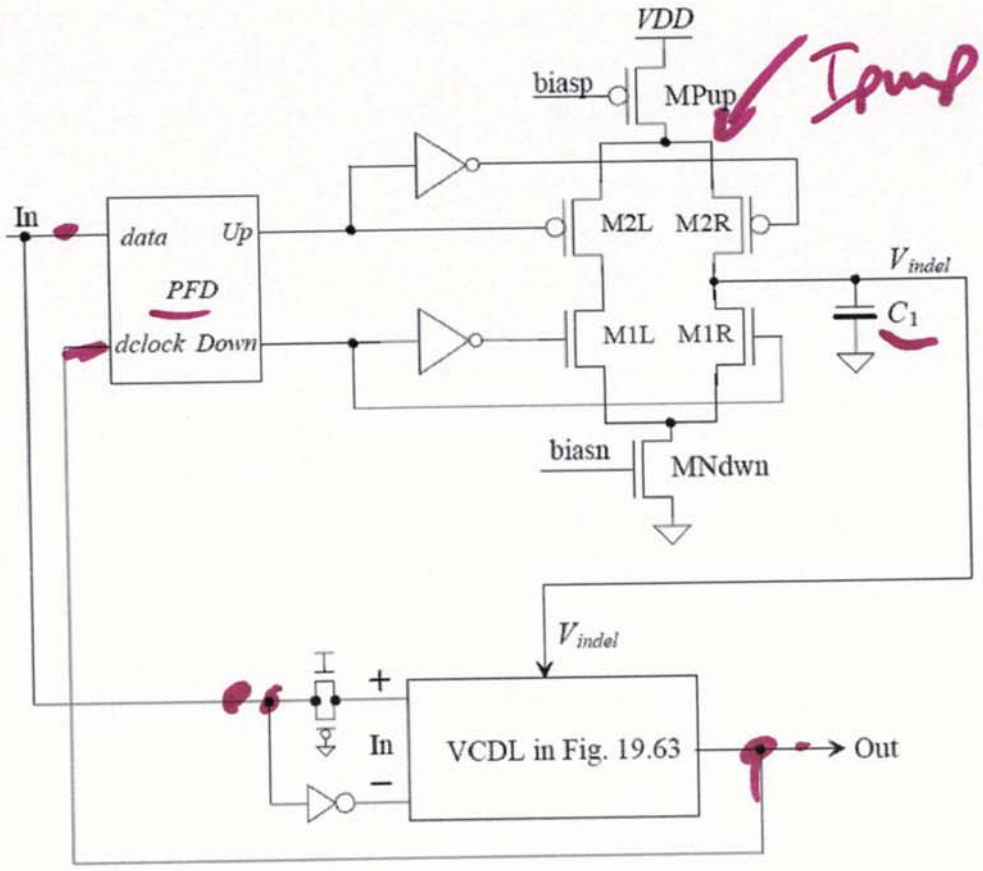


Figure 19.65 Block diagram of a DLL.

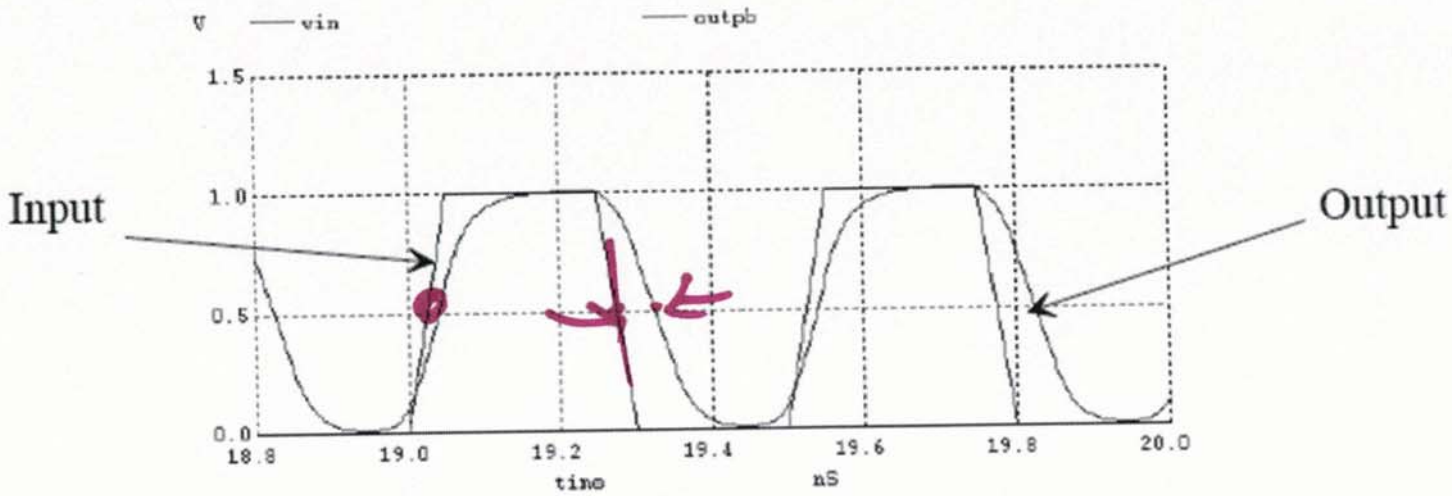


Figure 19.66 Input and output of the DLL in Fig. 19.65.

7)

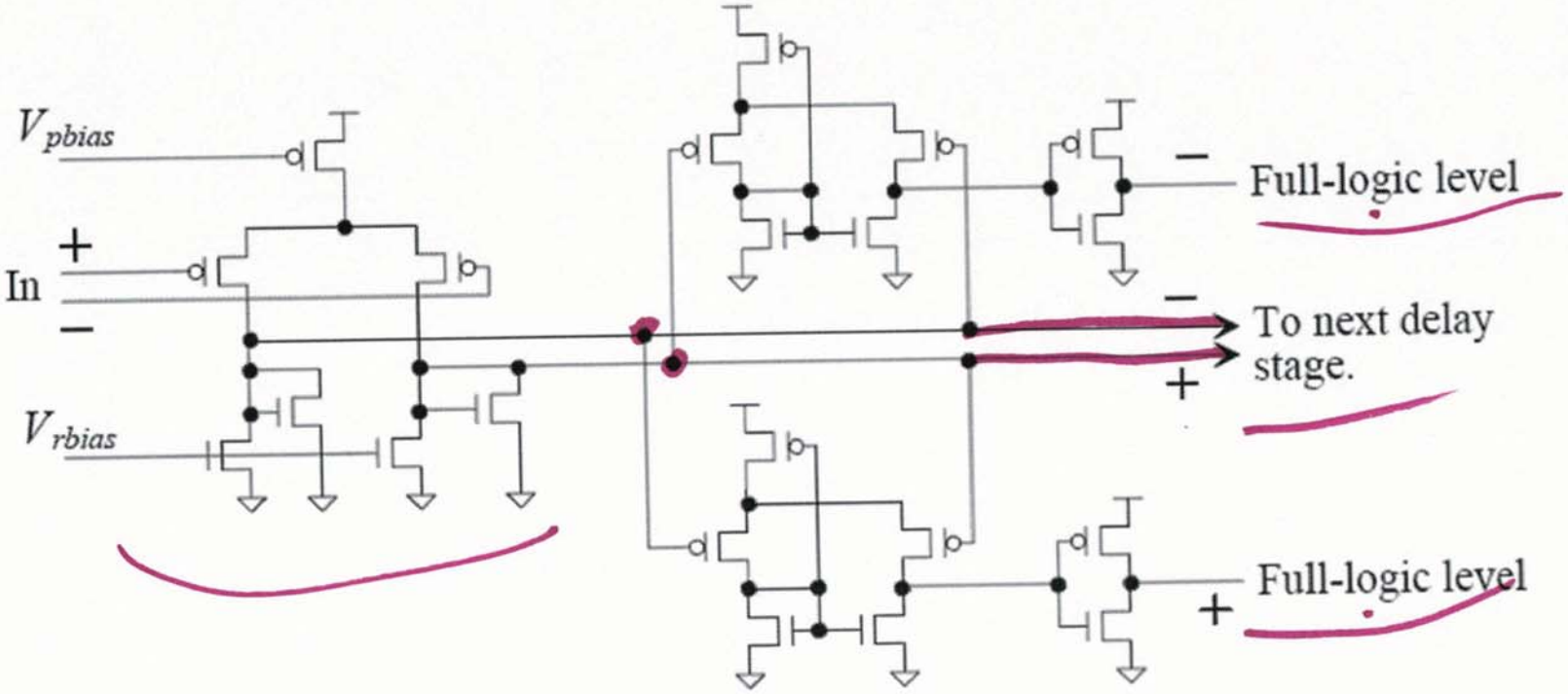


Figure 19.67 Generating full-logic levels in each delay stage.

8)

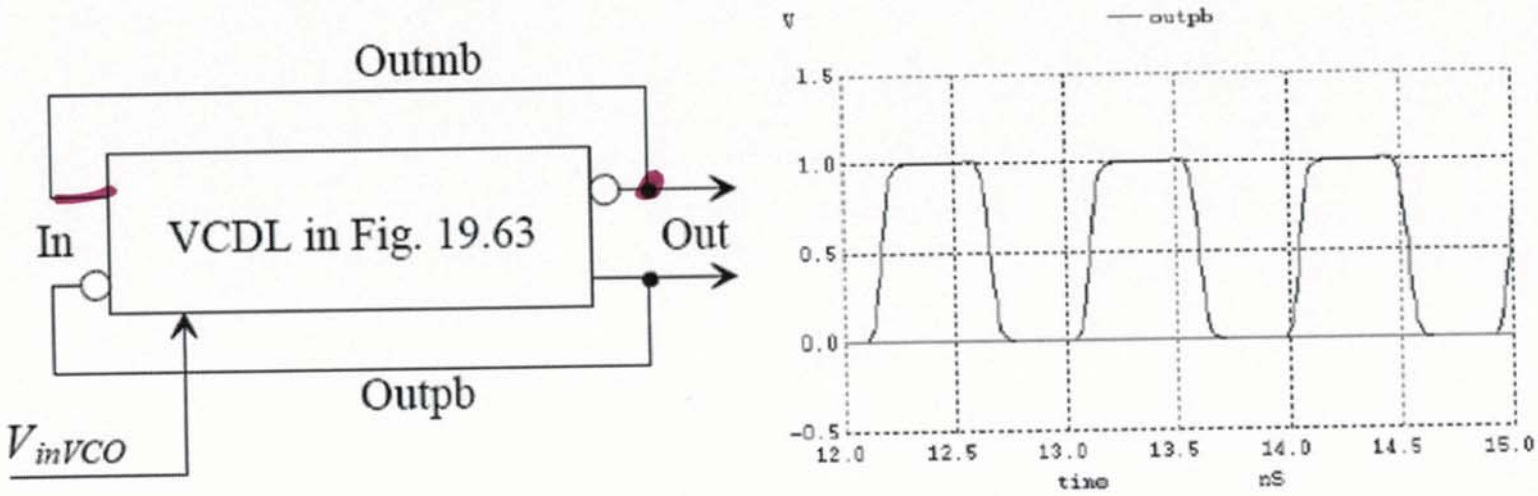


Figure 19.68 Making a VCO with the delay line in Fig. 19.63 and its output when Vinvco = 350 mV.

~~2GHz~~ PLL

16bit/s

9)

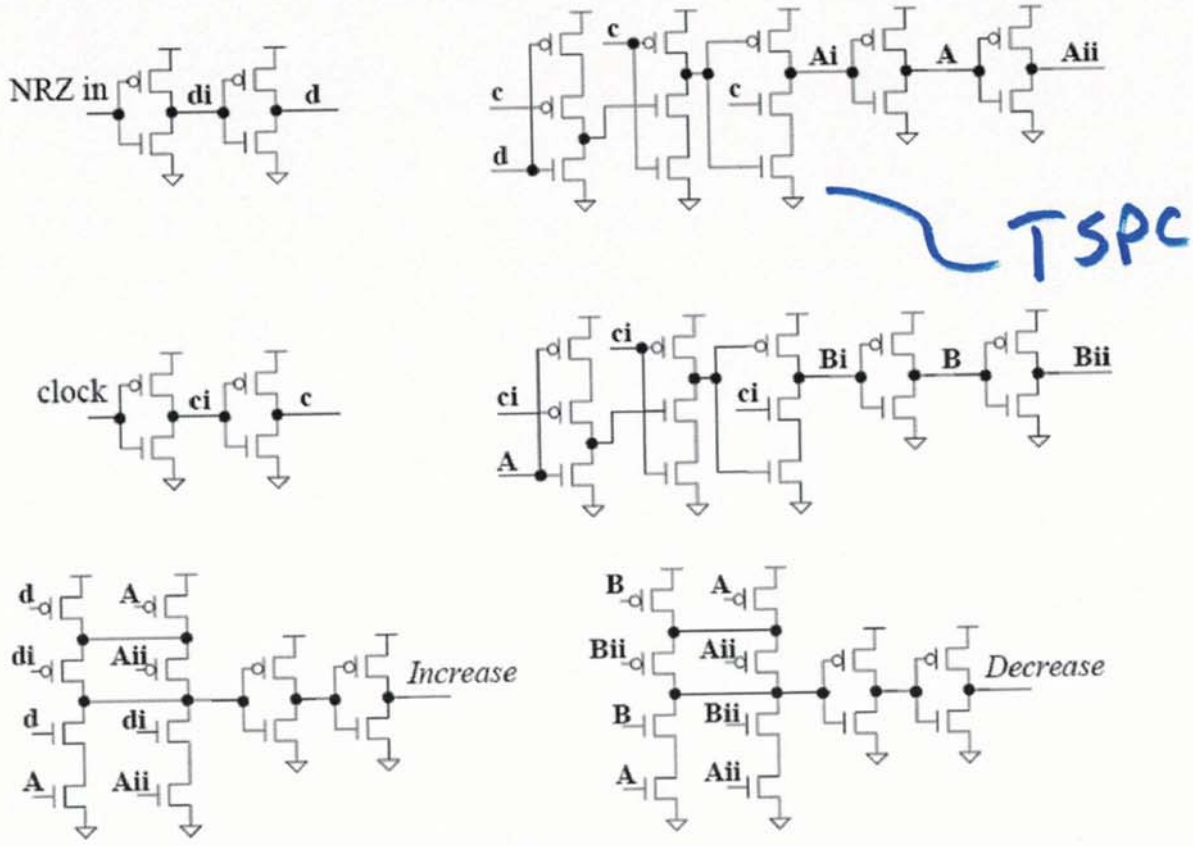


Figure 19.69 CMOS implementation of the Hogge PD.

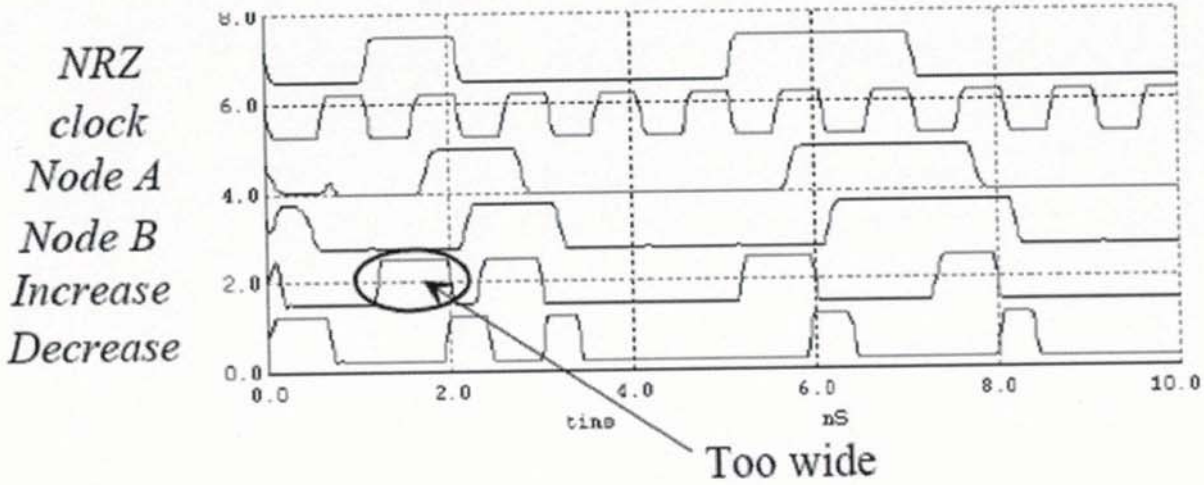


Figure 19.70 Simulating the Hogge PD in Fig. 19.69. These results should be compared to Fig. 19.49. Notice how the increased pulse widths are too wide. The result is that the Vinvco control voltage will increase above the desired value (and cause a static phase error or false locking).

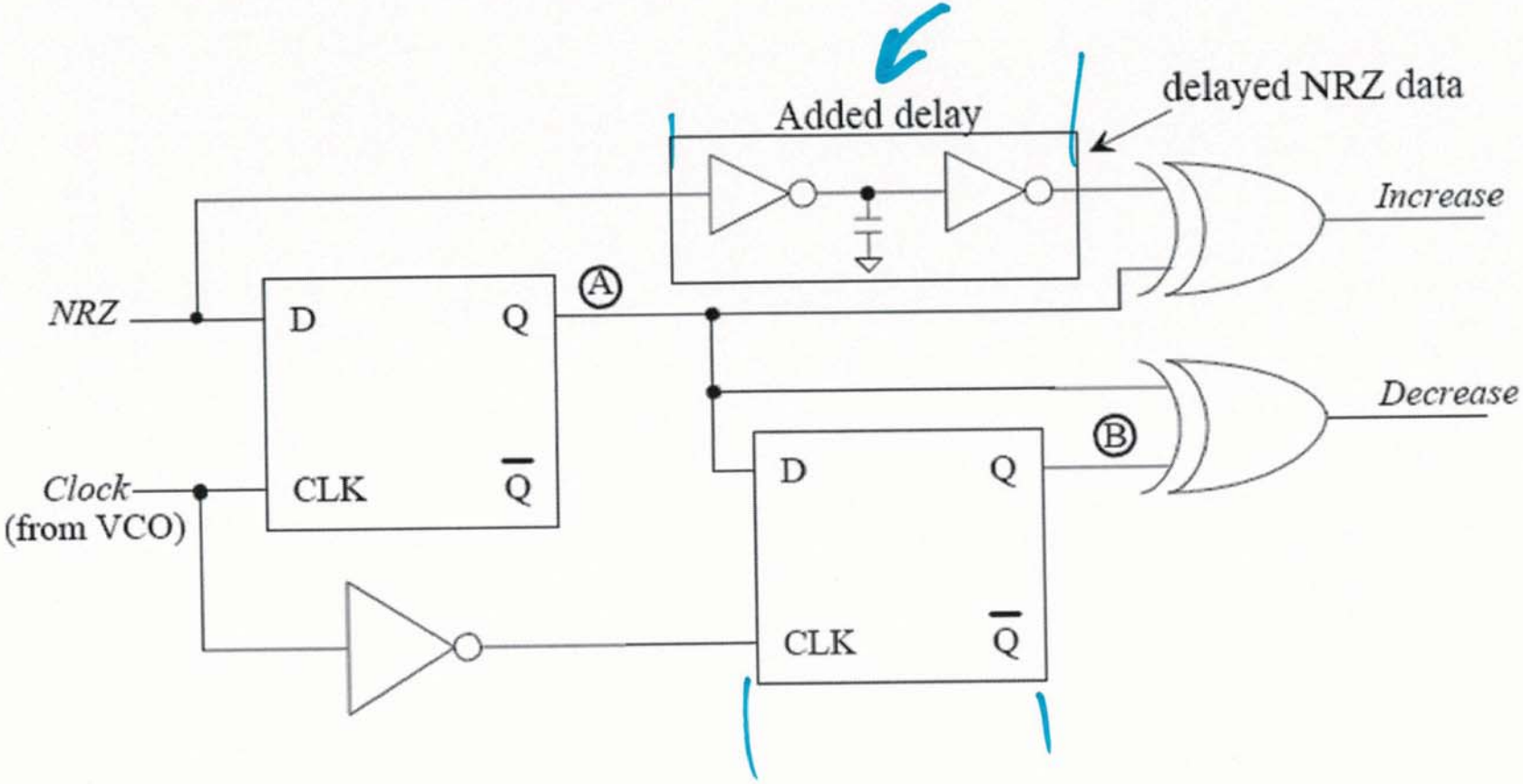


Figure 19.71 Adding a delay to the Hogge PD to compensate for the delay the NRZ data sees to node A.

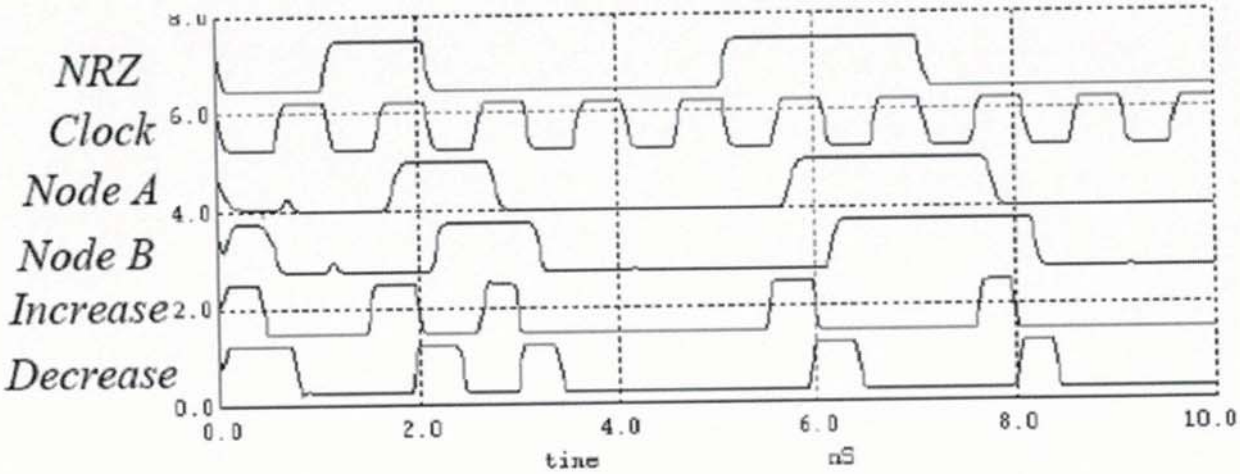


Figure 19.72 Resimulating the operation of the Hogge PD with the delay seen in Fig. 19.71 included.

Better!

13)

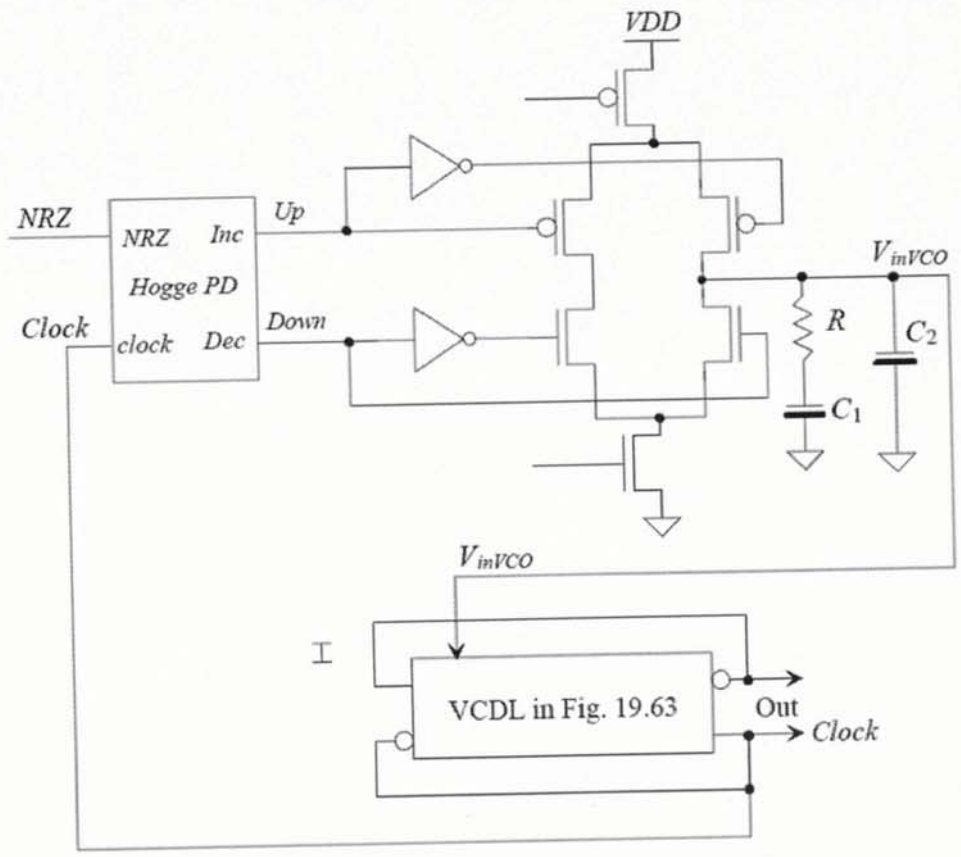


Figure 19.73 Block diagram of the DPLL used for clock-recovery discussed in this section.

14)

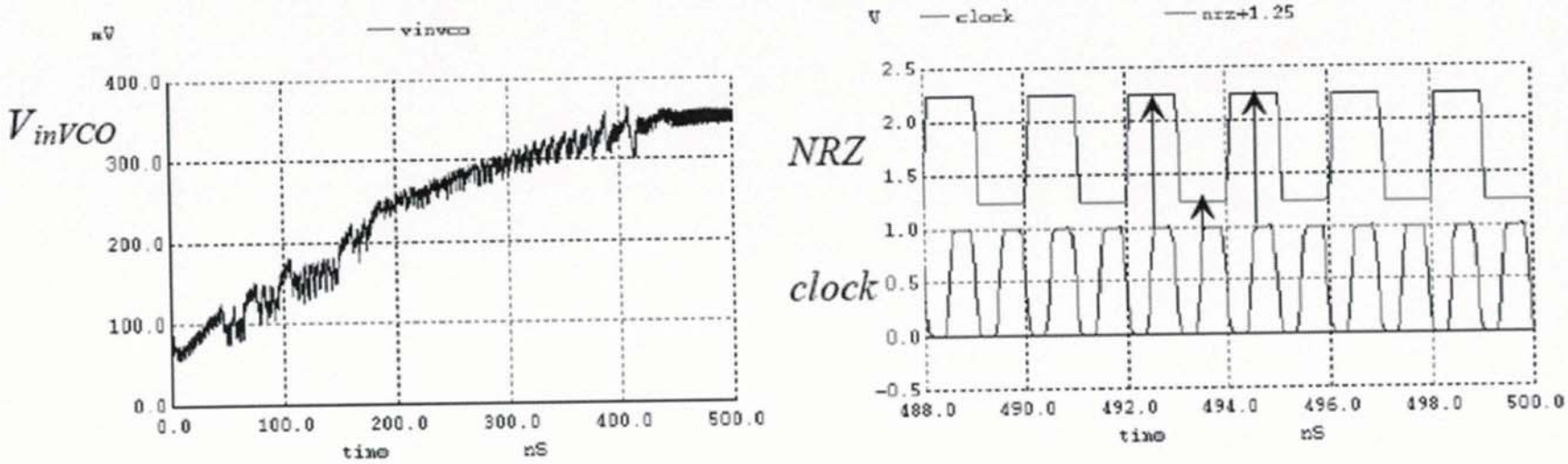


Figure 19.74 Simulating the PLL in Fig. 19.73 when the input NRZ data is an alternating string of ones and zeroes.

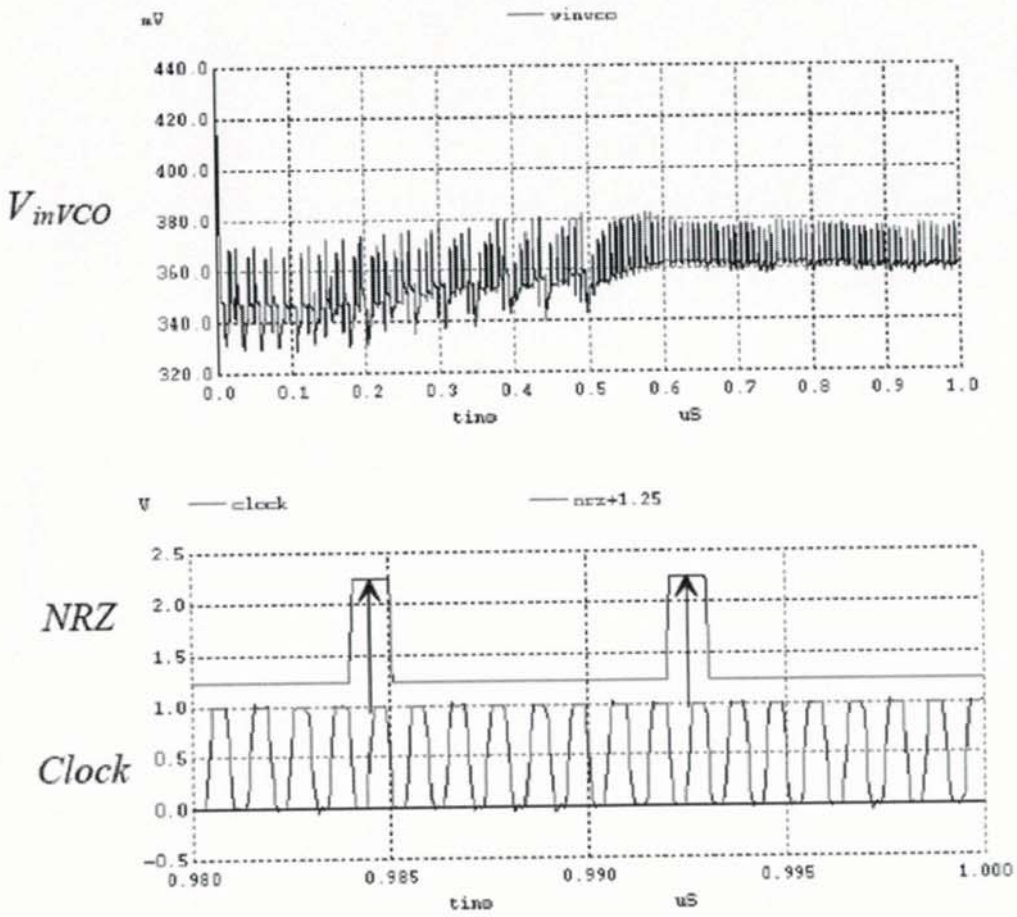


Figure 19.75 Simulating the PLL in Fig. 19.73 when the input data is a string of seven zeroes followed by a single one.