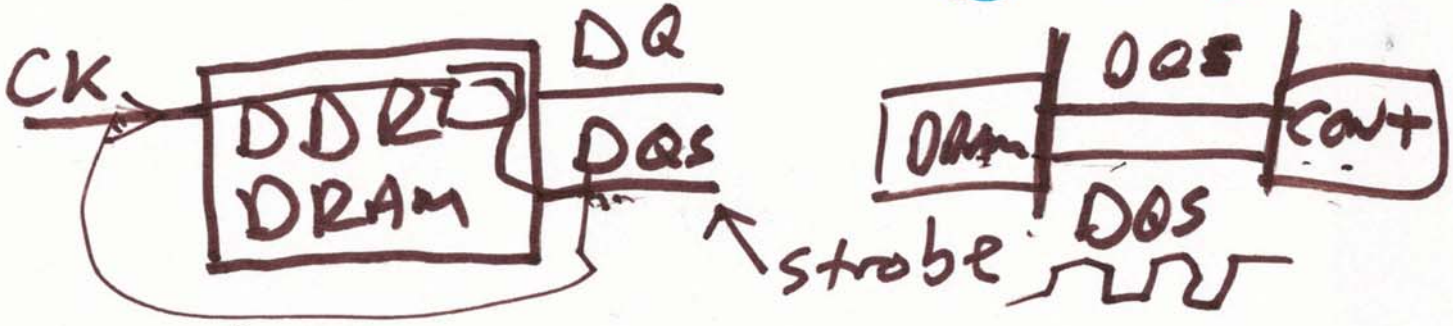
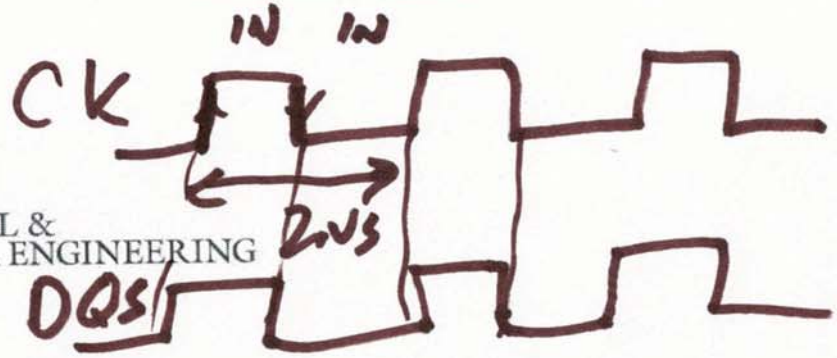
Lecture 20
NOV. 4, 2015

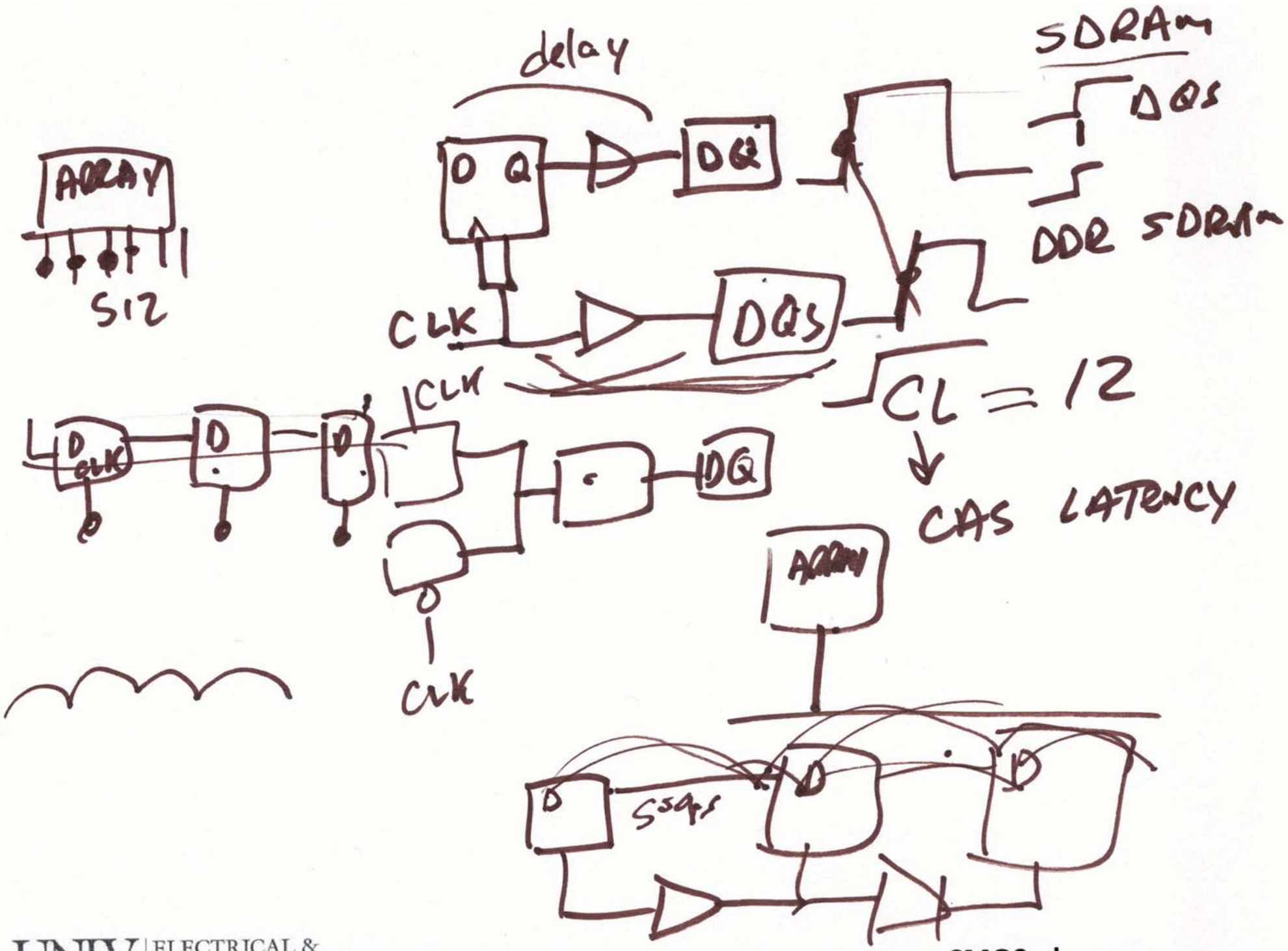
Delay-Locked loops (DLLs)

ELG 721

Memory circuit Design






delay
SDRAm
DQS
ARRAY
D Q
DQ
DDR SDRAm
512
CLK
DQS
CLK
CL = 12
CAS LATENCY
DQ
CLK
ARRAY
5348

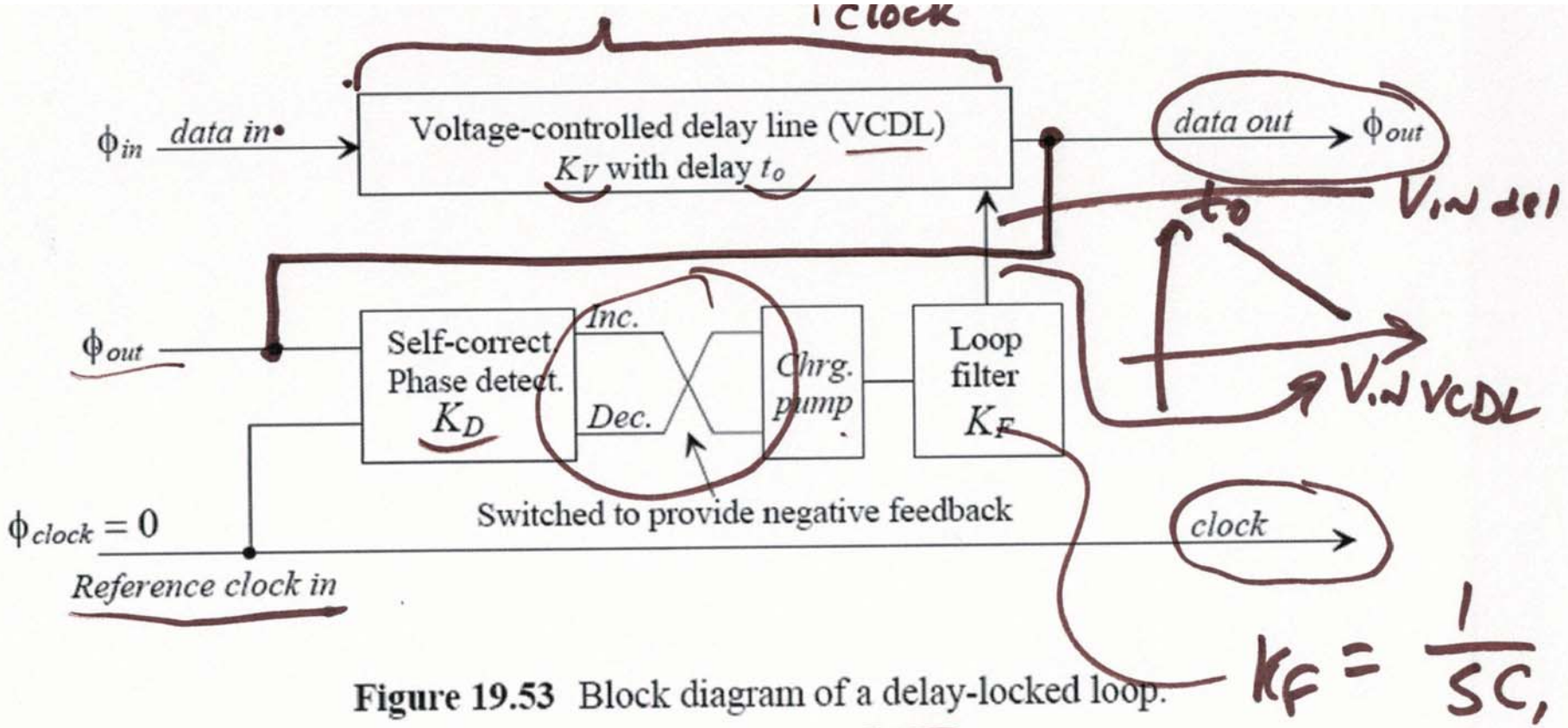


Figure 19.53 Block diagram of a delay-locked loop.

$K_F = \frac{1}{sC}$,

$\phi_{OUT} = \phi_{IN} + \frac{2\pi}{T_{CLOCK}}$

for a locked loop $t_o = T_{CLOCK}$

$t_o = K_V \cdot V_{in\,del}$

$V_{in\,del} = \phi_{OUT} \cdot K_F \cdot K_D$, $\frac{\phi_{OUT}}{\phi_{IN}} = \frac{1}{1 + K_D K_V K_F \cdot W_{CLK}}$

3)

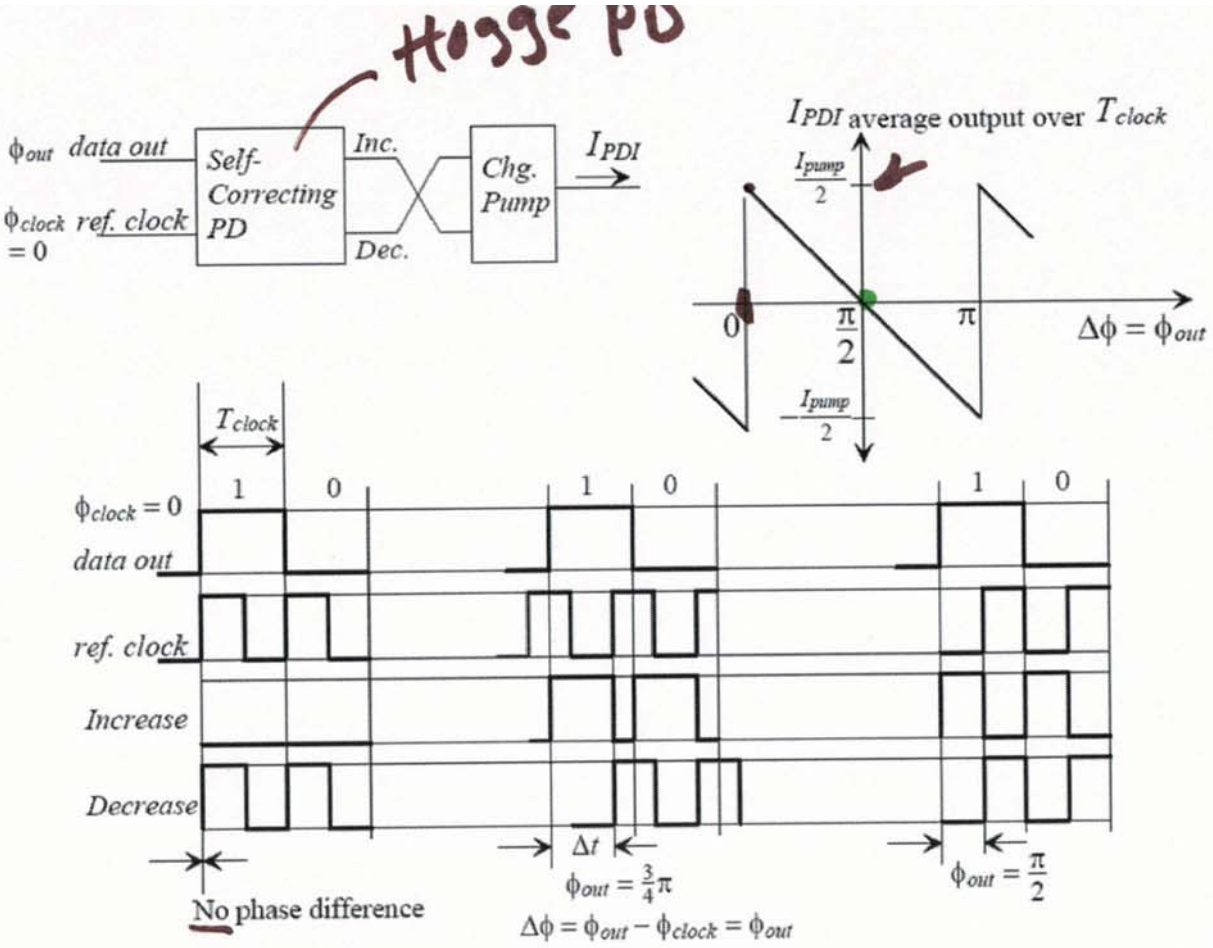


Figure 19.54 Self-correcting PD output for various inputs (assuming input data is a string of alternating ones and zeros).

4)

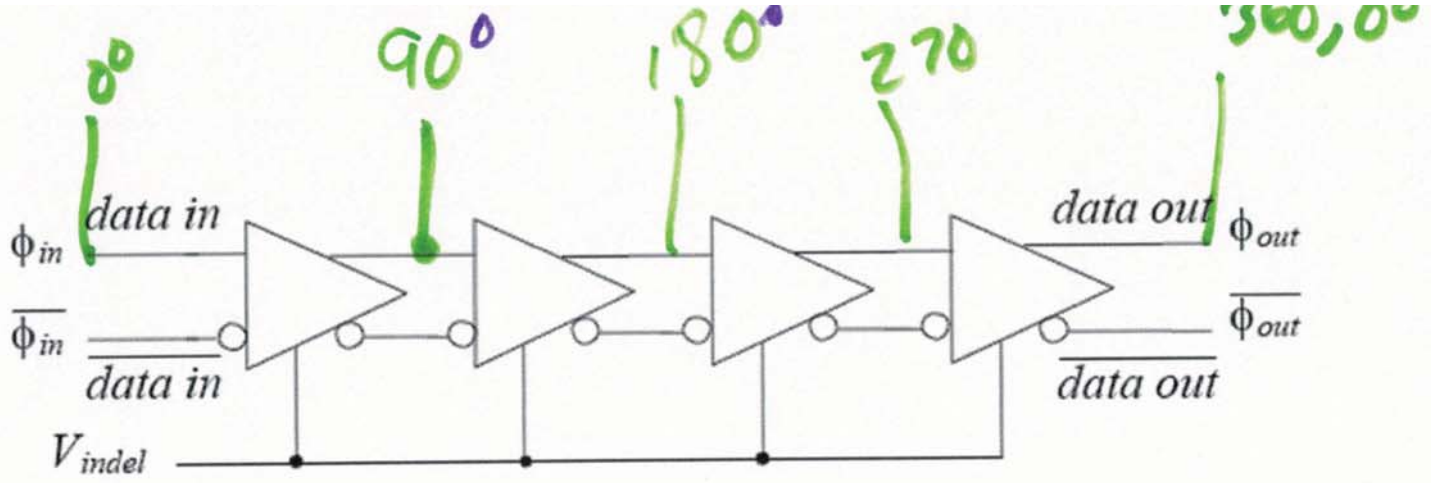
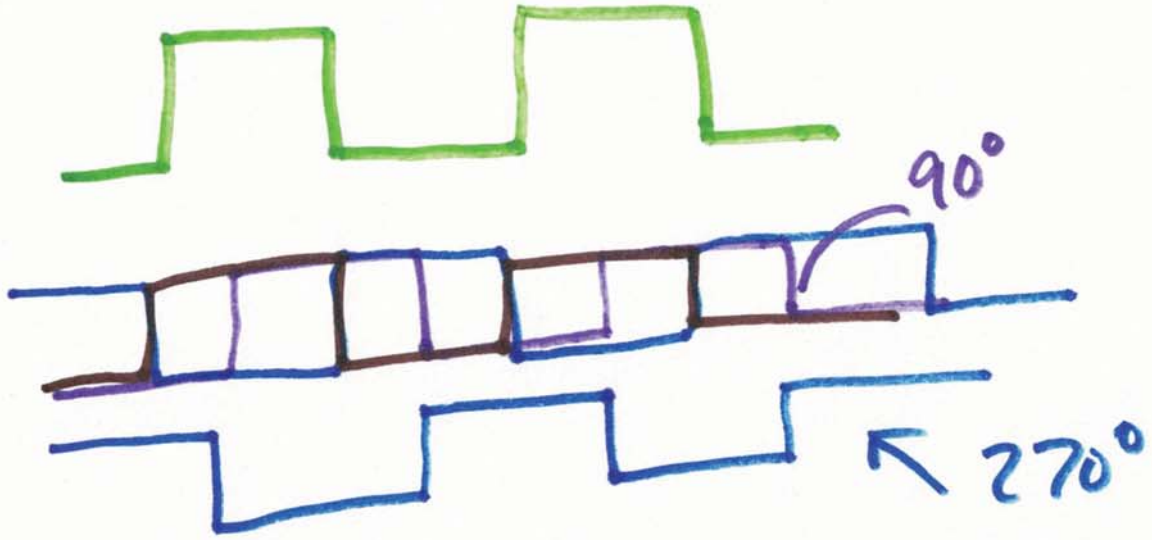


Figure 19.56 Implementation of a fully differential VCDL.



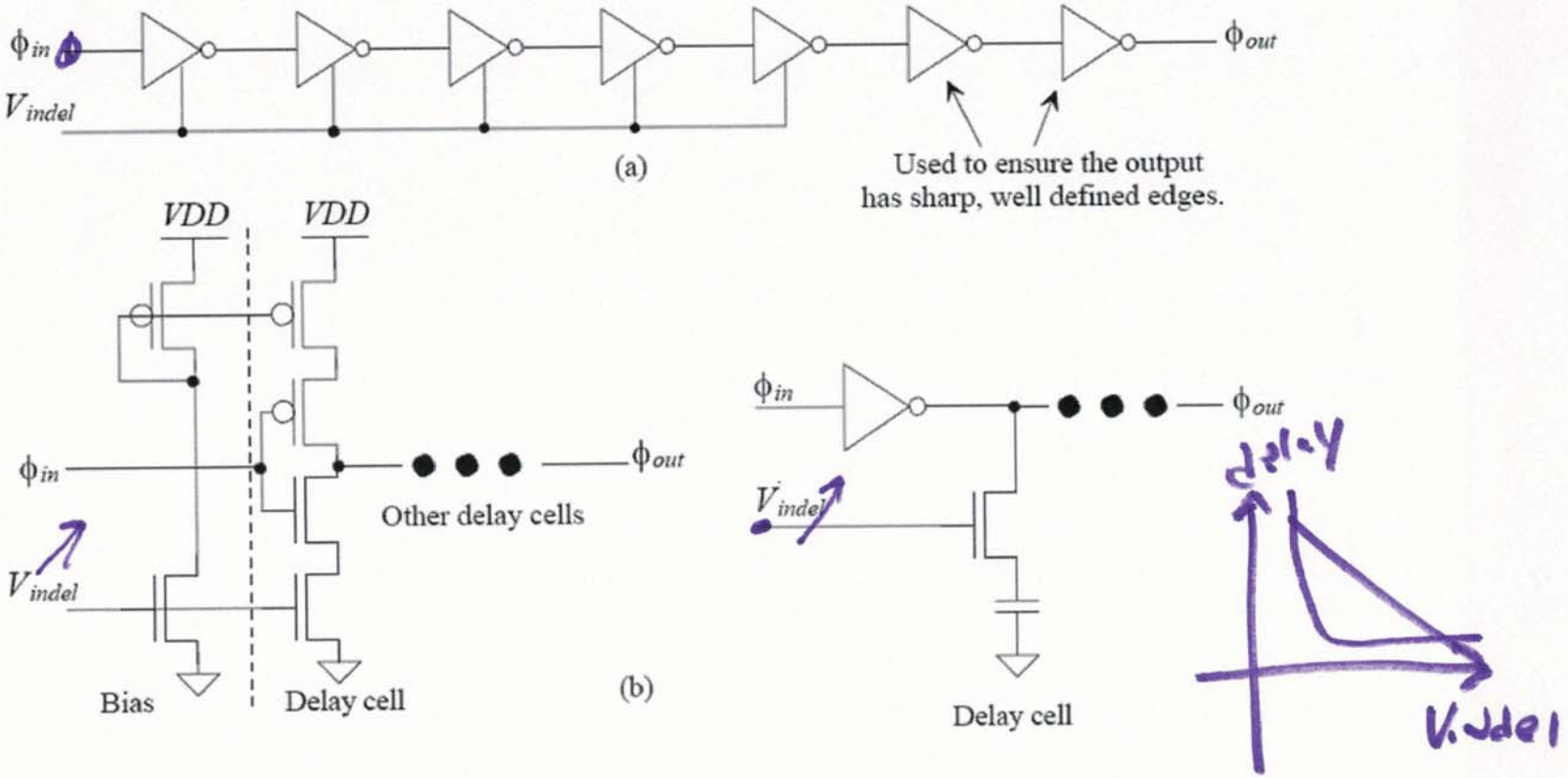


Figure 19.55 (a) VCDL made using inverter delay cells and (b) possible delay cells.

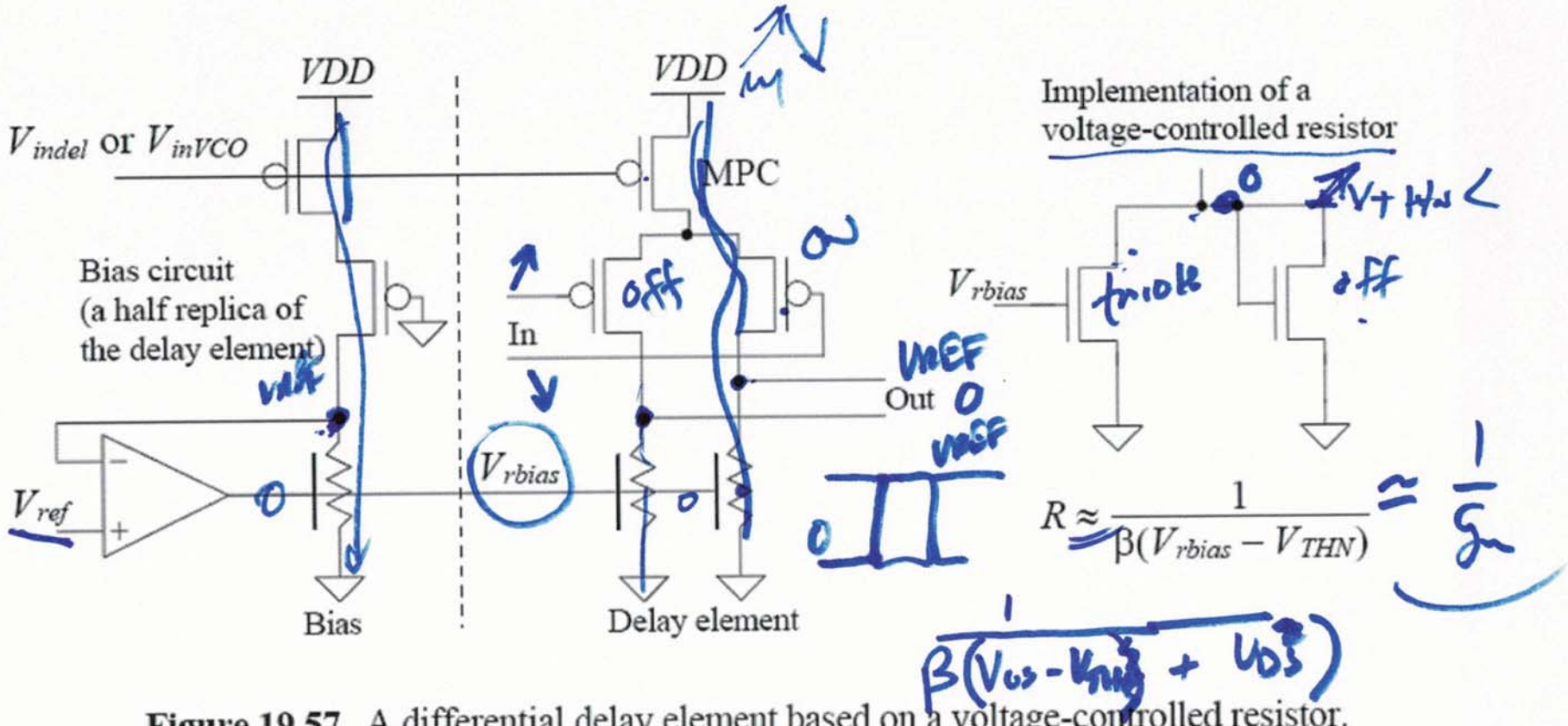


Figure 19.57 A differential delay element based on a voltage-controlled resistor. The bias circuit adjusts the value of the resistors used in the delay elements to sink the current sourced by the p-channel MOSFETs.

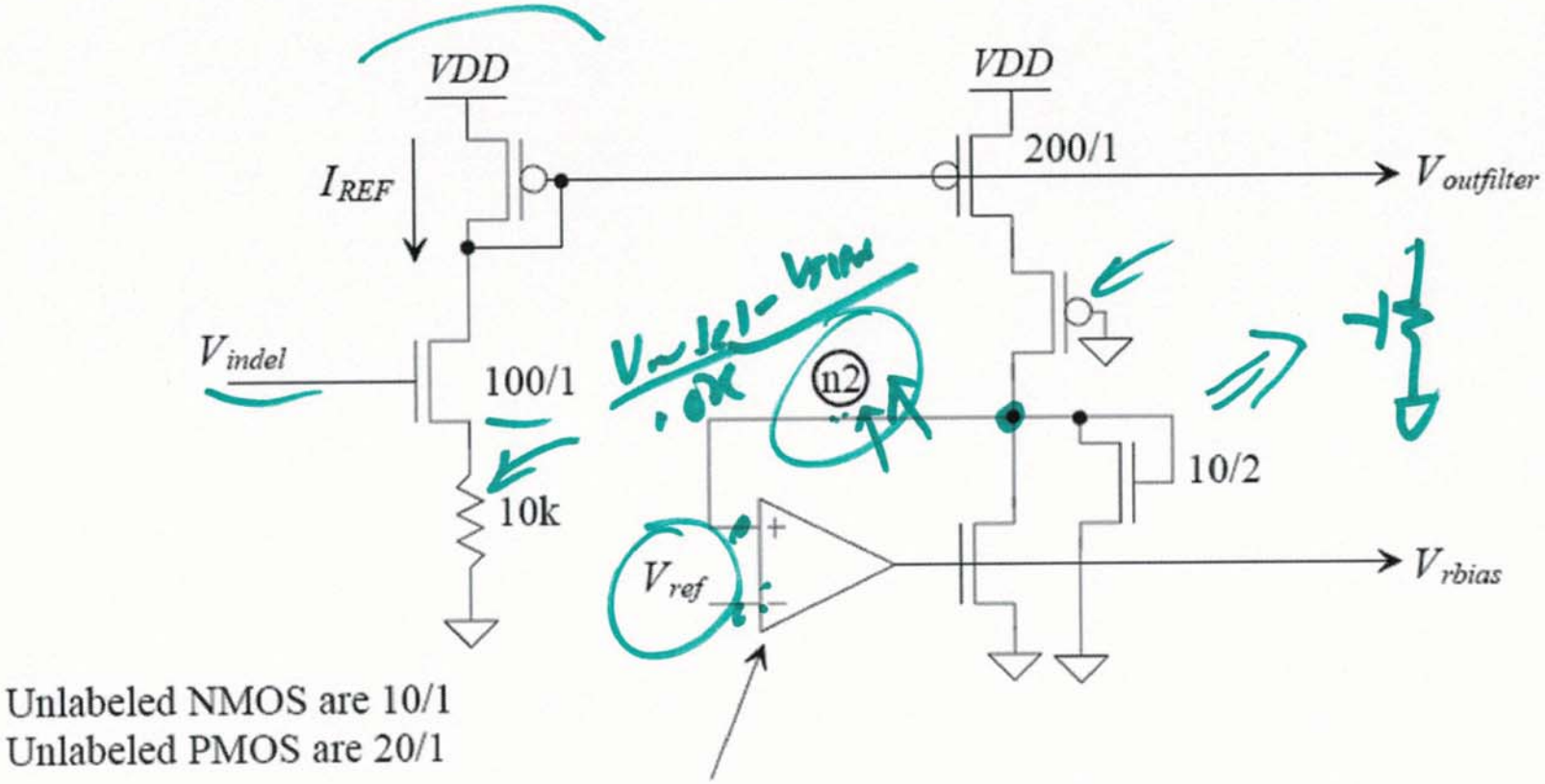


Figure 19.58 Bias circuit for a 500 ps delay line.

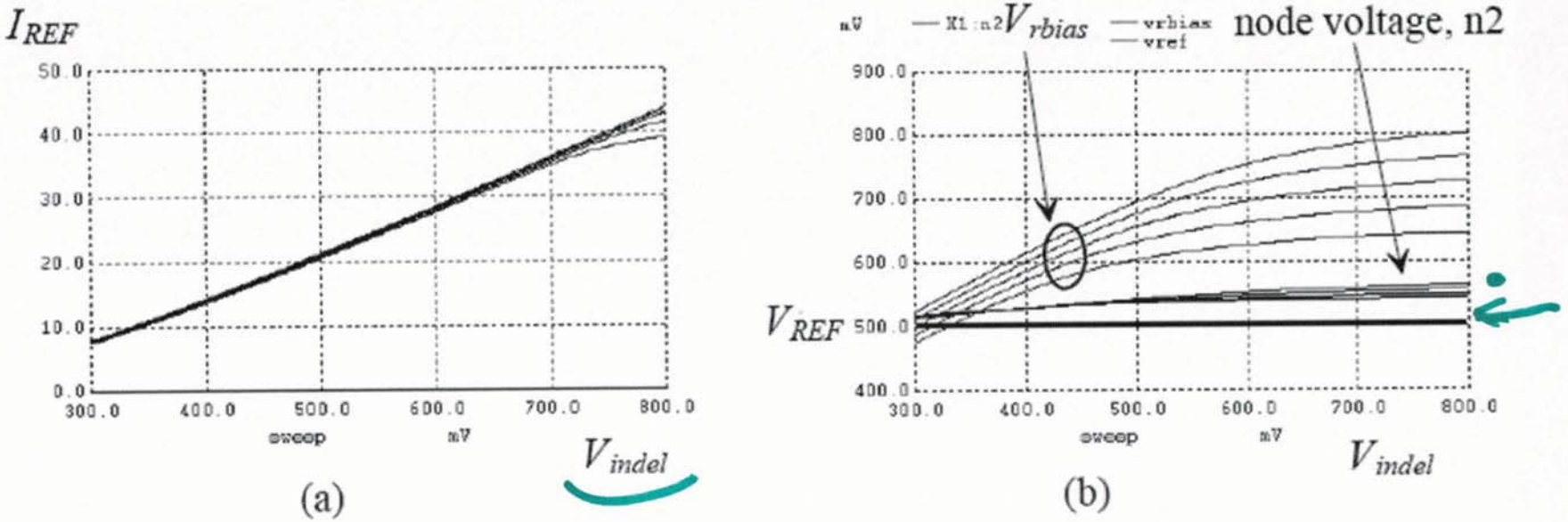


Figure 19.59 The performance of the bias circuit in Fig. 19.58.

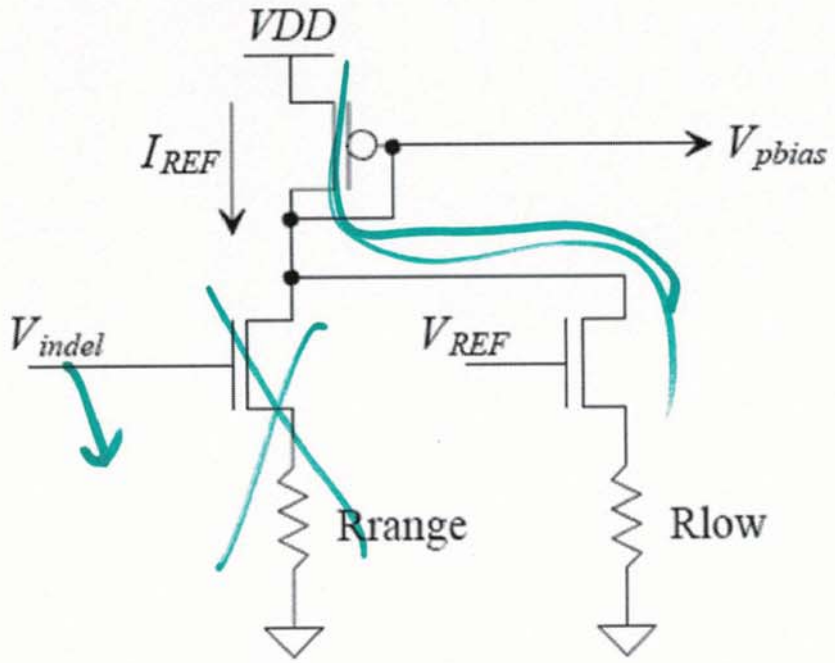


Figure 19.60 Lowering the current range in the bias circuit.