NOVEMBER 2, 2015

Lecture 19

EE 6 721

MEMORY circuit Design

19.4 System Considerations

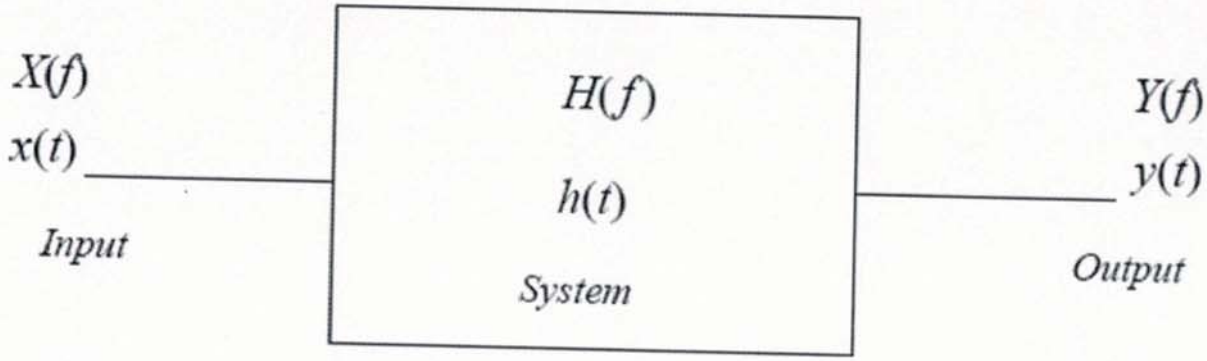


Figure 19.40 Representation of a system with input and output.

distortionless transmission

$$y(t) = x(t - t_d) \cdot K$$

↑ output

↑ delay through system

Spectrum

$$Y(f) = K \cdot X(f) \cdot e^{-t_d \cdot 2\pi f j}$$

$$\angle Y(f) = -2\pi f \cdot t_d$$

$$|Y(f)| = k \cdot |X(f)|$$

2)

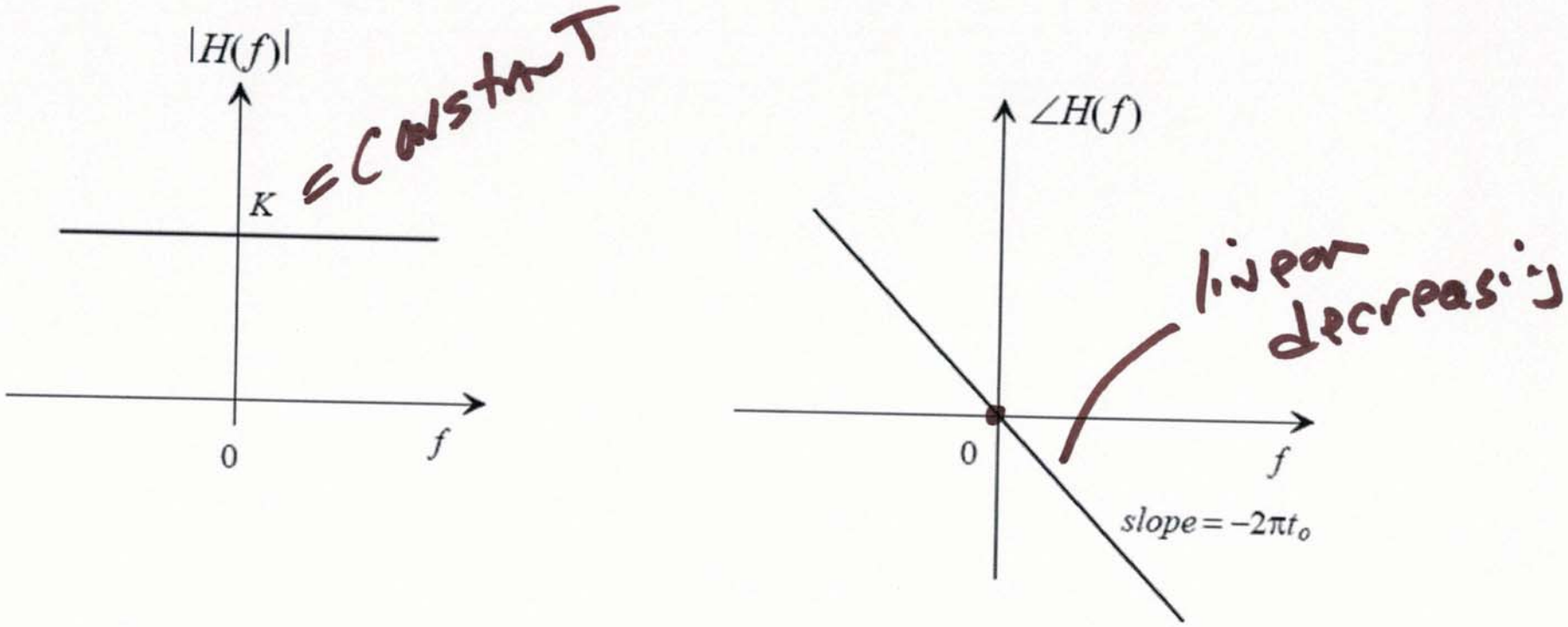
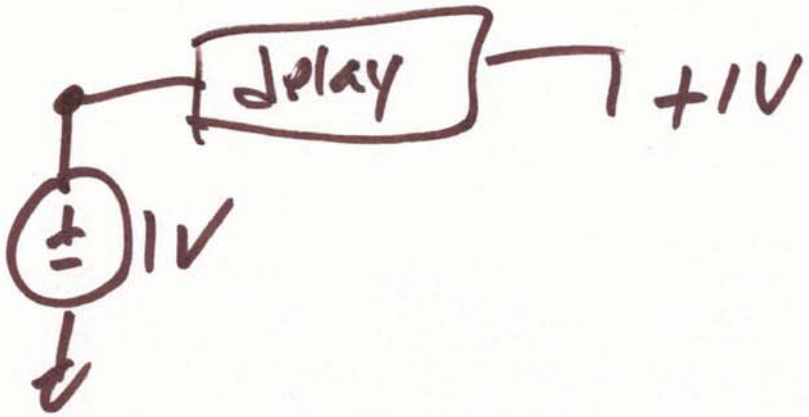


Figure 19.41 Magnitude and phase response of a distortionless system.



37)

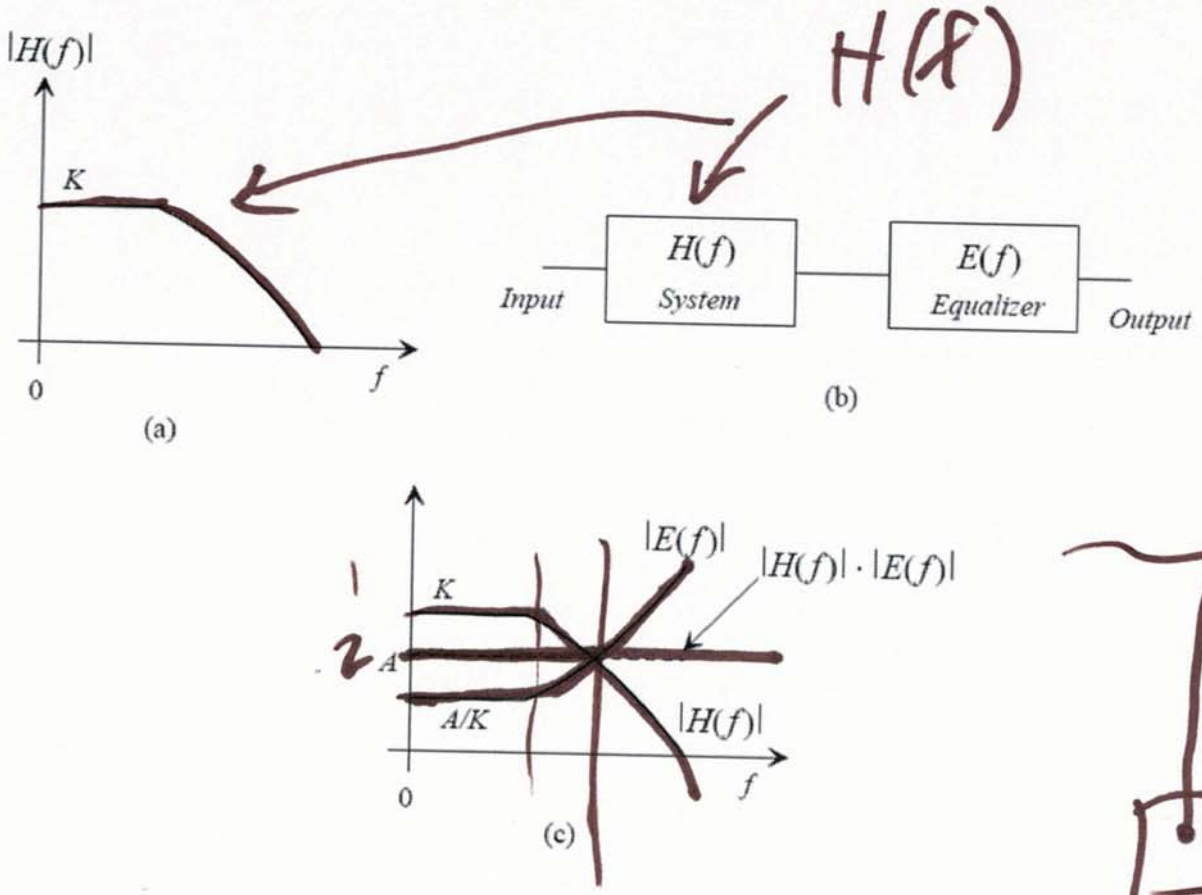


Figure 19.42 Using an equalizer to lower distortion in a system.

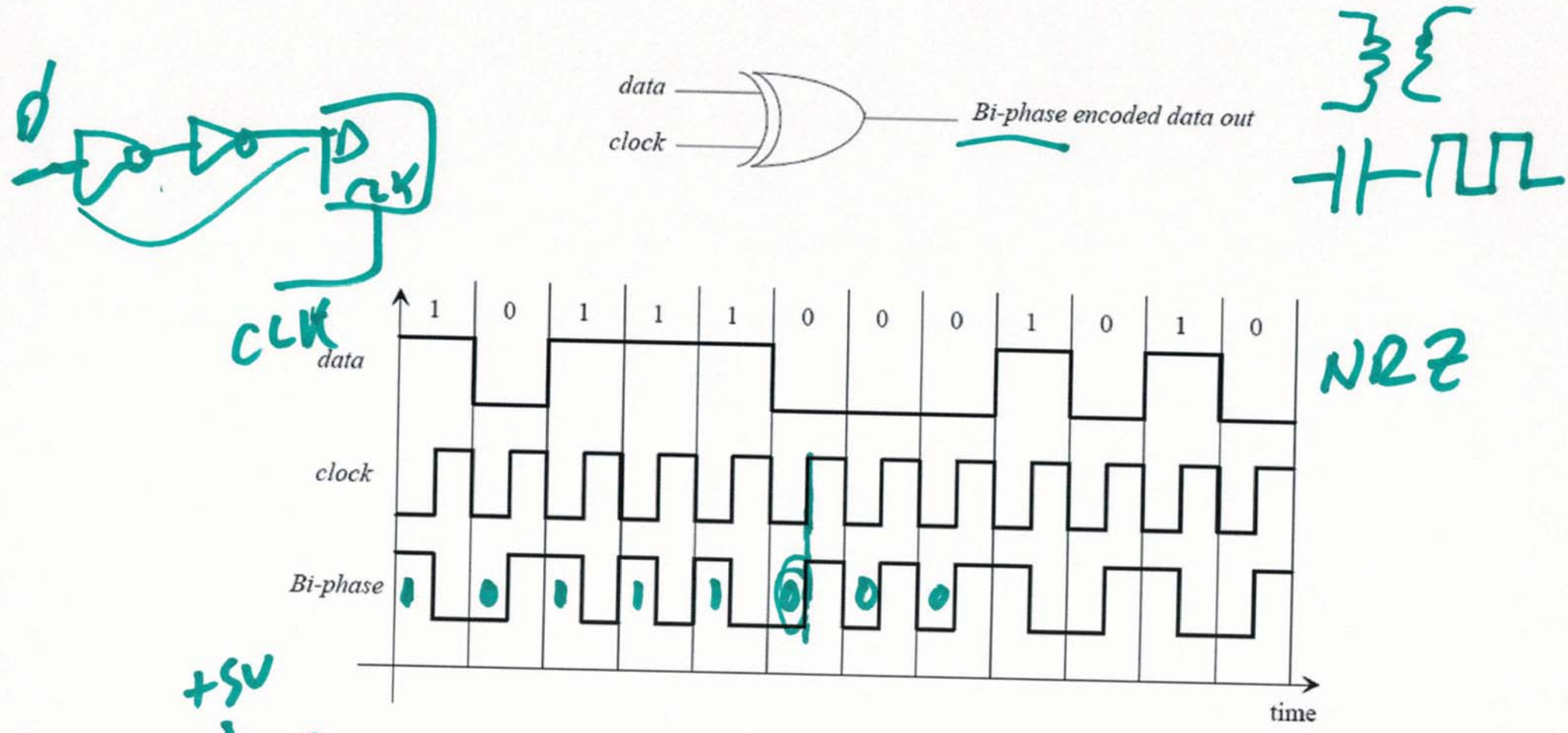
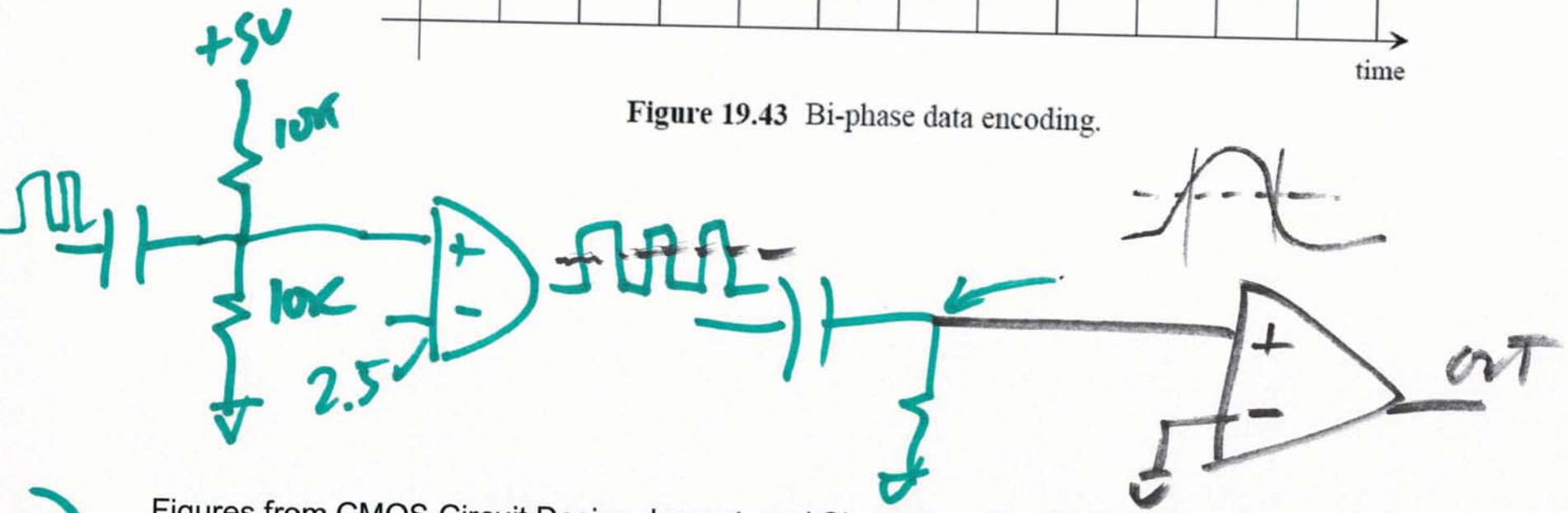


Figure 19.43 Bi-phase data encoding.



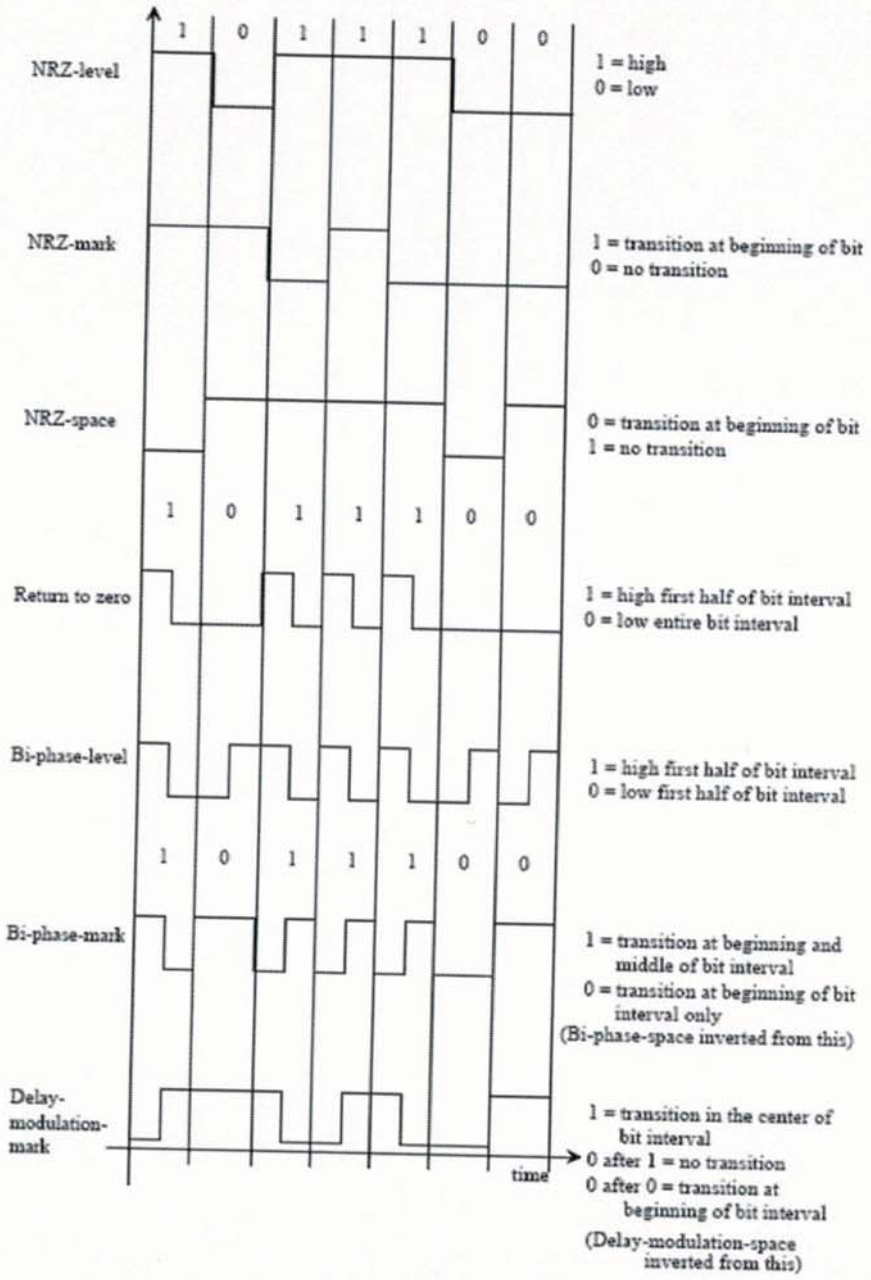


Figure 19.44 Data transmission formats.

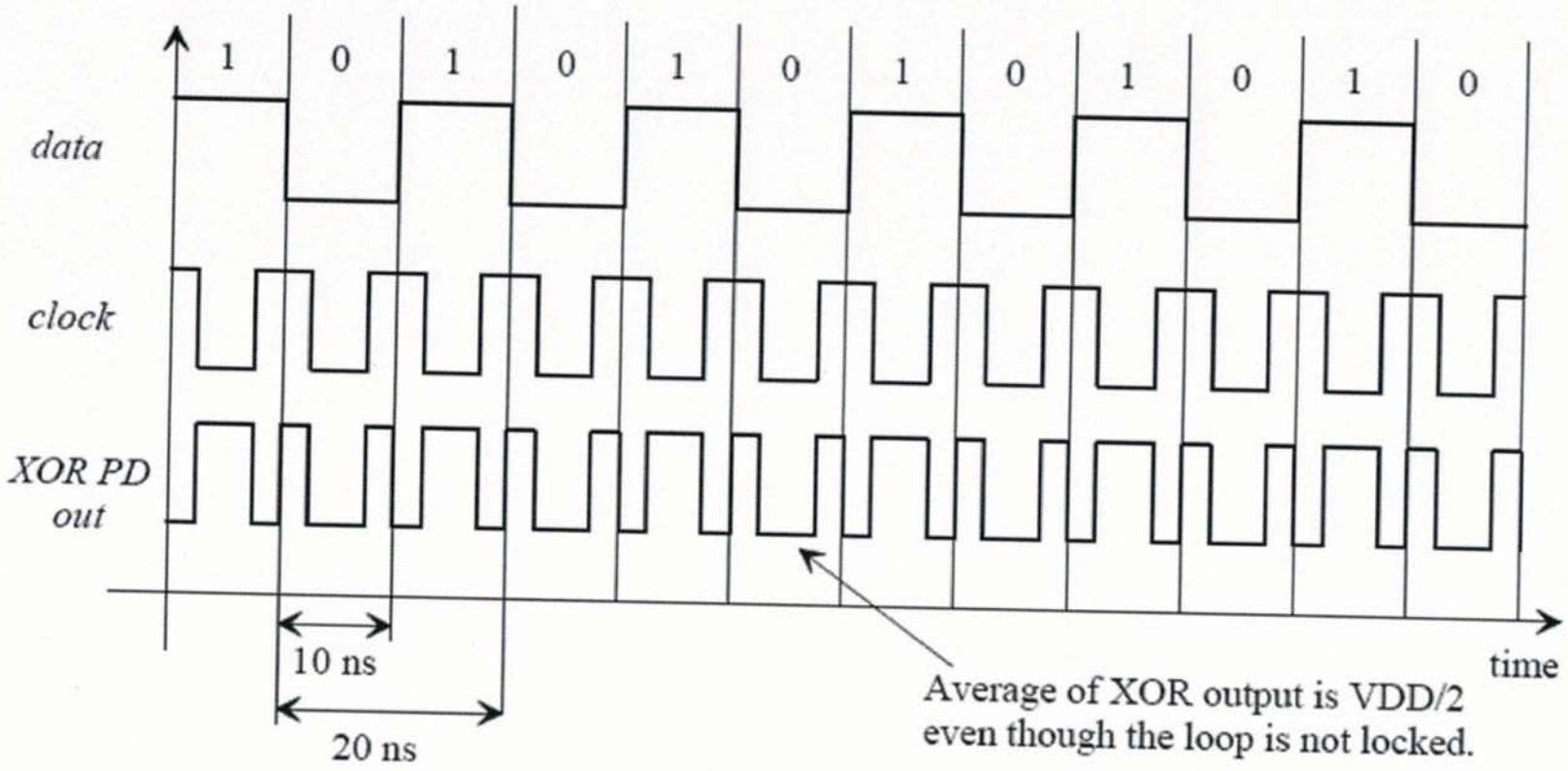


Figure 19.45 The problems of using clock without the divide by 2 to lock on data.

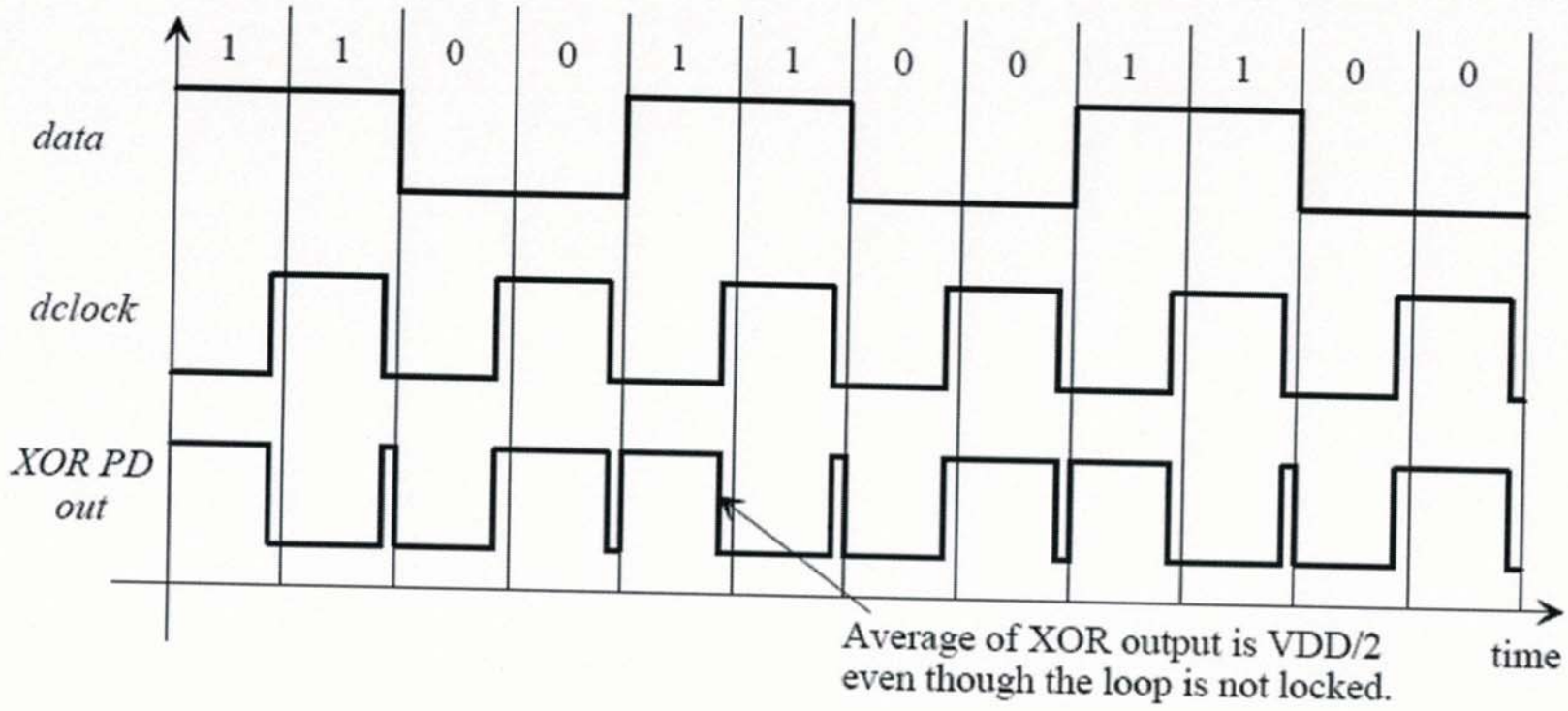


Figure 19.46 Problems trying to lock on a data stream that is one-half the dclock frequency.

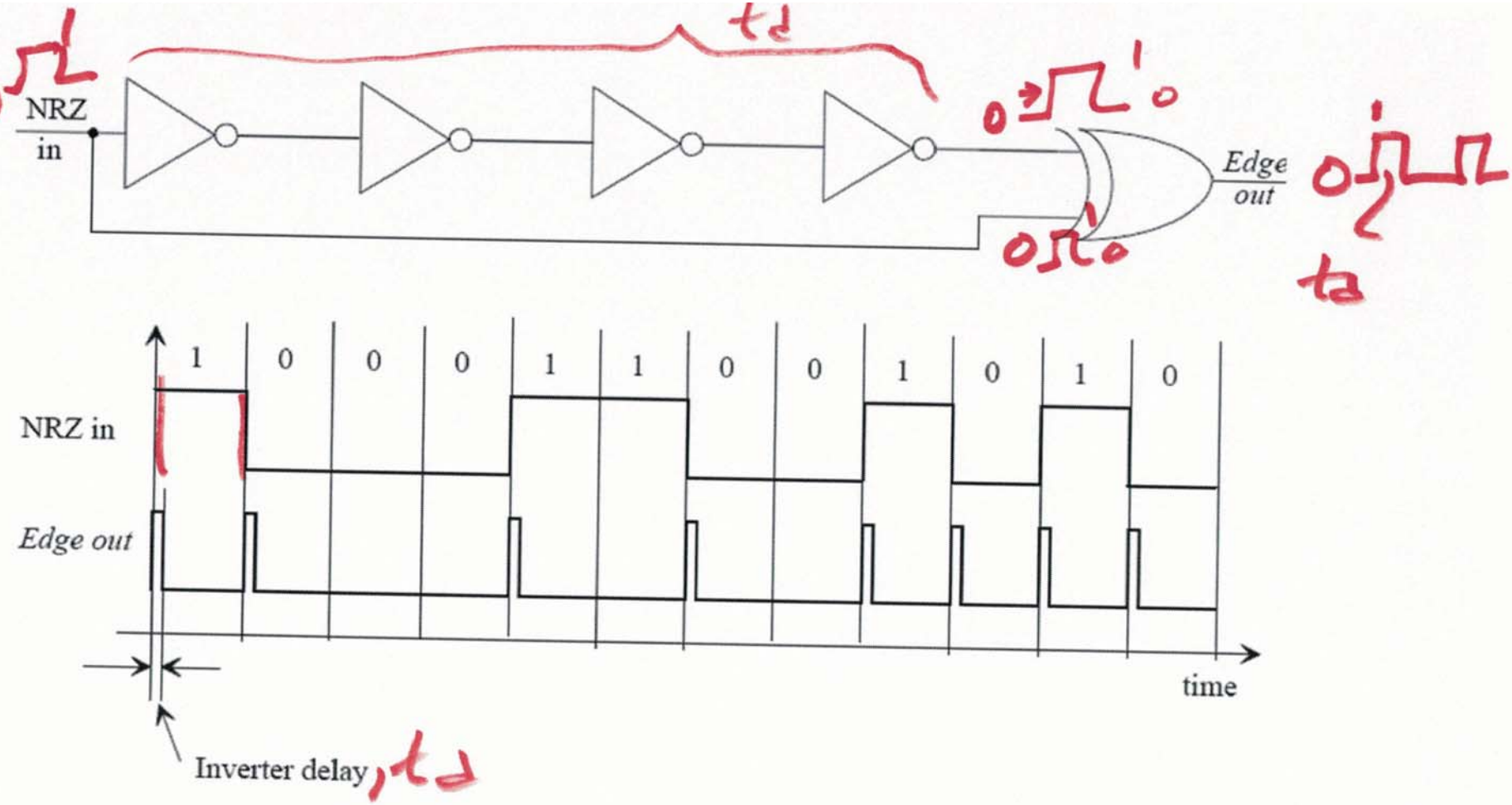


Figure 19.47 Detecting the edges in NRZ data.

Using an edge detector.

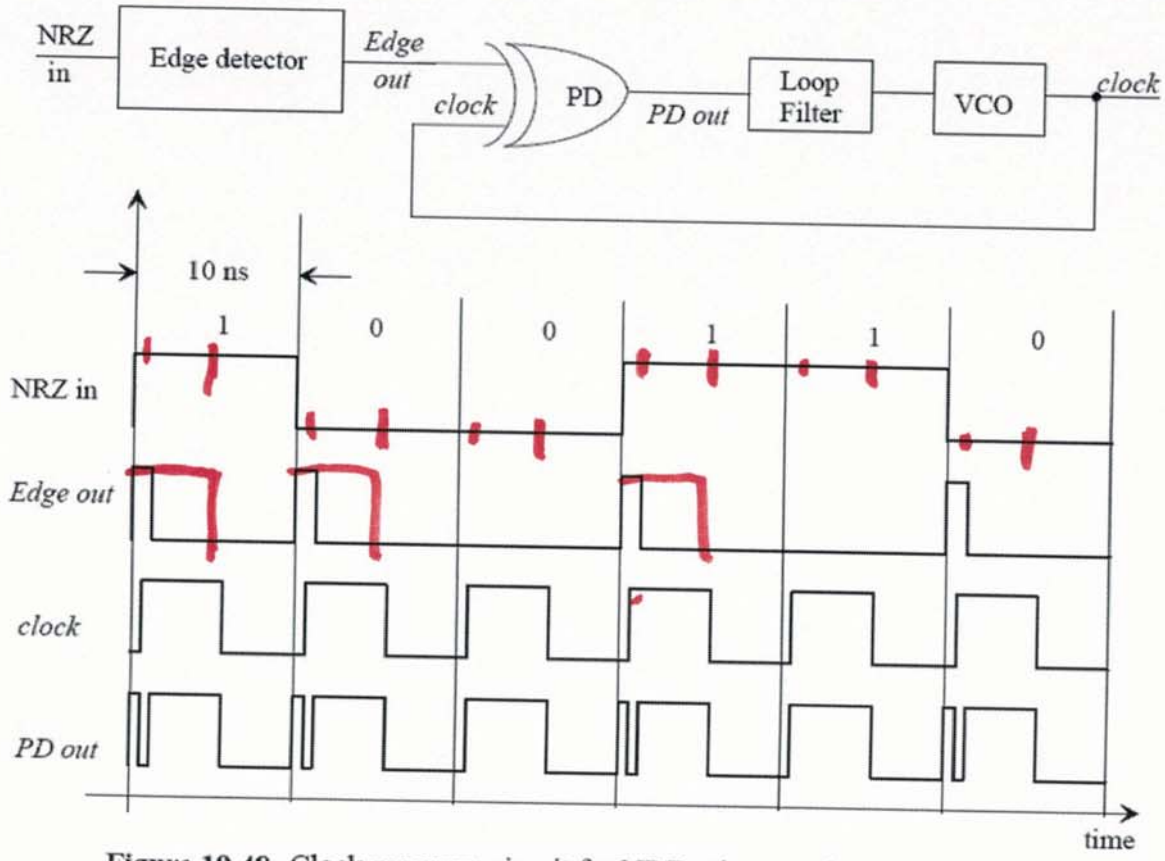
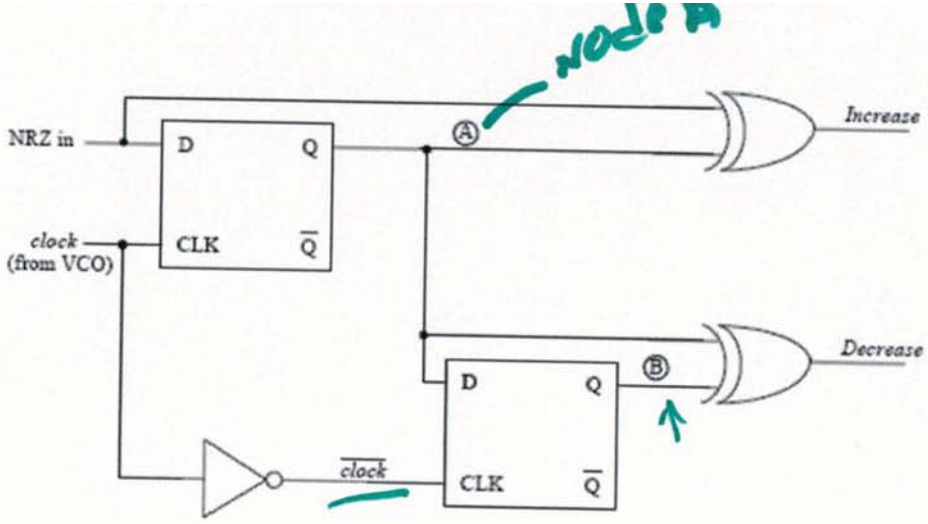


Figure 19.48 Clock-recovery circuit for NRZ using an edge detector. Note that the DPLL is in lock, when the rising edge of clock is centered on the edge output pulse.



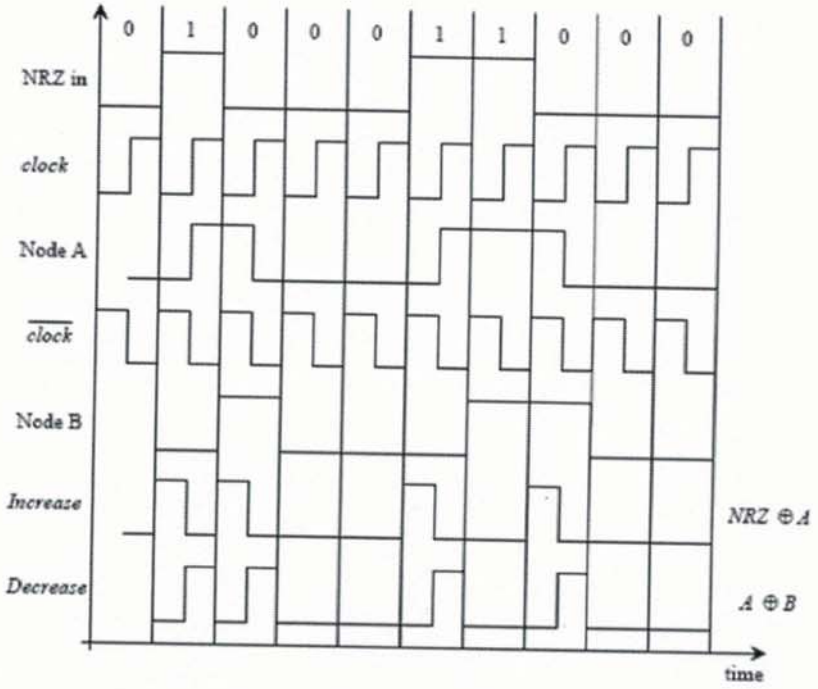
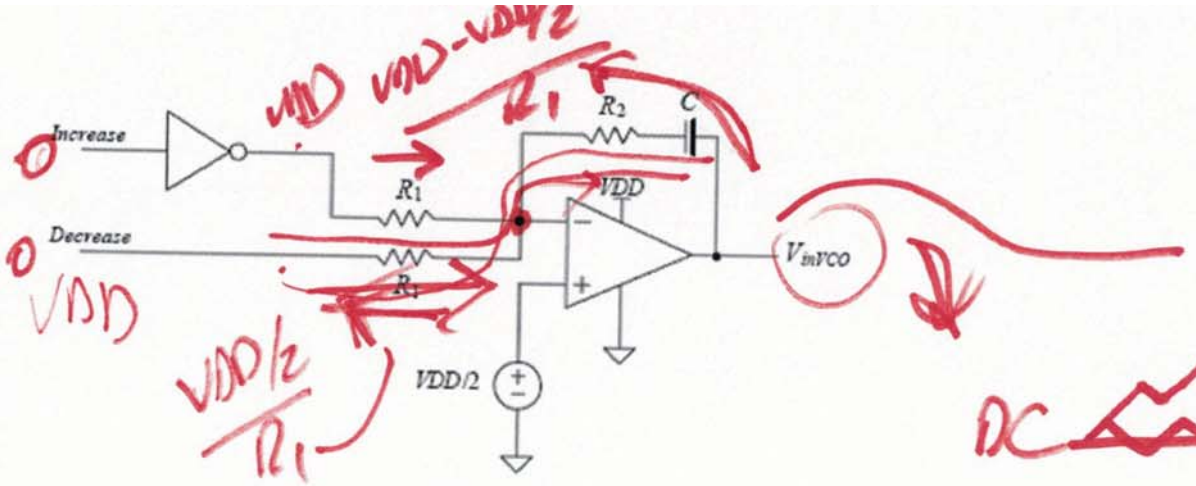
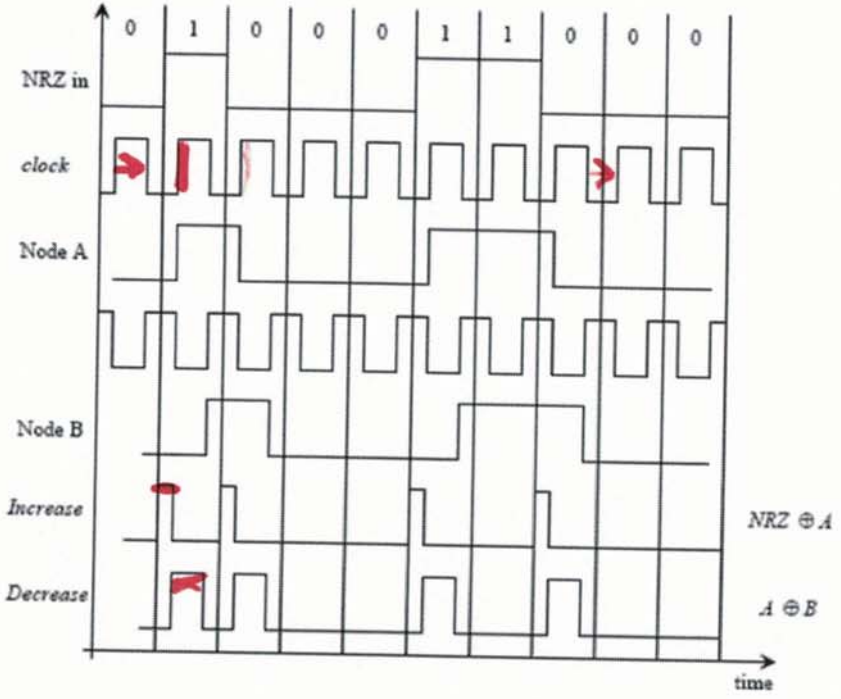


Figure 19.49 The PD (Hogge) portion of a self-correcting, clock-recovery circuit in lock.



(a)



(b)

Figure 19.50 (a) Possible loop filter used in a self-correcting (Hogge) DPLL and (b) waveforms when the loop is not in lock and the clock leads the center of the data.

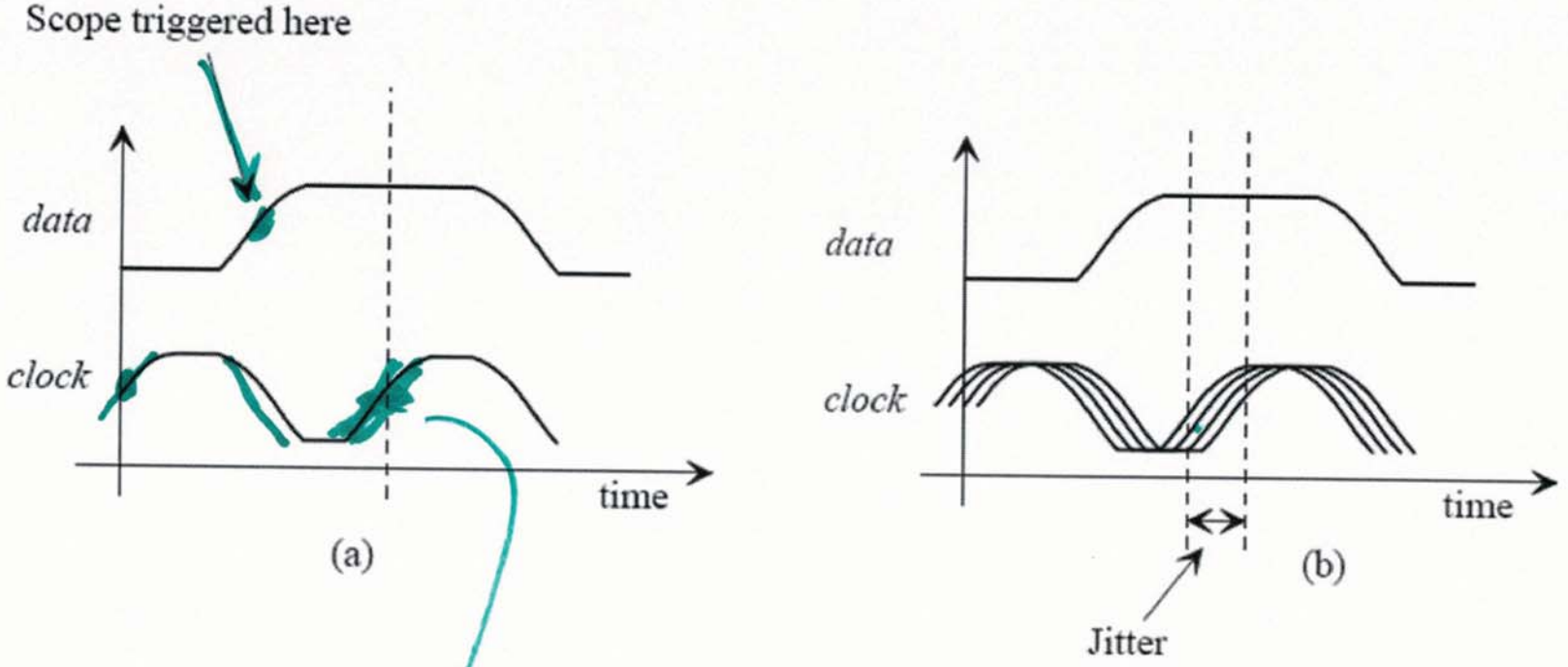


Figure 19.51 (a) Idealized view of clock and data without jitter and (b) with jitter.

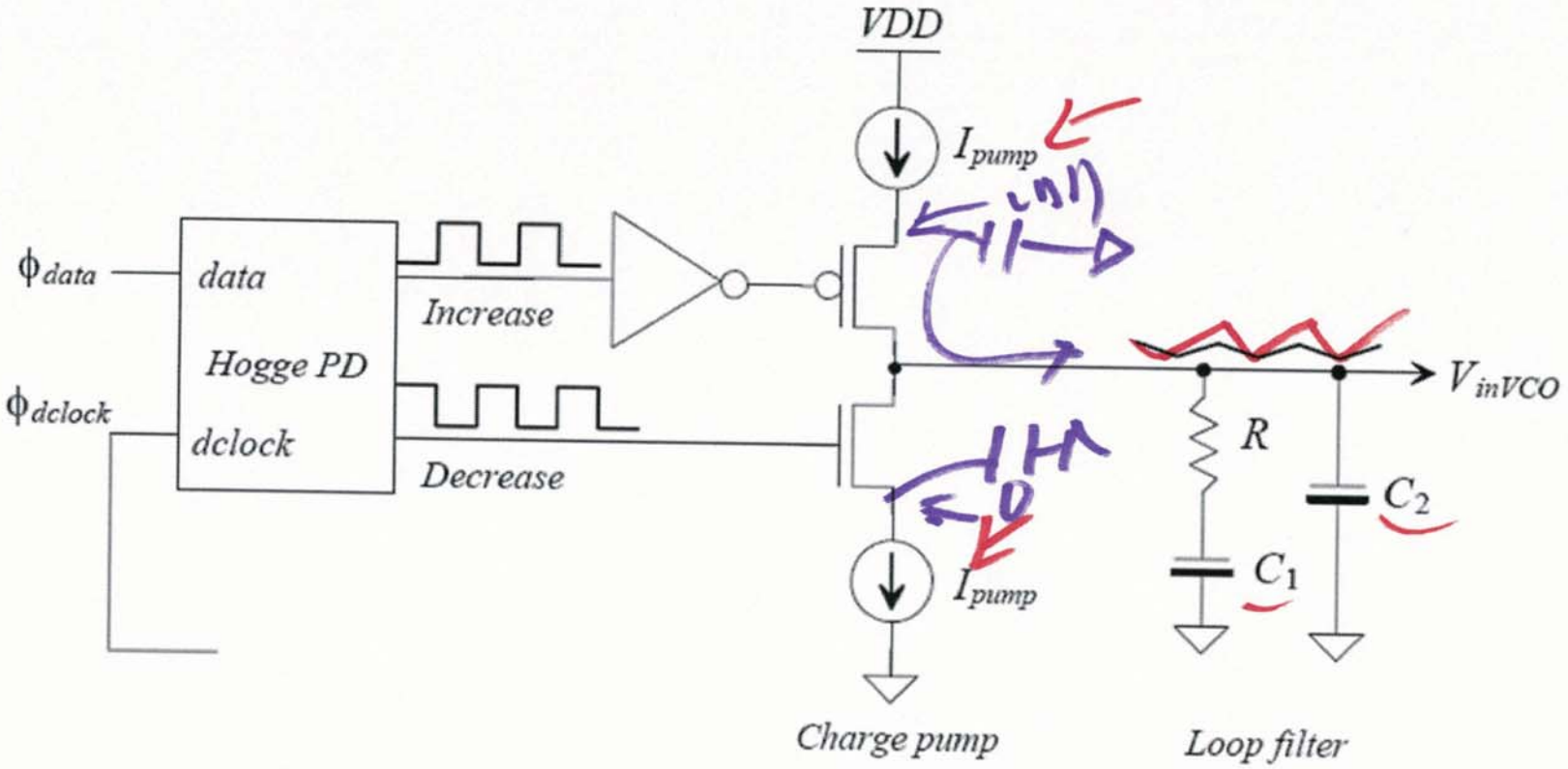


Figure 19.52 Self-correcting PD with charge pump output.