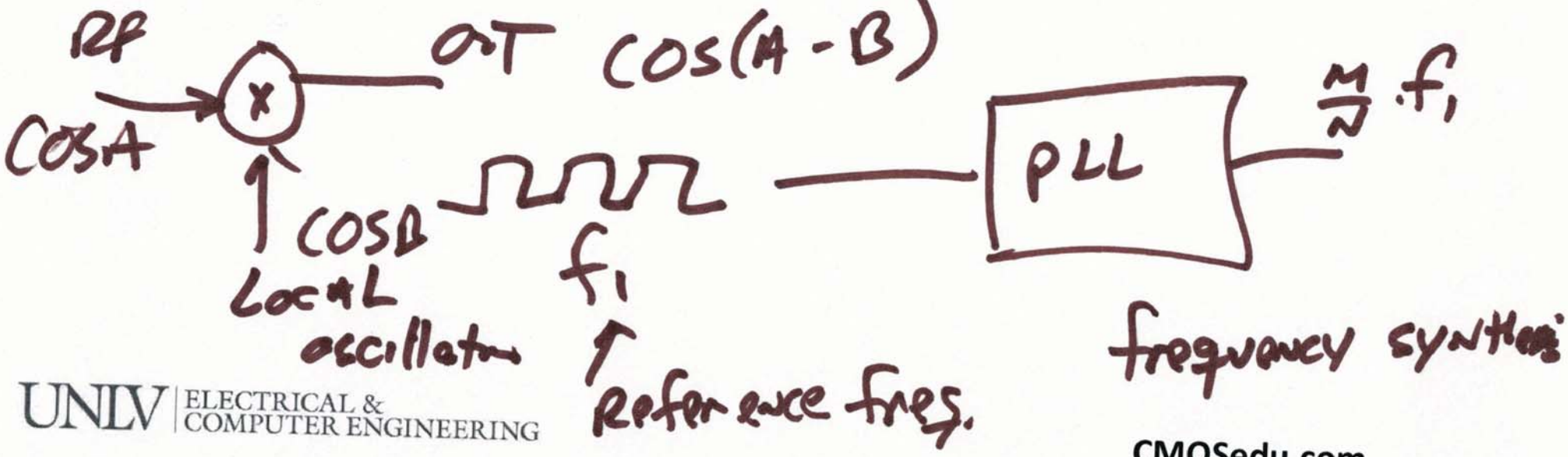
Lecture 16 ECG 721

OCT. 21, 2015

Ch. 19 Digital PLLs

Phase-Locked Loop



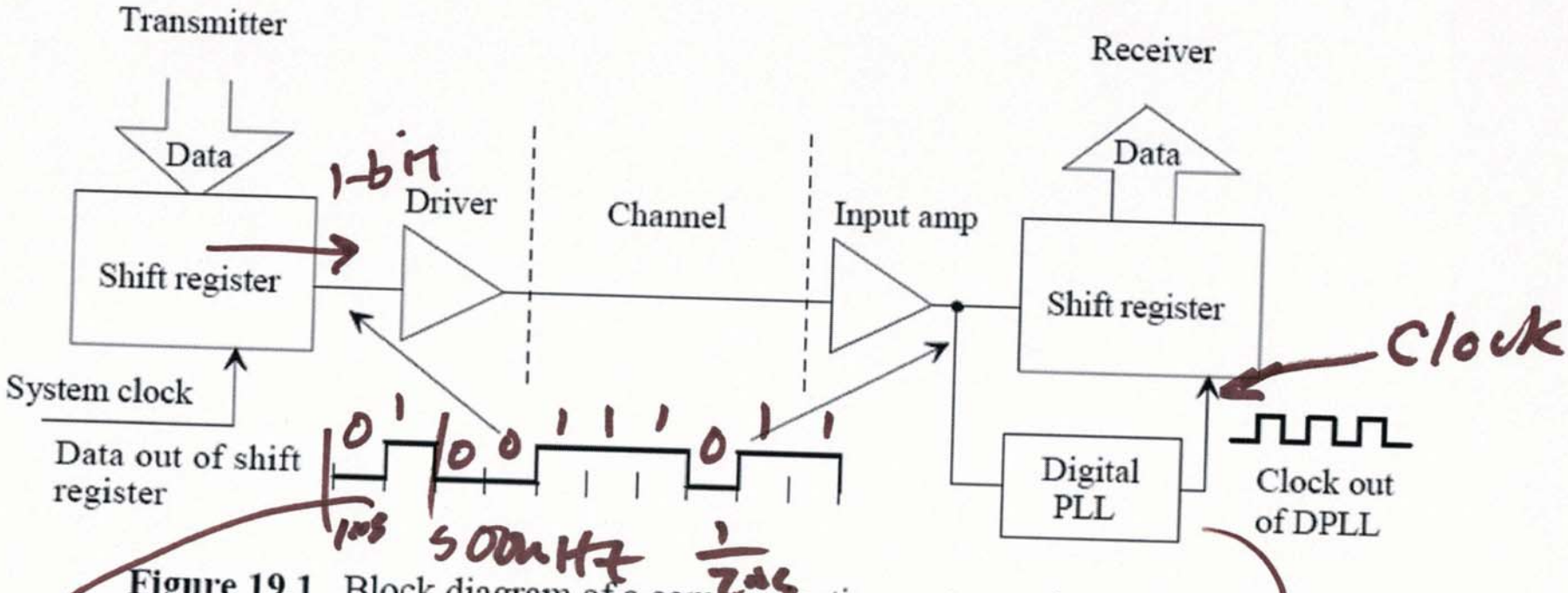


Figure 19.1 Block diagram of a communication system using a DPLL for the generation of a clock signal.

NRZ 1Gbit/s

Clock & data recovery (CDR)

2)

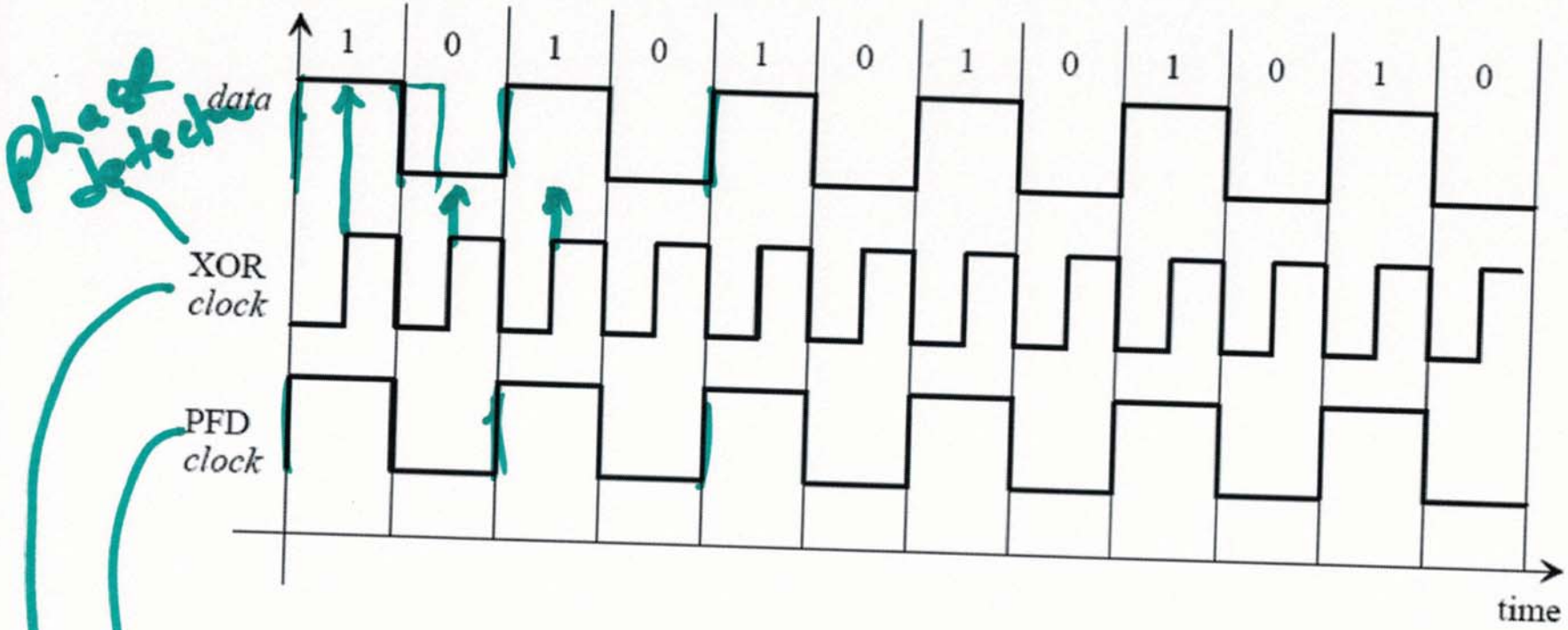


Figure 19.2 Data input to DPLL in lock and possible clock outputs using the XOR phase detector and PFD.

Frequency Synthesis

CDR

Phase Frequency Detector

3)

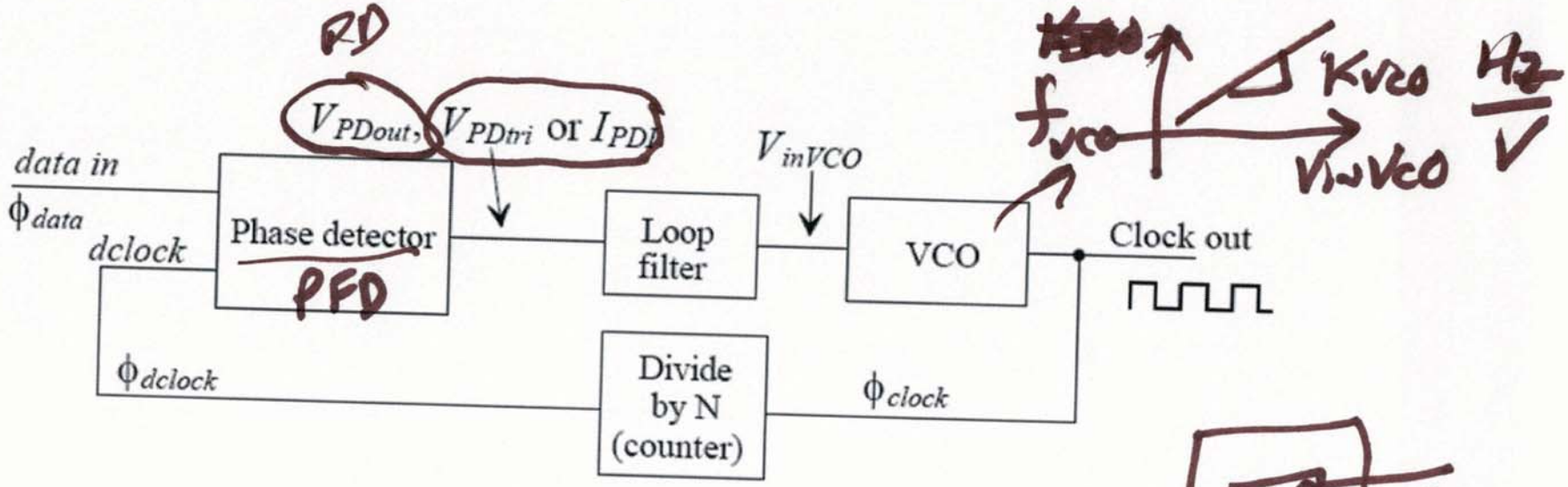
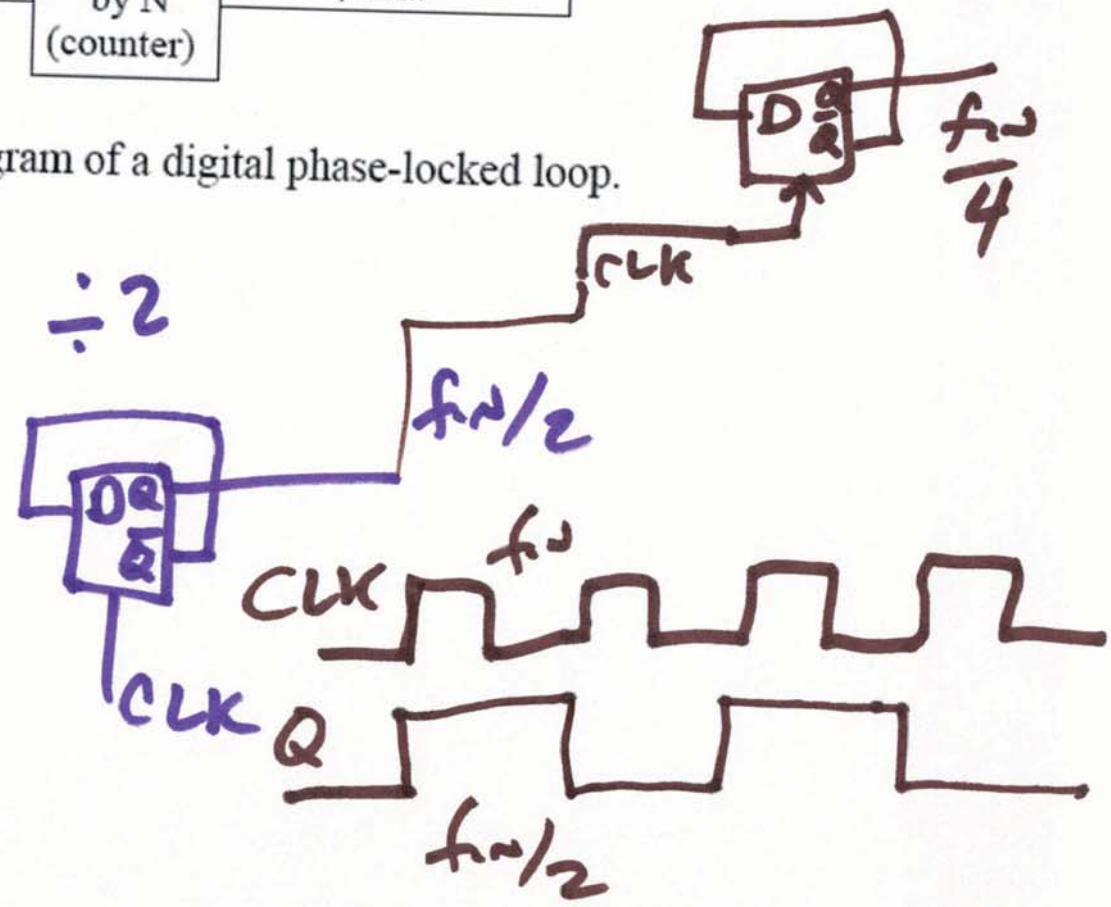
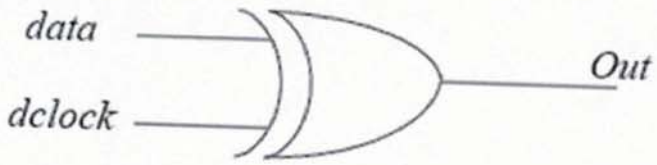


Figure 19.3 Block diagram of a digital phase-locked loop.



$$\theta_{dclock} = \frac{\Delta t}{2T} \cdot 2\pi = \frac{\theta_{clock}}{2}$$



data	dclock	Out
0	0	0
0	1	1
1	0	1
1	1	0

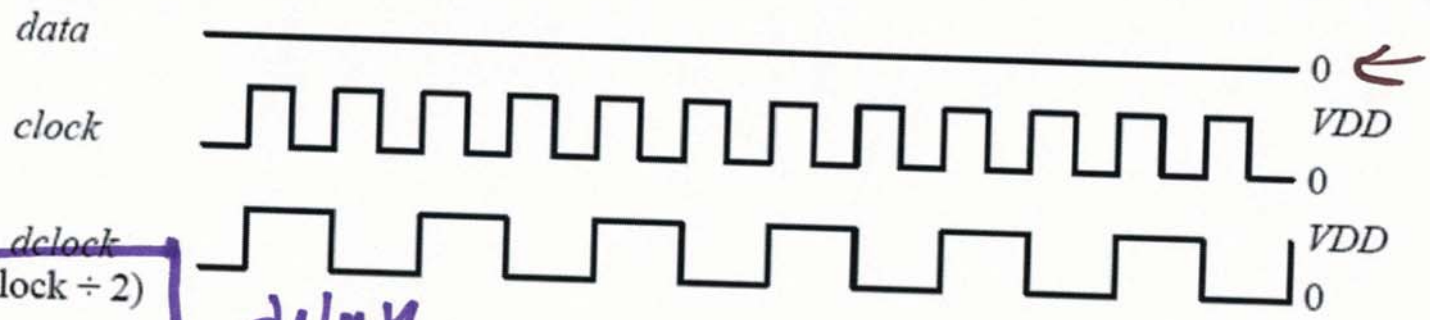
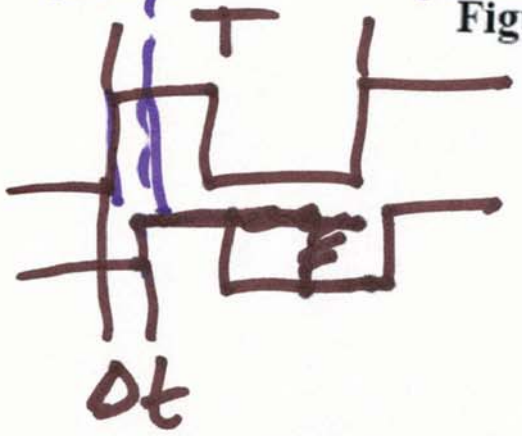
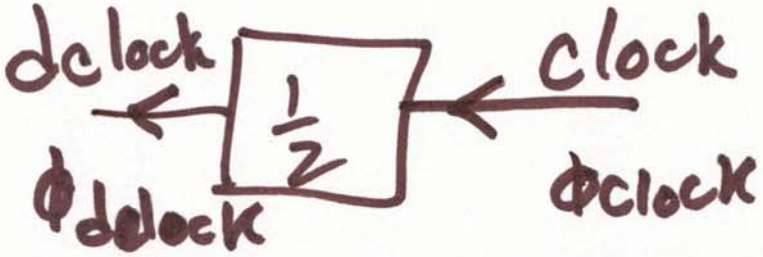


Figure 19.4 Operation of the XOR phase detector.



$$\theta = \frac{\Delta t}{T} \cdot 2\pi$$



$$\phi_{dclock} = \frac{\phi_{clock}}{2}$$

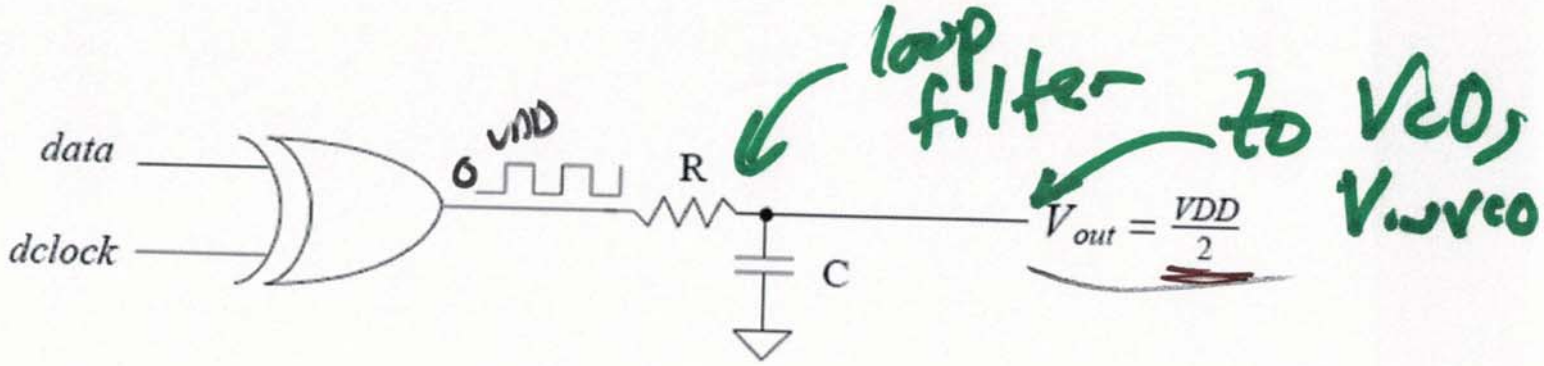
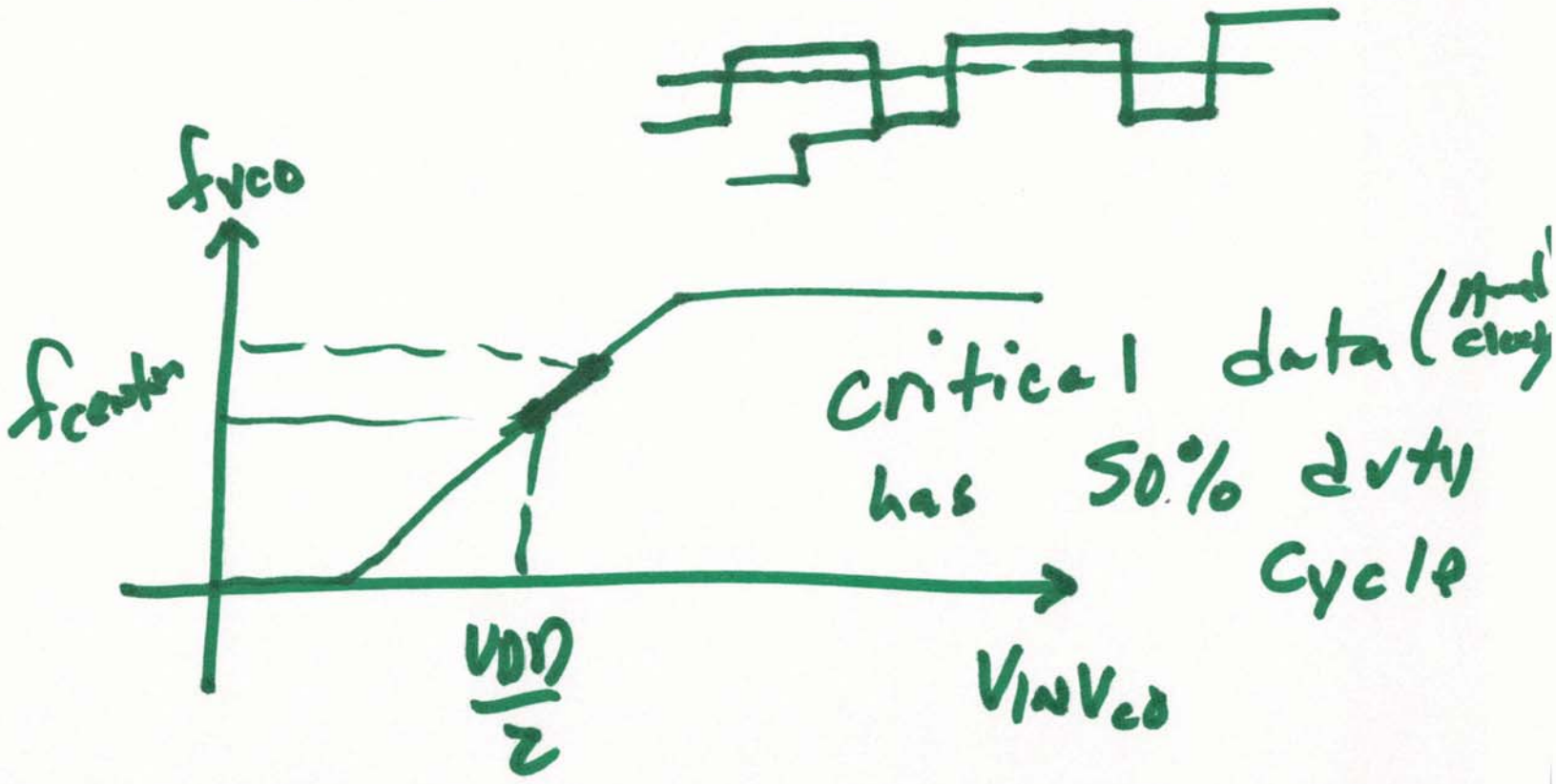


Figure 19.5 How the filtered output of the phase detector becomes VDD/2.



6)

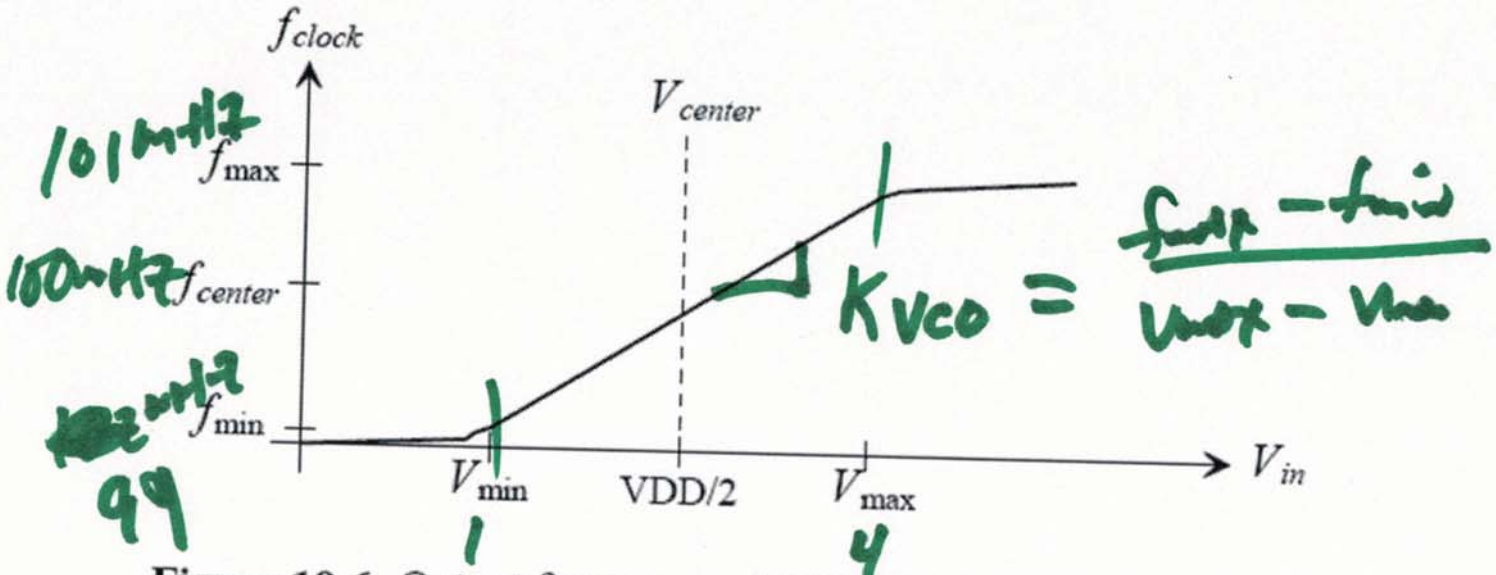


Figure 19.6 Output frequency of VCO versus input control voltage.

XOR

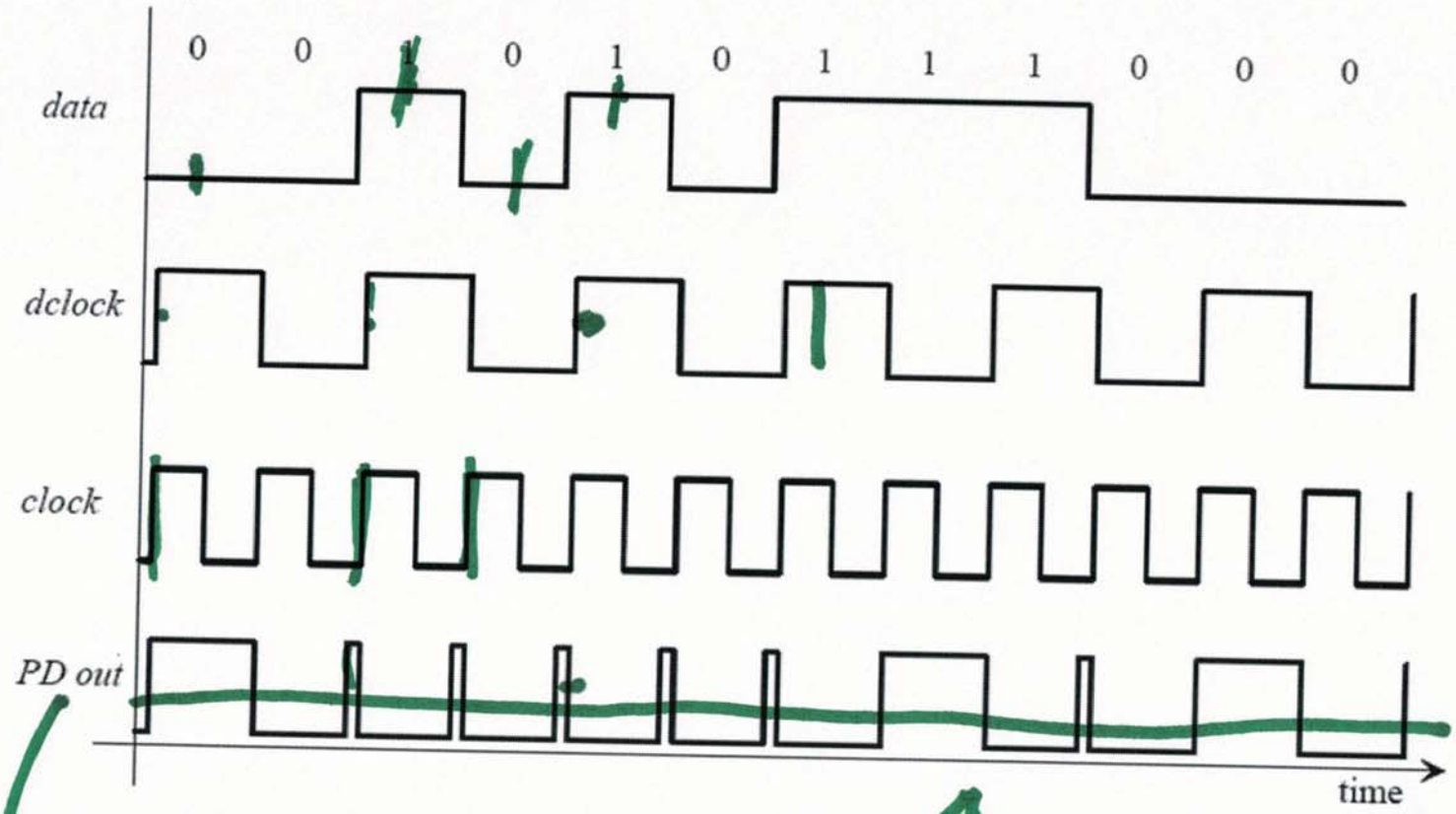
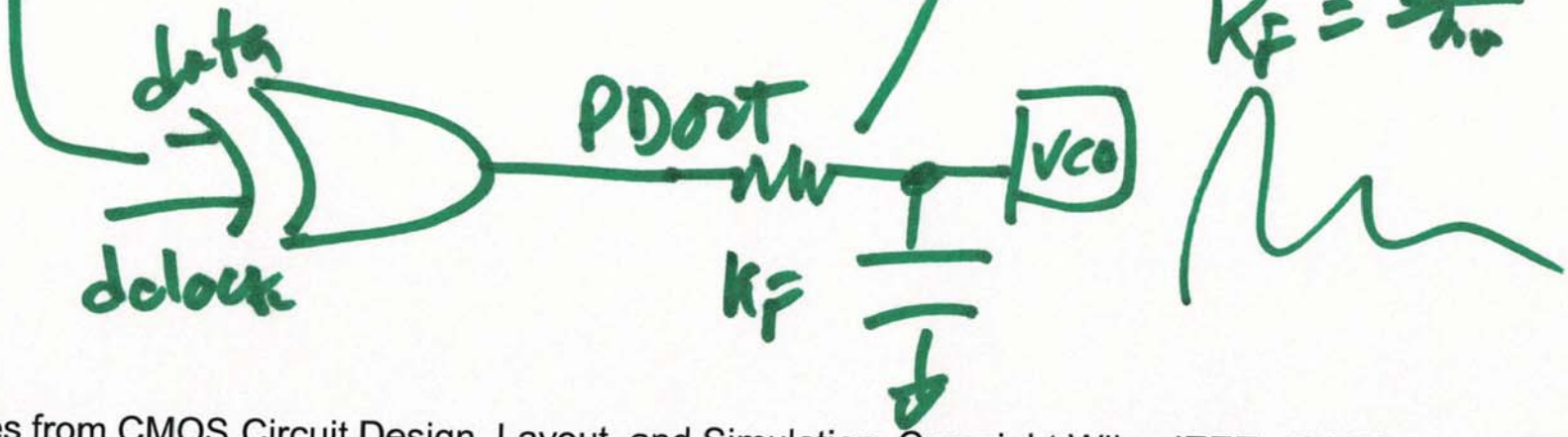
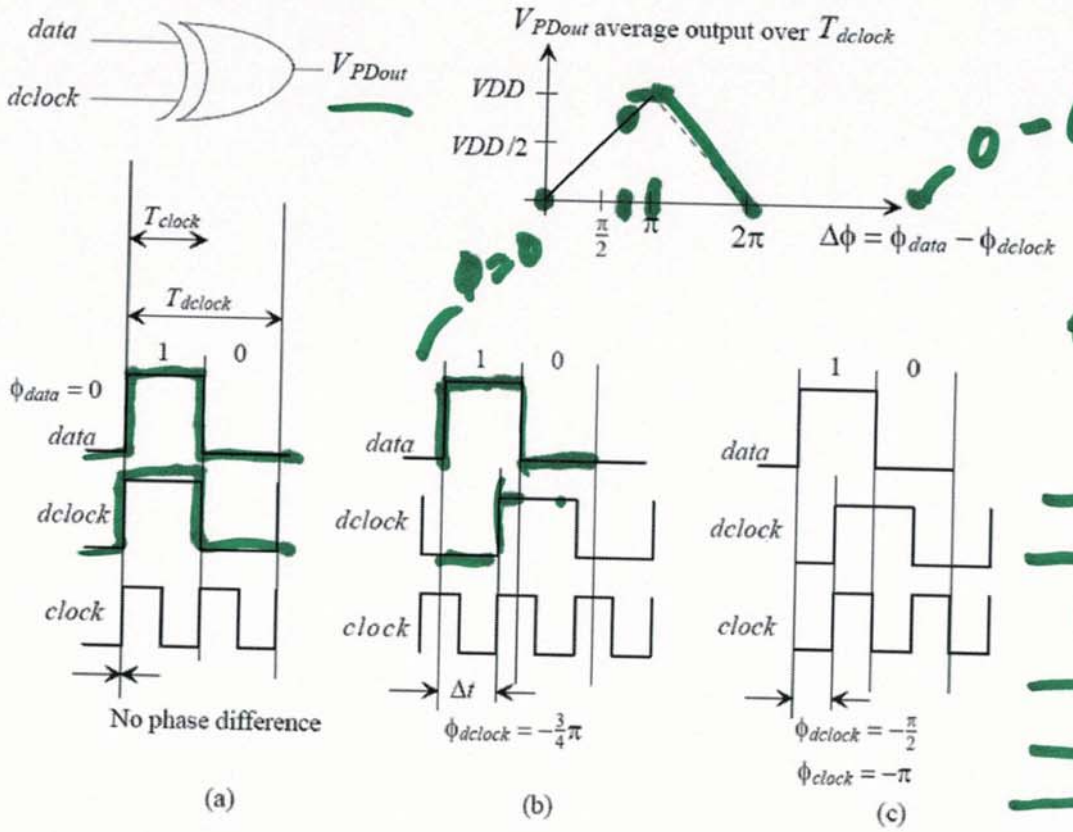


Figure 19.7 Possible XOR phase-detector inputs and the resulting output.

$K_F = \frac{2\pi}{\lambda_0} = \frac{1}{1+j\omega RC}$



8)



$0-(-\frac{3}{4}\pi)$

$\Delta\phi = \frac{3}{4}\pi$

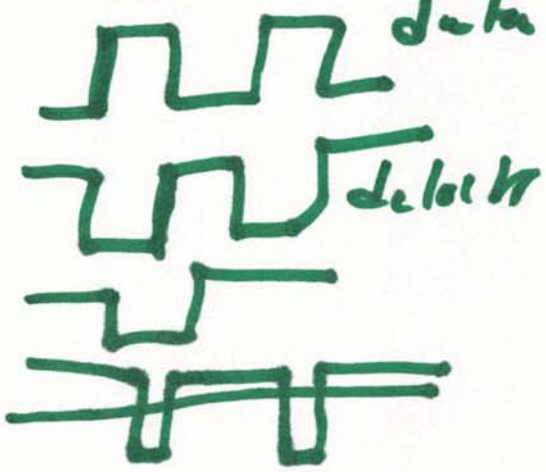
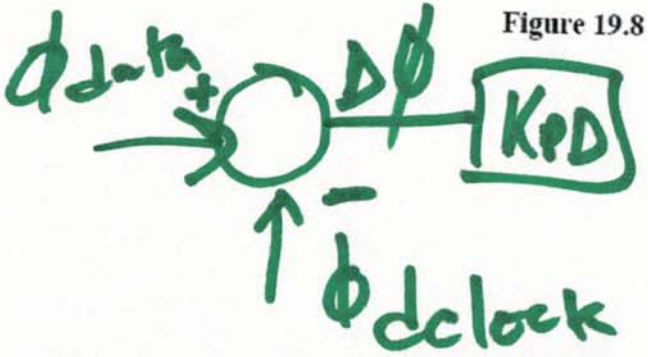
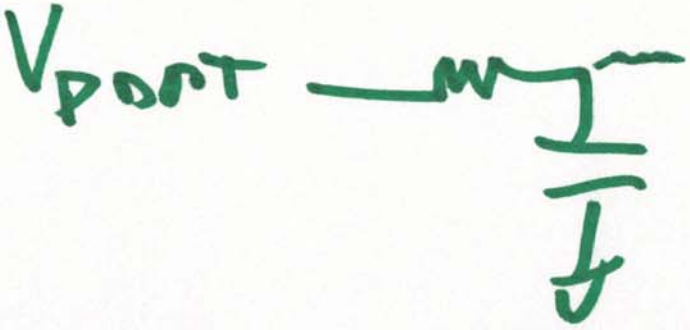


Figure 19.8 XOR PD output for various inputs (assuming input data are a string of alternating ones and zeros).



$\Delta\phi = 0-(-\pi)$

$= \pi$



a)

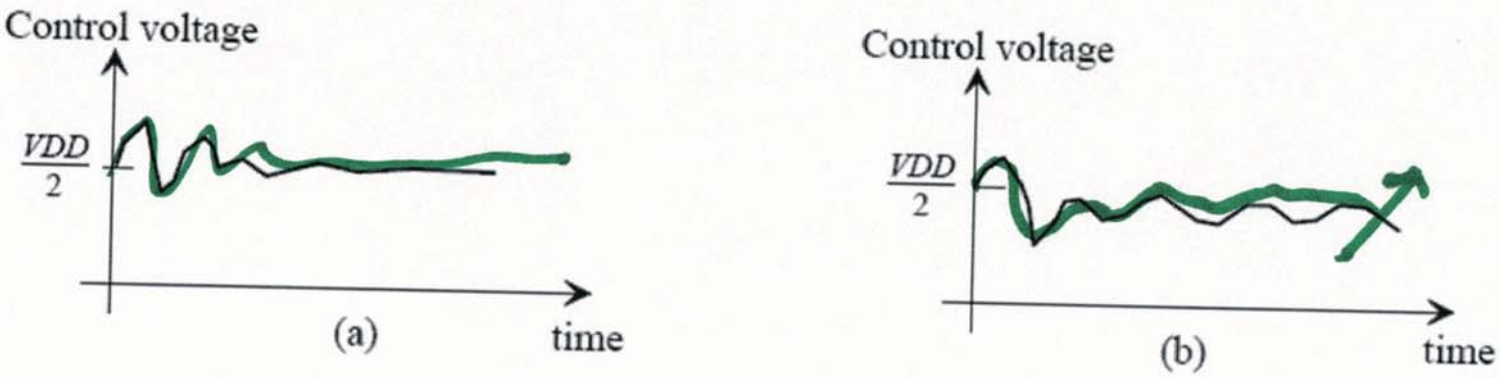
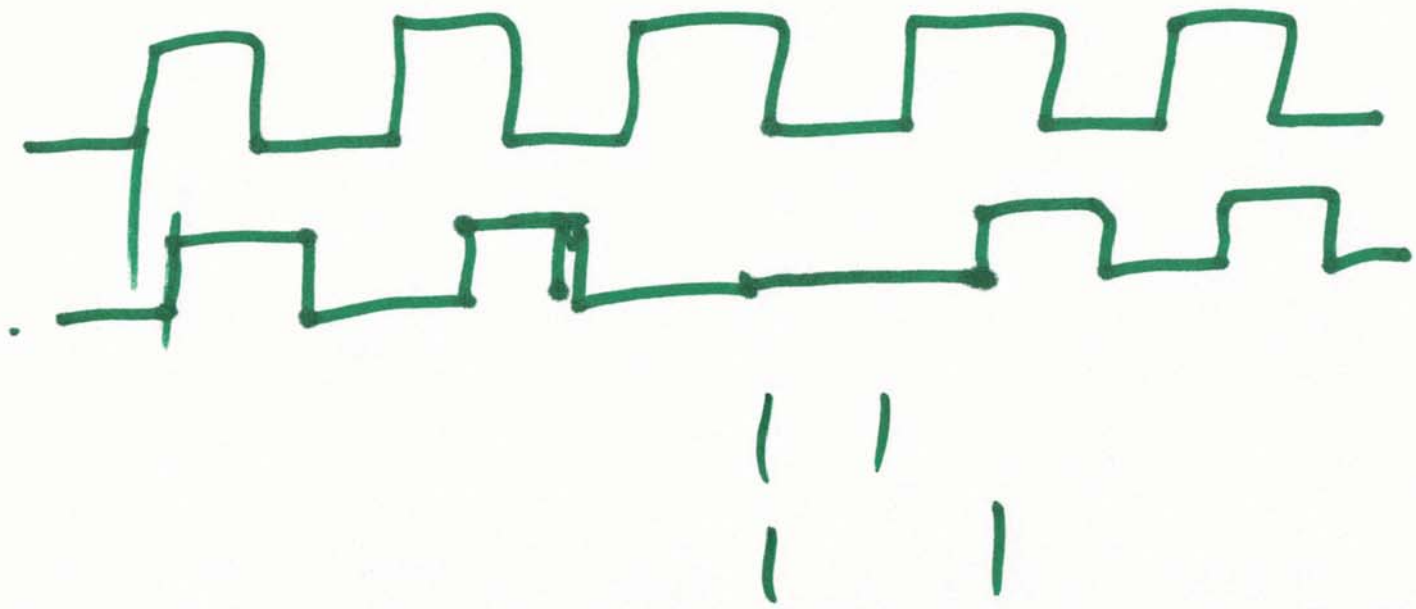


Figure 19.9 Average output voltage of phase detector during acquisition.



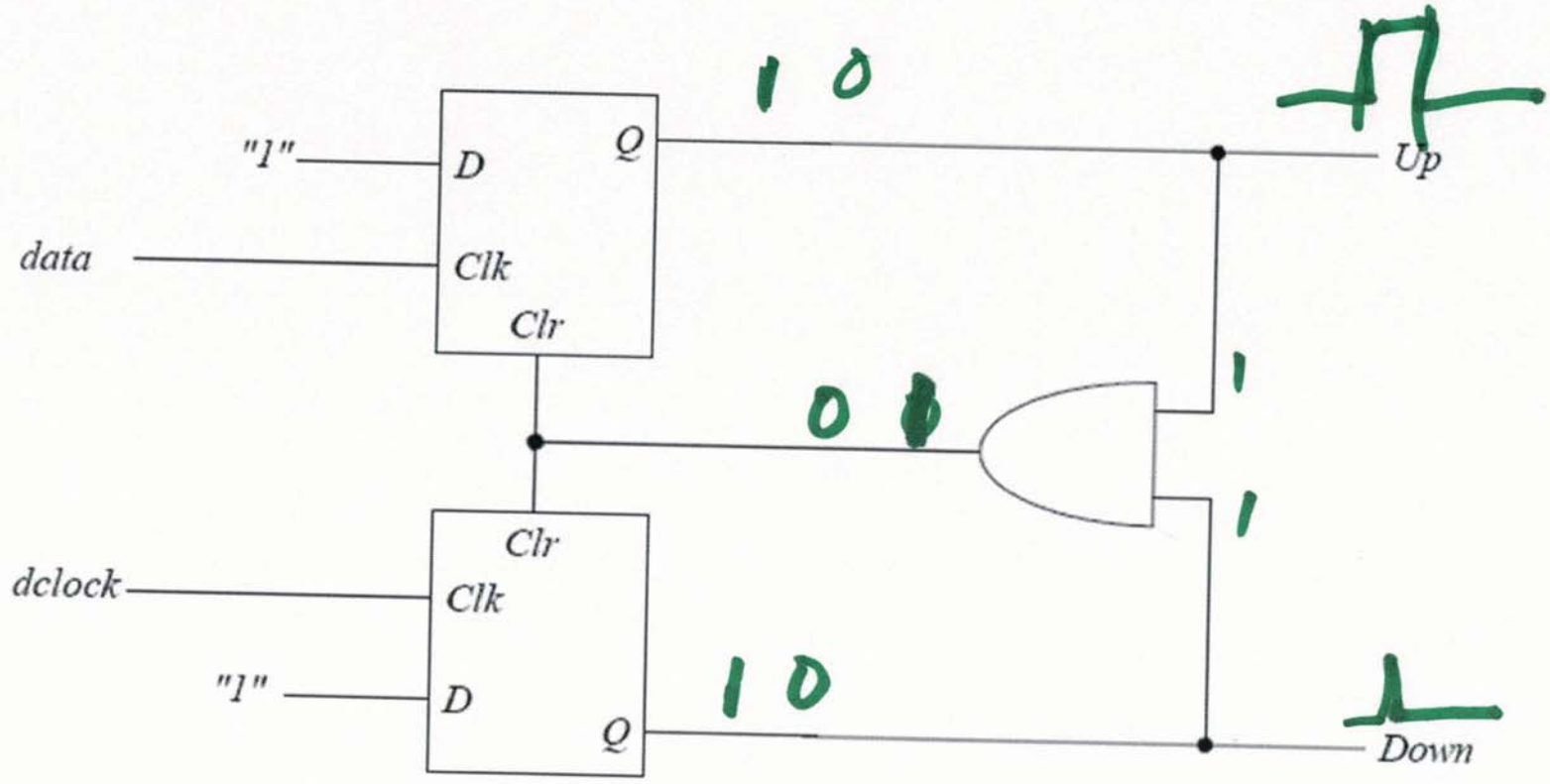
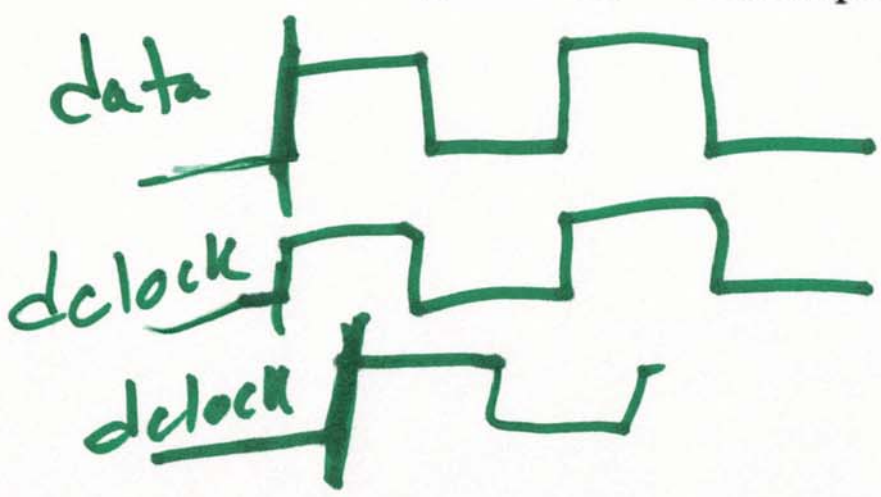
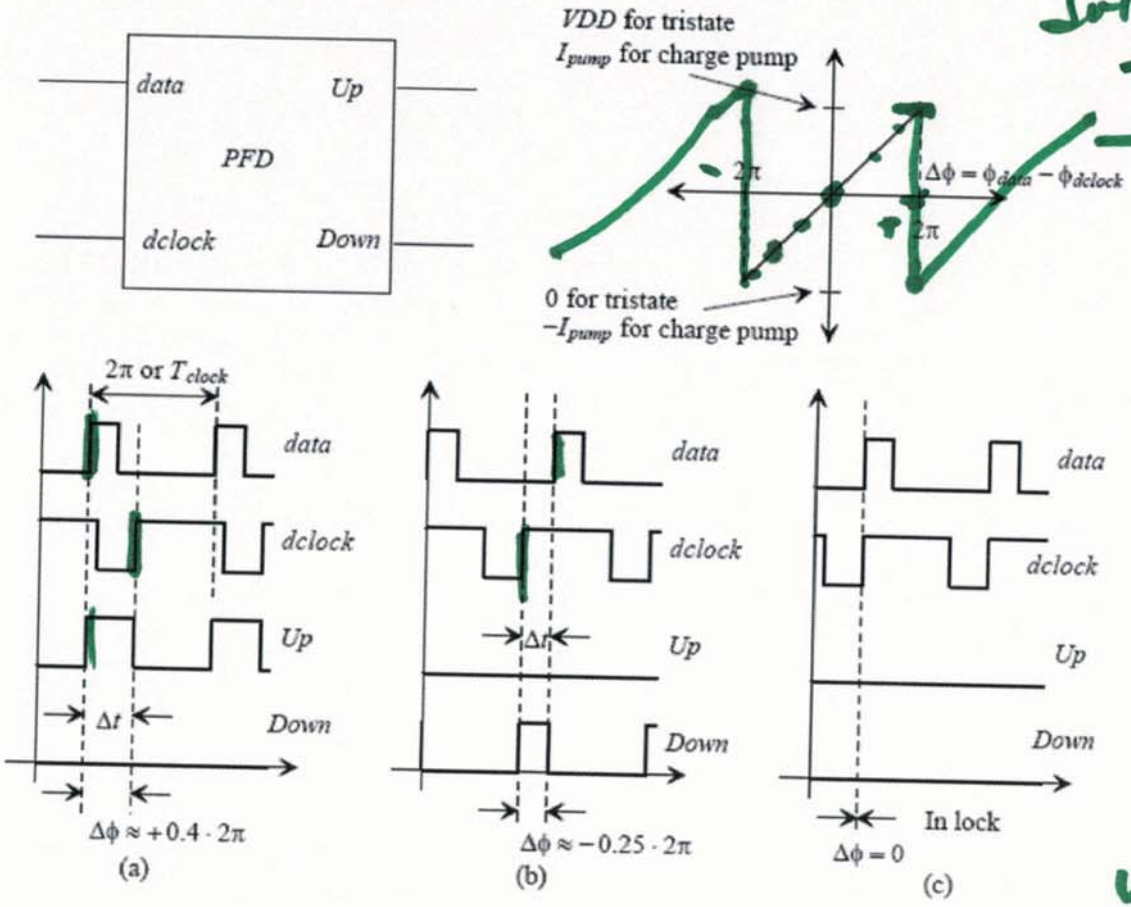


Figure 19.10 Phase frequency detector (PFD).



11)



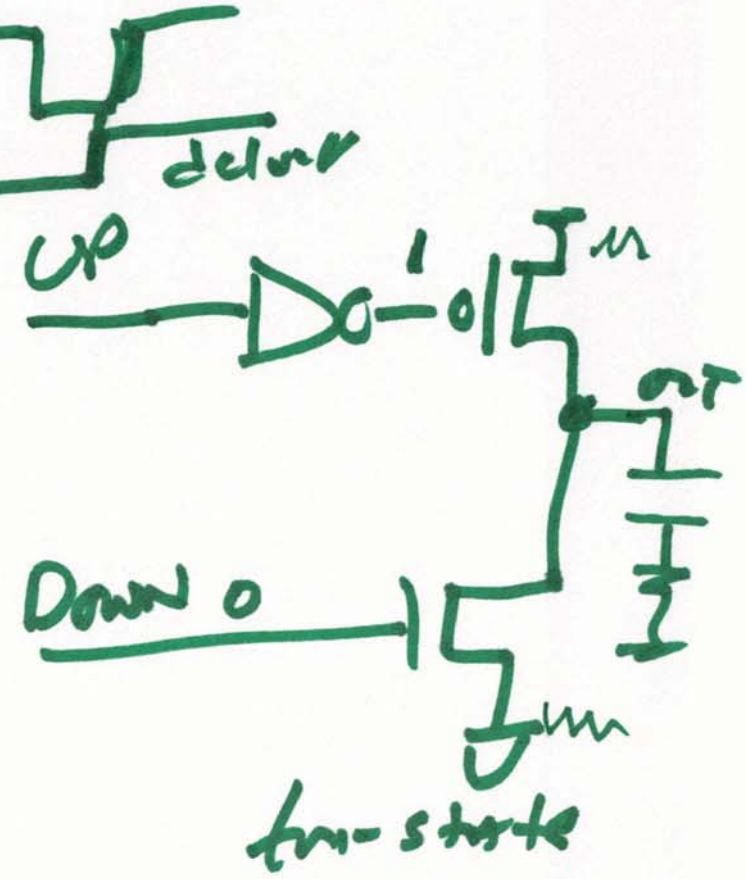
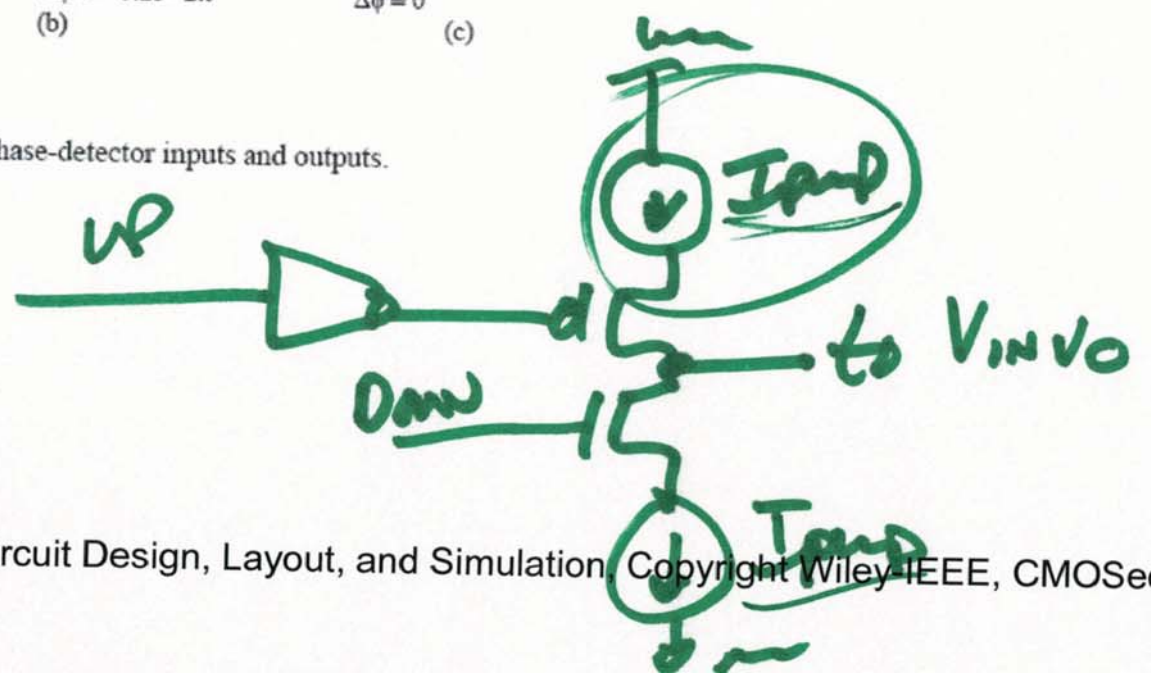


Figure 19.11 PFD phase-detector inputs and outputs.



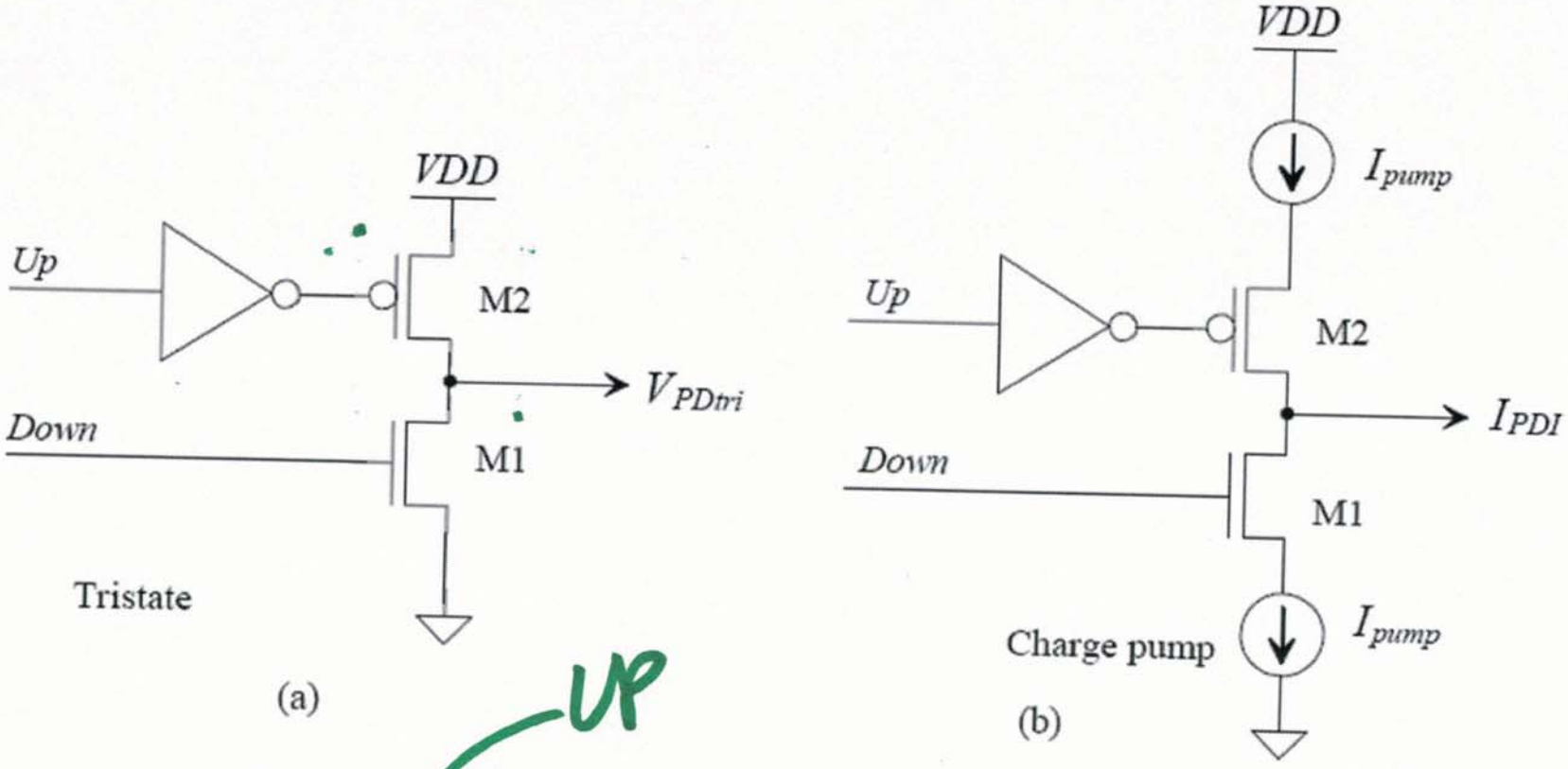
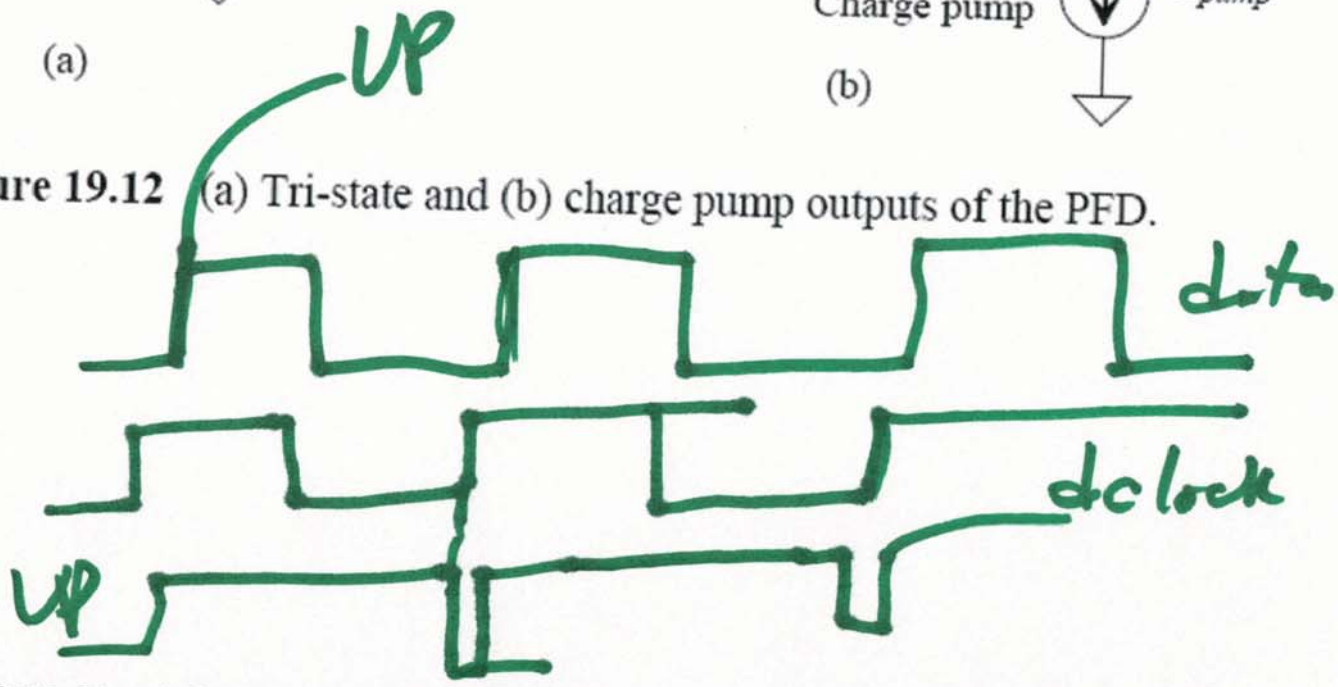


Figure 19.12 (a) Tri-state and (b) charge pump outputs of the PFD.



13)

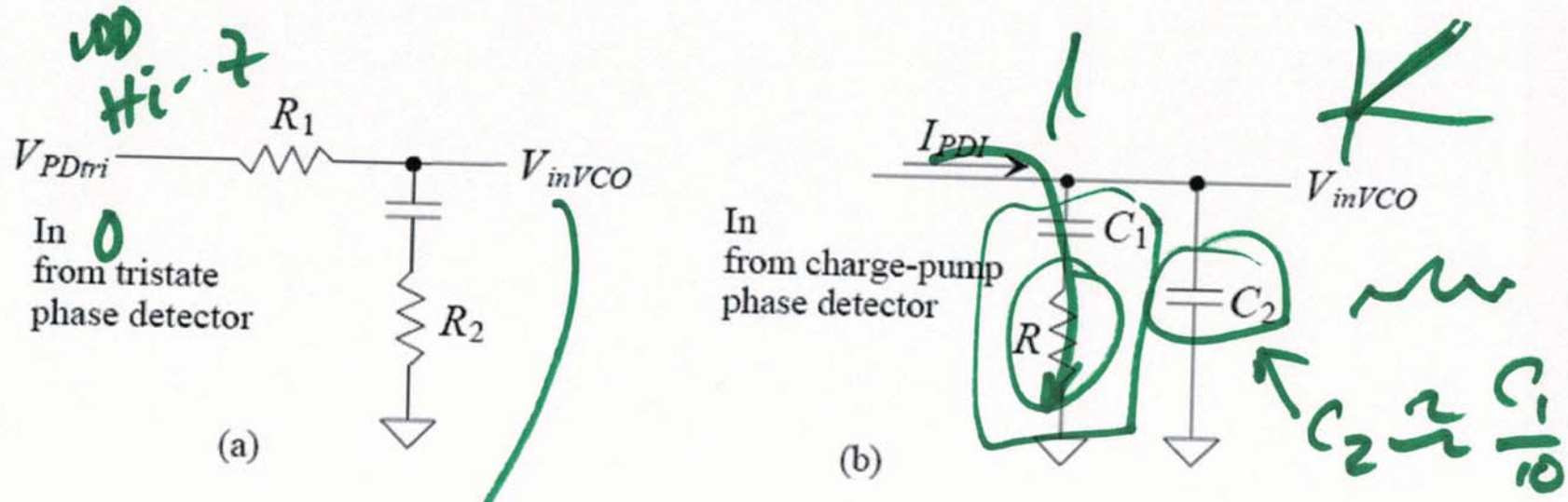
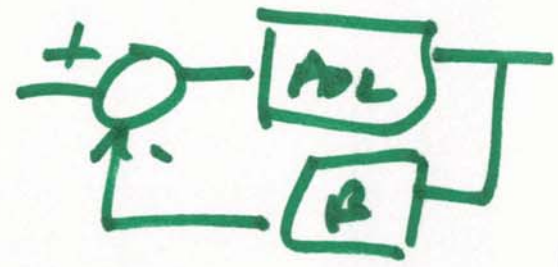


Figure 19.13 Loop filters for (a) tristate output and (b) charge-pump output.

$$\frac{V_{inVCO}}{V_{PDtri}} = K_F = \frac{R_2 + \frac{1}{j\omega C}}{R_1 + R_2 + \frac{1}{j\omega C}} = \frac{1 + j\omega C R_2}{1 + j\omega C (R_1 + R_2)}$$

K_{PD} K_{VCO} K_F $\beta = \frac{1}{N}$



K_{PFD}

$$\frac{V_{inVCO}}{I_{PDI}} = R + \frac{1}{j\omega C_1}$$

14)