EC6 721
MEMORY CIRCUIT
Sept. 28, 2015
17.2 SENSING RESISTIVE MEMORY
Resistive Memory

Programmable Contact RAM (PCRAM)

I

V

High resistance

Chalcogenide (metal)

Glass

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VDD / 2 → VDD (program) 0 (erasins)

BL proj.

10K

VDD + 50mV - VDD / 2

ERASED → 100K

5mA

VDD + Vos

PCRAM

WL

ITIC

ITIR

VDD / 2

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Crystalline - lower R (PCRAM - Phase Change RAM)
Amorphous - higher R
Resistor memory
Memristors
Comparator inputs for ΔE they are basically the same voltage
\[ \frac{V_{OS}}{R_{bit}} = \frac{I_{REF} \cdot m}{N} \]

\[ R_{bit} = \frac{V_{OS}}{I_{REF} \cdot \frac{m}{N}} \]

The diagram shows a circuit with labels and equations related to biasing and offset. The text notes:

- \( V_{OS} \) with offset from \( V_{DD} \)
- \( N = \# \) of clocks
- \( m = \# \) of times \( \text{OUT} \) goes high
$V_{os} = \frac{V_{DD} - V_{os}}{2} \cdot \frac{M}{2}$

$\frac{V_{os}}{R_{bit}} = \frac{V_{DD} - V_{os}}{R_{ref}}$

$R_{bit} = \frac{N}{M} \cdot V_{os} \cdot \frac{R_{ref}}{\frac{V_{DD}}{2} - V_{os}}$

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