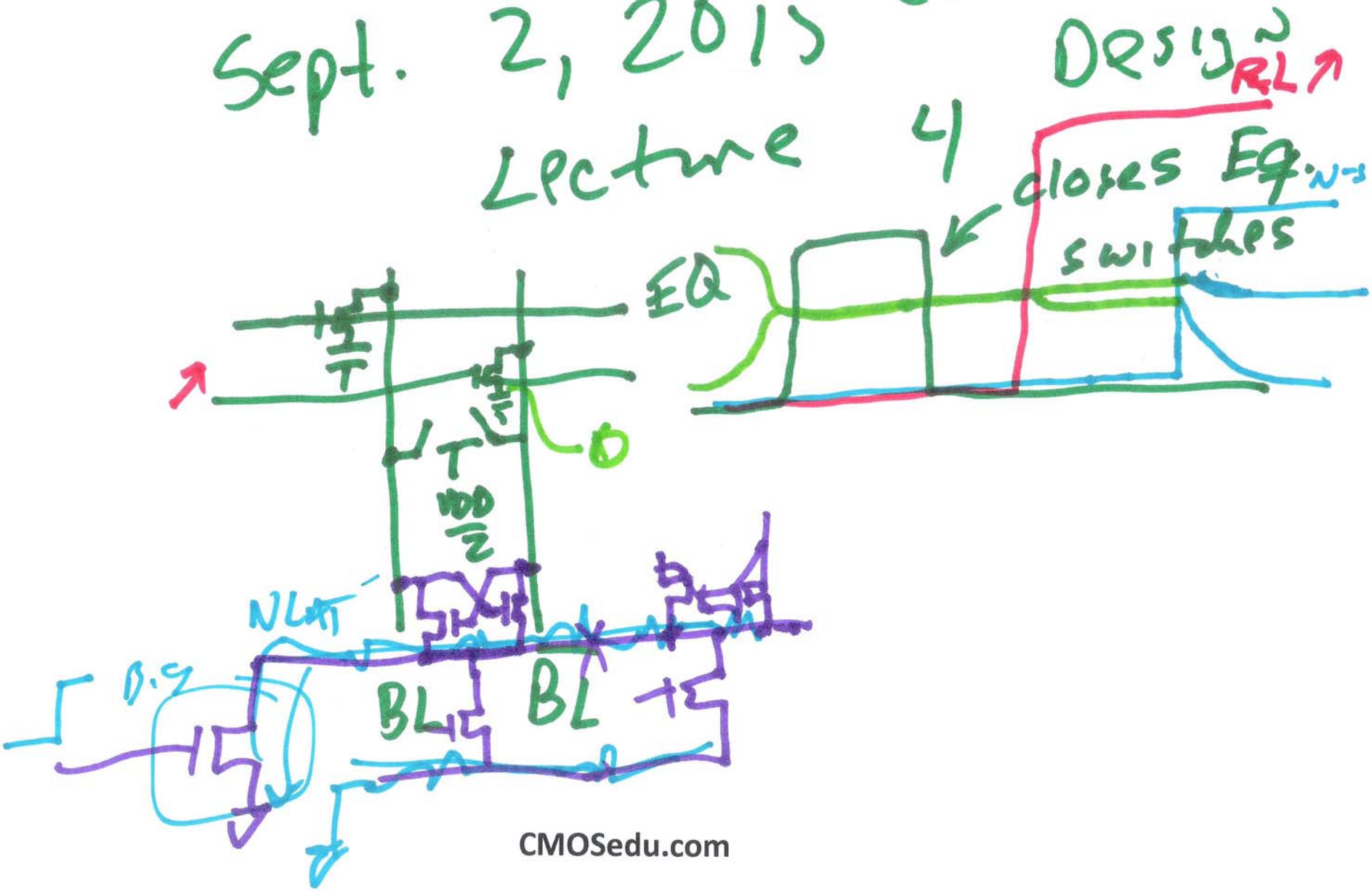
ECG 721 MEMORY CIRCUIT DESIGN

Sept. 2, 2015

Lecture 4



1)

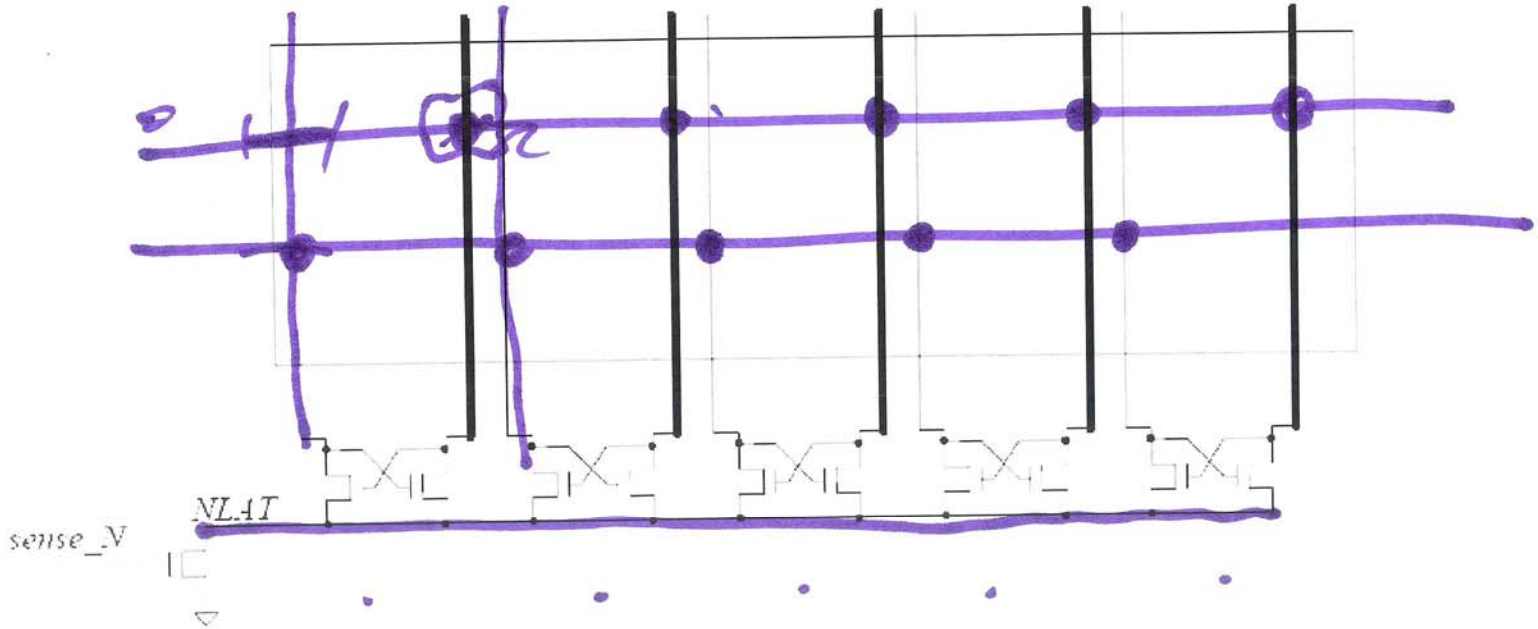


Figure 16.16 The folded array is formed by taking the open array architecture (open book) topology seen in Fig. 16.6 and "closing the book," that is, folding array 1 on top of array 0. Note that the bold lines indicate the bitlines from array 1 in the newly formed array.

2)

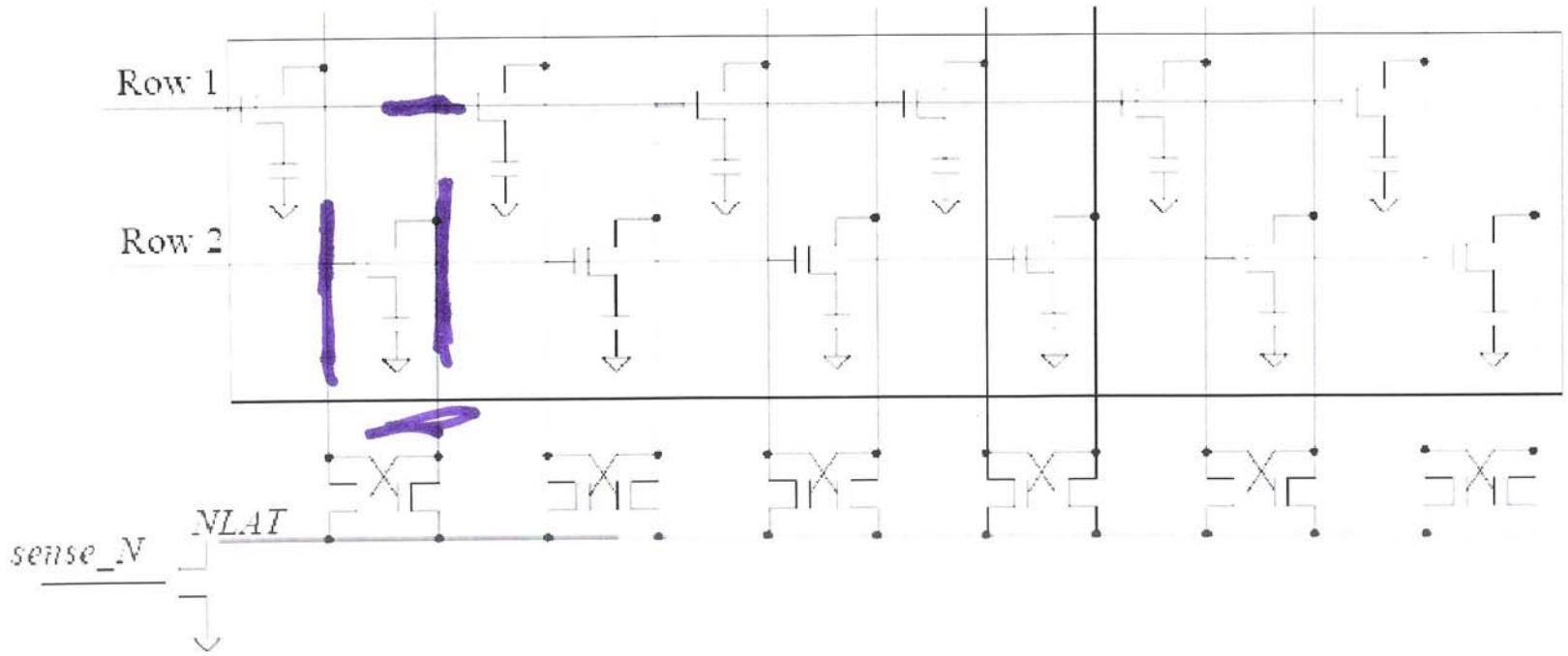
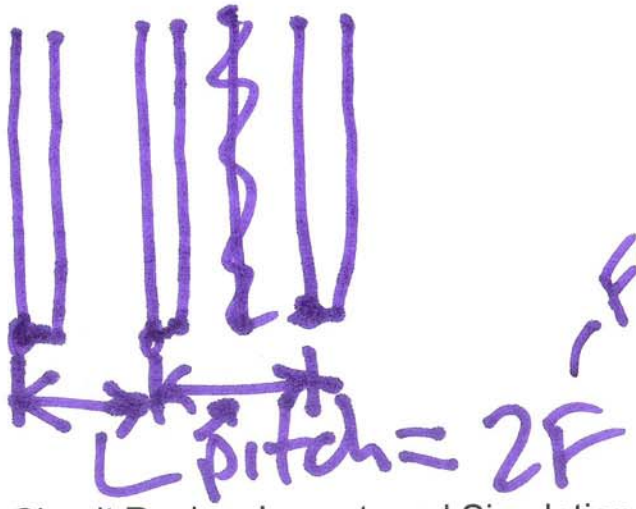


Figure 16.17 How a memory cell is located at every other intersection of a row line and a column line in a folded-area architecture.



ARRAY

MEMORY

FPGA

IMAGE SENSOR

DISPLAY

3)

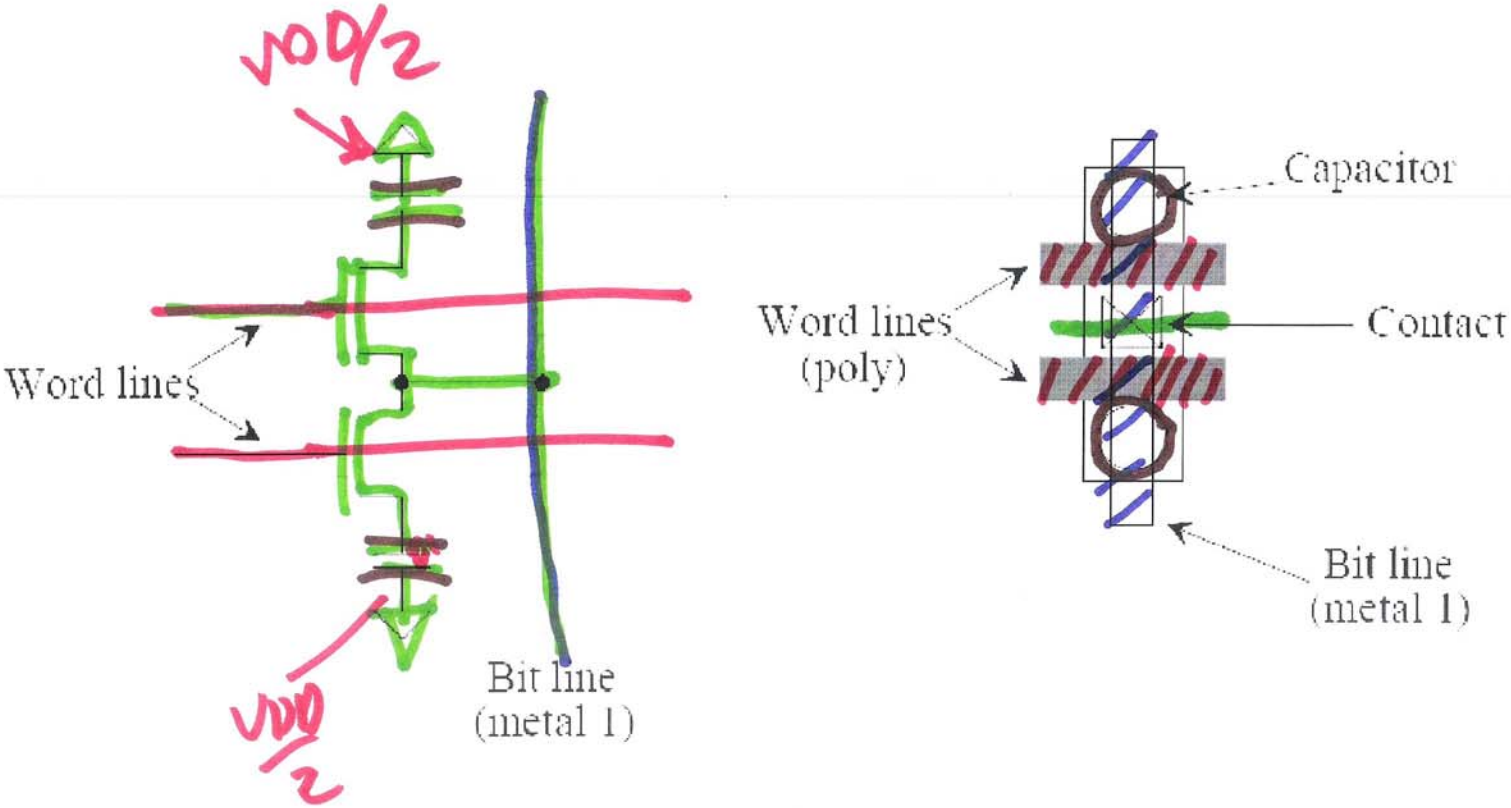
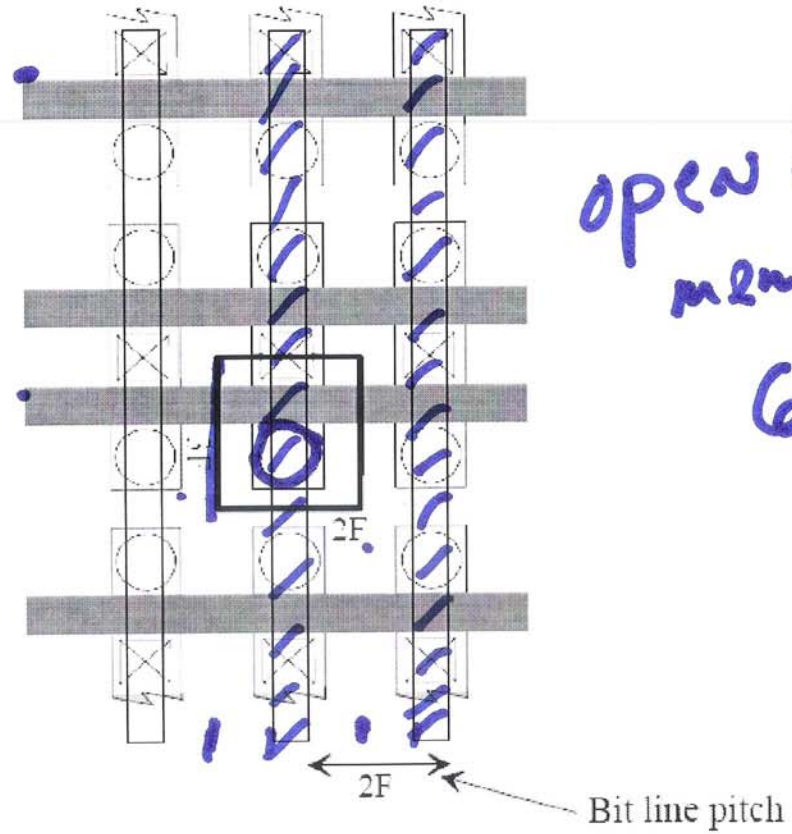


Figure 16.18 Two mbits sharing a contact to the bit line.

4)

F is feature size, which is half the bit line pitch; that is, F = pitch/2.



open bit line memory cell
$6F^2$

Figure 16.19 Layout of mbit used in an open bit line configuration.

5)

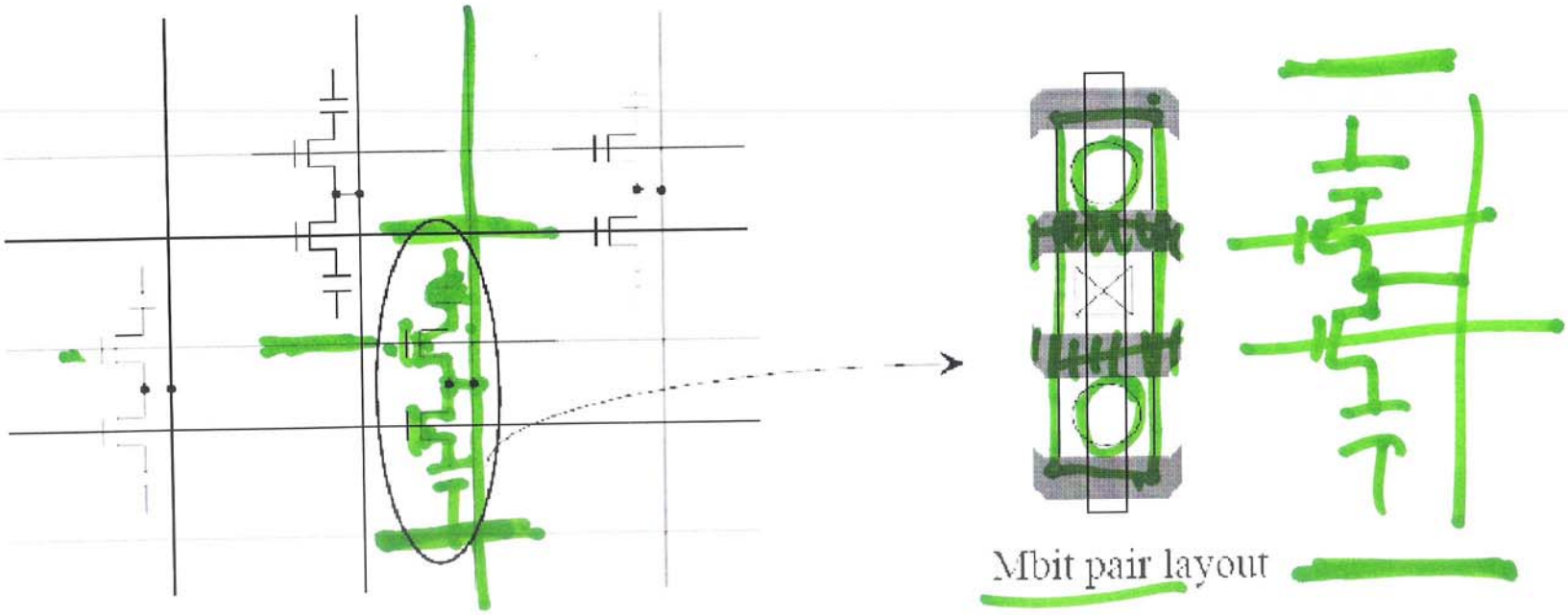


Figure 16.20 The mbit pair used for a folded architecture.

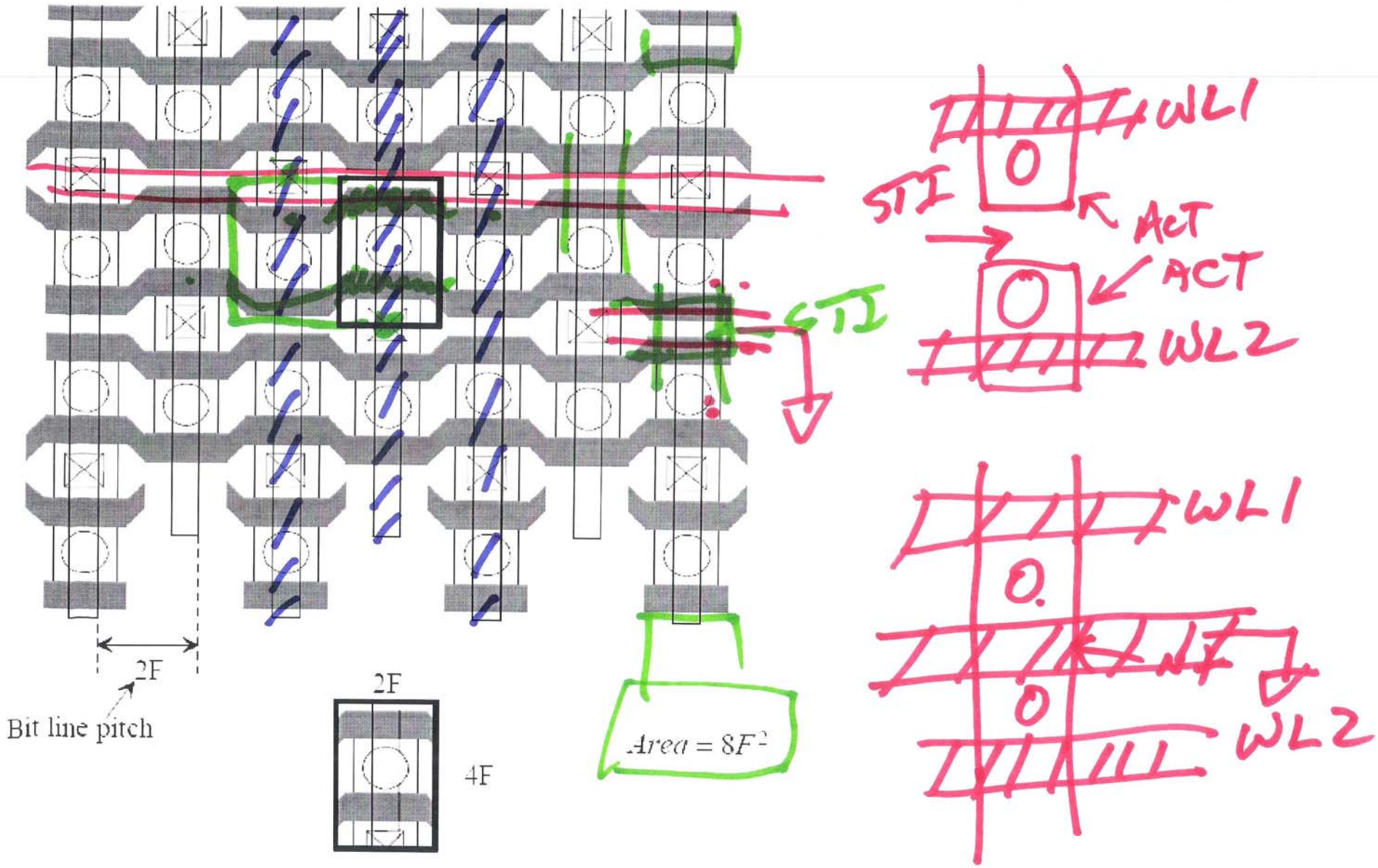
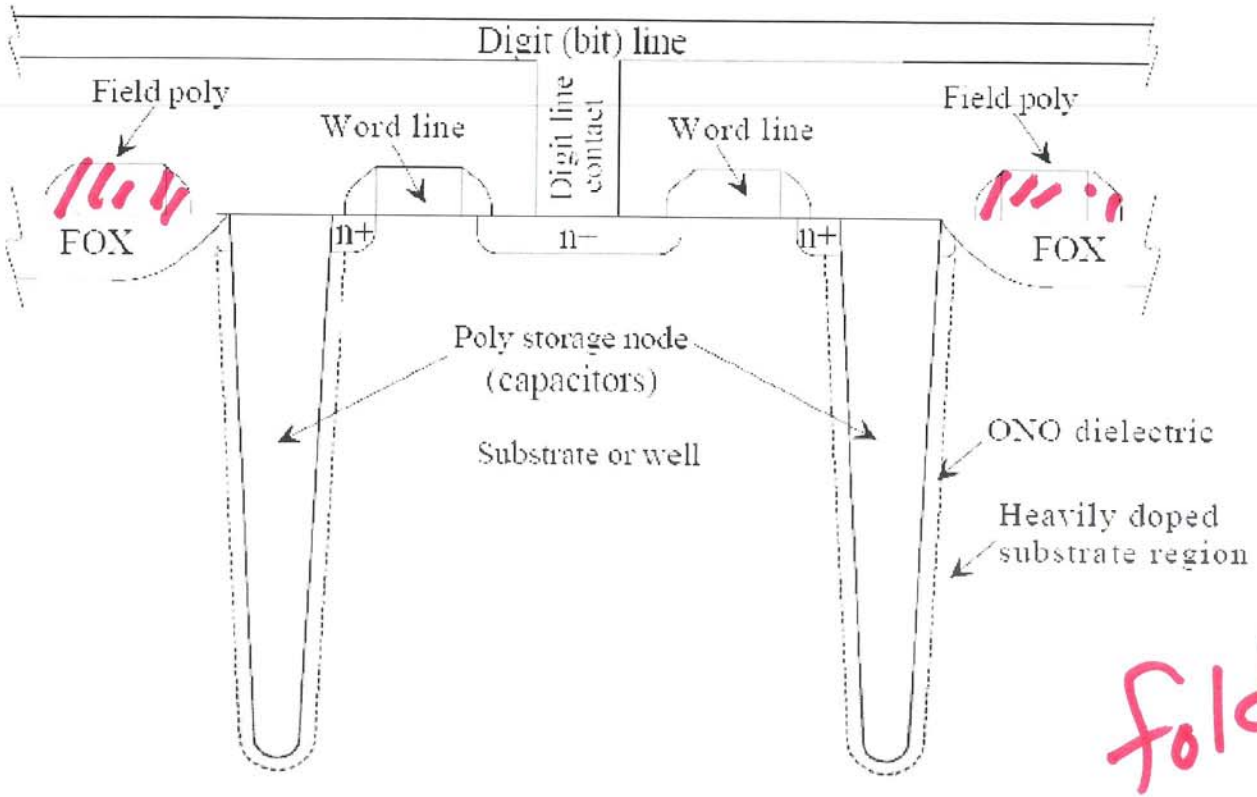


Figure 16.21 Folded architecture layout and cell size.

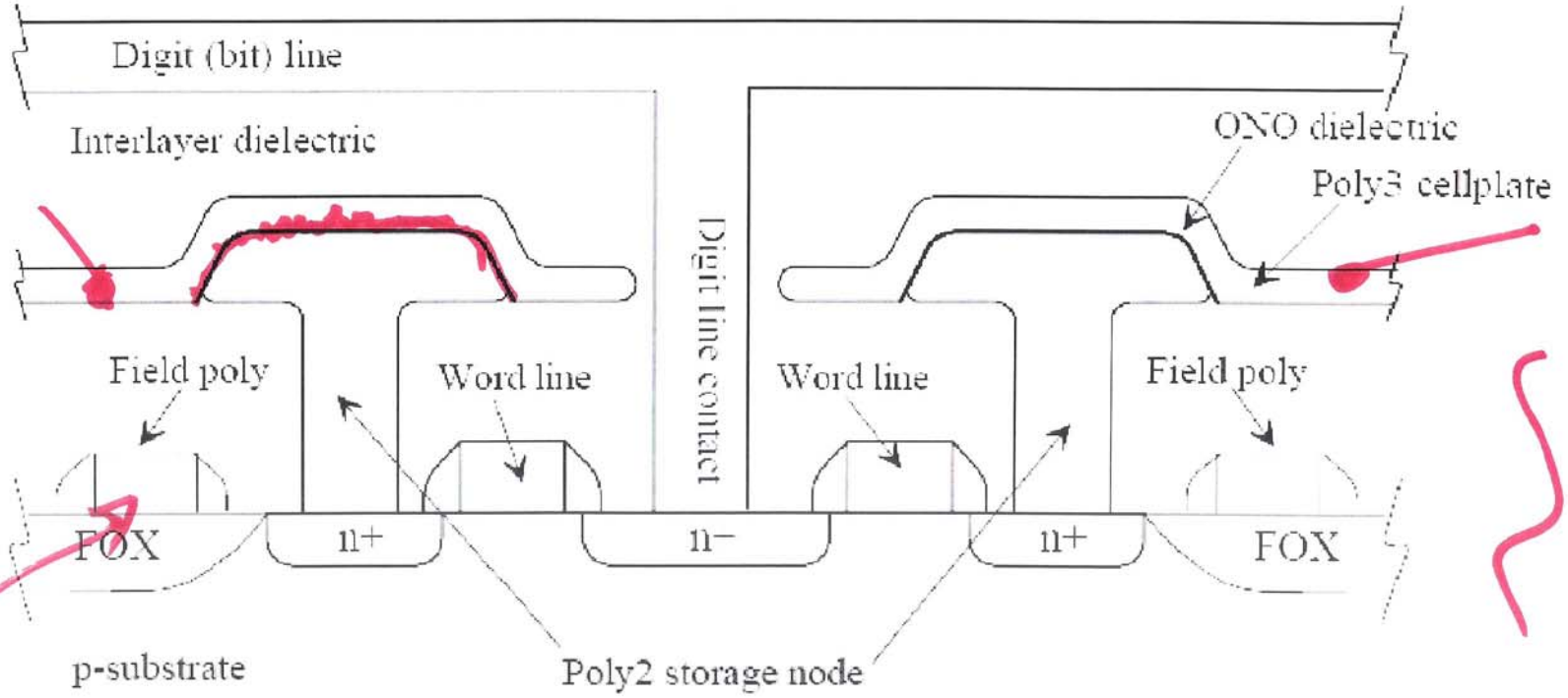
7)



folded

Figure 16.22 Cross-sectional view of a trench capacitor cell.

8)



VDD/2

folded

Figure 16.23 Cross-sectional view of a buried capacitor cell.

Cap under b.t line

COB

a)

$Q = CV$

$$\left(V_{mbit} - \frac{VDD}{2}\right) C_{mbit} + V_{init} \cdot C_{COL} = \left(V_f - \frac{VDD}{2}\right) C_{mbit} + V_f \cdot C_{COL}$$

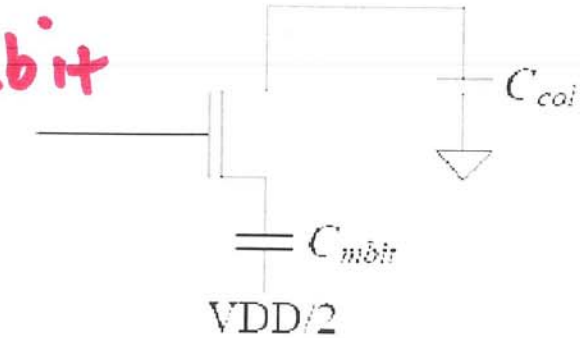
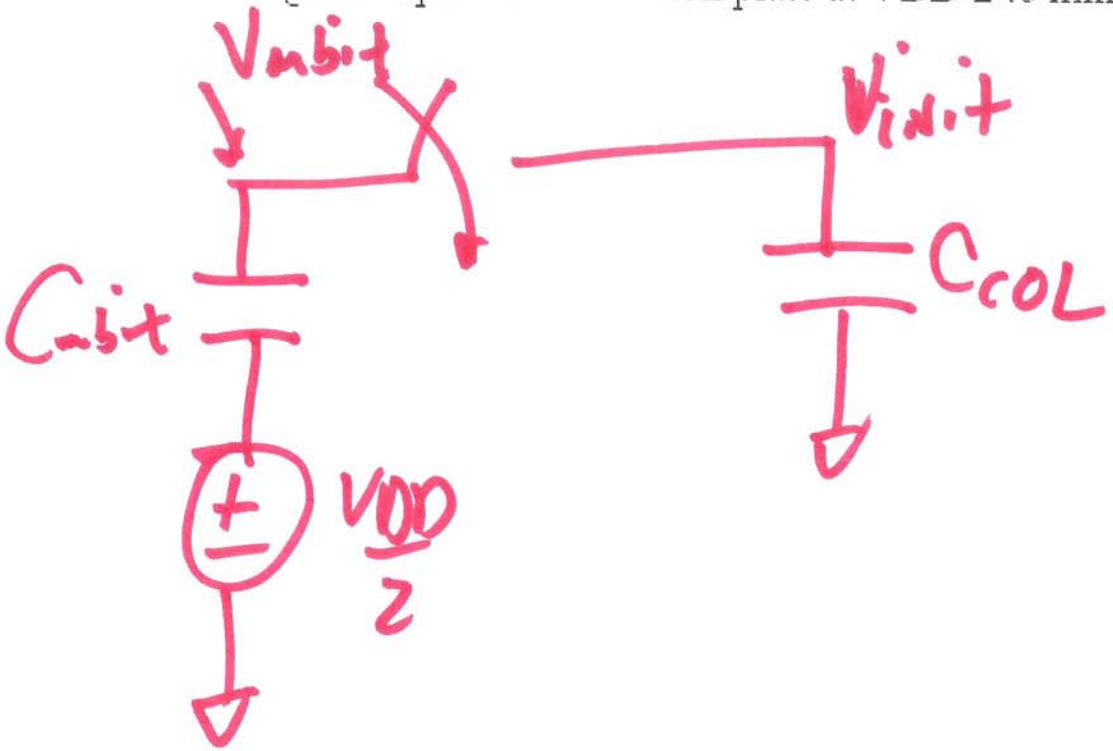
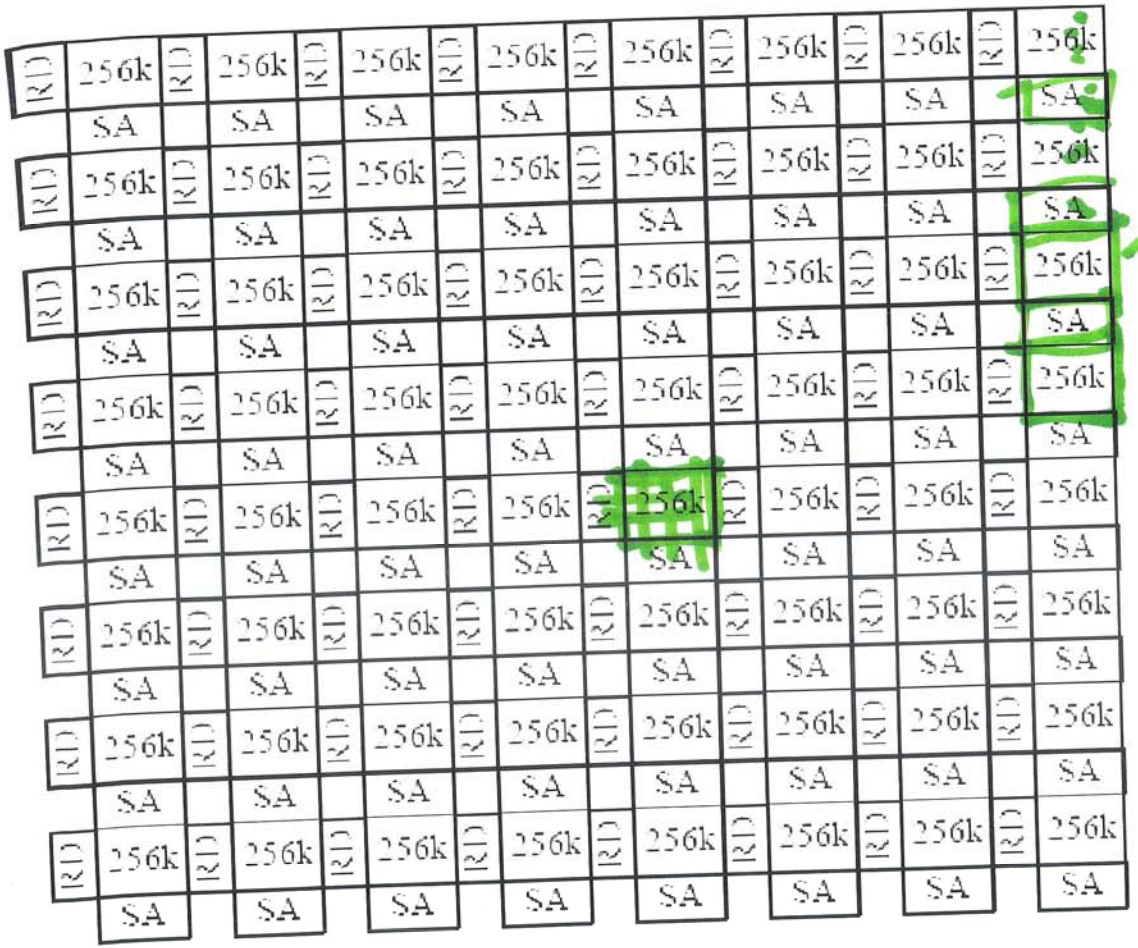
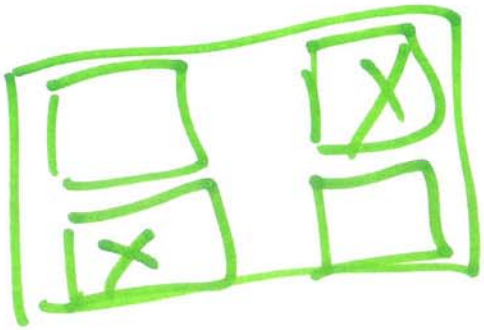


Figure 16.24 Holding the capacitor's common plate at VDD/2 to minimize oxide stress.





512 RLs (rows) X
512 BLs (cols)



RD Row decoder and driver circuitry

SA Sense amplifier and column decoder circuitry.

Figure 16.25 A 16-Mbit array block.