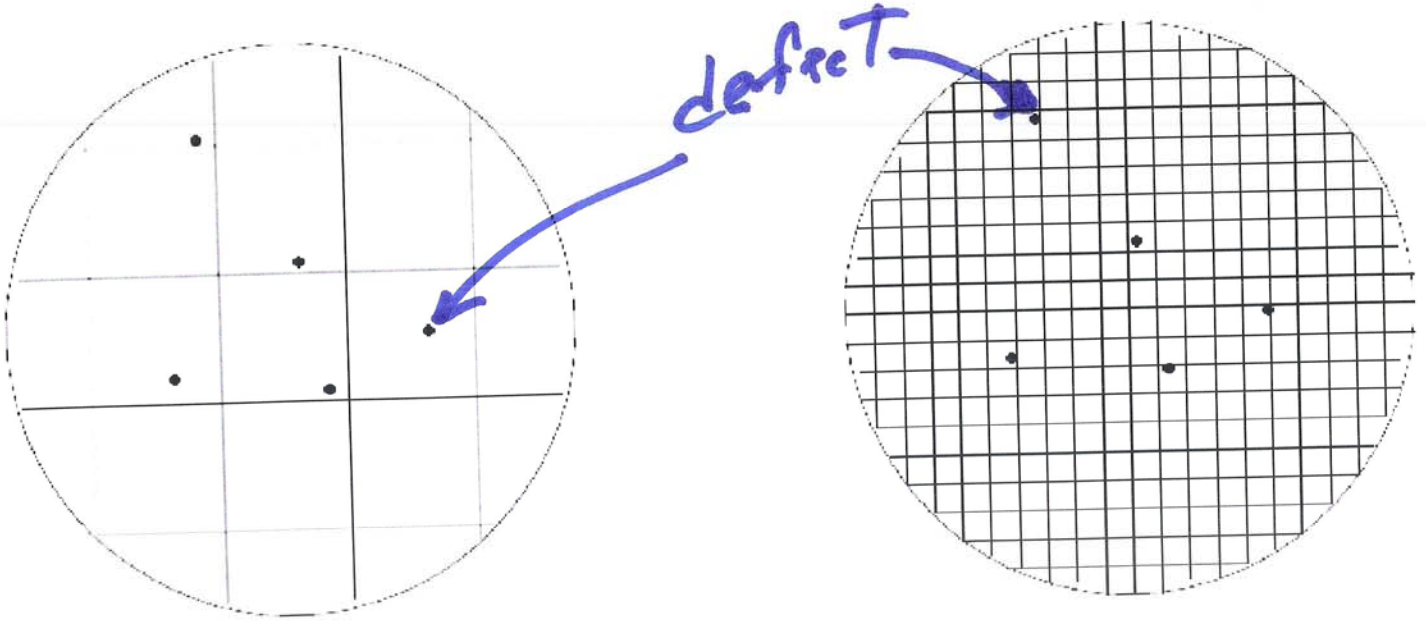


22:23

Figure 15.1 Defect density effects on yield.

1)

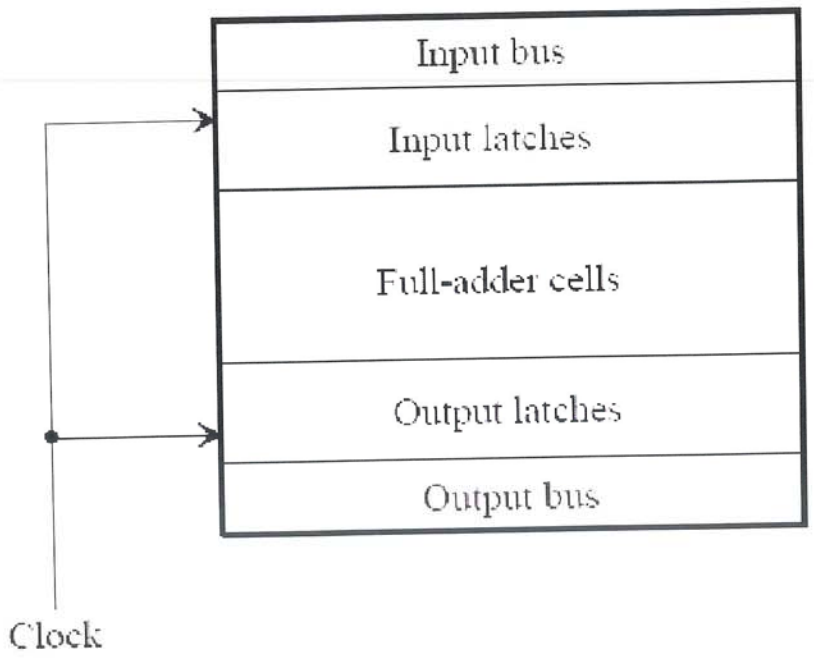


Figure 15.2 Floor plan for an adder.

2)

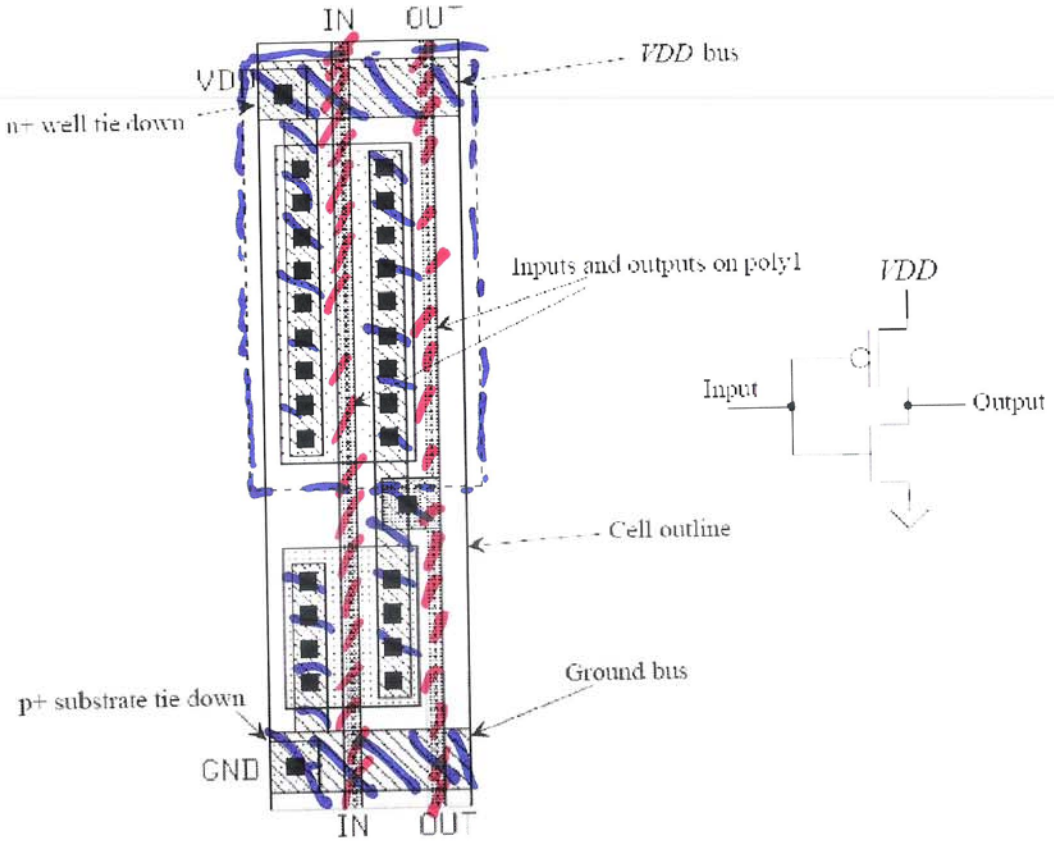
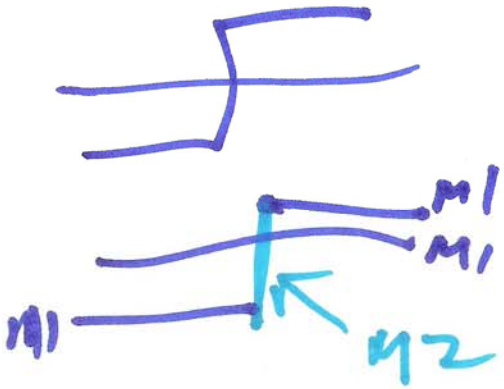


Figure 15.3 Standard cell layout of an inverter.



3)

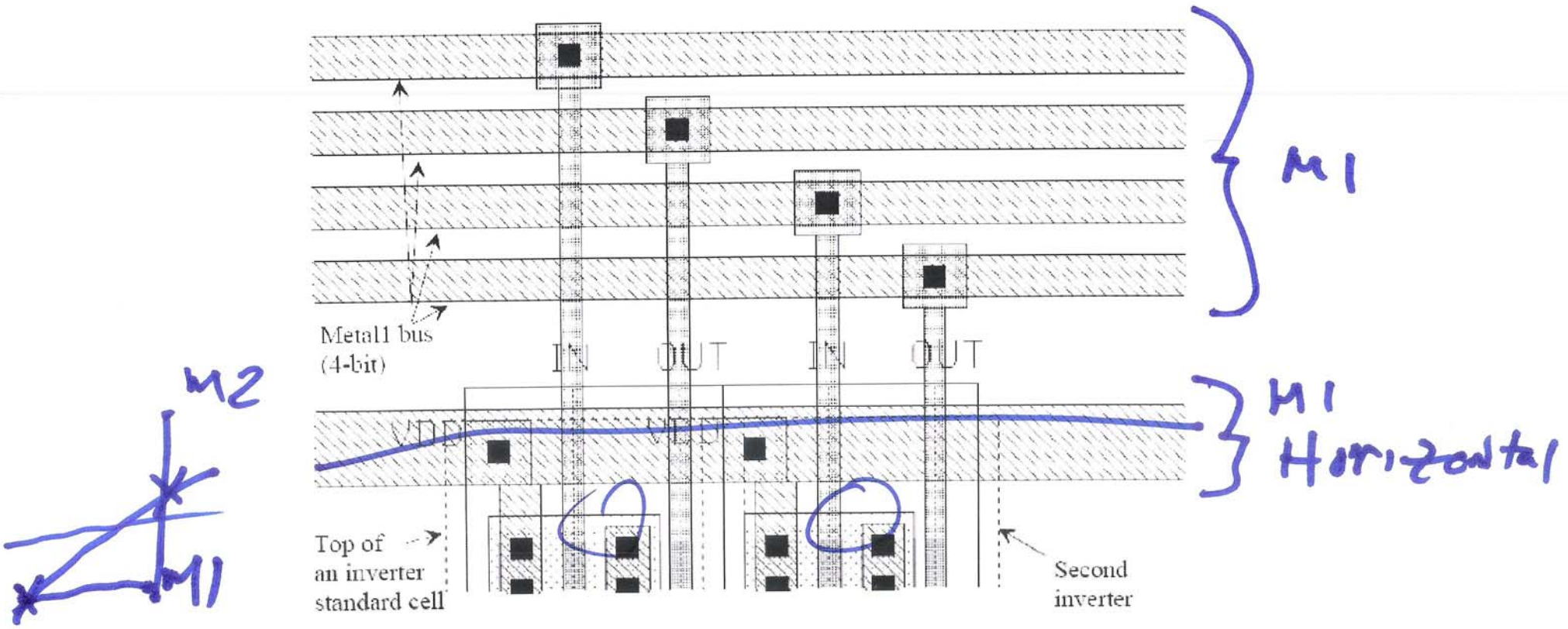


Figure 15.4 Connection of two inverter standard cells to a bus.

4)

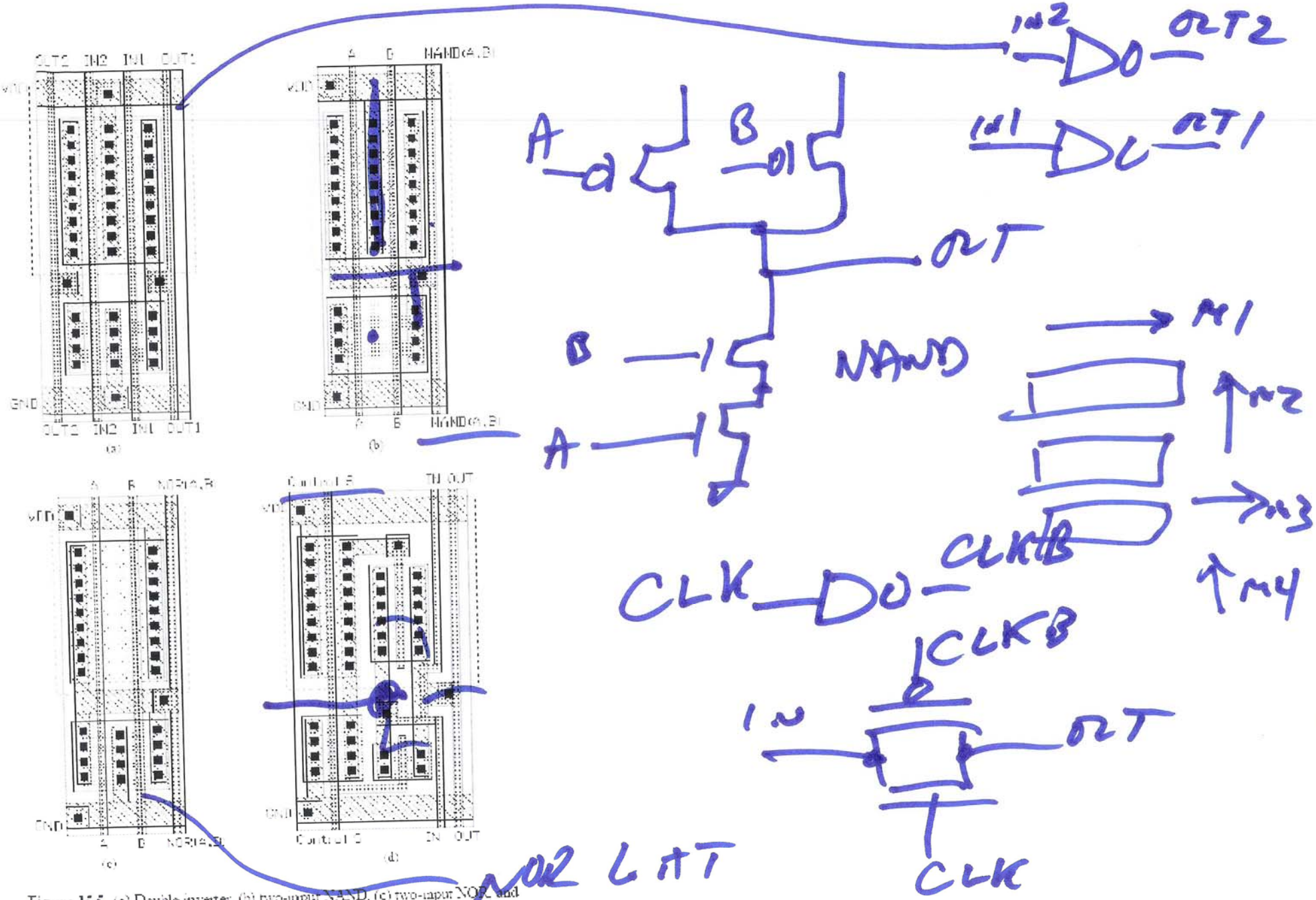


Figure 15.5 (a) Double inverter. (b) two-input NAND. (c) two-input NOR, and (d) transmission gate.

5)

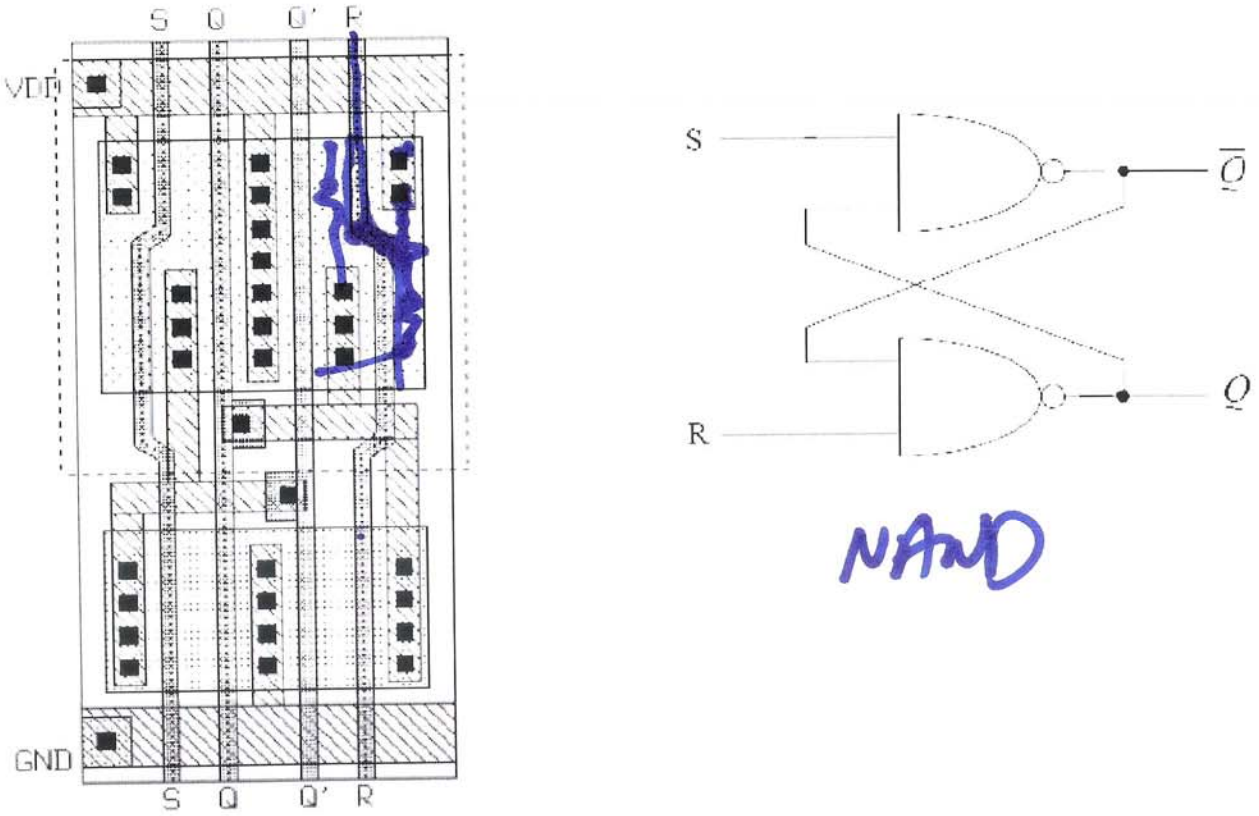


Figure 15.6 SR latch using NAND gates.

6)

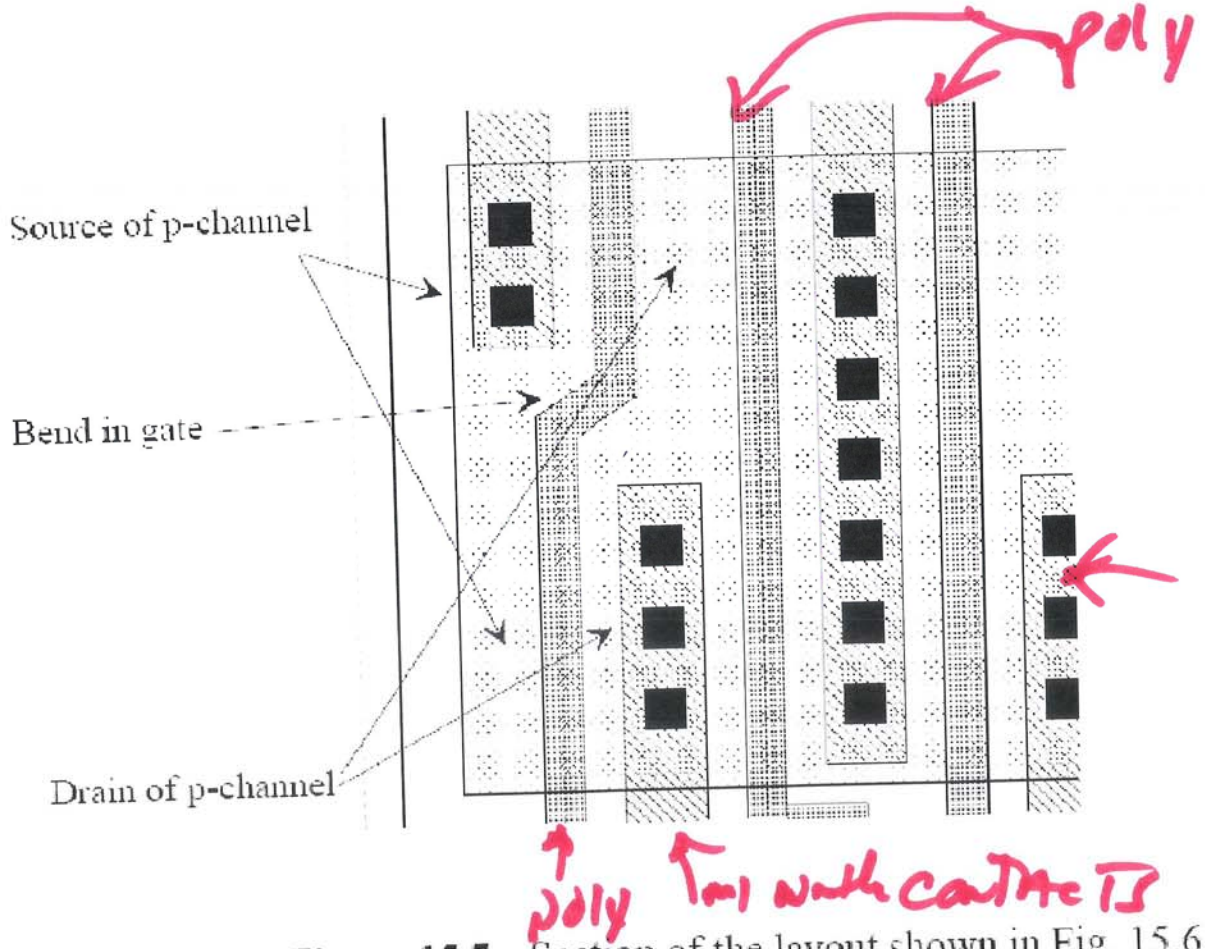


Figure 15.7 Section of the layout shown in Fig. 15.6.

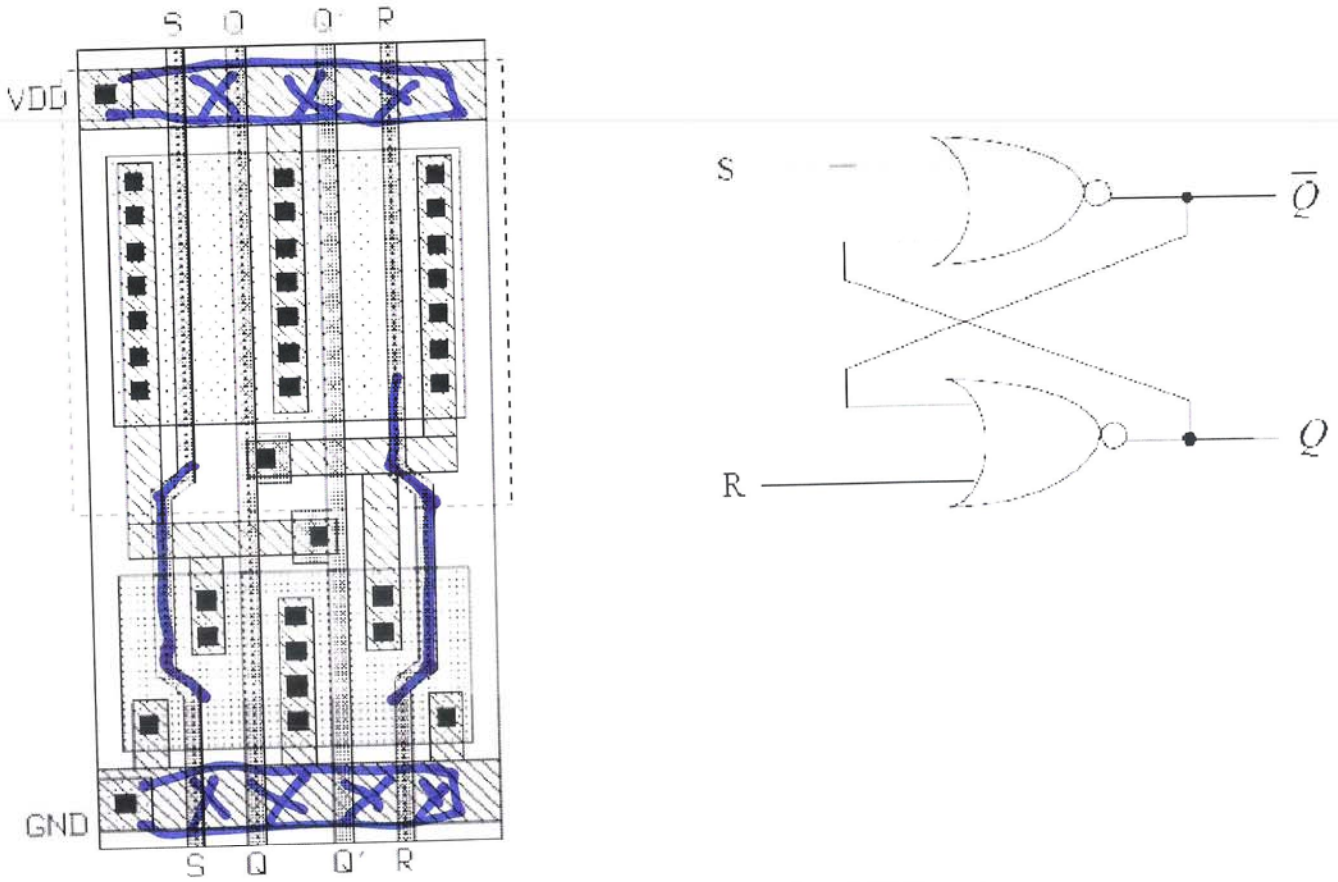
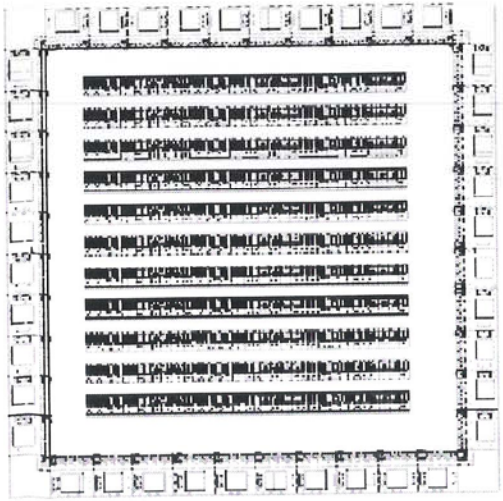
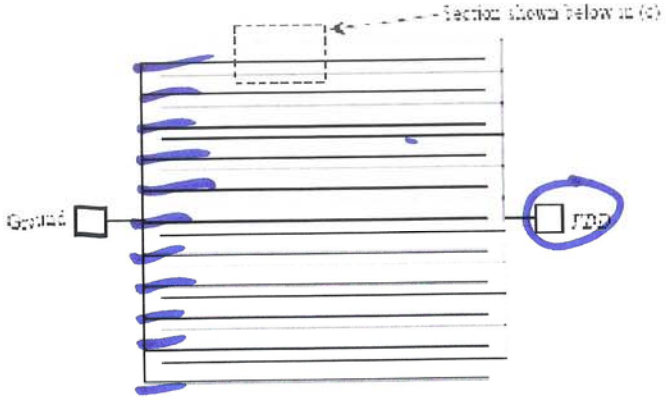


Figure 15.8 SR latch using NOR gates.

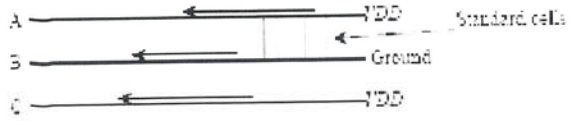
8)



(a)



(b)



(c)

Figure 16.9 Connection of power and ground to standard cells.

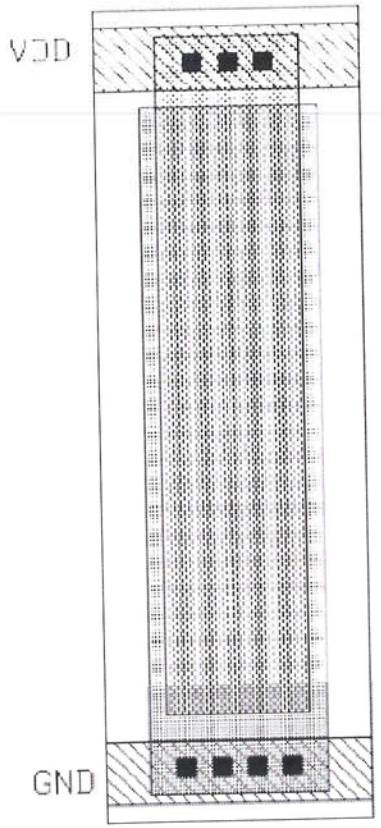


Figure 15.10 Decoupling capacitor.

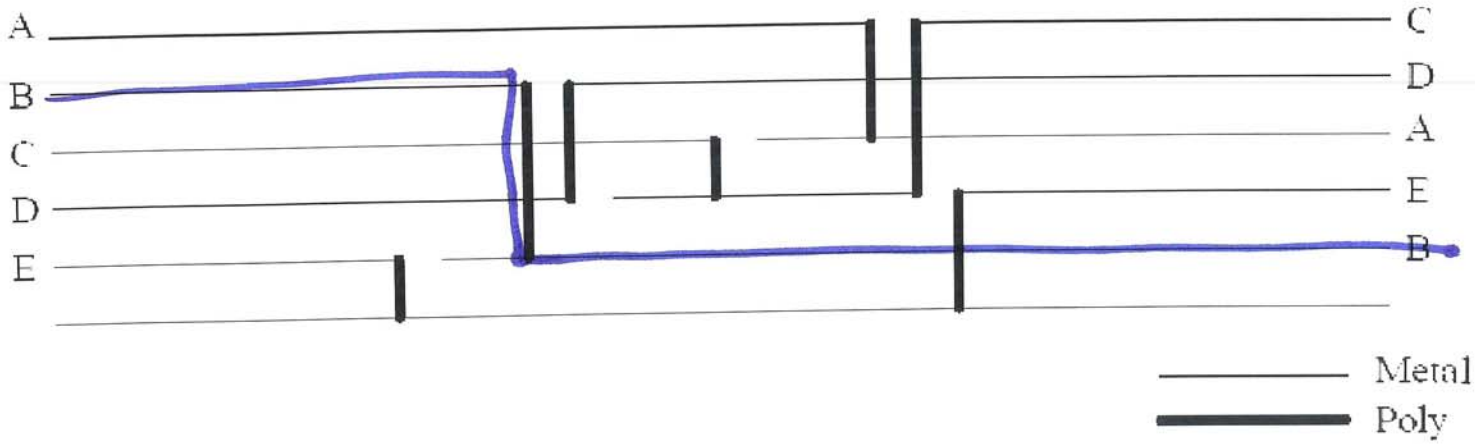
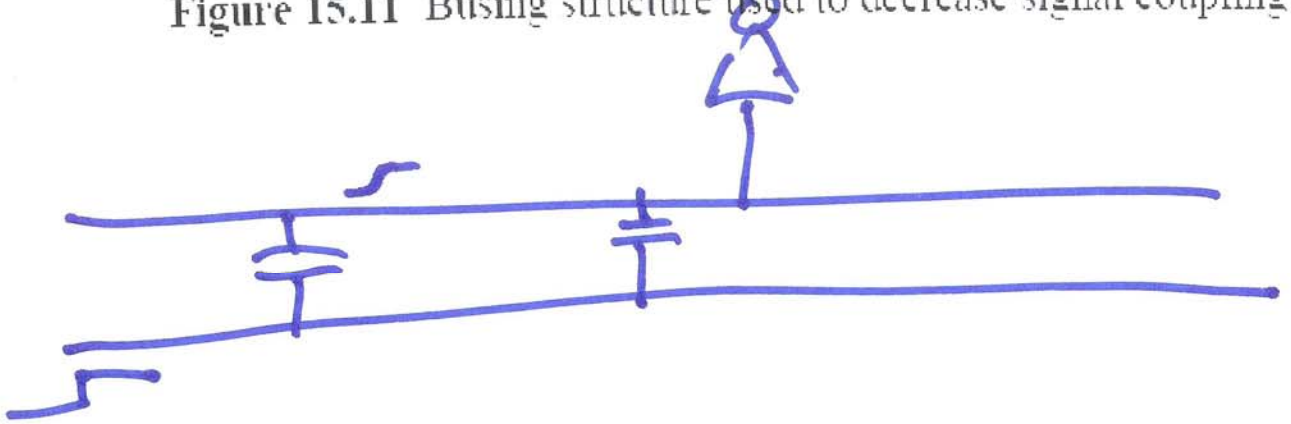
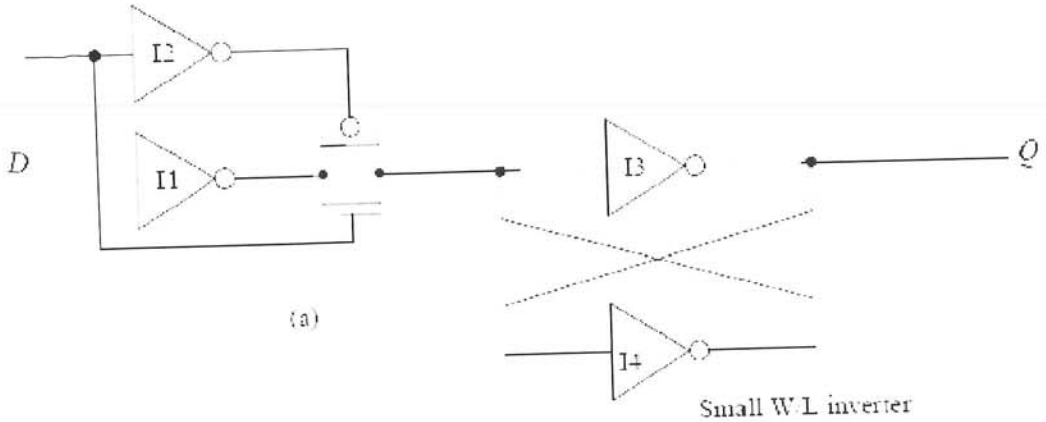


Figure 15.11 Busing structure used to decrease signal coupling.





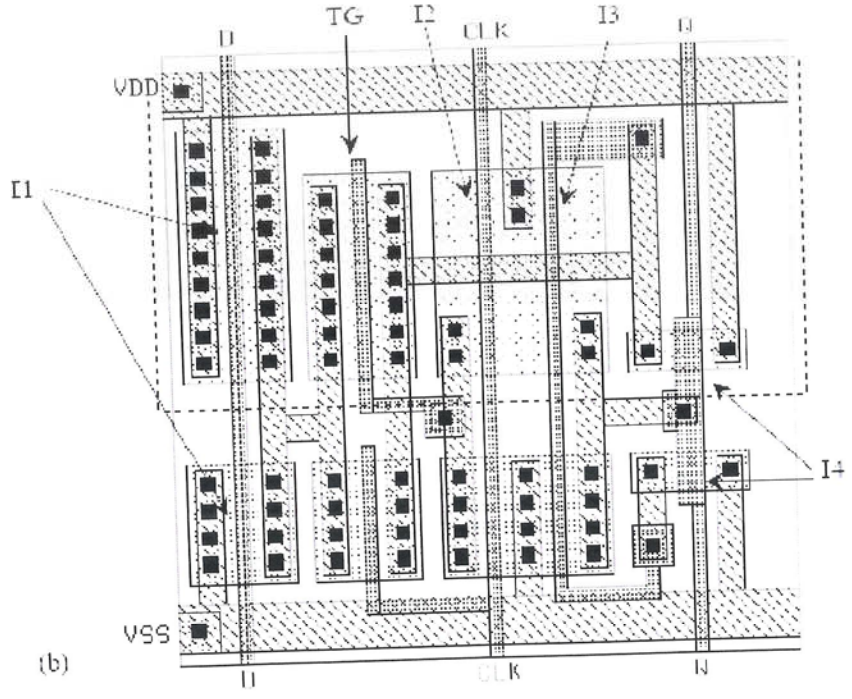


Figure 15.12 Schematic and layout of a latch.

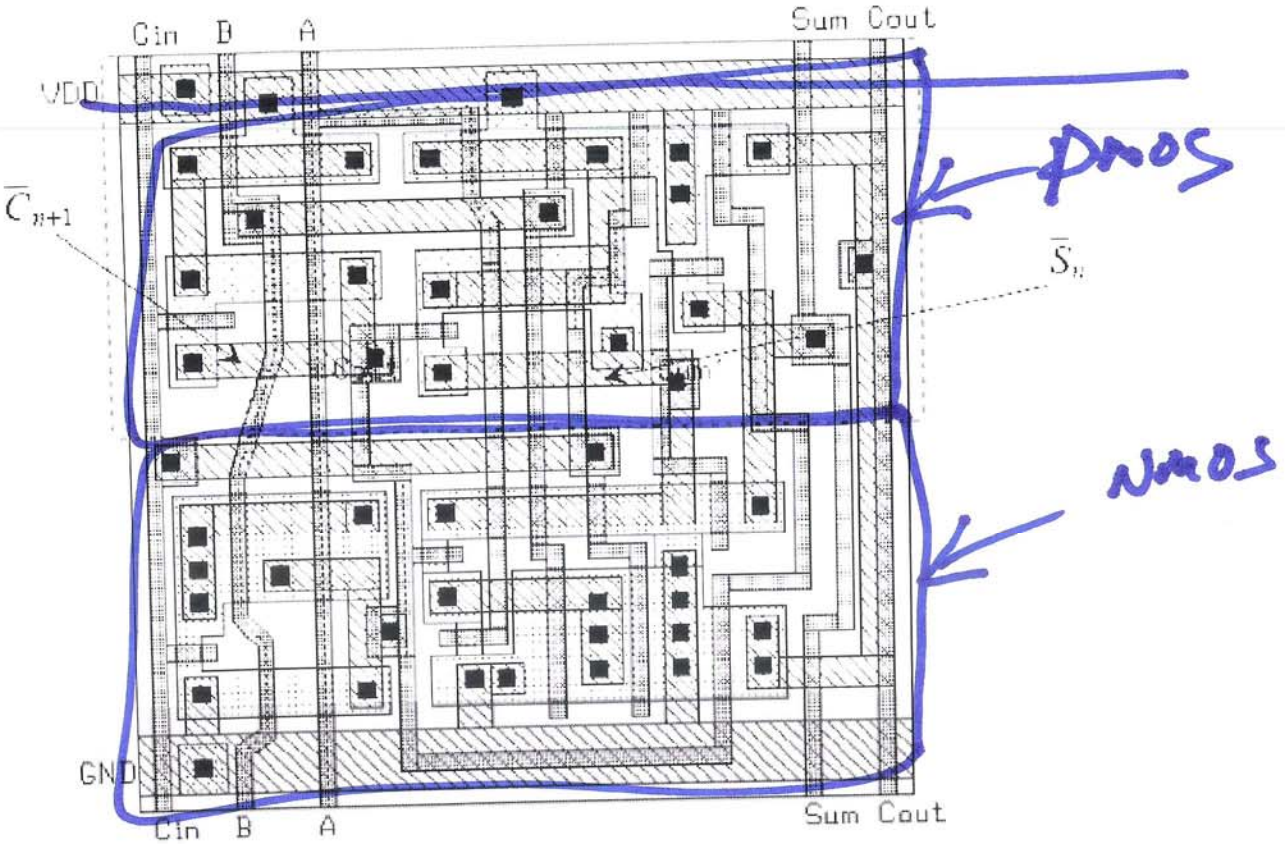


Figure 15.13 Layout of an AOI static adder.

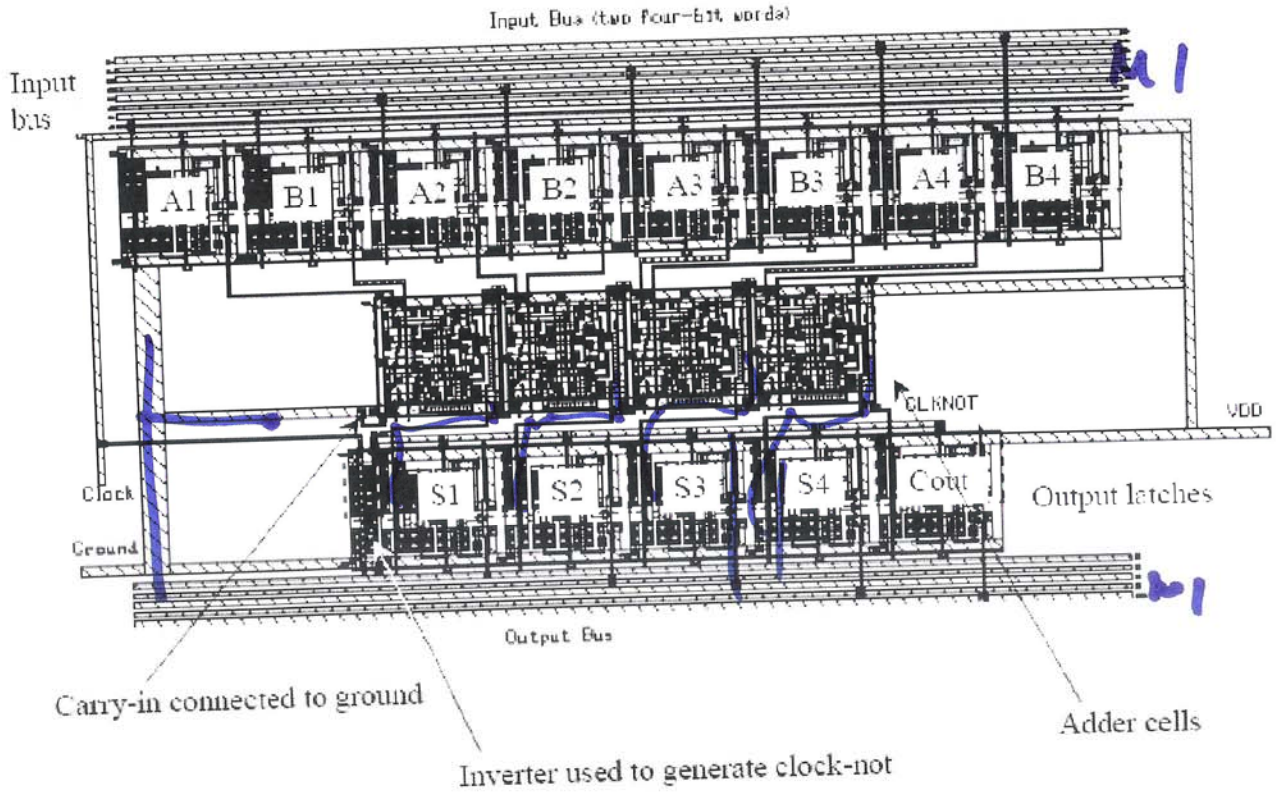


Figure 15.14 Layout of the complete adder.

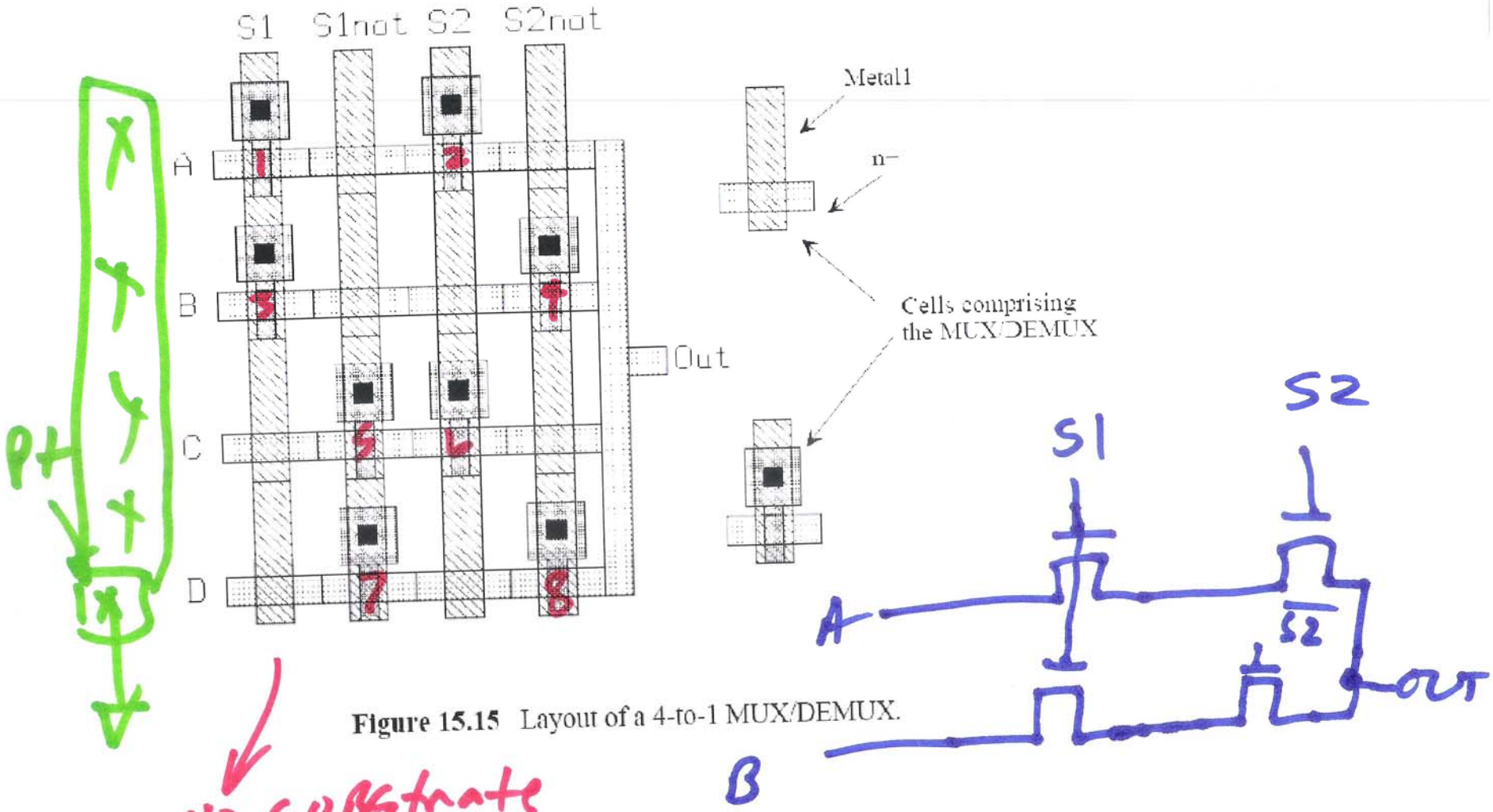


Figure 15.15 Layout of a 4-to-1 MUX/DEMUX.