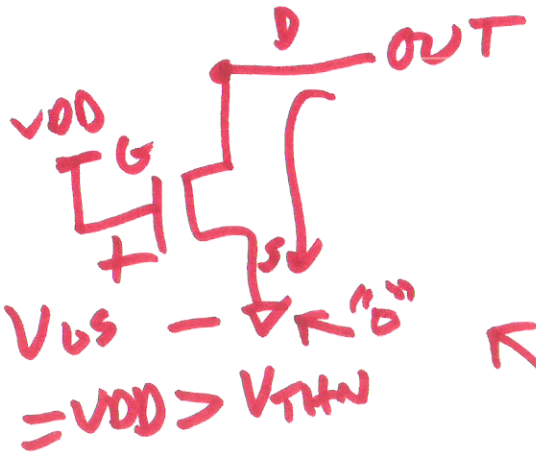
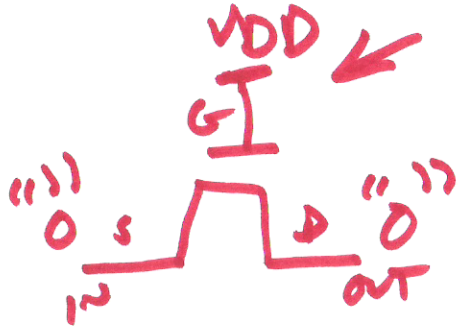
The Pass Gate



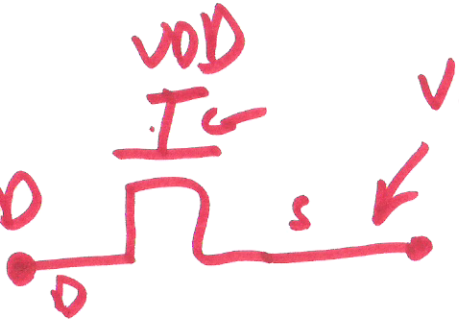


Gate at ground
Switch is
off

AT VDD
Switch is
ON

Equivalent

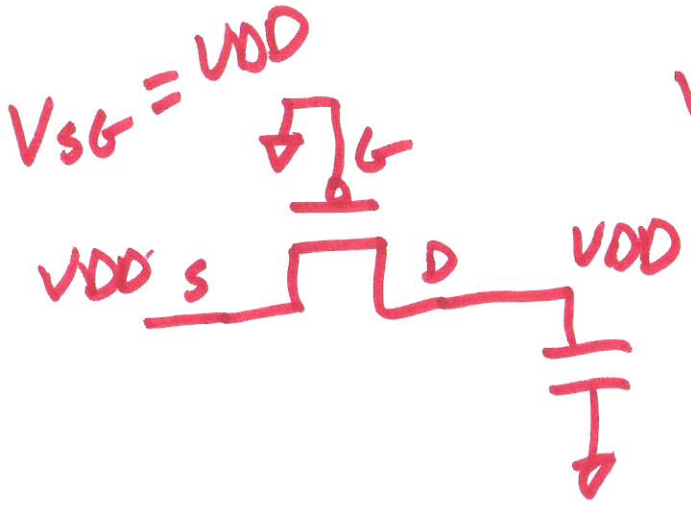
NMOS passes
a "0" well
but NOT a "1"



goes close to "1" VDD-V_{THN}

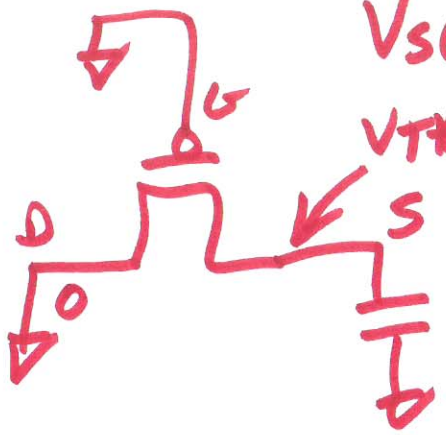
$$V_{GS} = V_G - V_S = VDD - (VDD - V_{THN}) = V_{THN}$$

V_G V_S



$V_{SG} > V_{THP}$

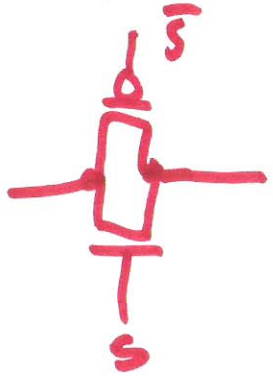
pmos passes a "1" well



$V_{SG} \geq V_{THP}$

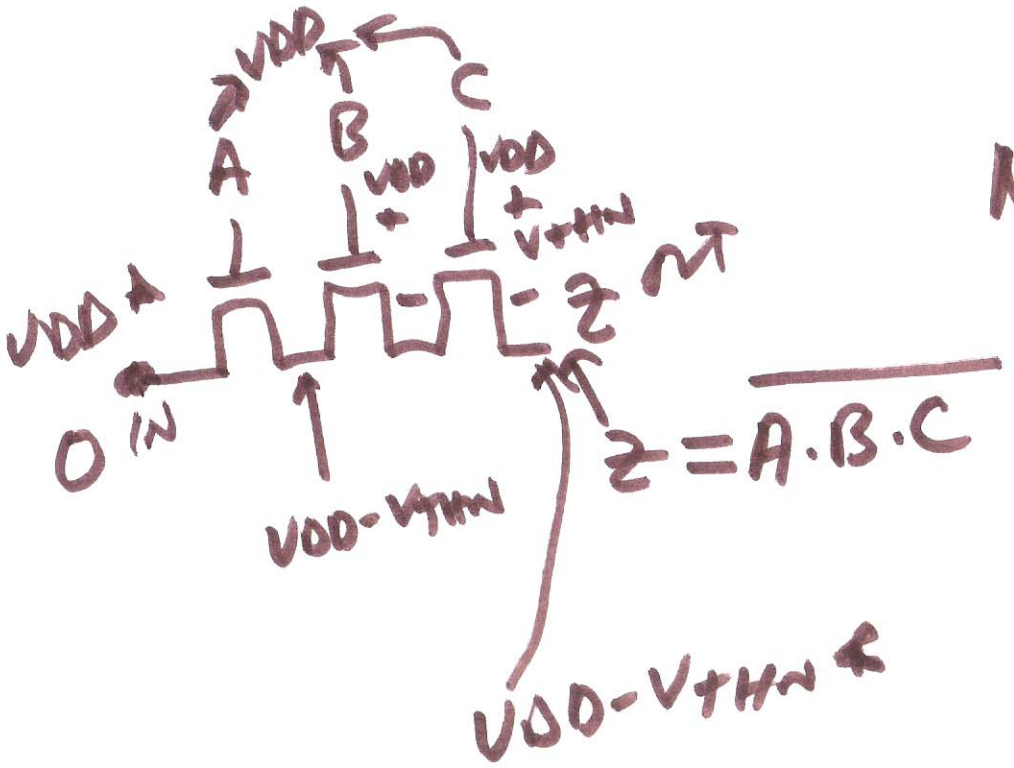
$V_{SG} = V_S - V_G = V_{THP}$

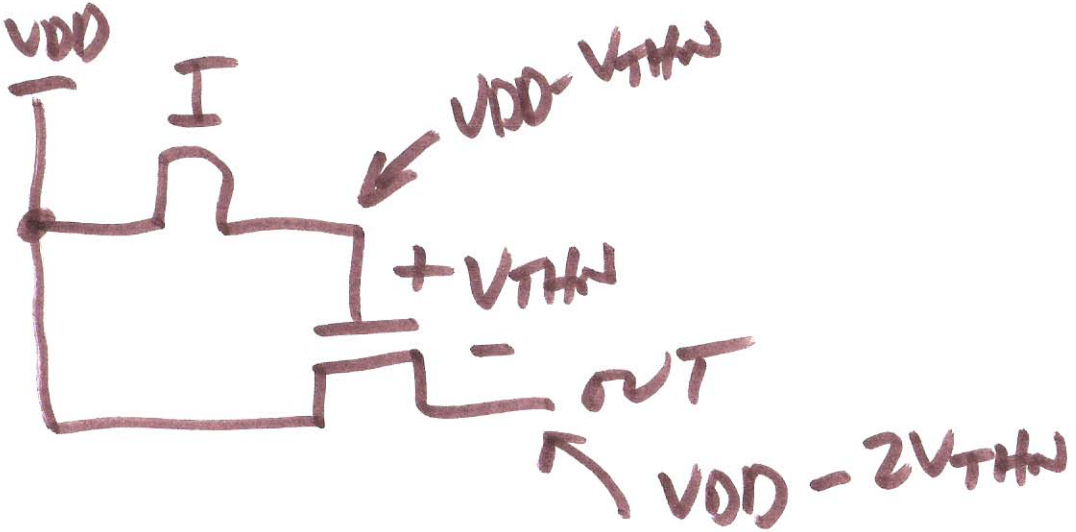
V_{THP}



Transmission gate, TG passes 1 & 0 well

NMOS, PG

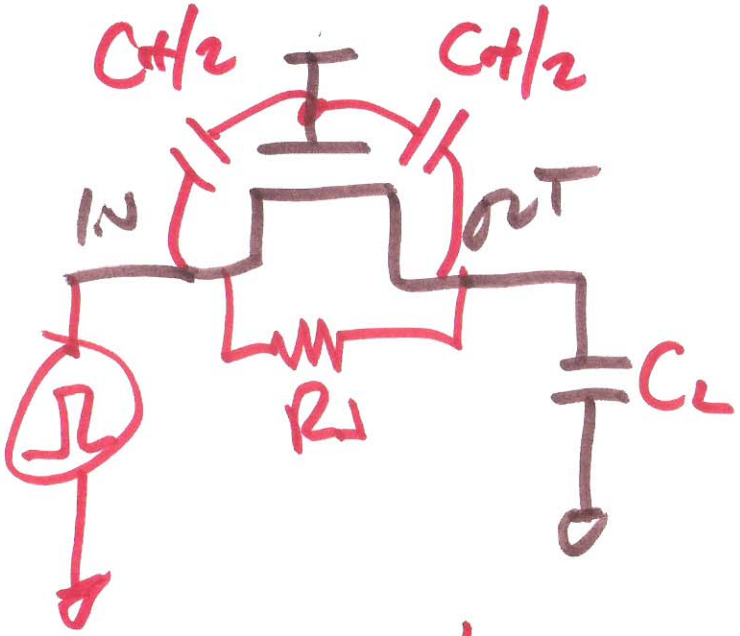

VDD
A
B
C
VDD
VDD + VTHN
OUT
VDD
0 IN
VDD - VTHN
Z = $\overline{A \cdot B \cdot C}$
VDD - VTHN


VDD
I
VDD - VTHN
+ VTHN
-
OUT
VDD - 2VTHN

3)

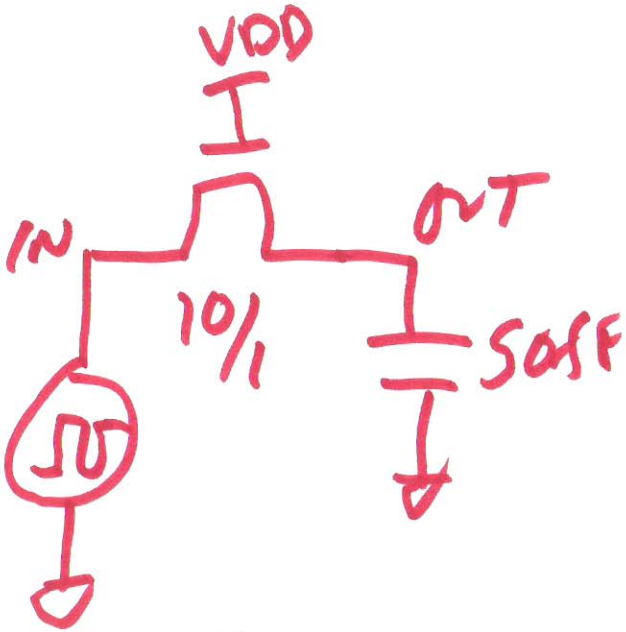
Delay through PGs

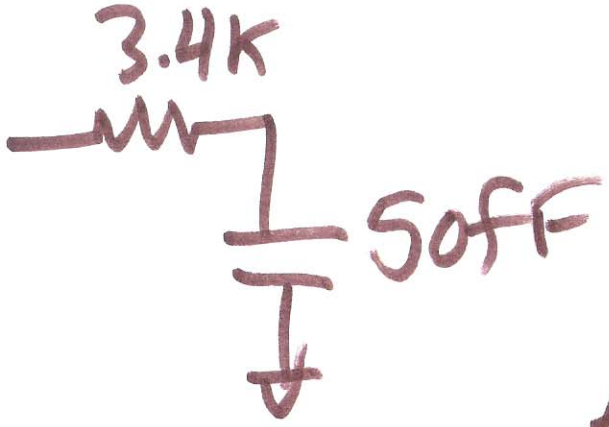
Δ C_{ot} = at gate C



$$t_{delay} = 0.7 R_N \left(C_L + \frac{C_{ot}}{2} \right)$$

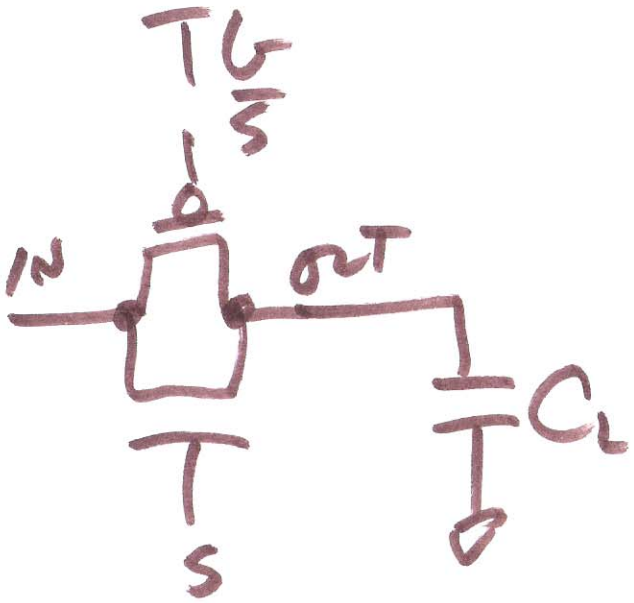
$$\simeq 0.7 R_N \cdot C_L$$

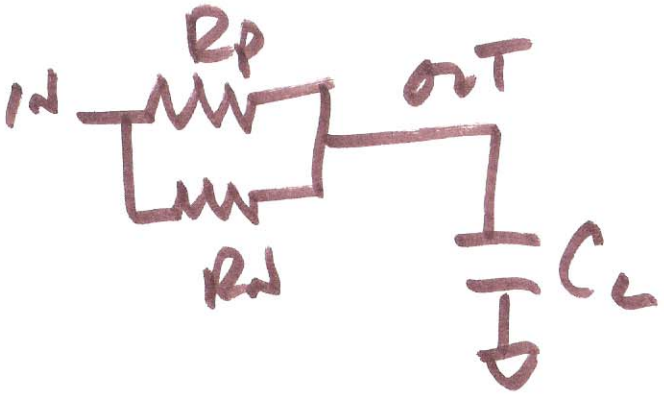




$$t_d = 0.7 \cdot 3.4k \cdot Soff$$
$$= 120\,ps$$

5)

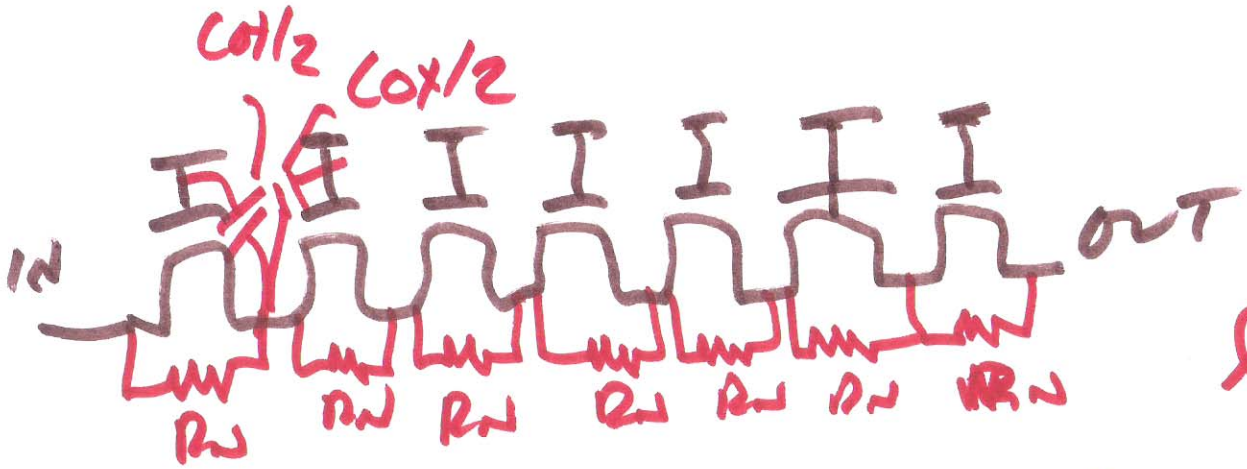




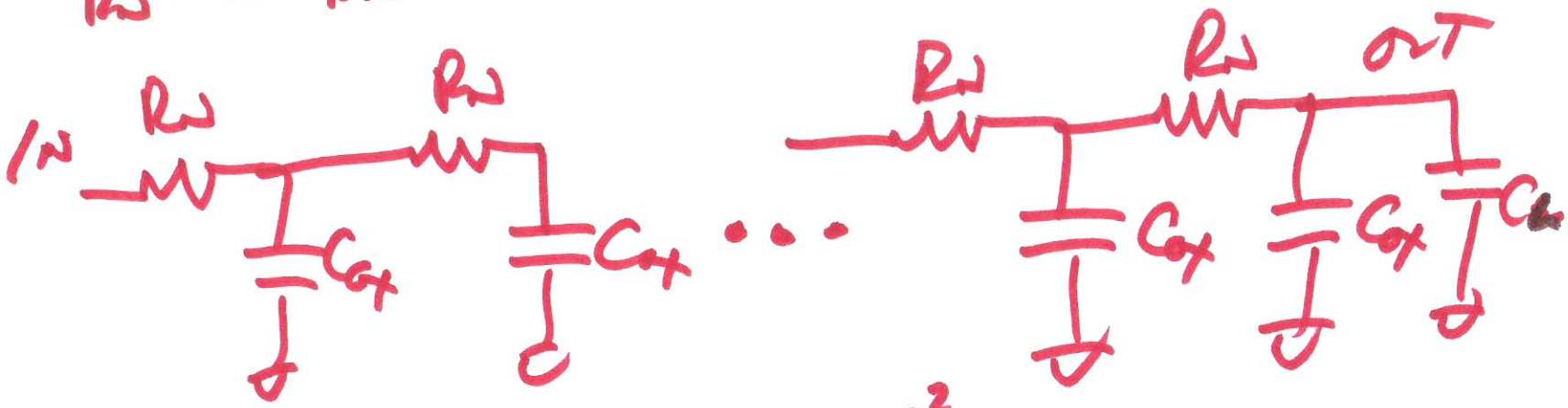
$$t_d = 0.7(R_N \| R_P) \cdot C_L$$

6)

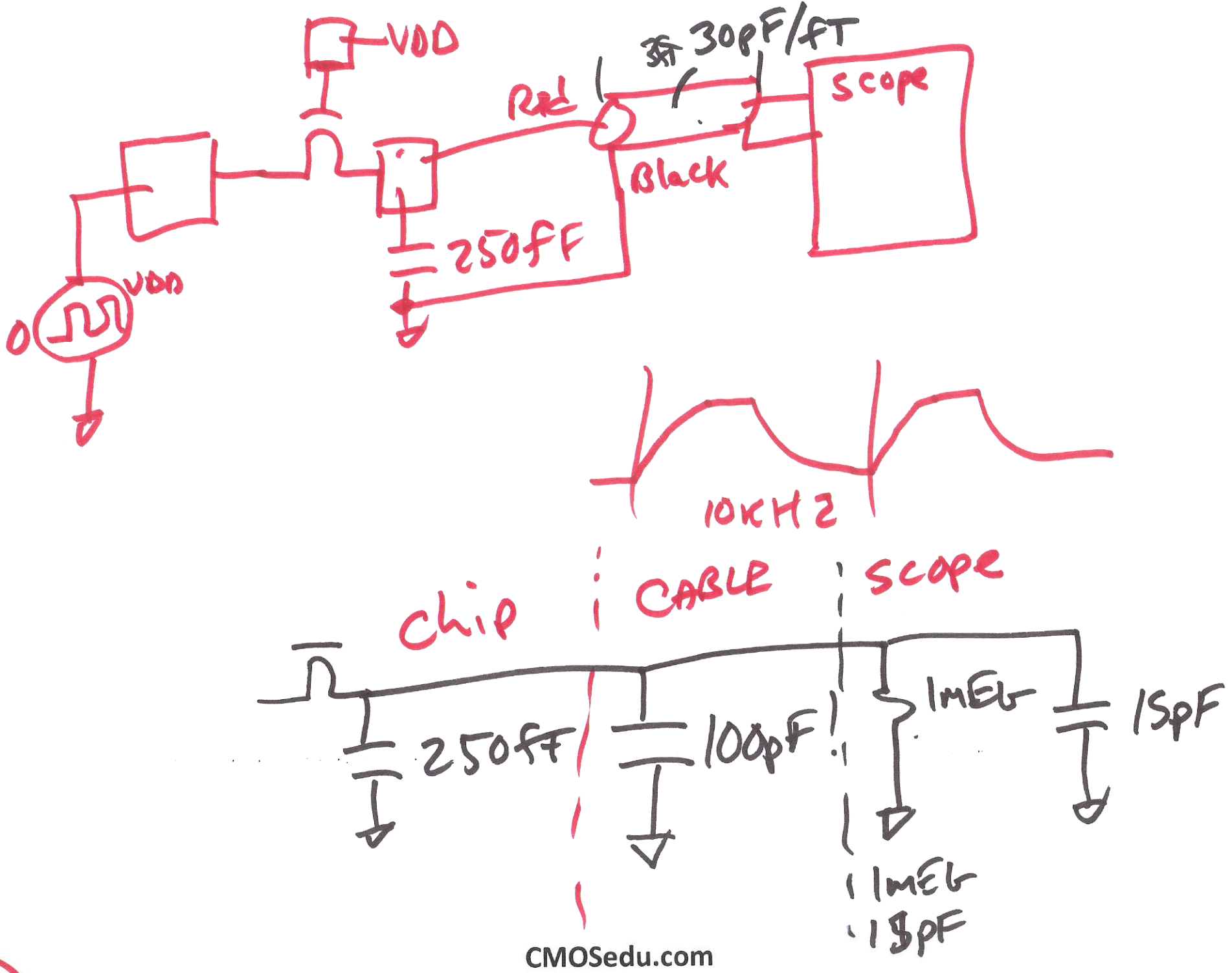
Delay through long string of PGs



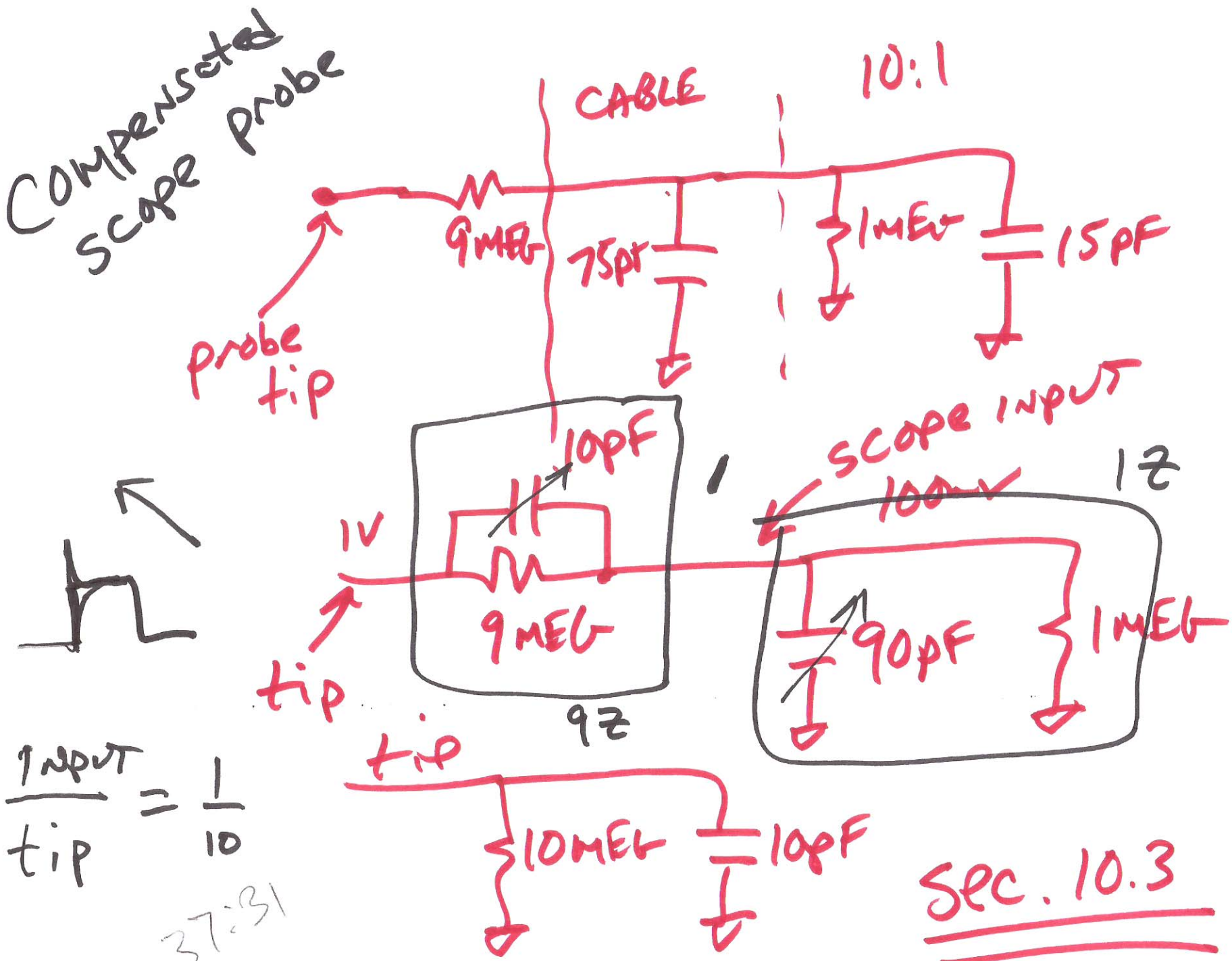
ℓ = # of stages



$$t_d = 0.35 \cdot R_N \cdot C_x \cdot \ell^2 + 0.7 \cdot \ell R_N \cdot C_L$$



8)



$$\frac{\text{INPUT}}{\text{tip}} = \frac{1}{10}$$

37:31

Sec. 10.3

9)