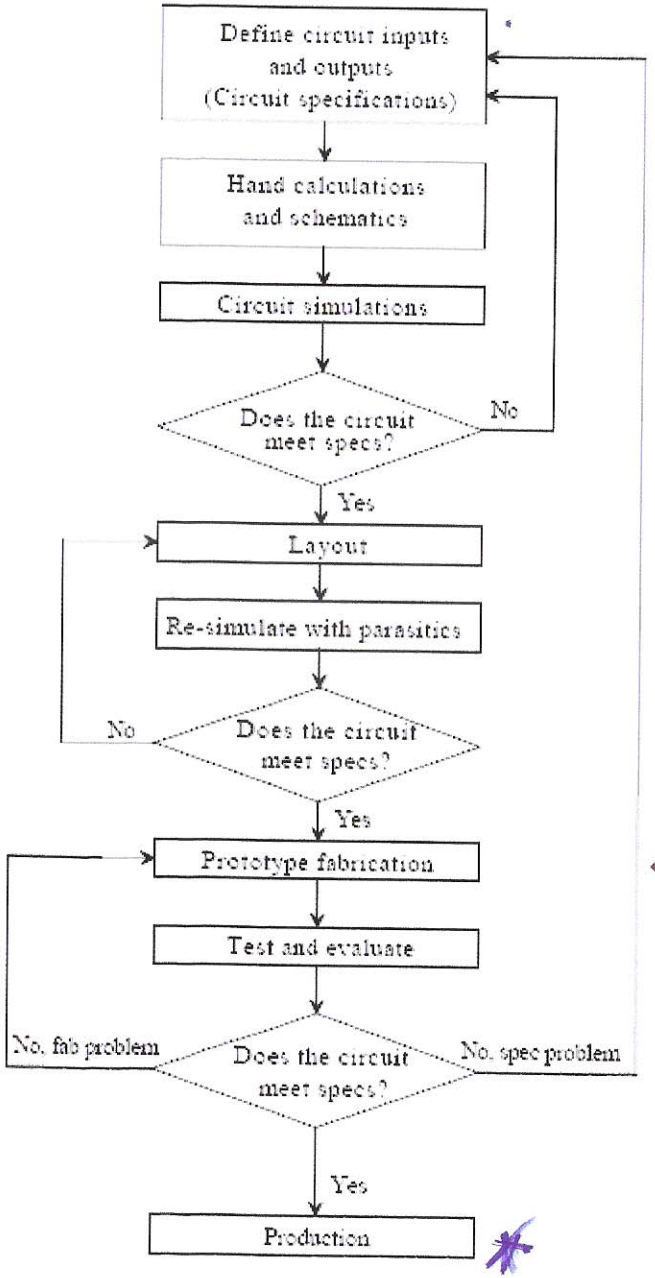
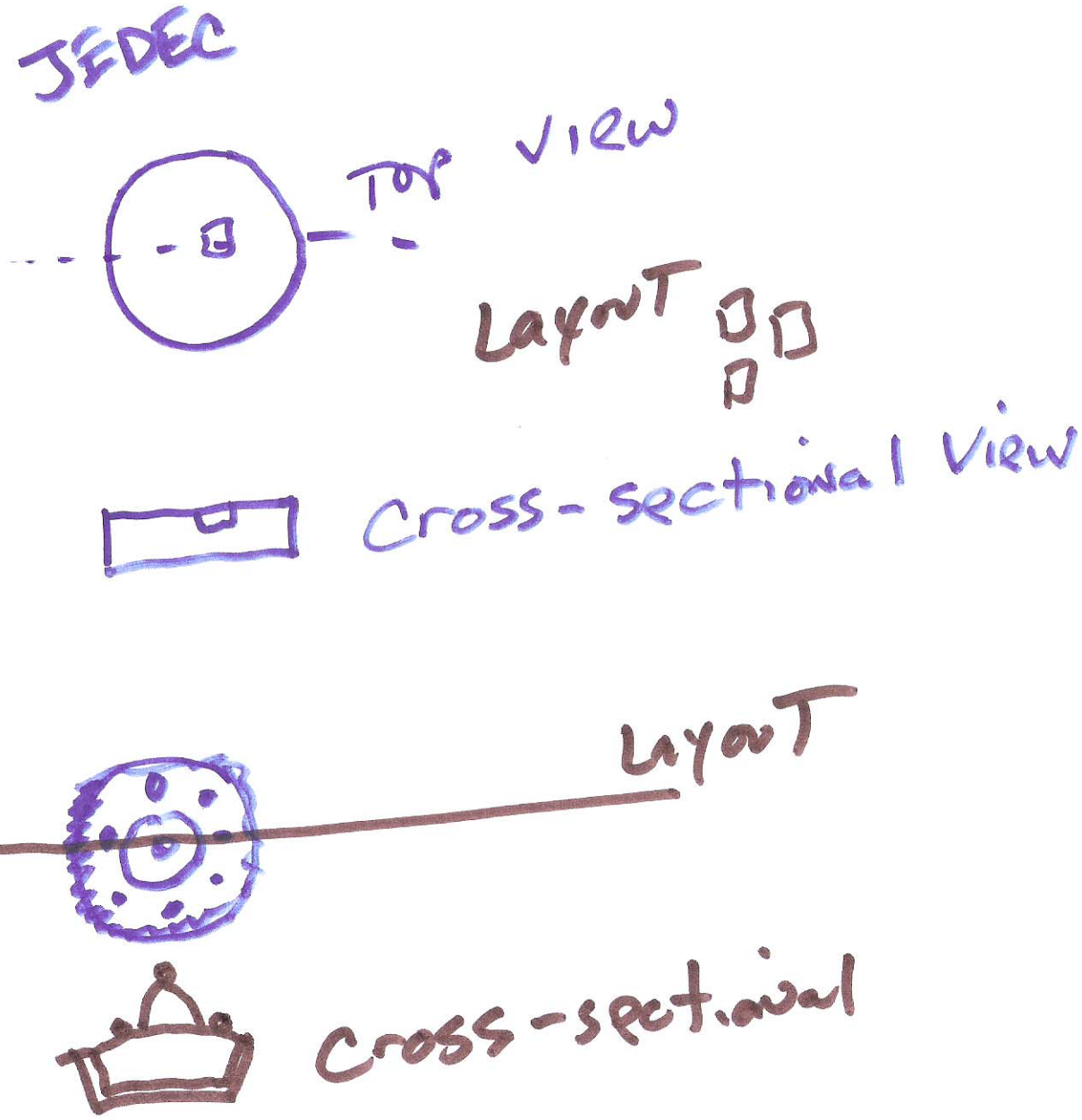


Figure 1.1 Flowchart for the CMOS IC design process.



Complementary Metal oxide semiconductor

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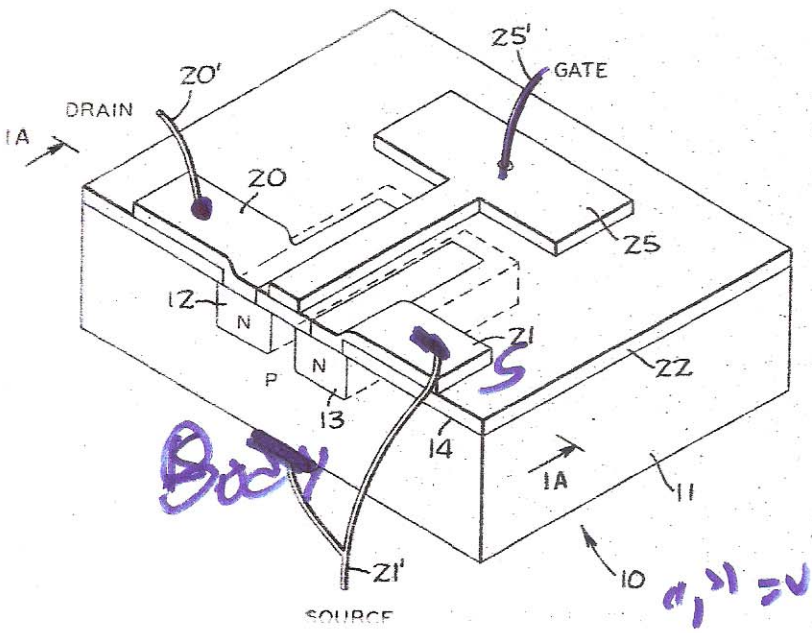
Fig. 1



VDD
PMOS
NMOS
"1" = VDD
0
on
off

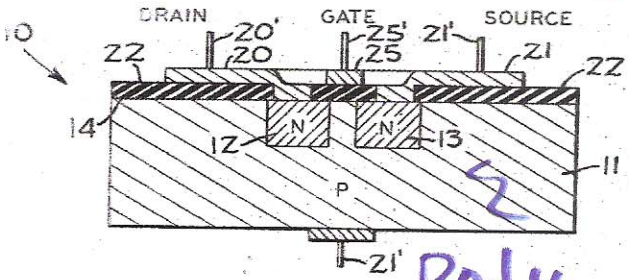


Fig. 1A

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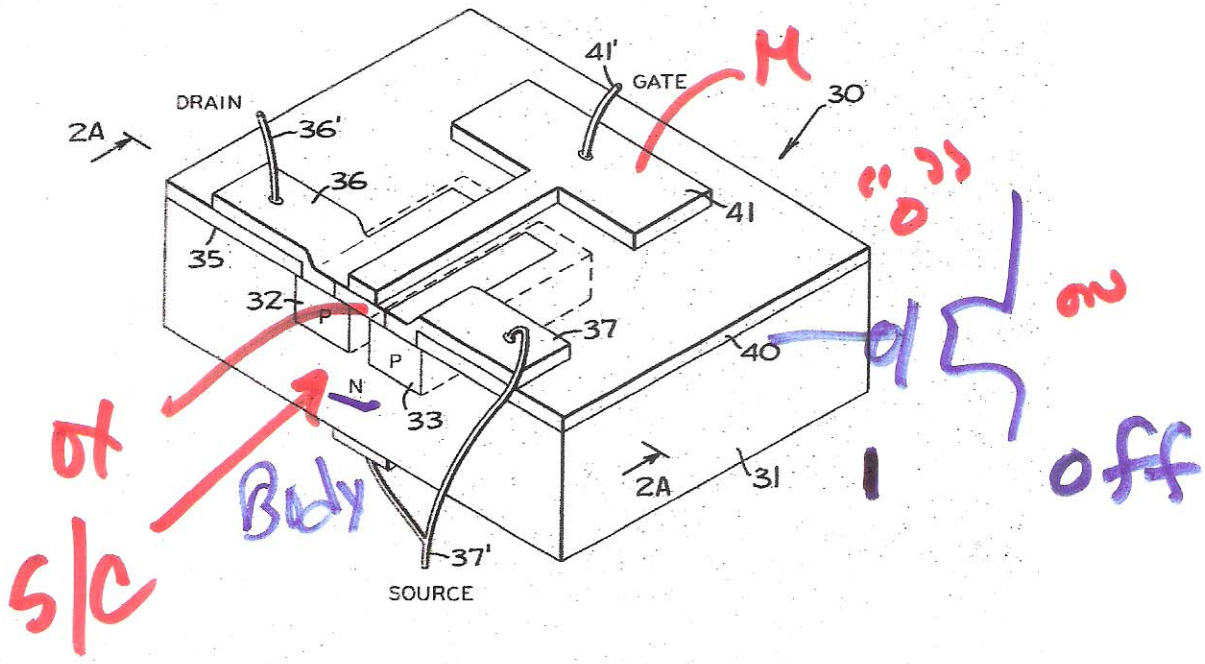
Fig. 2



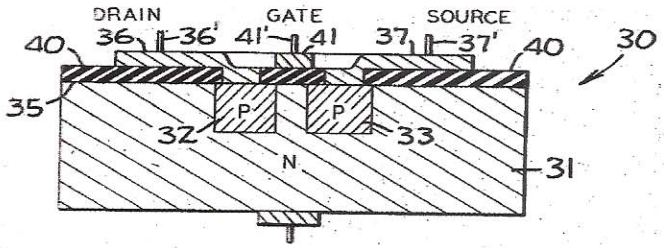


Fig. 2A

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Fig. 3

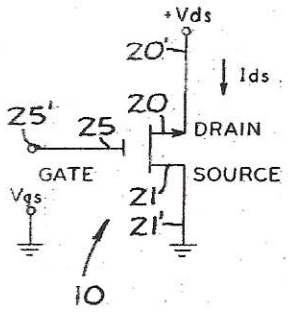


Fig. 4

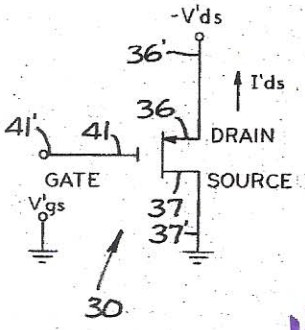
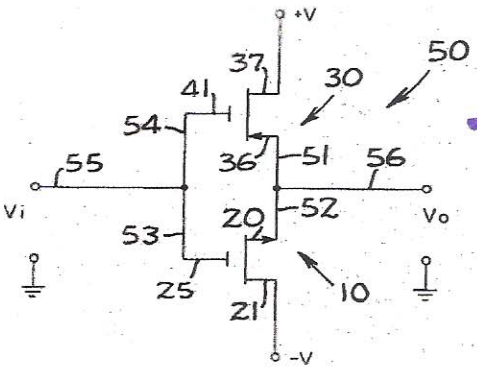


Fig. 5



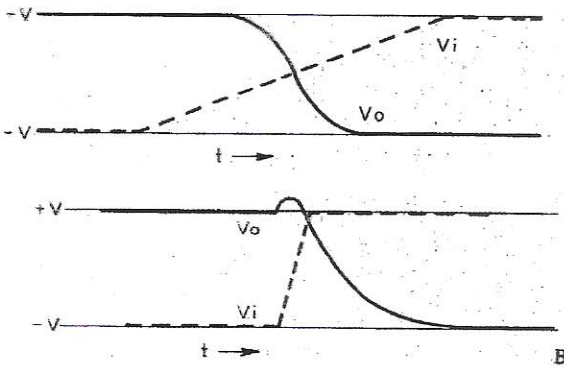


Fig. 5A

Fig. 5B

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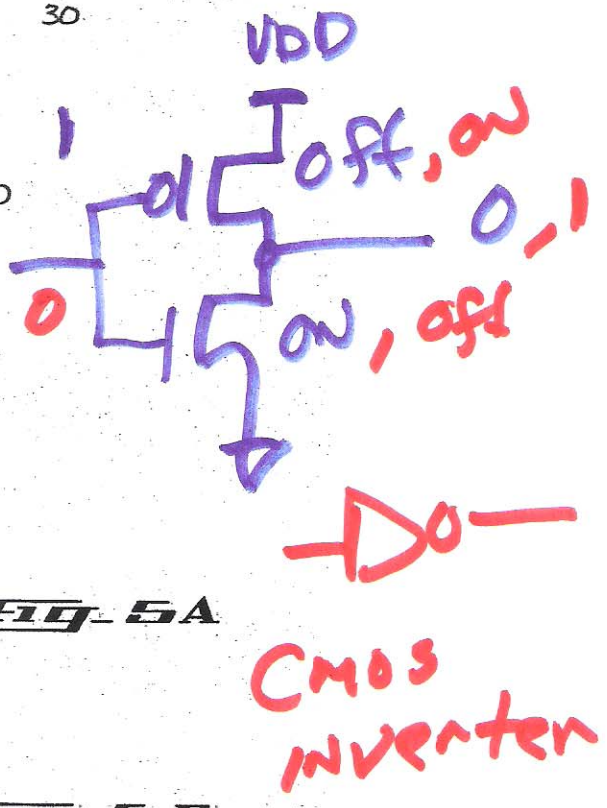

41