

## [Cadence Design System Tutorials from CMOSedu.com](#) ([Return](#))

### Tutorial 5 - Design, layout, and simulation of a ring oscillator

In this [tutorial](#) we'll design, lay out, and simulate the operation of a ring oscillator.

At this point we should be getting comfortable with the tools.

One of the goals of this tutorial is to teach how to use arrays and buses

Copy the library, Tutorial\_4, into a new library called Tutorial\_5.

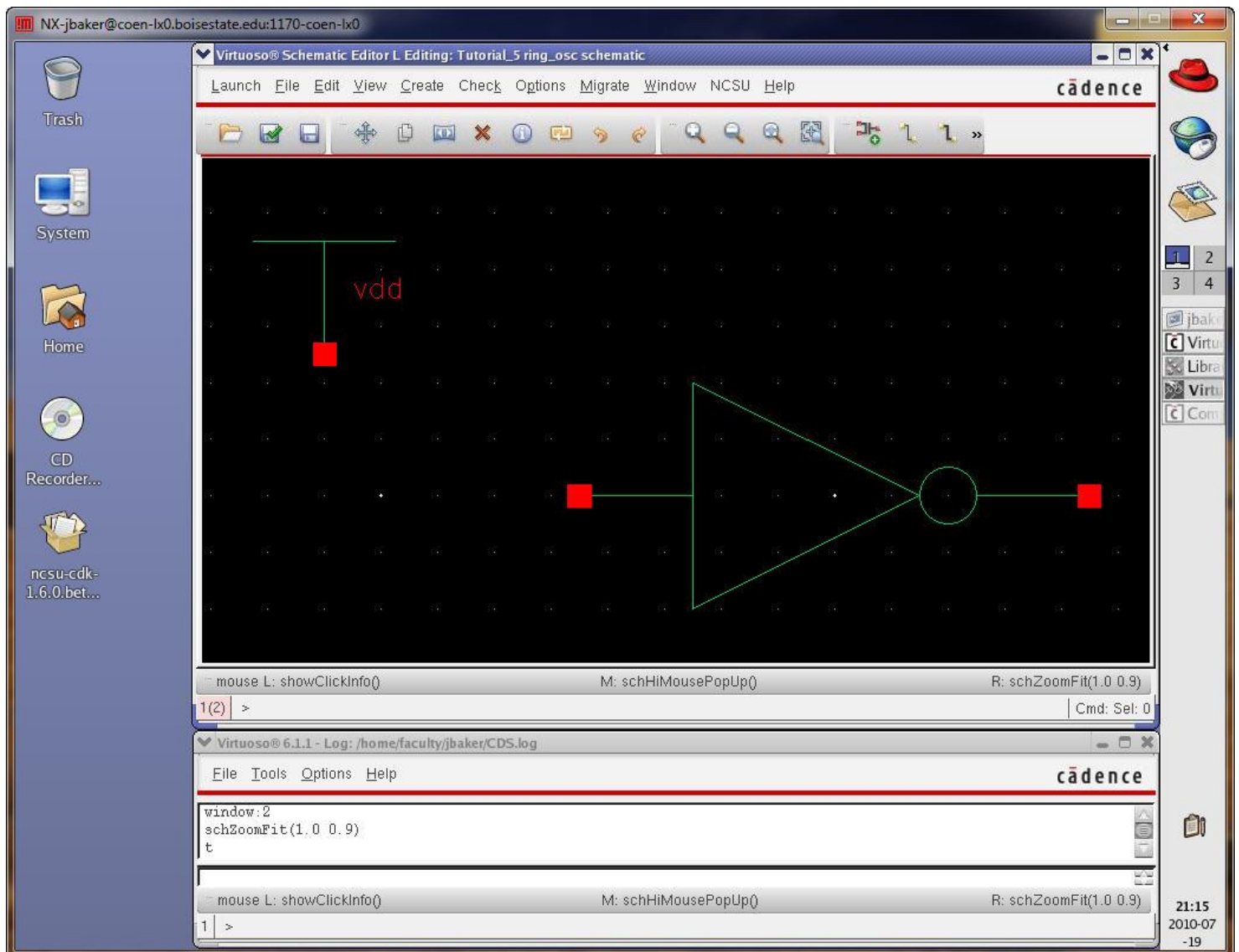
Ensure, when you copy, that "update instances" is selected so that the new library doesn't reference cells in the other libraries.

As always, put the new library in \$HOME/CMOSedu

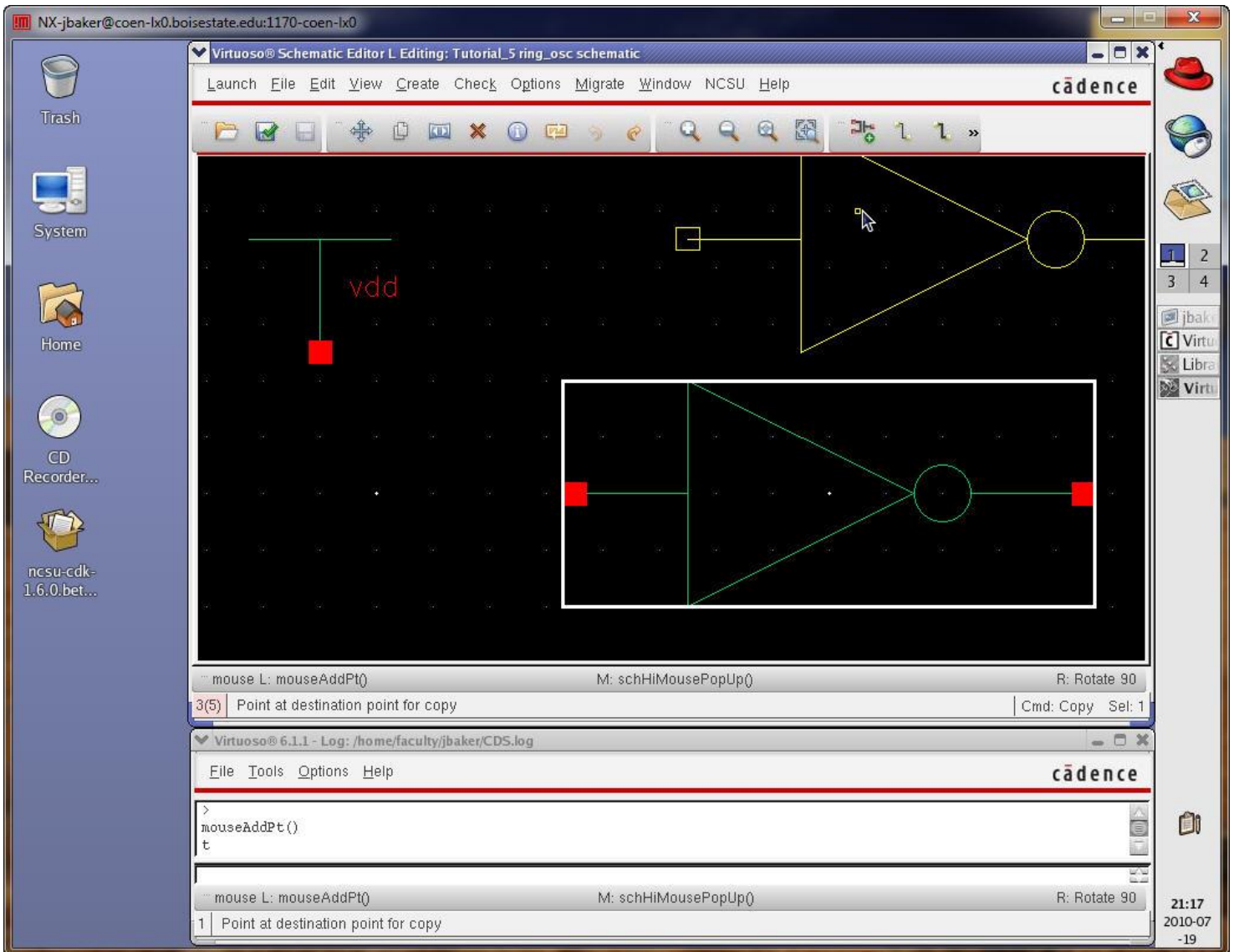
Create a new schematic cell view called ring\_osc.

In this cell view place the inverter symbol that was created in tutorial 3.

Also place the vdd supply net symbol, see below.

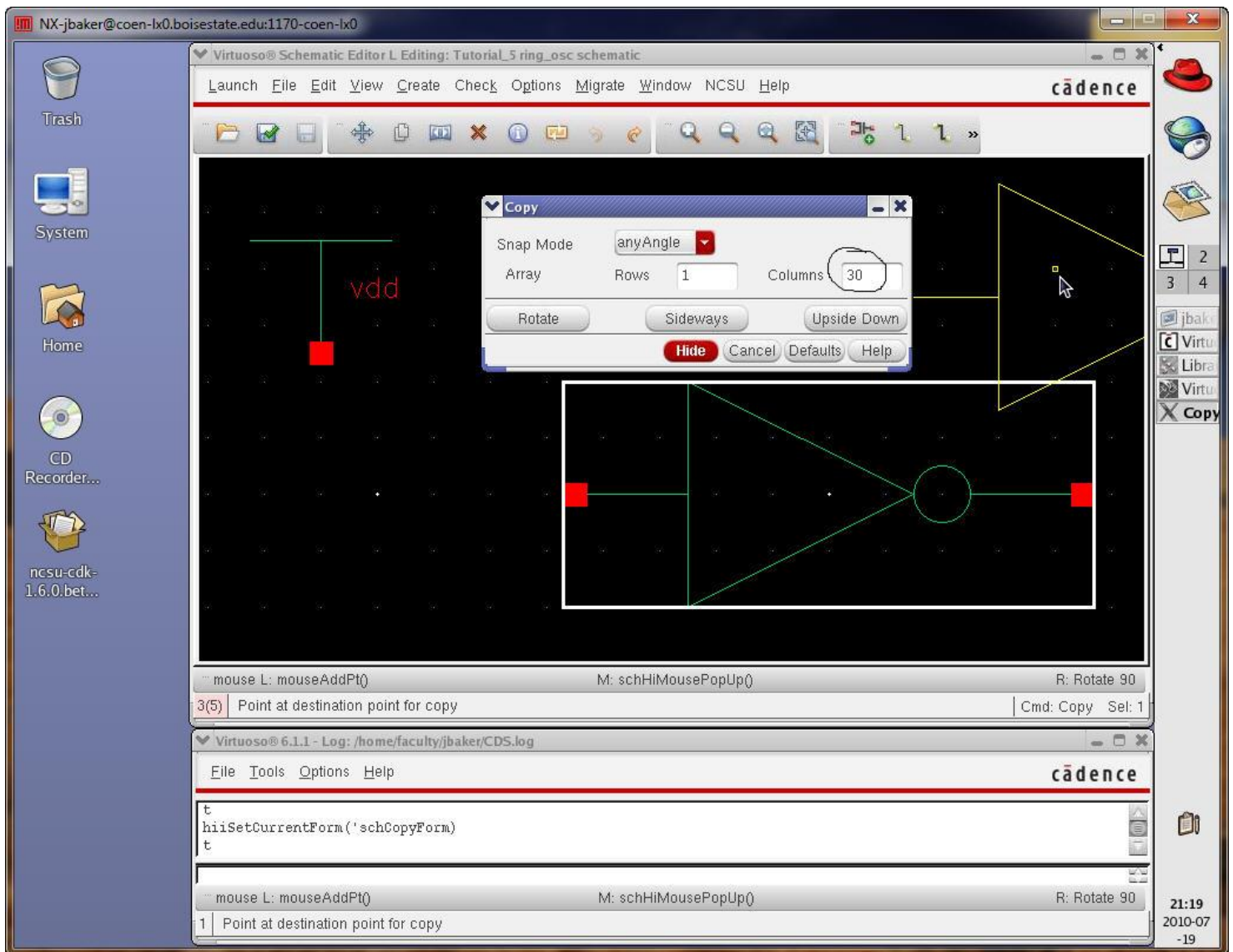


Next press **c** (for copy) and the inverter (to copy the inverter).



Before placing the copy of the inverter press **F3** (special options).

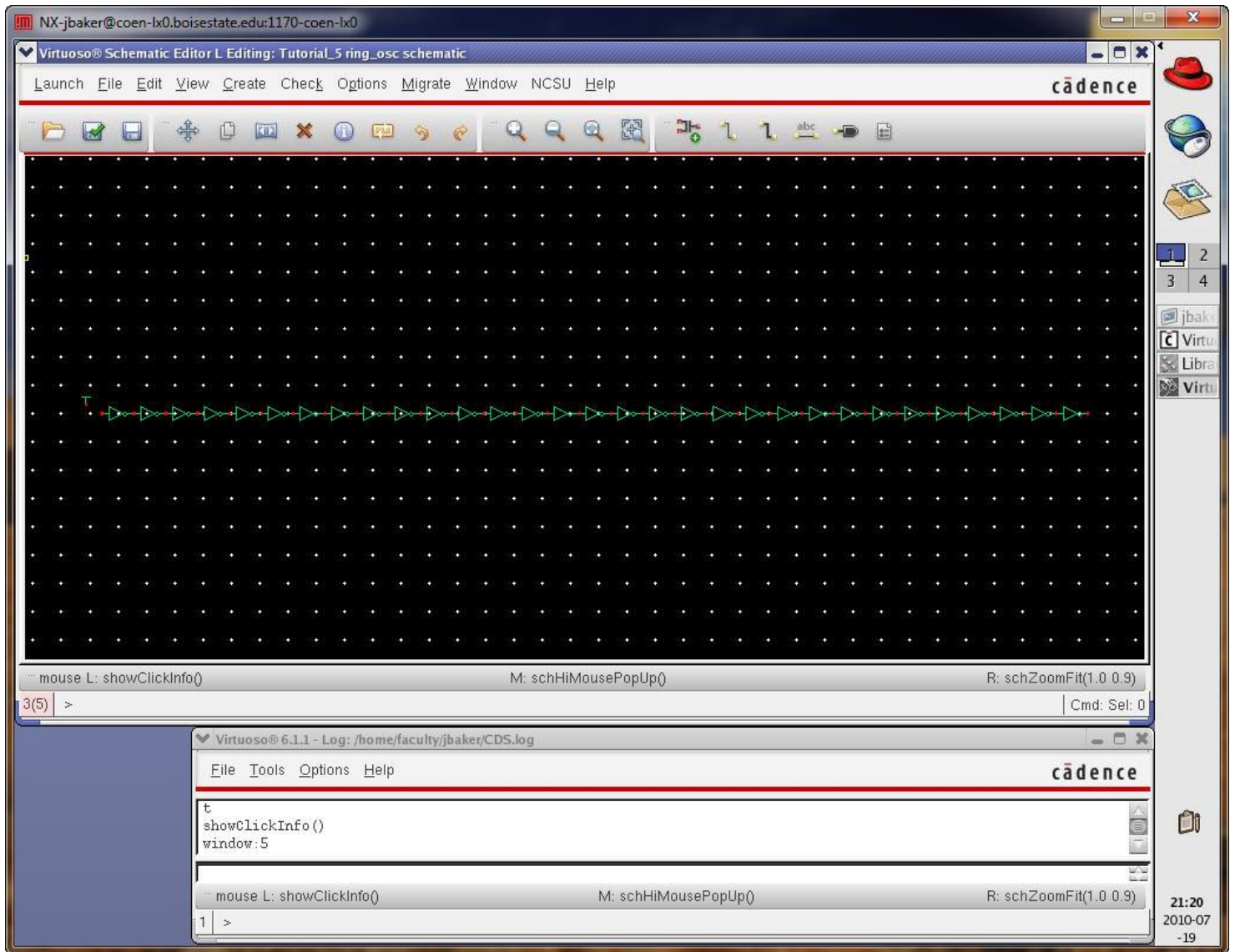
We'll make a 31 stage ring oscillator so select 30 columns as seen below (to add 30 inverters to the existing one).



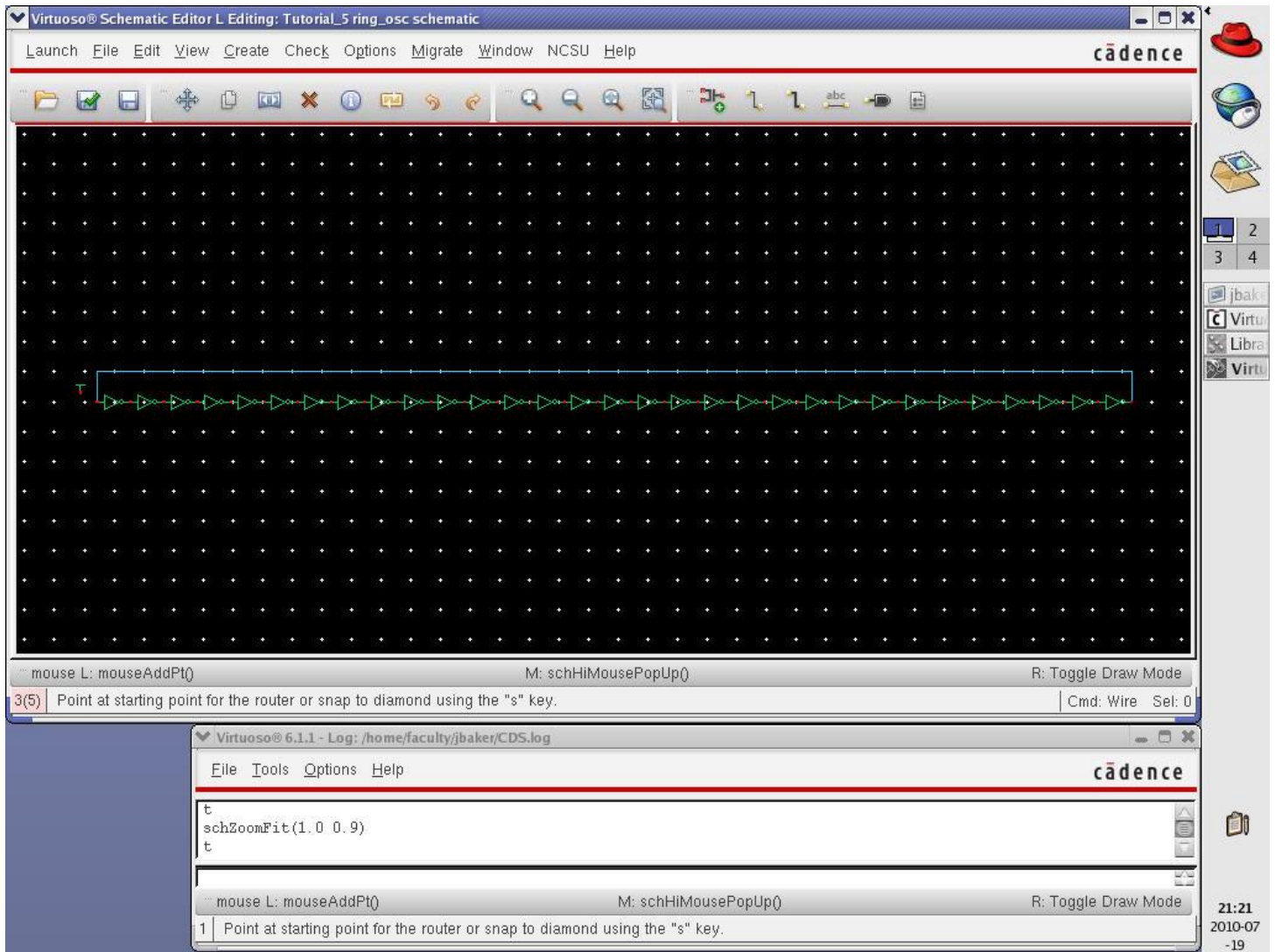
Instantiate the (first copied) inverter on the output of the existing inverter.

Repeat for the second copied inverter to get the following.

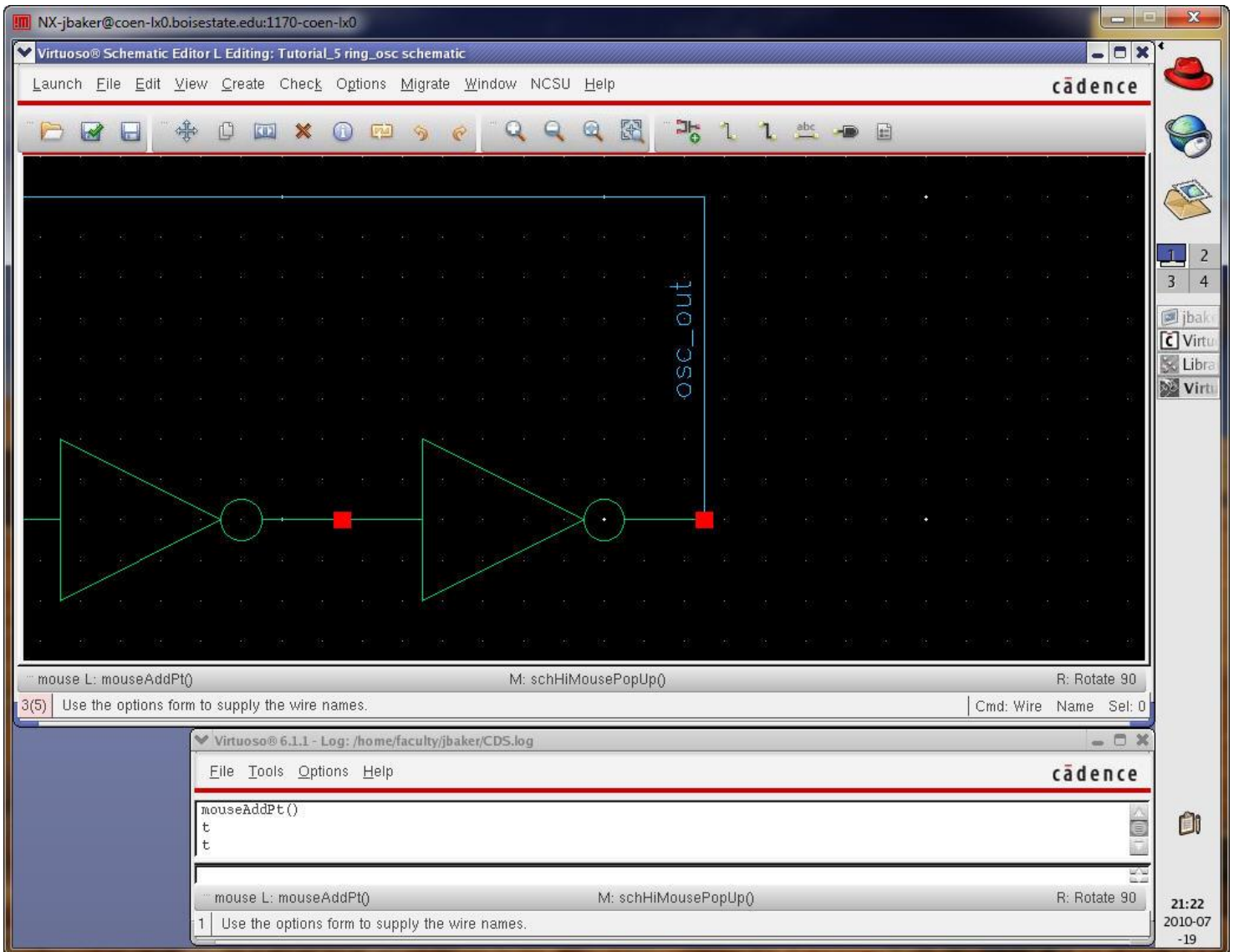
Note that if we wanted a wire between the inverters we could have added the wire on the output of the first inverter and then copy both the inverter and wire.



Add a wire connecting the output of the last inverter to the input of the first inverter.



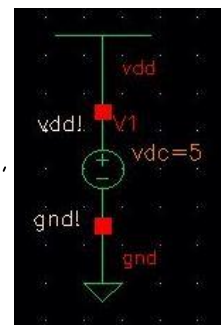
Label the wire `osc_out` as seen below.  
Check and Save the schematic.



Now start the ADE.

Set the MOSFET models (Setup -> Model Libraries).

Set the vdd! to 5 V (Setup -> Stimuli), or add a vdc (but **not** both as discussed in [Tutorial 3](#)).

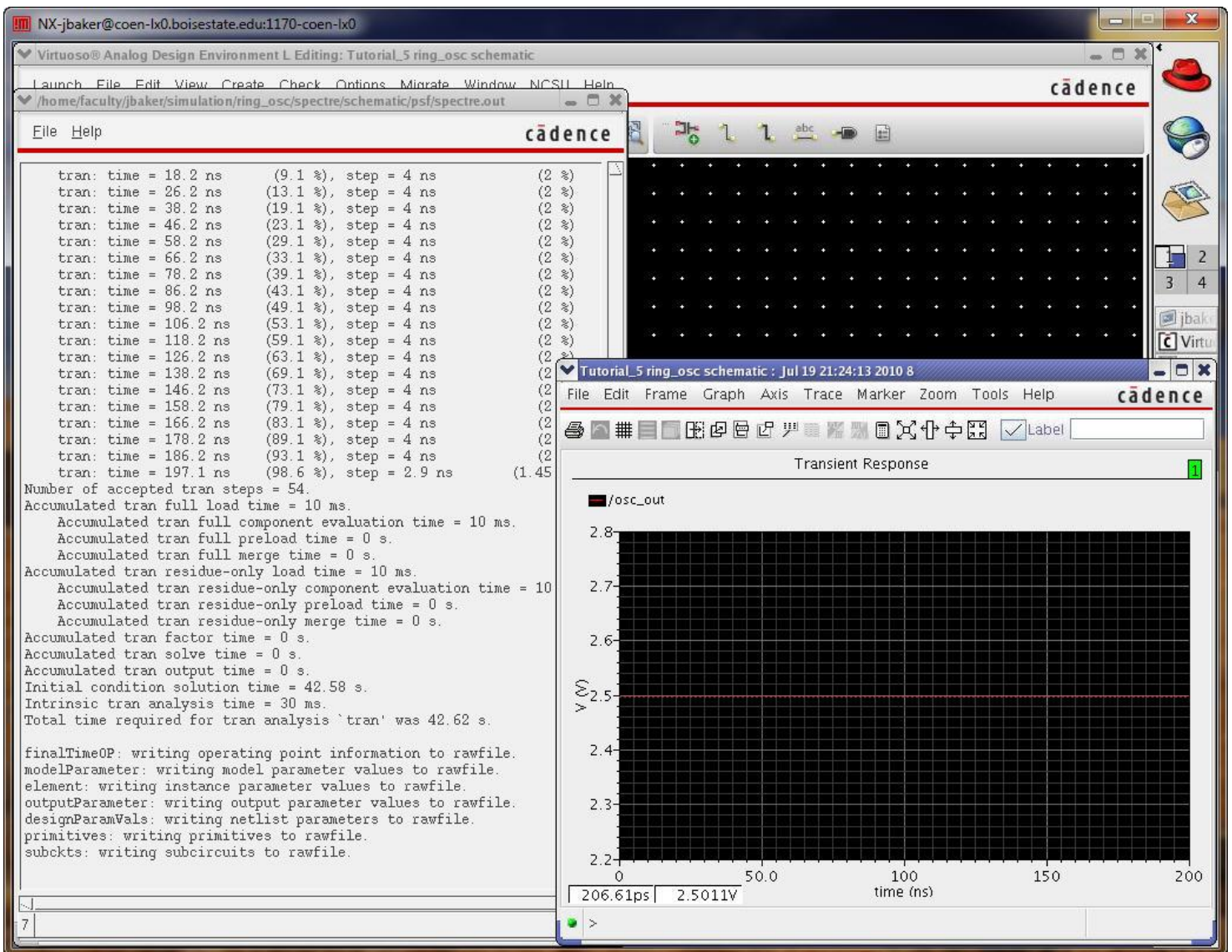


Select the outputs to plot (select osc\_out)

Set the analysis to a transient with a length of 200 ns.

If doing any of these things is a challenge review tutorials 3 or 4.

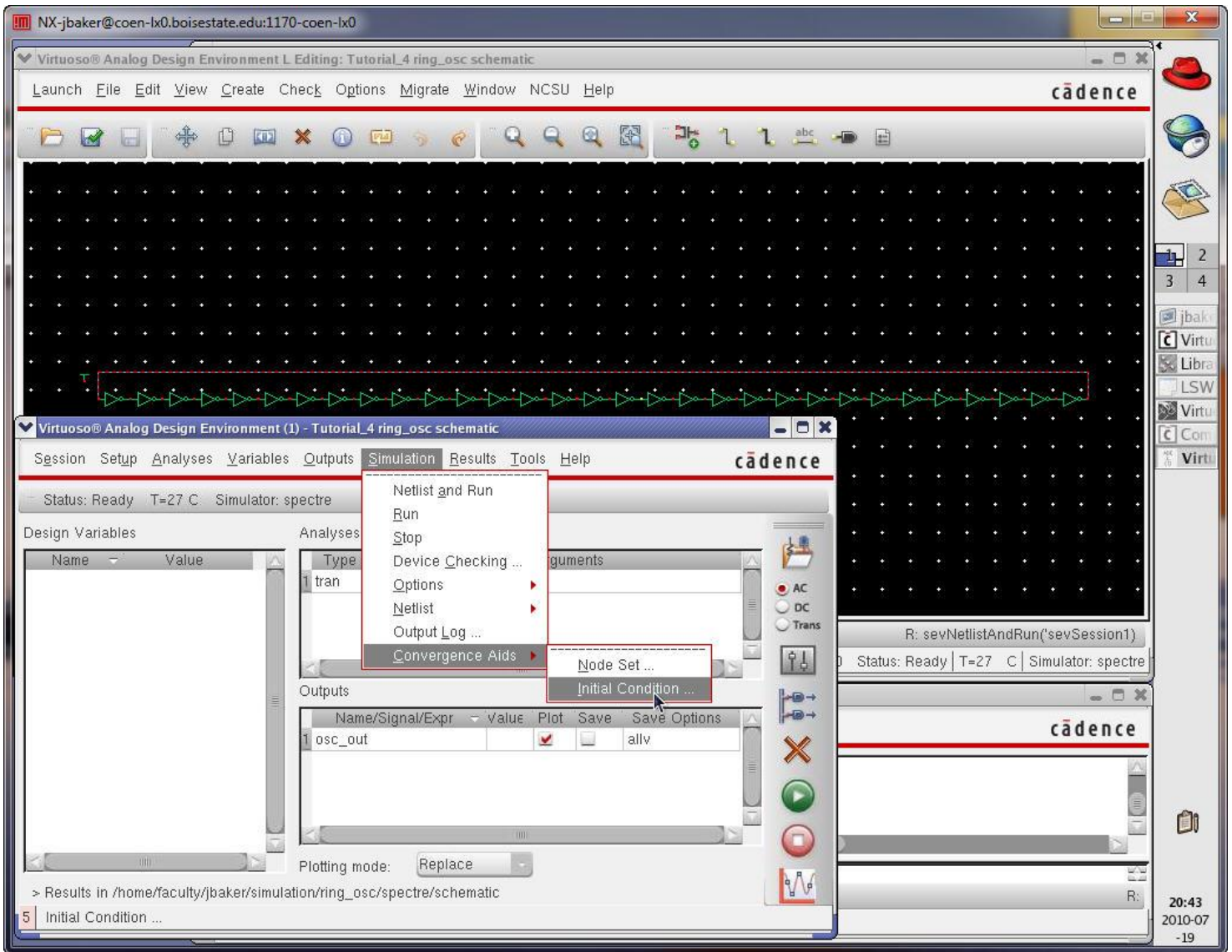
Save the State (Cellview) and "Netlist and Run" the simulation.



The output is steady at 2.5V!

In a real circuit noise would kick-start the oscillations.

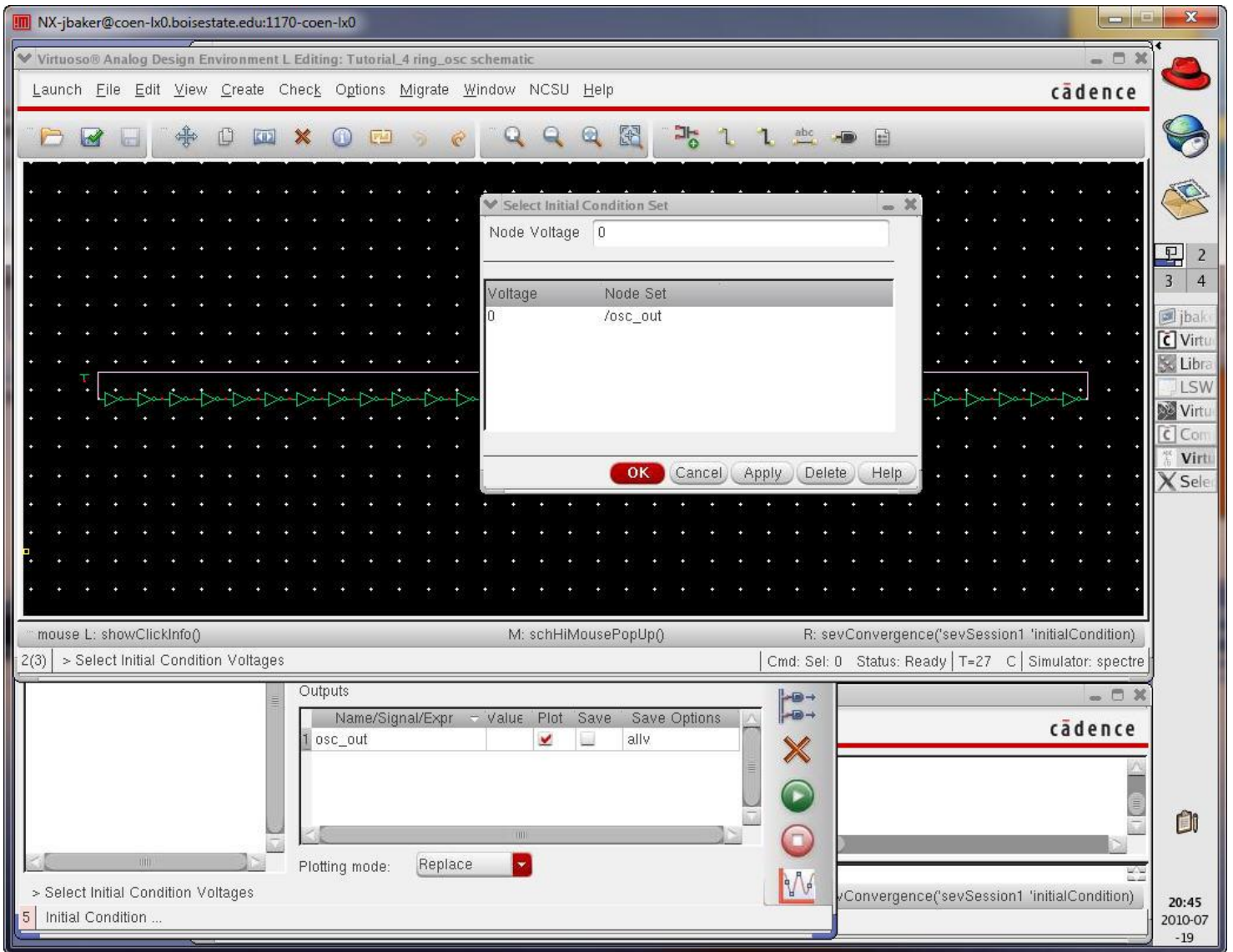
Let's do this in the simulation by adding an initial condition.



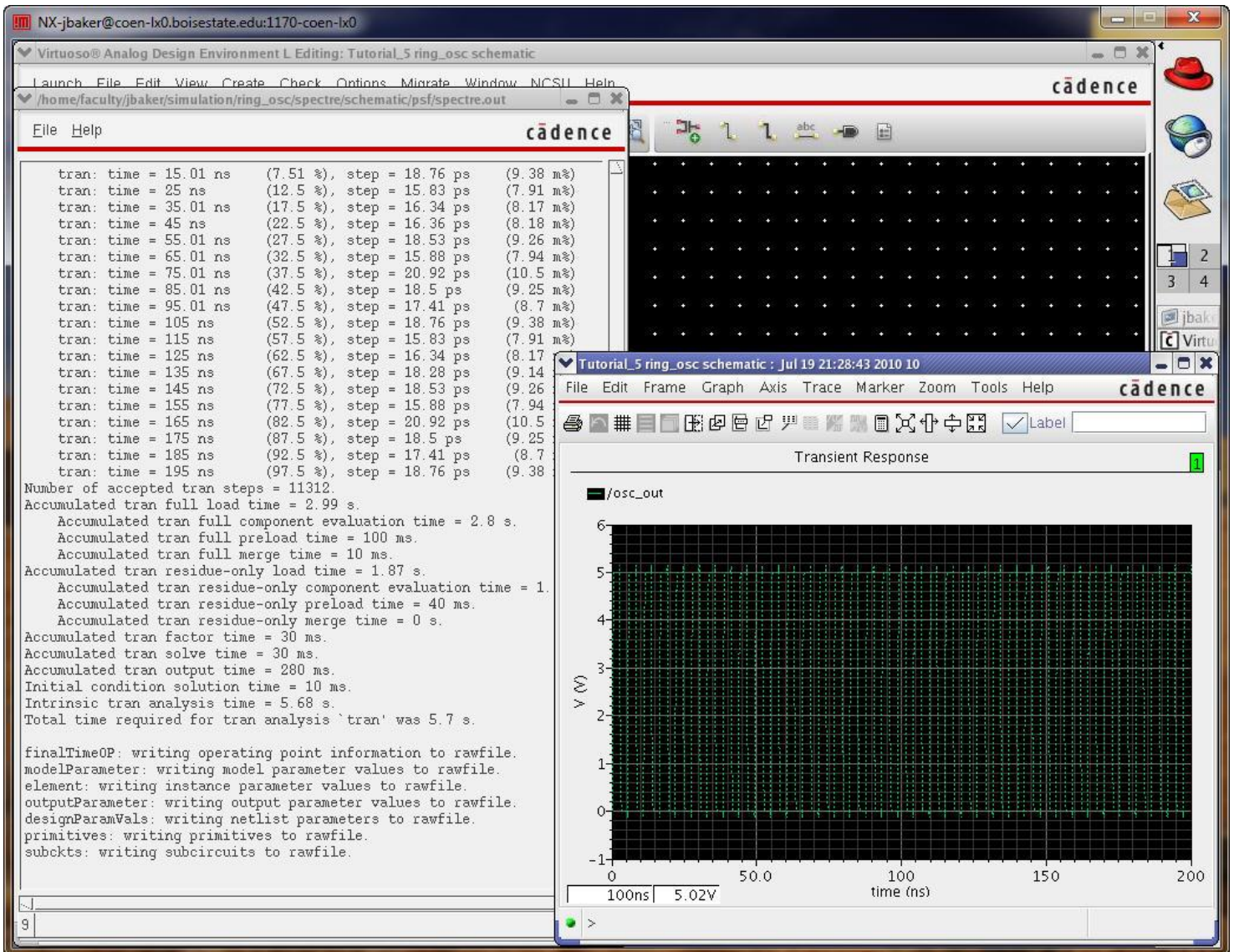
Select a node voltage of 0 and click on the wire labeled osc\_out results in what is seen below (you may have to access the menu again to view this condition).

Save the state of the simulation.





After saving the state and simulating again we get



which is what we expect a ring oscillator to do :-)

Save the state and close the ADE.

Let's make the schematic more pleasant to look at.

Delete all of the inverters and the wires except for the first inverter.

Change the inverters name from IO to IO<1:31> (an array of 31) and display the name (value).

The screenshot shows the Cadence Virtuoso Schematic Editor interface. The main window displays a schematic with a red square labeled 'vdd' connected to an inverter symbol. A dialog box titled 'Edit Object Properties' is open, showing the following details:

- Apply To: **only current** (dropdown), **instance** (dropdown)
- Show:  system,  user,  CDF
- Buttons: Browse, Reset Instance Labels Display
- Property Table:
 

| Property      | Value      | Display |
|---------------|------------|---------|
| Library Name  | Tutorial_5 | off     |
| Cell Name     | inverter   | off     |
| View Name     | symbol     | off     |
| Instance Name | I0<1:31>   | value   |
- Buttons: Add, Delete, Modify
- User Property Table:
 

| User Property     | Master Value     | Local Value | Display |
|-------------------|------------------|-------------|---------|
| interfaceLastCh.. | 18 13:51:23 2010 |             | off     |
- Buttons: OK, Cancel, Apply, Defaults, Previous, Next, Help

The status bar at the bottom of the editor shows: mouse L: showClickInfo() M: schHiMousePopUp() R: schHiObjectProperty() Cmd: Sel: 1

Below the editor is a log window titled 'Virtuoso@ 6.1.1 - Log: /home/faculty/jbaker/CDS.log' with the following content:

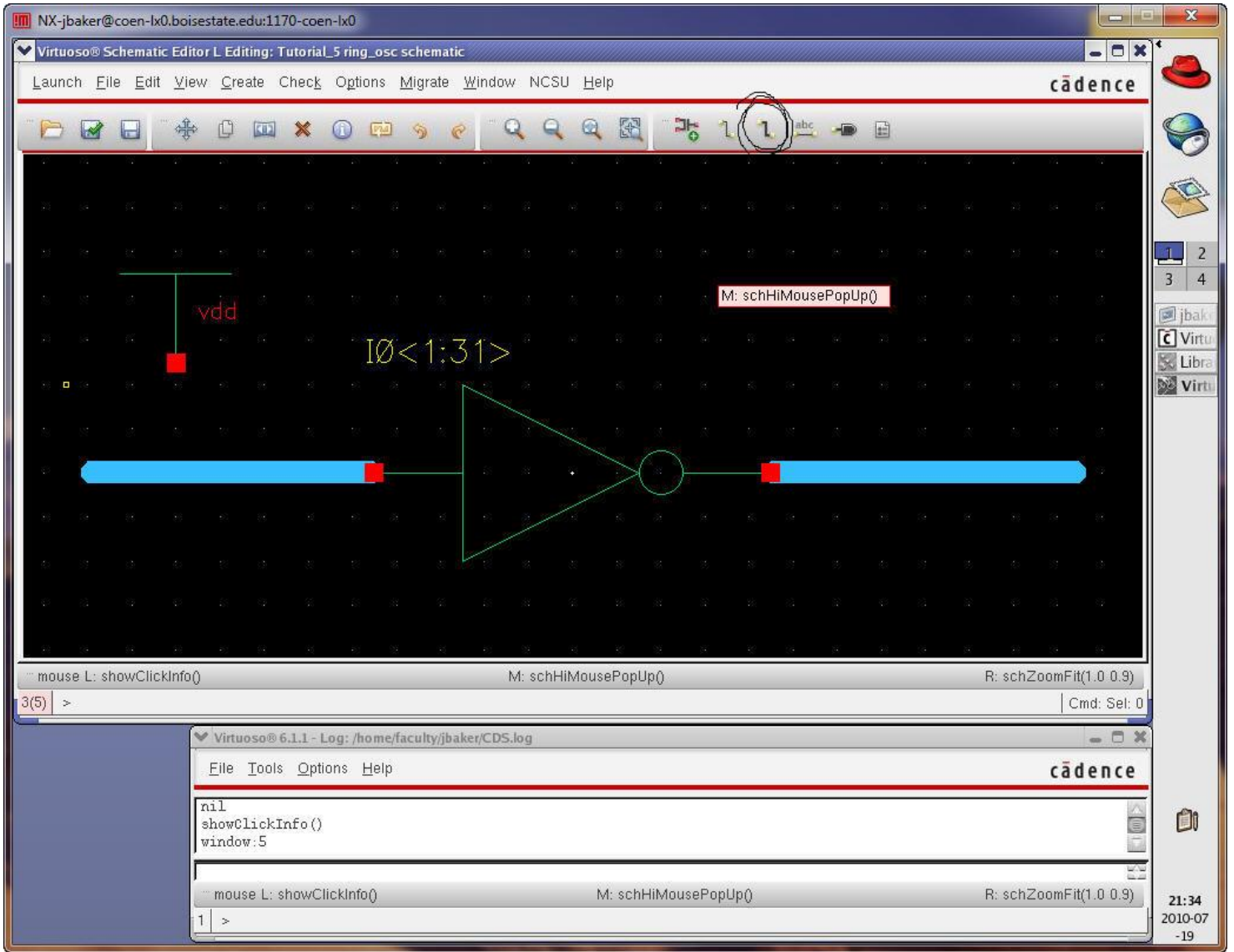
```

File Tools Options Help
"IO<1:31>"
schObjPropForm->instanceName_dsp->value="value"
"value"
mouse L: showClickInfo() M: schHiMousePopUp() R: schHiObjectProperty()
1 >

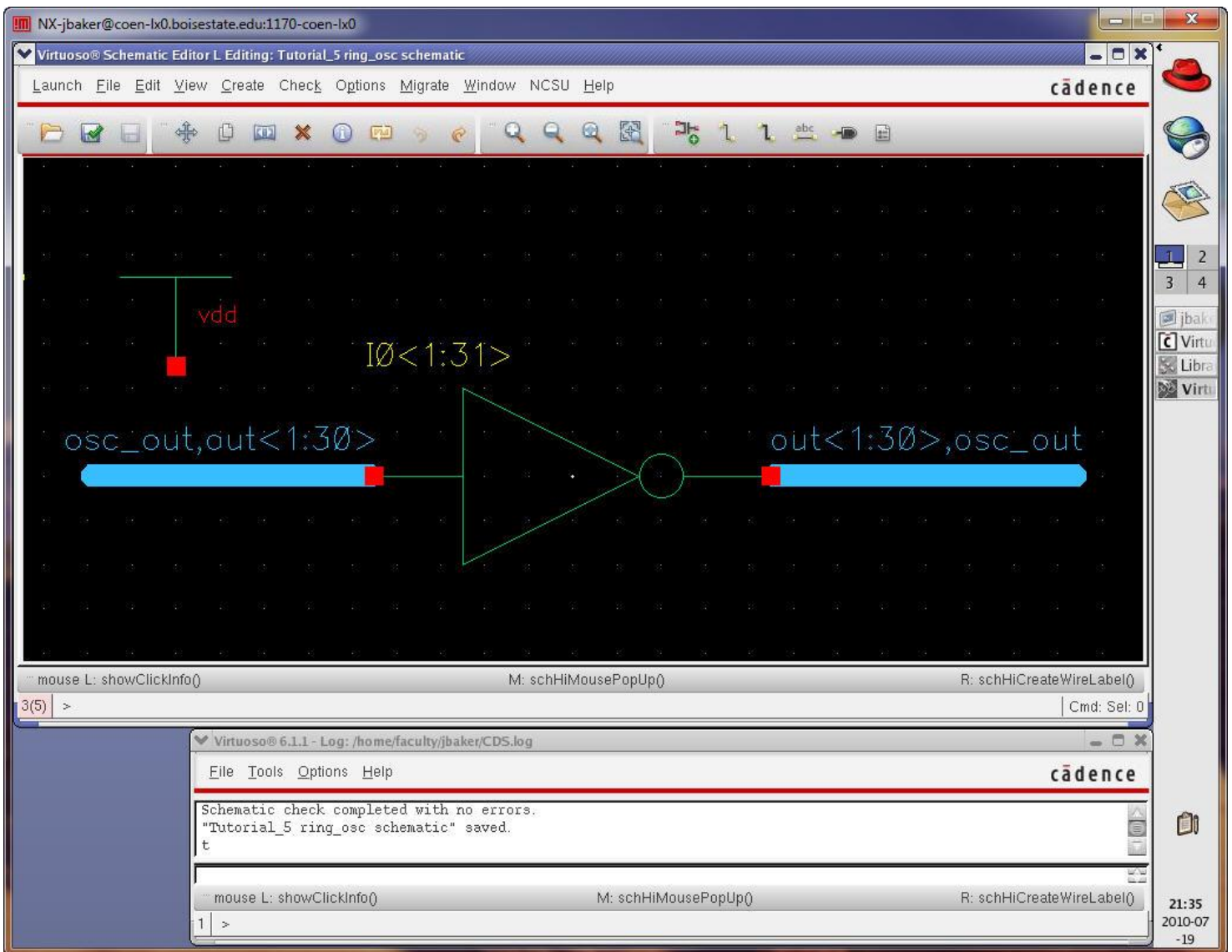
```

The system tray on the right shows the date and time: 21:32 2010-07 -19.

Now use the wide wire (**W**) to connect to the input and output of the symbol.



Use the wire label (I) to add names as seen below.

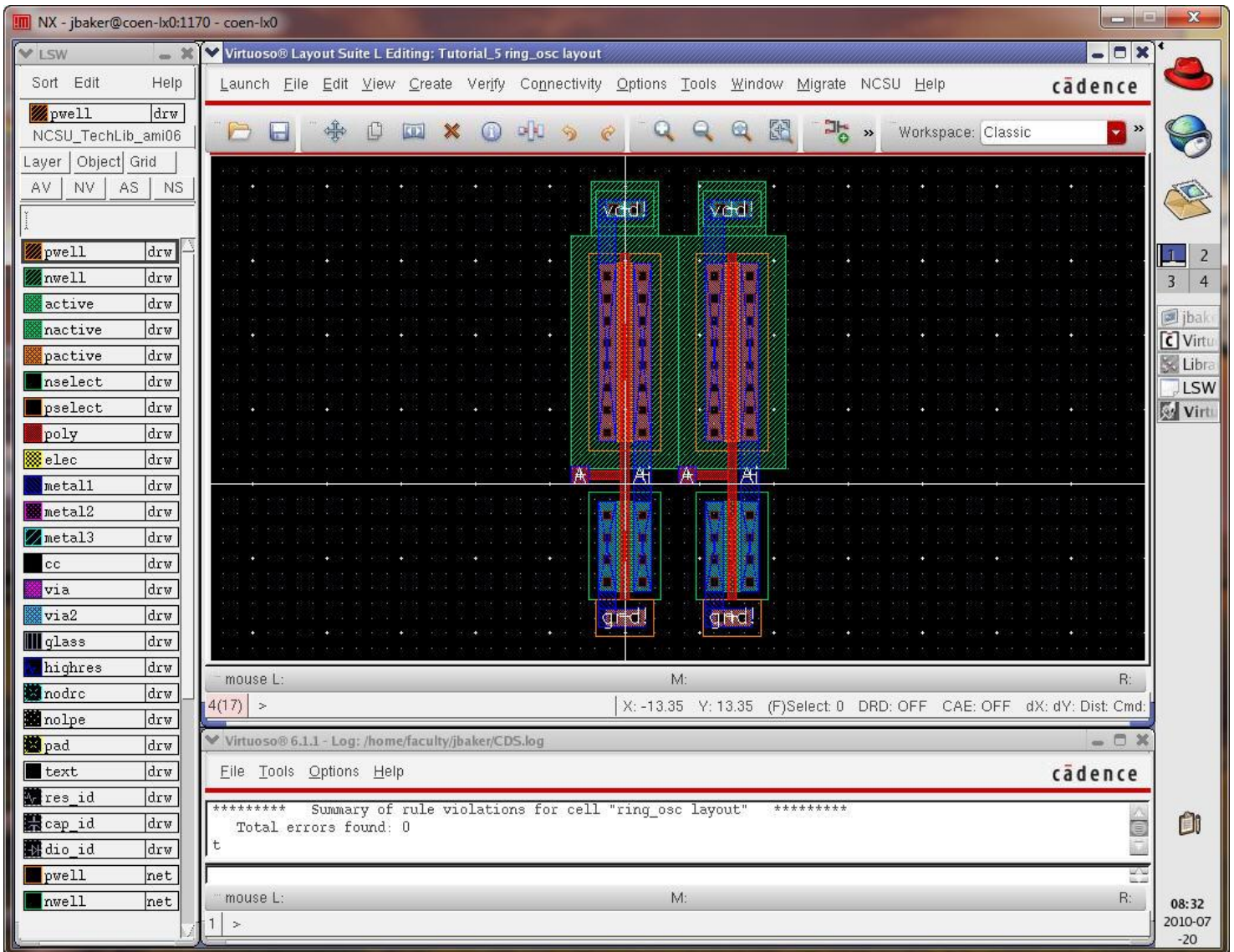


The input of IO<1> is osc\_out and its output is out<1>  
 The input of IO<2> is out<1> and its output is out<2>  
 The input of IO<3> is out<2> and its output is out<3>  
 The input of IO<31> is out<30> and its output is osc\_out

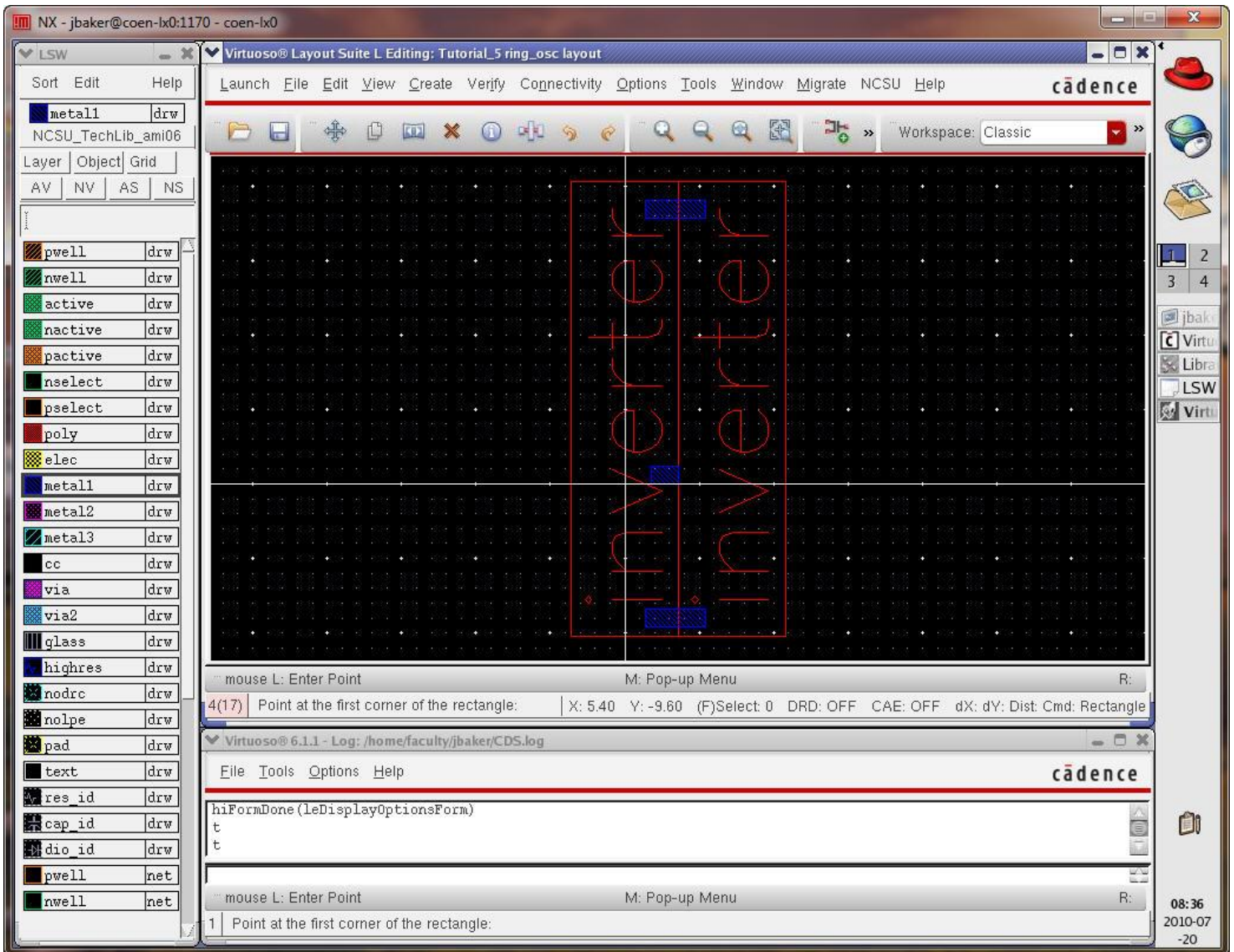
The schematic is exactly the same as the one we drew earlier but clearly nicer to look at (more concise).  
 Re-simulating this ring oscillator gives the exact same results as seen above.

Save and close all cell views.

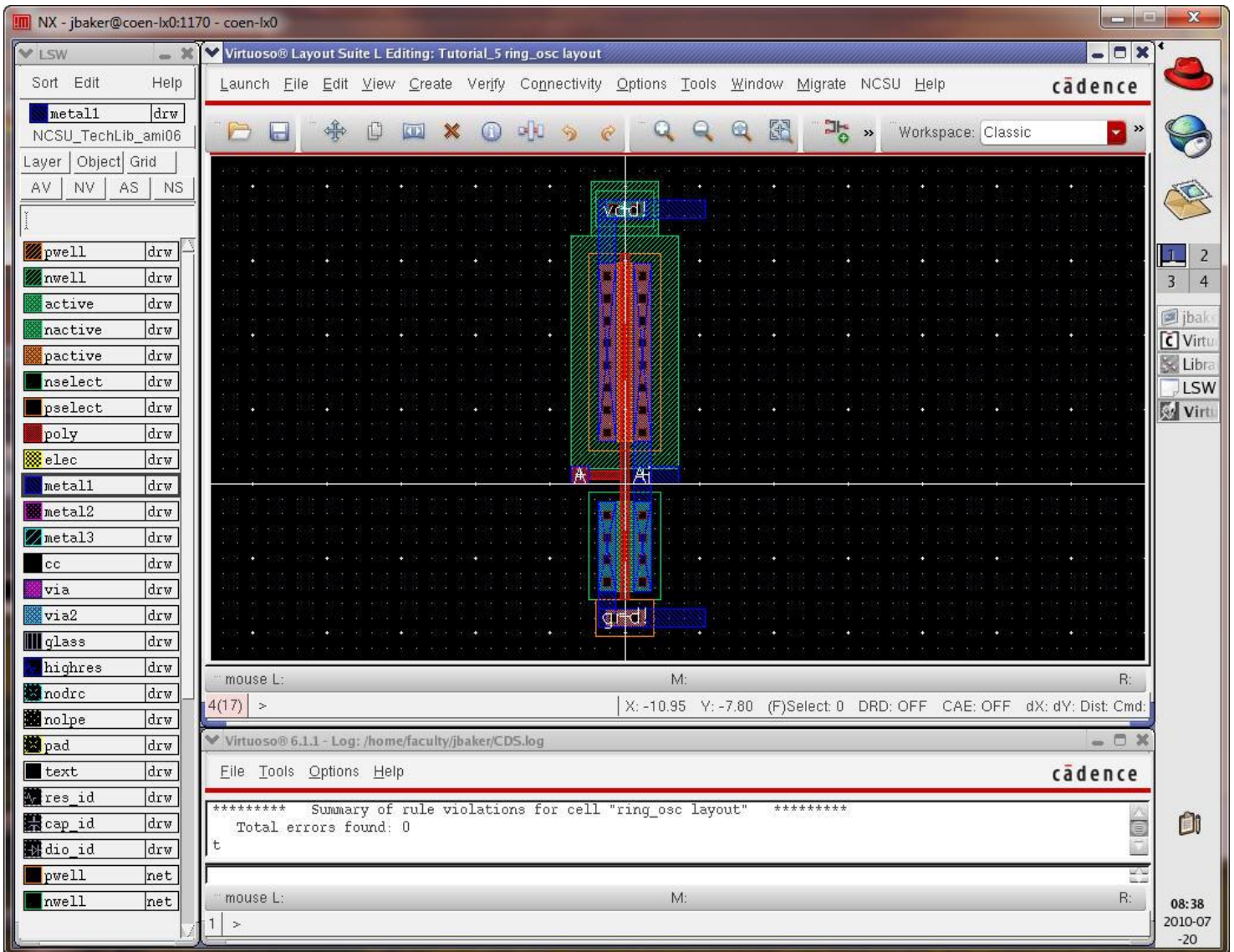
Create layout view for the ring oscillator and place two inverter layouts in the cell next to each other.  
 DRC the layout.



Add rectangles of metal between vdd!, Ai of the first inverter and A of the second inverter, and gnd! as seen below (where **e** was pressed and the stop display level was set to 0 to hide the layout of the inverter).  
DRC the layout.



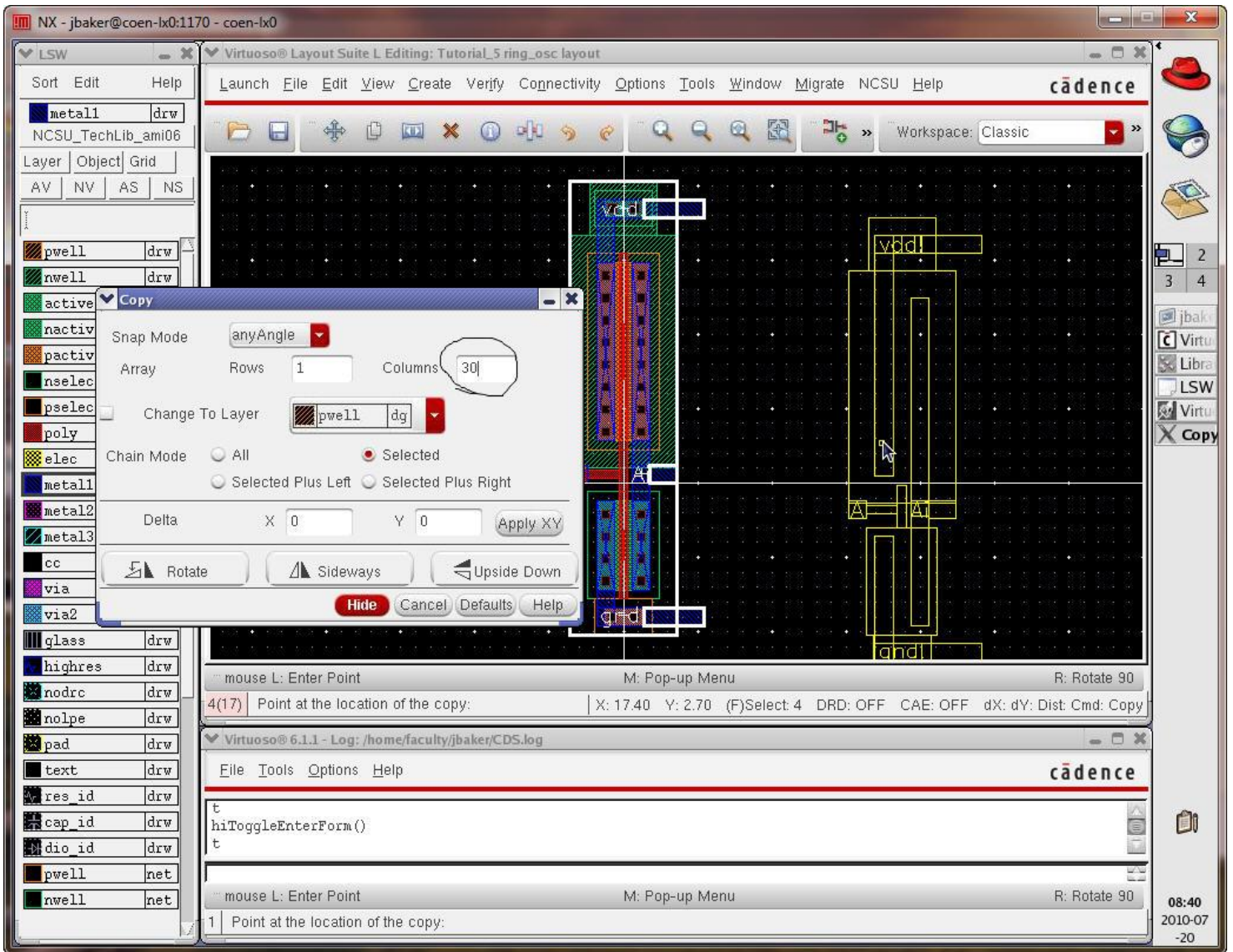
Set the stop display level back to 10 and delete the right inverter.



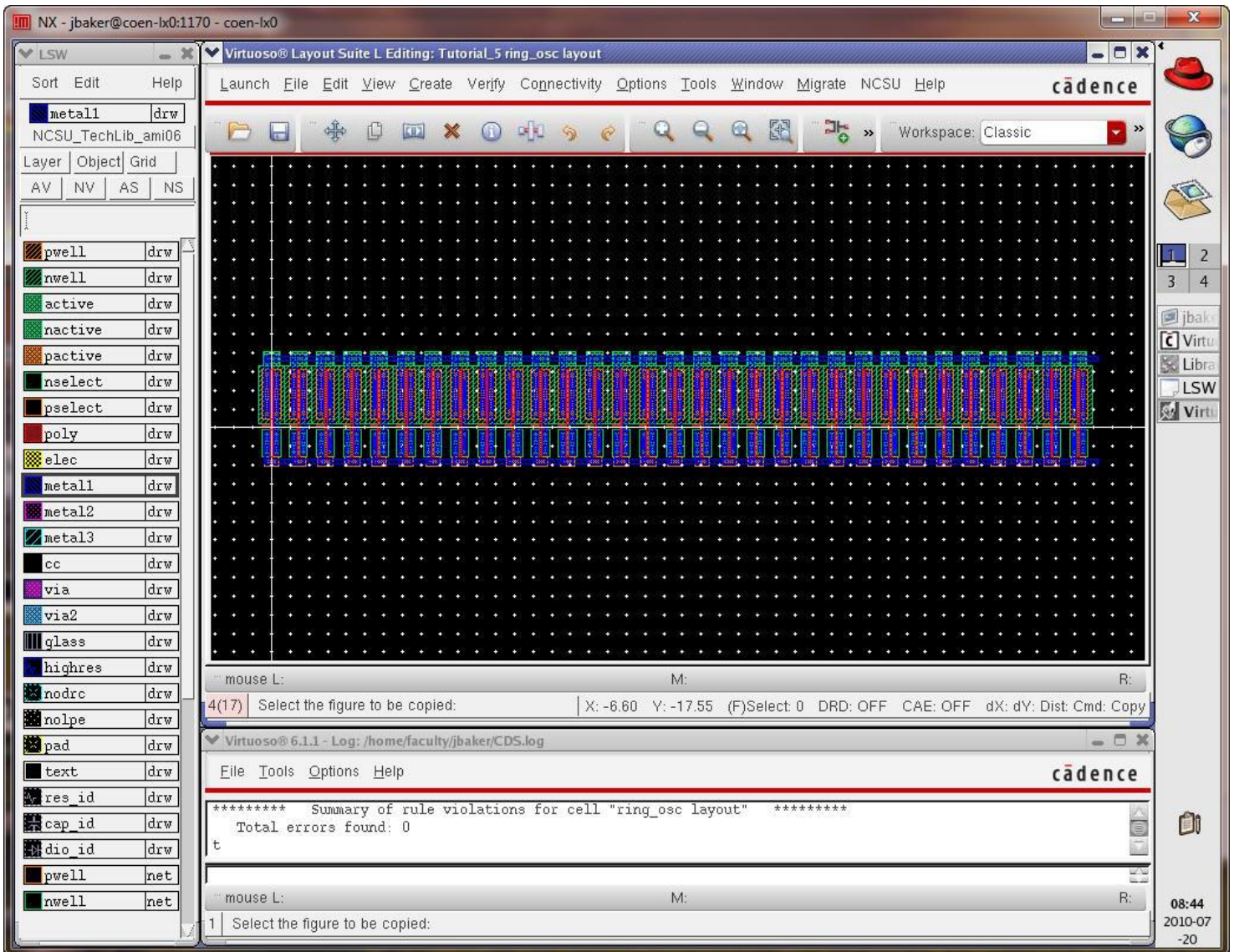
Next select press c (to copy) and select the entire layout.

Press F3, special options, and set the number of columns to 30 (as was done above).

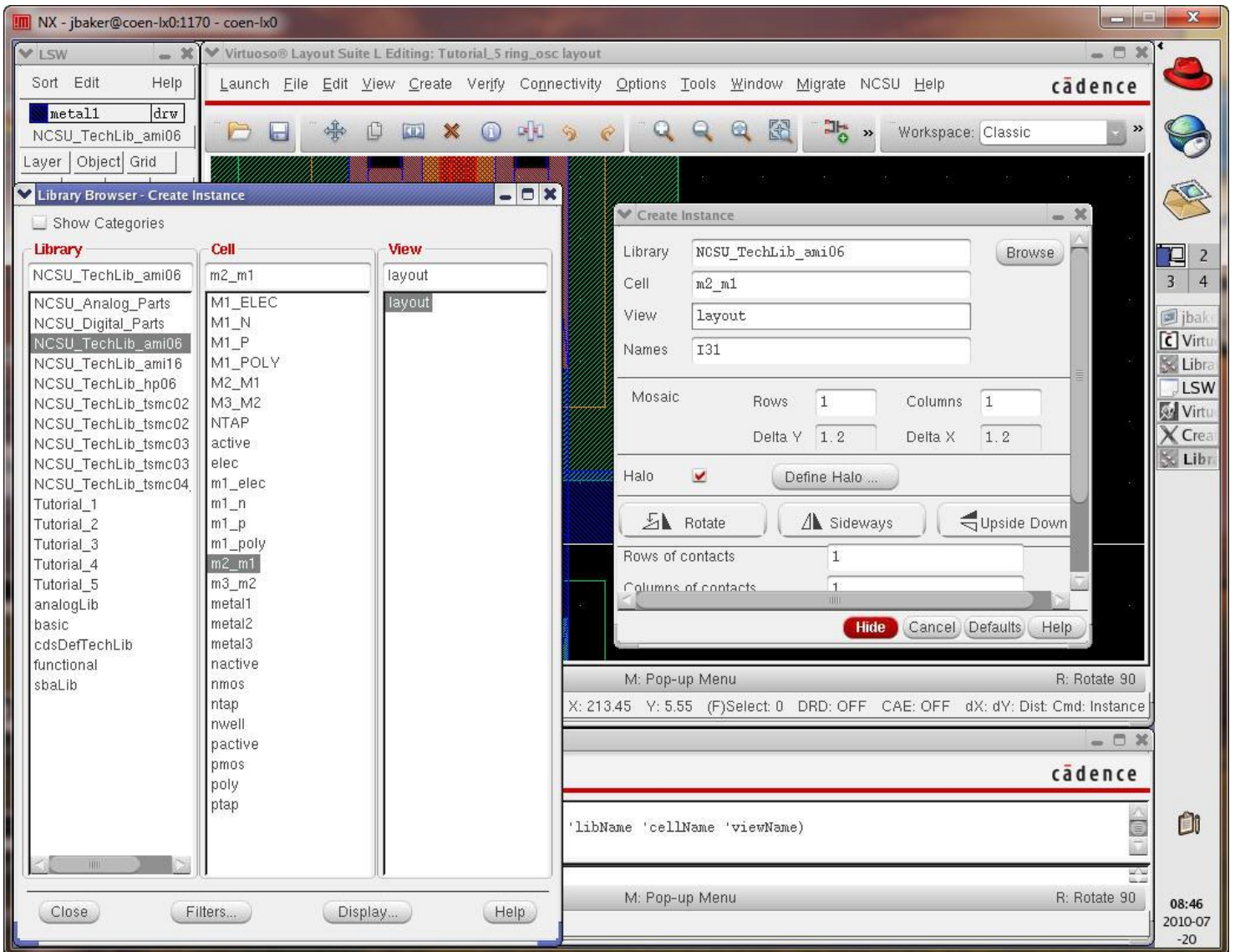




Place the inverters end-to-end as seen below.  
DRC the layout

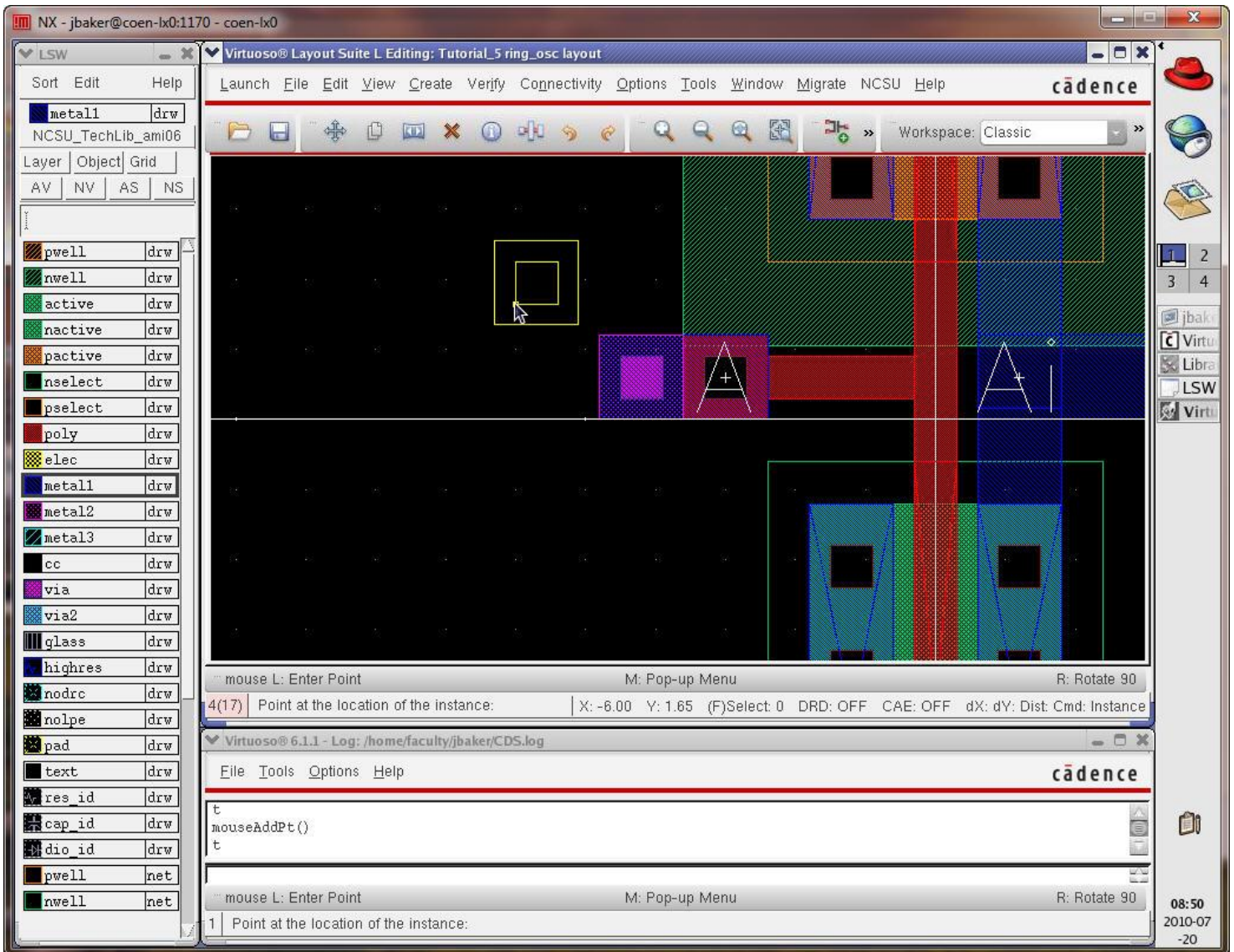


Next add m2\_m1 vias at the left and right of the layout as seen below.

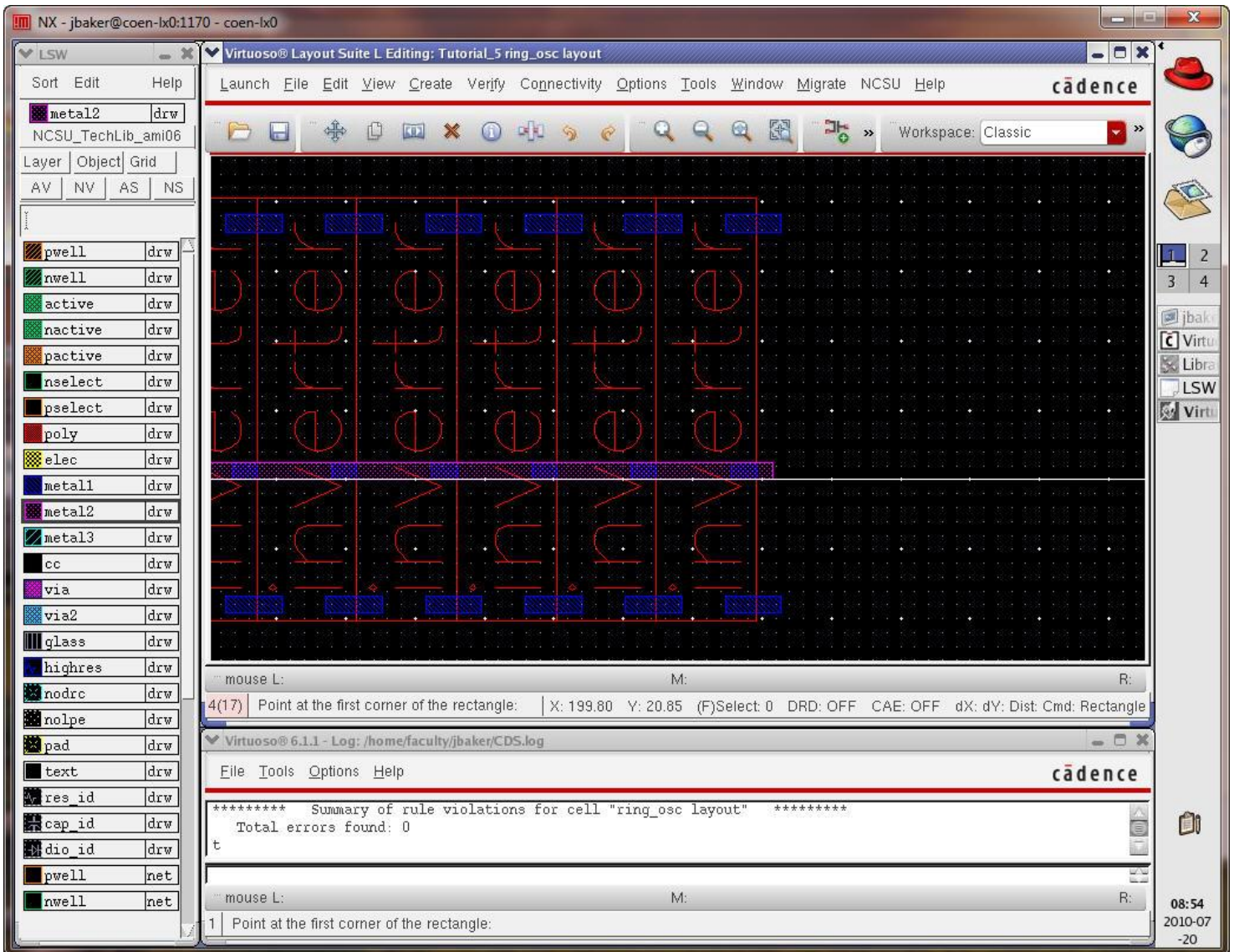


The screenshot displays the Cadence Virtuoso Layout Suite L Editing environment. The main window shows a circuit layout with various layers and components. The left sidebar contains a layer list with items like 'metall1', 'nwell', 'active', etc. The top menu bar includes 'Launch', 'File', 'Edit', 'View', 'Create', 'Verify', 'Connectivity', 'Options', 'Tools', 'Window', 'Migrate', 'NCSU', and 'Help'. The workspace is titled 'Workspace: Classic'. The bottom status bar shows 'mouse L: Enter Point', 'M: Pop-up Menu', and 'R: Rotate 90'. The command console at the bottom displays the following text:

```
Virtuoso@ 6.1.1 - Log: /home/faculty/jbaker/CDS.log  
File Tools Options Help  
cadence  
t  
mouseAddPt()  
t  
mouse L: Enter Point M: Pop-up Menu R: Rotate 90  
1 Point at the location of the instance:
```



Next add a rectangle on metal2 connecting these two vias.  
Below is the result where the stop display level is set to 0.  
DRC the layout.



Add pins for gnd!, vdd! (both have a direction of inputOutput), and osc\_out (set the direction to output). Put vdd! and gnd! pins on the metal1 layer and osc\_out on the metal2 layer.

NX - j baker@coen-ix0:1170 - coen-ix0

Virtuoso® Layout Suite L Editing: Tutorial\_5\_ring\_osc layout

Sort Edit Help

metal1 drw  
NCSU\_TechLib\_ami06

Layer Object Grid  
AV NV AS NS

Layer Object Grid  
AV NV AS NS

Terminal Names vdd1

Keep First Name X Pitch 0 Y Pitch 0

Display Pin Name Display Pin Name Option...

As ROD Object

ROD Name rect0

Mode  rectangle  dot  polygon  circle  auto pin

I/O Type  input  output  inputOutput  switch  jumper

Snap Mode orthogonal

Access Direction  Top  Bottom  Left  Right  Any  None

Hide Cancel Help

mouse L: M: R:

4(17) Use the options form to enter a valid terminal name: | X: 210.15 Y: -7.50 (F)Select: 0 DRD: OFF CAE: OFF dX: dY: Dist: Cmd: Pin

Virtuoso® 6.1.1 - Log: /home/faculty/jbaker/CDS.log

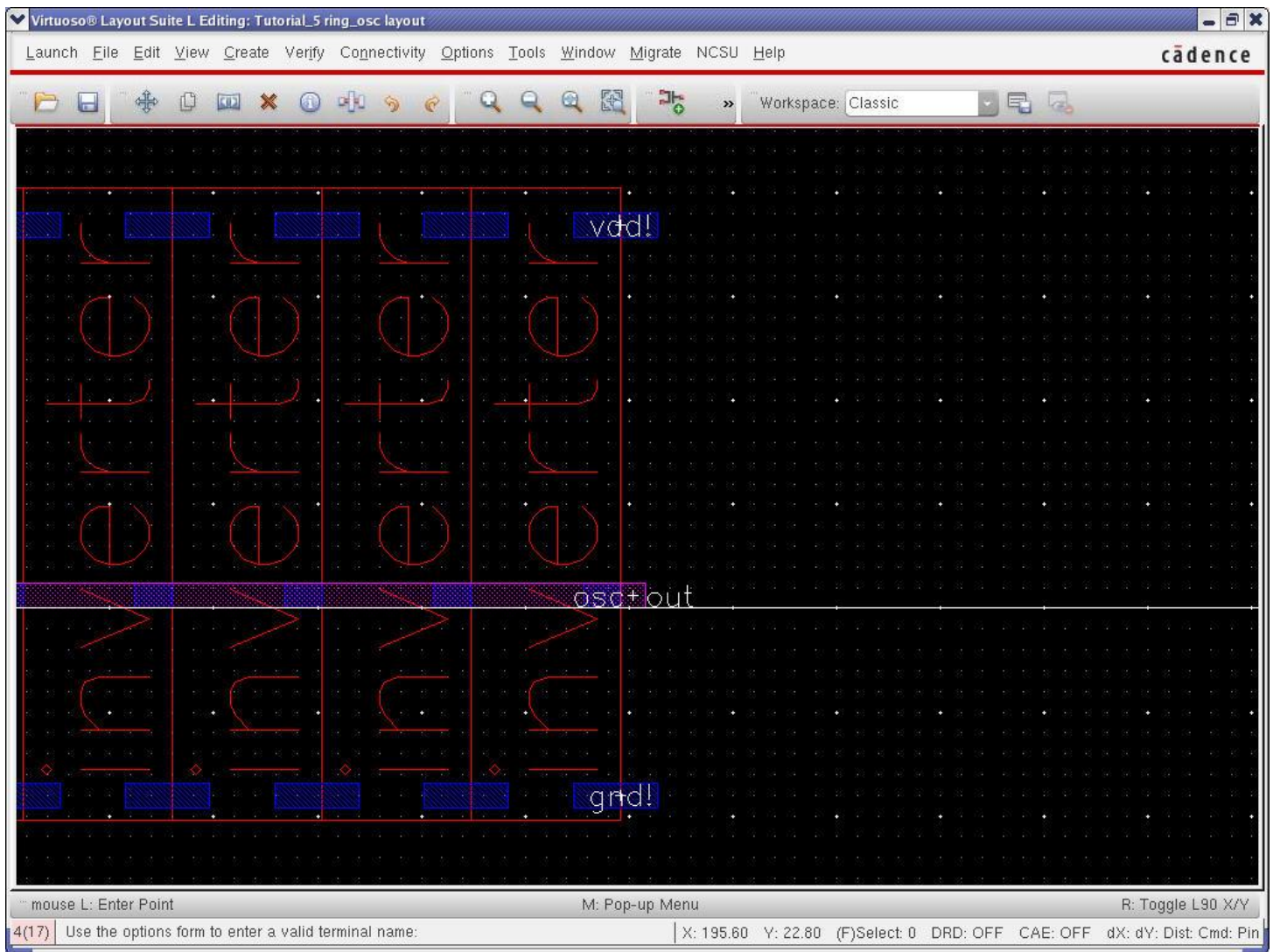
File Tools Options Help

lePinForm->createPinLabel->value= t  
t

mouse L: M: R:

1 Use the options form to enter a valid terminal name:

09:04  
2010-07  
-20



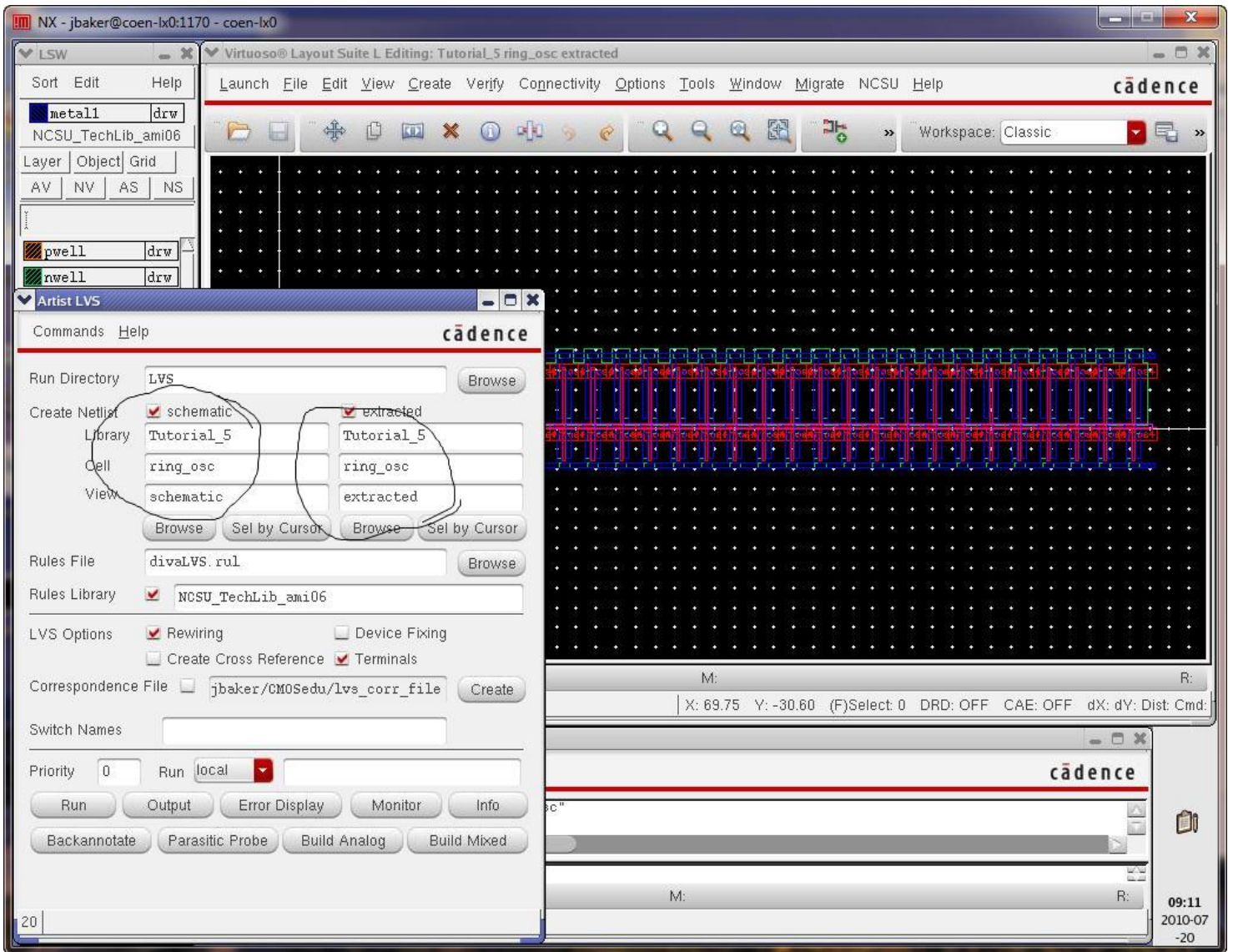
DRC the layout.

Run extraction on the layout.

Save and close the layout view.

Open the extracted view and run an LVS.





The LVS fails.

Devices in the rules but not in the netlist:  
cap nfet pfet nmos4 pmos4

1 net-list ambiguity was resolved by random selection.

The net-lists failed to match.

|                            | layout | schematic |
|----------------------------|--------|-----------|
| instances                  |        |           |
| un-matched                 | 0      | 0         |
| rewired                    | 0      | 0         |
| size errors                | 0      | 0         |
| pruned                     | 0      | 0         |
| active                     | 62     | 62        |
| total                      | 62     | 62        |
| nets                       |        |           |
| un-matched                 | 0      | 0         |
| merged                     | 0      | 0         |
| pruned                     | 0      | 0         |
| active                     | 33     | 33        |
| total                      | 33     | 33        |
| terminals                  |        |           |
| un-matched                 | 1      | 0         |
| matched but different type | 0      | 0         |
| total                      | 3      | 2         |

Probe files from /home/faculty/jbaker/CMOSedu/LVS/schematic  
devbad.out:

21

Priority 0 Run local

Run Output Error Display Monitor Info

Backannotate Parasitic Probe Build Analog Build Mixed

20

09:14  
2010-07  
-20

Why? Looking at the information in si.out file above we see that terminals are not matched.

We used a pin for osc\_out in the layout but not in the schematic.

Let's add a pin to the schematic (and then Check and Save).

Make sure that the pin's direction is output (so it matches the layout).

Also note that the wire connection between the pin and the bus (wide wire) must be labeled as seen.

The screenshot displays the Cadence Virtuoso Schematic Editor interface. The main window shows a schematic diagram of a ring oscillator. The schematic includes a power supply labeled 'vdd', an inverter component labeled 'I0<1:31>', and two delay elements labeled 'osc\_out,out<1:30>' and 'out<1:30>,osc\_out'. The output of the second delay element is labeled 'osc\_out'. The interface also shows the LSW (Layer Set) window on the left, which lists various layers such as 'metall1', 'NCSU\_TechLib\_ami06', 'pwell', 'nwell', 'active', 'nactive', 'pactive', 'nselect', 'pselect', 'poly', 'elec', 'metal1', 'metal2', 'metal3', 'cc', 'via', 'via2', 'glass', 'highres', 'nodrc', 'nolpe', 'pad', 'text', 'res\_id', 'cap\_id', 'dio\_id', 'pwell', and 'nwell'. The bottom window shows the Virtuoso 6.1.1 Log, which contains the message: '"Tutorial\_5 ring\_osc schematic" saved.'

Check and Save the schematic.

Close the schematic and open the ring\_oscillator's extracted view.

Run the LVS to see that the layout and schematic match.

The screenshot shows the Cadence LVS tool interface. The main window displays the following text:

```

@(#)SCDS: LVS.exe version 6.1.1 10/23/2007 02:12 (cds126047) $
Command line: /usr/local/Cadence/IC610/tools.lnx86/dfII/bin/32bit/LVS.exe -dir /home/faculty/jbaker/CMOSedu/LVS -l -s -t /ho
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

Net-list summary for /home/faculty/jbaker/CMOSedu/LVS/layout/netlist
count
33      nets
3       terminals
31      pmos
31      rmos

Net-list summary for /home/faculty/jbaker/CMOSedu/LVS/schematic/netlist
count
33      nets
3       terminals
31      pmos
31      rmos

Terminal correspondence points
N30     N1      gnd!
N32     N33     osc_out
N31     N0      vdd!

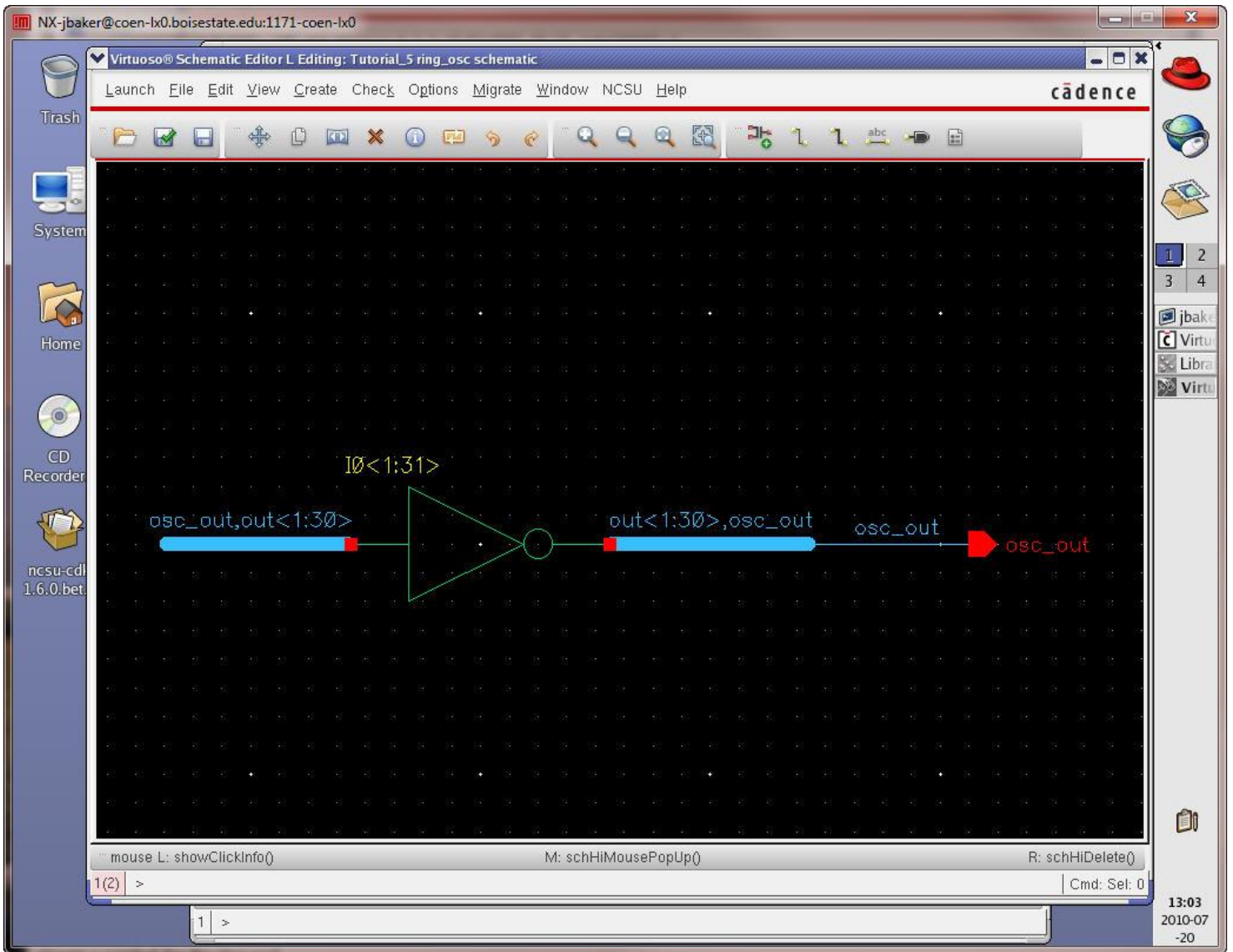
Devices in the rules but not in the netlist:
cap nfet pfet rmos4 pmos4

The net-lists match.
  
```

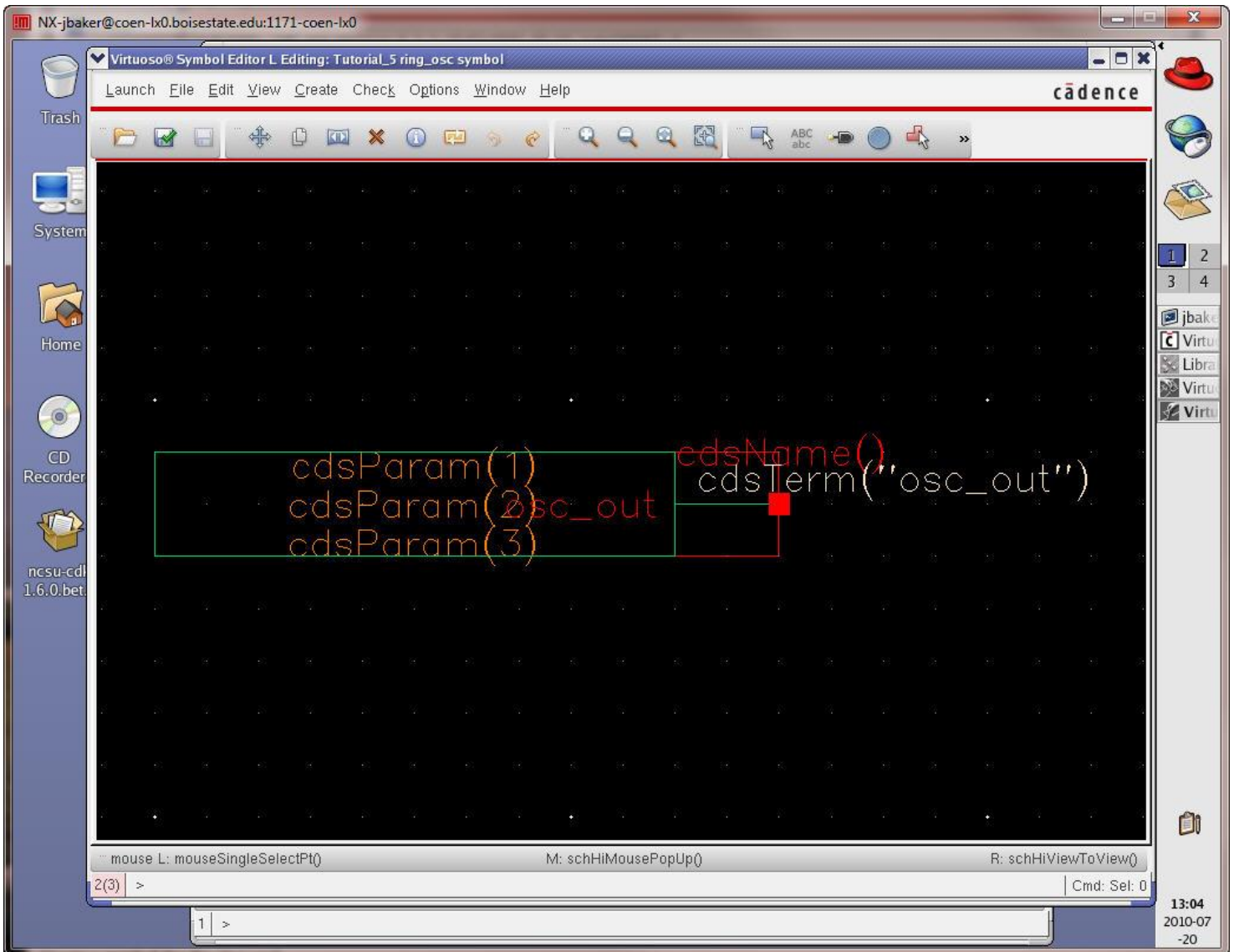
The interface also shows a left-hand menu with options like 'Run Directory', 'Create Netlist', 'Library', 'Cell', 'View', 'Rules File', 'Rules Library', 'LVS Options', and 'Correspondence F'. At the bottom, there are buttons for 'Run', 'Output', 'Error Display', 'Monitor', 'Info', 'Backannotate', 'Parasitic Probe', 'Build Analog', and 'Build Mixed'. The status bar at the bottom right shows the time '09:24' and date '2010-07-20'.

It's useful to compare the simulation results of both a layout and a schematic.

Delete the vdd symbol in the ring oscillator schematic.



Create a symbol for the ring oscillator.



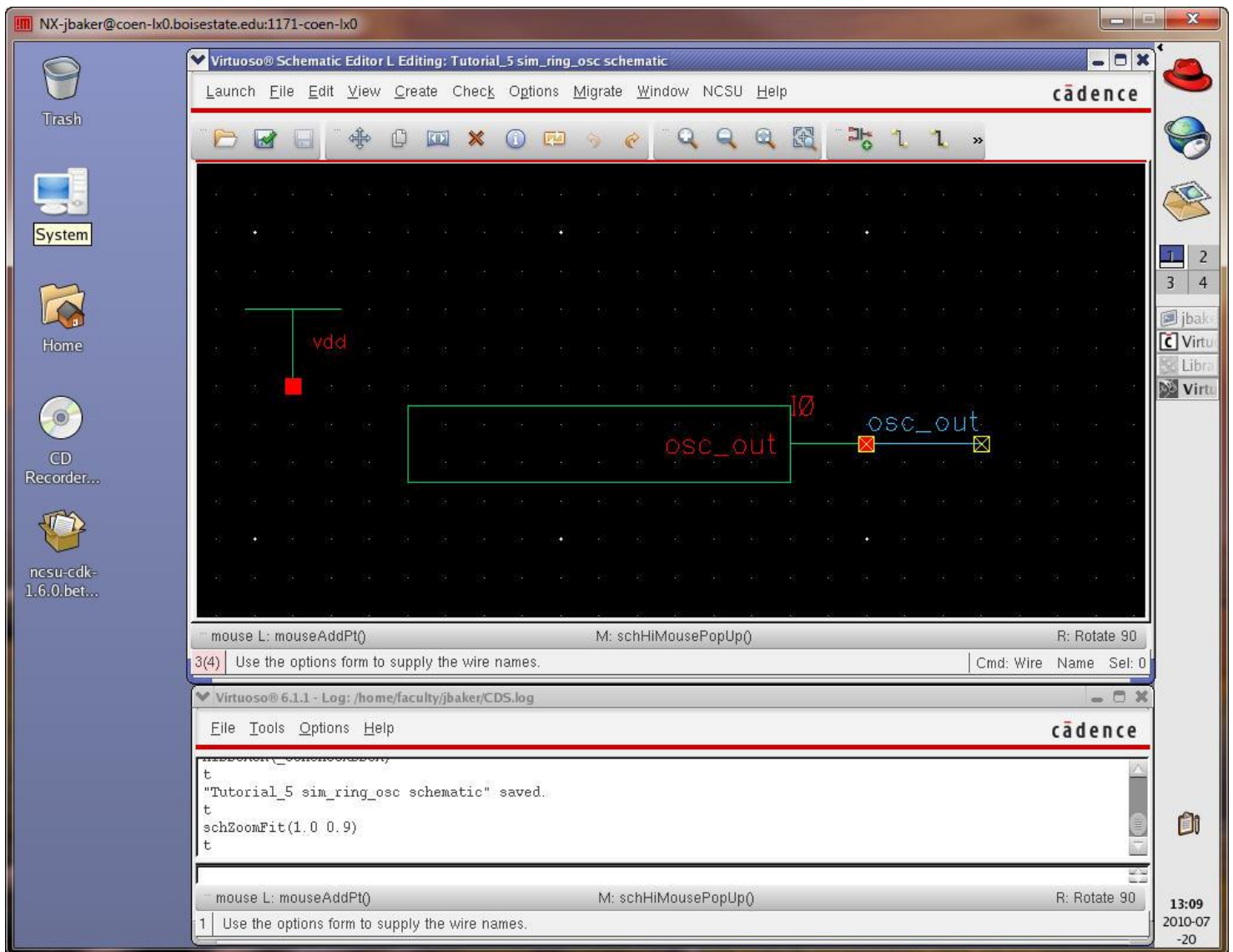
Save and close all cell views.

Create a new schematic cell view call `sim_ring_osc`.

Please the `ring_osc` and `vdd` symbols in this cell.

Add a wire to the output of the `ring_osc` symbol labeled `osc_out` as seen below.

Check and Save the schematic.



We get two warnings (floating net/wire)

Use Check -> Find Markers then press ignore twice and close the window.

Check and Save again to verify no warnings/errors.

Launch the ADE and enter the models, stimuli, outputs to plot, etc. as we did above.

Don't forget to set the osc\_out to have an initial condition of 0.

When finished save the state.

Netlist and Run (hit the green button) to see the following.

The screenshot displays the Cadence Virtuoso Analog Design Environment. The main window shows the simulation results for a transient analysis. The results are presented in a table format, showing time, percentage of total time, and step size for each step. The simulation parameters and timing information are also displayed below the table.

| tran: time | (%)    | step     | (m%)    |
|------------|--------|----------|---------|
| 15.01 ns   | 7.51 % | 18.76 ps | 9.38 m% |
| 25 ns      | 12.5 % | 15.83 ps | 7.91 m% |
| 35.01 ns   | 17.5 % | 16.34 ps | 8.17 m% |
| 45 ns      | 22.5 % | 16.36 ps | 8.18 m% |
| 55.01 ns   | 27.5 % | 18.53 ps | 9.26 m% |
| 65.01 ns   | 32.5 % | 15.88 ps | 7.94 m% |
| 75.01 ns   | 37.5 % | 20.92 ps | 10.5 m% |
| 85.01 ns   | 42.5 % | 18.5 ps  | 9.25 m% |
| 95.01 ns   | 47.5 % | 17.41 ps | 8.7 m%  |
| 105 ns     | 52.5 % | 18.76 ps | 9.38 m% |
| 115 ns     | 57.5 % | 15.83 ps | 7.91 m% |
| 125 ns     | 62.5 % | 16.34 ps | 8.17 m% |
| 135 ns     | 67.5 % | 18.28 ps | 9.14 m% |
| 145 ns     | 72.5 % | 18.53 ps | 9.26 m% |
| 155 ns     | 77.5 % | 15.88 ps | 7.94 m% |
| 165 ns     | 82.5 % | 20.92 ps | 10.5 m% |
| 175 ns     | 87.5 % | 18.5 ps  | 9.25 m% |
| 185 ns     | 92.5 % | 17.41 ps | 8.7 m%  |
| 195 ns     | 97.5 % | 18.76 ps | 9.38 m% |

Number of accepted tran steps = 11312.  
 Accumulated tran full load time = 2.88 s.  
 Accumulated tran full component evaluation time = 2.69 s.  
 Accumulated tran full preload time = 120 ms.  
 Accumulated tran full merge time = 0 s.  
 Accumulated tran residue-only load time = 1.72 s.  
 Accumulated tran residue-only component evaluation time = 1.  
 Accumulated tran residue-only preload time = 40 ms.  
 Accumulated tran residue-only merge time = 20 ms.  
 Accumulated tran factor time = 60 ms.  
 Accumulated tran solve time = 80 ms.  
 Accumulated tran output time = 320 ms.  
 Initial condition solution time = 10 ms.  
 Intrinsic tran analysis time = 5.56 s.  
 Total time required for tran analysis 'tran' was 5.58 s.

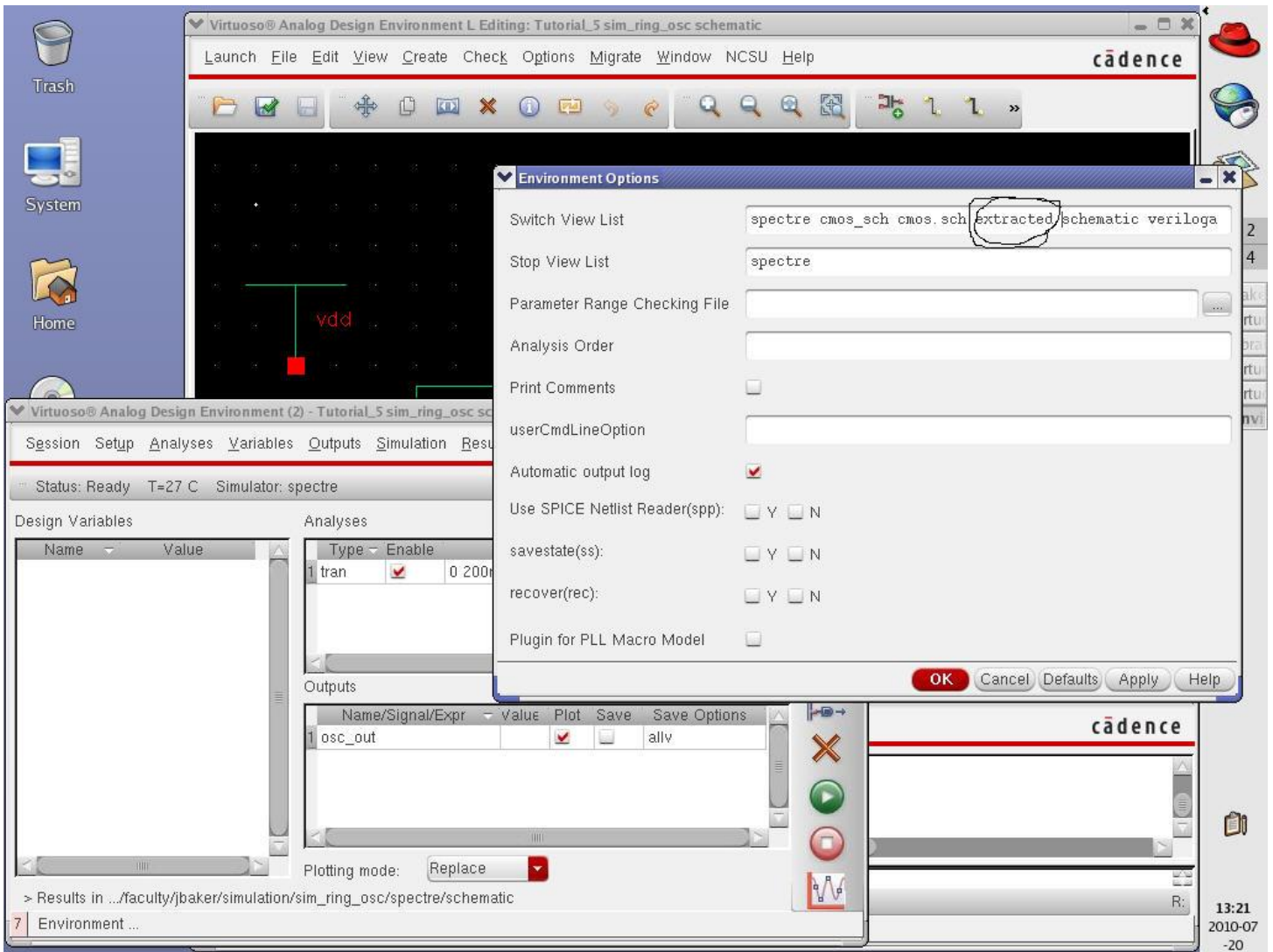
finalTimeOP: writing operating point information to rawfile.  
 modelParameter: writing model parameter values to rawfile.  
 element: writing instance parameter values to rawfile.  
 outputParameter: writing output parameter values to rawfile.  
 designParamVals: writing netlist parameters to rawfile.  
 primitives: writing primitives to rawfile.  
 subckts: writing subcircuits to rawfile.

The right-hand window shows a transient response plot for the signal `/osc_out`. The plot displays a square wave signal oscillating between approximately -1 V and 6 V over a time period of 0 to 200 ns. The signal is labeled `V(N)` on the y-axis and `time (ns)` on the x-axis.

Let's simulate the extracted view.

As before use Setup -> Environment to enter extracted before schematic.





To get the following results.

The screenshot displays the Cadence Virtuoso Analog Design Environment interface. The main window shows the simulation results for a transient analysis. The results are presented in a table format, showing the time, percentage of total time, and step size for each step. The simulation parameters are as follows:

| tran: time | (%)    | step     | (m%)    |
|------------|--------|----------|---------|
| 15 ns      | 7.5 %  | 16.86 ps | 8.43 m% |
| 25.01 ns   | 12.5 % | 18.26 ps | 9.13 m% |
| 35.01 ns   | 17.5 % | 15.08 ps | 7.54 m% |
| 45.02 ns   | 22.5 % | 16.58 ps | 8.29 m% |
| 55.01 ns   | 27.5 % | 15.76 ps | 7.88 m% |
| 65.01 ns   | 32.5 % | 14.06 ps | 7.03 m% |
| 75.01 ns   | 37.5 % | 15.19 ps | 7.59 m% |
| 85.01 ns   | 42.5 % | 16.27 ps | 8.13 m% |
| 95 ns      | 47.5 % | 16.02 ps | 8.01 m% |
| 105 ns     | 52.5 % | 14.45 ps | 7.22 m% |
| 115 ns     | 57.5 % | 23.07 ps | 11.5 m% |
| 125 ns     | 62.5 % | 18.26 ps | 9.13 m% |
| 135 ns     | 67.5 % | 15.08 ps | 7.54 m% |
| 145 ns     | 72.5 % | 16.58 ps | 8.29 m% |
| 155 ns     | 77.5 % | 16.27 ps | 8.13 m% |
| 165 ns     | 82.5 % | 16.02 ps | 8.01 m% |
| 175 ns     | 87.5 % | 15.19 ps | 7.59 m% |
| 185 ns     | 92.5 % | 23.07 ps | 11.5 m% |
| 195 ns     | 97.5 % | 18.26 ps | 9.13 m% |

Summary statistics for the simulation:

- Number of accepted tran steps = 12143.
- Accumulated tran full load time = 3.28 s.
- Accumulated tran full component evaluation time = 3.07 s.
- Accumulated tran full preload time = 110 ms.
- Accumulated tran full merge time = 30 ms.
- Accumulated tran residue-only load time = 1.75 s.
- Accumulated tran residue-only component evaluation time = 1.
- Accumulated tran residue-only preload time = 50 ms.
- Accumulated tran residue-only merge time = 10 ms.
- Accumulated tran factor time = 90 ms.
- Accumulated tran solve time = 120 ms.
- Accumulated tran output time = 290 ms.
- Initial condition solution time = 10 ms.
- Intrinsic tran analysis time = 5.91 s.
- Total time required for tran analysis 'tran' was 5.92 s.

The simulation also includes the following output files:

- finalTimeOP: writing operating point information to rawfile.
- modelParameter: writing model parameter values to rawfile.
- element: writing instance parameter values to rawfile.
- outputParameter: writing output parameter values to rawfile.
- designParamVals: writing netlist parameters to rawfile.
- primitives: writing primitives to rawfile.
- subckts: writing subcircuits to rawfile.

The right-hand side of the window shows a plot titled "Transient Response" for the signal "/osc\_out". The plot displays a square wave signal with a period of approximately 100 ns, oscillating between approximately -1 V and 6 V. The x-axis is labeled "time (ns)" and ranges from 0 to 200. The y-axis is labeled "V (V)" and ranges from -1 to 6.

Just to verify that we are actually using the extracted cell view use Simulations -> Netlist -> Display

The screenshot displays the Cadence Virtuoso Analog Design Environment. The main window shows a netlist editor with the following content:

```
// Generated for: spectre
// Generated on: Jul 20 13:21:25 2010
// Design library name: Tutorial_5
// Design cell name: sim_ring_osc
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
include "/home/faculty/jbaker/ncsu-cdk-1.6.0.beta/models/spectre/stand
include "/home/faculty/jbaker/ncsu-cdk-1.6.0.beta/models/spectre/stand

// Library name: Tutorial_5
// Cell name: ring_osc
// View name: extracted
subckt ring_osc_extracted_osc_out
 \+61 (osc_out 33 vdd! vdd!) ami06P w=1.2e-05 l=6e-07 as=1.8e-11 \
 ad=1.8e-11 ps=1.5e-05 pd=1.5e-05 m=1 region=sat
 \+60 (33 32 vdd! vdd!) ami06P w=1.2e-05 l=6e-07 as=1.8e-11 ad=1.8e
 ps=1.5e-05 pd=1.5e-05 m=1 region=sat
 \+59 (32 31 vdd! vdd!) ami06P w=1.2e-05 l=6e-07 as=1.8e-11 ad=1.8e
 ps=1.5e-05 pd=1.5e-05 m=1 region=sat
 \+58 (31 30 vdd! vdd!) ami06P w=1.2e-05 l=6e-07 as=1.8e-11 ad=1.8e
 ps=1.5e-05 pd=1.5e-05 m=1 region=sat
 \+57 (30 29 vdd! vdd!) ami06P w=1.2e-05 l=6e-07 as=1.8e-11 ad=1.8e
 ps=1.5e-05 pd=1.5e-05 m=1 region=sat
 \+56 (29 28 vdd! vdd!) ami06P w=1.2e-05 l=6e-07 as=1.8e-11 ad=1.8e
 ps=1.5e-05 pd=1.5e-05 m=1 region=sat
 \+55 (28 27 vdd! vdd!) ami06P w=1.2e-05 l=6e-07 as=1.8e-11 ad=1.8e
 ps=1.5e-05 pd=1.5e-05 m=1 region=sat
 \+54 (27 26 vdd! vdd!) ami06P w=1.2e-05 l=6e-07 as=1.8e-11 ad=1.8e
 ps=1.5e-05 pd=1.5e-05 m=1 region=sat
 \+53 (26 25 vdd! vdd!) ami06P w=1.2e-05 l=6e-07 as=1.8e-11 ad=1.8e
 ps=1.5e-05 pd=1.5e-05 m=1 region=sat
 \+52 (25 24 vdd! vdd!) ami06P w=1.2e-05 l=6e-07 as=1.8e-11 ad=1.8e
 ps=1.5e-05 pd=1.5e-05 m=1 region=sat
 \+51 (24 23 vdd! vdd!) ami06P w=1.2e-05 l=6e-07 as=1.8e-11 ad=1.8e
 ps=1.5e-05 pd=1.5e-05 m=1 region=sat
 \+50 (23 22 vdd! vdd!) ami06P w=1.2e-05 l=6e-07 as=1.8e-11 ad=1.8e
 ps=1.5e-05 pd=1.5e-05 m=1 region=sat
 \+49 (22 21 vdd! vdd!) ami06P w=1.2e-05 l=6e-07 as=1.8e-11 ad=1.8e
 ps=1.5e-05 pd=1.5e-05 m=1 region=sat
 \+48 (21 20 vdd! vdd!) ami06P w=1.2e-05 l=6e-07 as=1.8e-11 ad=1.8e
 ps=1.5e-05 pd=1.5e-05 m=1 region=sat
 \+47 (20 19 vdd! vdd!) ami06P w=1.2e-05 l=6e-07 as=1.8e-11 ad=1.8e
```

The simulation window shows a plot of the signal over time, with the x-axis ranging from 150 to 200. The plot displays a periodic waveform, likely a sine wave, with a period of approximately 10 units. The y-axis represents the signal amplitude, ranging from -1 to 1. The plot is titled "Axis Trace Marker Zoom Tools Help" and includes a "Save Options" dialog box with the "allv" option selected.

Save and close everything.

Remember that if you save the simulation state with extracted before schematic (above) changes to the schematic won't appear in the simulation results.

Rather Spectre will continue to simulate the extracted view. To fix this simply remove extracted above.

This concludes Tutorial 5.

For your reference the Tutorial\_5 directory is available in [Tutorial\\_5.zip](#).

[Return](#)

