

[Cadence Design System Tutorials from CMOSedu.com](#) ([Return](#))

Tutorial 3 - Design, layout, and simulation of a CMOS inverter

In this third tutorial we'll draw the schematic, symbol, and layout of a CMOS inverter. We'll also simulate the DC behavior of the inverter.

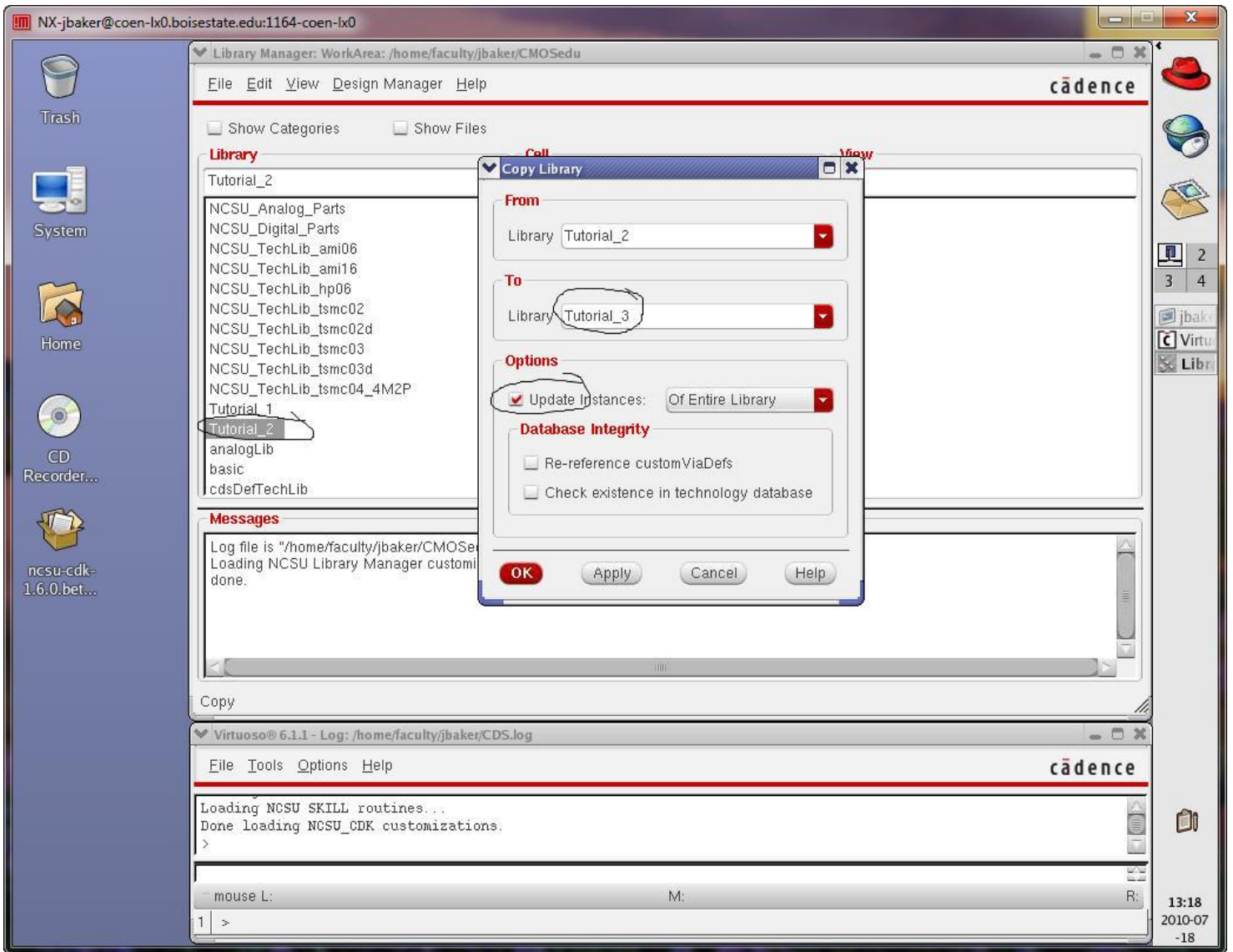
Before we get going with this tutorial please make sure you know the answers to the following questions. If you don't, or the answers don't come to you quickly, then go back through [Tutorial 1](#) and [Tutorial 2](#)

1. What does the Bindkey **q** do?
2. Which two Cell Views are used when doing an LVS?
3. What is the difference between the nmos and nmos4 schematic cells?
4. How do you select the MOSFET models in the ADE window? What does ADE stand for?
5. What is the difference between moving and stretching?
6. How do you layout a rectangle on the metal1 layer?
7. What does the ! indicate at the end of gnd! and vdd!
8. What do the acronyms LSW and CIW stand for?
9. How is the ruler used? Cleared?

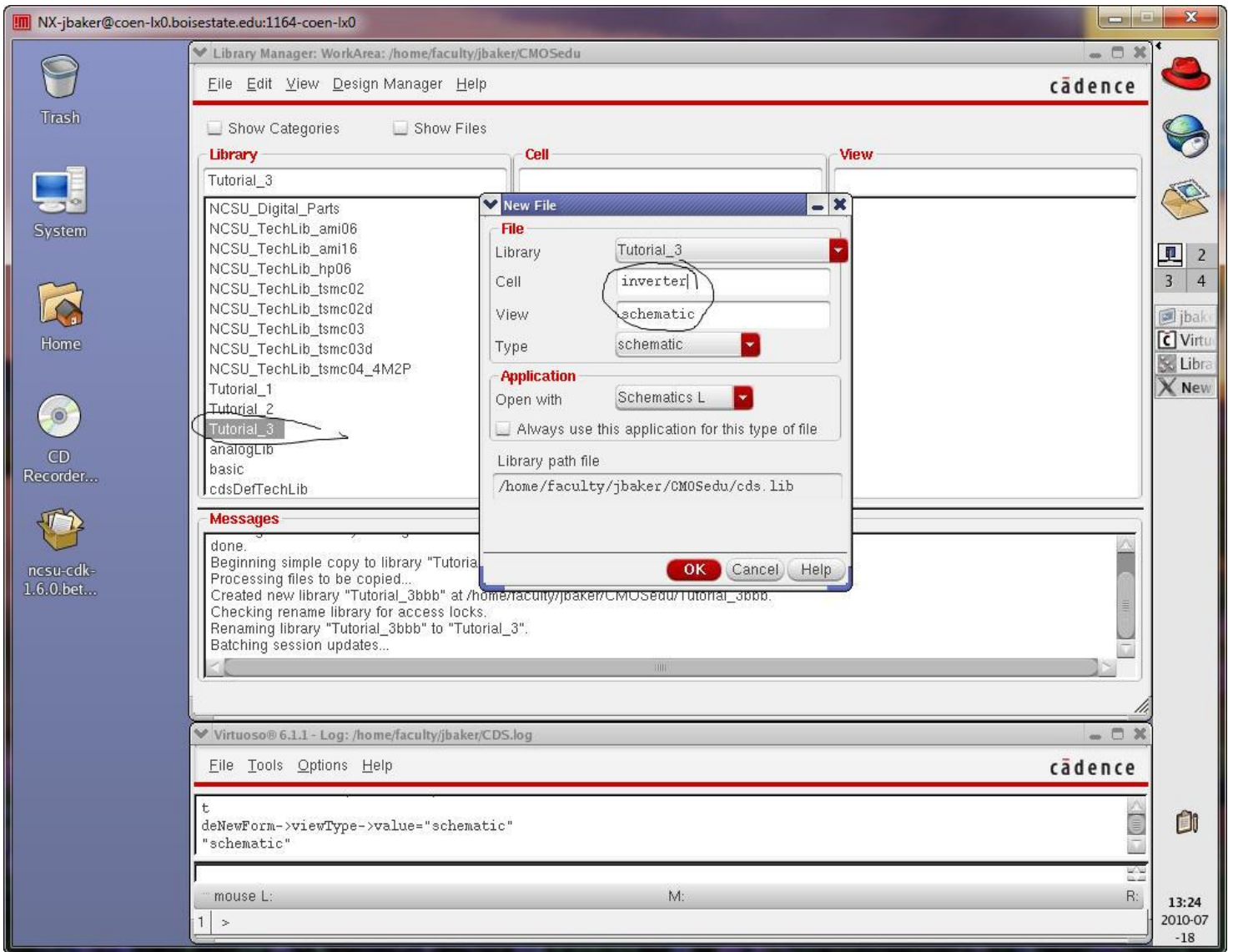
Okay, hopefully these are easy.

Let's start out, assuming Virtuoso has been started in the CMOSedu directory, by copying the Tutorial_2 library to a library named Tutorial_3.

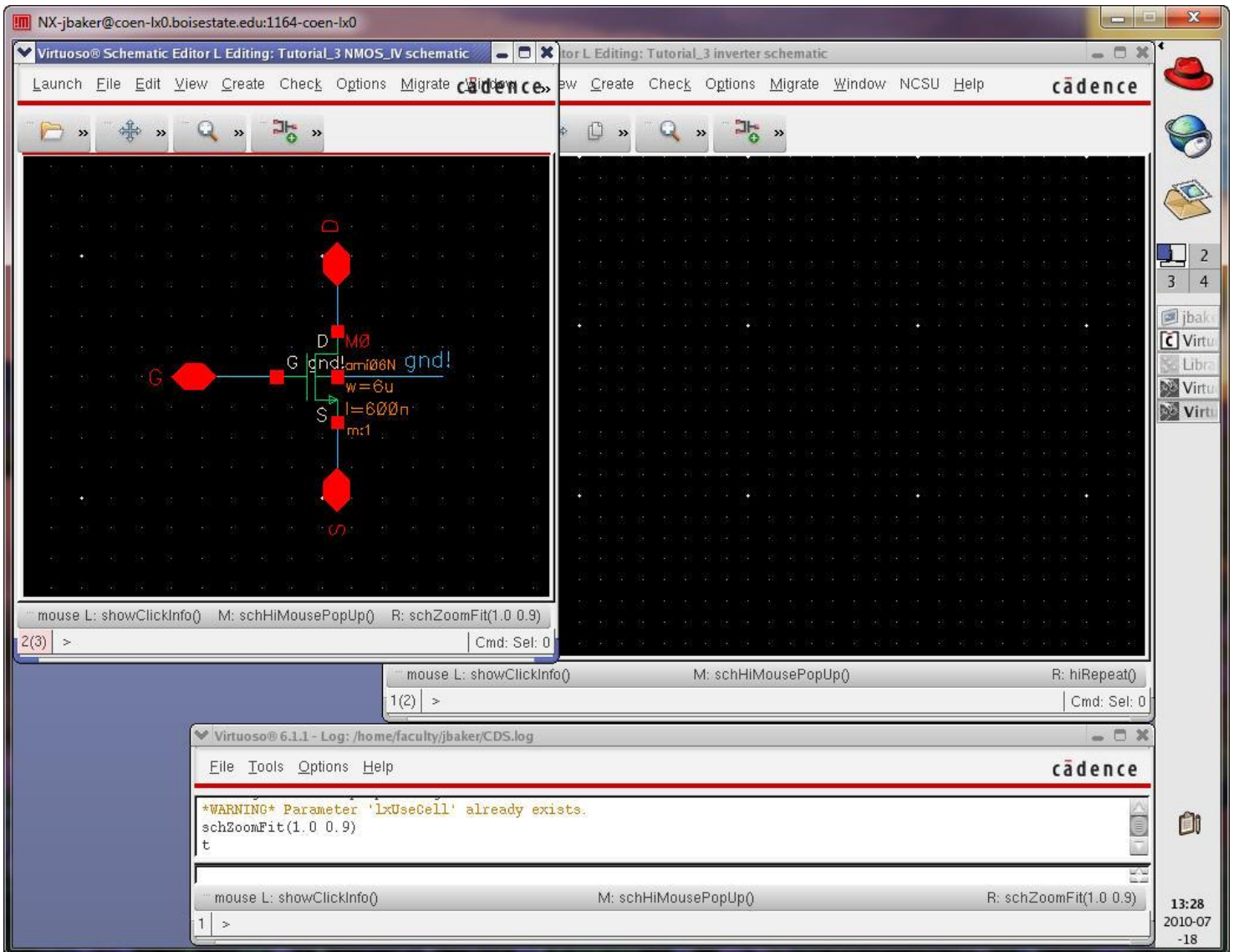
Ensure the new library is placed in \$HOME/CMOSedu



Next create a schematic Cell View called inverter.



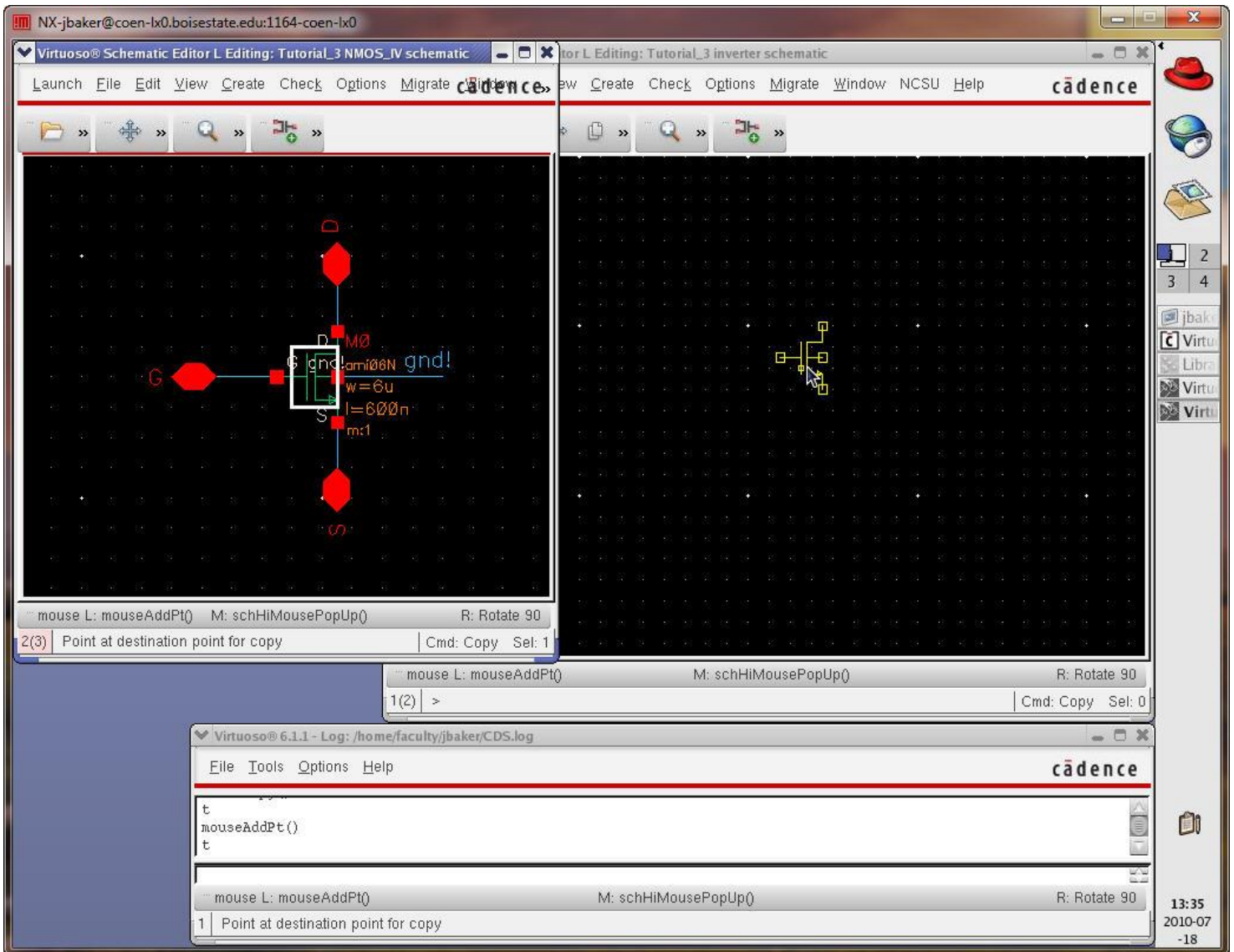
With this new schematic view open also open the schematic view of NMOS_IV as seen below.



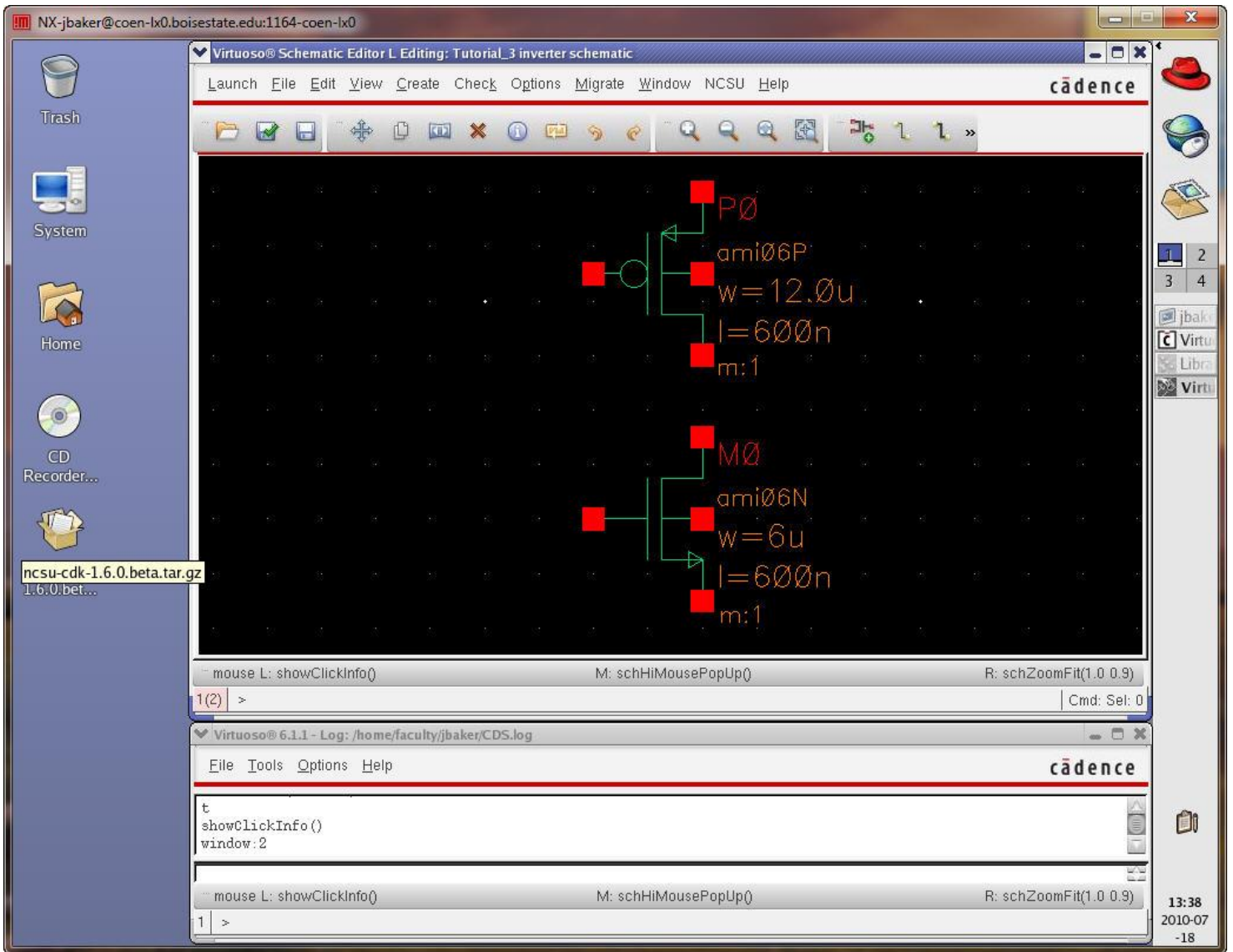
What we are going to do is copy the NMOS symbol from the NMOS_IV cell into the inverter cell.

To do this we need to have both windows open (no clipboard that we can copy items to).

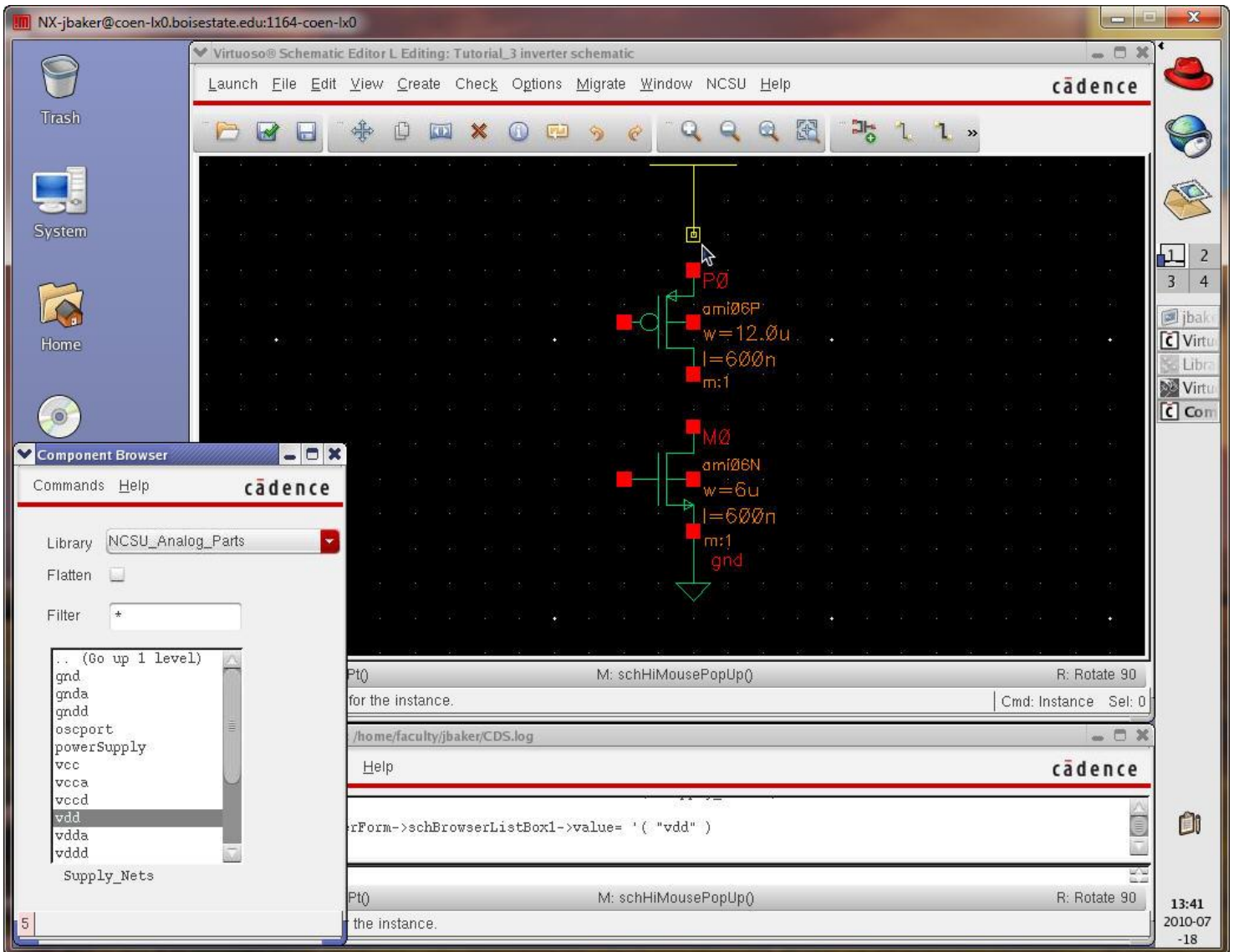
Press the copy Bindkey c (or use the menu) then click on the nmos4 symbol and drag over into the inverter window (and click the left mouse button to instantiate).



Close the NMOS_IV window and open the PMOS_IV window.
Repeat for the pmos4 cell to get the following.



Instantiate vdd and gnd supply nets.



Finally, wire up the inverter and add pins as seen below.
The A pin should have an input direction and pin Ai should have an output direction.

The screenshot displays the Cadence Virtuoso Schematic Editor interface. The main window shows a schematic of an inverter circuit. The input is labeled 'A' and the output is labeled 'Ai'. The circuit consists of a PMOS transistor (P0) and an NMOS transistor (M0) connected in series between 'vdd' and 'gnd'. The PMOS transistor has parameters: $w = 12.0u$, $l = 600n$, and $m = 1$. The NMOS transistor has parameters: $w = 6u$, $l = 600n$, and $m = 1$. The schematic is overlaid on a dark grid background.

Below the schematic, there is a console window titled 'Virtuoso@ 6.1.1 - Log: /home/faculty/jbaker/CDS.log'. The console shows the following text:

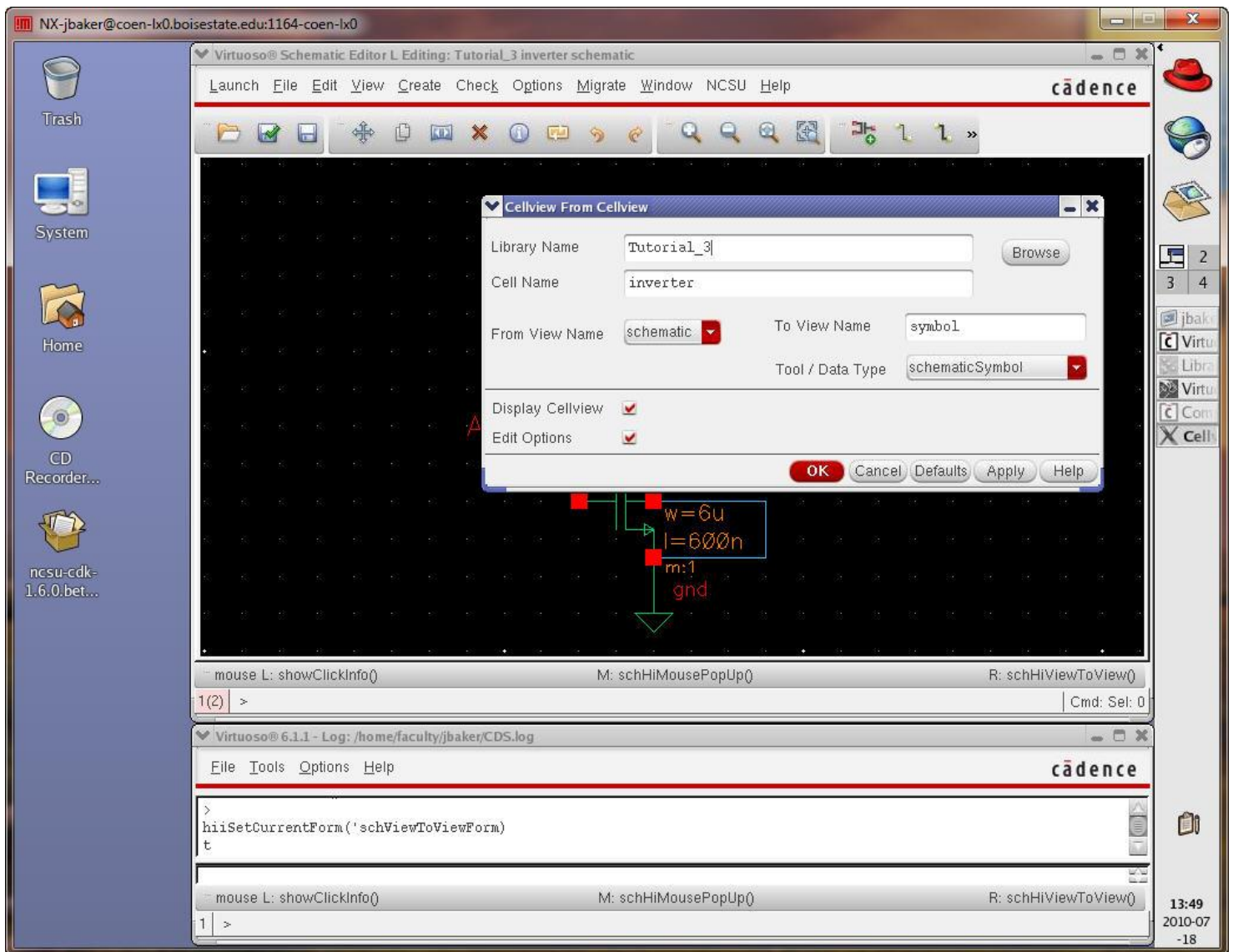
```

File Tools Options Help
nil
showClickInfo()
window:2

```

The console also displays mouse and window management events: 'mouse L: showClickInfo()', 'M: schHiMousePopUp()', and 'R: schZoomFit(1.0 0.9)'. The system tray in the bottom right corner shows the time '13:46', date '2010-07', and page number '-18'.

Next use the menu items to Create -> Cell View -> From Cell View to create the symbol for the inverter.



Select OK (twice).

Check and Save the schematic view of the inverter (and then close this window).

Delete everything in the inverter's symbol view except for the pins.

Draw the inverter symbol seen below (Create -> Shape -> Line/Circle)

Since we aren't showing the pin names select the pin and verify that it's in the right location (A is an input Ai is the inverter's output)

Virtuoso® Symbol Editor L Editing: Tutorial_3 inverter symbol

Launch File Edit View Create Check Options Window Help

cadence

Apply To: only current symbol pin

Show: system user

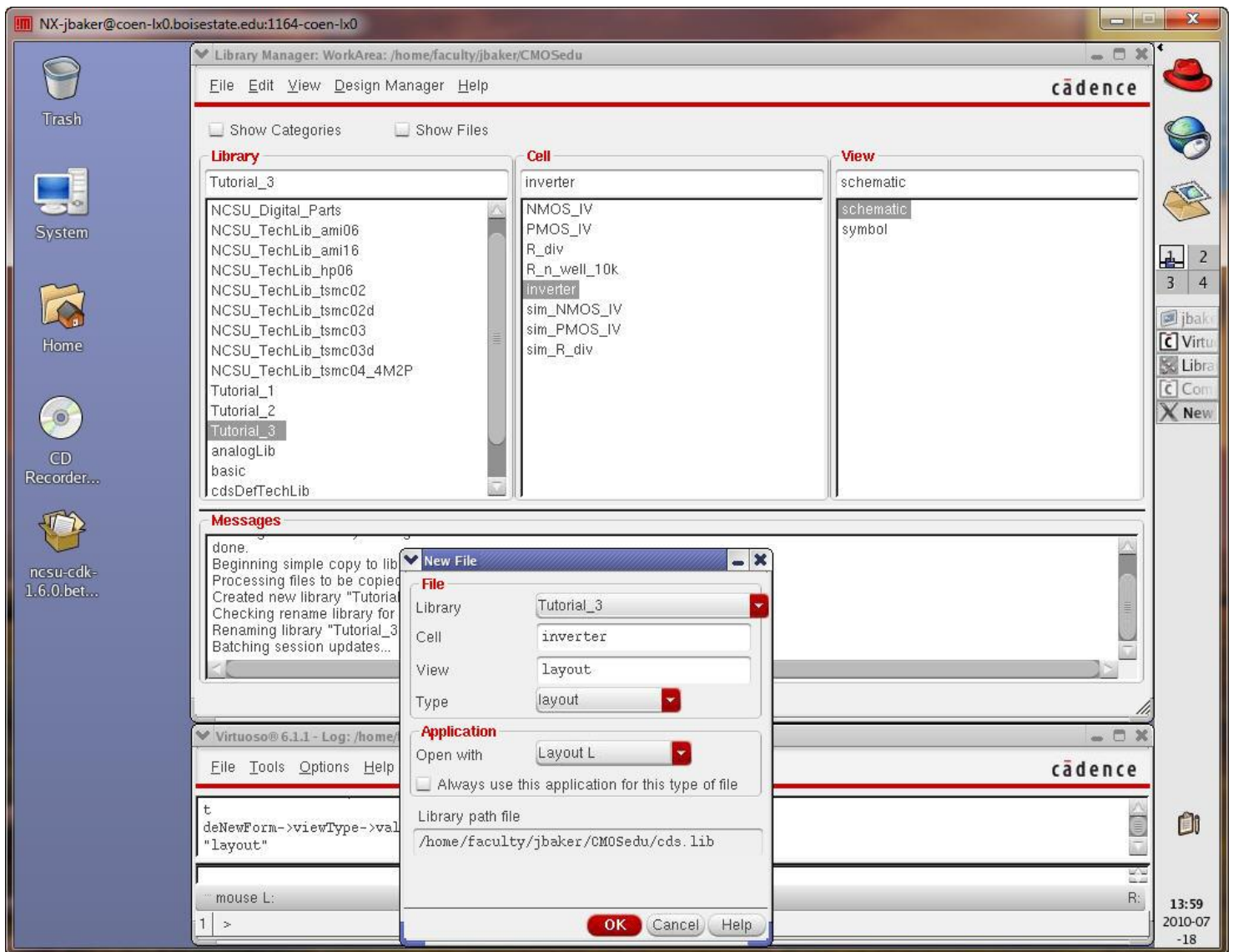
Property	Value	Display
Name	Ai	off
Direction	output	
Pwr Sensitivity	None	
Gnd Sensitivity	None	

Add Delete Modify

OK Cancel Apply Defaults Previous Next Help

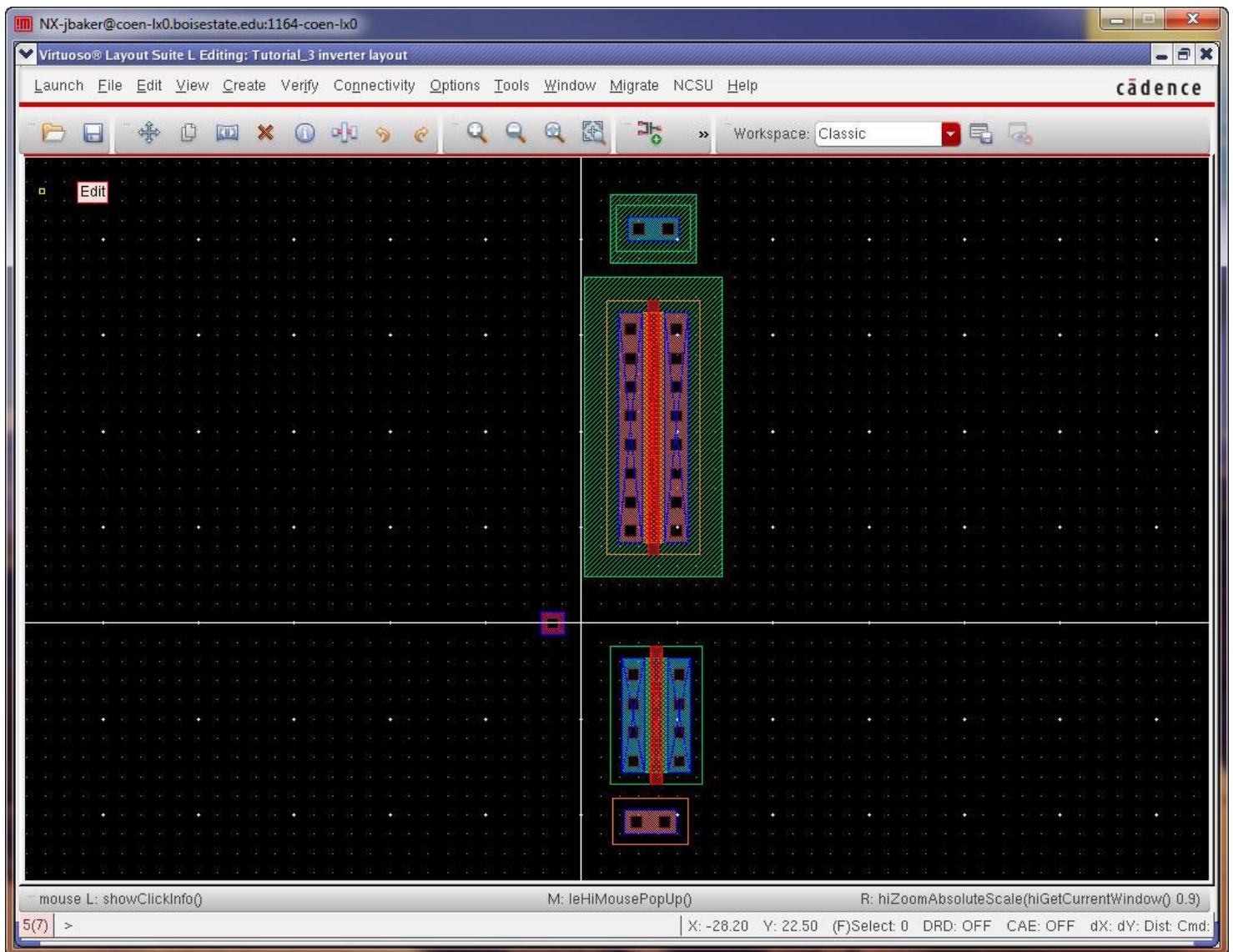
13:57
2010-07
-18

Check and Save the inverter symbol.
Next Create the layout view for the inverter.



Add the following cells (nmos, pmos, ntap, ptap, and m1_poly) to this layout view as seen below (you can copy as before but here we will instantiate cells).

Ensure the nmos is 6u/0.6u and pmos is 12u/0.6u and the ntap and ptap use two columns.



Next align the cells until you get something similar to what is seen below.
DRC your layout to ensure no errors (fix as needed).
Save the layout.

The screenshot shows the Cadence Virtuoso Layout Suite L Editing interface. The main window displays a layout of an inverter cell on a dark background with a grid. The layout consists of several rectangular regions: a large green rectangle at the top, a smaller blue rectangle below it, and another green rectangle at the bottom. The layout is centered on a vertical axis.

The left sidebar shows a list of layers and objects, including:

- metal1 (drw)
- NCSU_TechLib_ami06
- Layer | Object | Grid
- AV | NV | AS | NS
- pwell (drw)
- nwell (drw)
- active (drw)
- nactive (drw)
- pactive (drw)
- nselect (drw)
- pselect (drw)
- poly (drw)
- elec (drw)
- metal1 (drw)
- metal2 (drw)
- metal3 (drw)
- cc (drw)
- via (drw)
- via2 (drw)
- glass (drw)
- highres (drw)
- nodrc (drw)
- nolpe (drw)
- pad (drw)
- text (drw)
- res_id (drw)
- cap_id (drw)
- dio_id (drw)
- pwell (net)
- nwell (net)

The bottom status bar shows the following information:

- mouse L: Set Entry Layer
- M: Toggle Visibility
- R: Toggle Selectability
- 5(7) >
- X: -33.00 Y: 2.85 (F)Select: 0 DRD: OFF CAE: OFF dX: dY: Dist: Cmd:

The bottom window shows the DRC summary for the cell "inverter layout":

```

Virtuoso@6.1.1 - Log: /home/faculty/jbaker/CDS.log
File Tools Options Help
CPU TIME = 00:00:00 TOTAL TIME = 00:00:01
***** Summary of rule violations for cell "inverter layout" *****
Total errors found: 0
t
mouse L: Set Entry Layer M: Toggle Visibility R: Toggle Selectability
1 >
15:38
2010-07
-18

```

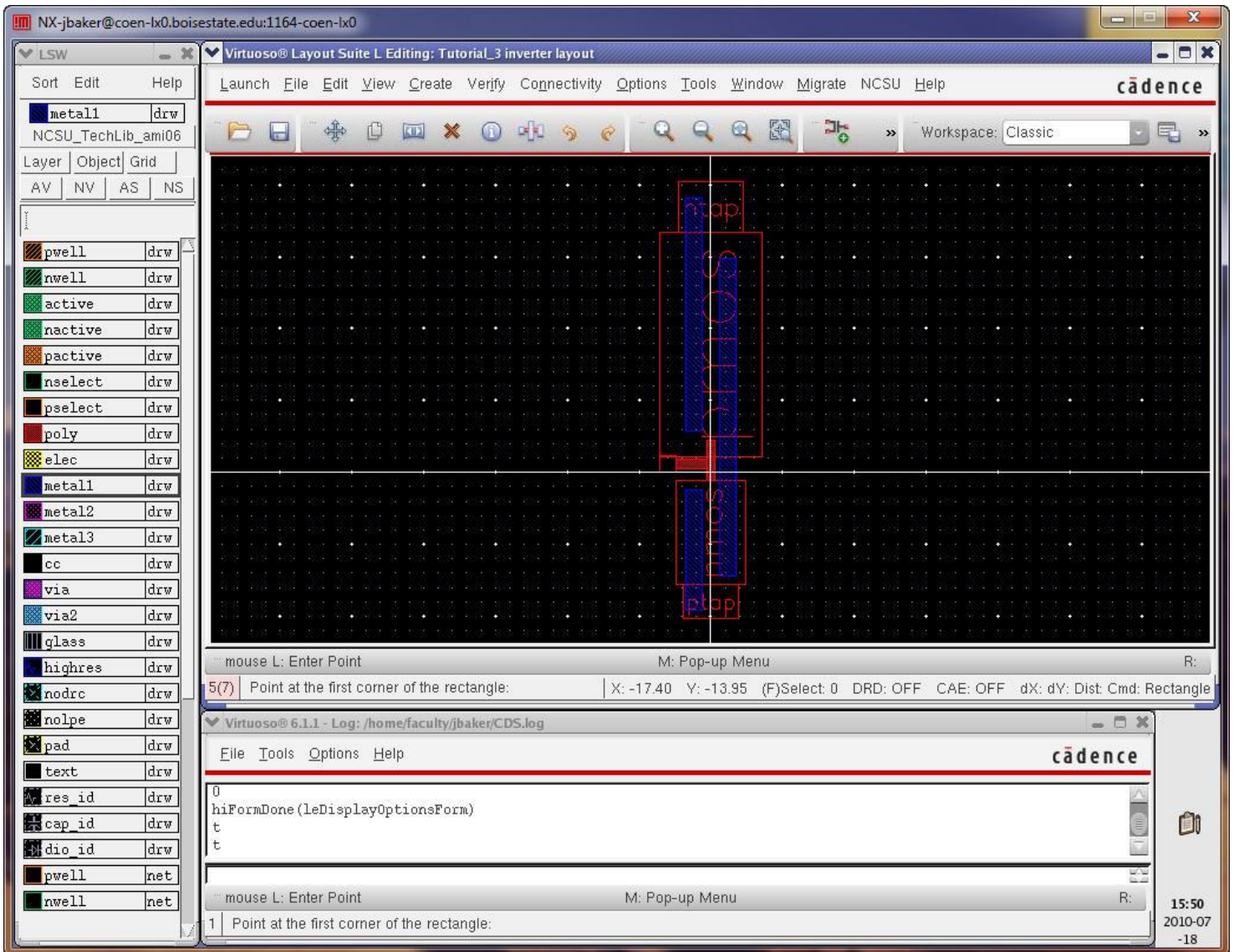
Add rectangles on poly and metal1 as seen below.
DRC and save your design.

The screenshot displays the Cadence Virtuoso Layout Suite L Editing interface for a project named 'Tutorial_3 inverter layout'. The main workspace shows a detailed layout of an inverter circuit on a dark grid background. The layout includes a central vertical structure with various colored regions representing different materials and layers. A red vertical line is visible, likely representing a signal path or a specific layer. The interface includes a menu bar with options like 'Launch', 'File', 'Edit', 'View', 'Create', 'Verify', 'Connectivity', 'Options', 'Tools', 'Window', 'Migrate', 'NCSU', and 'Help'. A toolbar with various icons is located below the menu bar. On the left side, there is a 'LSW' (Layer Set Window) with a list of layers and their types. The bottom of the window features a status bar with mouse coordinates and a log window showing system information and a summary of rule violations.

Layer	Object	Grid	
metal1	drw		
NCSU_TechLib_ami06			
AV	NV	AS	NS

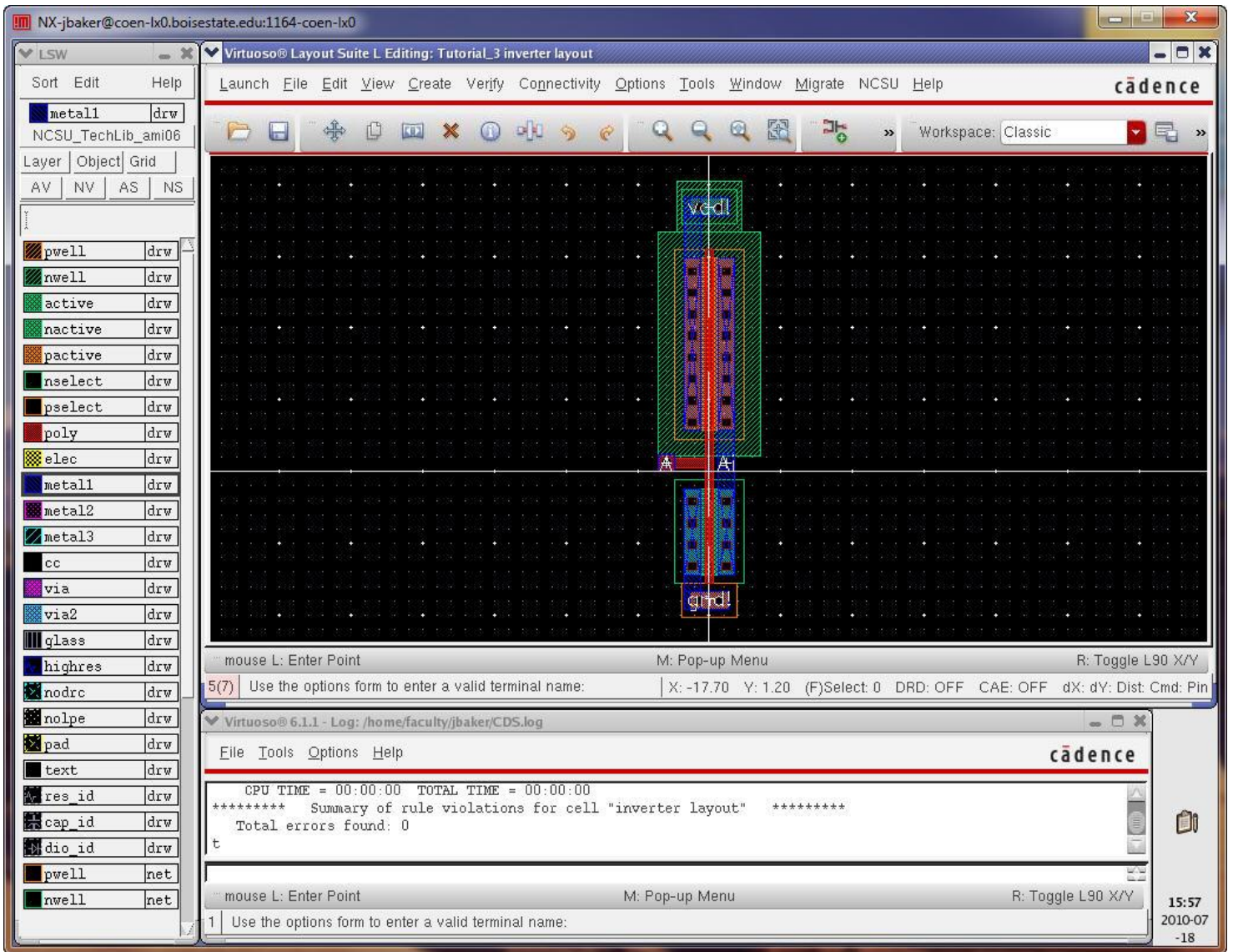
pwell	drw		
nwell	drw		
active	drw		
nactive	drw		
pactive	drw		
nselect	drw		
pselect	drw		
poly	drw		
elec	drw		
metal1	drw		
metal2	drw		
metal3	drw		
cc	drw		
via	drw		
via2	drw		
glass	drw		
highres	drw		
nodrc	drw		
nolpe	drw		
pad	drw		
text	drw		
res_id	drw		
cap_id	drw		
dio_id	drw		
pwell	net		
nwell	net		

```
Virtuoso@6.1.1 - Log: /home/faculty/jbaker/CDS.log
File Tools Options Help
-----
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "inverter layout" *****
Total errors found: 0
t
-----
1 | Point at the first corner of the rectangle: | X: -23.70 Y: -8.85 (F)Select: 0 DRD: OFF CAE: OFF dx: dY: Dist: Cmd: Rectangle
```



Next add pins on metal1 for gnd!, vdd! (both have a direction of inputOutput), A (input), and Ai (output).
DRC and save the design.

The screenshot displays the Cadence Virtuoso Layout Suite L Editing interface for a tutorial inverter layout. The main workspace shows a complex layout with various colored regions representing different layers. A vertical red bar is prominent in the center. The left sidebar contains a layer list with items such as pwell, nwell, active, nactive, pactive, nselect, pselect, poly, elec, metall, metal2, metal3, cc, via, via2, glass, highres, nodrc, nolpe, pad, text, res_id, cap_id, dio_id, pwell, and nwell, each with a corresponding color swatch and 'drw' or 'net' type. The top menu bar includes options like Launch, File, Edit, View, Create, Verify, Connectivity, Options, Tools, Window, Migrate, NCSU, and Help. The workspace title is 'Virtuoso@ Layout Suite L Editing: Tutorial_3 inverter layout'. Below the workspace, a status bar shows 'mouse L: Enter Point', 'M: Pop-up Menu', and 'R: Rotate 90'. A command log window at the bottom displays the following text: '5(7) Point at location of pin name. | X: 3.00 Y: 0.60 (F)Select: 0 DRD: OFF CAE: OFF dX: dY: Dist: Cmd: Pin', 'Virtuoso@6.1.1 - Log: /home/faculty/jbaker/CDS.log', 'File Tools Options Help', 'cadence', 'mouseAddPt()', 't', 'mouseAddPt()', 't', 'mouse L: Enter Point', 'M: Pop-up Menu', 'R: Rotate 90', and '1 Point at location of pin name.'. The system clock in the bottom right corner shows 15:56 on 2010-07-18.



Next run extraction on the layout.

The screenshot shows the Cadence Virtuoso Layout Suite L Editing interface. The main workspace displays a schematic diagram of an inverter layout on a grid. The interface includes a menu bar (Launch, File, Edit, View, Create, Verify, Connectivity, Options, Tools, Window, Migrate, NCSU, Help) and a toolbar. A command console at the bottom shows the following commands and output:

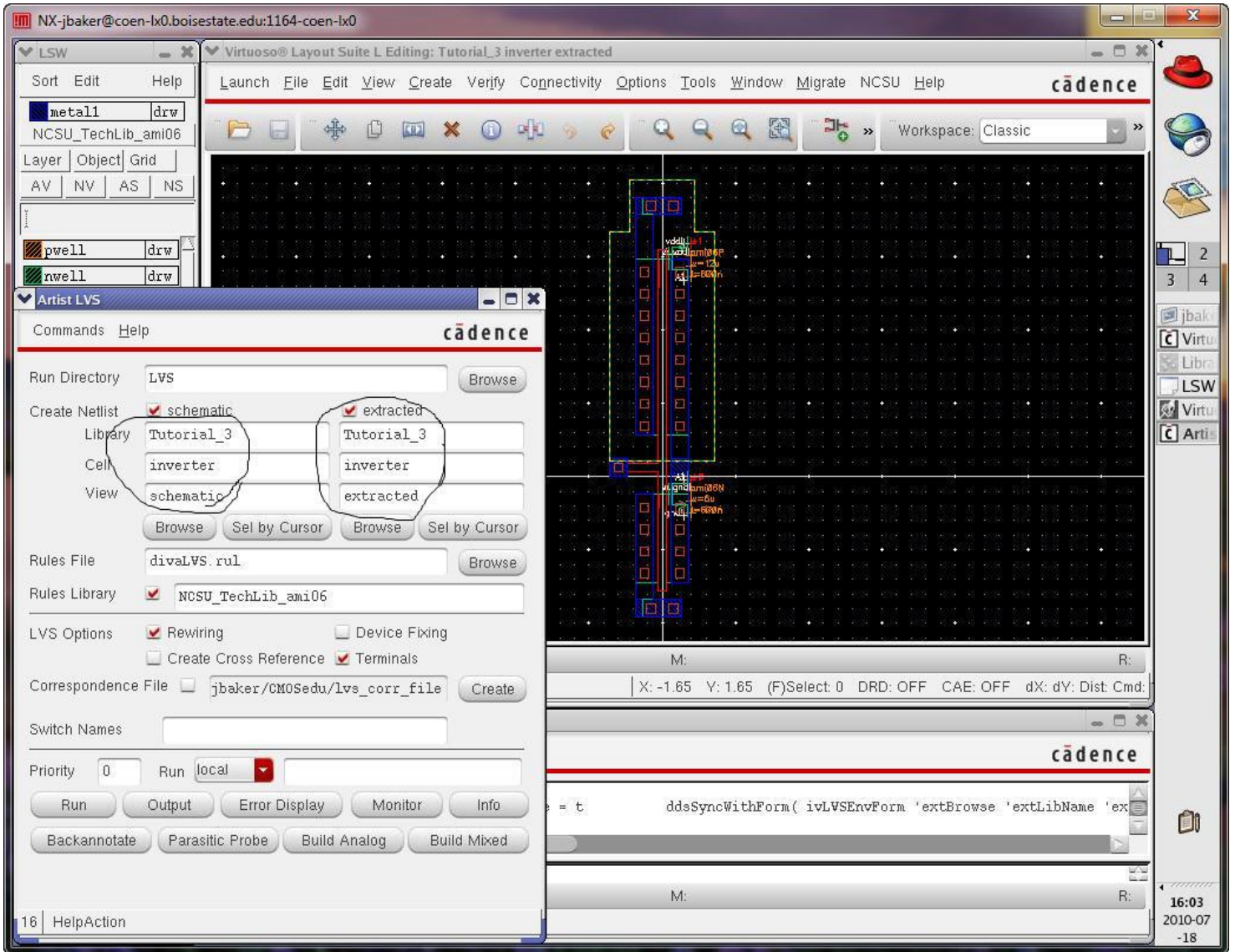
```

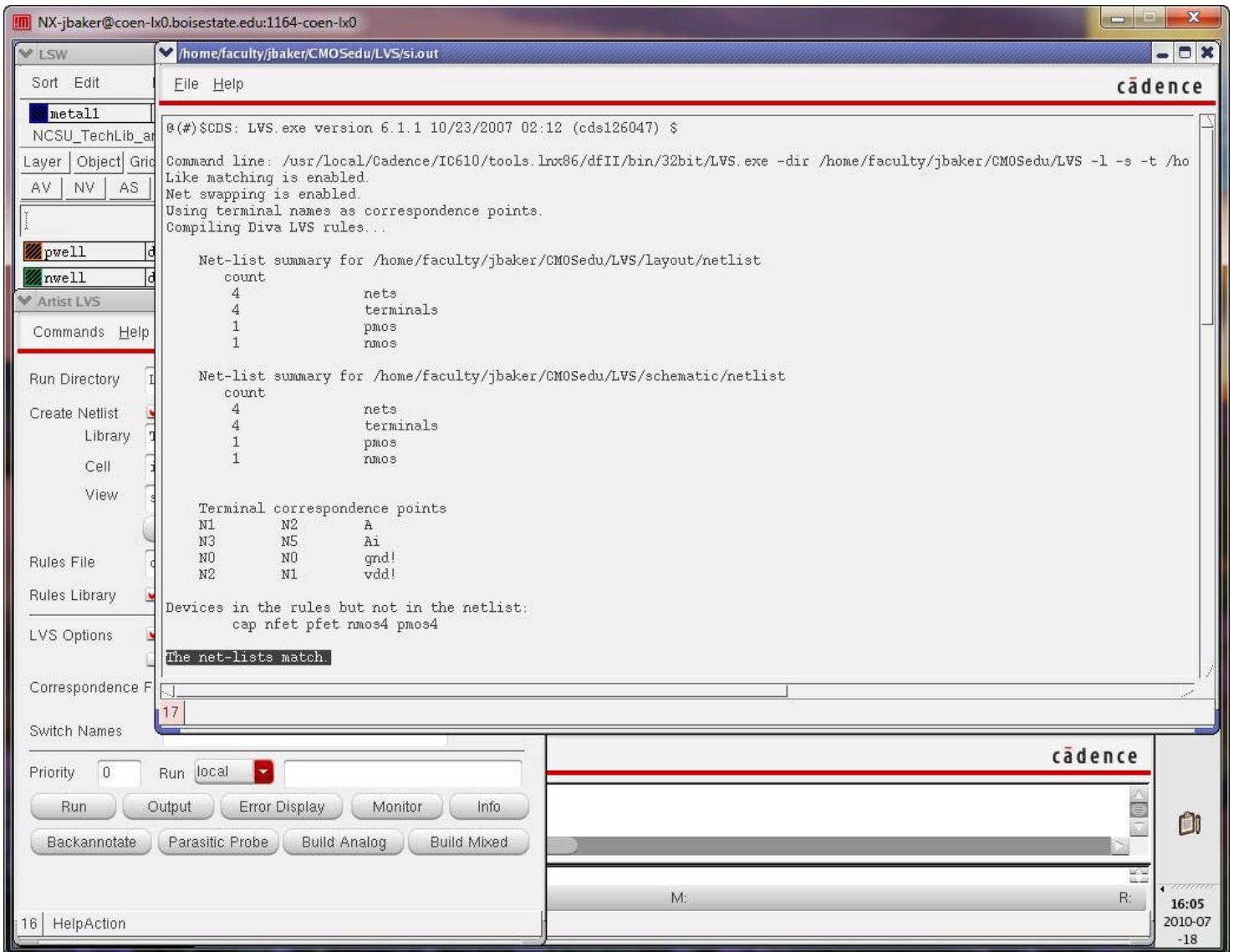
Virtuoso@6.1.1 - Log: /home/faculty/jbaker/CDS.log
File Tools Options Help
showClickInfo()
window:14
hiZoomAbsoluteScale(hiGetCurrentWindow() 0.9)
t

```

The status bar at the bottom right indicates the time 15:59, date 2010-07, and page number -18.

Finally, run the LVS on the inverter.





Okay, we are ready to simulate the operation of the inverter.

Create a cell called `sim_inverter_dc` (File -> New -> Cell View)

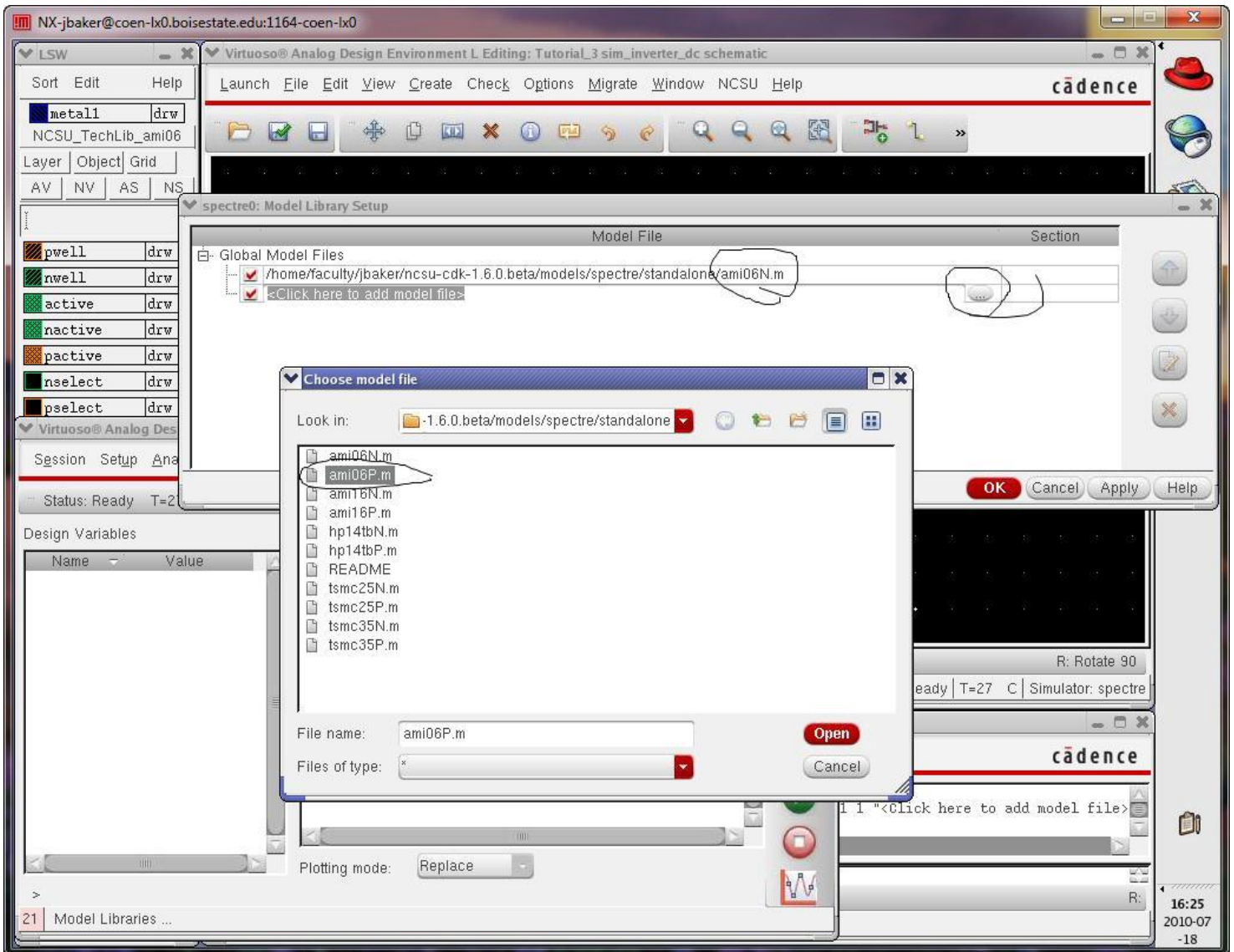
Draft the following schematic.

The symbol on the right is the no-connection symbol (in the basic library, Misc -> noConn) We add this symbol to be different and to avoid getting the warnings

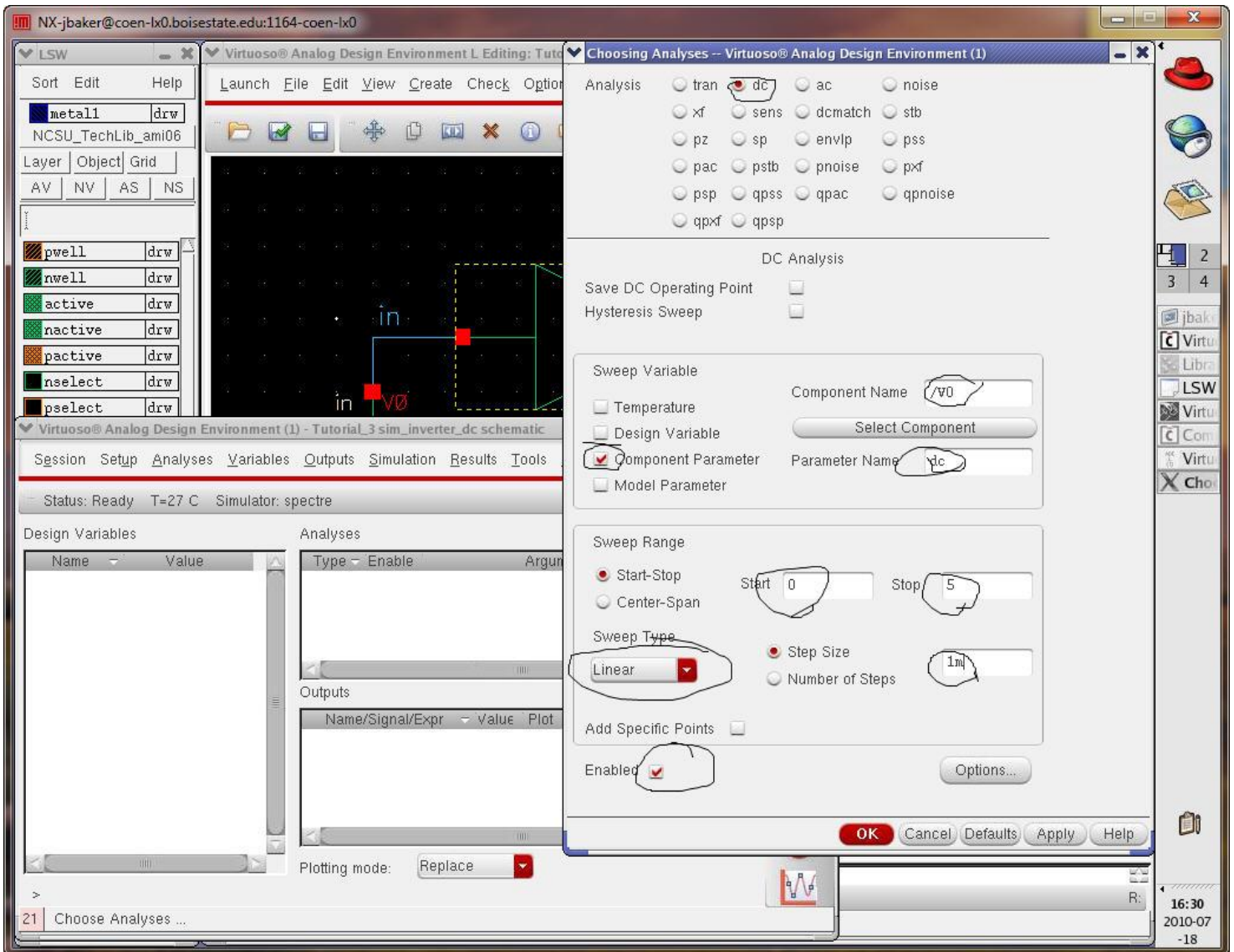
related to floating pins/nets that we ignore via the menu items Check -> Find Marker -> ignore, ignore

The screenshot displays the Cadence Virtuoso Schematic Editor interface. The main window shows a schematic diagram of an inverter circuit. The circuit consists of an input node labeled 'in', a voltage source labeled 'V0' with a value of 'vdc=0', a ground symbol labeled 'gnd!', and an output node labeled 'out'. The schematic is displayed in a window titled 'Virtuoso@ Schematic Editor L Editing: Tutorial_3 sim_inverter_dc schematic'. The interface includes a menu bar (Launch, File, Edit, View, Create, Check, Options, Migrate, Window, NCSU, Help), a toolbar, and a layer/object grid panel on the left. The layer/object grid panel shows various layers and objects, including 'metal1', 'NCSU_TechLib_ami06', 'pwell', 'nwell', 'active', 'nactive', 'pactive', 'nselect', 'pselect', 'poly', 'elec', 'metal1', 'metal2', 'metal3', 'cc', 'via', 'via2', 'glass', 'highres', 'nodrc', 'nolpe', 'pad', 'text', 'res_id', 'cap_id', 'dio_id', 'pwell', and 'nwell'. A command window at the bottom shows the command 'mouse L: mouseAddPt()' and 'M: schHiMousePopUp()'.

Start the ADE and select the model files (Setup -> Model Libraries located in `/$HOME/ncsu-cdk-1.6.0.beta/models/spectre/standalone`)



Next select Analyses -> Choose
 Note that the input vdc is named VO.



Next go to Outputs -> To Be Plotted -> Select On Schematic (select in and out)

The screenshot shows the Cadence Virtuoso Analog Design Environment. The main window displays a schematic of an inverter circuit. The input is labeled 'in' and is connected to a voltage source 'v0' with a value of 'vdc=0'. The output is labeled 'out' and is connected to a load. The circuit is powered by a ground symbol labeled 'gnd!'.

A dialog box titled 'modify_plot' is open, showing a table of signals to be plotted:

Name/Signal/Expr	Value	Plot	Save	Save Options
1 in		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv
2 out		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv

The 'Plot' column for both 'in' and 'out' is circled in red. The 'Plotting mode' is set to 'Replace'.

Save the state in the cellview.

Netlist and Run the simulation (hit the green button).

We get the results seen below.

The "Strip Chart Mode" was used to display the results (circled menu item).

Note how the output is zero!

Well, we didn't specify a vdd! anywhere so it should be zero. Let's fix this.

The screenshot shows the Cadence Virtuoso Analog Design Environment. The main window displays a schematic of an inverter circuit with an output node labeled 'out'. A DC sweep simulation has been performed, and the results are shown in a graph titled 'DC Response'. The graph plots the output voltage 'v(out)' against the input voltage 'dc (V)'. The output voltage is constant at approximately 5.24 mV for input voltages from 0.0 V to 5.0 V. The simulation log on the left provides details of the sweep parameters and results.

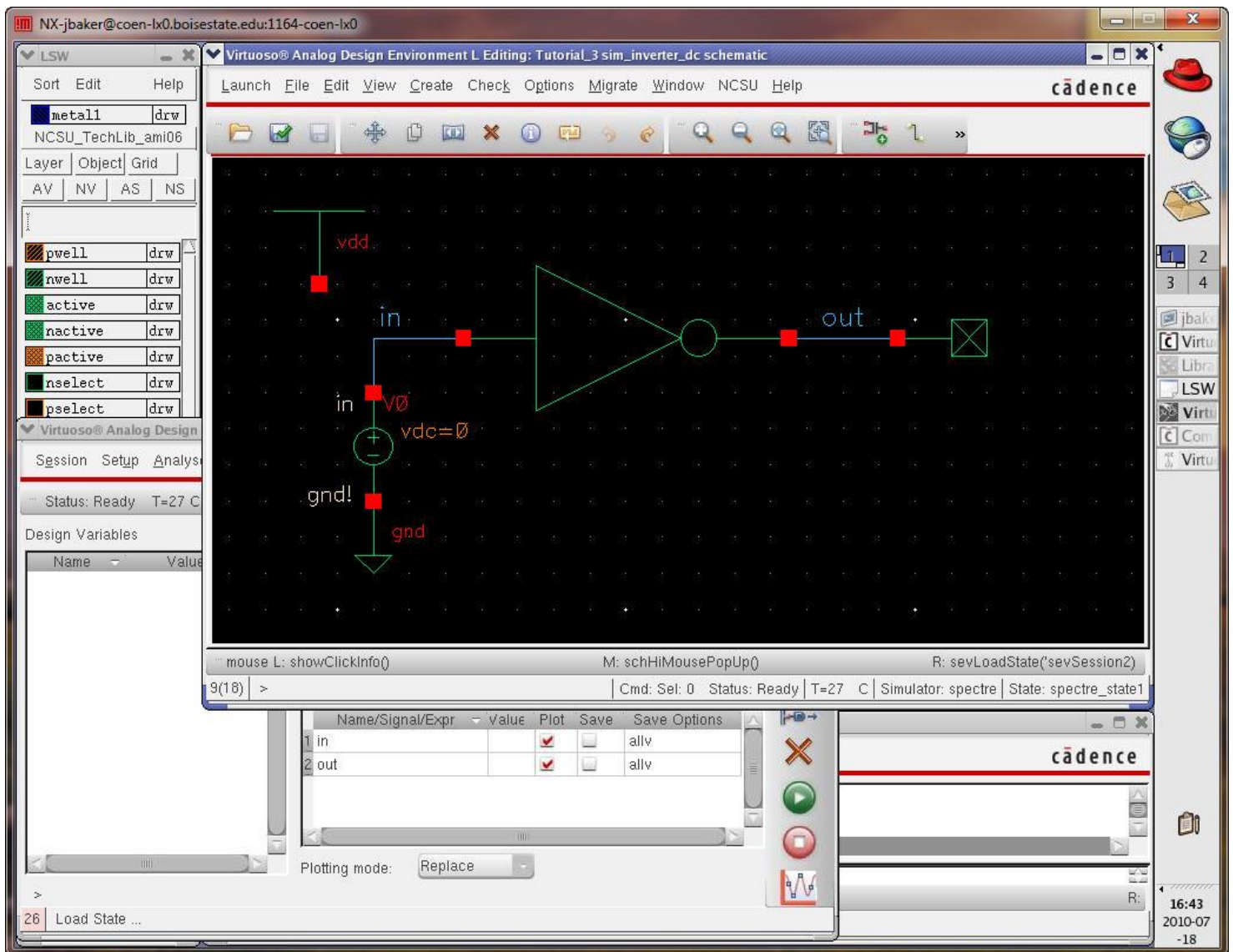
```

reftol = 1e-03
abstol(I) = 1 pA
abstol(V) = 1 uV
temp = 27 C
tnom = 27 C
tempeffects = all
gmin = 1 pS
maxrsd = 0 Ohm
mos_method = s
mos_vres = 50 mV
dc: dc = 125 mV (2.5 %), step = 1 mV (20 m%)
dc: dc = 375 mV (7.5 %), step = 1 mV (20 m%)
dc: dc = 625 mV (12.5 %), step = 1 mV (20 m%)
dc: dc = 875 mV (17.5 %), step = 1 mV (20 m%)
dc: dc = 1.125 V (22.5 %), step = 1 mV (20 m%)
dc: dc = 1.375 V (27.5 %), step = 1 mV (20 m%)
dc: dc = 1.625 V (32.5 %), step = 1 mV (20 m%)
dc: dc = 1.875 V (37.5 %), step = 1 mV (20 m%)
dc: dc = 2.125 V (42.5 %), step = 1 mV (20 m%)
dc: dc = 2.375 V (47.5 %), step = 1 mV (20 m%)
dc: dc = 2.625 V (52.5 %), step = 1 mV (20 m%)
dc: dc = 2.875 V (57.5 %), step = 1 mV (20 m%)
dc: dc = 3.125 V (62.5 %), step = 1 mV (20 m%)
dc: dc = 3.375 V (67.5 %), step = 1 mV (20 m%)
dc: dc = 3.625 V (72.5 %), step = 1 mV (20 m%)
dc: dc = 3.875 V (77.5 %), step = 1 mV (20 m%)
dc: dc = 4.125 V (82.5 %), step = 1 mV (20 m%)
dc: dc = 4.375 V (87.5 %), step = 1 mV (20 m%)
dc: dc = 4.625 V (92.5 %), step = 1 mV (20 m%)
dc: dc = 4.875 V (97.5 %), step = 1 mV (20 m%)
Accumulated dc load time = 130 ms.
Accumulated dc factor time = 30 ms.
Accumulated dc solve time = 0 s.
Accumulated dc output time = 50 ms.
Total time required for dc analysis `dc' was 480 ms.

modelParameter: writing model parameter values to rawfile.
element: writing instance parameter values to rawfile.
outputParameter: writing output parameter values to rawfile.
designParamVals: writing netlist parameters to rawfile.
primitives: writing primitives to rawfile.
subckts: writing subcircuits to rawfile.

```

Let's add vdd as seen below.



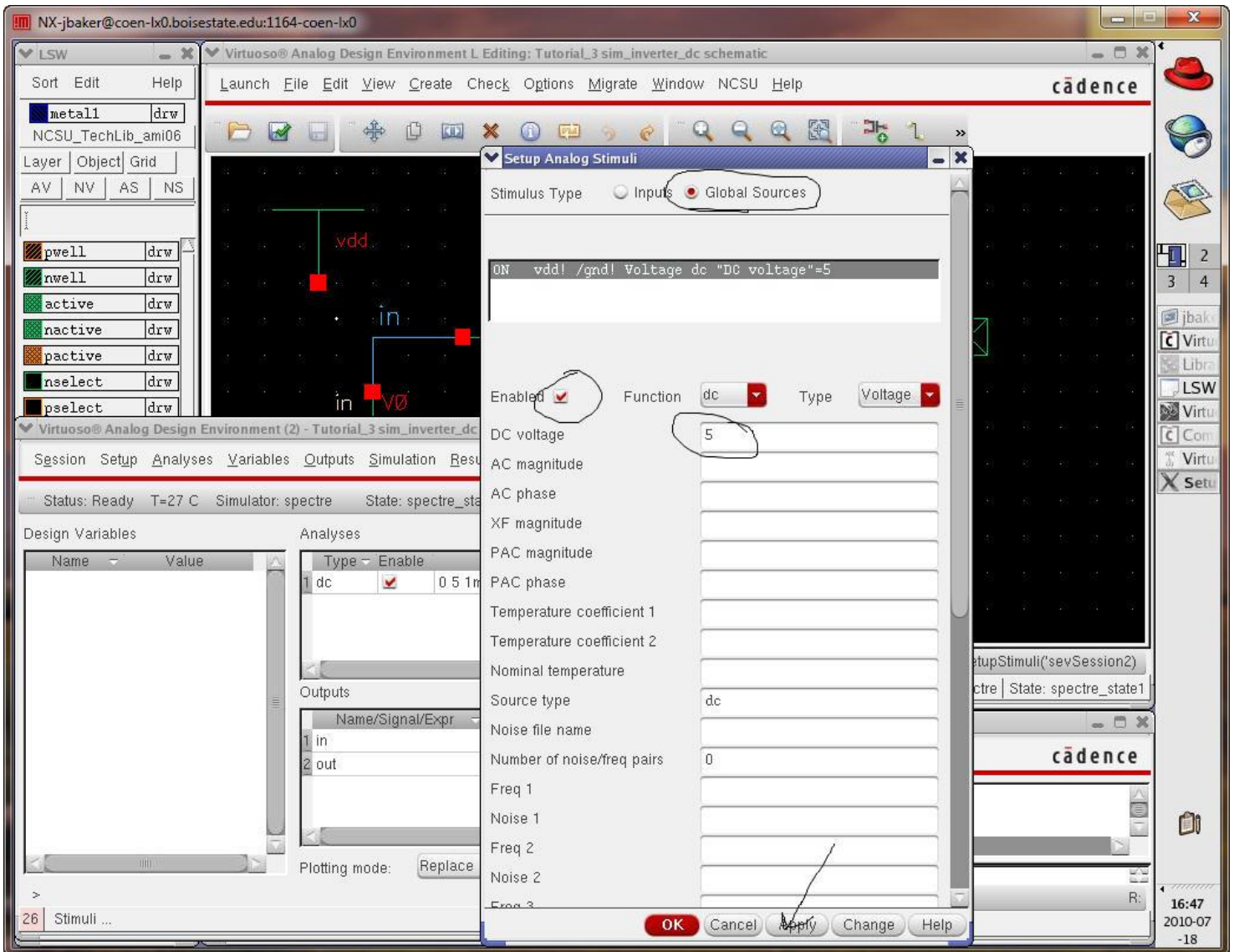
Check and Save the schematic. Note that if the inverter and vdd symbols overlap there will be errors when you Check and Save (so don't put vdd too close to the inverter symbol).

Next, in the ADE, select Setup -> Stimuli and the parameters seen below (after hitting the Apply button).



If you directly add a voltage source to your schematic like the following, you should **NOT** also use a Stimuli (Global

source) since the result is two voltage sources connected to the same node (which will result in error and the simulation not running!)



Save the state (Cellview) so we don't have to do this again next time we run the simulation.

Hit OK and run the simulation.

The results are what we expect the inverter voltage transfer curves to look like.

The screenshot displays the Cadence Virtuoso interface. The top window shows the schematic editor with a circuit diagram of an inverter. The bottom window shows the DC Response plot. The plot title is "DC Response". The x-axis is labeled "dc (V)" and ranges from 0.0 to 5.0. The y-axis is labeled "V (V)" and ranges from 0.0 to 6.0. Two traces are shown: a solid blue line for "/out" and a dashed yellow line for "/in". The "/in" trace is a straight line from (0,0) to (5,5). The "/out" trace starts at approximately 5.1V for low input, remains relatively flat until about 2.5V, then drops sharply to approximately 0.1V for high input. The plot is titled "Tutorial_3 sim_inverter_dc schematic: Jul 18 16:50:24 2010 28".

```

reftol = 1e-03
abstol(I) = 1 pA
abstol(V) = 1 uV
temp = 27 C
tnom = 27 C
tempeffects = all
gmin = 1 pS
maxrsd = 0 Ohm
mos_method = s
mos_vres = 50 mV
dc: dc = 125 mV (2.5 %), step = 1 mV (20 m%)
dc: dc = 375 mV (7.5 %), step = 1 mV (20 m%)
dc: dc = 625 mV (12.5 %), step = 1 mV (20 m%)
dc: dc = 875 mV (17.5 %), step = 1 mV (20 m%)
dc: dc = 1.125 V (22.5 %), step = 1 mV (20 m%)
dc: dc = 1.375 V (27.5 %), step = 1 mV (20 m%)
dc: dc = 1.625 V (32.5 %), step = 1 mV (20 m%)
dc: dc = 1.875 V (37.5 %), step = 1 mV (20 m%)
dc: dc = 2.125 V (42.5 %), step = 1 mV (20 m%)
dc: dc = 2.375 V (47.5 %), step = 1 mV (20 m%)
dc: dc = 2.625 V (52.5 %), step = 1 mV (20 m%)
dc: dc = 2.875 V (57.5 %), step = 1 mV (20 m%)
dc: dc = 3.125 V (62.5 %), step = 1 mV (20 m%)
dc: dc = 3.375 V (67.5 %), step = 1 mV (20 m%)
dc: dc = 3.625 V (72.5 %), step = 1 mV (20 m%)
dc: dc = 3.875 V (77.5 %), step = 1 mV (20 m%)
dc: dc = 4.125 V (82.5 %), step = 1 mV (20 m%)
dc: dc = 4.375 V (87.5 %), step = 1 mV (20 m%)
dc: dc = 4.625 V (92.5 %), step = 1 mV (20 m%)
dc: dc = 4.875 V (97.5 %), step = 1 mV (20 m%)
Accumulated dc load time = 160 ms.
Accumulated dc factor time = 0 s.
Accumulated dc solve time = 10 ms.
Accumulated dc output time = 90 ms.
Total time required for dc analysis `dc' was 520 ms.

modelParameter: writing model parameter values to rawfile.
element: writing instance parameter values to rawfile.
outputParameter: writing output parameter values to rawfile.
designParamVals: writing netlist parameters to rawfile.
primitives: writing primitives to rawfile.
subckts: writing subcircuits to rawfile.

```

Let's go ahead and simulate the extracted layout at this point (Setup -> Environment and add extracted in front of schematic as discussed in the last tutorial).

The screenshot shows the Cadence Virtuoso Analog Design Environment interface. The main window displays a schematic diagram of an inverter circuit with nodes labeled 'vdd' and 'in'. An 'Environment Options' dialog box is open, showing the following settings:

- Switch View List: spectre cmos_sch cmos.sch **extracted** schematic verilog (the 'extracted' view is circled in red)
- Stop View List: spectre
- Parameter Range Checking File: (empty)
- Analysis Order: (empty)
- Print Comments:
- userCmdLineOption: (empty)
- Automatic output log:
- Use SPICE Netlist Reader(spp): Y N
- savestate(ss): Y N
- recover(rec): Y N
- Plugin for PLL Macro Model:

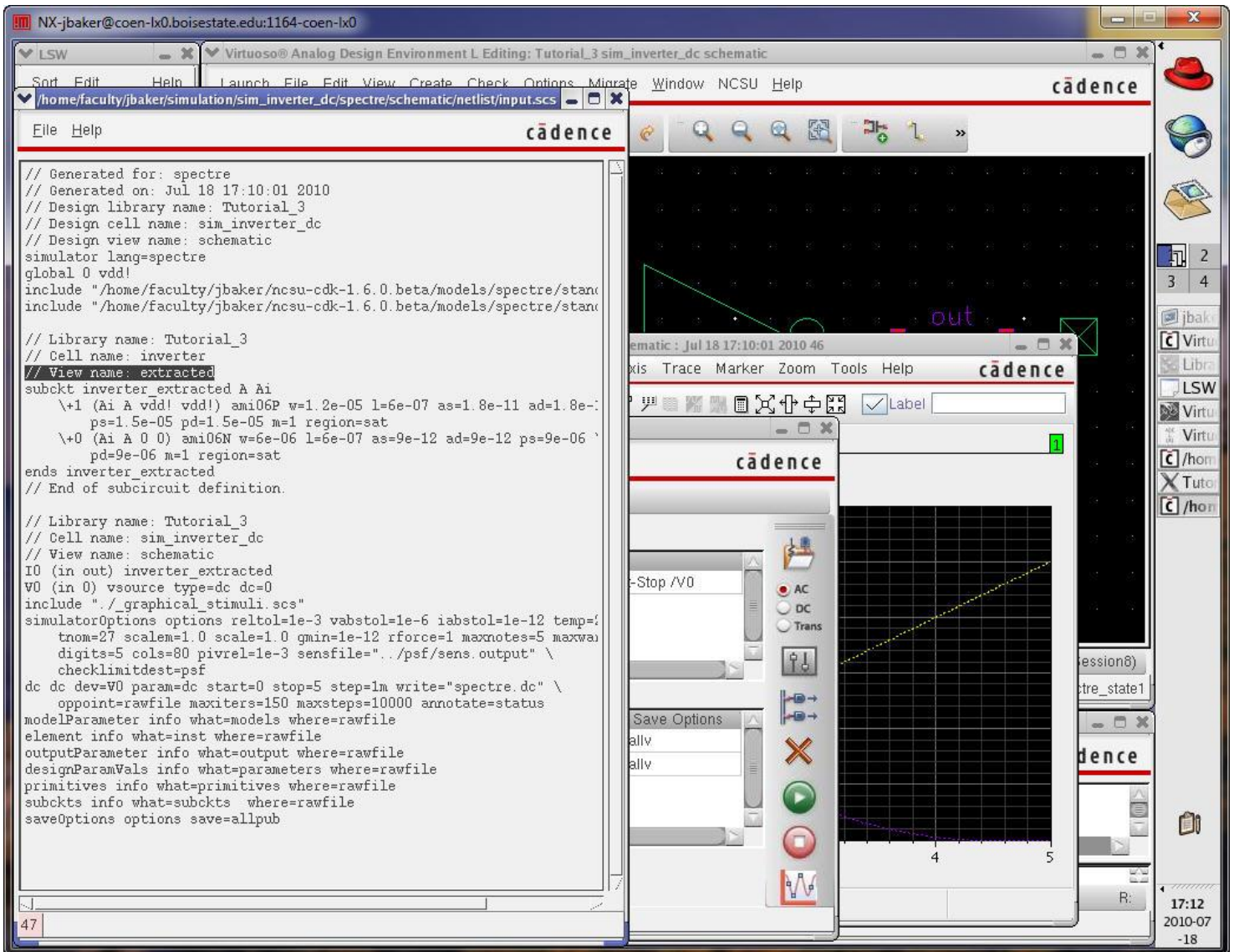
The 'Outputs' table at the bottom of the dialog shows the following data:

Name/Signal/Expr	Value	Plot	Save	Save Options
1 in		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv
2 out		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv

The 'Plotting mode' is set to 'Replace'. The status bar at the bottom right shows the time 17:09, date 2010-07, and page number -18.

Which gives the same results as the schematic.

To verify we are simulating the extracted view and not the schematic view go to Simulations -> Netlist -> Display



Save and close everything. This concludes Tutorial 3.

For your reference the Tutorial_3 directory is available in [Tutorial_3.zip](#).

[Return](#)