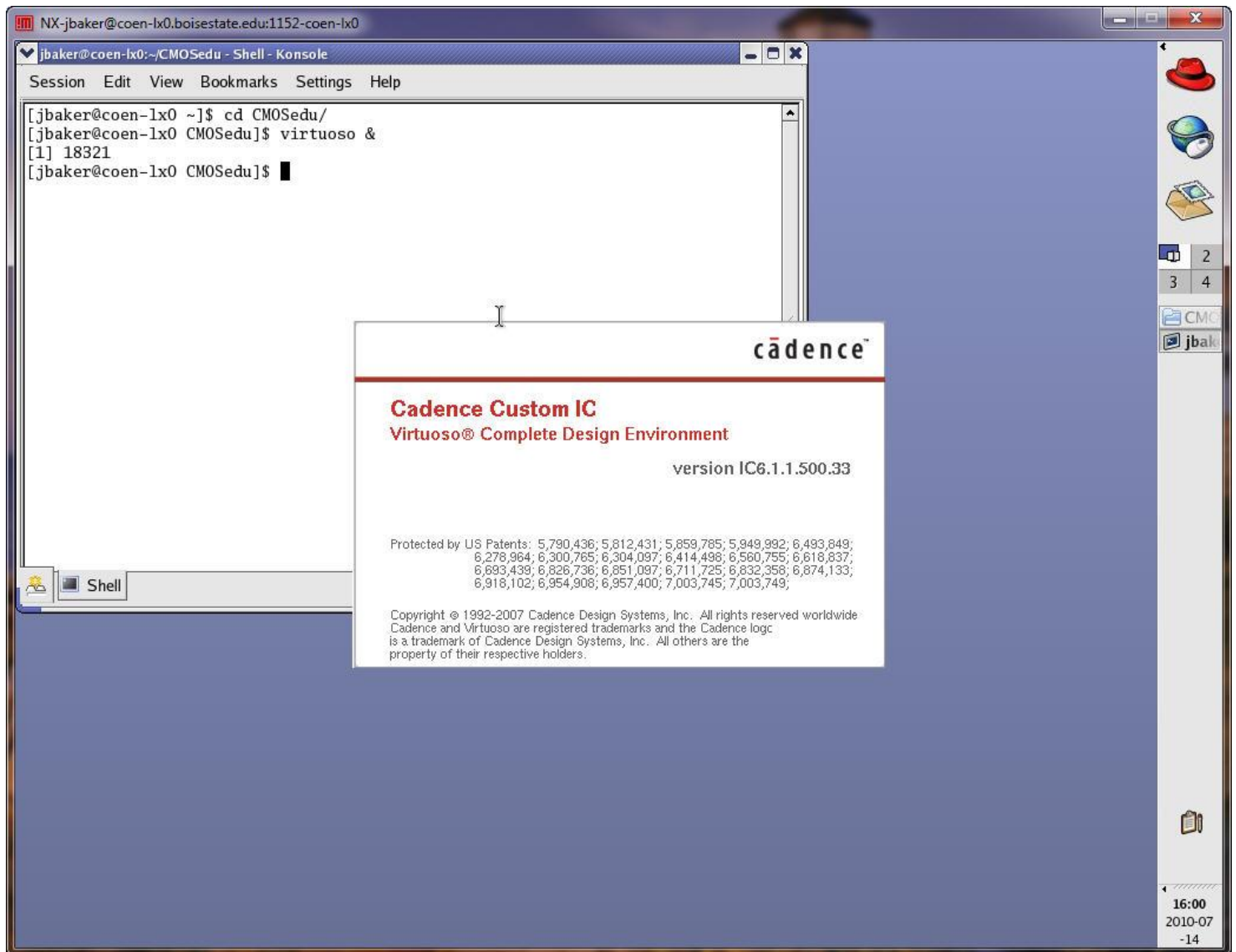


[Cadence Design System Tutorials from CMOSedu.com](#) ([Return](#))

Tutorial 2 - Layout and simulating the IV curves of PMOS and NMOS devices

In this tutorial we'll lay out and simulate the operation of NMOS and PMOS transistors using the C5 process from [Tutorial 1](#). Note that we'll simulate both the schematic and layout (extracted) views.

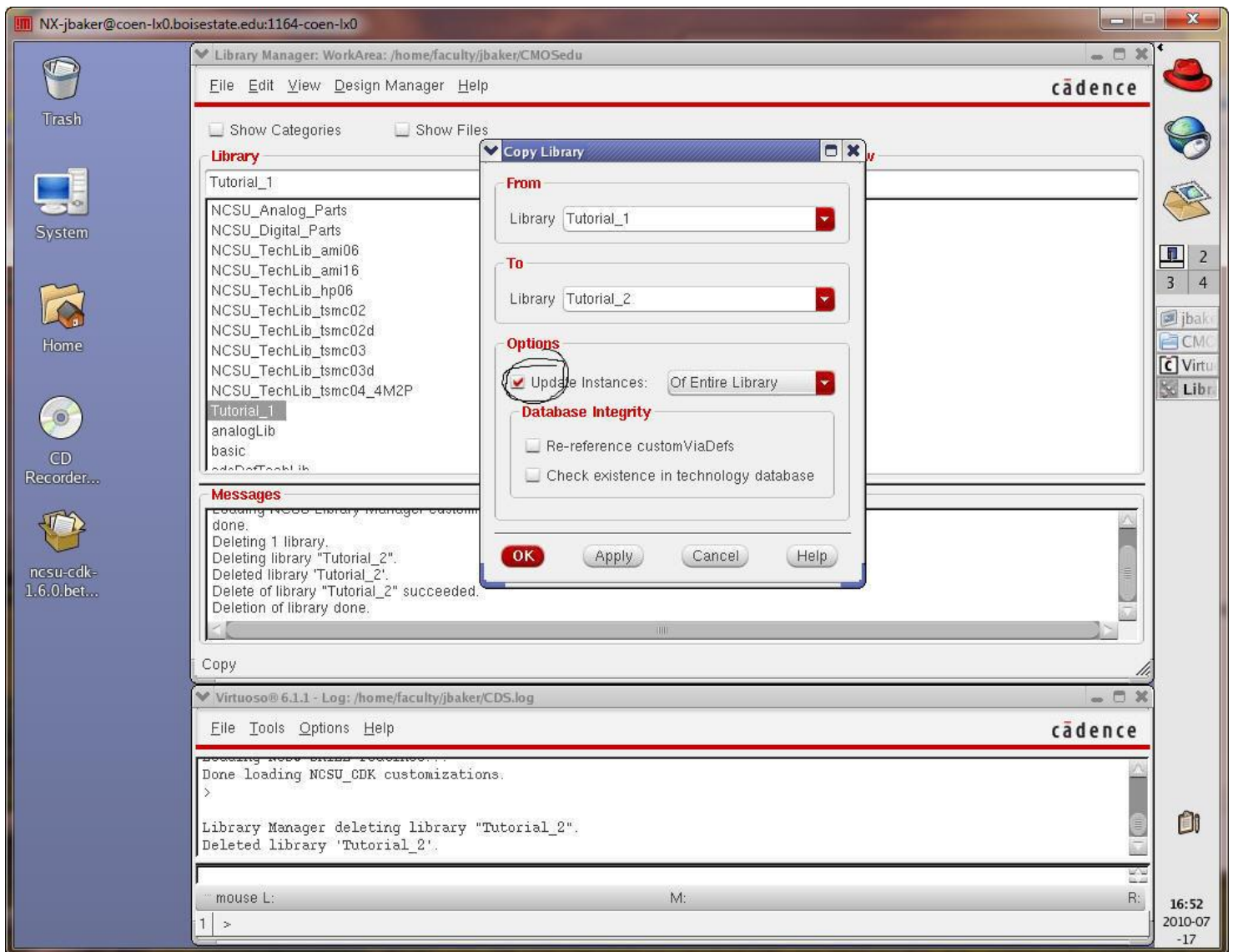
To begin Tutorial 2 first start Cadence's Virtuoso in the CMOSedu directory as seen below.



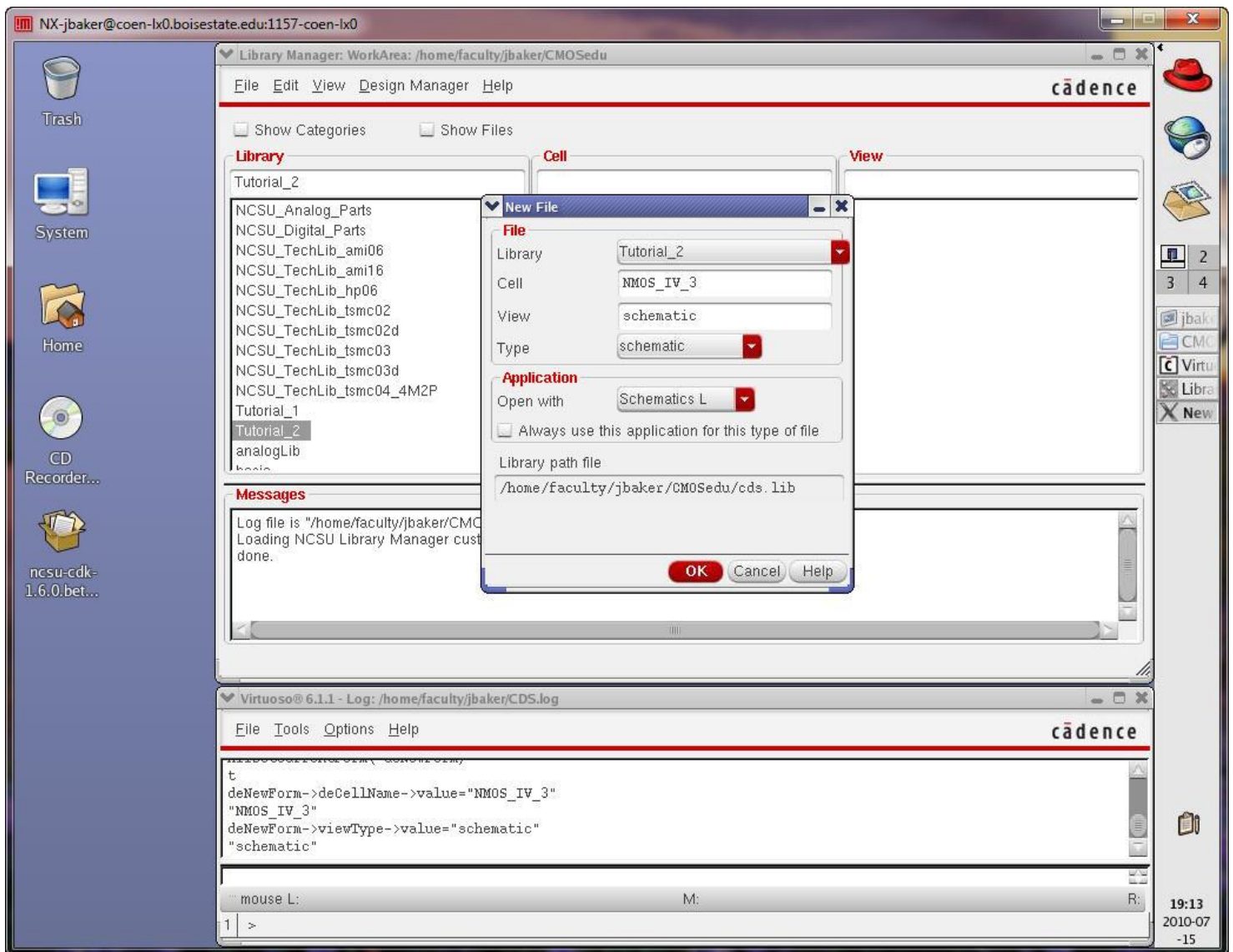
Next copy Tutorial_1 into a new library called Tutorial_2 by right clicking on Tutorial_1 (below).

Note that if you don't select Update Instances many of the cells in Tutorial_2 will reference Tutorial_1 (we want the libraries to be self-contained).

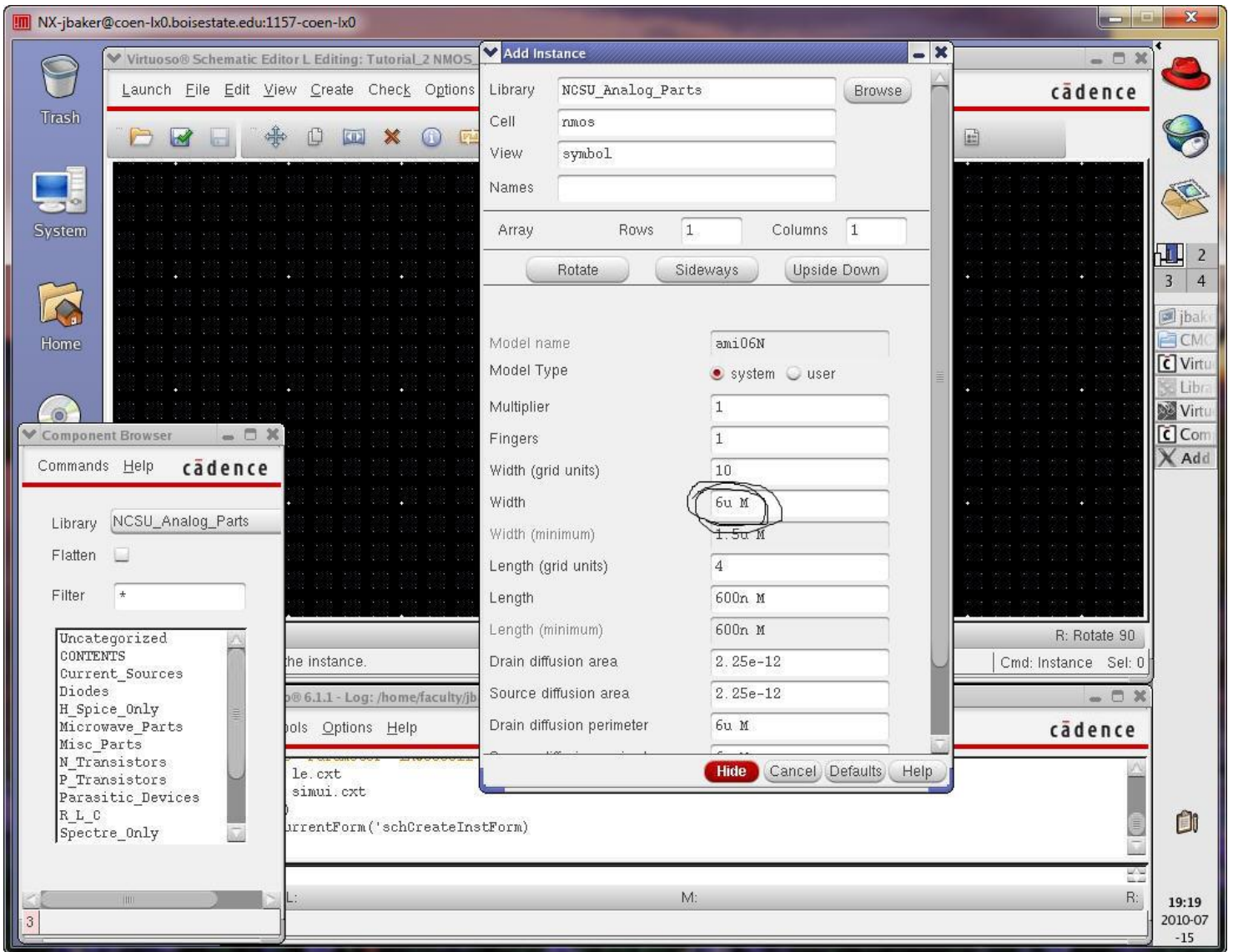
After pressing OK you will be asked where the Tutorial_2 directory should be placed. The default location should be the same as Tutorial_1, that is, CMOSedu, so hit OK a second time to create the library.



Next, with the Tutorial_2 Library highlighted, select in the Library Manager File -> New -> Cell View. Create a schematic cell called NMOS_IV_3 as seen below. The 3 indicates we'll use a 3 terminal transistor. Using a 3-terminal NMOS the body (p-well or p-substrate) is connected to gnd!



Press **i** (or use the menu Create -> Instance) and select, in the Component Browser Window, NCSU_Analog_Parts, N_Transistors, nmos. Remember that often Windows are opened that are behind other windows so you have to use the Task bar to bring them to the front. Set the transistors Width to 6u and leave its length at 600 nm. Place the transistor and fit the screen (press **f**).



Virtuoso® Schematic Editor L Editing: Tutorial_2 NMOS_IV_3 schematic

Launch File Edit View Create Check Options Migrate Window NCSU Help

cadence

M0
ami06N
w=6u
l=600n
m:1

mouse L: showClickInfo() M: schHiMousePopUp() R: schZoomFit(1.0 0.9)

1(2) > Cmd: Sel: 0

Virtuoso® 6.1.1 - Log: /home/faculty/jbaker/CDS.log

File Tools Options Help

cadence

```
cancelEnterFun()
t
nil
schZoomFit(1.0 0.9)
t
```

mouse L: showClickInfo() M: schHiMousePopUp() R: schZoomFit(1.0 0.9)

1 >

19:25
2010-07
-15

Next add Pins with the direction inputOutput and wires as seen below.
Remember that right+clicking the mouse when instantiating the Pin rotates it.
Z (zoom out by 2) and f (fit) can be used while instantiating the pin.
w can be used to wire the Pin to the MOSFET.
Check and Save the schematic when finished.

Virtuoso® Schematic Editor L Editing: Tutorial_2 NMOS_IV_3 schematic

Launch File Edit View Create Check Options Migrate Window NCSU Help

cādence

mouse L: mouseAddPt() M: schHiMousePopUp() R: Toggle Draw Mode

2(3) | Point at starting point for the router or snap to diamond using the "s" key. | Cmd: Wire Sel: 0

Virtuoso® 6.1.1 - Log: /home/faculty/jbaker/CDS.log

File Tools Options Help

Schematic check completed with no errors.
 "Tutorial_2 NMOS_IV_3 schematic" saved.
 t

mouse L: mouseAddPt() M: schHiMousePopUp() R: Toggle Draw Mode

1 | Point at starting point for the router or snap to diamond using the "s" key.

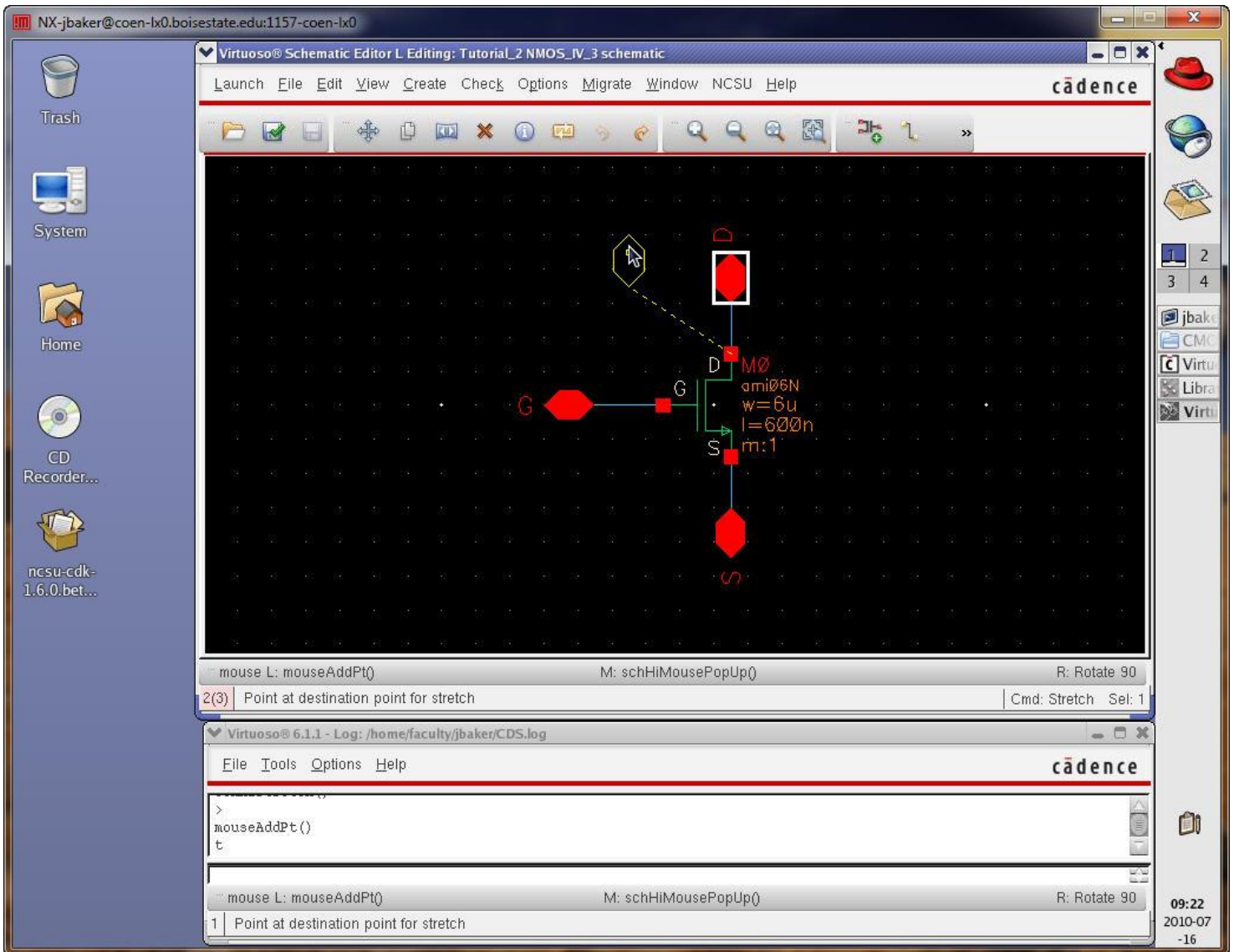
09:09
2010-07
-16

Before making a symbol for this schematic let's talk about stretching (Bindkey **s**).

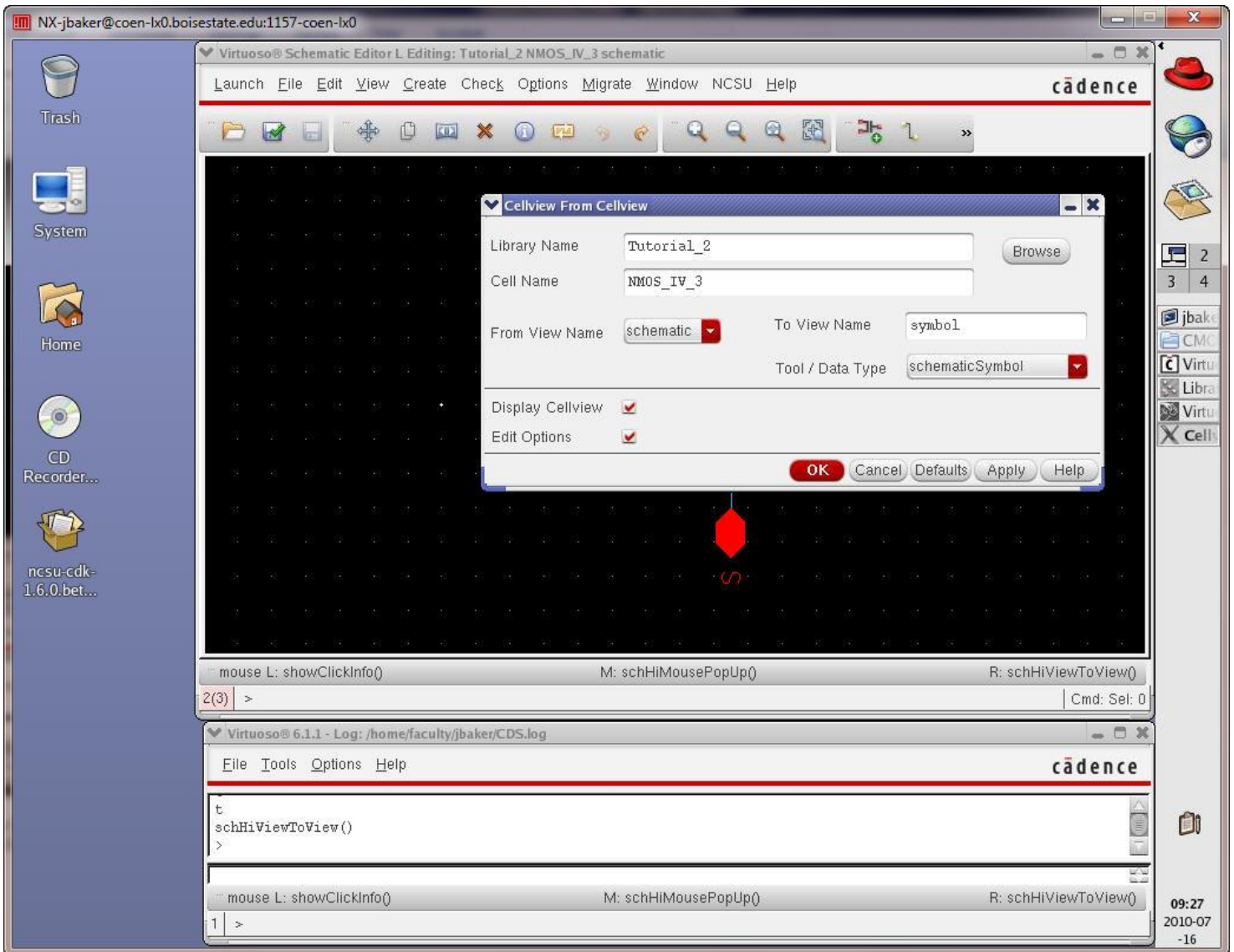
We know that to move an object we select it then press **m**.

Stretching is similar except that the object stays attached to the wire or whatever you haven't selected.

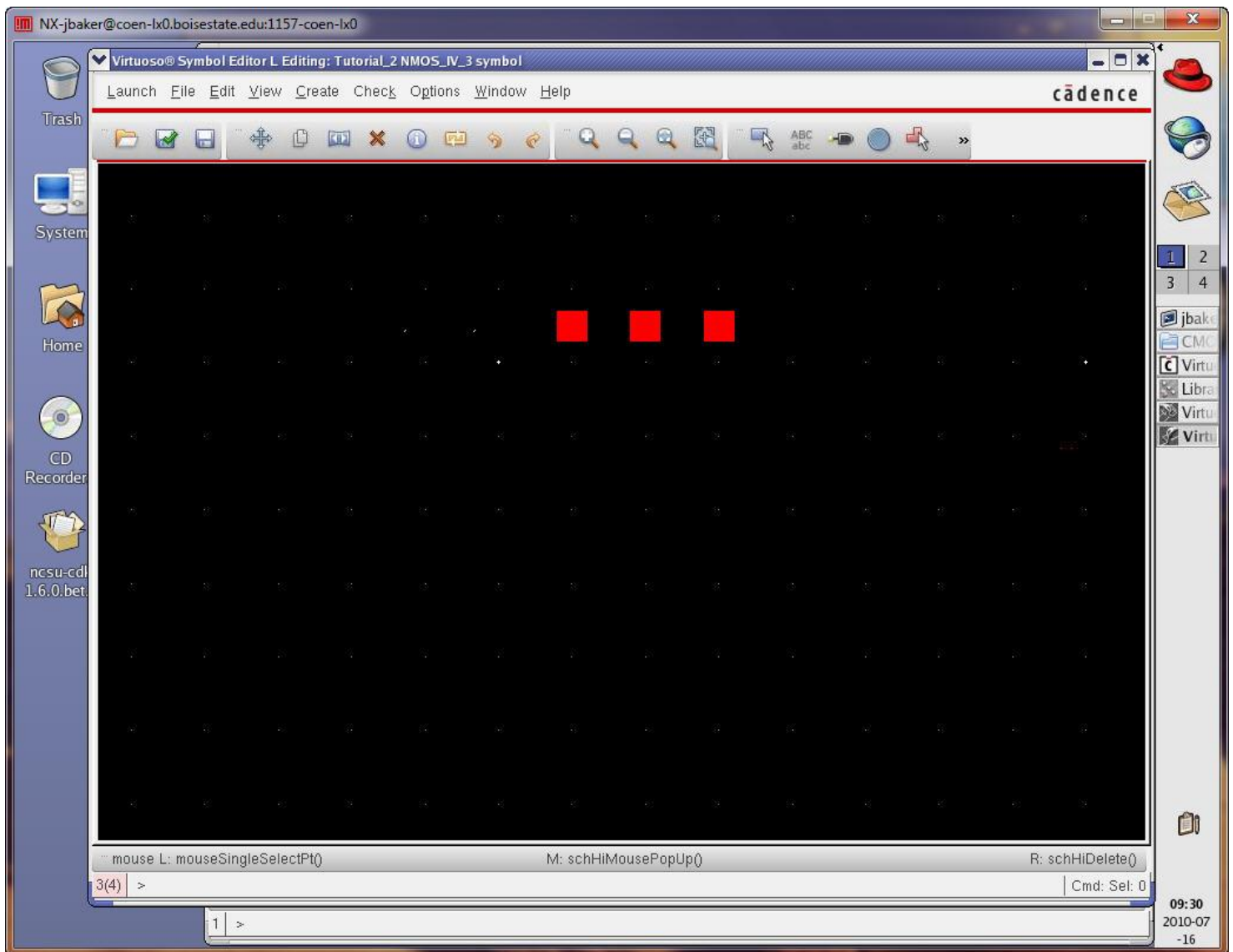
Below is an example.



Next create a symbol view for this schematic.
 Create -> Cell View -> From Cell View



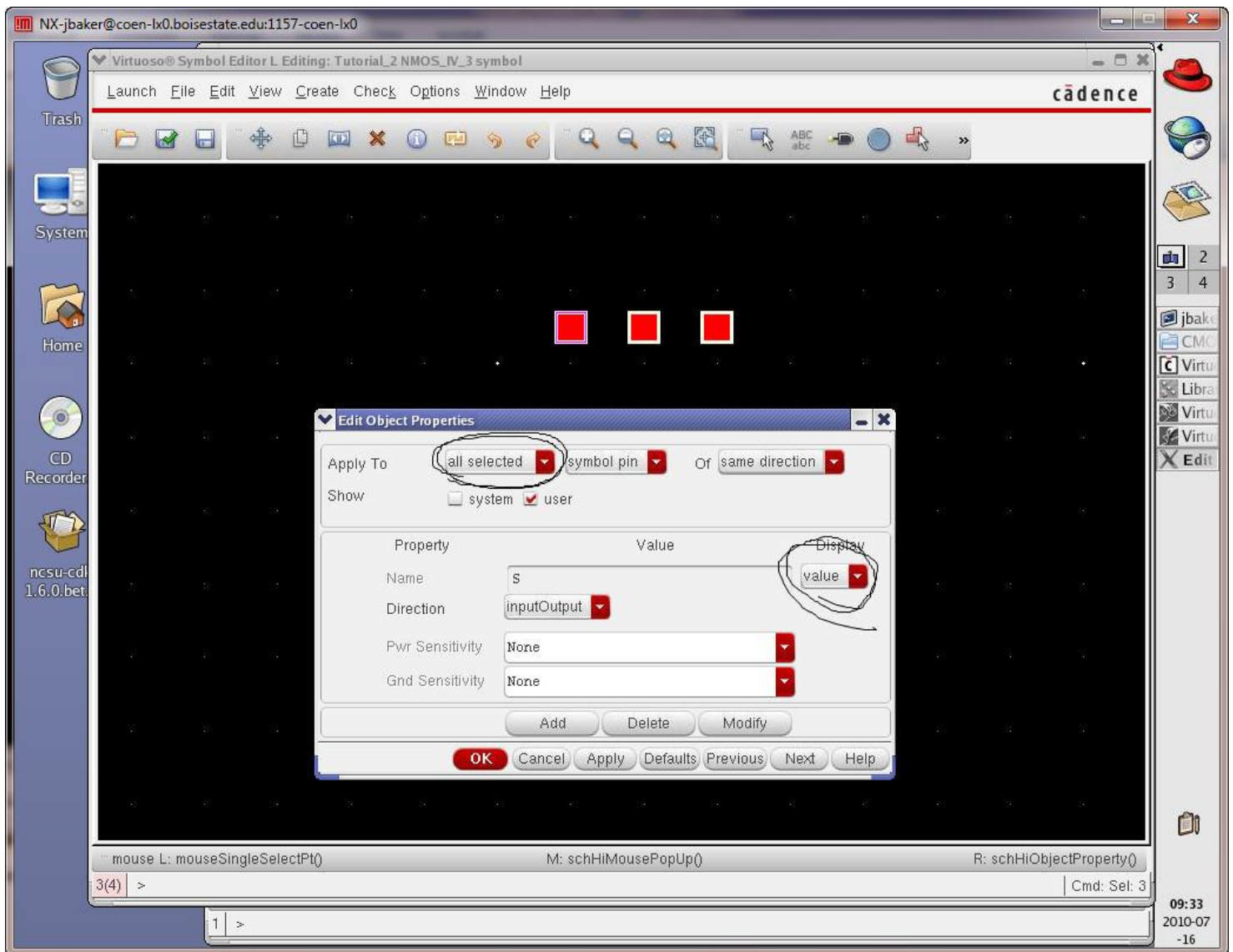
Virtuoso will ask where the pins should be located (it doesn't matter). Hit OK.
Delete everything in the cell except the pins.



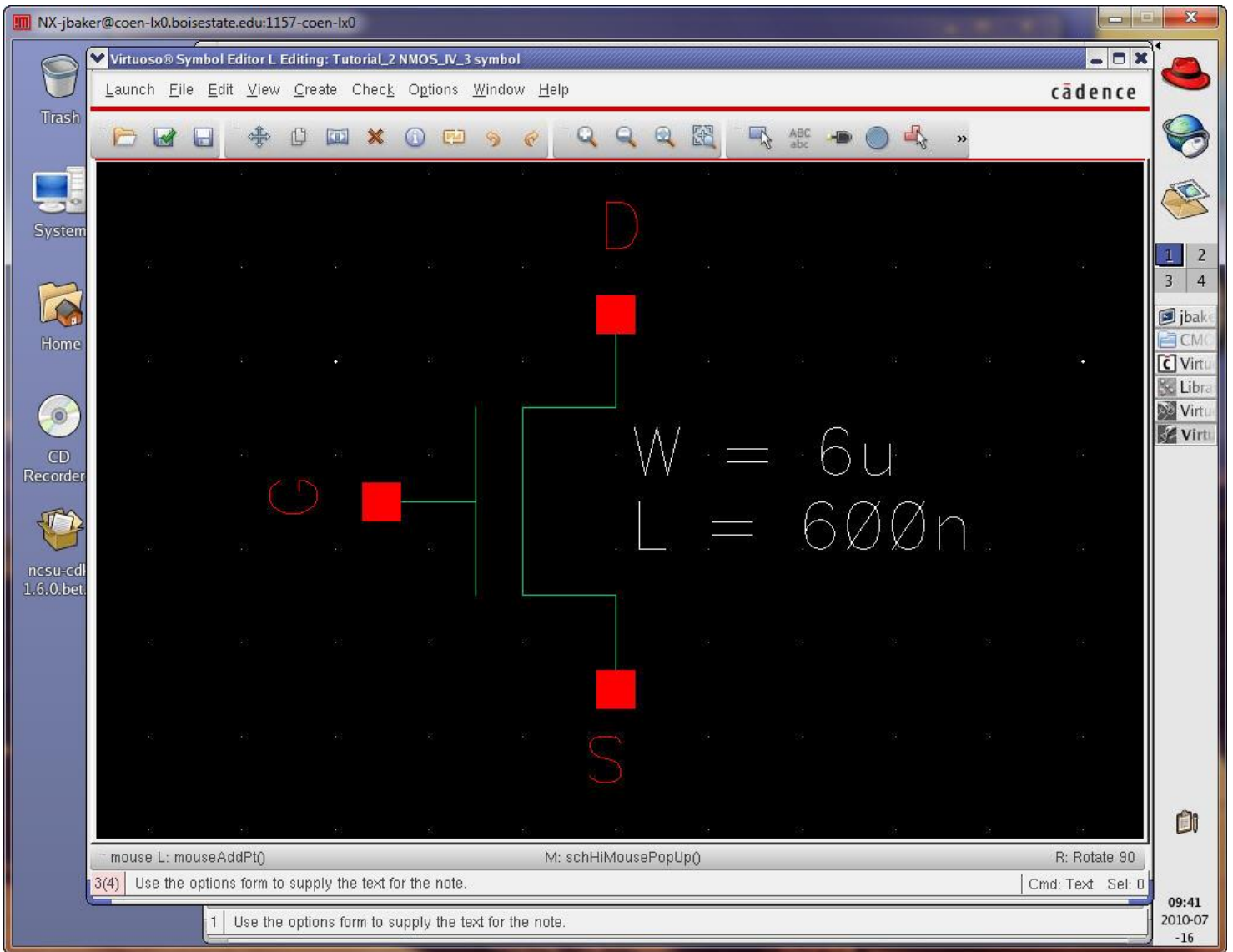
Notice we can't see the pin names.

Select all of the pins and then edit their properties (q).

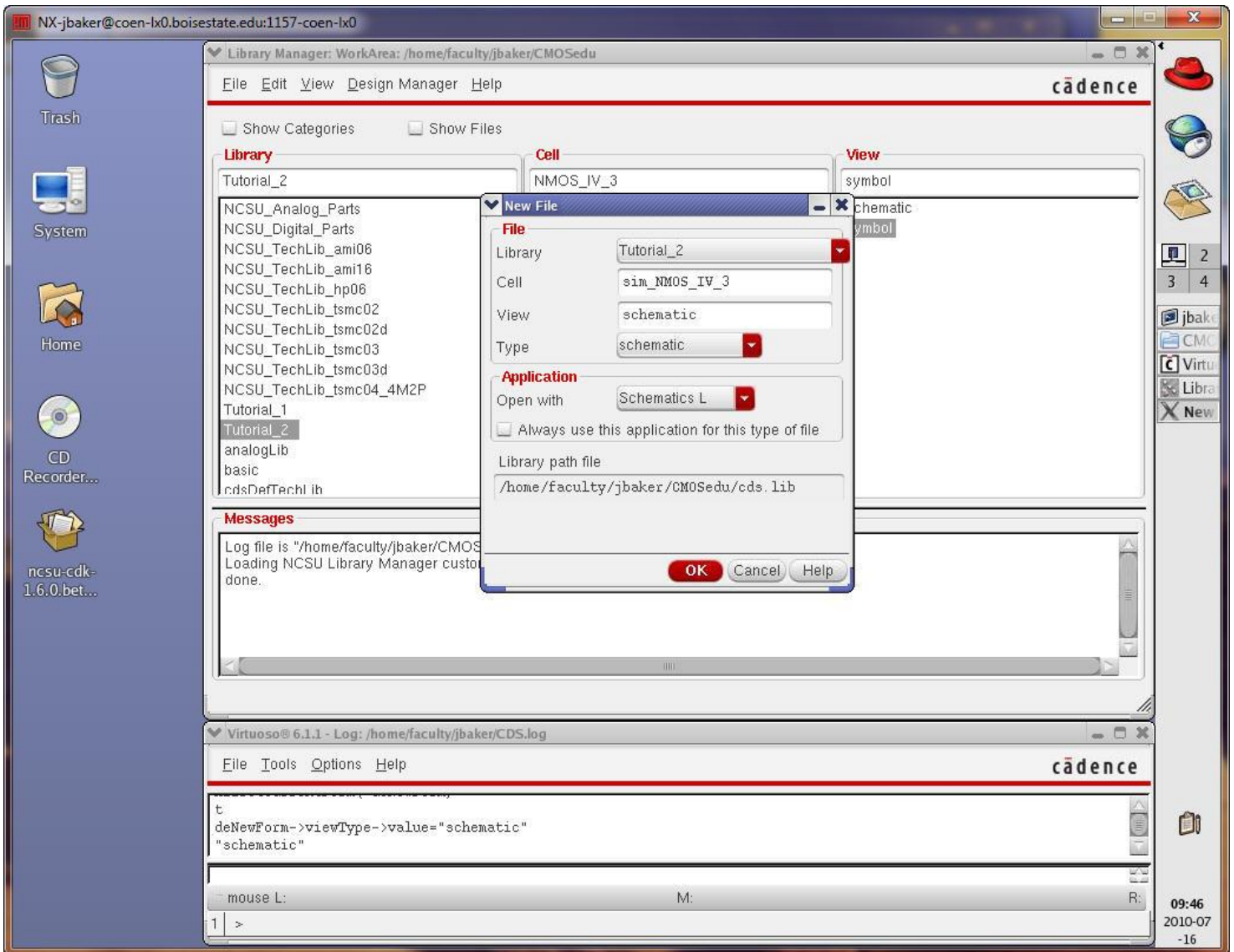
Select "all selected" and Display "value" as seen below.



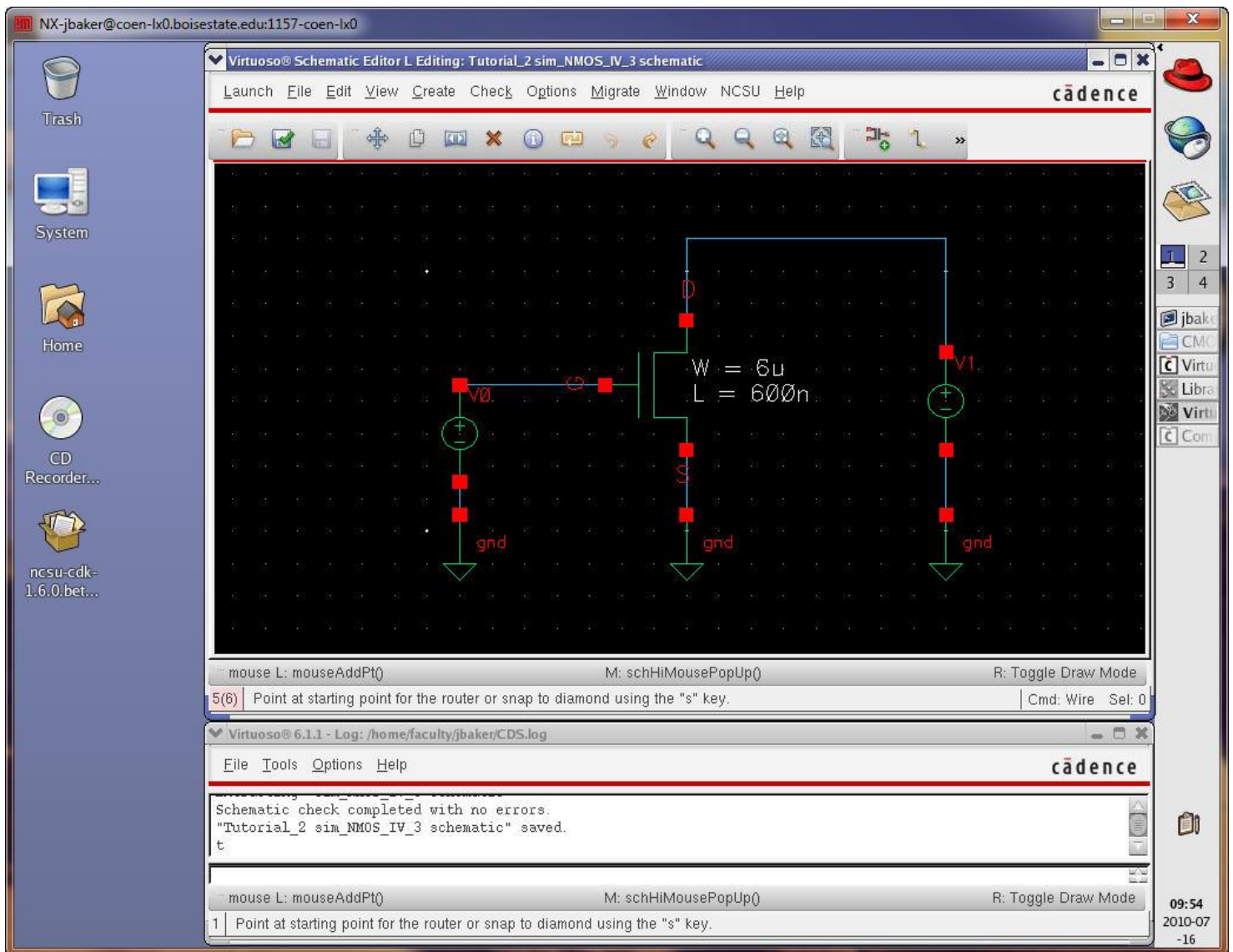
Draw a MOSFET symbol and move the pins (rotate as necessary) to get (something similar to) the following.
 Remember to draw a line use Create -> Shape -> Line.
 Adding the width and length text using Create -> Note -> Text
 When finished "Check and Save"



Next, create, File -> New -> Cell View, a cell (schematic) called sim_NMOS_IV_3.



Instantiate the NMOS_IV_Cell View just created and the DC voltage sources seen below (and wire things together).



Notice how the wires are drawn through the pin names? This is sloppy so let's fix it.

Use the Library Manager to open the NMOS_IV_3 symbol.

Move the labels as seen below. You'll need to rotate the G once and the S twice (right+click the mouse while moving).

"Check and Save" the Symbol, close it, then return to the sim_NMOS_IV_3 schematic.

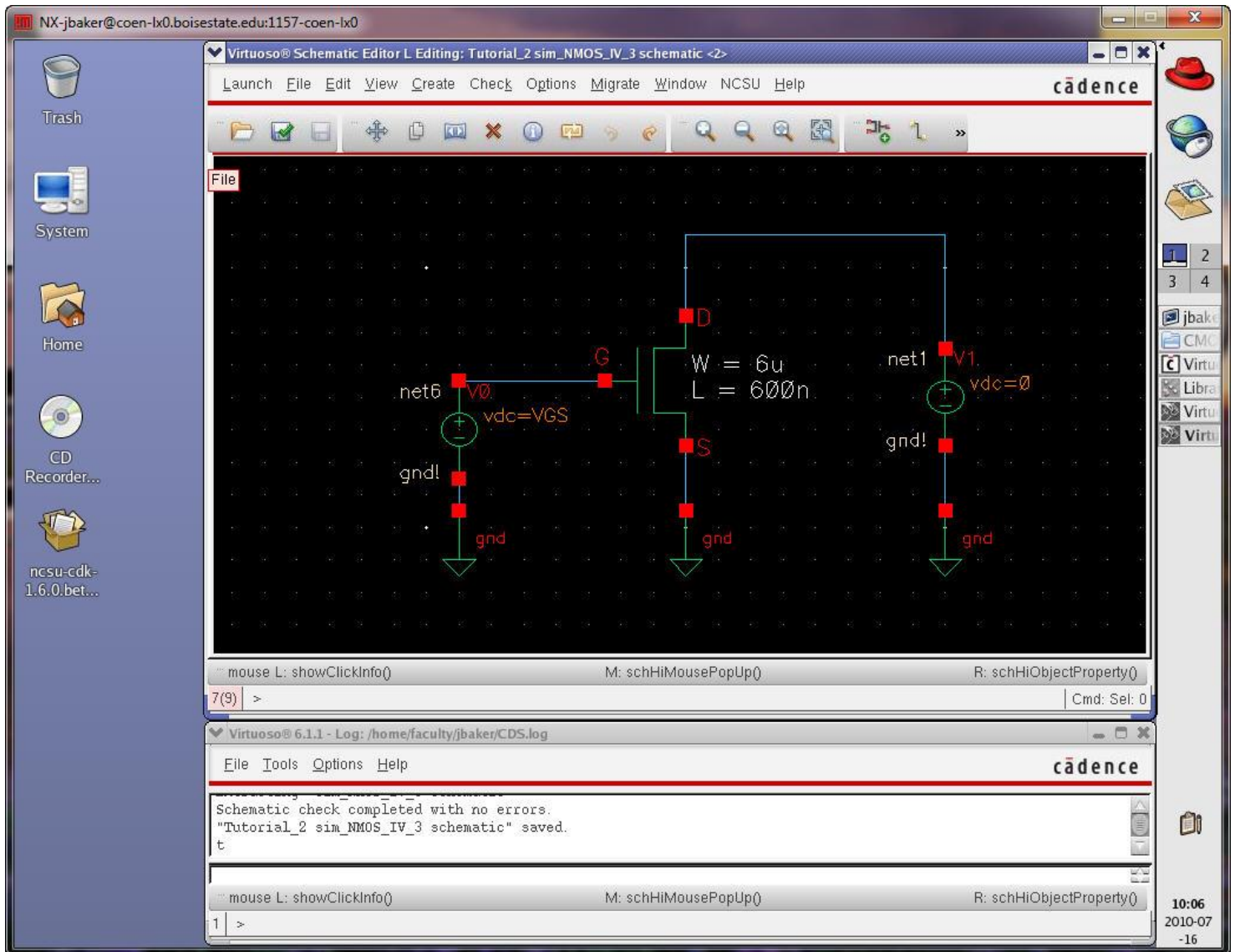
The screenshot shows the Cadence Virtuoso Symbol Editor L interface. The main workspace is a black canvas with a circuit diagram drawn in green lines. The diagram consists of a central vertical line with a horizontal branch to the left. A red square is placed on the horizontal branch, with a red letter 'G' to its left. The central vertical line has a red square at the top, with a red letter 'D' to its right, and another red square at the bottom, with a red letter 'S' to its right. A white box highlights the bottom red square. To the right of the circuit, the handwritten equations $W = 6u$ and $L = 600n$ are visible. The interface includes a menu bar (Launch, File, Edit, View, Create, Check, Options, Window, Help), a toolbar with various icons, and a status bar at the bottom with the text "mouse L: mouseAddPt()", "M: schHiMousePopUp()", and "R: Rotate 90". The system tray on the right shows the time "09:59" and date "2010-07-16".

The screenshot shows the Cadence Virtuoso Schematic Editor interface. The main window displays a schematic diagram of an NMOS transistor circuit. The circuit includes a voltage source V_0 connected to the gate (G) of an NMOS transistor. The transistor's width (W) is 6μ and length (L) is $600n$. The source (S) and drain (D) are connected to ground. A voltage source V_1 is connected to the drain (D) and ground. The schematic is titled "Tutorial_2 sim_NMOS_IV_3 schematic". The interface shows the Cadence logo, menu bar, and toolbar. The bottom status bar displays "10:03 2010-07 -16".

We are almost ready to simulate.

Set the value of V_0 to V_{GS} and the value of V_1 to 0 as seen below.

Check and Save the schematic.

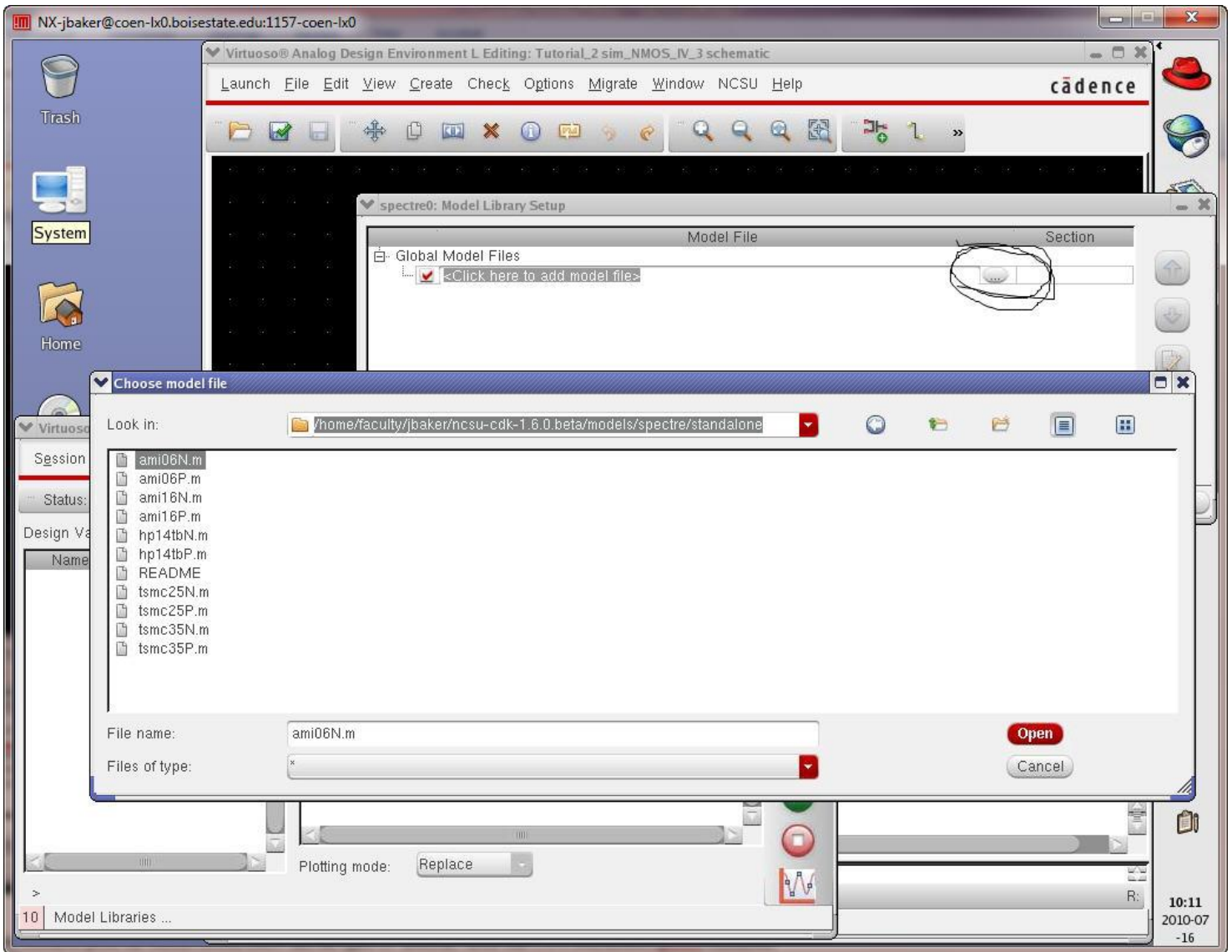


Launch the ADE.

Go to the menu Setup -> Model Libraries press the button circled below and navigate to $HOME/ncsu-cdk-1.6.0.beta/models/spectre/standalone$

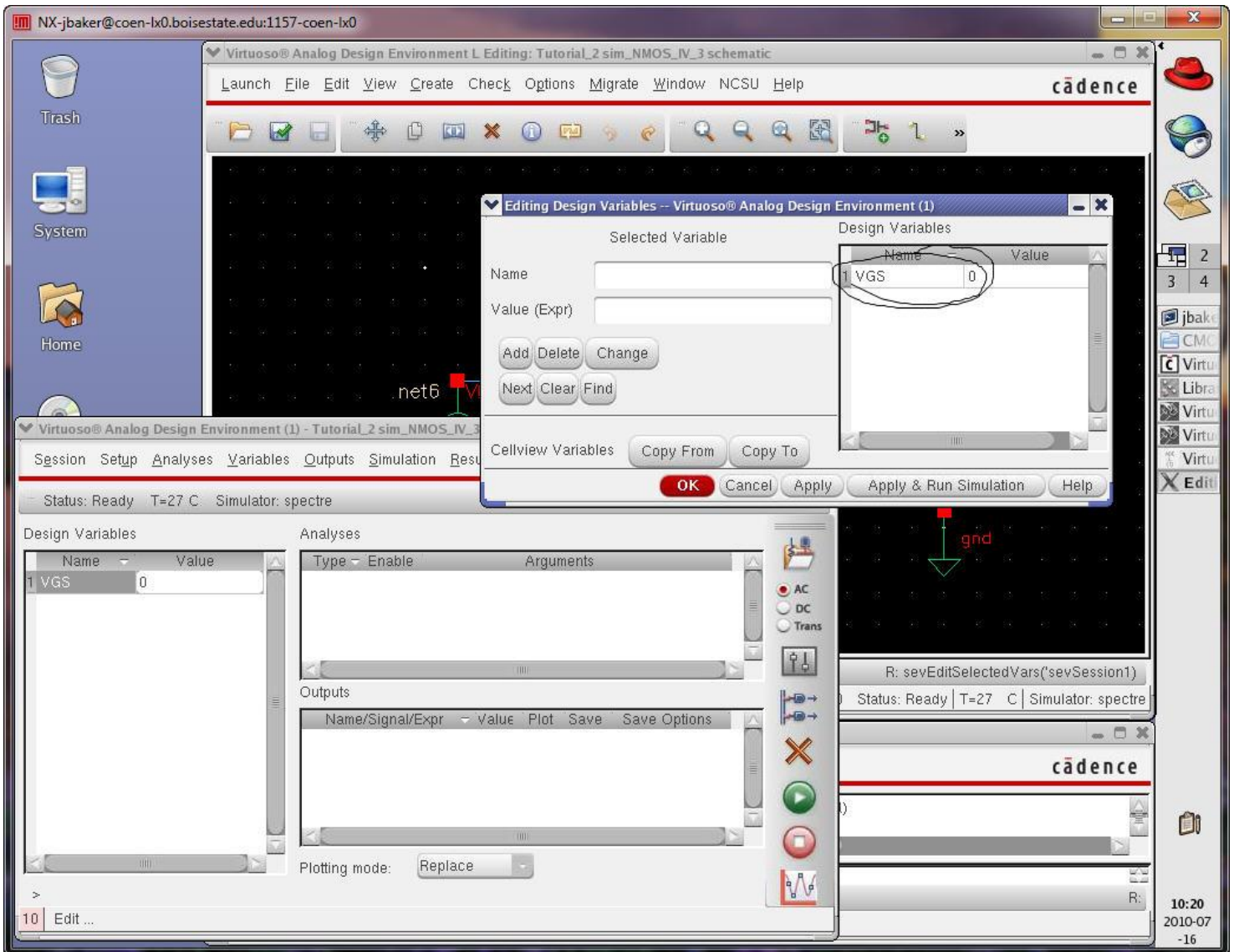
Select ami06N.m (NMOS model) then Press Open and OK.

Note that for general purpose simulation we would also select ami06P.m for the PMOS models.



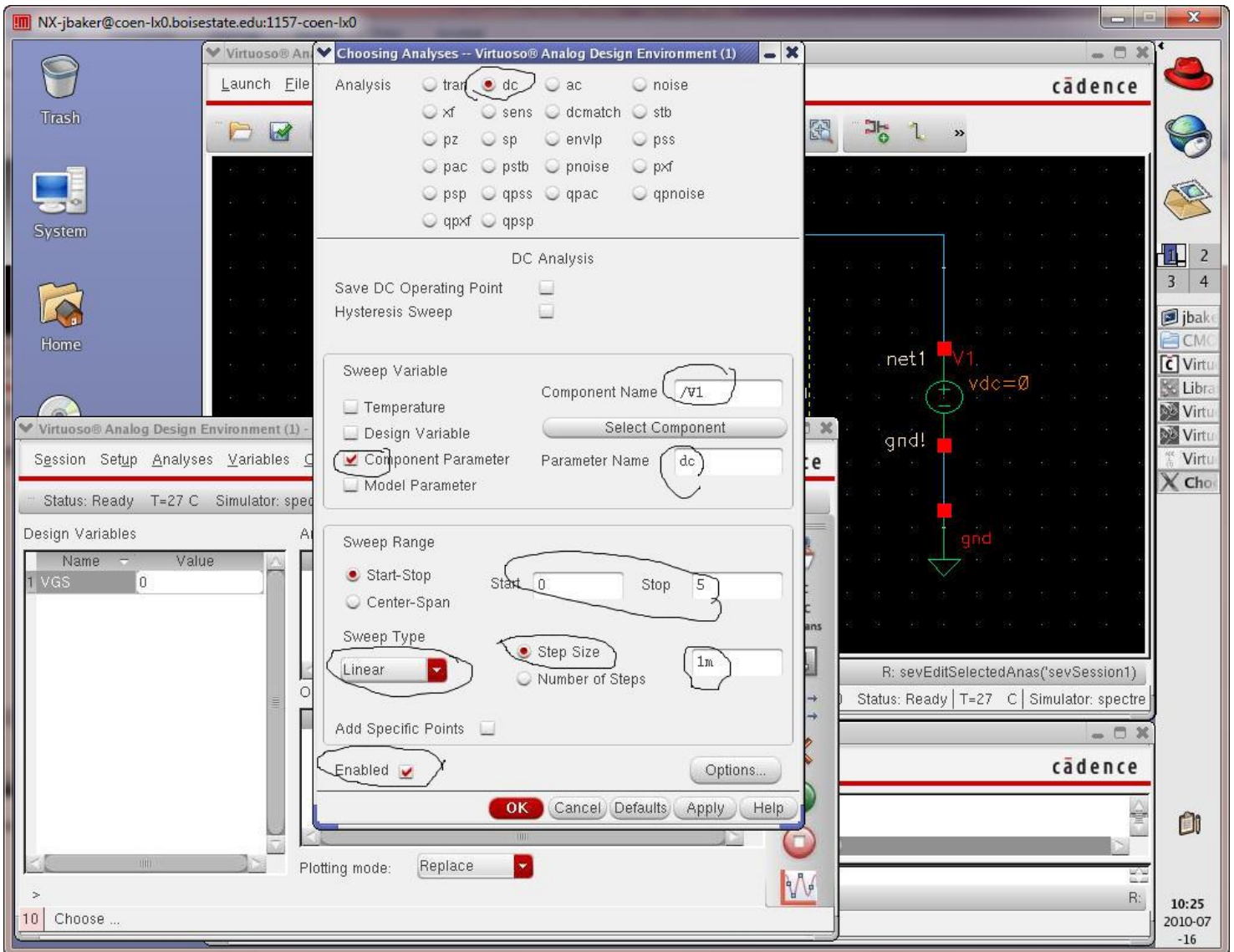
Next, in the ADE window, select Variables -> Edit and add VGS (value for the left DC voltage source in our schematic) and an arbitrary value of 0.

Press OK and notice how the Design Variable shows up in the ADE.



Next select Analyses -> Choose and set the parameters seen below.

Note that V1 is the right DC voltage source in the schematic connected to the Drain.



Select Output -> To Be Plotted -> Select On Schematic and click on the D Pin to select the current.
Ensure that both plotted and saved are selected, circled below.

The screenshot displays the Cadence Virtuoso Analog Design Environment. The main window shows a schematic diagram of a circuit with a MOSFET model. The MOSFET parameters are $W = 6\mu$ and $L = 600n$. The circuit includes a gate terminal connected to a node labeled 'net6', a drain terminal connected to a node labeled 'net1', and a source terminal connected to ground ('gnd!'). A voltage source 'V1' is connected between 'net1' and 'gnd!', with a DC voltage of $vdc=0$. A current source 'G' is also present in the circuit.

An overlay window titled 'Virtuoso@ Analog Design Environment (1) - Tutorial_2 sim_NMOS_IV_3 schematic' is open, showing the simulation configuration. The 'Design Variables' table is as follows:

Name	Value
VGS	0

The 'Analyses' table shows a DC analysis:

Type	Enable	Arguments
dc	<input checked="" type="checkbox"/>	0 5 1m Linear Step Size Start-Stop /V1

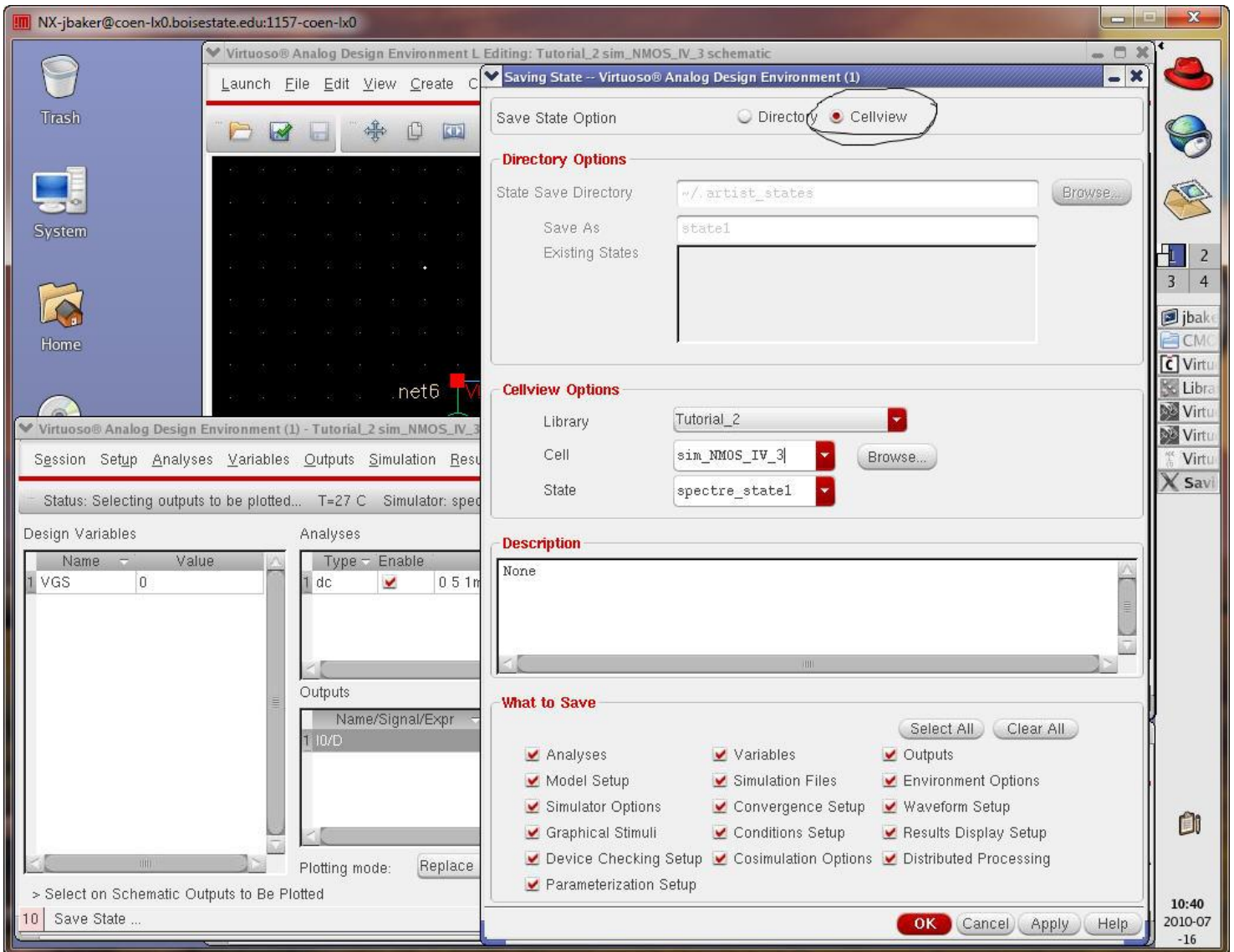
The 'Outputs' table shows the output configuration for the current source 'I0/D':

Name/Signal/Expr	Value	Plot	Save	Save Options
I0/D		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes

The 'Plotting mode' is set to 'Replace'. The status bar at the bottom indicates '10 Select On Schematic'.

Now let's save the simulation state.

Select Session -> State and save the in the Cell View (you can use the Library Manager to verify it has been saved).



Next choose Tools -> Parametric Analysis and set the parameters seen below.

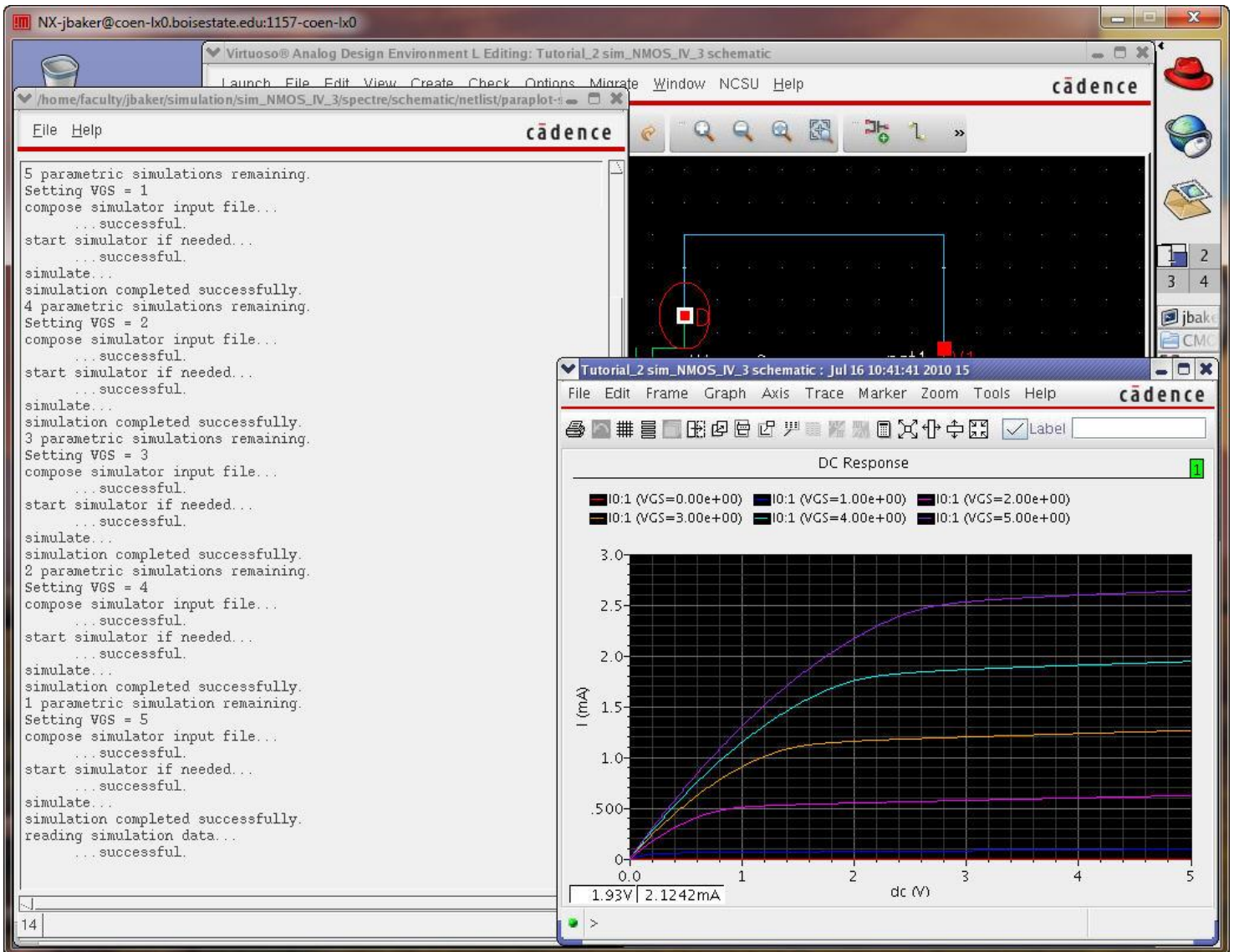
The screenshot displays the Cadence Virtuoso Analog Design Environment. The main window shows a schematic diagram of a MOSFET circuit. The MOSFET is connected to a gate terminal (G) and a drain terminal (D). The gate is connected to a voltage source (V0) and a gate terminal (G). The drain is connected to a voltage source (V1) and a drain terminal (D). The source is connected to ground (gnd!). The MOSFET parameters are set to $W = 6\mu$ and $L = 600n$. The schematic also shows a net1 and a net6. The voltage source V1 is labeled with $vdc=0$.

The Parametric Analysis window is open, showing the following settings:

- Sweep 1: Variable Name: **VGS**
- Range Type: **From/To**
- From: **0**
- To: **5**
- Step Control: **Linear Steps**
- Step Size: **1**

The status bar at the bottom right shows the date and time: 10:33 2010-07 -16.

Finally, select Analysis and Start, in the Parametric Analysis window, to see the MOSFET IV curves below.



Note that we could have avoided making the symbol view so that plotting these curves would take less effort.

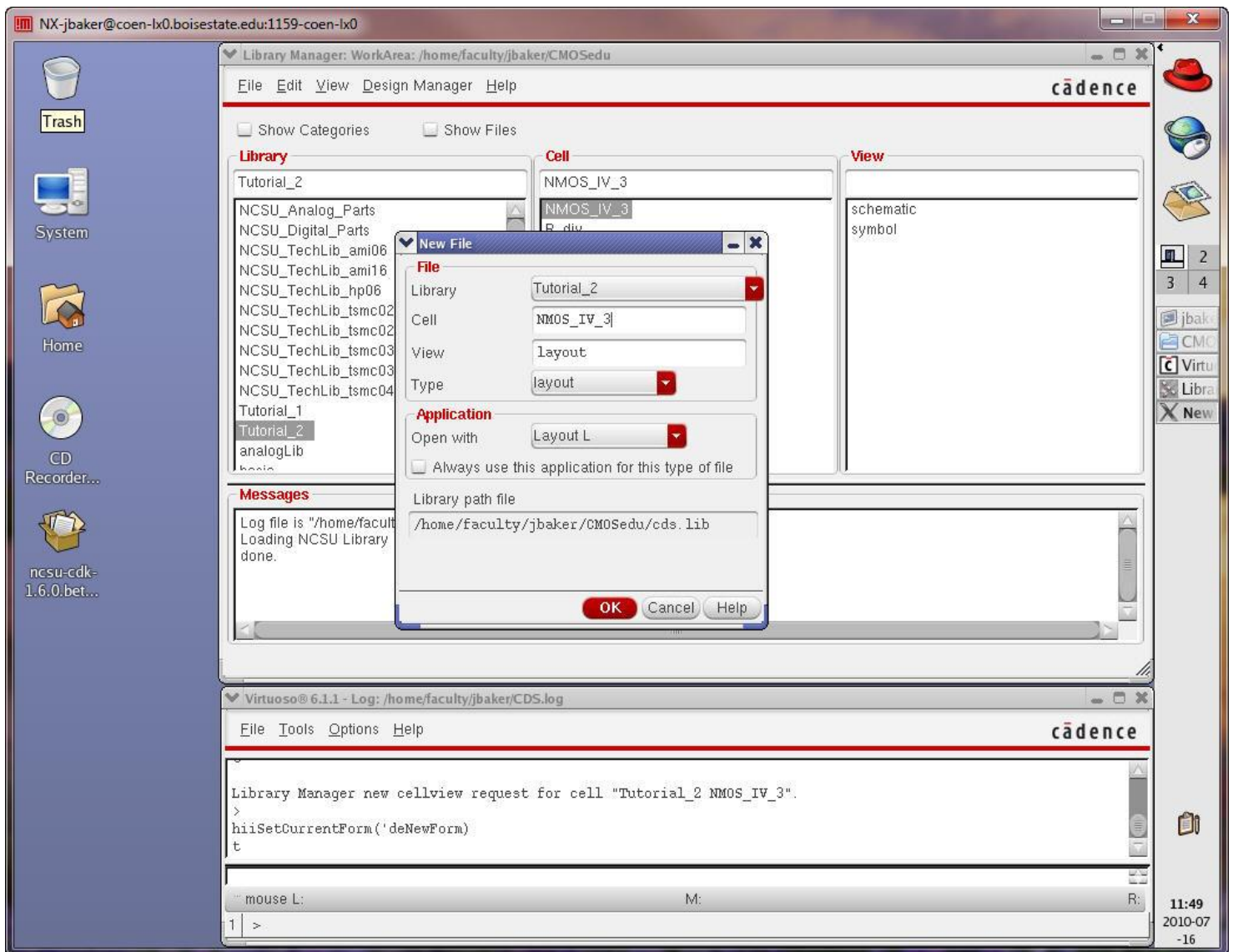
Why we chose this path will become clearer later in the tutorial (having a symbol allows us to simulate either the schematic or extracted, from layout, views)

Quit the ADE and Save the State (okay to overwrite existing state).

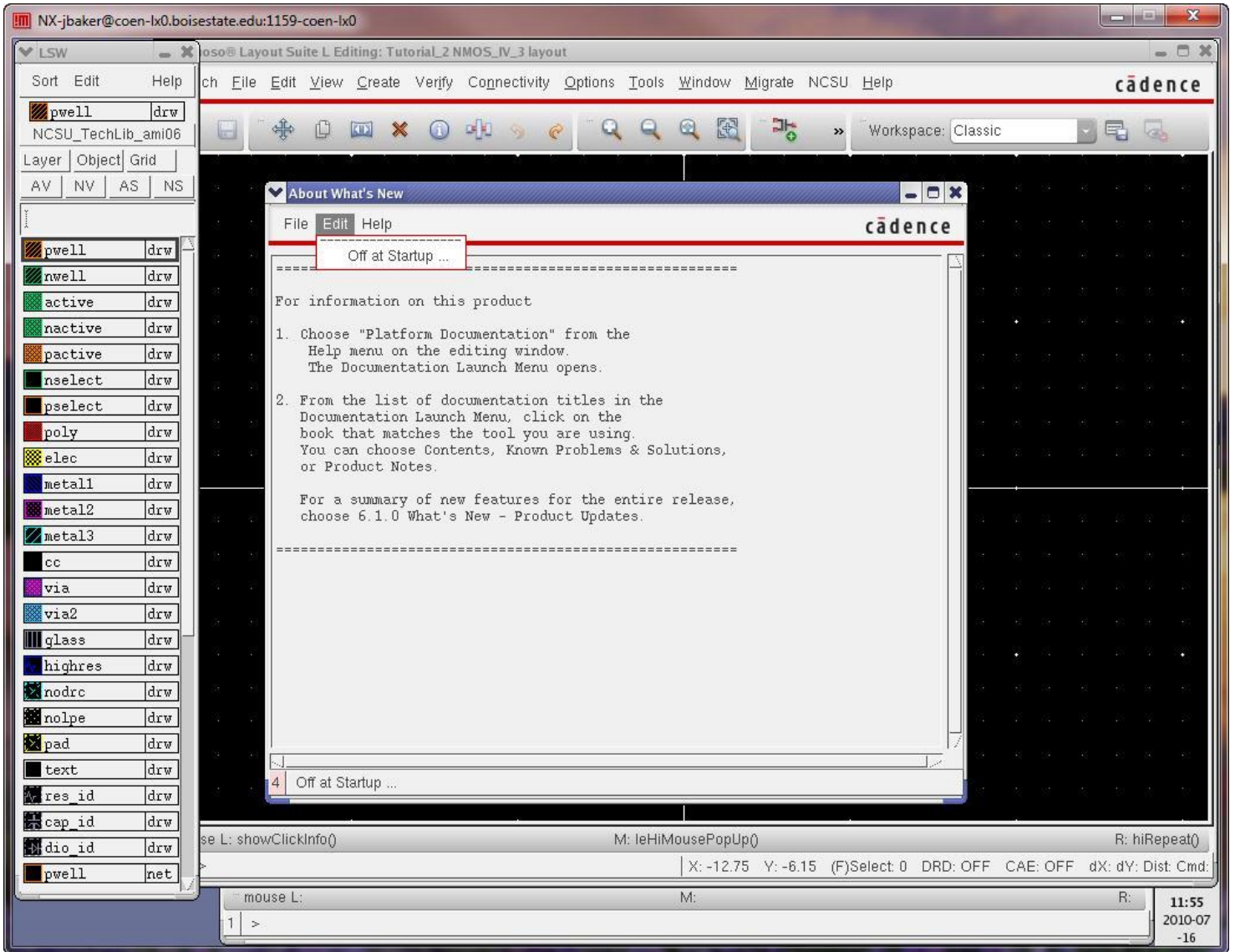
Close the schematic of sim_NMOS_IV_3 (close all Cell Views).

We are now ready to lay out this cell and simulate it.

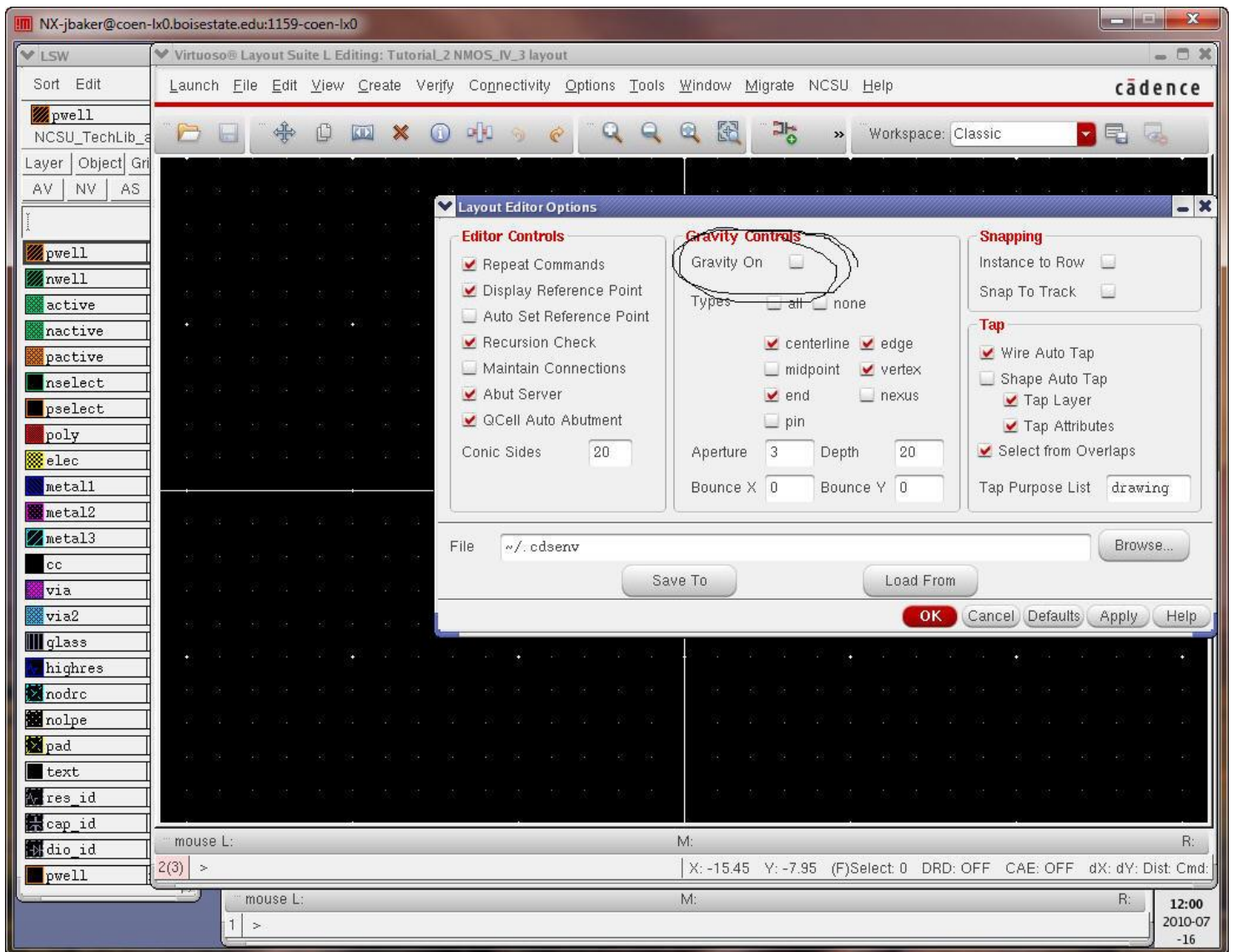
Create a layout view for NMOS_IV_3 (not sim_NMOS_IV_3)



We get that pesky start-up Window again even though we set it to be Off at Start-up before (below). We'll also see that our Editor Options, E, and Display Options, e, (also below) have reverted back to the original states. Change the values back to those seen below.



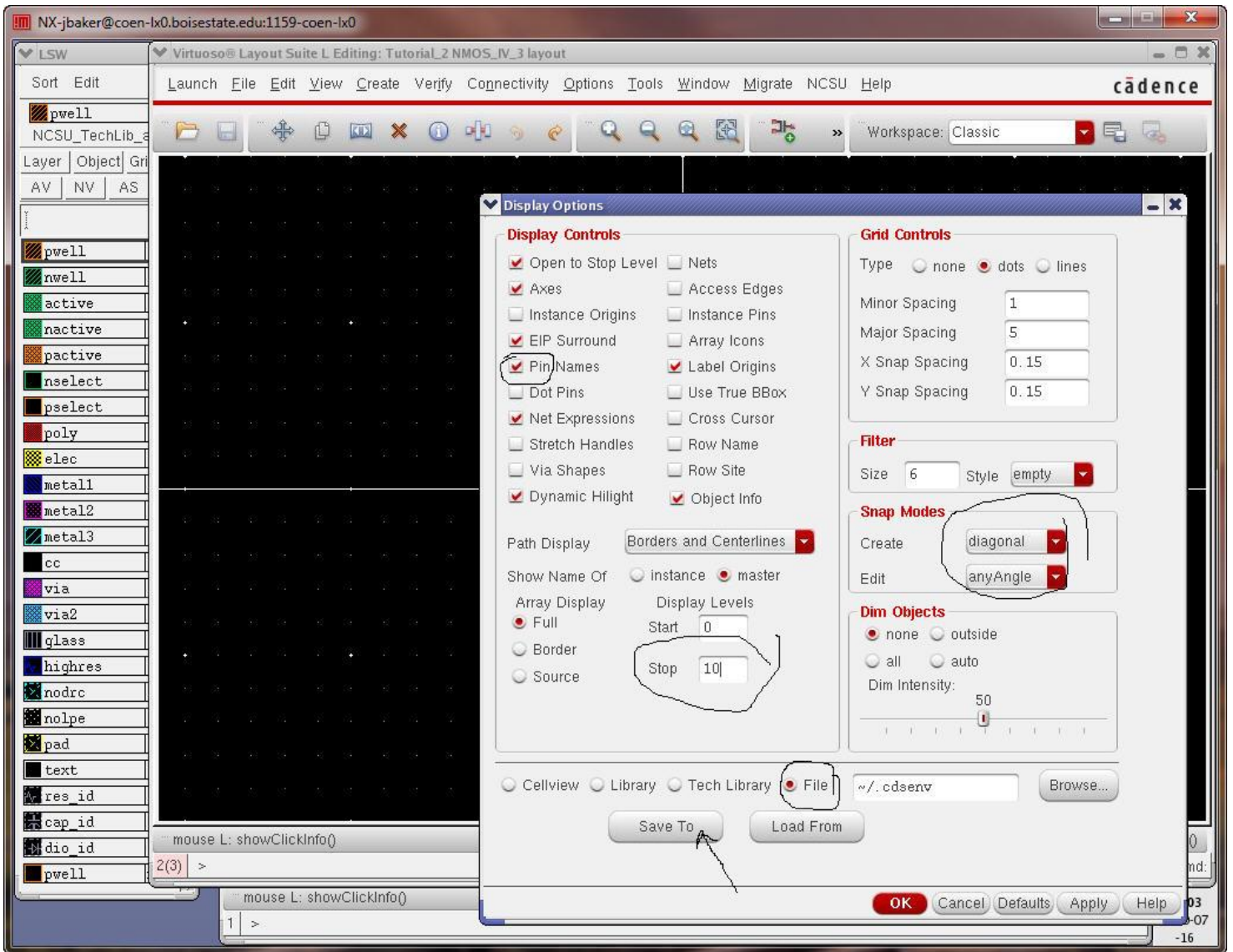
e



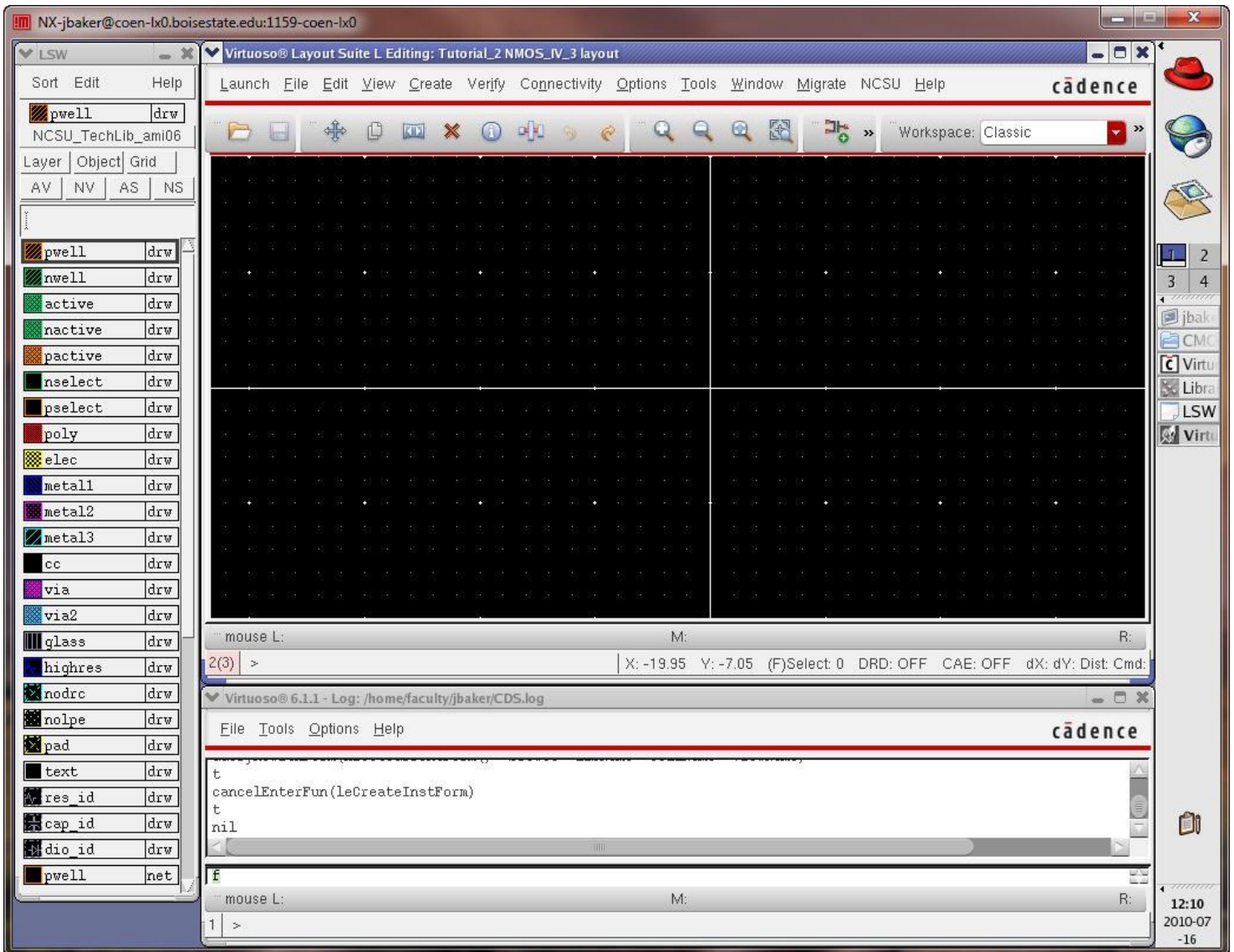
After pressing **e** we get the following.

To ensure that the options are remembered Save To File (the CDS, Cadence Design System, Environment, .cdserv) as seen below (saved in \$HOME, aka, ~/).

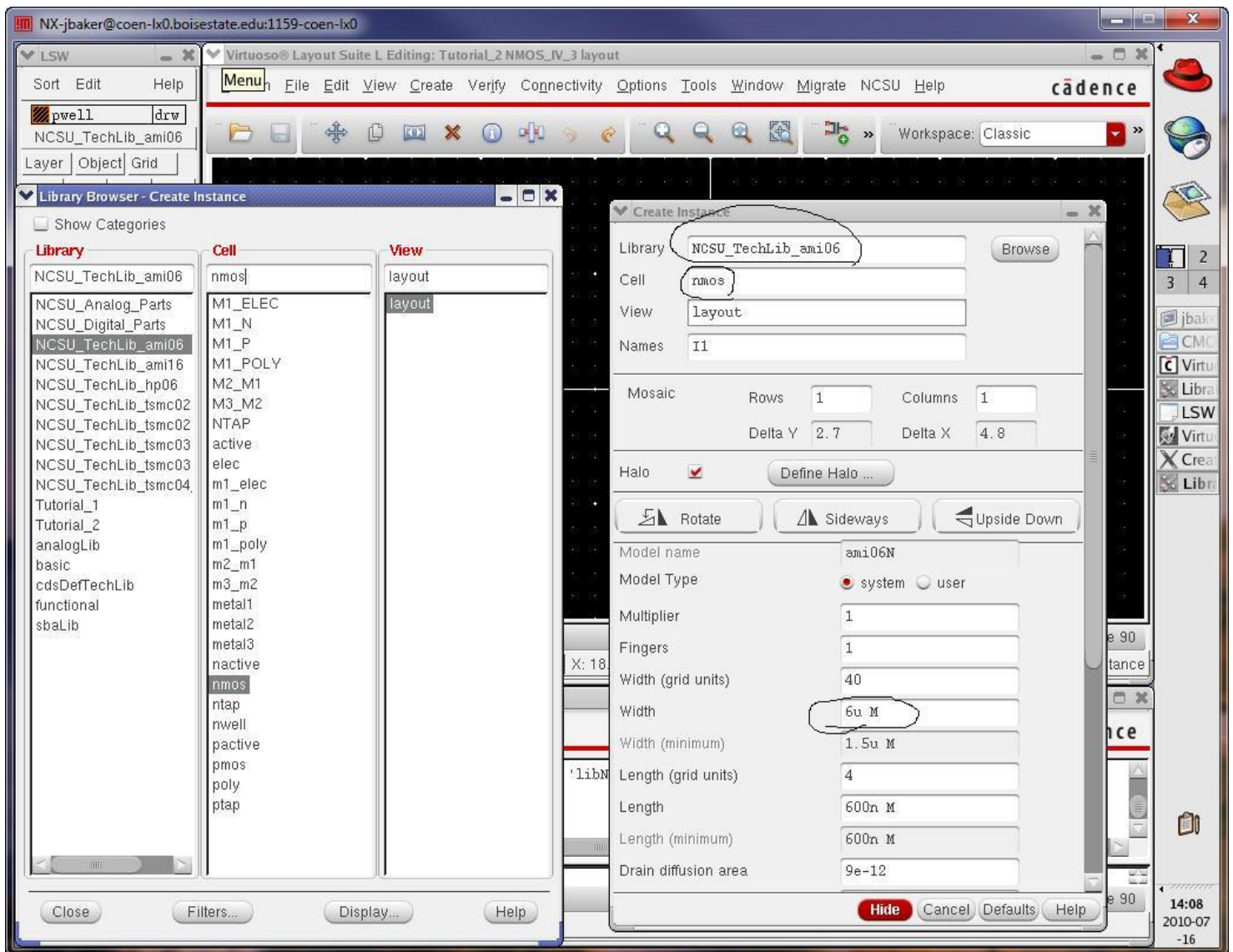
Note that to see the Save To button you may need to re-size the Display Options dialog window.



When finished hit OK and re-size the layout window as seen below.



Next instantiate an nmos device that is 6 um wide and 600 nm long.



Next instantiate a ptap cell (metal1 connection to p+) in the p-substrate so you get something that looks like the following. DRC the layout (Verify -> DRC then OK).

The screenshot displays the Cadence Virtuoso Layout Suite L Editing interface. The main window shows a layout design for a cell named "NMOS_IV_3 layout". The layout features a central gate structure with a red vertical line and a blue horizontal line, surrounded by a green rectangular region. Below the gate structure is a square pad. The interface includes a menu bar (Launch, File, Edit, View, Create, Verify, Connectivity, Options, Tools, Window, Migrate, NCSU, Help) and a toolbar. The workspace is set to "Classic".

On the left side, there is a layer list (LSW) with the following items:

Layer	Object	Grid	
pwell	drw		
NCSU_TechLib_ami06			
Layer	Object	Grid	
AV	NV	AS	NS

Below the layer list, there is a list of objects with their respective layers:

pwell	drw
nwell	drw
active	drw
nactive	drw
pactive	drw
nselect	drw
pselect	drw
poly	drw
elec	drw
metal1	drw
metal2	drw
metal3	drw
cc	drw
via	drw
via2	drw
glass	drw
highres	drw
nodrc	drw
nolpe	drw
pad	drw
text	drw
res_id	drw
cap_id	drw
dio_id	drw
pwell	net

At the bottom of the main window, there is a status bar with the following information:

mouse L: Set Entry Layer M: Toggle Visibility R: Toggle Selectability
 2(3) > | X: -2.85 Y: 3.30 (F)Select: 0 DRD: OFF CAE: OFF dX: dY: Dist: Cmd:

Below the main window, there is a log window titled "Virtuoso@ 6.1.1 - Log: /home/faculty/jbaker/CDS.log". The log window shows the following output:

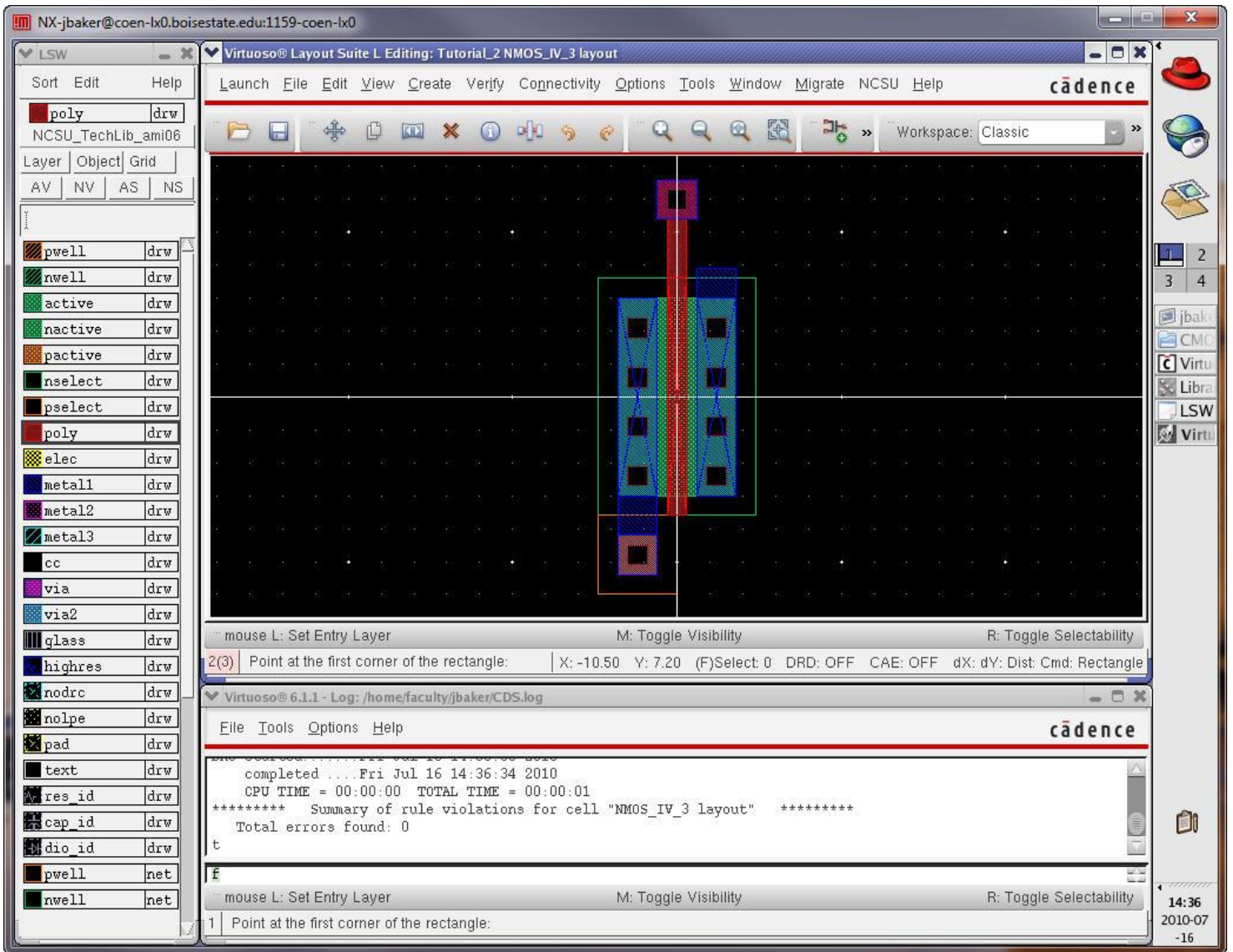
```
File Tools Options Help
CPU TIME = 00:00:00 TOTAL TIME = 00:00:01
***** Summary of rule violations for cell "NMOS_IV_3 layout" *****
Total errors found: 0
t
f
```

At the bottom of the log window, there is a status bar with the following information:

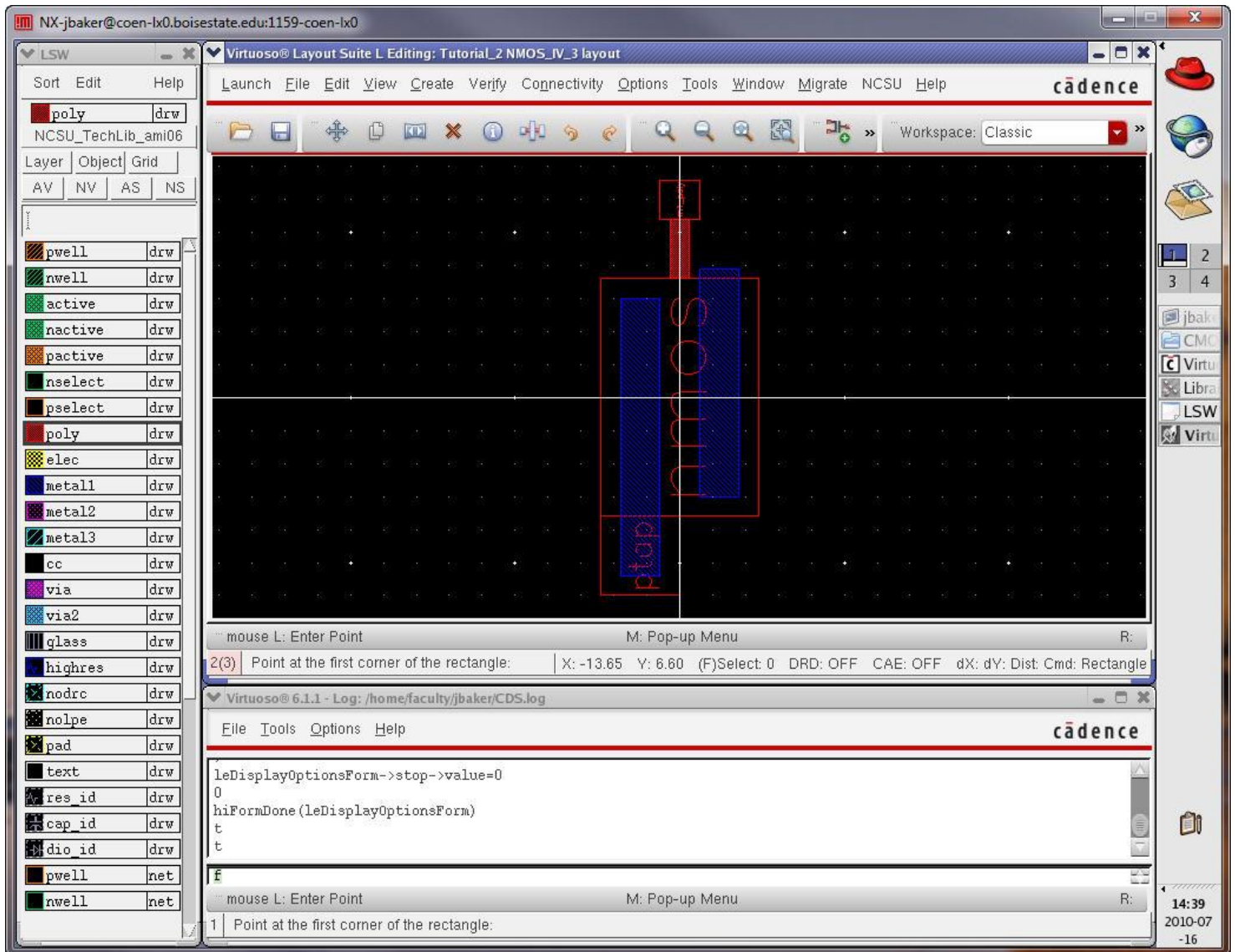
mouse L: Set Entry Layer M: Toggle Visibility R: Toggle Selectability
 1 >

The system clock in the bottom right corner shows 14:13 on 2010-07-16.

Next add rectangles on the metal1 layer to connect the source to the p-substrate and to the drain. Also add a metal1-connection-to-poly cell (m1_poly) and a poly rectangle to connect the gate to m1_poly. DRC your layout.



Pressing e and then setting the display level stop to 0 we can see the rectangles and cells.



Set the display stop level back to 10.

Add D, G, and S Pins on metal1 as seen below.

Ensure "Display Pin Name" is selected and I/O type is inputOutput to match the pins in the schematic.

Draw the pins so they overlap the metal1.

DRC the layout to ensure no errors (fix errors if you find them).

Save the cell view.

The screenshot displays the Cadence Virtuoso Layout Suite L Editing environment. The main window shows a layout view of a cell named "NMOS_IV_3 layout". The layout features a central vertical structure with a red line and a blue shaded area. The interface includes a menu bar (Launch, File, Edit, View, Create, Verify, Connectivity, Options, Tools, Window, Migrate, NCSU, Help) and a toolbar. The workspace is set to "Classic".

On the left, the LSW (Library Manager) panel is visible, showing a list of objects and their layers. The "metal1" layer is selected. The list includes:

Object	Layer		
metal1	drw		
NCSU_TechLib_ami06			
Layer	Object	Grid	
AV	NV	AS	NS

pwell	drw		
nwell	drw		
active	drw		
nactive	drw		
pactive	drw		
nselect	drw		
pselect	drw		
poly	drw		
clct	drw		
metal1	drw		
metal2	drw		
metal3	drw		
cc	drw		
via	drw		
via2	drw		
glass	drw		
highres	drw		
nodrc	drw		
nolpe	drw		
pad	drw		
text	drw		
res_id	drw		
cap_id	drw		
dio_id	drw		
pwell	net		
nwell	net		

At the bottom, a terminal window titled "Virtuoso@6.1.1 - Log: /home/faculty/jbaker/CDS.log" displays the following output:

```

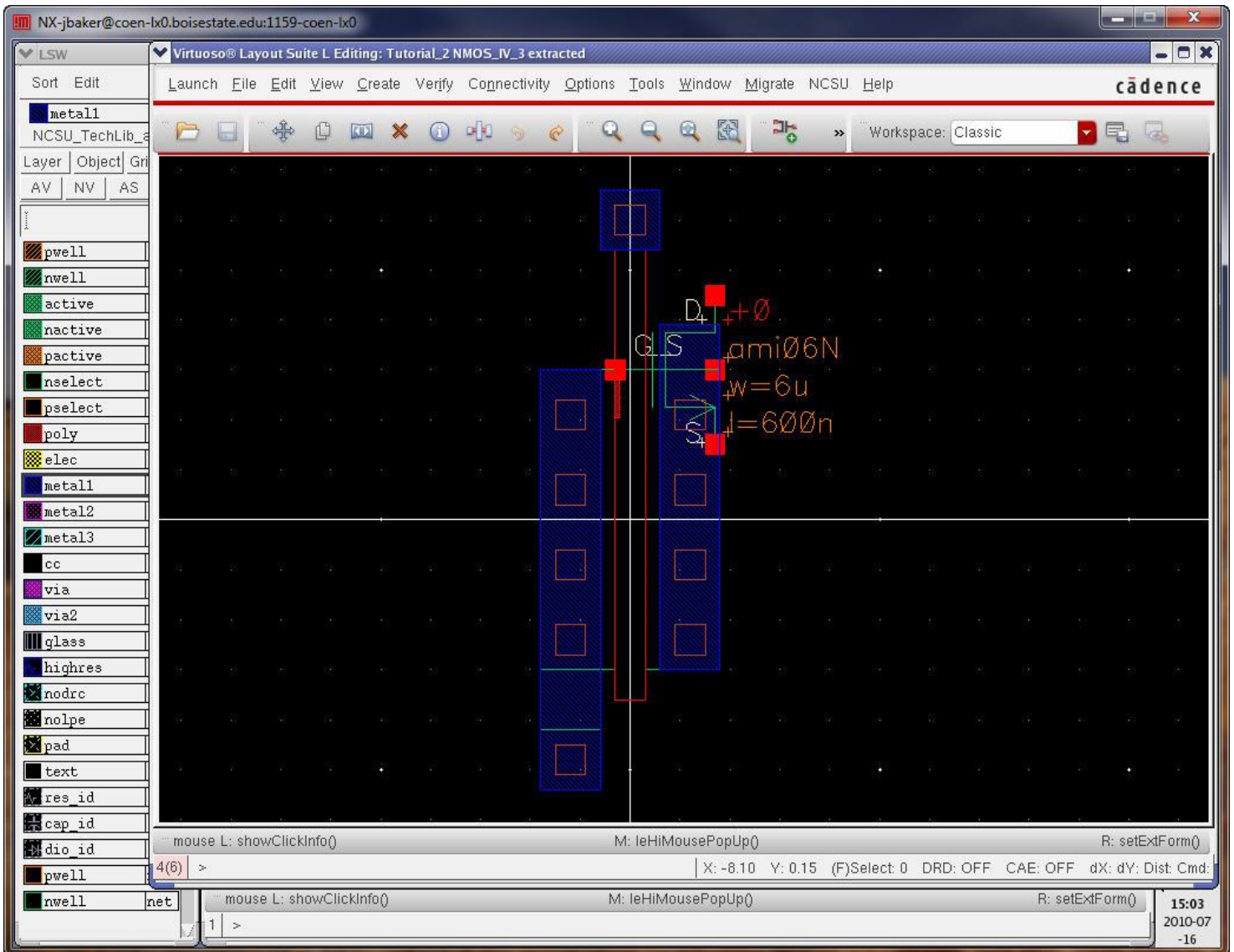
File Tools Options Help
-----
completed Fri Jul 16 14:58:15 2010
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "NMOS_IV_3 layout" *****
Total errors found: 0
t
fu
mouse L: M: R:
1 Use the options form to enter a valid terminal name:

```

The system clock in the bottom right corner shows 14:58 on 2010-07-16.

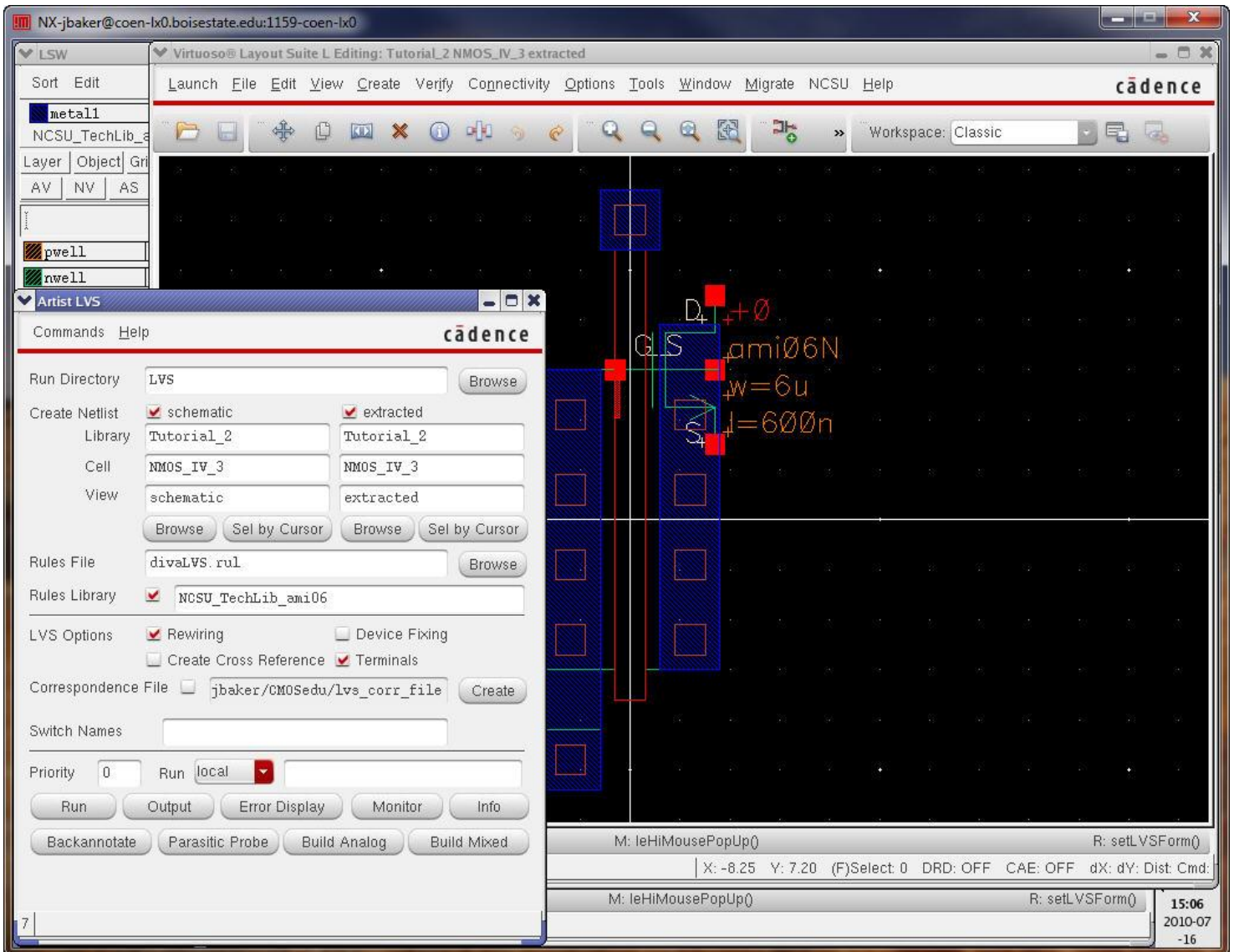
Next Extract the layout (Verify -> Extract).

Using the Library Manager open the extracted cell view (NMOS_IV_3).



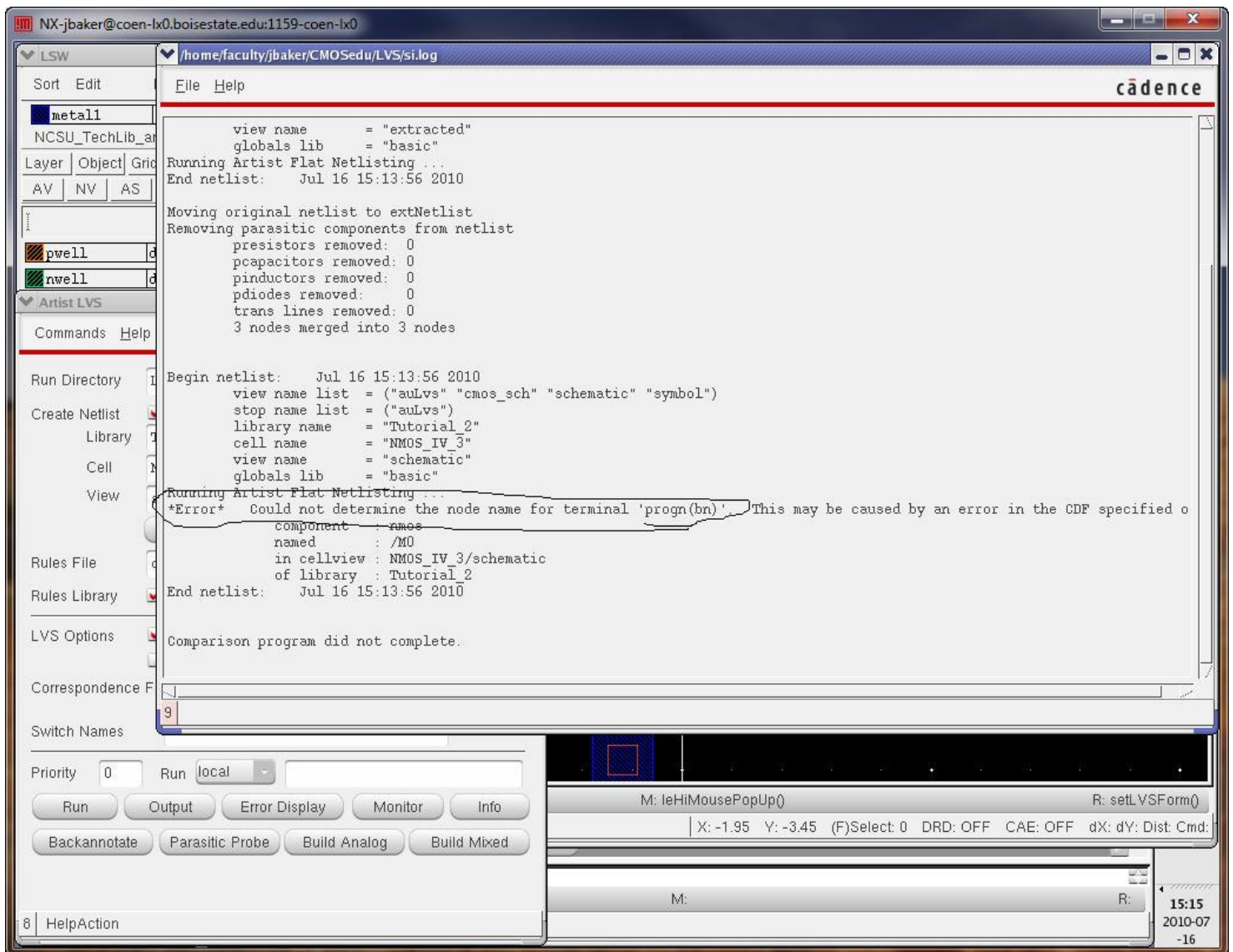
Notice that the symbol displayed here has 4 terminals, not the 3-terminal transistor we used in the schematic (where it's assumed the p-substrate is tied to gnd!)

Next run an LVS (Verify -> LVS).



After hitting Run you will be notified that the job failed. Click OK.

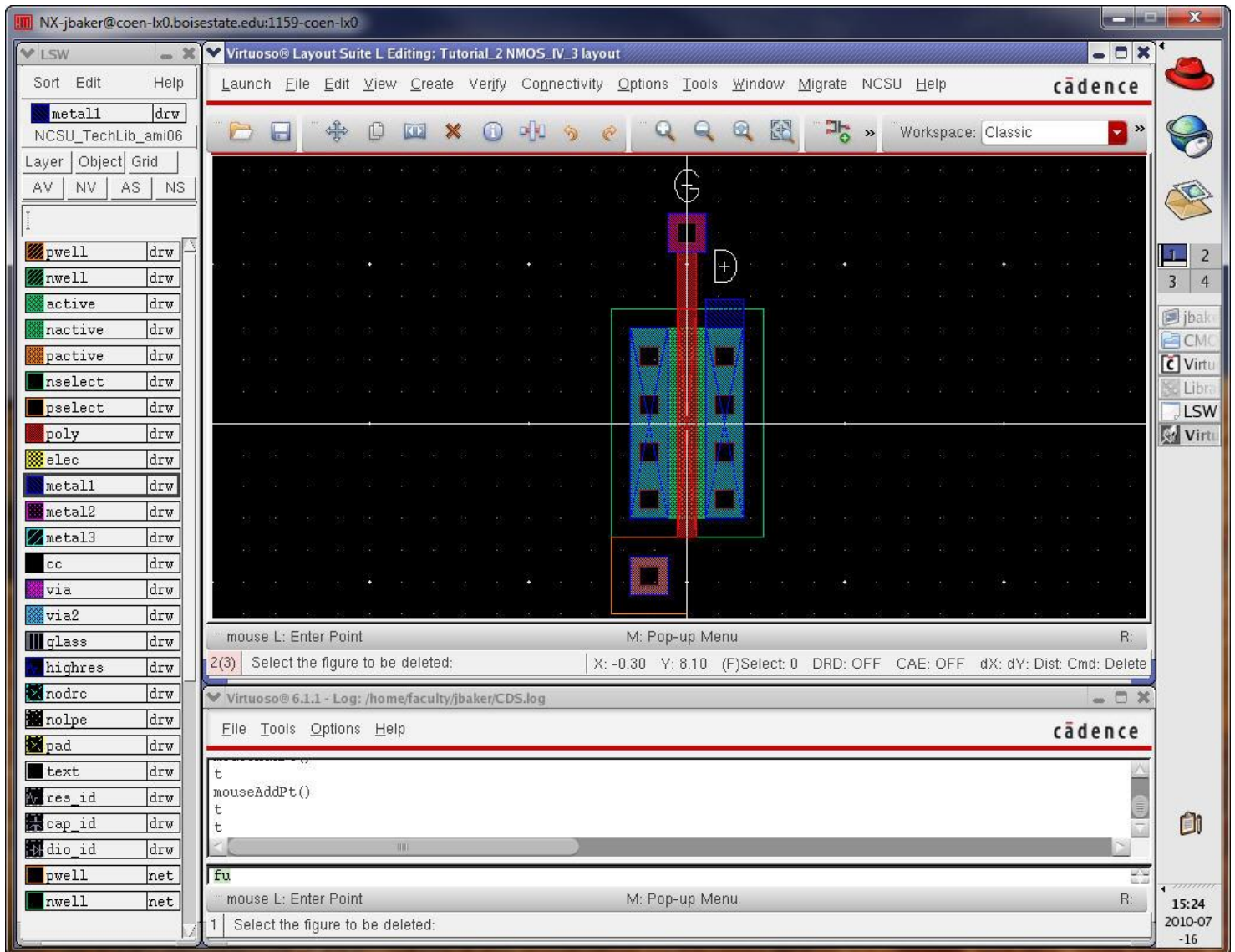
In the Artist LVS window click on Info and then Log File to get, after scrolling down, the following.



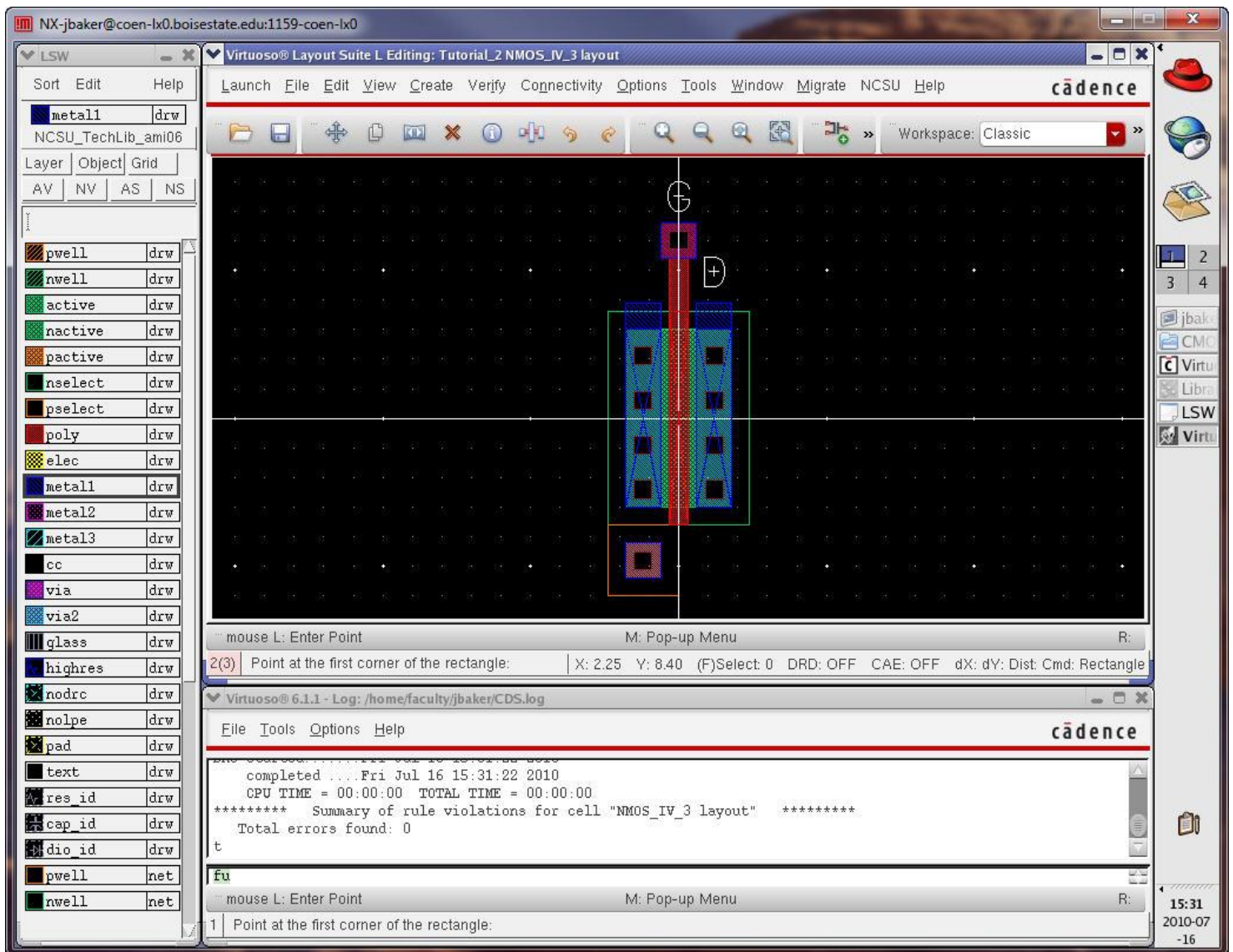
The error is related to the bulk (p-substrate) connection for the NMOS. Again, as mentioned above when the 3 terminal MOSFET symbol is used it's assumed that the bulk is tied to gnd! for an NMOS device and vdd! for a PMOS device.

Let's modify the layout as seen below.

Delete the metal1 rectangle and pin connecting the S to the bulk (ptap) as seen below.



Next, add metal rectangles on metal1 over the S and B metal.



Next add Pins, again make the Pin the same size as the metal1 rectangles (note that that making the Pins the same size is not a requirement).

Save your layout and DRC it.

The screenshot displays the Cadence Virtuoso Layout Suite L Editing interface. The main window shows a layout view of a cell named "NMOS_IV_3 layout". The layout features a central vertical red line, likely representing a signal path or a connection to ground. Several blue rectangular regions are visible, representing NMOS devices. A green box highlights a specific area, and a red box highlights another. The text ".gnd!" is visible in the layout view, indicating a connection to ground.

The left sidebar shows a list of layers and objects, including:

- metall1 drw
- NCSU_TechLib_ami06
- Layer Object Grid
- AV NV AS NS
- pwell drw
- nwell drw
- active drw
- nactive drw
- pactive drw
- nselect drw
- pselect drw
- poly drw
- elec drw
- metall1 drw
- metal2 drw
- metal3 drw
- cc drw
- via drw
- via2 drw
- glass drw
- highres drw
- nodrc drw
- nolpe drw
- pad drw
- text drw
- res_id drw
- cap_id drw
- dio_id drw
- pwell net
- nwell net

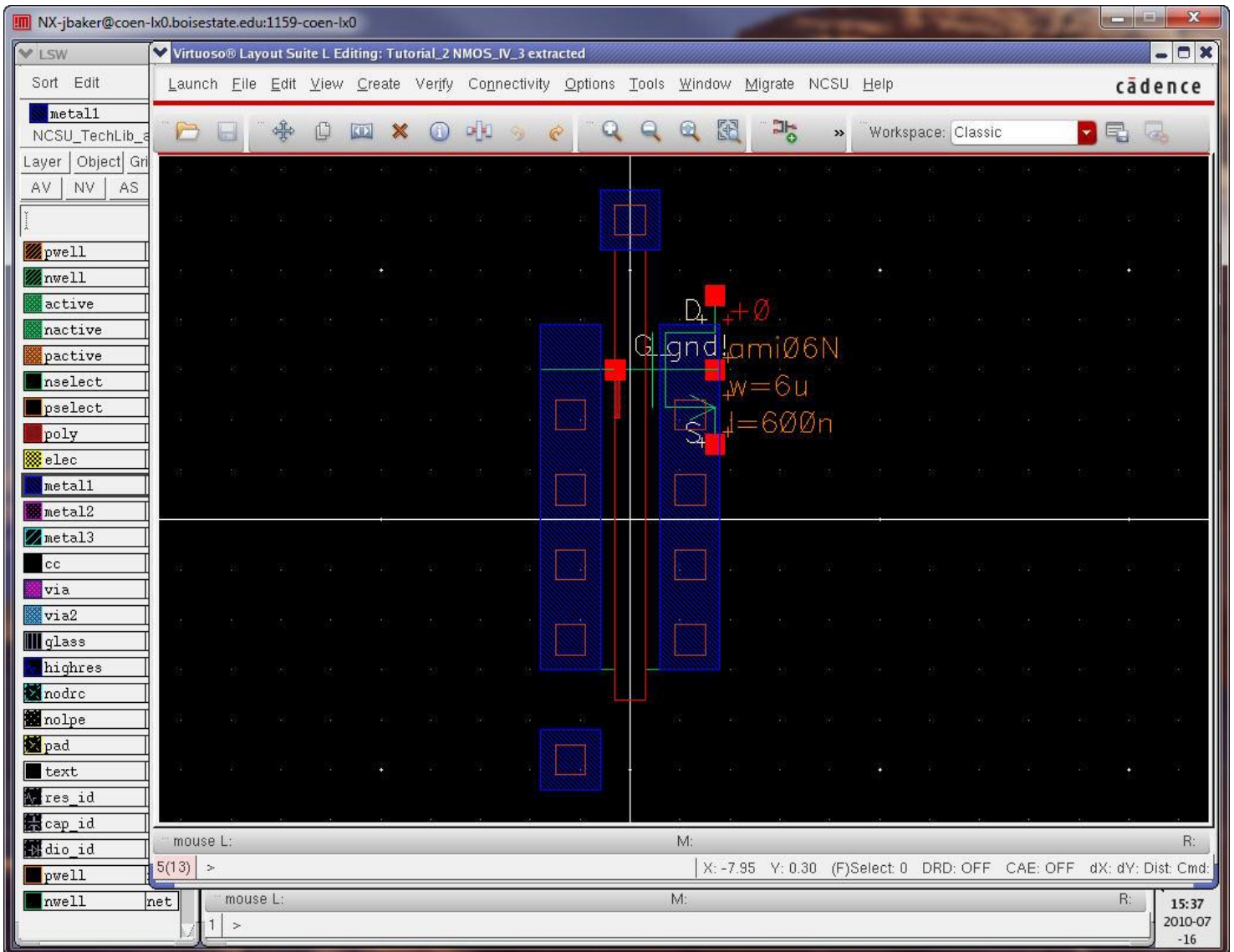
The bottom terminal window shows the output of the Extractor tool:

```

Virtuoso@6.1.1 - Log: /home/faculty/jbaker/CDS.log
File Tools Options Help
completed Fri Jul 16 15:35:41 2010
CPU TIME = 00:00:00 TOTAL TIME = 00:00:01
***** Summary of rule violations for cell "NMOS_IV_3 layout" *****
Total errors found: 0
t
fu

```

Once again run the Extractor and open the extracted view using the Library Manager.
Notice that it's basically the same view except that now the bulk of the NMOS devices is connected to gnd!



Again we get a failed LVS run and the error **"*Error* Could not determine the node name for terminal 'progn(bn)'.**" It looks like LVS

wants us to use

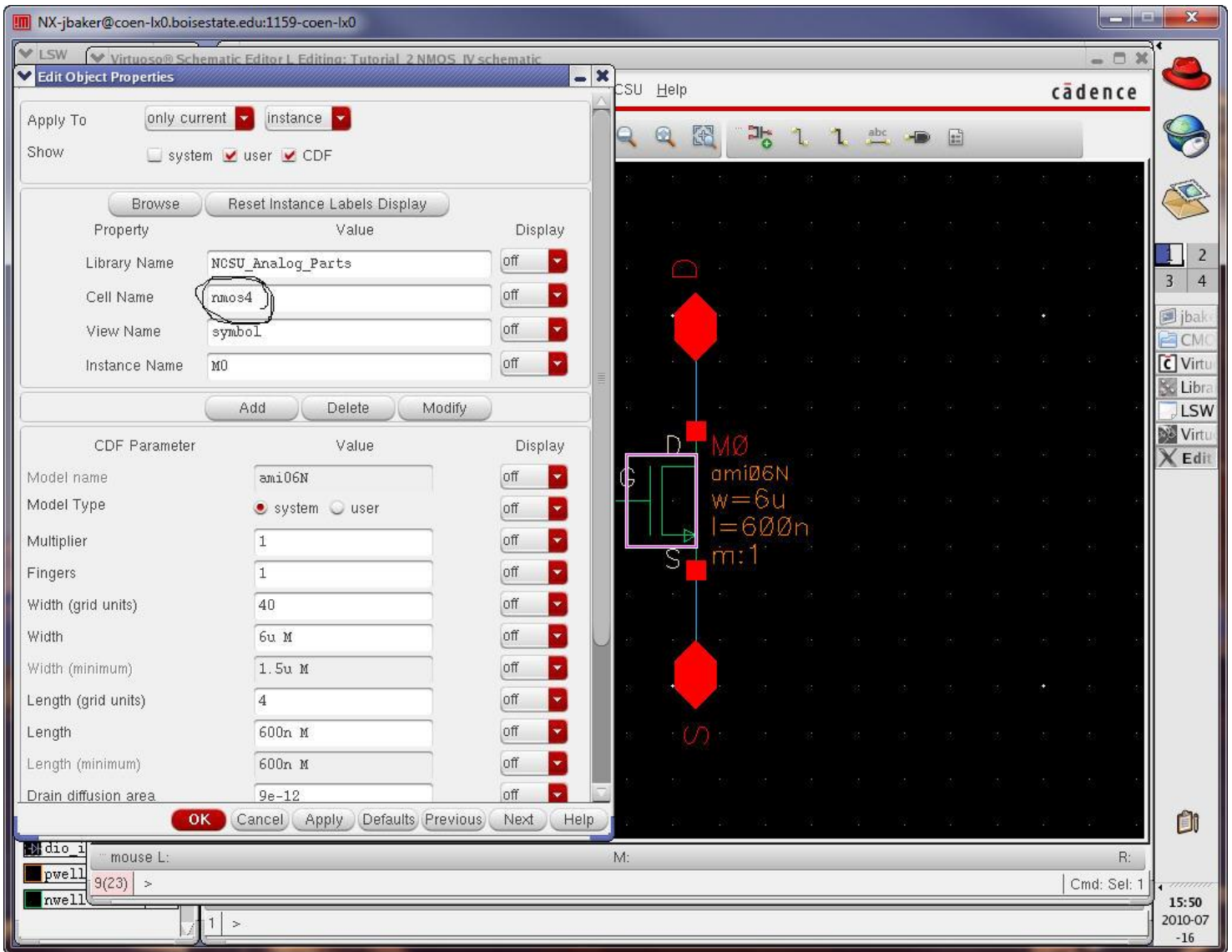
a 4-terminal transistor in our schematics! Let's try this.

Close all Cell views.

Open the Library Manager and rename NMOS_IV_3 to NMOS_IV.

Also, rename sim_NMOS_IV_3 to sim_NMOS_IV

Now open the schematic view of NMOS_IV and change the NMOS symbol as seen below.

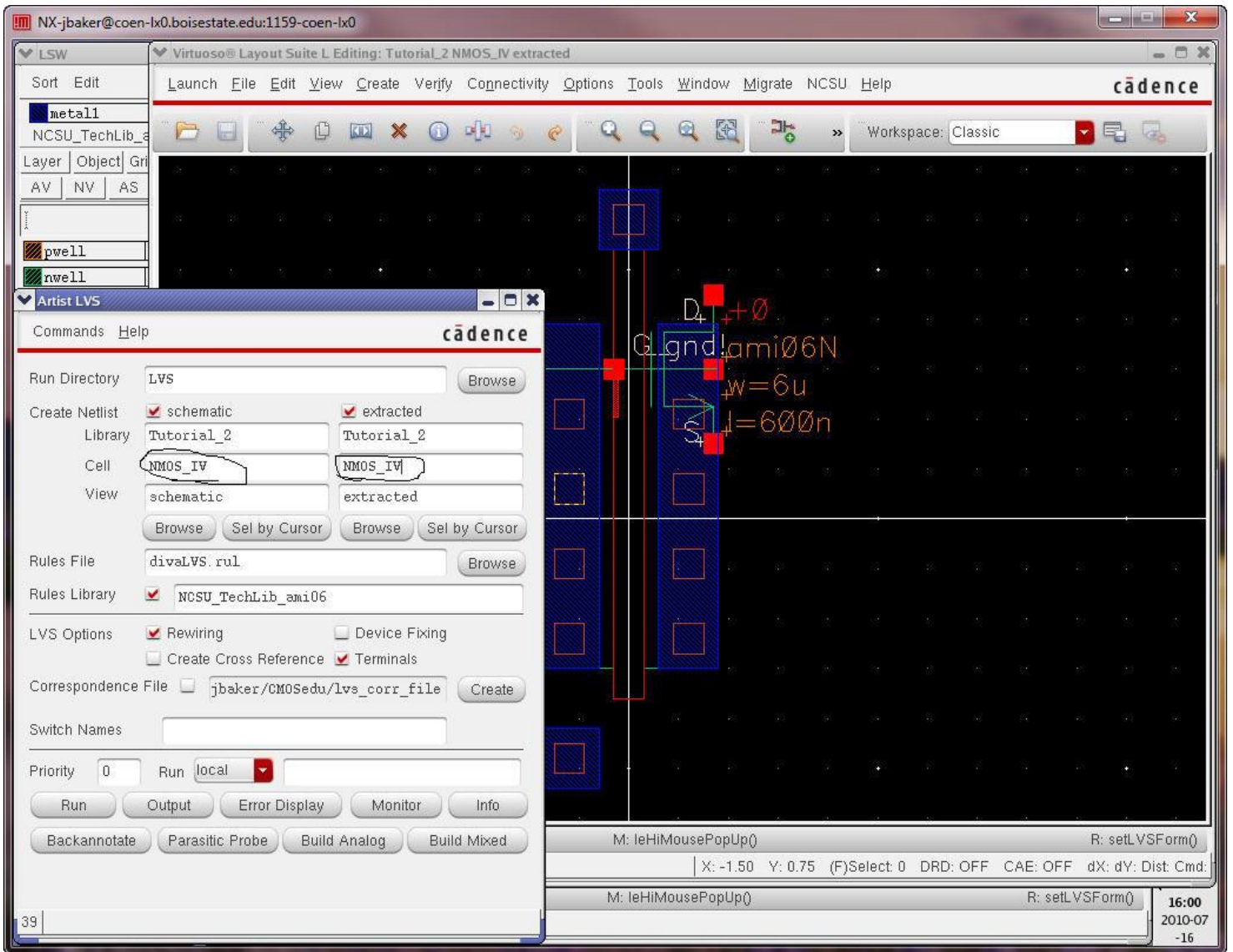


Move the symbol and then add the wire and label as seen below.

It may also be good to simulate this schematic (using the sim_NMOS_IV cell), following the steps seen above, to ensure that we still get the NMOS's IV curves.

The screenshot shows the Cadence Virtuoso Schematic Editor interface. The main window displays a schematic for an NMOS IV schematic. The schematic includes a red diamond-shaped component labeled 'M0' connected to a gate 'G' and a source 'S'. The gate is connected to a terminal 'G' and the source to a terminal 'S'. The drain is connected to a terminal 'D'. The schematic includes parameters: 'w=6u', 'l=600n', and 'm:1'. The background is dark with a grid. The left sidebar shows a layer list with various layers like 'pwell', 'nwell', 'active', etc. The bottom status bar shows '9(23) Use the options form to supply the wire names.' and 'Cmd: Wire Name Sel: 0'.

Open the extracted view and perform an LVS.
 Ensure that you select the correct cell, see circled text below.



And now!

The screenshot shows the Cadence LVS tool interface. The main window displays the output of the LVS command, which includes the following text:

```
@(#)SCDS: LVS.exe version 6.1.1 10/23/2007 02:12 (cds126047) $
Command line: /usr/local/Cadence/IC610/tools.lnx86/dfII/bin/32bit/LVS.exe -dir /home/faculty/jbaker/CMOSedu/LVS -l -s -t /ho
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

Net-list summary for /home/faculty/jbaker/CMOSedu/LVS/layout/netlist
count
4          nets
4          terminals
1          rmos

Net-list summary for /home/faculty/jbaker/CMOSedu/LVS/schematic/netlist
count
4          nets
4          terminals
1          rmos

Terminal correspondence points
N3      N3      D
N2      N1      G
N1      N4      S
N0      N0      gnd!

Devices in the rules but not in the netlist:
cap nfet pfet pmos rmos4 pmos4

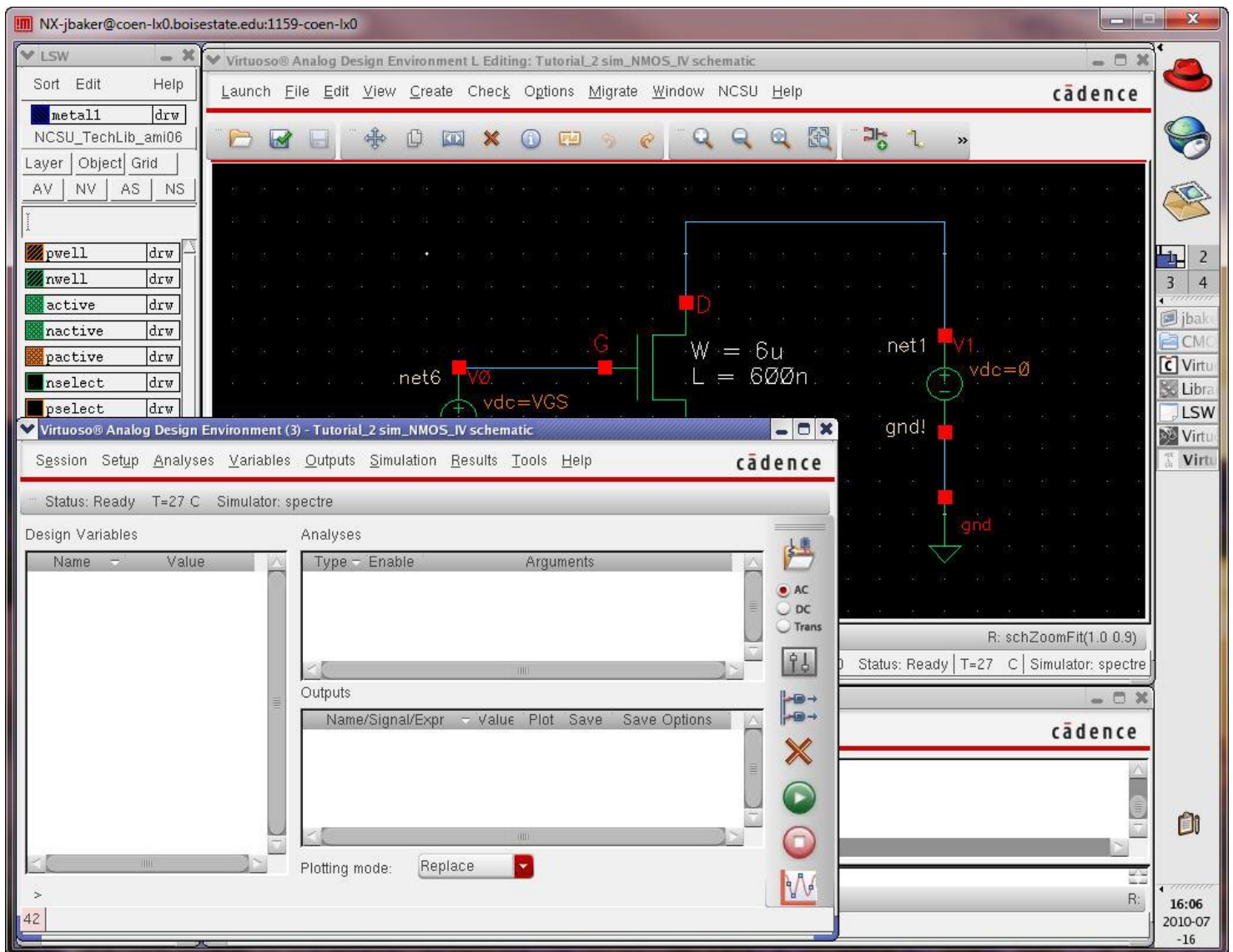
The net-lists match.

                                layout schematic
```

At the bottom of the window, there is a control panel with the following elements:

- Priority: 0
- Run: local
- Buttons: Run, Output, Error Display, Monitor, Info, Backannotate, Parasitic Probe, Build Analog, Build Mixed
- Status bar: M: leHiMousePopUp() R: setLVSForm() | X: -1.50 Y: 0.75 (F)Select 0 DRD: OFF CAE: OFF dX: dY: Dist: Cmd: | M: R: 16:02 2010-07 -16

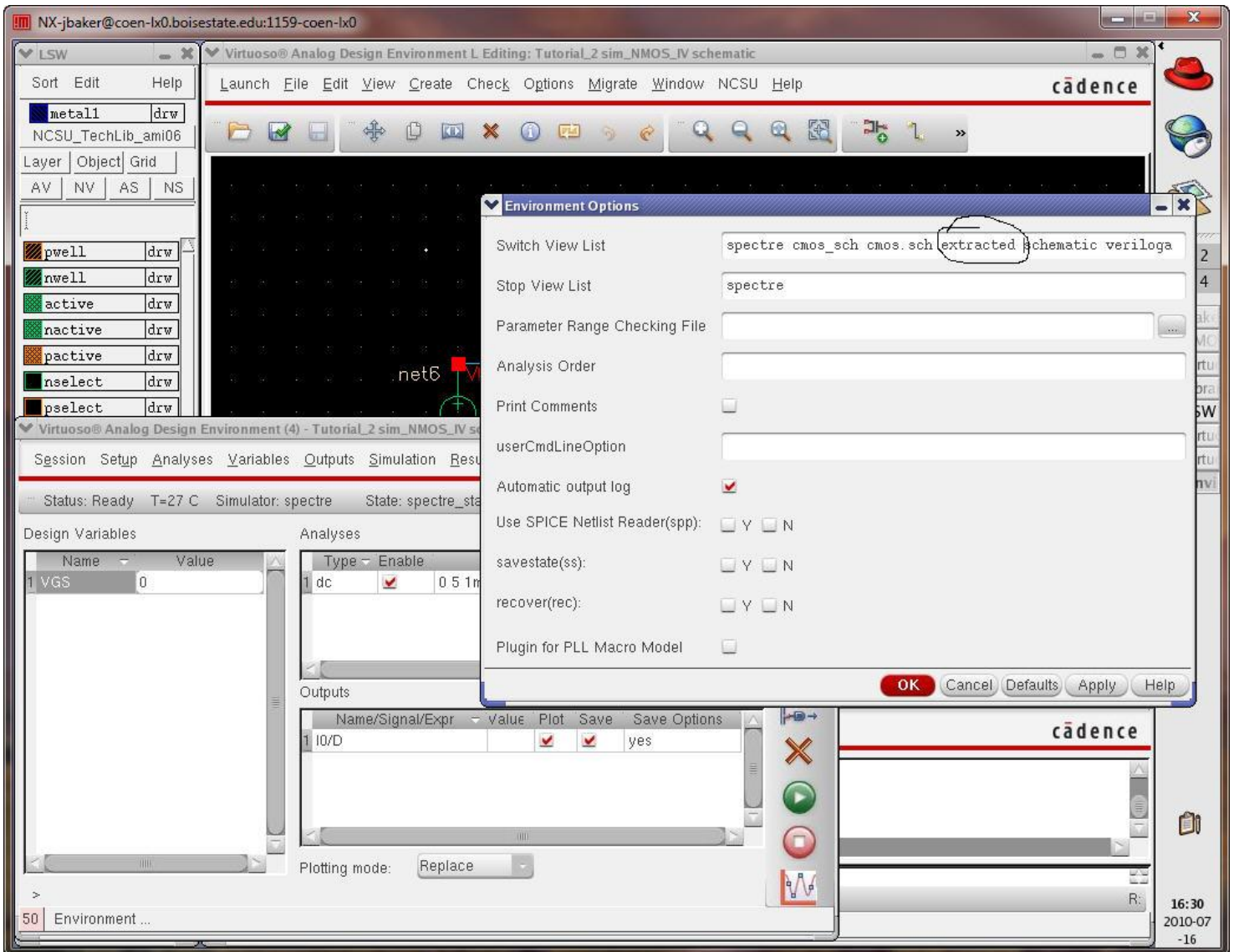
Okay, let's simulate the extracted layout.
Open the schematic view of sim_NMOS_IV and then Launch the ADE L.



Go to Session -> Load State then select Cellview and OK.

Then, on the ADE menu, select Setup -> Environment and enter extracted before schematic as seen below (so the extracted view is used before the schematic view when running the sim).

An important note: if you save the state with extracted view in front of schematic view you may get frustrated when you change your schematic and the simulation doesn't change!



Next, again as we did earlier, select Tools -> Parametric Analysis, enter the values seen below and then select the menu items Analysis -> Start to simulate.

The screenshot displays the Cadence Virtuoso Analog Design Environment interface. The main window shows a "DC Response" plot titled "Tutorial_2 sim_NMOS_IV schematic : Jul 16 16:14:24 2010 46". The plot shows current I (mA) versus DC voltage (V) for five different gate-source voltages (V_{GS}): 0.00e+00, 1.00e+00, 2.00e+00, 3.00e+00, 4.00e+00, and 5.00e+00. The current increases with V_{GS} and then levels off. The plot shows a current of 183 mV and 157.51 uA at the current point.

The "Parametric Analysis - spectre(2): Tutorial_2 sim_NMOS_IV schematic" window is open, showing the following settings:

- Sweep 1: Variable Name V_{GS}
- Range Type: From/To
- From: 0, To: 5
- Step Control: Linear Steps
- Step Size: 1

The bottom status bar shows the time 16:15, date 2010-07, and page number -16.

Just to ensure that we are simulating the extracted view and not the schematic view go to the ADE and select Simulation -> Netlist -> Display (see below).

The screenshot displays the Cadence Virtuoso Analog Design Environment. The main window shows a schematic netlist editor with the following content:

```
// Generated for: spectre
// Generated on: Jul 16 16:14:19 2010
// Design library name: Tutorial_2
// Design cell name: sim_NMOS_IV
// Design view name: schematic
simulator lang=spectre
global 0
parameters VGS=0
include "/home/faculty/jbaker/ncsu-cdk-1.6.0.beta/models/spectre/stand

// Library name: Tutorial_2
// Cell name: NMOS_IV
// View name: extracted
subckt NMOS_IV_extracted D G S
  \+0 (D G S 0) ami06N w=6e-06 l=6e-07 as=9e-12 ad=9e-12 ps=9e-06 \
  pd=9e-06 m=1 region=sat
ends NMOS_IV_extracted
// End of subcircuit definition.

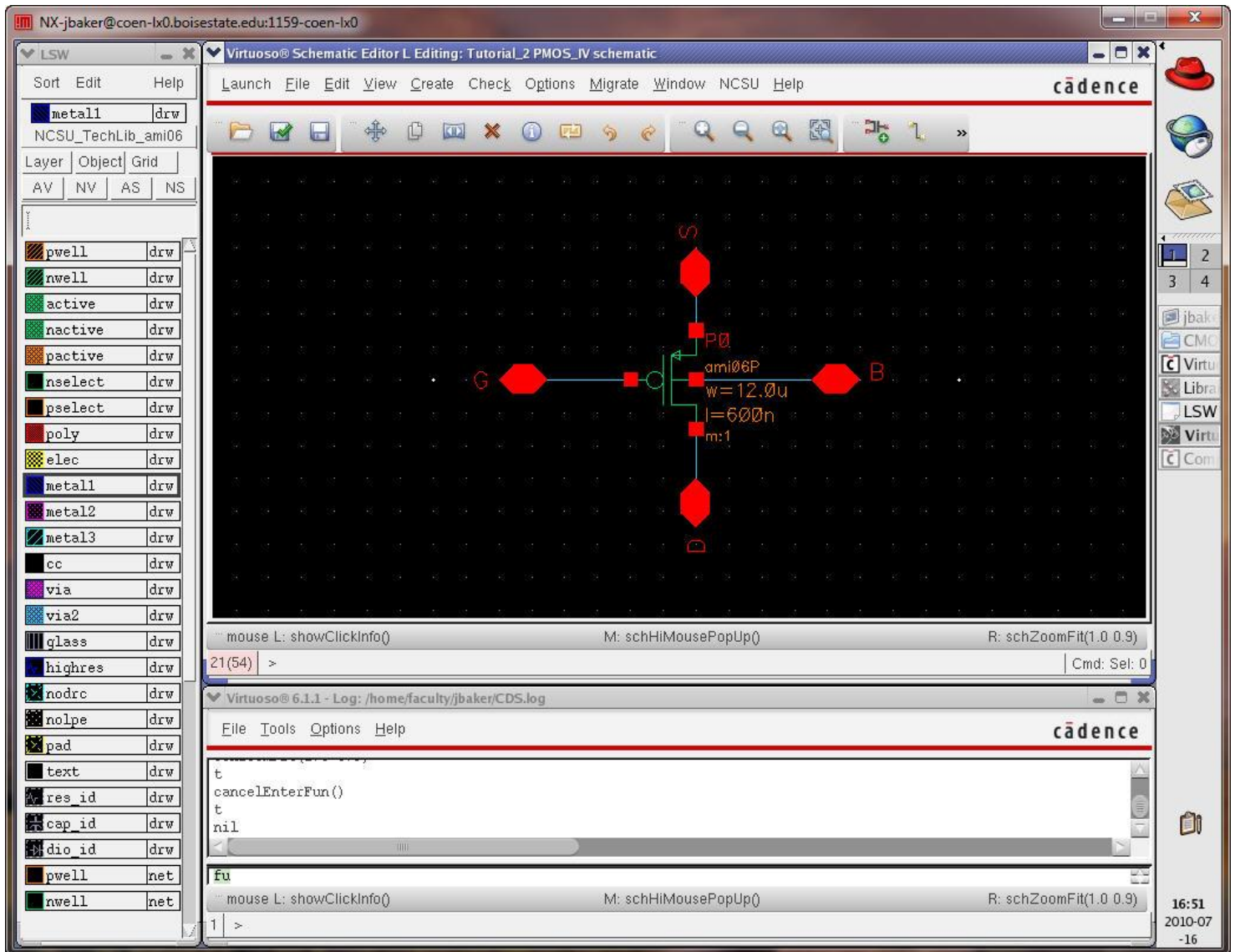
// Library name: Tutorial_2
// Cell name: sim_NMOS_IV
// View name: schematic
IO (net1 net6 0) NMOS_IV_extracted
V1 (net1 0) vsource type=dc dc=0
V0 (net6 0) vsource type=dc dc=VGS
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=
  tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwa
  digits=5 cols=80 pivrel=1e-3 sensfile="./psf/sens.output" \
  checklimitdest=psf
dc dev=V1 param=dc start=0 stop=5 step=1m write="spectre.dc" \
  oppoint=rawfile maxiters=150 maxsteps=10000 annotate=status
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
save IO:1
saveOptions options save=allpub
```

Overlaid on the netlist editor is a "DC Response" plot showing current (I0:1) versus voltage (V). The plot displays four curves for different gate-source voltages (VGS): 1.00e+00, 2.00e+00, 4.00e+00, and 5.00e+00. The current increases with VGS, and the curves are nearly horizontal at higher VGS values. A legend at the top of the plot identifies the curves: I0:1 (VGS=1.00e+00) in blue, I0:1 (VGS=2.00e+00) in green, I0:1 (VGS=4.00e+00) in orange, and I0:1 (VGS=5.00e+00) in purple.

Below the plot, a "Save Options" dialog box is open, showing "yes" for the "Save" option. To the right, a "Simulator" window shows the state "spectre_state1".

Let's repeat these steps for the PMOS device but in a much more concise manner (since now we are getting the hang of things and have made mistakes and fixed them).

Create a schematic Cell View called PMOS_IV with 4 pins as seen below. Note the W and L of the PMOS device.



Check and Save the schematic.

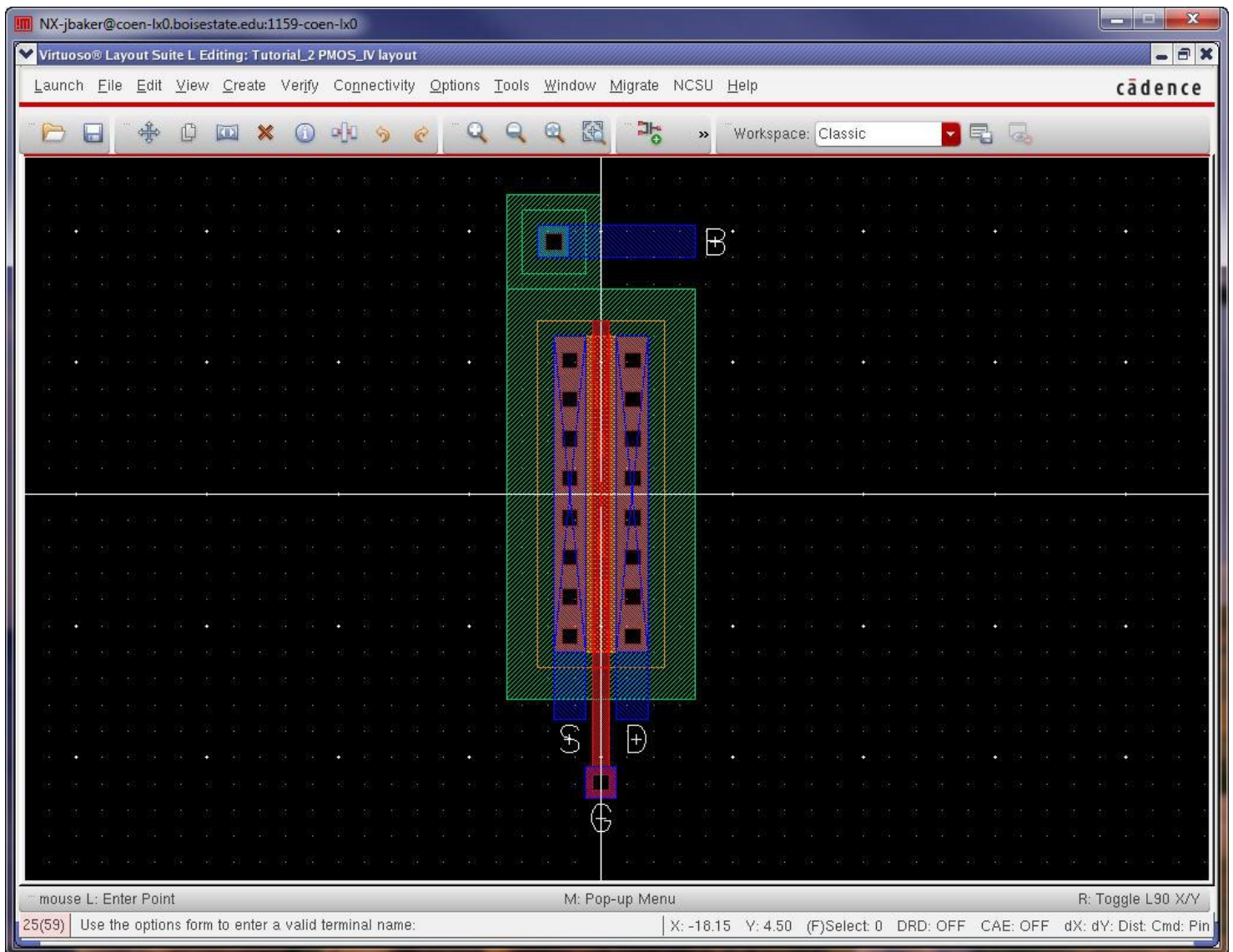
Next create a symbol for the schematic.

The screenshot displays the Cadence Virtuoso Symbol Editor interface. The main workspace shows a schematic diagram of a PMOS transistor symbol. The symbol consists of a central circle (gate) connected to a vertical line (source/drain), which is further connected to a horizontal line (body). The nodes are labeled G (gate), S (source), B (body), and D (drain). The channel width is specified as $W = 12 \text{ um}$ and the channel length as $L = 600 \text{ nm}$. The interface includes a layer list on the left, a command console at the bottom, and a log window showing the completion of a cross-view check and saving of the symbol.

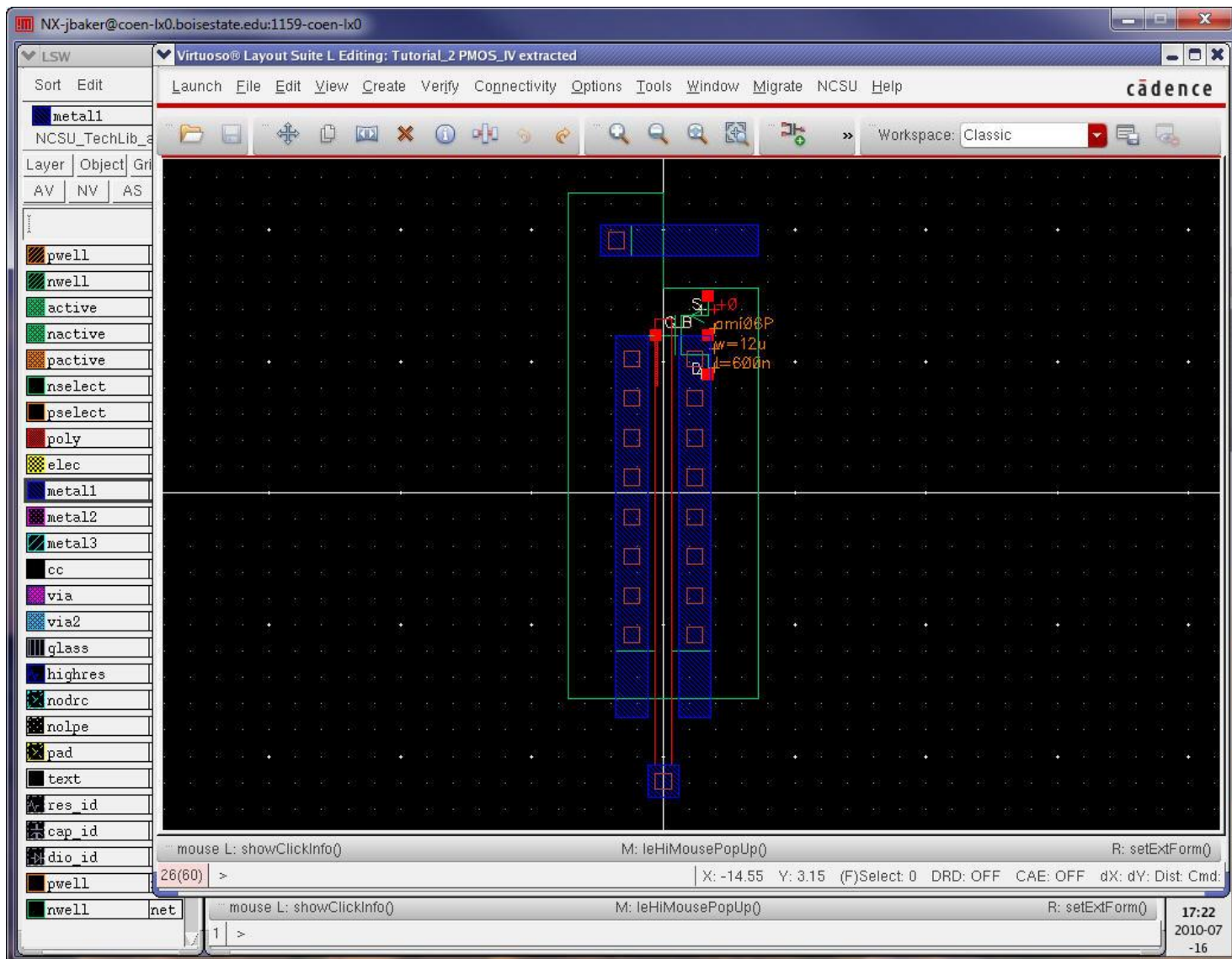
Check and Save the symbol.

Next create the layout (pmos cell and ntap).

DRC and Save the layout.



Next Extract the layout.
Open the extracted view in the Library Manager.



Save and close all open Views.

Next create a cell called sim_PMOS_IV and draft the following schematic.

Note the value of /V1 is VSG (not VGS as we used in the NMOS sim).

When finished Check and Save.

The screenshot displays the Cadence Virtuoso Schematic Editor interface. The main window shows a schematic of a PMOS transistor with the following parameters: $W = 12 \mu\text{m}$ and $L = 600 \text{ nm}$. The schematic includes a gate terminal (G), a source terminal (S), and a drain terminal (D). The gate is connected to a voltage source V_1 with $vdc = VSG$. The source is connected to a voltage source V_0 with $vdc = 0$. The drain is connected to a voltage source V_2 with $vdc = 5$. The source and drain are connected to a common ground (gnd.).

The left sidebar shows a list of layers and objects, including `metal1`, `metal2`, `metal3`, `cc`, `via`, `via2`, `glass`, `highres`, `nodrc`, `nolpe`, `pad`, `text`, `res_id`, `cap_id`, `dio_id`, `pwell`, and `nwell`.

The bottom window shows the Virtuoso log output:

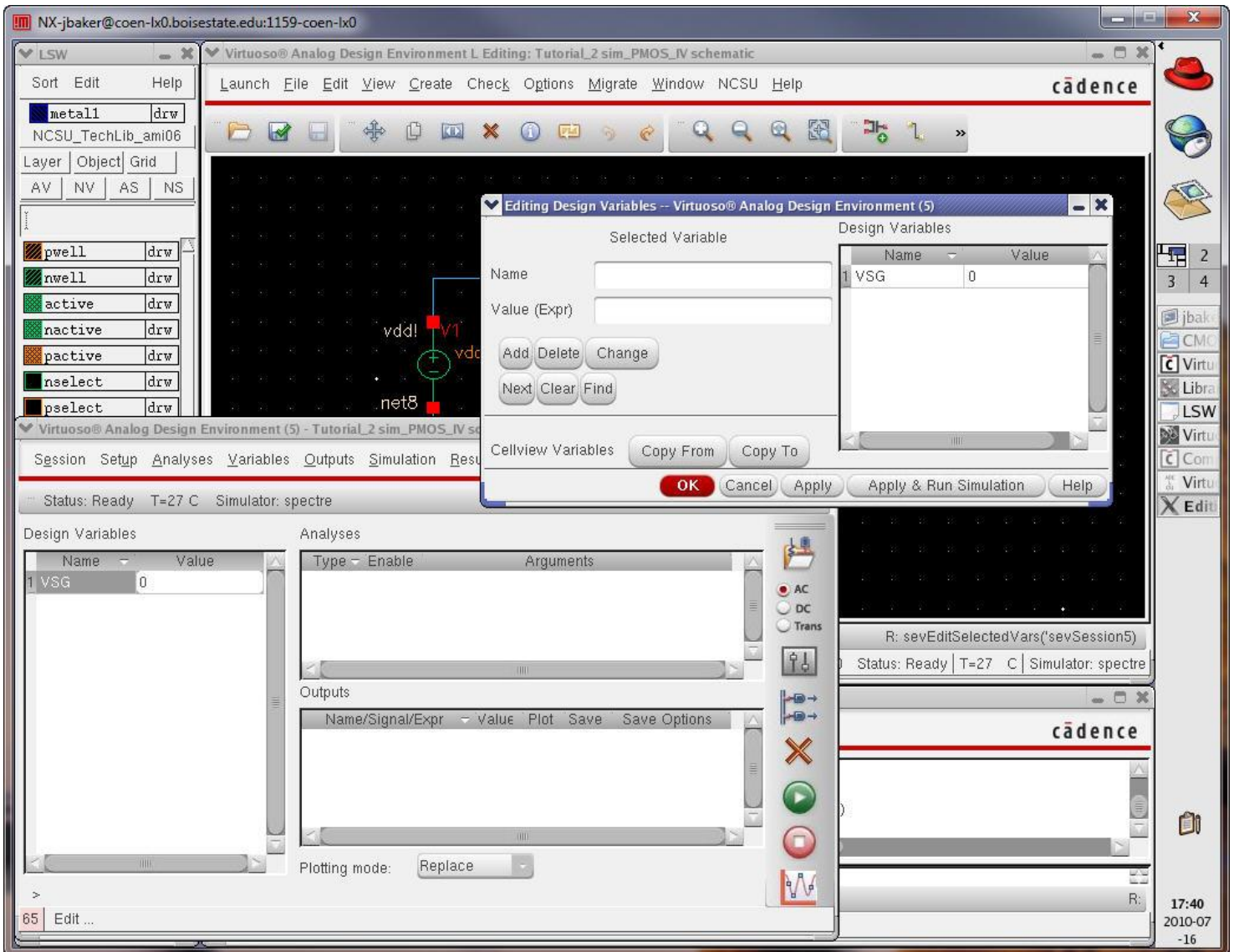
```

Virtuoso@6.1.1 - Log: /home/faculty/jbaker/CDS.log
File Tools Options Help
schHiCheckAndSave()
Extracting "sim_PMOS_IV schematic"
Schematic check completed with no errors.
"Tutorial_2 sim_PMOS_IV schematic" saved.
t
fu

```

We are now ready to simulate this design.

Launch the ADE then go to Setup -> Model Libraries and select the PMOS models for AMI06 (setting the models is important!).
Variables -> Edit and Add VSG with a value of 0 (not VGS)



Next select Outputs and the source terminal of the transistor.
Ensure, as seen below, that both Plot and Save are selected.

The screenshot displays the Cadence Virtuoso Analog Design Environment. The main window shows a schematic of a PMOS transistor with the following parameters: $W = 12 \mu\text{m}$ and $L = 600 \text{ nm}$. The transistor is connected to a $vdd!$ source (V1) through a resistor (R). The gate is connected to a $vdd!$ source (V0). The drain is connected to a $vdd!$ source (V2) and the source is connected to a $vdd!$ source (V1). The schematic is titled "Tutorial_2 sim_PMOS_IV schematic".

The command window shows the following simulation results:

```

5 parametric simulation
Setting VSG = 1
compose simulator input
... successful.
start simulator if ne
... successful.
simulate...
simulation completed
4 parametric simulation
Setting VSG = 2
compose simulator input
... successful.
start simulator if ne
... successful.
simulate...

```

The outputs window shows the following table:

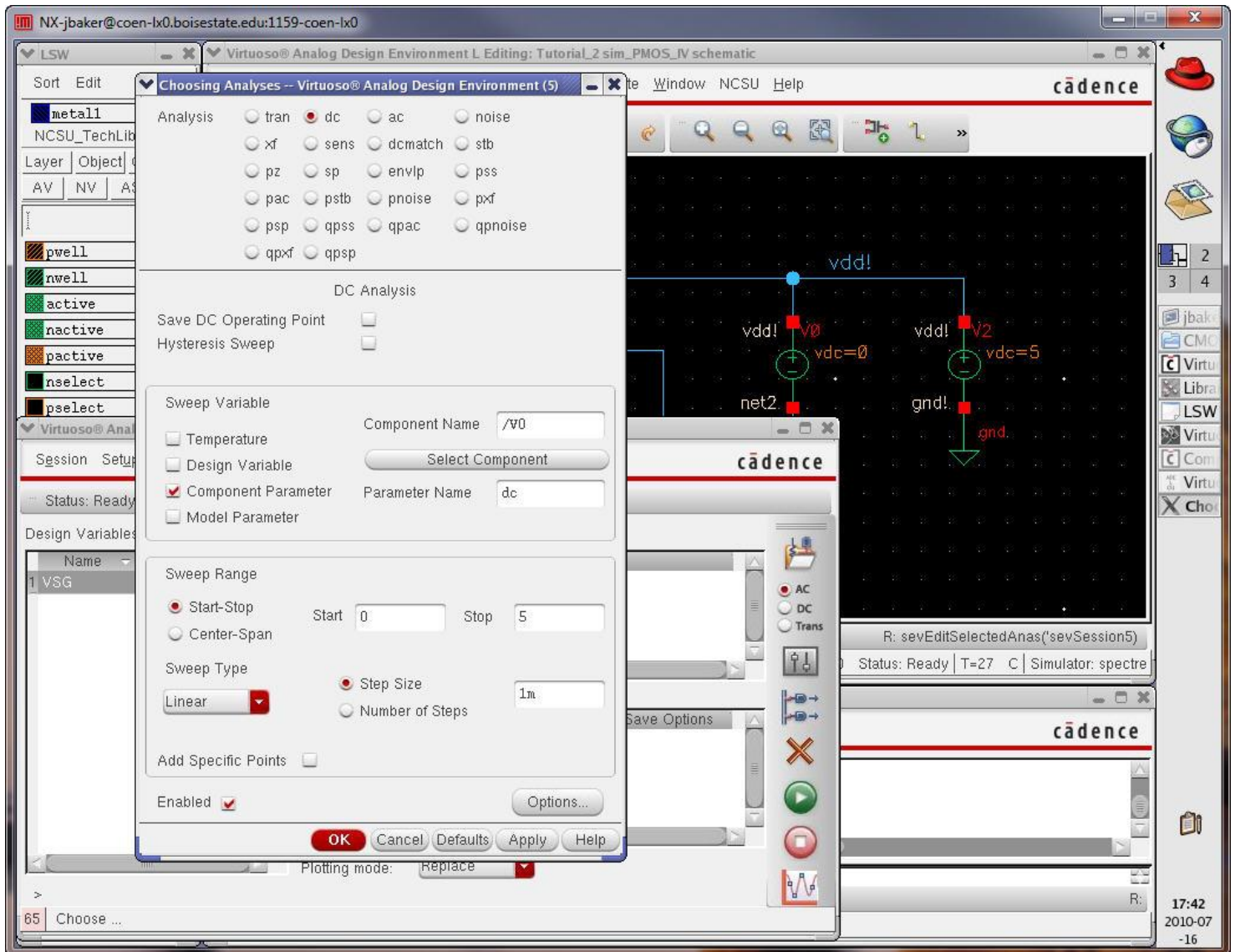
Name/Signal/Expr	Value	Plot	Save	Save Options
1 I0/S		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	yes

The status bar shows the time 17:50 on 2010-07-16.

Select Analyses and enter the following.

Note that /V0 is VSD.

Also note that the vdd! Source, that is /V2, really doesn't do anything. It could be zero but we include it since it's common to connect the S/B to vdd!



Save the state in the cellview.

Then go to Parametric Analysis and enter the values seen below (again, it's VSG not VGS).

The screenshot displays the Cadence Virtuoso Analog Design Environment. The main window shows a schematic diagram with three voltage sources labeled V1, V0, and V2. V1 is connected to net8 and has a DC value of VSG. V0 is connected to net2 and has a DC value of 0. V2 is connected to gnd and has a DC value of 5. The schematic is titled "Tutorial_2 sim_PMOS_IV schematic".

In the foreground, a "Parametric Analysis - spectre(4): Tutorial_2 sim_PMOS_IV schematic" dialog box is open. The "Analysis" tab is selected, and the "Start" button is highlighted. The dialog shows the following settings:

- Tool: spectre
- Range Type: From
- Step Control: Linear Steps
- Step Size: 1
- From: 0
- To: 5

The dialog also includes a table for Design Variables and a section for Sweep 1. The "Start" button is highlighted, indicating the beginning of the simulation process.

Starting the analysis results in the following. Note that this is the simulation of the schematic.

The screenshot displays the Cadence Virtuoso interface. The top window shows a terminal window with the following simulation logs:

```

5 parametric simulations remaining.
Setting VSG = 1
compose simulator input file...
... successful.
start simulator if needed...
... successful.
simulate...
simulation completed successfully.
4 parametric simulations remaining.
Setting VSG = 2
compose simulator input file...
... successful.
start simulator if needed...
... successful.
simulate...
simulation completed successfully.
3 parametric simulations remaining.
Setting VSG = 3
compose simulator input file...
... successful.
start simulator if needed...
... successful.
simulate...
simulation completed successfully.
2 parametric simulations remaining.
Setting VSG = 4
compose simulator input file...
... successful.
start simulator if needed...
... successful.
simulate...
simulation completed successfully.
1 parametric simulation remaining.
Setting VSG = 5
compose simulator input file...
... successful.
start simulator if needed...
... successful.
simulate...
simulation completed successfully.
reading simulation data...
... successful.

```

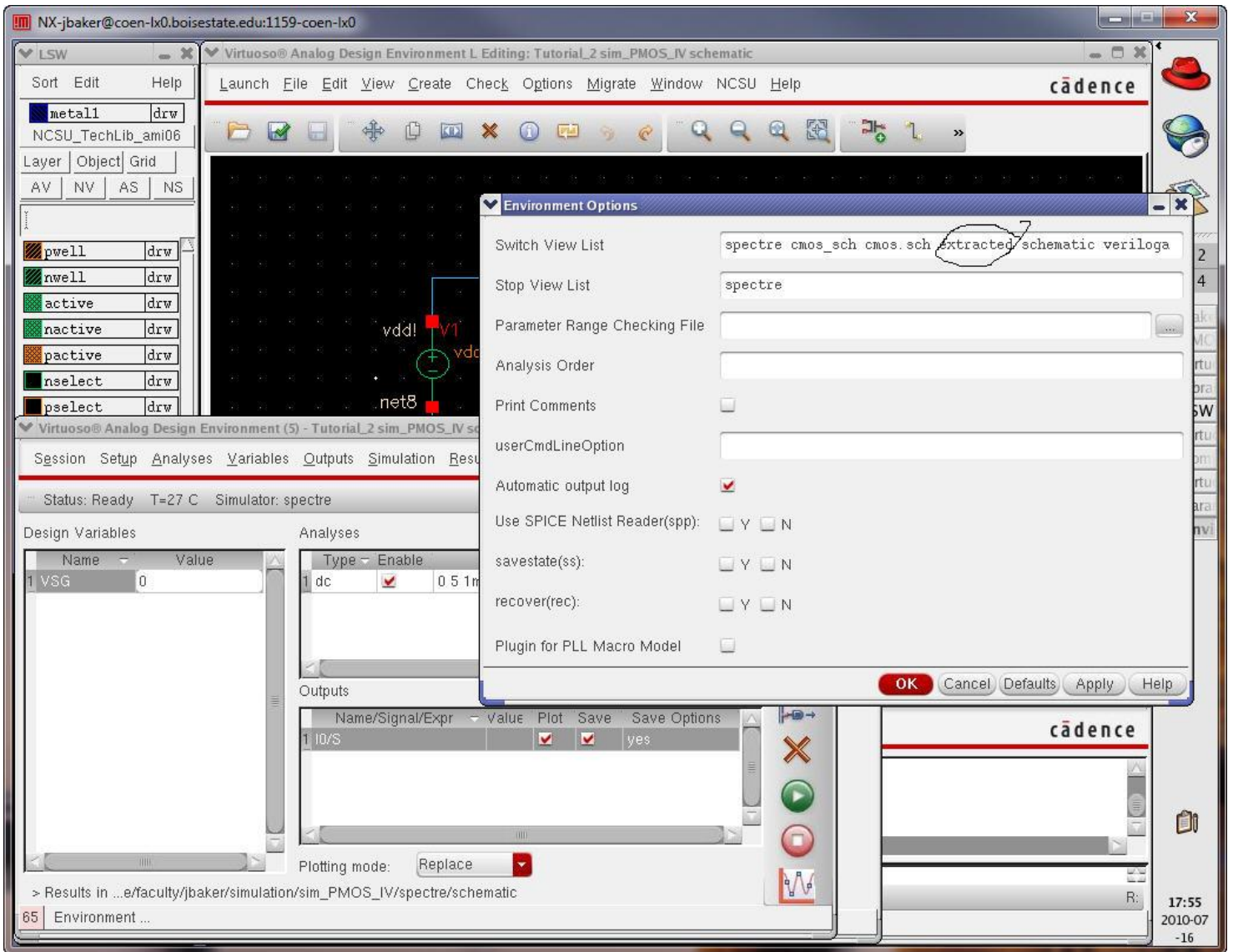
The bottom window shows a DC Response graph with the following legend and data series:

- VSG="0";/I0/S
- VSG="1";/I0/S
- VSG="2";/I0/S
- VSG="3";/I0/S
- VSG="4";/I0/S
- VSG="5";/I0/S

The graph plots YO (mA) on the y-axis (ranging from 0 to 3.5) against dc (V) on the x-axis (ranging from 0.0 to 5). The curves show that as the gate voltage (VSG) increases, the drain current (YO) also increases, with higher VSG values resulting in higher current levels across the entire range of drain voltages.

Now let's simulate the extracted layout.

In the ADE go to Setup -> Environment and add extracted before schematic.



And we get the same thing as with the schematic.

The screenshot displays the Cadence Virtuoso interface. The top window shows a terminal window with the following simulation logs:

```

5 parametric simulations remaining.
Setting VSG = 1
compose simulator input file...
... successful.
start simulator if needed...
... successful.
simulate...
simulation completed successfully.
4 parametric simulations remaining.
Setting VSG = 2
compose simulator input file...
... successful.
start simulator if needed...
... successful.
simulate...
simulation completed successfully.
3 parametric simulations remaining.
Setting VSG = 3
compose simulator input file...
... successful.
start simulator if needed...
... successful.
simulate...
simulation completed successfully.
2 parametric simulations remaining.
Setting VSG = 4
compose simulator input file...
... successful.
start simulator if needed...
... successful.
simulate...
simulation completed successfully.
1 parametric simulation remaining.
Setting VSG = 5
compose simulator input file...
... successful.
start simulator if needed...
... successful.
simulate...
simulation completed successfully.
reading simulation data...
... successful.

```

The bottom window shows a DC Response plot titled "DC Response". The plot displays current I (mA) versus DC voltage (V) for six different VSG values. The legend indicates the following series:

- IO:4 (VSG=0.00e+00)
- IO:4 (VSG=1.00e+00)
- IO:4 (VSG=2.00e+00)
- IO:4 (VSG=3.00e+00)
- IO:4 (VSG=4.00e+00)
- IO:4 (VSG=5.00e+00)

The plot shows that the current I increases with DC voltage and also increases with the VSG value. The current ranges from approximately 0.5 mA to 3.2 mA across the plotted range of 0.0 V to 5.0 V.

Just to verify that we are simulating the extracted view go to ADE Simulation -> Netlist -> Display.

The screenshot displays the Cadence Virtuoso Analog Design Environment. The main window shows a netlist editor with the following content:

```
// Generated for: spectre
// Generated on: Jul 16 17:56:33 2010
// Design library name: Tutorial_2
// Design cell name: sim_PMOS_IV
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
parameters VSG=0
include "/home/faculty/jbaker/ncsu-cdk-1.6.0.beta/models/spectre/stand

// Library name: Tutorial_2
// Cell name: PMOS_IV
// View name: extracted
subckt PMOS_IV_extracted B D G S
 \+0 (D G S B) ami06P w=1.2e-05 l=6e-07 as=1.8e-11 ad=1.8e-11 \
 ps=1.5e-05 pd=1.5e-05 m=1 region=sat
ends PMOS_IV_extracted
// End of subcircuit definition.

// Library name: Tutorial_2
// Cell name: sim_PMOS_IV
// View name: schematic
IO (vdd! net2 net8 vdd!) PMOS_IV_extracted
V2 (vdd! 0) vsource type=dc dc=5
V1 (vdd! net8) vsource type=dc dc=VSG
V0 (vdd! net2) vsource type=dc dc=0
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=
 tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwa
 digits=5 cols=80 pivrel=1e-3 sensfile="/psf/sens.output" \
 checklimitdest=psf
dc dc dev=V0 param=dc start=0 stop=5 step=1m write="spectre.dc" \
 oppoint=rawfile maxiters=150 maxsteps=10000 annotate=status
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
save IO:4
saveOptions options save=allpub
```

The simulation window shows a DC Response plot with the following data points:

Time (ns)	V0 (V)	V1 (V)	V2 (V)
0	0.00e+00	0.00e+00	5.00e+00
4	0.00e+00	0.00e+00	5.00e+00
5	0.00e+00	0.00e+00	5.00e+00

An important note: if you save the state with extracted view in front of schematic view you may get frustrated when you change your schematic and the simulation doesn't change! The simulator simulates your old extracted view instead of your modified schematic view.

Save the state and close everything. This concludes Tutorial 2.

For your reference the Tutorial_2 directory is available in [Tutorial_2.zip](#).

[Return](#)

