

# Method of Sealing 1.5mm × 1.5mm Standard CMOS Chip Bonding Wires

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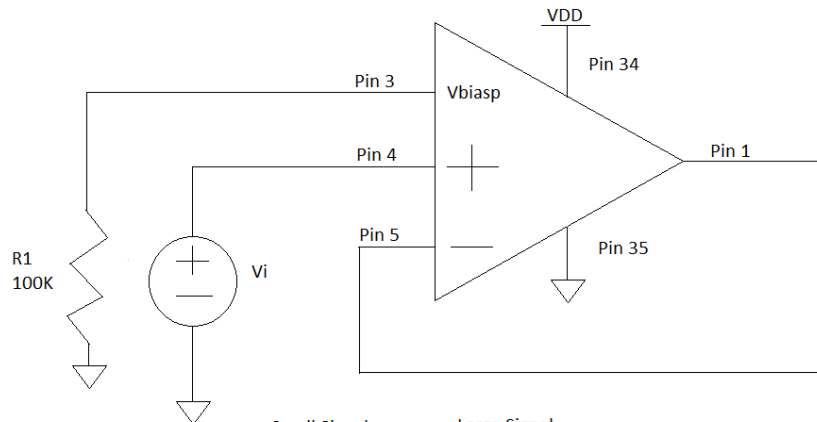
## Resin used:

RTV112-White (2.8 fl oz)

## Chip tested:

(MOSIS V35G-AC) Homemade Transimpedance Amplifier

## Test Circuit:



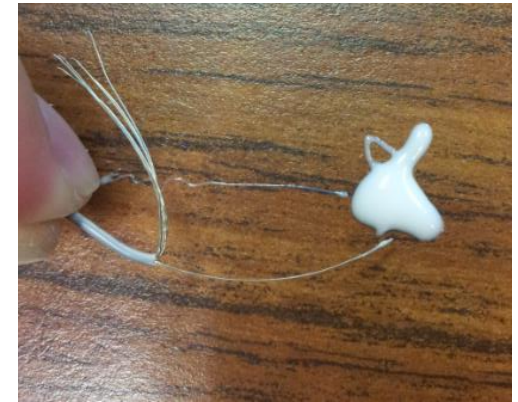
Small Signal	Large Signal
$f = 100\text{kHz}$	$f = 100\text{kHz}$
$V_{off} = 2.55\text{V}$	$V_{off} = 3.5\text{V}$
$V = 100\text{mV (pk-pk)}$	$V = 2\text{V (pk-pk)}$

1	$V_{out\_A}$	$V_{DD\_A}$	40
2	$gnd\_A$	$V_{bias1\_F}$	39
3	$V_{biasp\_A}$	$V_{bias2\_F}$	38
4	$Vp\_A$	$V_{bias3\_F}$	37
5	$Vm\_A$	$V_{bias4\_F}$	36
6	Pin6	$gnd$	35
7	$V_{out\_B}$	$V_{DD}$	34
8	$V_{biasp\_B}$	$V_{biasp\_F}$	33
9	$V_{DD\_B}$	Pin32	32
10	$gnd\_B$	Pin31	31
11	$Vp\_B$	$V_{out\_E}$	30
12	$Vm\_B$	$gnd\_E$	29
13	$V_{out\_C}$	$V_{DD\_E}$	28
14	$V_{biasp\_C}$	$Vm\_E$	27
15	$V_{DD\_C}$	$Vp\_E$	26
16	$Vp\_C$	$V_{biasp\_E}$	25
17	$gnd\_C$	$V_{out\_D}$	24
18	$Vm\_C$	$V_{biasp\_D}$	23
19	$Vp\_D$	$Vm\_D$	22
20	$gnd\_D$	$V_{DD\_D}$	21

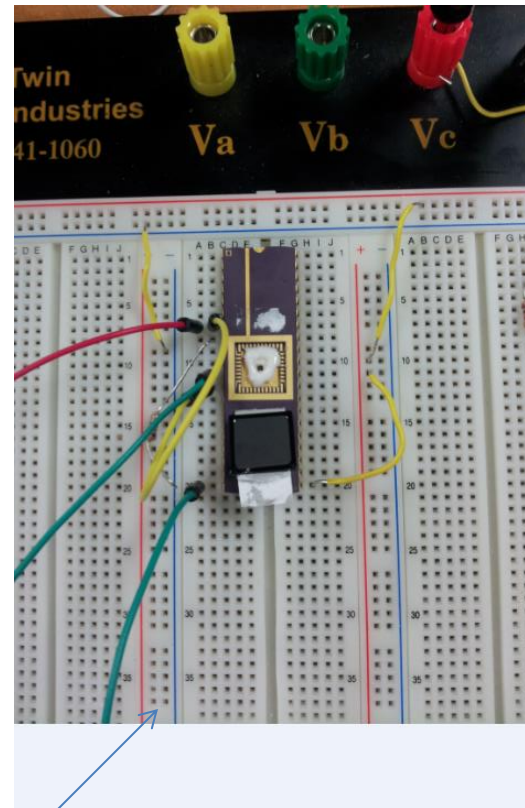
# Tools used for sealing

## 1. Stranded wire:

Using one branch of the stranded wires to daub the resin to the bottom of the bonding wires.

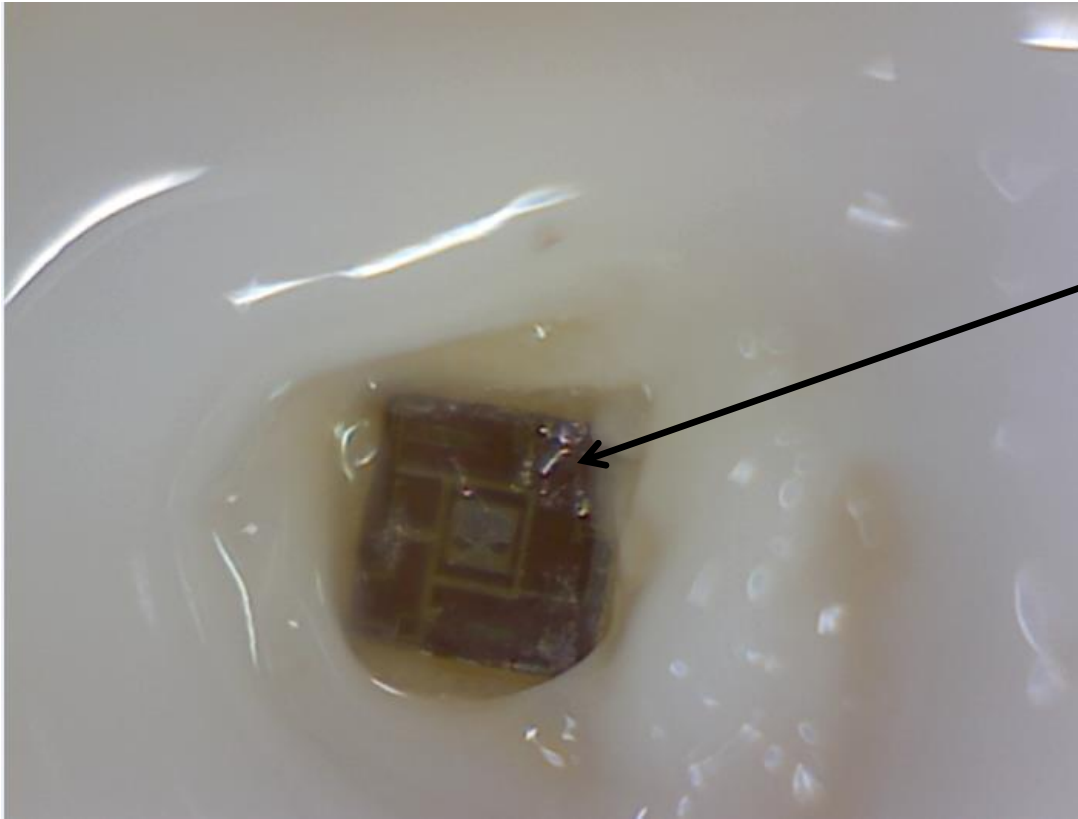


## 2. Celestron 10X-150X Microscope, PC and Breadboard



Bread Board is used to fix and test the chip

## Sealing Result

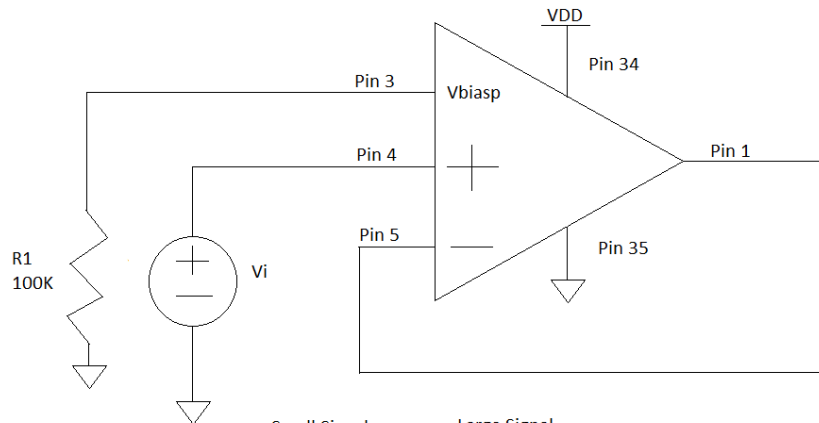


Don't worry about the remaining resin at the right up side of the chip, it can be totally avoided.

The opening is for microfluidic experiments. Water (transparent) is already filled the opening in this figure.

# Chip Testing Results

Amplifiers A-E are tested with the following circuit. Since this experiment is just testing the effect of sealing, the amplifier performance are not tested in detail.

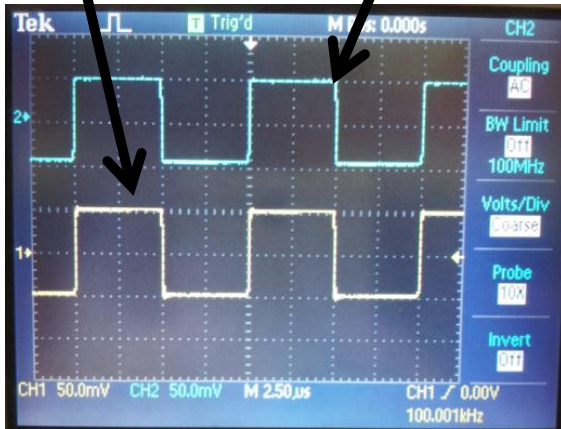


Small Signal	Large Signal
f = 100kHz	f = 100kHz
V <sub>off</sub> = 2.55V	V <sub>off</sub> = 3.5V
V = 100mV (pk-pk)	V = 2V (pk-pk)

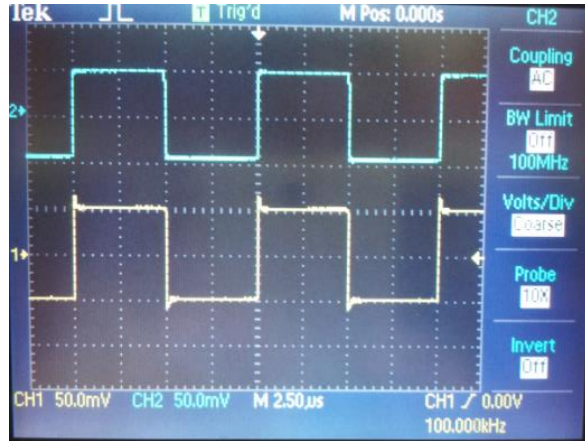
1	Vout_A	VDD_A	40
2	gnd_A	Vbias1_F	39
3	Vbiasp_A	Vbias2_F	38
4	Vp_A	Vbias3_F	37
5	Vm_A	Vbias4_F	36
6	Pin6	gnd	35
7	Vout_B	VDD	34
8	Vbiasp_B	Vbiasp_F	33
9	VDD_B	Pin32	32
10	gnd_B	Pin31	31
11	Vp_B	Vout_E	30
12	Vm_B	gnd_E	29
13	Vout_C	VDD_E	28
14	Vbiasp_C	Vm_E	27
15	VDD_C	Vp_E	26
16	Vp_C	Vbiasp_E	25
17	gnd_C	Vout_D	24
18	Vm_C	Vbiasp_D	23
19	Vp_D	Vm_D	22
20	gnd_D	VDD_D	21

# Chip Testing Results

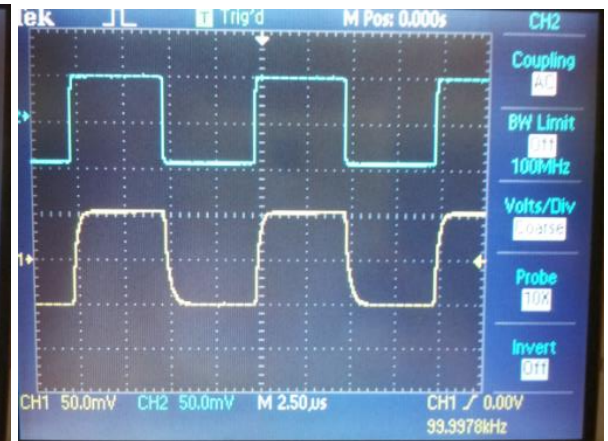
Output      Input



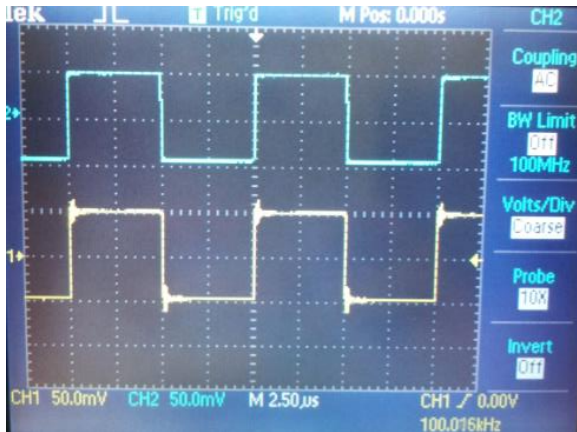
Amplifier A



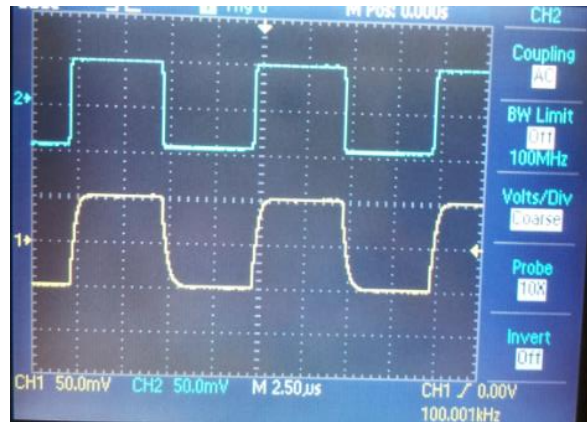
Amplifier B



Amplifier C



Amplifier D



Amplifier E

Notice:  
Channel 2 is input  
signal, Channel 1 is  
output signal