

The issue of High impedance (XXX) result of JK flip flop when simulating with QuartusII

1. When you are doing sequential circuits, the time delay cannot be neglected especially when some inputs are dependent on any output.
2. The delay of the gates in our DE2 boards are also not negligible. Your default clock cycle is too fast for our DE2 board in sequential circuits. You have to try to slow it down to wait for the result to be settled.

Change your clk period to mili seconds level, and also change the period of the J and K to the similar level as the clock so you can see them in the same screen. (You can scroll you mouse to see more compacted waveforms.)

The screenshot shows the Quartus II simulation environment. The main window displays a timing diagram with a clock signal (clk) and two data signals (J and K). The clock signal has a period of 30.0 ns. The J and K signals have a period of 482.76 ms. A context menu is open over the clock signal, with the 'Clock...' option selected. The menu options are:

- Cut (Ctrl+X)
- Copy (Ctrl+C)
- Paste
- Delete (Del)
- Select Entire Waveform Interval
- Insert
- Value
- Grouping
- Display Format
- Nodes
- Group and Bus Bit Order
- Locate
- Zoom
- Properties
- Stretch or Compress Waveform Interval... (Ctrl+Alt+S)
- Offset Waveform Interval... (Ctrl+Alt+O)
- Uninitialized (U) (Ctrl+Alt+U)
- Forcing Unknown (X) (Ctrl+Alt+X)
- Forcing Low (0) (Ctrl+Alt+0)
- Forcing High (1) (Ctrl+Alt+1)
- High Impedance (Z) (Ctrl+Alt+Z)
- Weak Unknown (W) (Ctrl+Alt+W)
- Weak Low (L) (Ctrl+Alt+L)
- Weak High (H) (Ctrl+Alt+H)
- Don't Care (DC) (Ctrl+Alt+D)
- Invert (Ctrl+Alt+I)
- Count Value... (Ctrl+Alt+V)
- Clock... (Ctrl+Alt+K)**
- Arbitrary Value... (Ctrl+Alt+B)
- Random Values... (Ctrl+Alt+R)

The Messages window at the bottom shows the following information:

```
Info: Command: quartus_sim --read_settings_files=on --write_settings_files=off jk -c jk
Info: Using vector source file "C:/quartusproject/jk/jk.vwf"
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is 100.00 %
Info: Number of transitions in simulation is 697
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
```

Don't forget to change the simulation mode to 'Timing'

The screenshot displays the Quartus II IDE interface. The main window shows a timing simulation waveform for a design named 'jk'. The waveform includes signals for 'clk', 'i', 'k', and 'out'. A 'Settings - jk' dialog box is open, showing the 'Simulator Settings' tab. The 'Simulation mode' is set to 'Timing'. The 'Simulation period' is set to 'Run simulation until all vector stimuli are used'. The 'Glitch filtering options' are set to 'Auto'. The 'Messages' window at the bottom shows the following log:

```
Info: Command: quartus_sim --read_settings_files=on --write_settings_files=off jk -c jk
Info: Using vector source file "C:/quartusproject/jk/jk.vwf"
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
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```

The status bar at the bottom indicates the current mode is 'Idle'.

Result

The JK flip flop is rising edge triggered

