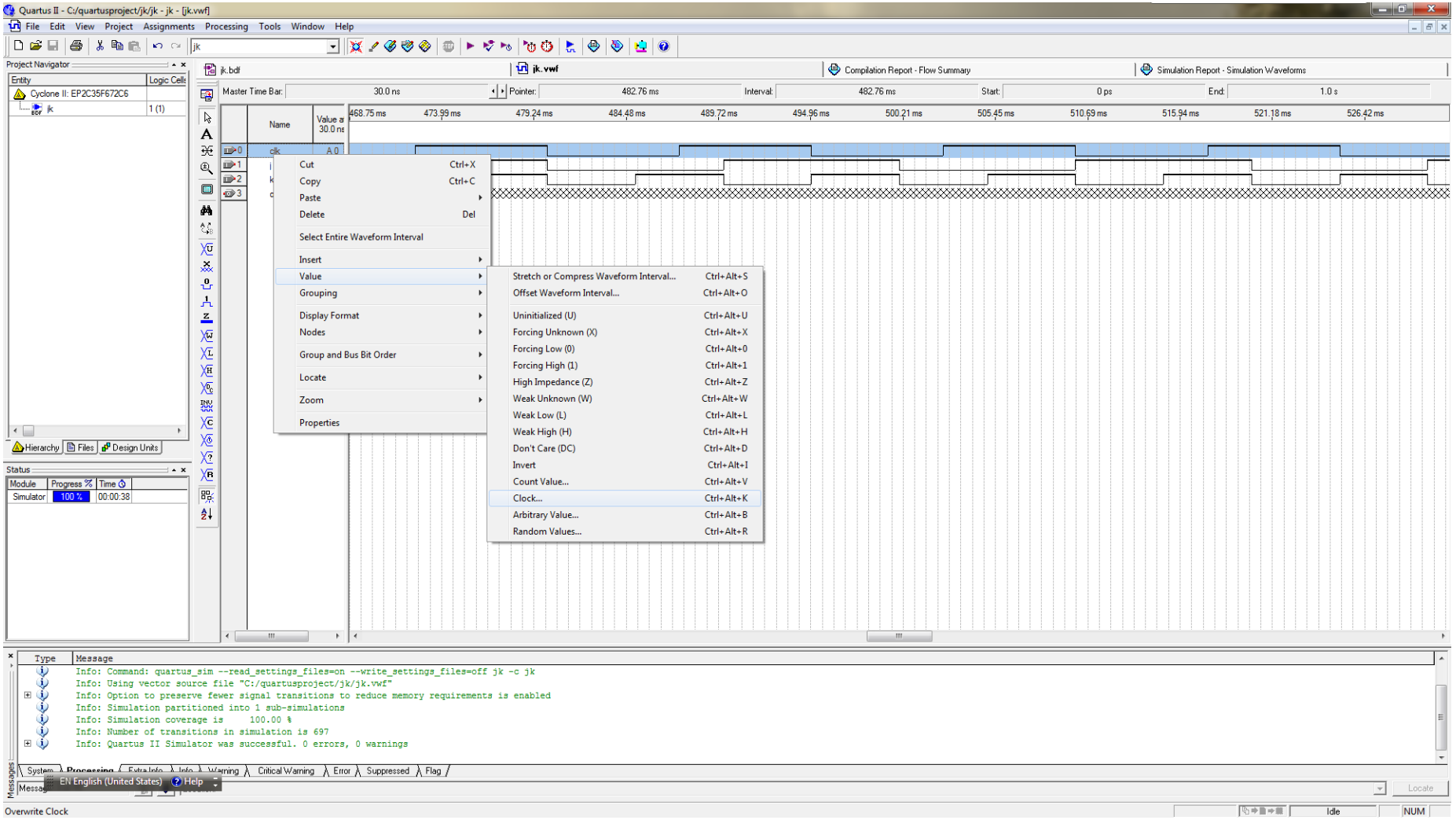
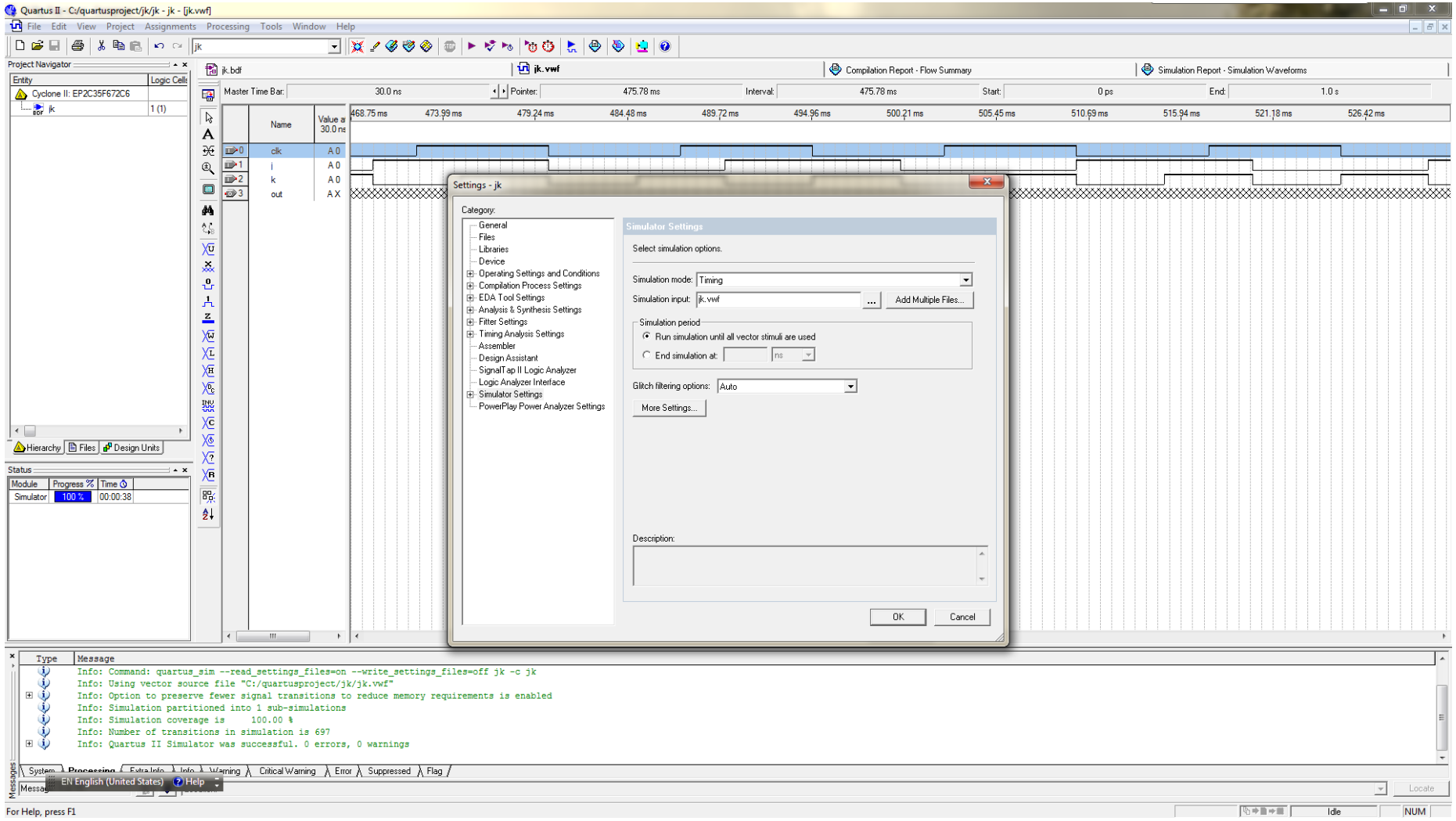
The issue of High impedance (XXX) result of JK flip flop when simulating with QuartusII

1. When you are doing sequential circuits, the time delay cannot be neglected especially when some inputs are dependent on any output.
2. The delay of the gates in our DE2 boards are also not negligible. Your default clock cycle is too fast for our DE2 board in sequential circuits. You have to try to slow it down to wait for the result to be settled.

Change your clk period to mili seconds level, and also change the period of the J and K to the similar level as the clock so you can see them in the same screen. (You can scroll you mouse to see more compacted waveforms.)



Don’t forget to change the simulation mode to ‘Timing’



Result

The JK flip flop is rising edge triggered