Low-Voltage Op-Amp

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EE 420

Final Project

The objective of this project is to design a low-voltage op-amp, one that can operate with a VDD down to 2V while driving a 10pF and 1k load. I will use On Semiconductor's C5 process. My design should be able to satisfy the following requirements:

- DC open-loop gain > 80dB under all load and VDD conditions
- Gain-bandwidth product should be > 1 MHz
- CMRR > 90dB at 100 kHz
- PSRR > 90dB at 100 kHz
- Slew-rate with maximum load > 1V/microsecond
- Input CMR extends above VDD and below ground
- Output swing within 100 mV of VDD and ground

I will use the following models text for my LTspice simulations:

NMOS

```
.MODEL NMOS NMOS (
+VERSION = 3.1            TNOM    = 27            LEVEL   = 8
+XJ      = 1.5E-7         NCH     = 1.7E17        TOX     = 1.39E-8
+K1      = 0.8351612      K2      = -0.0839158    VTH0    = 0.6696061
+K3B     = -7.6841108     W0      = 1E-8          K3      = 23.1023856
+DVT0W   = 0              DVT1W   = 0             NLX     = 1E-9
+DVT0    = 2.9047241      DVT1    = 0.4302695     DVT2W   = 0
+U0      = 458.439679     UA      = 1E-13         DVT2    = -0.134857
+UC      = 1.629939E-11   VSAT    = 1.643993E5    UB      = 1.485499E-18
+AGS     = 0.1194608      B0      = 2.674756E-6   A0      = 0.6103537
+KETA    = -2.640681E-3   A1      = 8.219585E-5   B1      = 5E-6
+RDSW    = 1.387108E3     PRWG    = 0.0299916     A2      = 0.3564792
+WR      = 1              WINT    = 2.472348E-7   PRWB    = 0.0363981
+XL      = 0              XW      = 0             LINT    = 3.597605E-8
+DWB     = 5.306586E-8    VOFF    = 0             DWG     = -1.287163E-8
+CIT     = 0              CDSC    = 2.4E-4        NFACTOR = 0.8365585
+CDSCB   = 0              ETA0    = 0.0246738     CDSCD   = 0
+DSUB    = 0.2543458      PCLM    = 2.5945188     ETAB    = -1.406123E-3
+PDIBLC2 = 2.311743E-3    PDIBLCB = -0.0272914    PDIBLC1 = -0.4282336
+PSCBE1  = 5.598623E8     PSCBE2  = 5.461645E-5   DROUT   = 0.7283566
+DELTA   = 0.01           RSH     = 81.8          PVAG    = 0
+PRT     = 8.621          UTE     = -1            MOBMOD  = 1
+KT1L    = -2.58E-9       KT2     = 0             KT1     = -0.2501
+UB1     = -4.8E-19       UC1     = -7.5E-11      UA1     = 5.4E-10
+WL      = 0              WLN     = 1             AT      = 1E5
+WWN     = 1              WWL     = 0             WW      = 0
+LLN     = 1              LW      = 0             LL      = 0
+LWL     = 0              CAPMOD  = 2             LWN     = 1
+CGDO    = 2E-10          CGSO    = 2E-10         XPART   = 0.5
+CJ      = 4.197772E-4    PB      = 0.99          CGBO    = 1E-9
+CJSW    = 3.242724E-10   PBSW    = 0.1           MJ      = 0.4515044
+CJSWG   = 1.64E-10       PBSWG   = 0.1           MJSW    = 0.1153991
+CF      = 0              PVTH0   = 0.0585501     MJSWG   = 0.1153991
+PK2     = -0.0299638     WKETA   = -0.0248758    PRDSW   = 133.285505
+AF      = 1              KF      = 0)            LKETA   = 1.173187E-3
*
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PMOS

```
.MODEL PMOS PMOS (                                LEVEL   = 8
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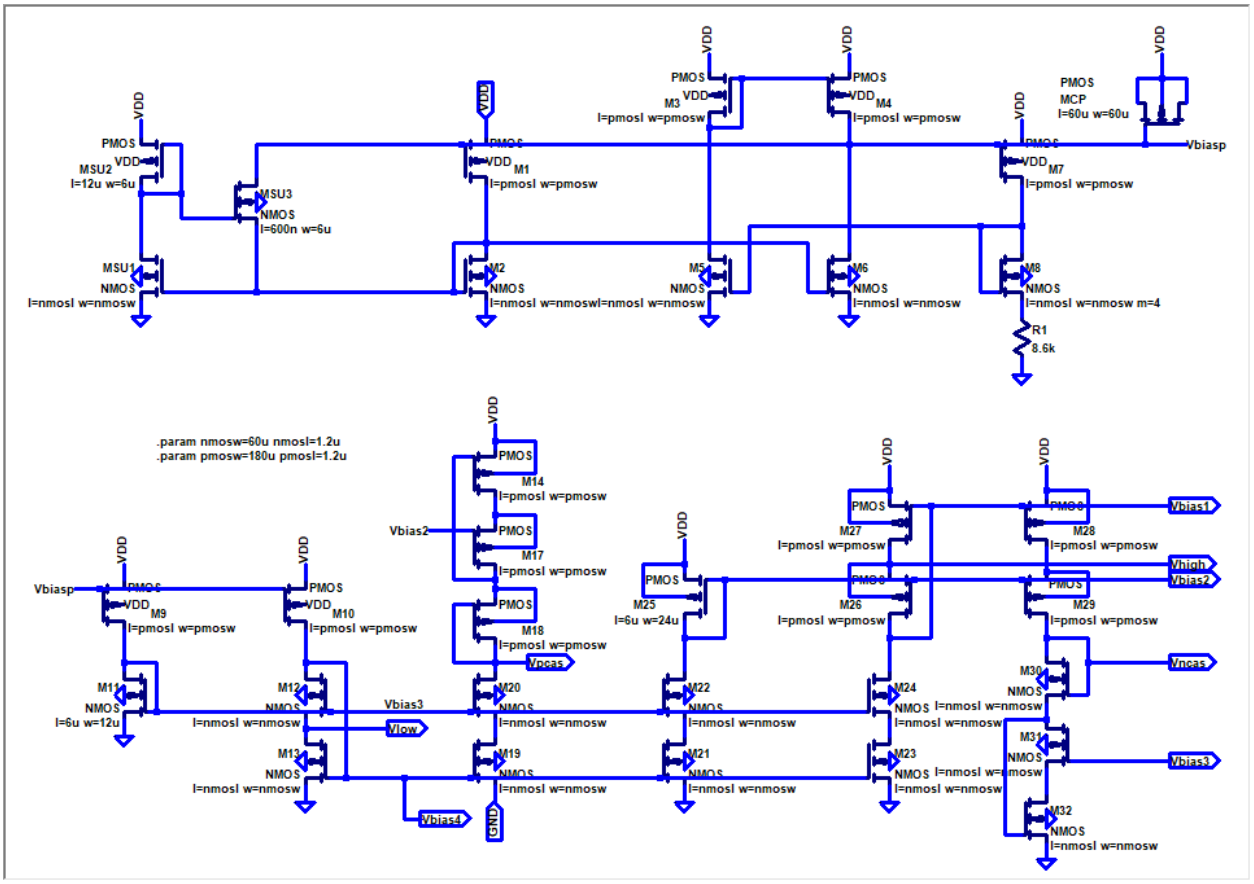
+XJ      = 1.5E-7         NCH     = 1.7E17        VTH0    = -0.9214347
+K1      = 0.5553722      K2      = 8.763328E-3   K3      = 6.3063558
+K3B     = -0.6487362     W0      = 1.280703E-8   NLX     = 2.593997E-8
+DVT0W   = 0              DVT1W   = 0             DVT2W   = 0
+DVT0    = 2.5131165      DVT1    = 0.5480536     DVT2    = -0.1186489
+U0      = 212.0166131    UA      = 2.807115E-9   UB      = 1E-21
+UC      = -5.82128E-11   VSAT    = 1.713601E5    A0      = 0.8430019
+AGS     = 0.1328608      B0      = 7.117912E-7   B1      = 5E-6
+KETA    = -3.674859E-3   A1      = 4.77502E-5    A2      = 0.3
+RDSW    = 2.837206E3     PRWG    = -0.0363908    PRWB    = -1.016722E-5
+WR      = 1              WINT    = 2.838038E-7   LINT    = 5.528807E-8
+XL      = 0              XW      = 0             DWG     = -1.606385E-8
+DWB     = 2.266386E-8    VOFF    = -0.0558512    NFACTOR = 0.9342488
+CIT     = 0              CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0              ETA0    = 0.3251882     ETAB    = -0.0580325
+DSUB    = 1              PCLM    = 2.2409567     PDIBLC1 = 0.0411445
+PDIBLC2 = 3.355575E-3    PDIBLCB = -0.0551797    DROUT   = 0.2036901
+PSCBE1  = 6.44809E9      PSCBE2  = 6.300848E-10  PVAG    = 0
+DELTA   = 0.01           RSH     = 101.6         MOBMOD  = 1
+PRT     = 59.494         UTE     = -1            KT1     = -0.2942
+KT1L    = 1.68E-9        KT2     = 0             UA1     = 4.5E-9
+UB1     = -6.3E-18       UC1     = -1E-10        AT      = 1E3
+WL      = 0              WLN     = 1             WW      = 0
+WWN     = 1              WWL     = 0             LL      = 0
+LLN     = 1              LW      = 0             LWN     = 1
+LWL     = 0              CAPMOD  = 2             XPART   = 0.5
+CGDO    = 2.9E-10        CGSO    = 2.9E-10       CGBO    = 1E-9
+CJ      = 7.235528E-4    PB      = 0.9527355     MJ      = 0.4955293
+CJSW    = 2.692786E-10   PBSW    = 0.99          MJSW    = 0.2958392
+CJSWG   = 6.4E-11        PBSWG   = 0.99          MJSWG   = 0.2958392
+CF      = 0              PVTH0   = 5.98016E-3    PRDSW   = 14.8598424
+PK2     = 3.73981E-3     WKETA   = 5.292165E-3   LKETA   = -4.205905E-3
+AF      = 1              KF      = 0)
```

I started my project by designing my bias circuit. A bias circuit is used to generate known voltages to apply to the gates of my circuits transistors. The voltages generated by my bias circuit will supply/sink my circuit with a known bias current. I first built the general short channel biasing circuit and tuned my sizes and resistor according to the bias current I was looking for. I chose to use a bias current of 5uA to keep my cascode branch voltages below VDD.

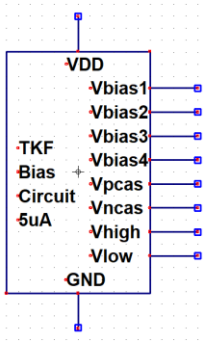
Image of my bias circuit:



LTspice file: mybiascircuit.asc

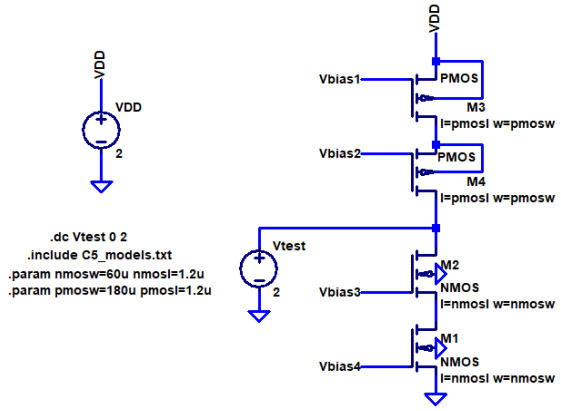
I created a symbol to represent this circuit to be used in my op-amp schematics. This will make my op-amp schematic easier to understand.

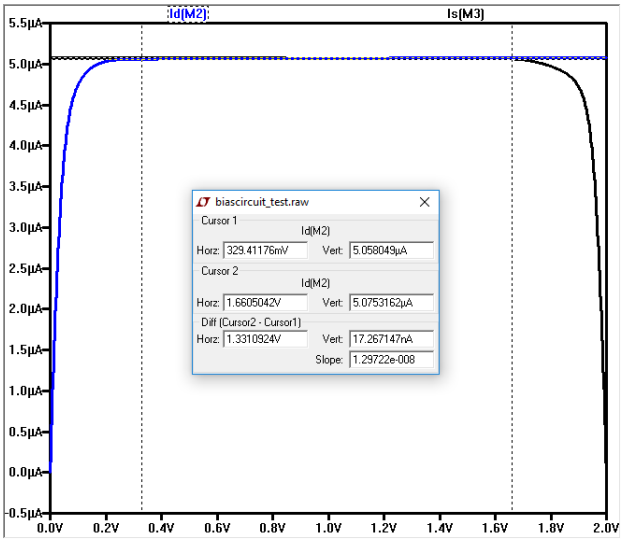
Image of my bias circuit symbol:



LTspice file: mybiascircuit.asy

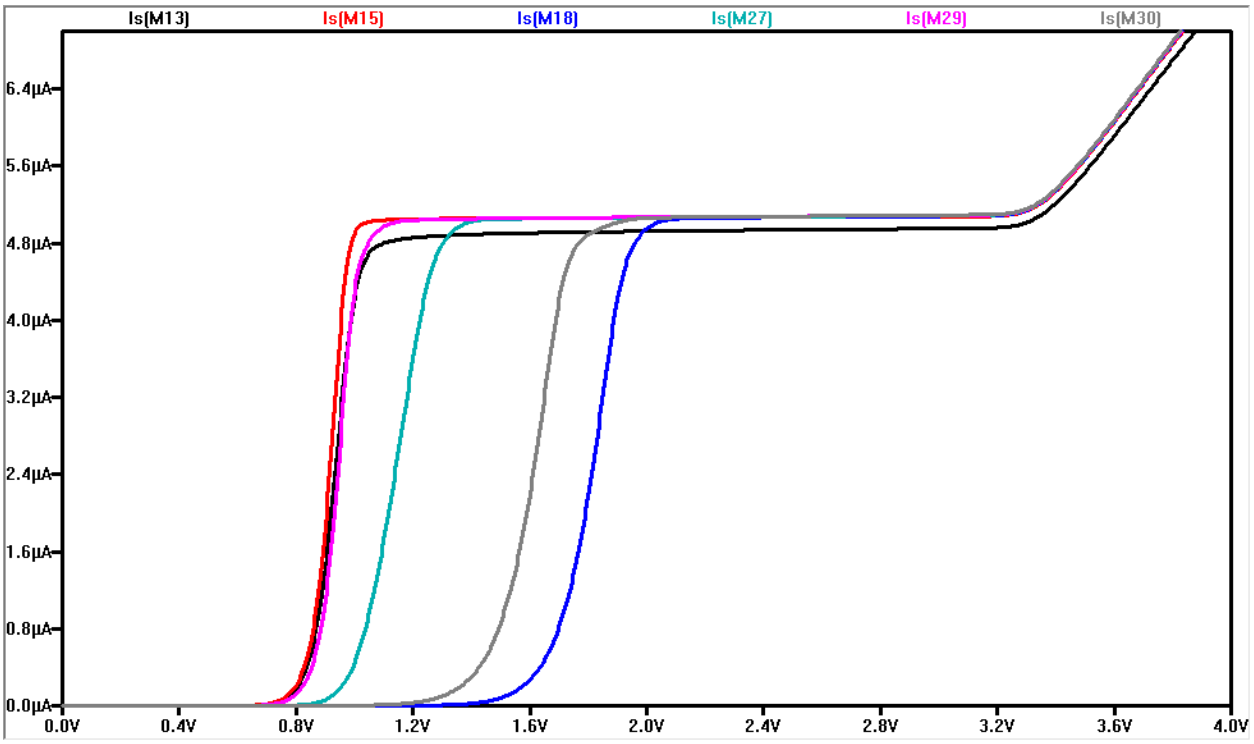
Testing my bias circuit by using current mirrors:





LTspice file: biascircuit_test.asc

I will also vary my VDD to see how the current changes with increases in power supply voltage. By doing this simulation I will be able to see how long my bias circuit will give me the correct bias voltages.

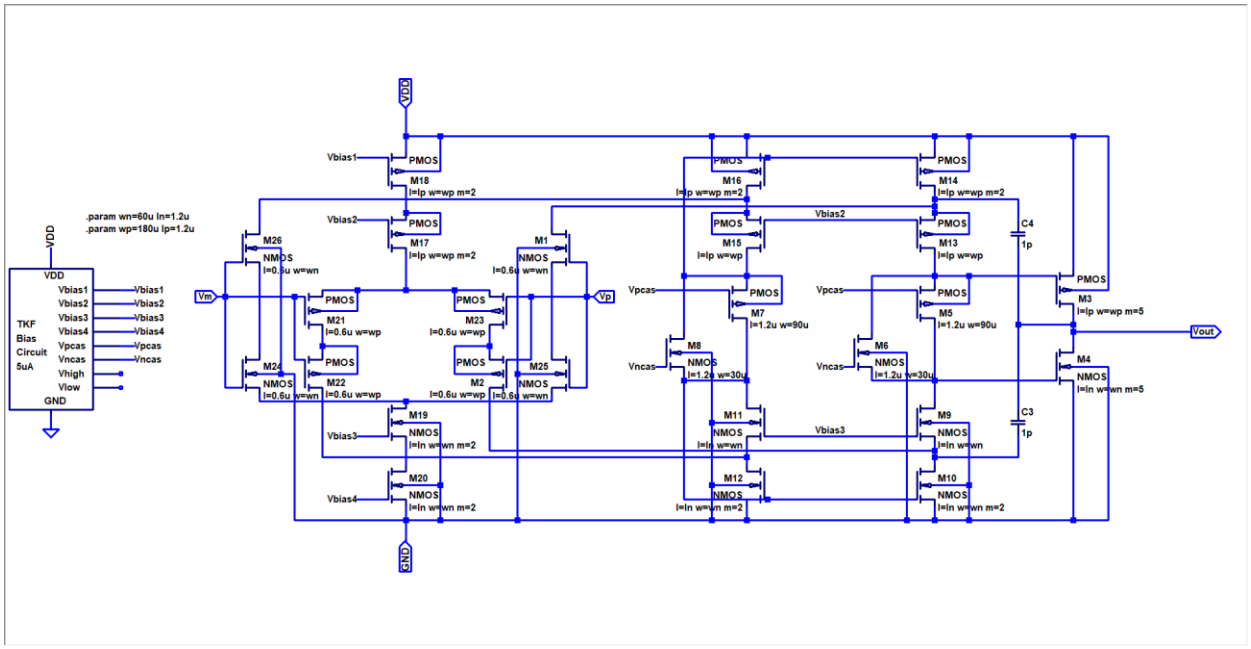


LTspice file: biascircuit_test1.asc

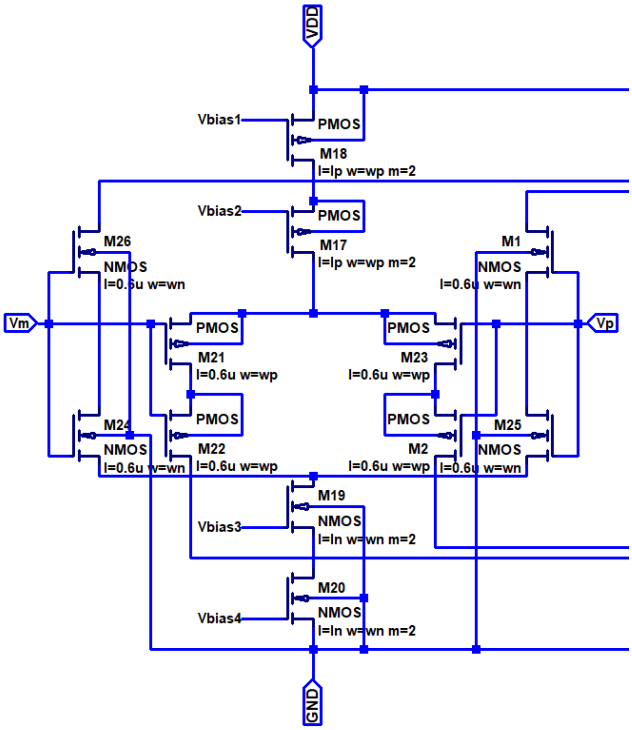
This simulation shows the current through each branch in my bias circuit as my VDD varies from 0 to 4 V. All of my branch currents are around 5uA before the power supply reaches 2V. The current begins to rise linearly when VDD passes 3.2V. This is good for our design since the voltages we will obtain from our circuit will give us 5uA from 2V to 3.2V.

Now that I have my bias circuit I will create the schematic for my op-amp. I will use an NMOS and PMOS diff amp connected to a push-pull amplifier for my general design. This topology will ensure that my input common-mode range extends above VDD and below ground and be able to drive the given load.

Image of my op-amp schematic and differential amplifier stage:



LTspice file: myopamp.asc

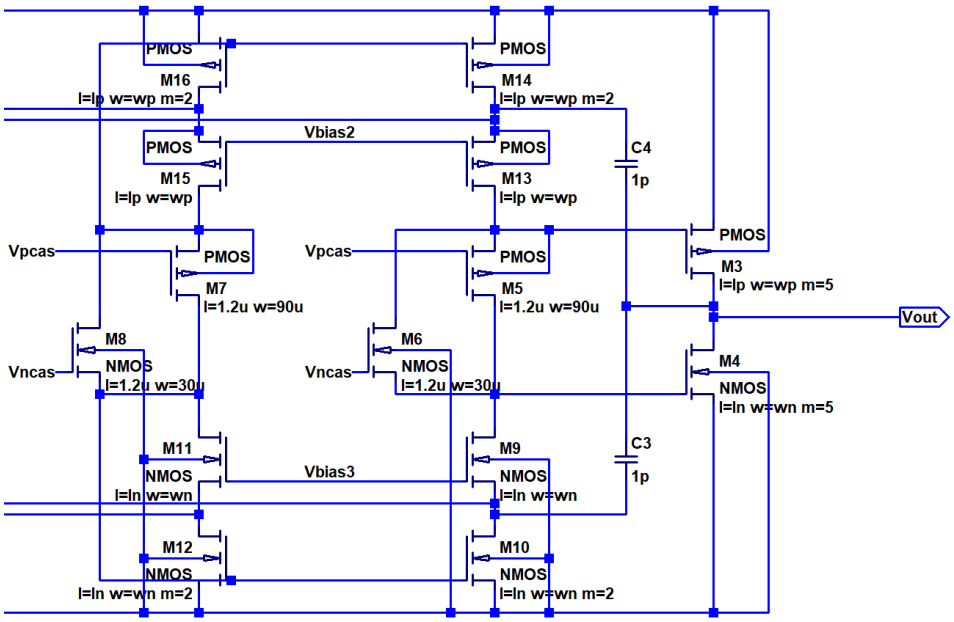


LTspice file: myopamp.asc

The basic operation of the diff amp is to compare the inputs on nodes Vm and Vp and amplify the difference between them. This topology allows an input CMR that extends above VDD and below ground. I decided to use split length input transistors to connect a compensation capacitor that will increase my circuit stability.

The push-pull stage of my op-amp is important to be able to drive the required load and meet the slew rate specification. This is done by increasing the widths of the output transistors so that enough current may flow to the load. The amplifier will also amplify the output of the diff amp, increasing the overall gain of my op-amp.

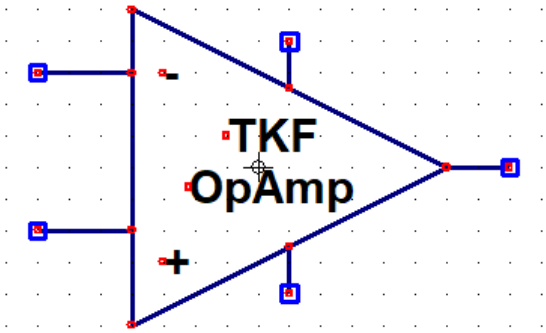
Image of my push-pull amplifier stage:



LTspice file: myopamp.asc

The top PMOS and bottom NMOS are used to source/sink current through this stage and are connected to the differential amplifier. The middle transistors are connected to the bias circuit and will limit the current flowing to the input of the push-pull. The widths are half the size of the other transistors to ensure half of the current will flow through the two branches to match the total current sink of the NMOS devices and current supply of the PMOS devices.

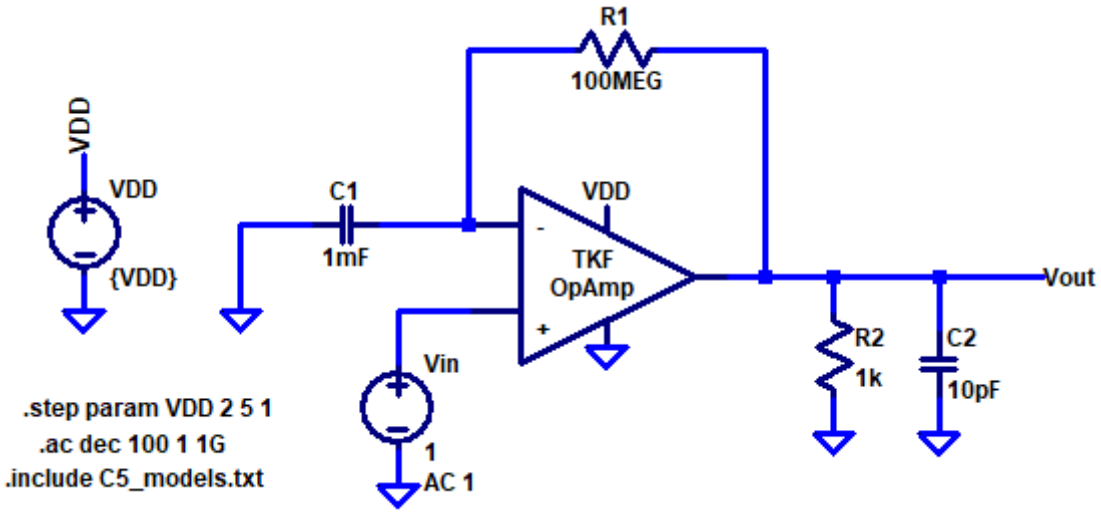
The symbol I made to represent my op-amp circuit:



LTspice file: myopamp.asy

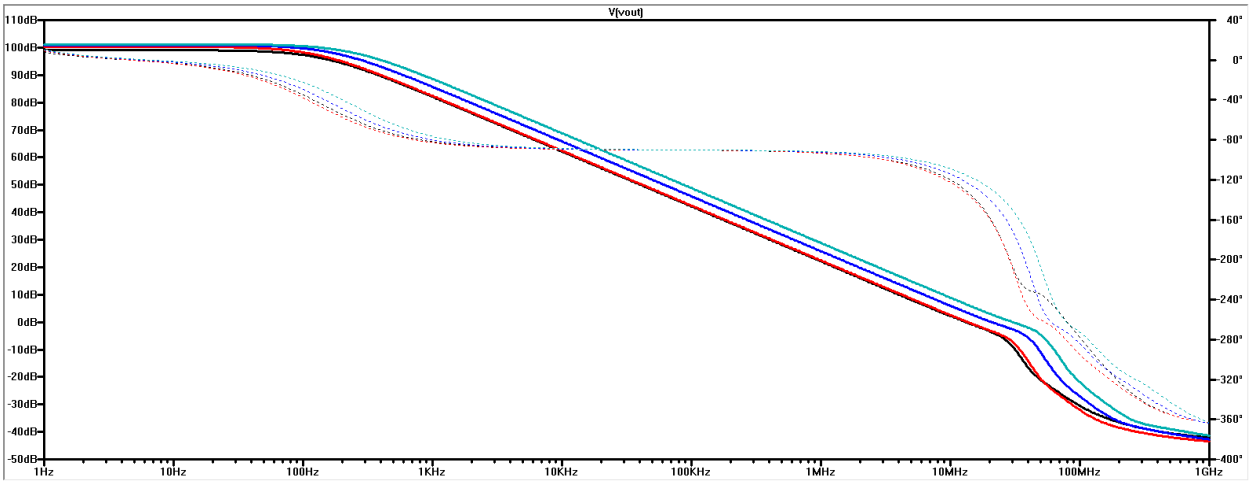
The top pin is connected to VDD in my circuit and the bottom pin is connected to ground. This symbol will be used in place of the original schematic to make the circuits easier to understand and easier to run different simulations. The first simulation I will perform is the frequency response of my op-amp while varying my power supply voltage.

Frequency response schematic:



LTspice file: opamp_ac_analysis1.asc

Simulation results:

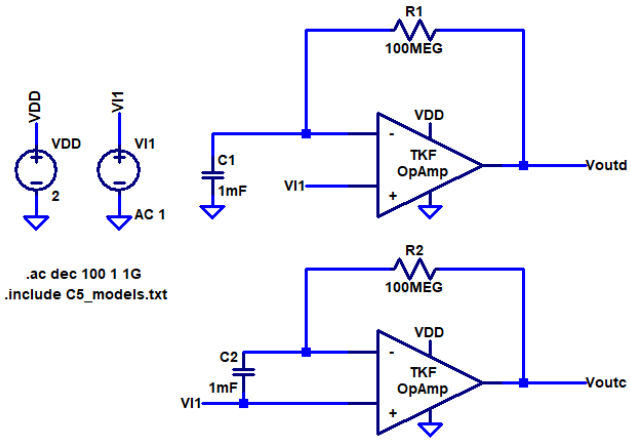


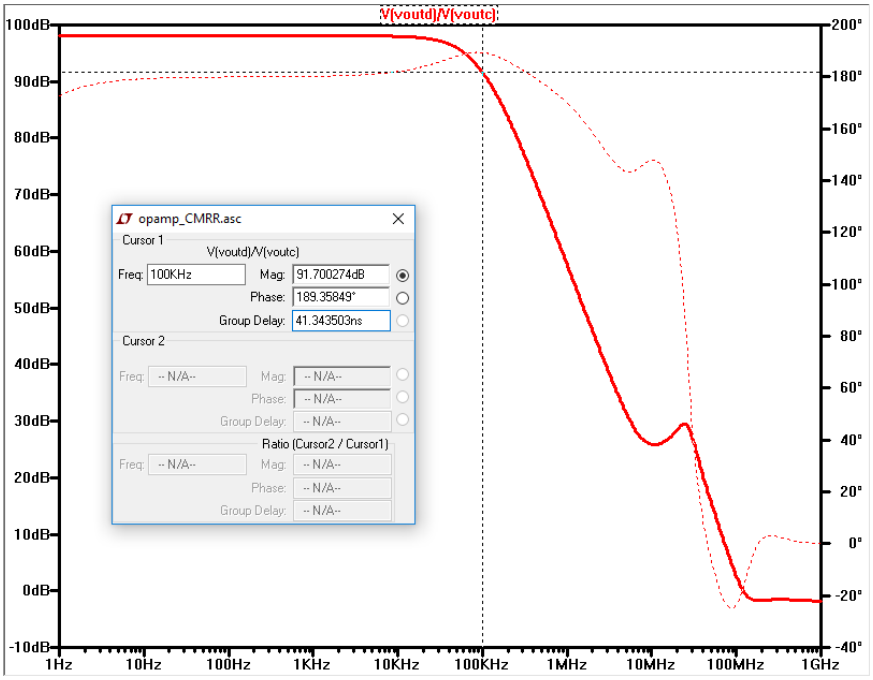
LTspice file: opamp_ac_analysis1.raw

VDD	DC Gain	Bandwidth	Phase at 0dB	Power
2	98.9dB	13.2MHz	-131°	2.16mW
3	100.2dB	13.6MHz	-136°	3.31mW
4	100.8dB	21.7 MHz	-144°	4.71mW
5	101.0dB	30.1 MHz	-149°	6.62mW

These simulations show me that I have a DC open-loop gain > 80dB and a gain-bandwidth product > 1MHz. My design has satisfied two of the requirements so far. One tradeoff I had to make was removing the split length transistor compensation capacitor to satisfy the CMRR requirement. Since I removed these capacitors I lost some high frequency stability and pushed my gain-bandwidth product further out.

I will now perform a simulation to show my op-amps common-mode rejection ratio. Common-mode rejection ratio is important for amplifier design because it allows the amplifier to reject input noise to the system. Below is the schematic and simulation that I made to show the CMRR.

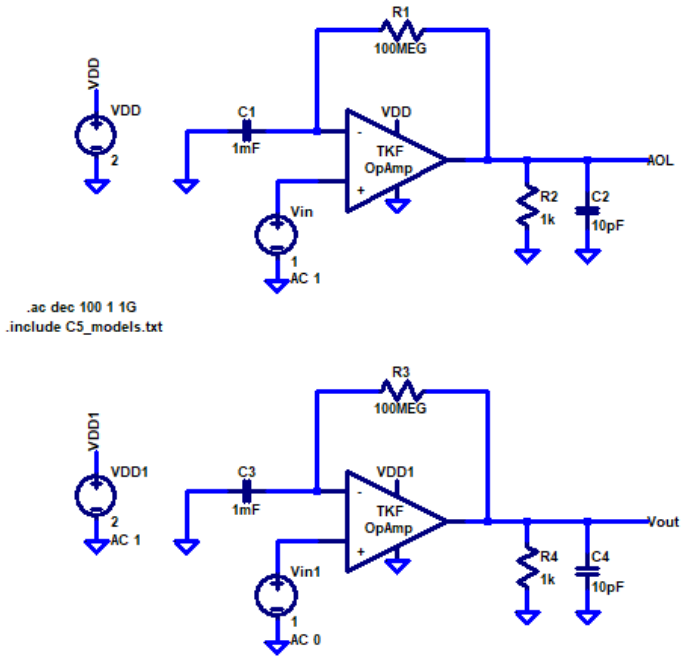


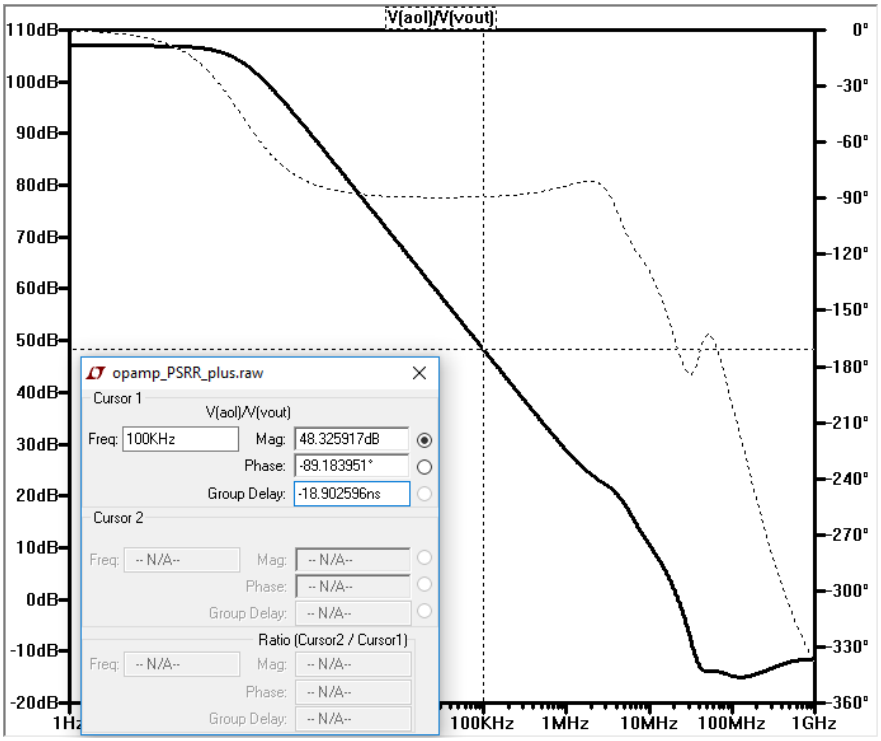


LTspice file: opamp_CMRR.asc

In the above simulation I could obtain a common-mode rejection ratio of 91.7dB at 100kHz satisfying the CMRR requirement.

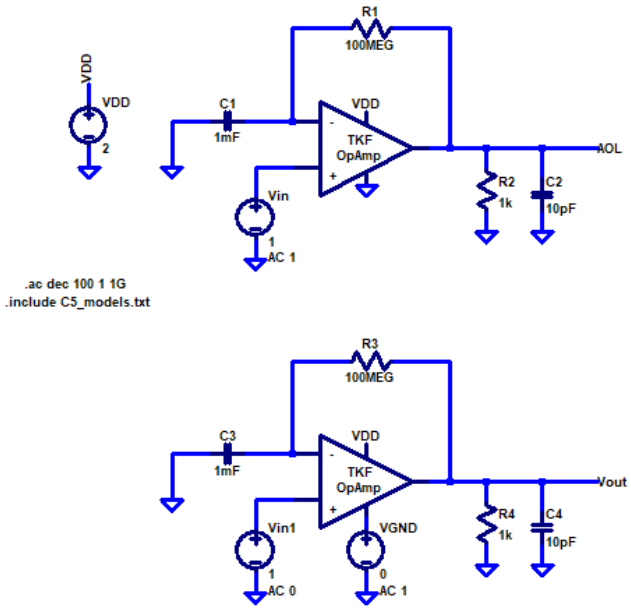
I will now check the power supply rejection ratio of my op-amp. Below is the schematic and simulation for the positive power supply rejection ratio.

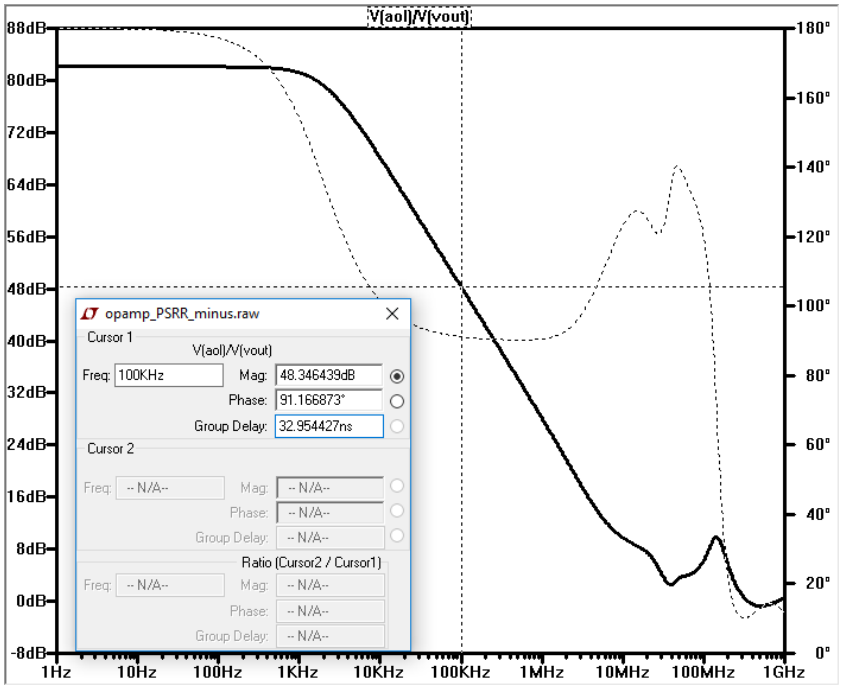




LTspice file: opamp_PSRR_plus.asc

Below is the schematic and simulation for the negative power supply rejection ratio.

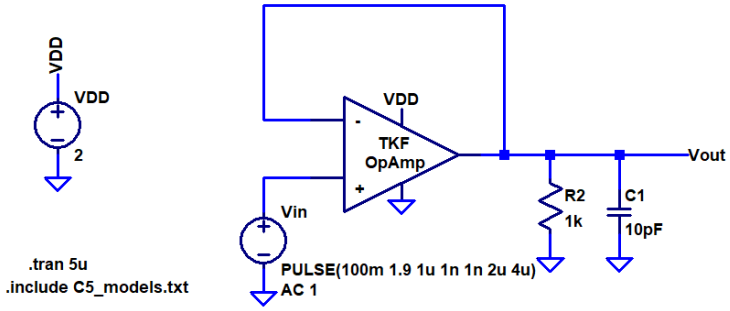


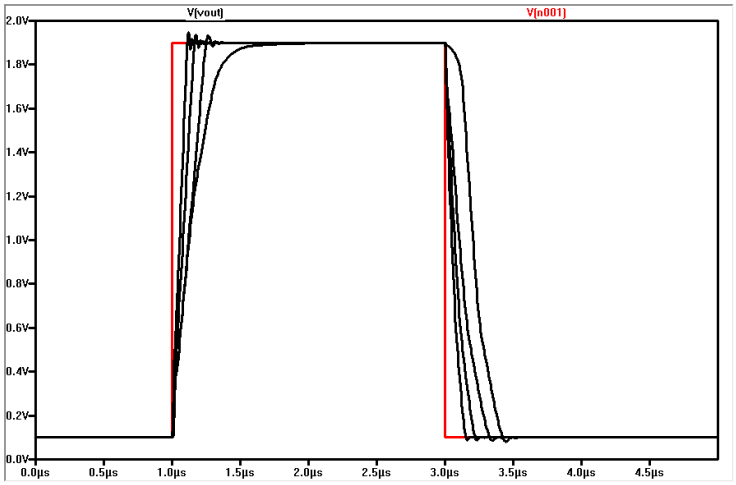


LTspice file: opamp_PSRR_minus.asc

Looking at the PSRR plus and minus of my op-amp I was not able to obtain the design requirement of the project. After many trials I was not able to obtain PSRR > 90dB at 100kHz while still meeting the other 6 requirements.

The next requirement for my project is to have a slew-rate greater than 1V/us. The slew-rate is how quickly my circuit will charge and discharge a capacitive load. Below is the schematic and corresponding simulation results.





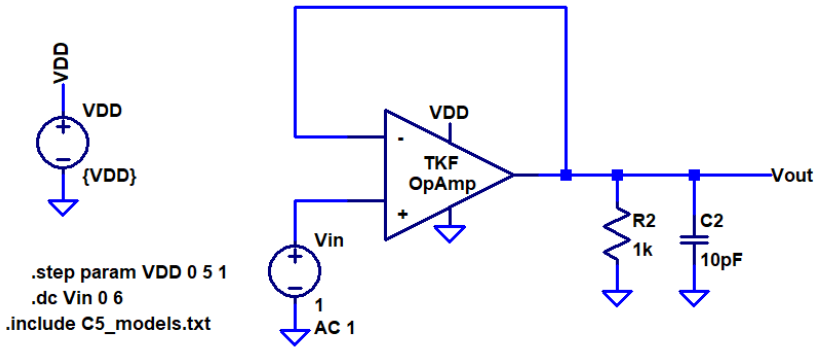
LTspice file: opamp_transient2.asc

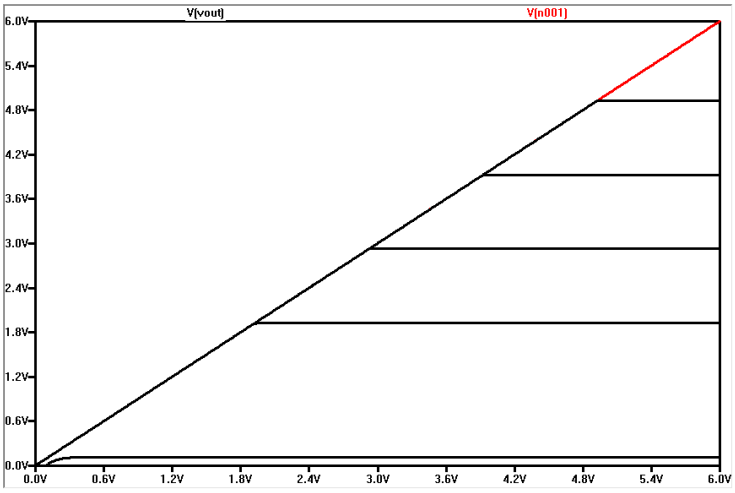
Table of cursor values for the above simulation:

VDD	2	3	4	5
Slew-Rate	2.50V/us	5.81V/us	8.68V/us	12.3V/us

I was able to get my op-amp design to have a slew-rate greater than 1V/us. I can also fix the overshoot of the output by adding compensation capacitors to the split length transistors at the cost of my CMRR.

I will now test my op-amps output swing by putting the op-amp in a follower configuration and sweeping the input voltage and comparing it the output which changes in VDD.



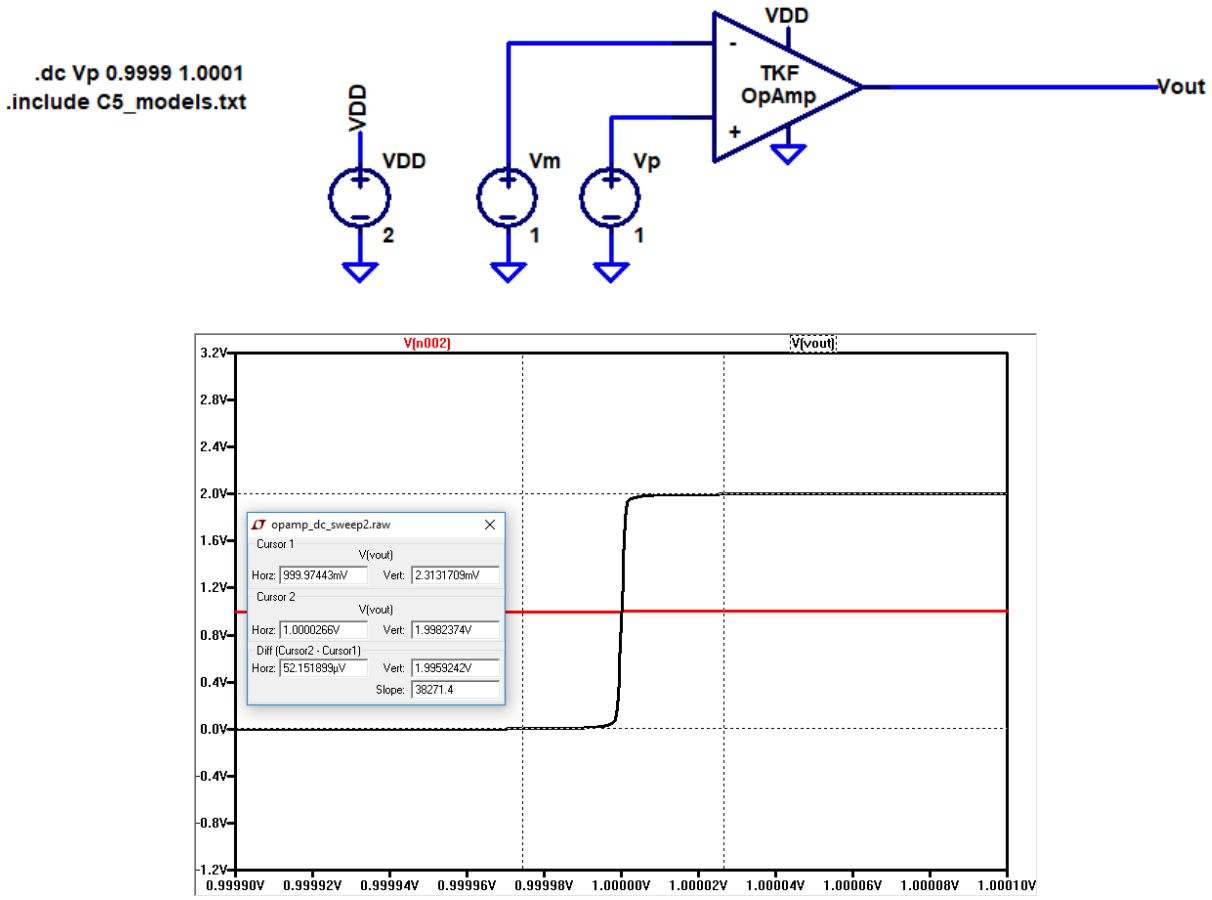


LTspice file: opamp_dc_sweep1.asc

Table with cursor values for the above simulation:

VDD	0V	1V	2V	3V	4V	5V
Vin	0V	575.5mV	1.95V	2.95V	3.92V	4.92V
Vout	0V	112.3mV	1.92V	2.93V	3.92V	4.92V

I will also do a simulation holding the minus terminal at a constant voltage and varying the plus terminal. This will show the full output swing of my op-amp.

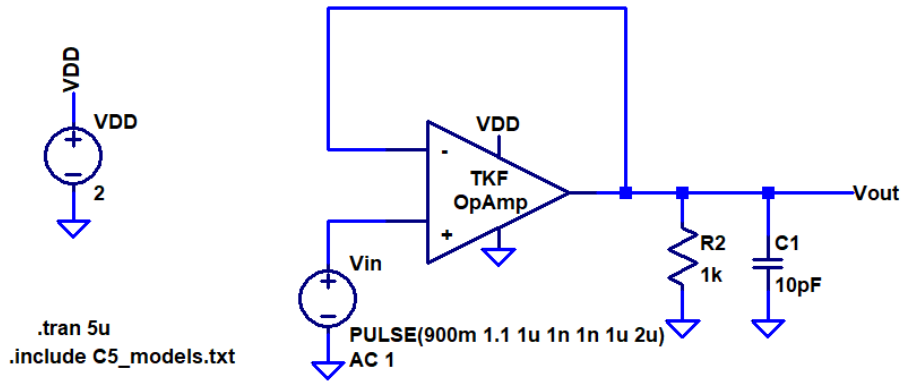


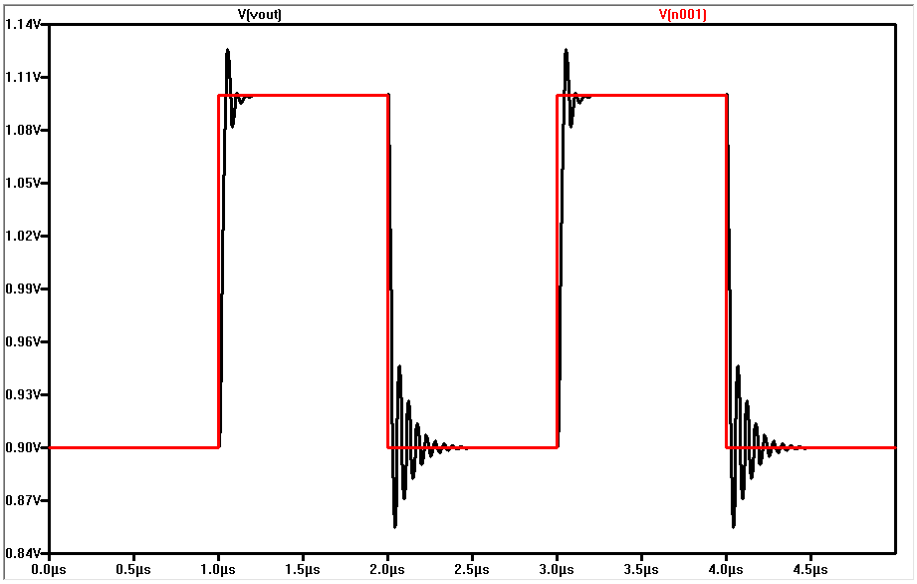
LTspice file: opamp_dc_sweep2.asc

In my simulation my output will swing from 2.31mV to 1.99V which is within 100mV of ground and VDD respectively. My op-amp satisfies my output swing design requirement.

I will test the stability of my output when there is a pulsed input. I will do this by putting my op-amp in the follower configuration and pulse the positive terminal. I will compare the output signal to my input signal.

Schematic:





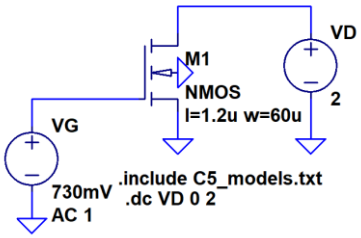
LTspice file: opamp_transient1.asc

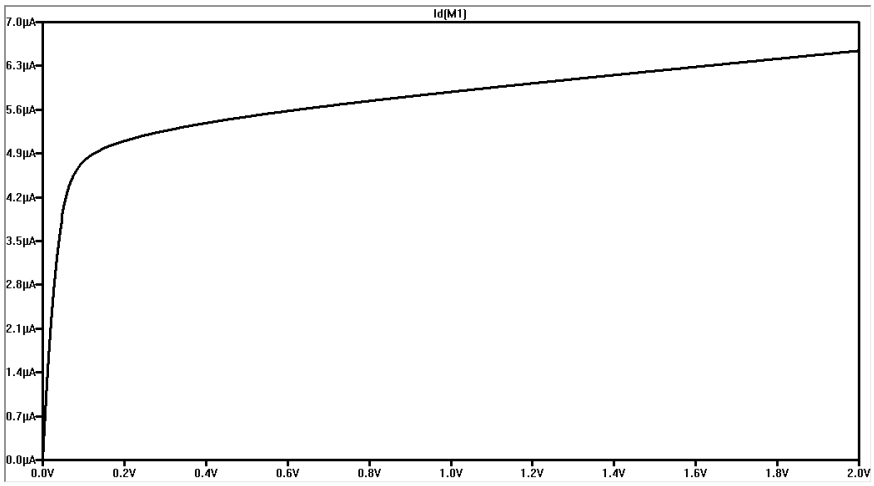
I have some ringing on my output which can be lowered by changing the lengths of my bias transistors. If I decrease the length of the bias current sources the ringing will lower. I can also add compensation capacitors to the split length transistors to lower the ringing.

MOSFET Parameters followed by the simulations I used to obtain them:

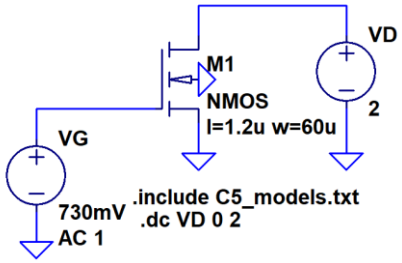
Parameter	NMOS Device	PMOS Device	Comments
Bias current, ID	$5\mu A$	$5\mu A$	Chosen Bias ID
W/L	$60\mu/1.2\mu$	$180\mu/1.2\mu$	Selected
Vds,sat and Vsd,sat	25mV	25mV	Found in ro sim
Vovn and Vovp	30mV	30mV	1.5% VDD
Vgs and Vsg	730mV	930mV	Vth+Vov
Vthn and Vthp	700mV	900mV	Found in sims
C'ox	$2.5fF/\mu m^2$	$2.5fF/\mu m^2$	$\frac{\epsilon_{ox}}{t_{ox}}$
Coxn and Coxp	$180fF$	$540fF$	C'ox *WL
Cgsn and Csgp	$120fF$	$360fF$	$\frac{2}{3}Cox$
Cgdn and Cdgp	$12fF$	$52.2fF$	$CGDO * W$
gmn and gmp	148uA/V	136uA/V	Found in sims
ron and rop	$1.14M\Omega$	$1.06M\Omega$	Found in sims
gmn*ron and gmp*rop	168V/V	144V/V	
λ_n and λ_p	$0.175V^{-1}$	$0.188V^{-1}$	$\frac{1}{I_{D,sat} * r_o}$
f_{Tn} and f_{Tp}	177.8MHz	64.56MHz	Found in sims

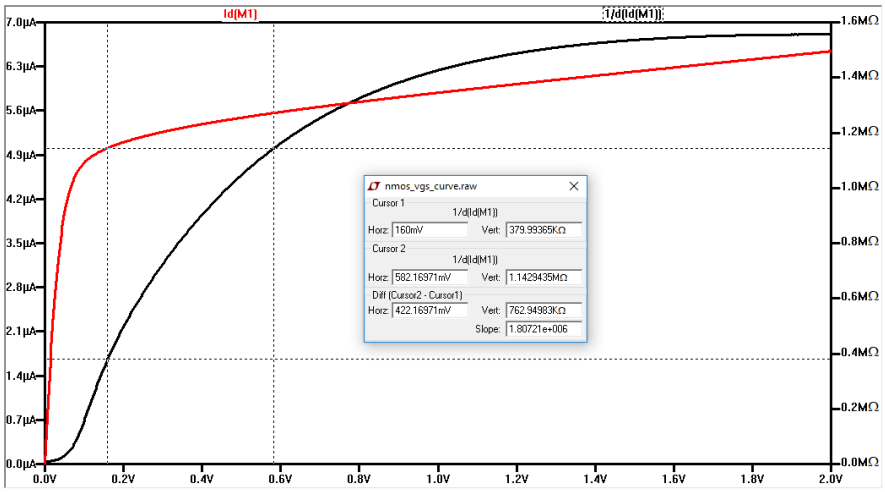
NMOS VGS Curve



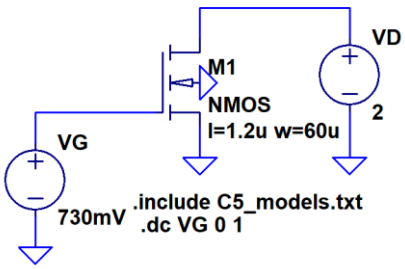


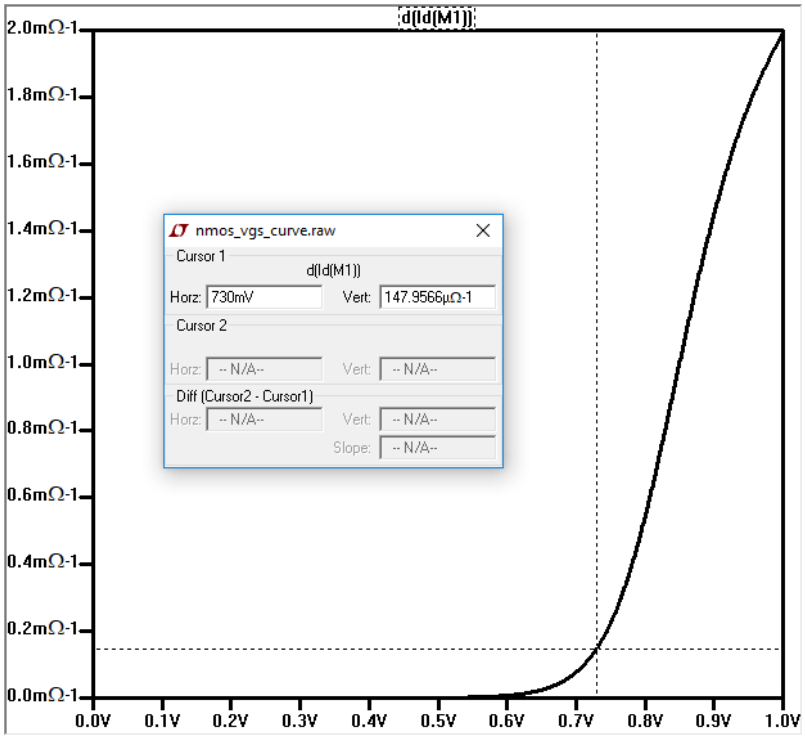
NMOS Output Resistance



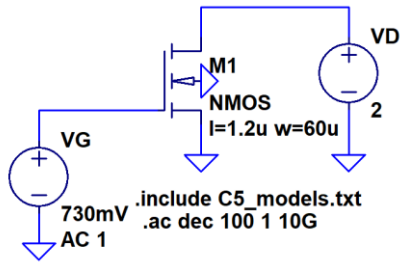


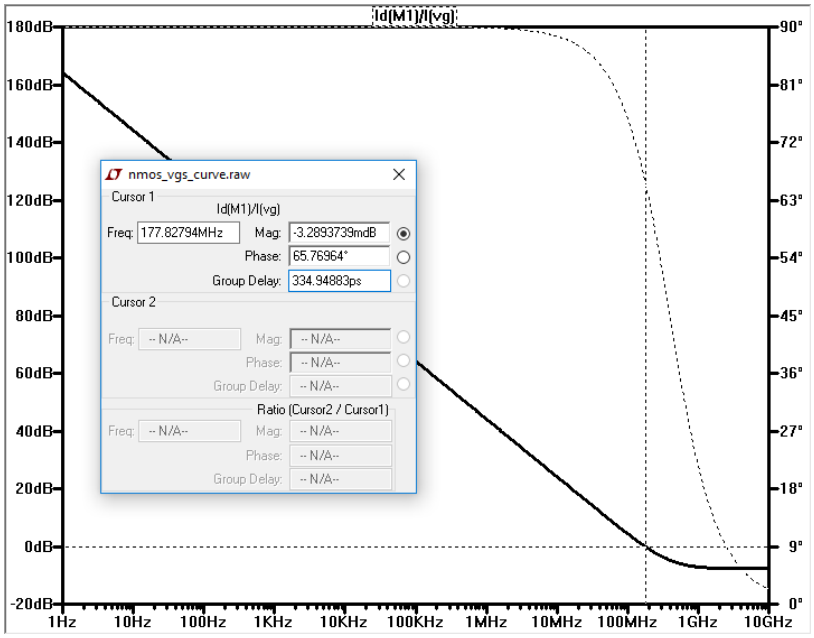
NMOS Transconductance



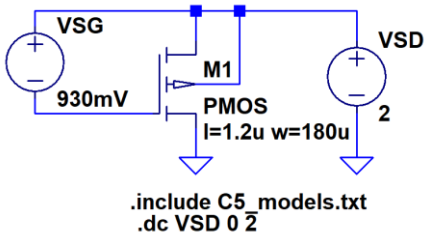


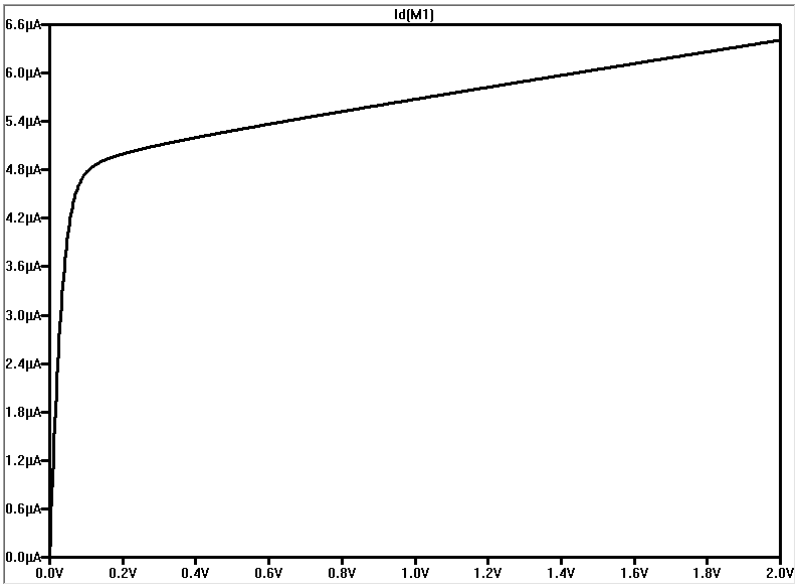
NMOS Transition Frequency



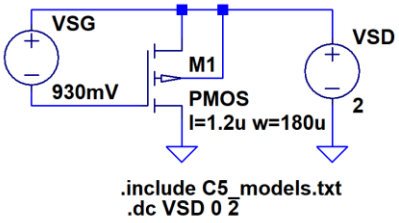


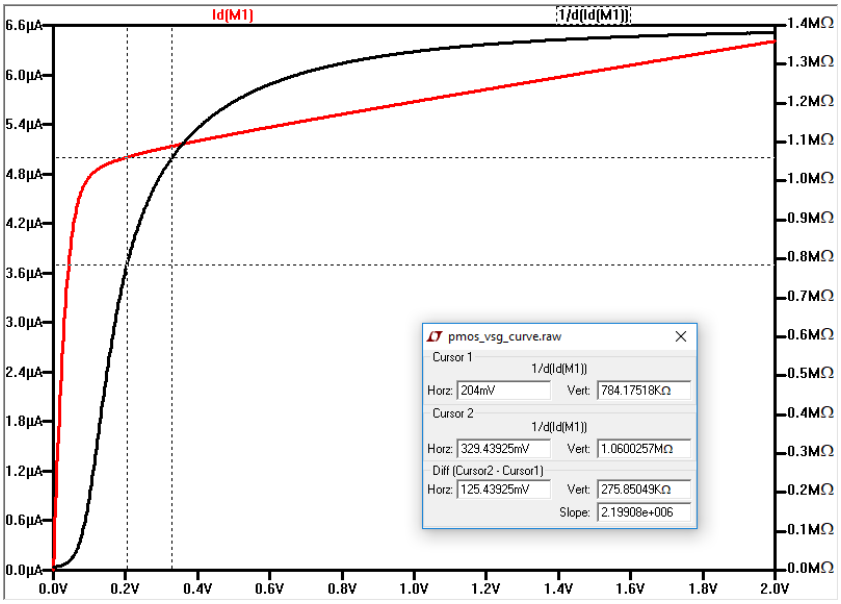
PMOS VSG Curve



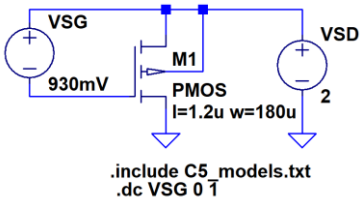


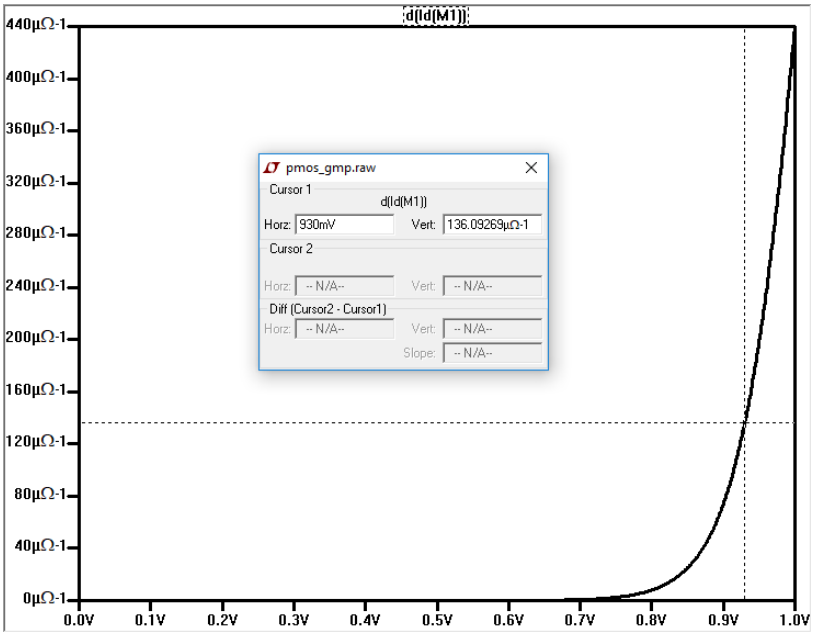
PMOS Output Resistance





PMOS Transconductance





PMOS Transition Frequency