CMOS Synchronous Buck Switching Power Supply

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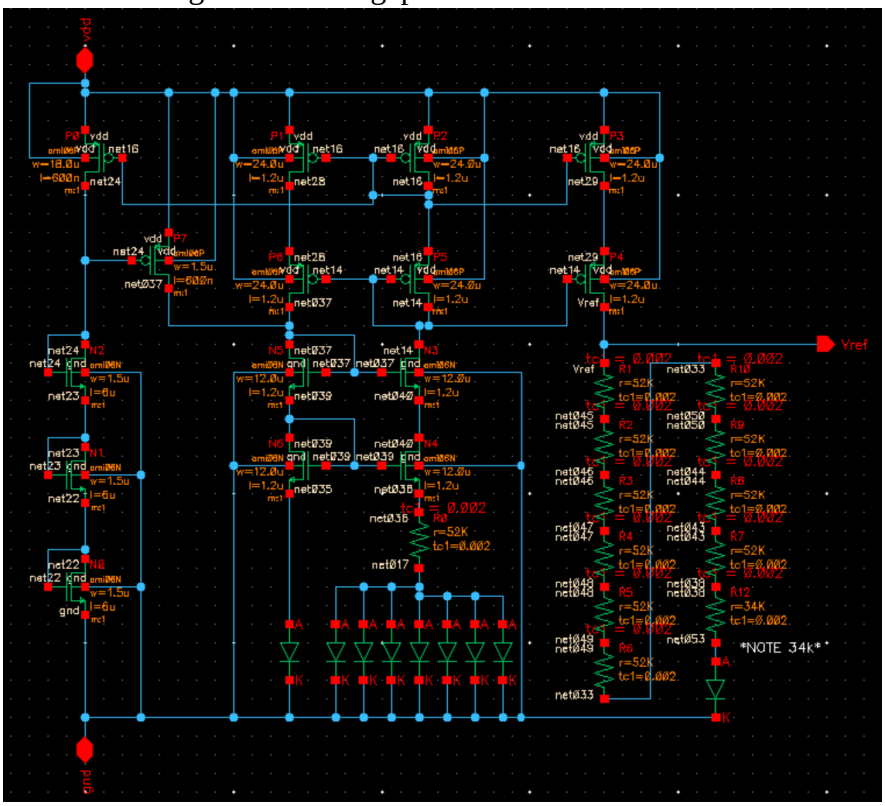
EE 421

Final Project

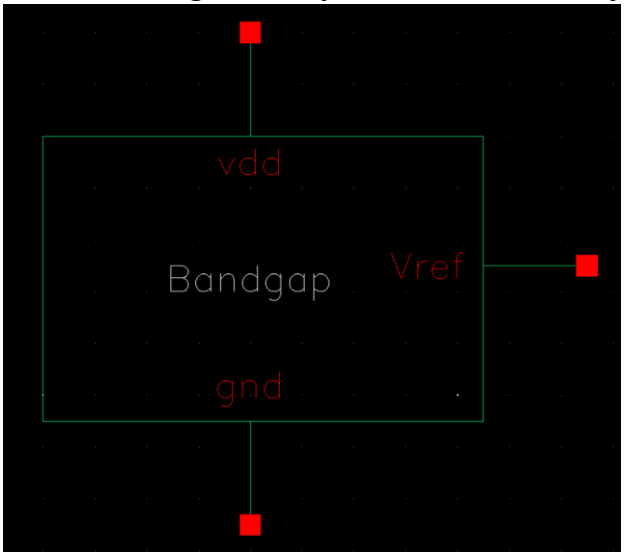
Bandgap Circuit

The first part for this project is to layout and understand the bandgap circuit. A bandgap circuit is used to generate a reference voltage that does not vary with changes in temperature or source voltage. This will be useful in this project because it will allow me to create a feedback loop in my circuit to compare the output voltage. This will allow the circuit to sense what the output voltage is and make the correct fixes to obtain a stable output voltage.

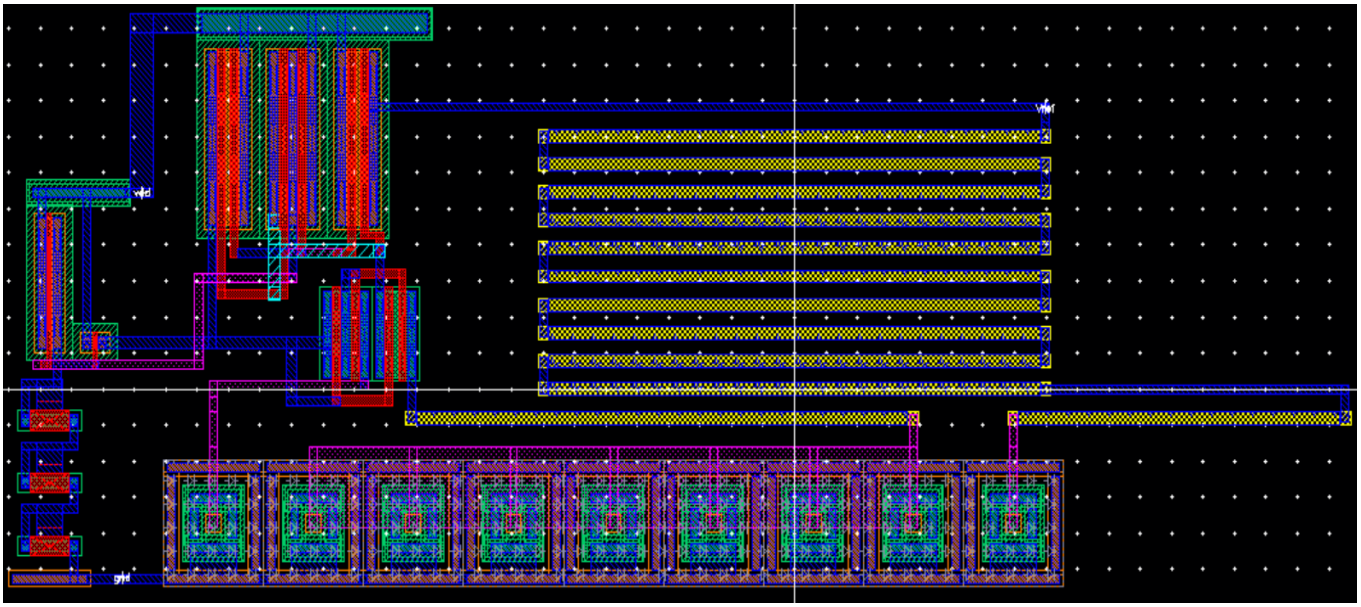
Here is an image of the bandgap schematic:



Here is an image of the symbol that I used in my circuit:



Here is the layout for the bandgap circuit:



Verifying my layout:

DRC:

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**********   Summary of rule violations for cell "bandgap layout"   **********
   Total errors found: 0
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LVS:

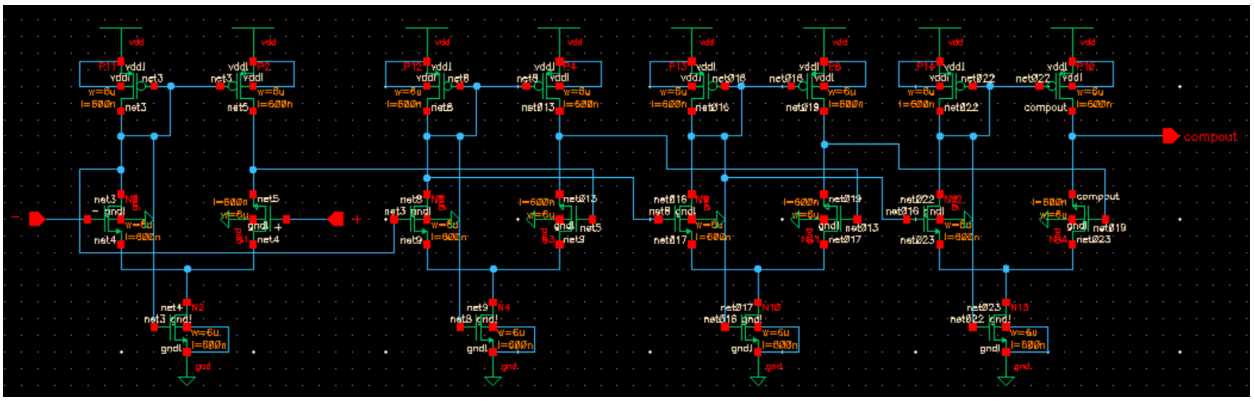
Comparator Circuit

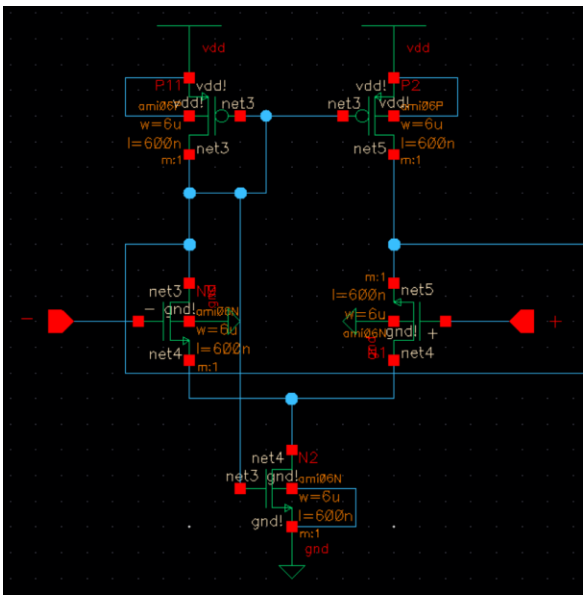
For the circuit to consistently have a desired output voltage the circuit must have something to sense and compare. The comparator circuit will take two input voltages, compare them, and output a corresponding voltage depending on which voltage is higher or lower. This will allow for the circuit to make corrections to output the desired voltage by having the comparator circuit dictate whether the PMOS should turn on or the NMOS should turn on.

Case	Output
V+ < V-	Logic Low
V+ > V-	Logic High

Using the above logic, I can design my circuit according to what I need in order to obtain a consistent output voltage.

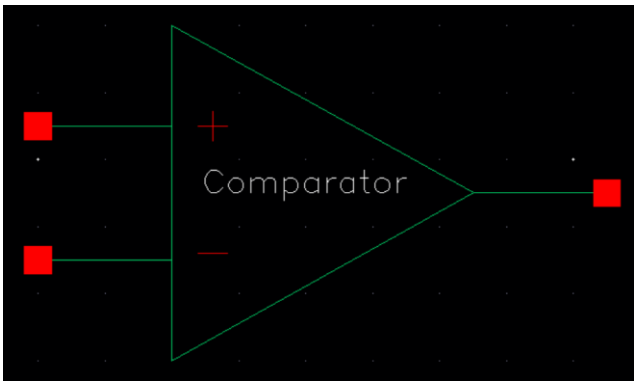
Here is an image of my comparator circuit:





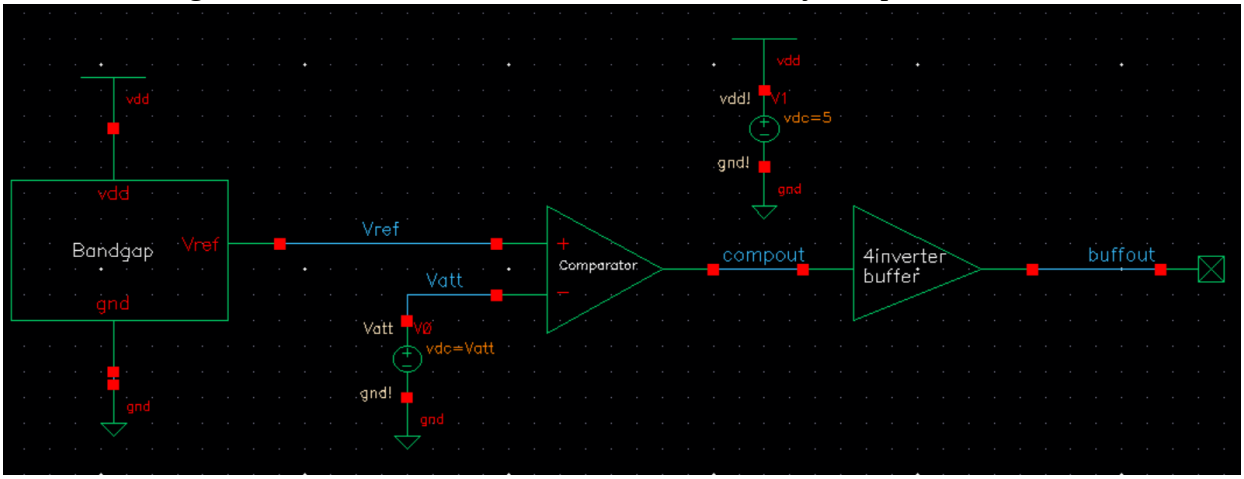
I am using a four-stage comparator to keep my transistor sizes low but still obtain a high gain. A tradeoff of high gain is low current and slow speeds. The slow speeds will be useful in this design to allow the feedback loop to send the error back to the comparator. The reason I need a high gain is to sense the difference in voltage at my inputs. If my gain is low the circuit will not sense as much error compared to a high gain comparator. In the schematic I have sized all of my devices as 6u/0.6u in order for a nicer layout.

Here is an image of the symbol that I will use in my converter circuit:



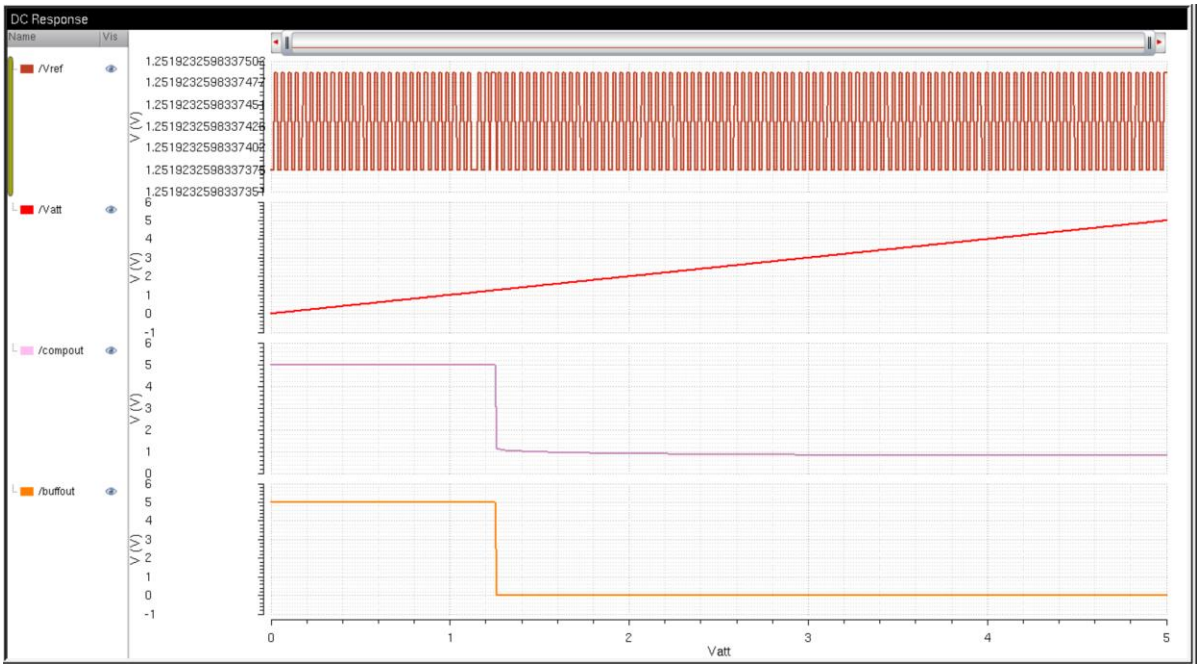
The implementation of this circuit in my overall design will be used to compare the output voltage with the bandgap voltage and dictate whether the PMOS or the NMOS should be on. Since the bandgap reference voltage is at 1.25V and our desired output voltage is 2.5V we will need to have our output voltage go through a voltage divider before entering our comparator.

Here is an image of the schematic that I will use to simulate my comparator:

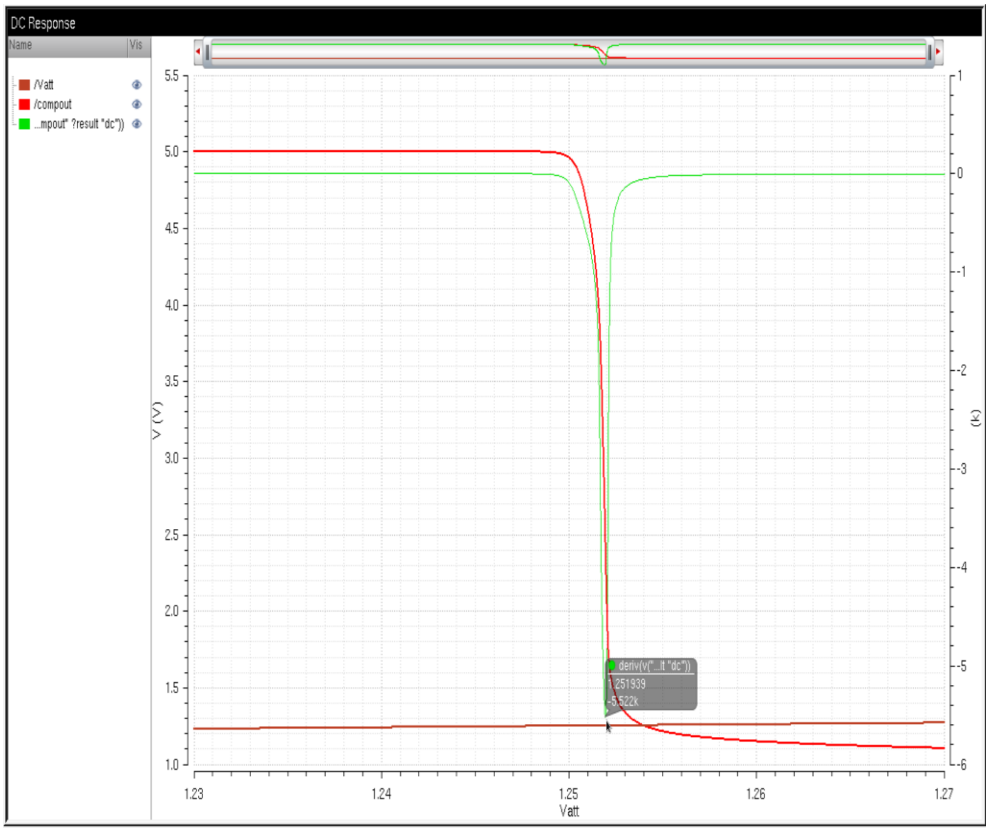


In this schematic I am using the bandgap circuit as my reference voltage and a dc voltage source as my Vout. I will sweep the voltage on the source to simulate the output voltage oscillating around 2.5V.

Here is the resulting simulation:



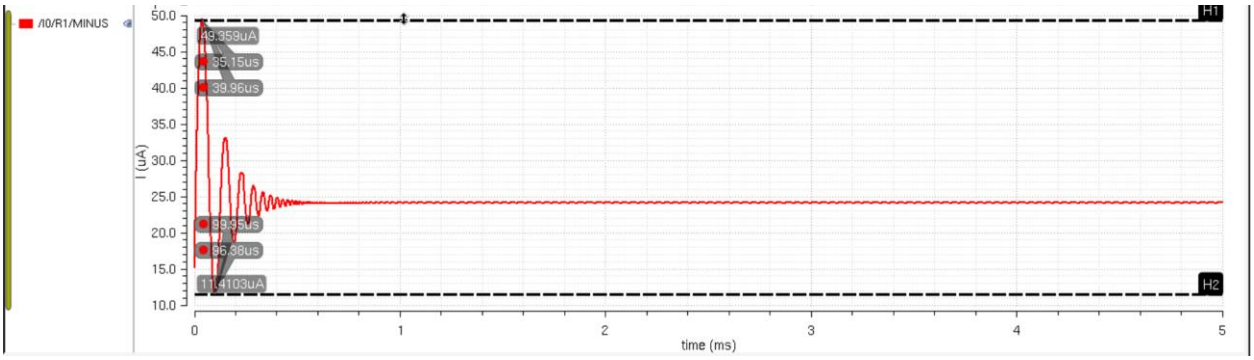
Now that I have my simulations I can find the gain of my comparator by taking the derivative of the output from the comparator. This will plot a line on the graph that will show me my gain at the point the output switches.



In this simulation, we can see that the gain is a negative number. This is because the output voltage is going from high to low giving us a negative slope. The maximum magnitude of this line is the gain of the comparator.

The gain of this comparator is 5.522K

For this project the comparator circuit is supposed to draw between 10uA and 50uA from the output. Here is an image of the current drawn from the output:



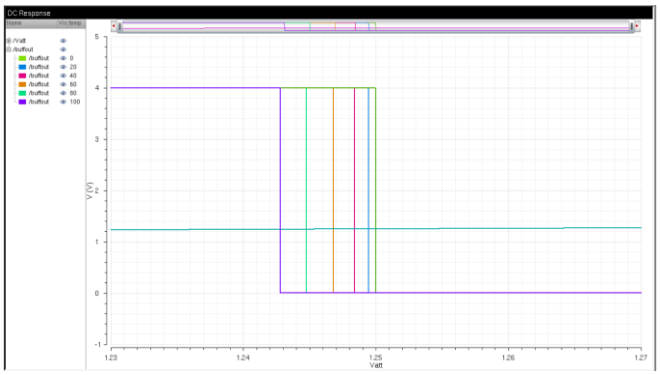
To stay below 50uA and above 10uA I chose resistor values of 52K Ω.

The drawn current is found by: $I_{drawn} = \frac{V_{out}}{R_{total}} = \frac{2.5V}{104K} = 24uA.$

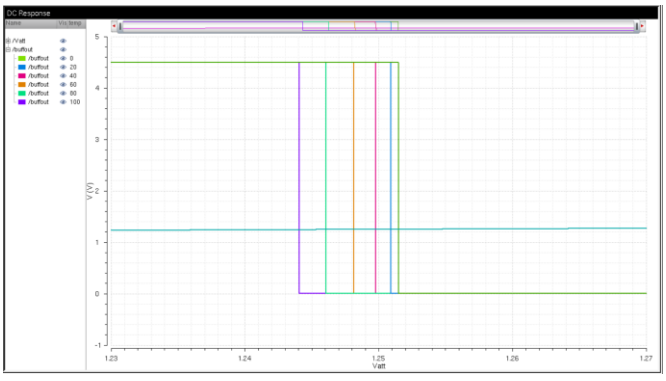
Another reason I choose these values is because I already had the layouts for these resistors.

Now that I have the gain of my comparator and the current it draws I can do parametric analysis varying the temperature of the circuit. I will plot the output of my comparator with changes in temperature at different values of VDD.

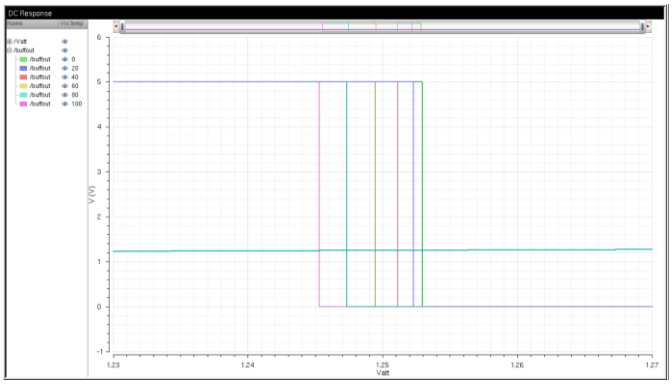
VDD = 4V



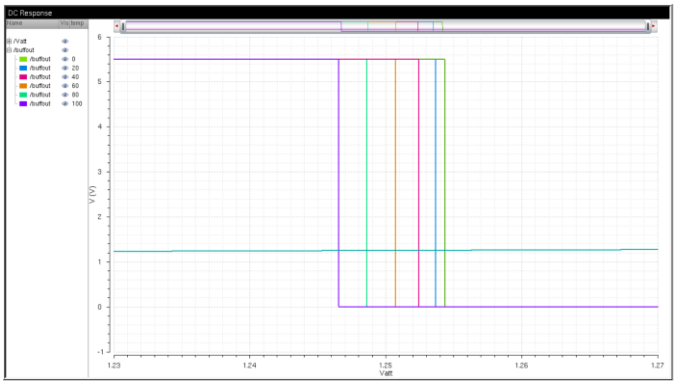
VDD = 4.5V



VDD = 5V



VDD = 5.5V



Temperature Increases	Switching Point Decreases
VDD Increases	Switching Point Increases

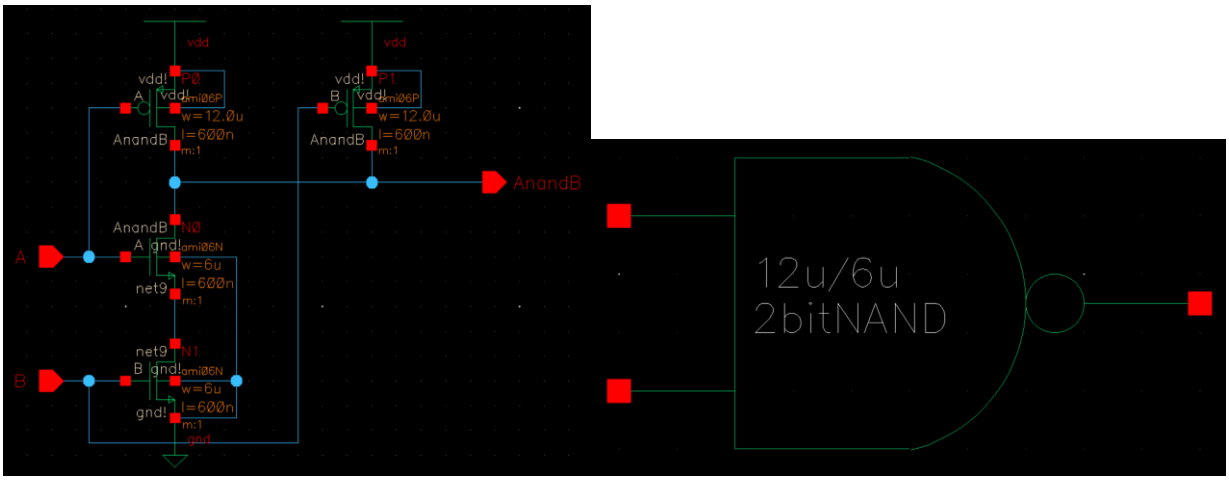
In these analyses the switching point voltage is shifting to the right when the VDD increases. The switching point also increases with a lower temperature. These analyses show that the temperature and VDD influence the switching point voltages of this circuit.

Nonoverlapping Clock Generator

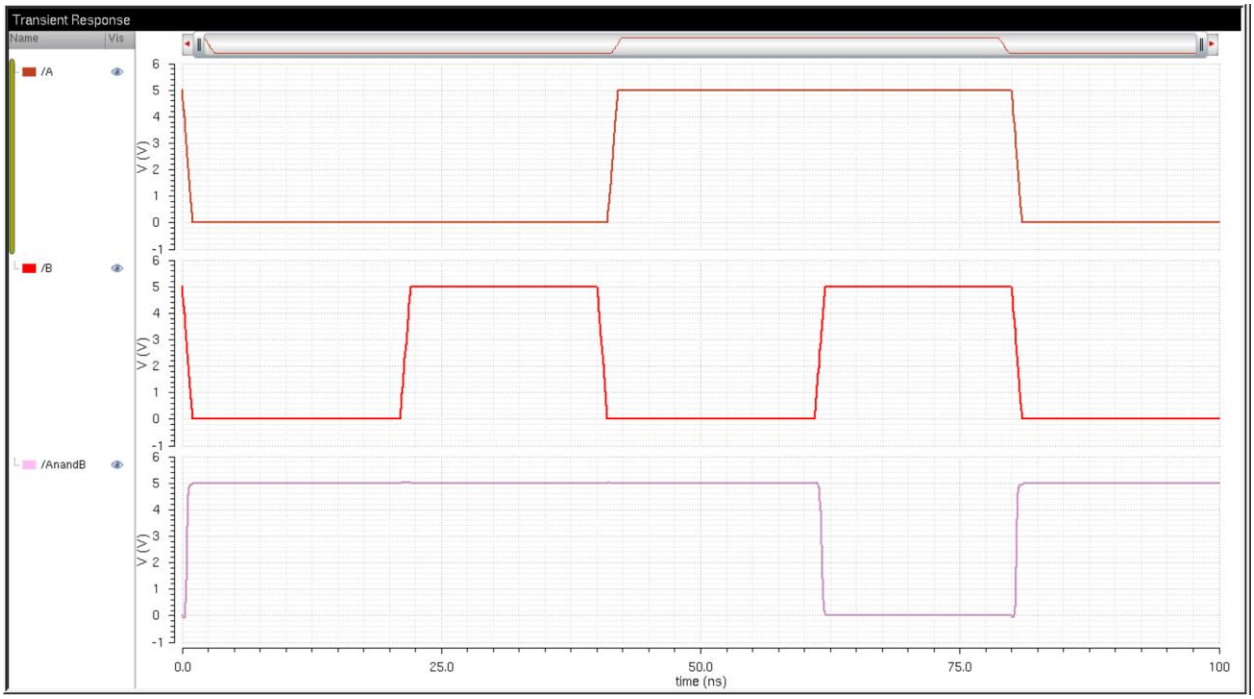
To design a clock generator for this circuit I will use an SR latch. This will allow me to have a nonoverlapping clock to turn the PMOS and NMOS on at different times. This is important because if the PMOS and NMOS is on at the same time the efficiency will be low because we will be shorting the source to ground.

The SR latch will be made using inverters and 2bit NAND gates.

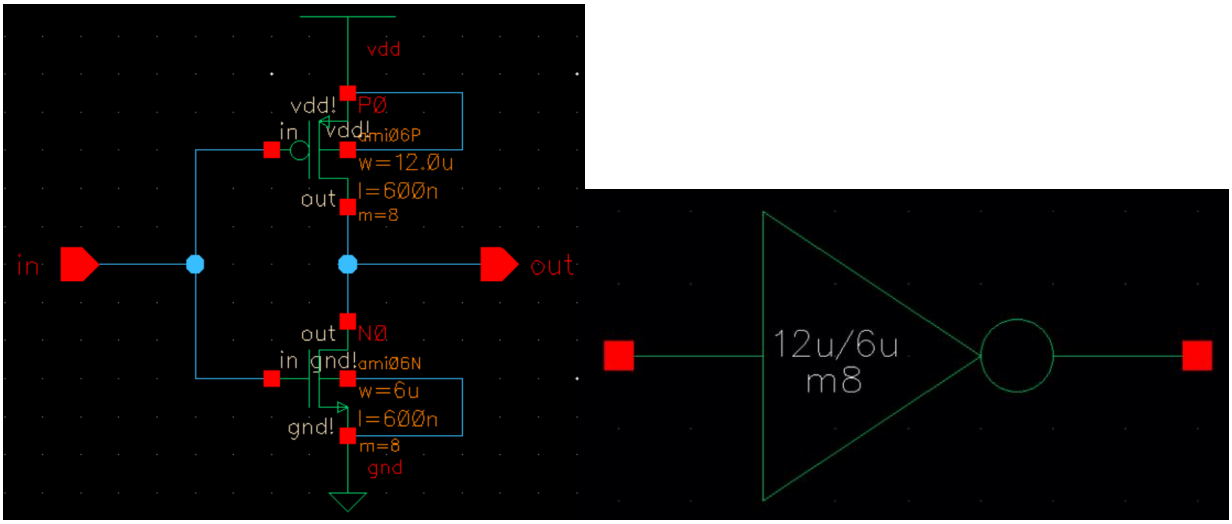
Here is the schematic of my 2bit NAND gate:



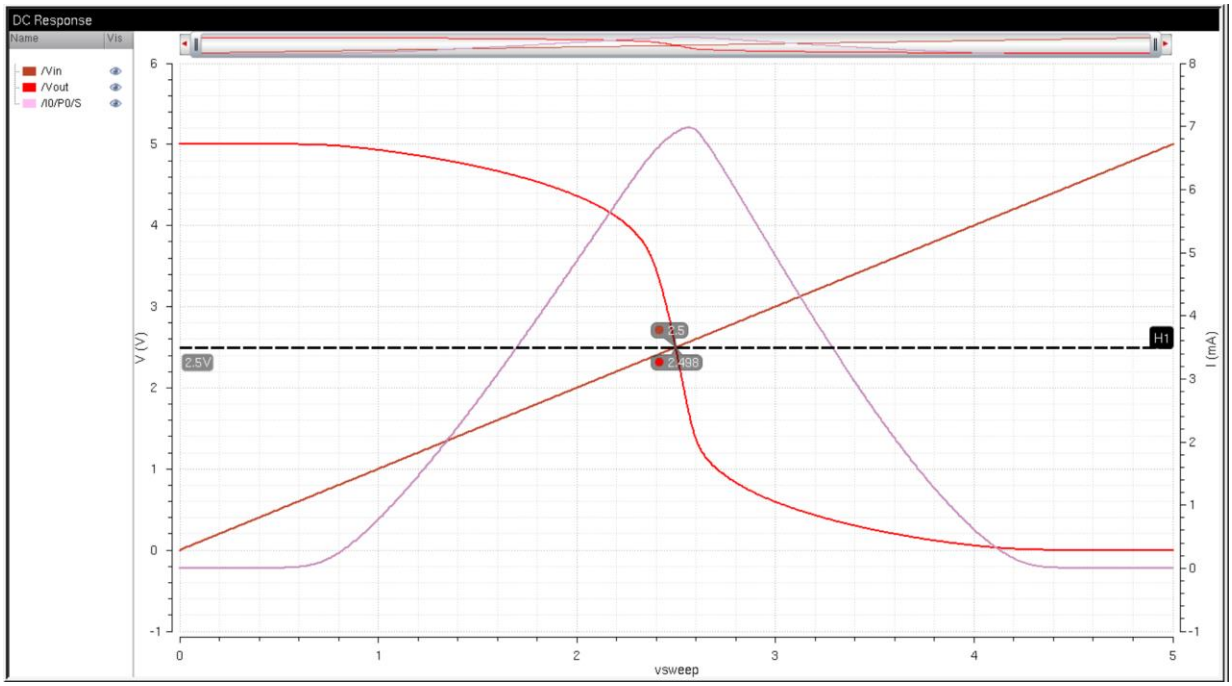
The operation of my NAND gate:



Here is my inverter schematic and symbol:

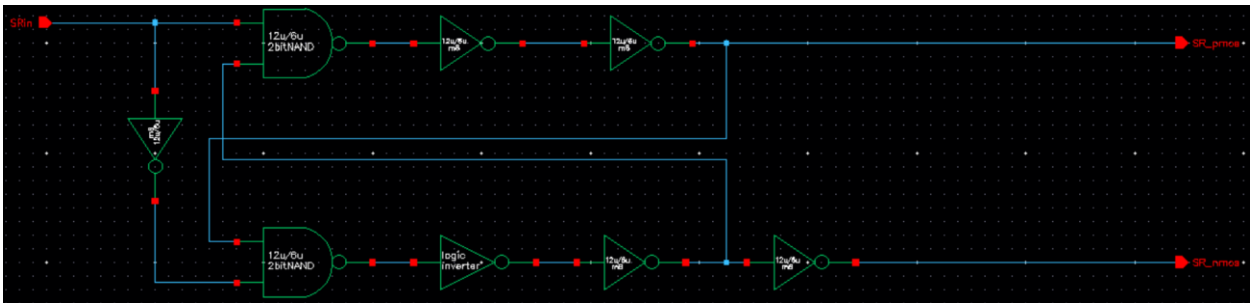


Operation of my inverter:



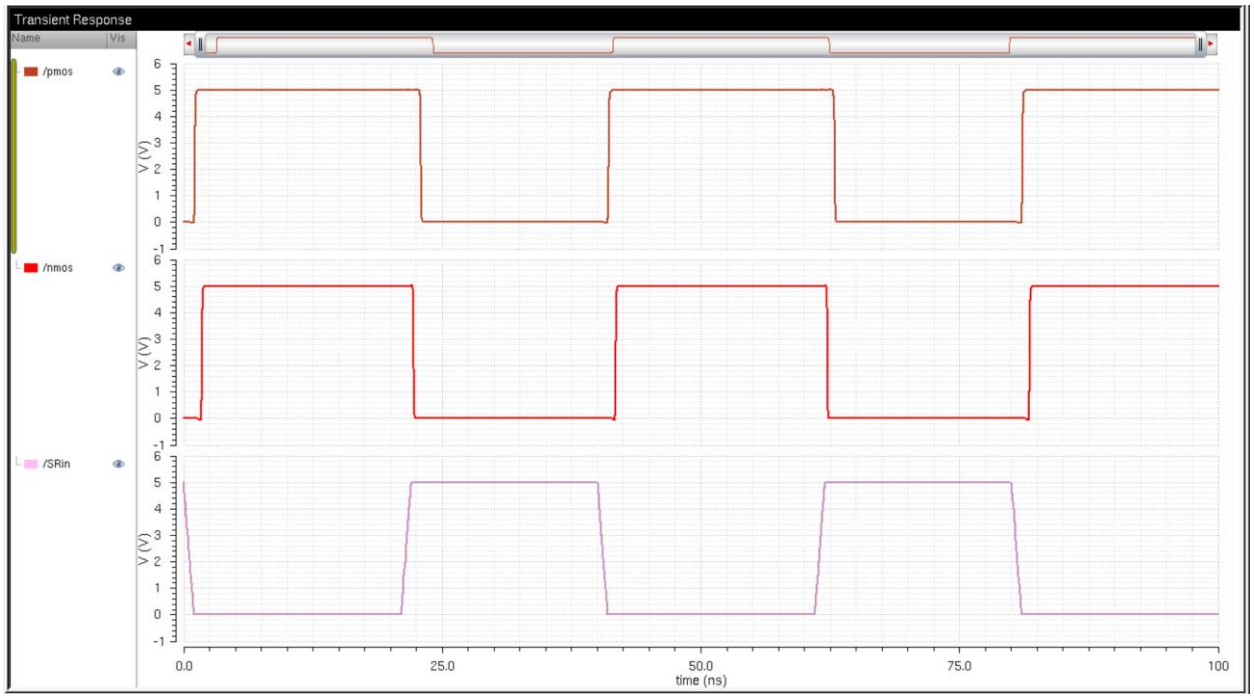
We can see that the switching point of my inverter is at 2.5V. This is because the width of my PMOS is twice the width of my NMOS. We can also see that the only time current will flow is during the change from 5V to 0V.

Here is an image of the SR latch schematic:



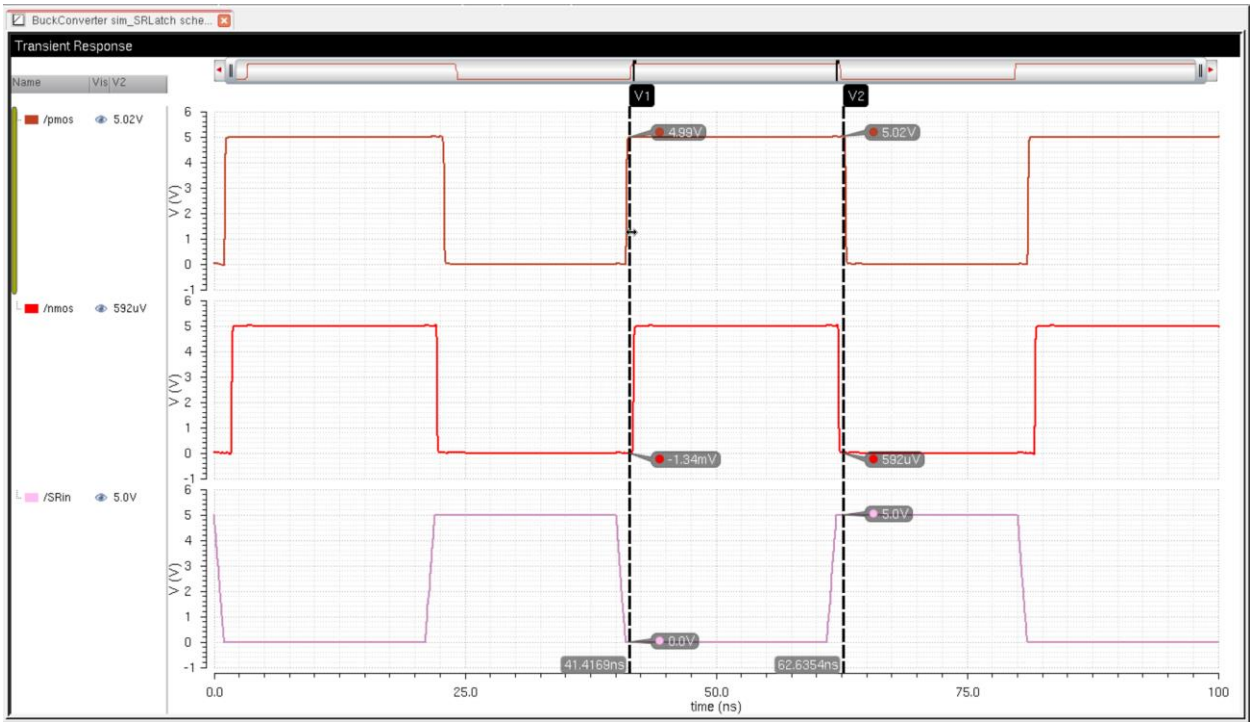
The reason for the inverter multiplier of 8 is to drive the PMOS and NMOS at the output.

Here is a simulation demonstrating the operation of the SR latch:



We can see that both outputs are at the same logic. This is because we want the PMOS and NMOS to be enabled at different times. This is to eliminate cross-over current and improve efficiency.

Here is an image of the simulation showing that the signals are nonoverlapping:

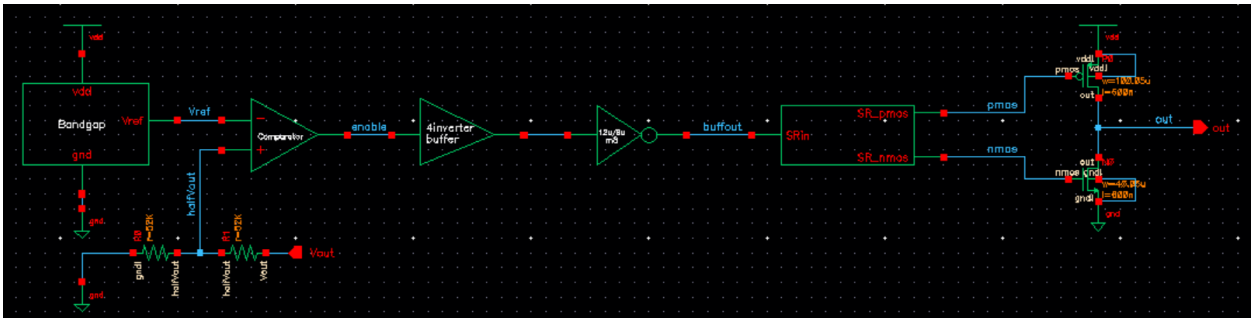


We can see that the PMOS turns off before the NMOS turns on. This helps improve the efficiency of the circuit since we won't be shorting the source to ground. This is accomplished by having a big enough time delay from the NAND gates and the inverters.

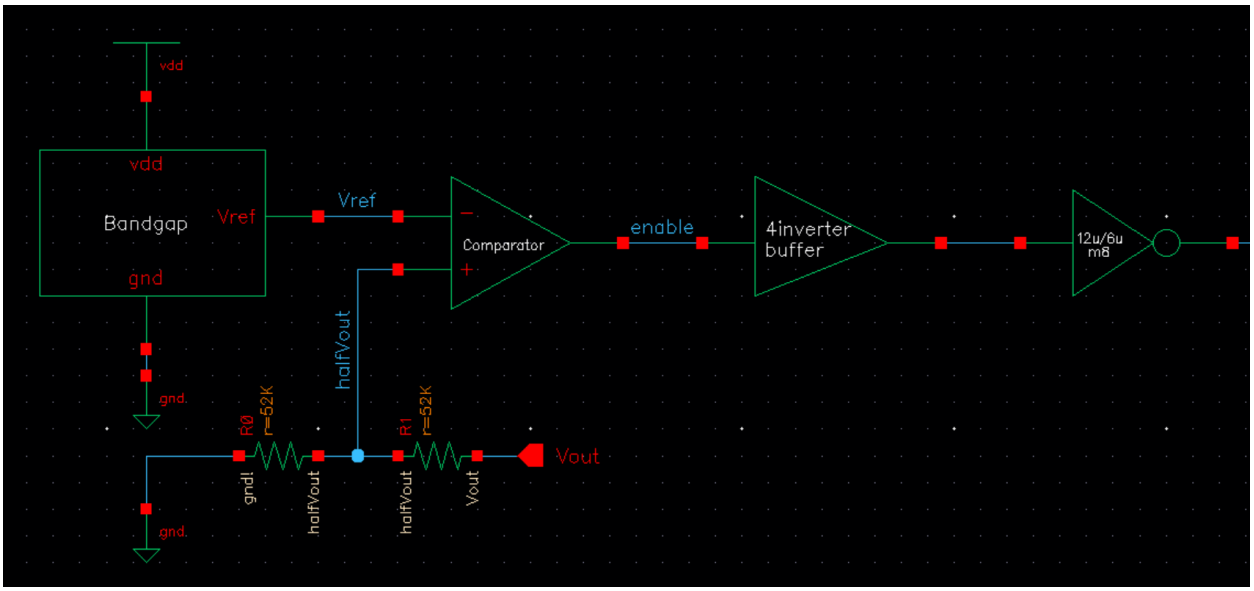
CMOS Synchronous Buck Switching Power Supply

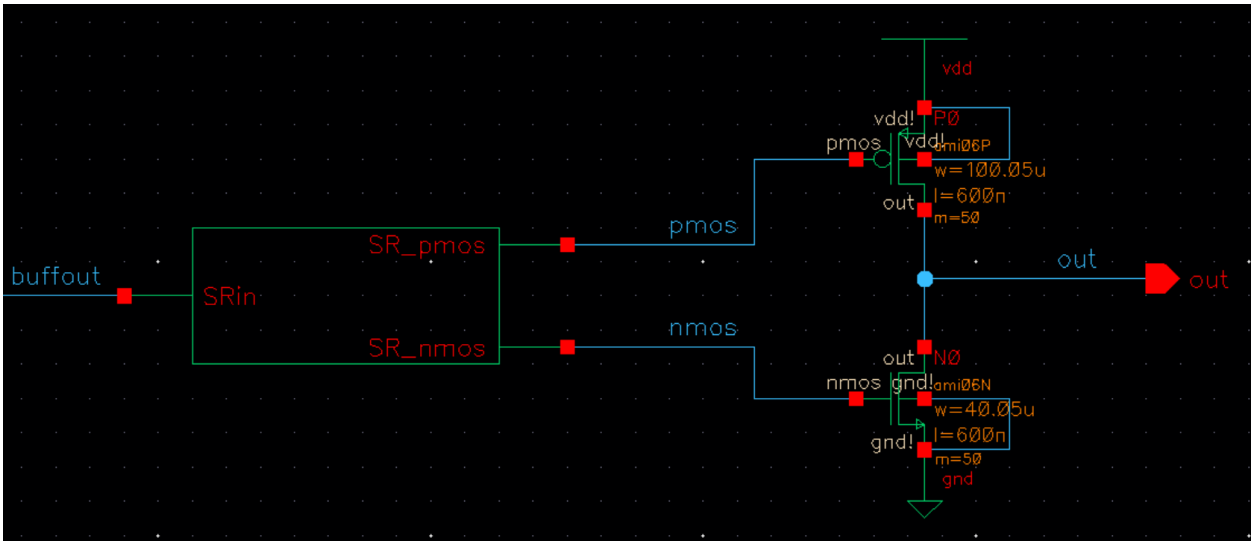
The synchronous switching power supply is driven by a PMOS and an NMOS. This allows the output to be pulled up or down by switching on the PMOS or the NMOS. The size of the PMOS and NMOS will be very large to drive the output capacitance. The output voltage will be obtained by having an inductor and a capacitor form a low pass filter which will pass a voltage depending on the VDD and the duty cycle.

Here is an image of the entire schematic:

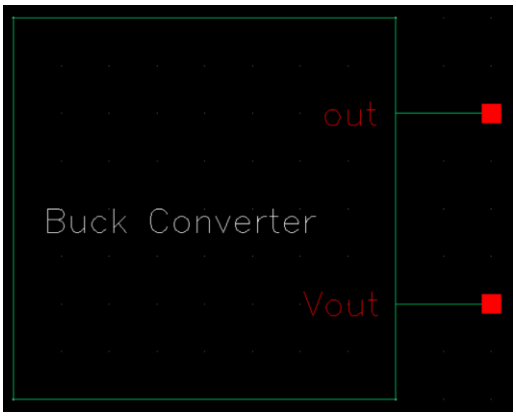


Here are zoomed in pictures of my schematic:

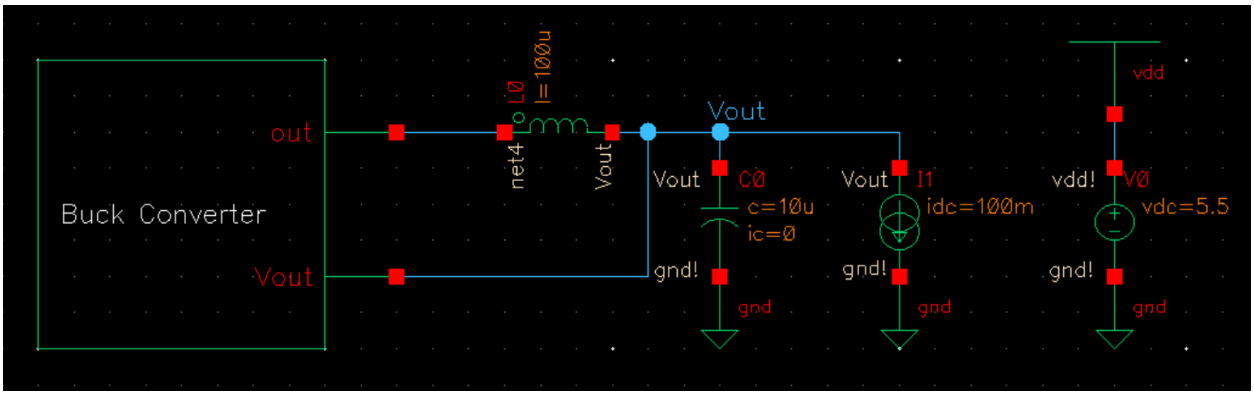




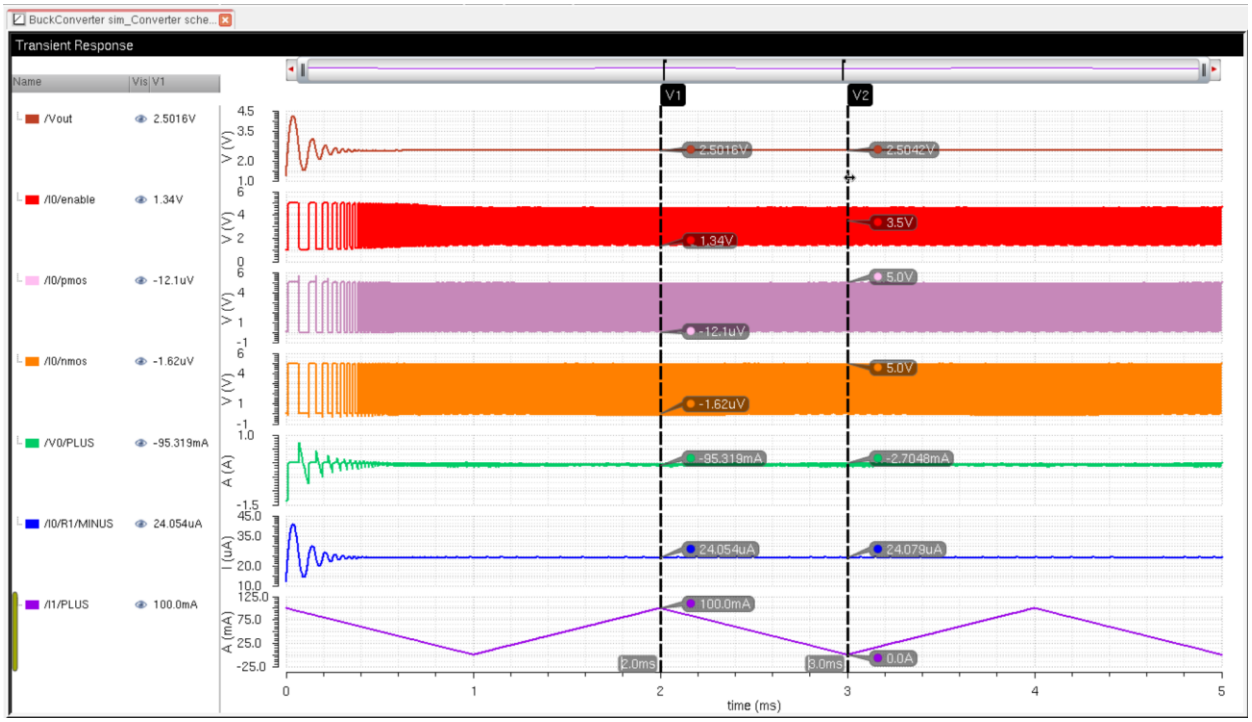
The symbol used for simulation:



Circuit used to perform simulations:



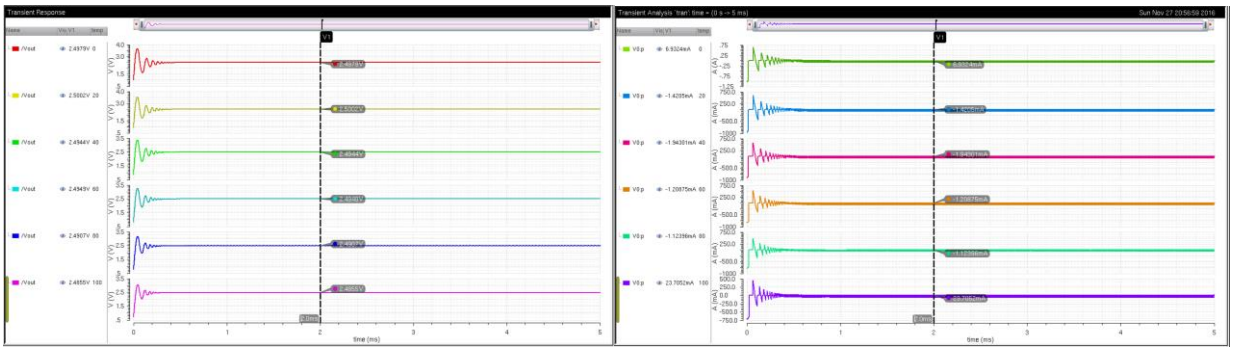
Simulation of the power supply using a pulsed current source to simulate a load:



The output voltage is at a 2.5V with very small oscillations around 2.50X. These oscillations are from the comparator turning the PMOS and NMOS on and off. Although the current is changing the output voltage stays a constant 2.5V.

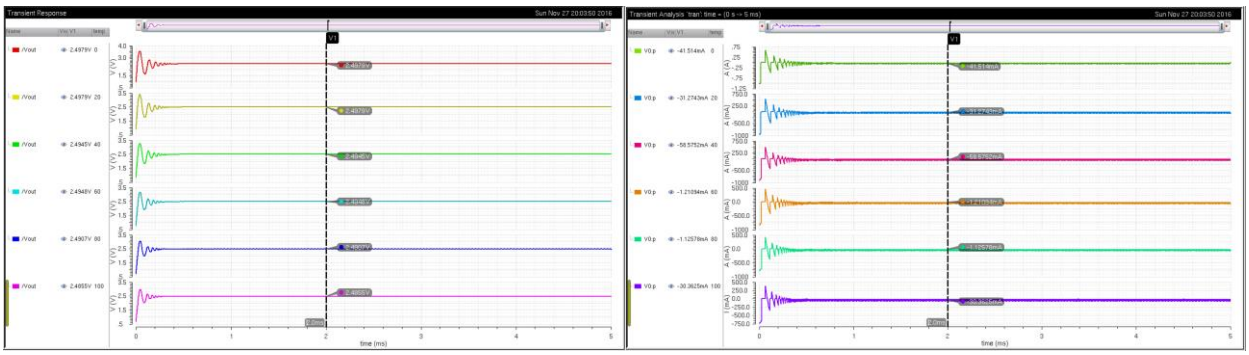
Now I will run simulations varying my VDD, load current, and temperature and calculate the efficiency of the circuit at these points:

VDD = 4V and Iload = 1mA



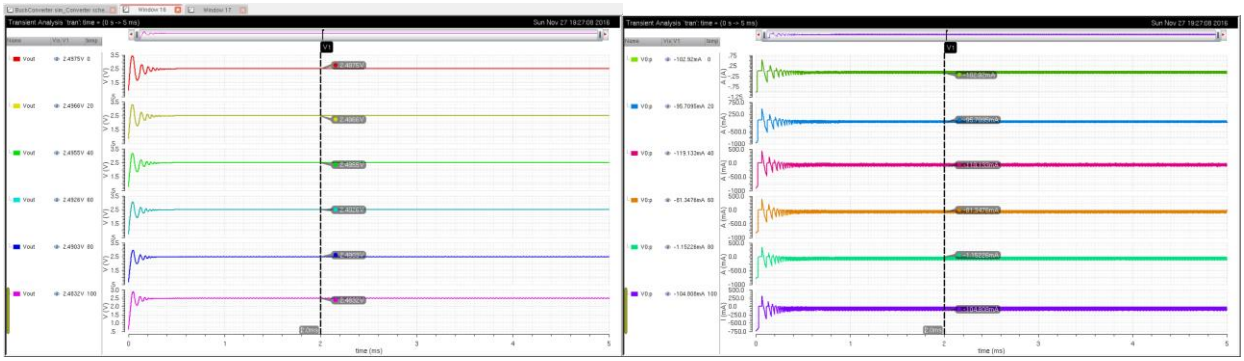
Vdd V	Load Current mA	Average Source Current mA	Temp C	Efficiency %
4	1	5.377	0	11.62358192
4	1	5.394	20	11.58694846
4	1	5.41	40	11.55268022
4	1	5.416	60	11.53988183
4	1	5.436	80	11.49742458
4	1	5.445	100	11.47842057

VDD = 4V and Iload = 50mA



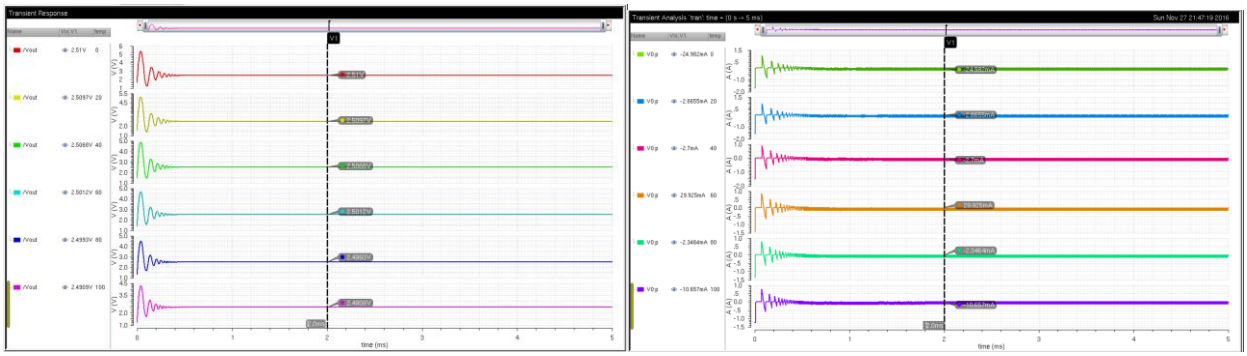
Vdd V	Load Current mA	Average Source Current mA	Temp C	Efficiency %
4	50	36.92	0	84.64247021
4	50	37.03	20	84.3910343
4	50	37.12	40	84.18642241
4	50	37.22	60	83.96023643
4	50	37.28	80	83.8251073
4	50	37.37	100	83.62322719

VDD = 4V and Iload = 100mA



Vdd V	Load Current mA	Average Source Current mA	Temp C	Efficiency %
4	100	71.2	0	87.78089888
4	100	71.53	20	87.37592618
4	100	71.87	40	86.96257131
4	100	72.21	60	86.55310899
4	100	72.54	80	86.15936035
4	100	72.89	100	85.74564412

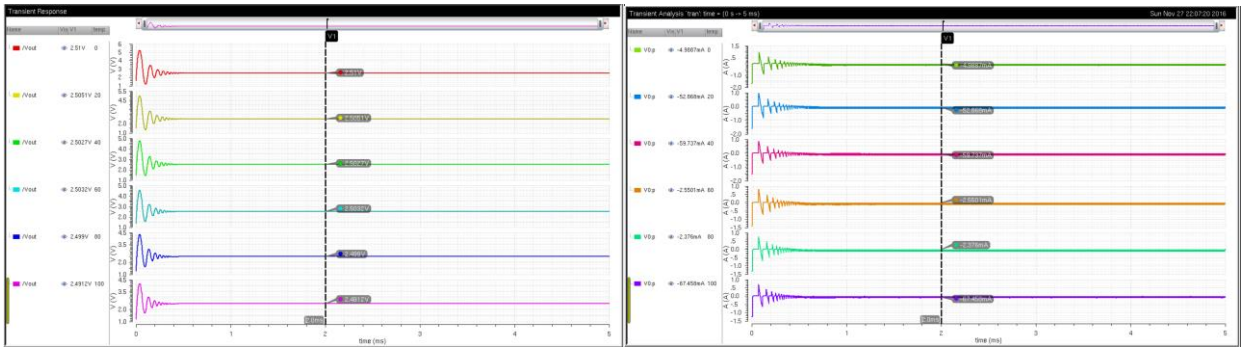
VDD = 5.5V and Iload = 1mA



Vdd V	Load Current mA	Average Source Current mA	Temp C	Efficiency %
5.5	1	5.742	0	7.916152117
5.5	1	5.715	20	7.953551261
5.5	1	5.688	40	7.99130546
5.5	1	5.665	60	8.023750301
5.5	1	5.643	80	8.055031978
5.5	1	5.623	100	8.083682279

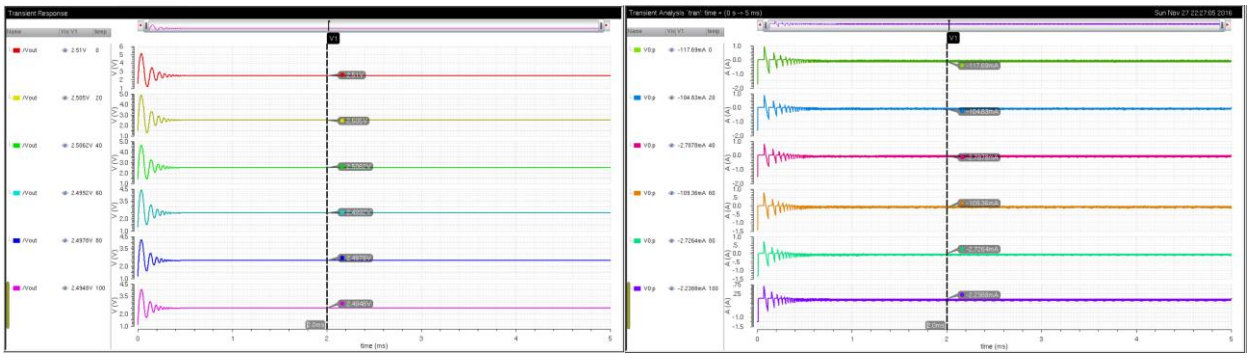
With low load currents my efficiency is drastically reduced. This is expected because the highest efficiency is expected at maximum load current. My lowest efficiency is at minimum load current and maximum VDD.

VDD = 5.5V and Iload = 50mA

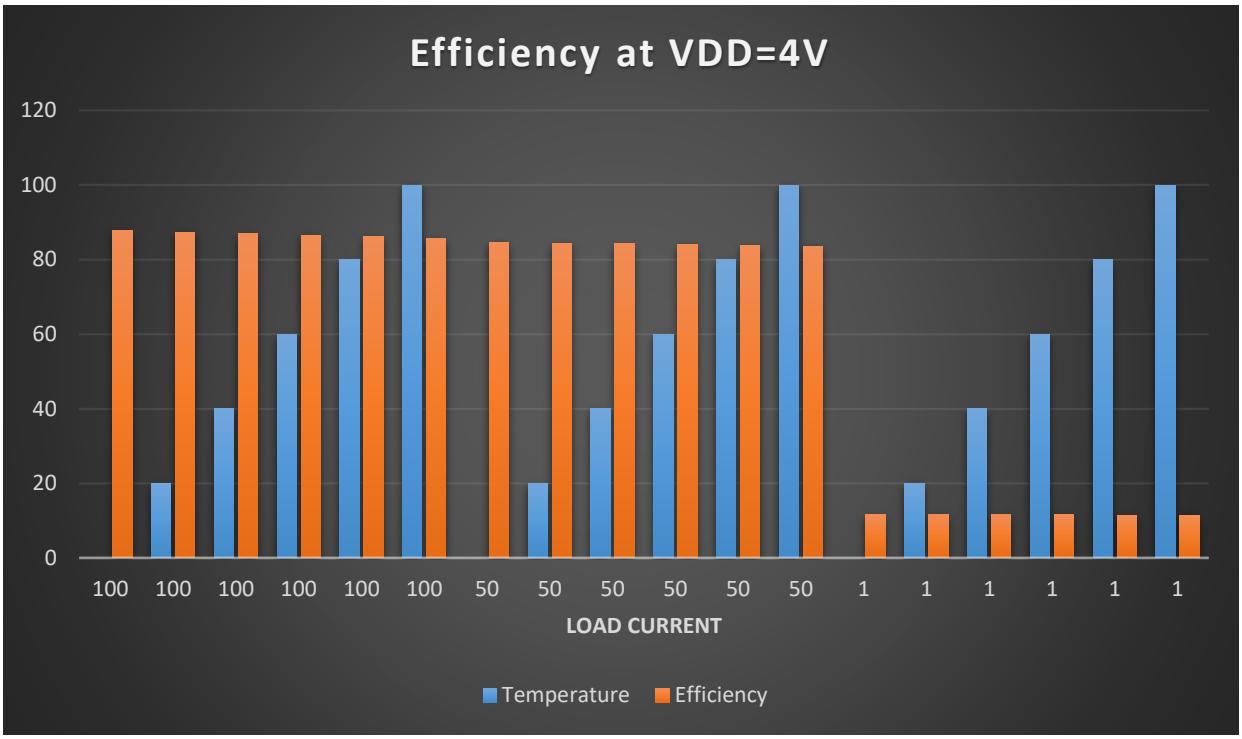


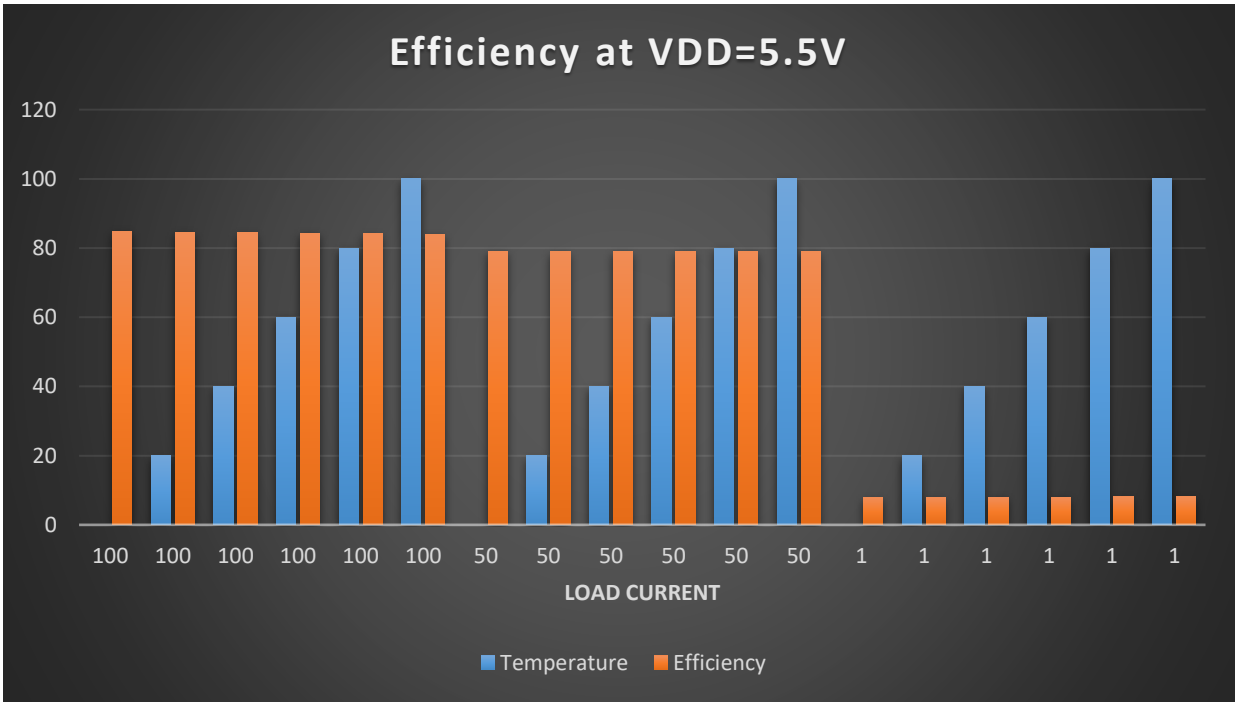
Vdd V	Load Current mA	Average Source Current mA	Temp C	Efficiency %
5.5	50	28.74	0	79.0788891
5.5	50	28.75	20	79.0513834
5.5	50	28.75	40	79.0513834
5.5	50	28.75	60	79.0513834
5.5	50	28.75	80	79.0513834
5.5	50	28.75	100	79.0513834

VDD = 5.5V and Iload = 100mA



Vdd V	Load Current mA	Average Source Current mA	Temp C	Efficiency %
5.5	100	53.6	0	84.80325645
5.5	100	53.72	20	84.61382251
5.5	100	53.81	40	84.47230153
5.5	100	53.92	60	84.29997302
5.5	100	54.02	80	84.14391976
5.5	100	54.14	100	83.9574168





To calculate the efficiency in these tables I used the equation:

$$\varepsilon = \frac{V_{out} * I_{load}}{VDD * I_{source_{avg}}}$$

Design Equations:

$$VDD * D = V_{out}$$

$$\frac{VDD - V_{out}}{L} = \frac{I_{MAX} - I_{MIN}}{D * T}$$

$$\frac{0 - V_{out}}{L} = \frac{I_{MAX} - I_{MIN}}{(1 - D) * T}$$

$$I_{AVG} = \frac{I_{MAX} + I_{MIN}}{2}$$

I will arbitrarily choose a frequency to use these equations.

Project Design Specifications

VDD	Vary from 4V to 5.5V
I_{Load}	Vary from 0mA to 100mA
Vout	2.5V
Frequency	100K Hz to 1M Hz

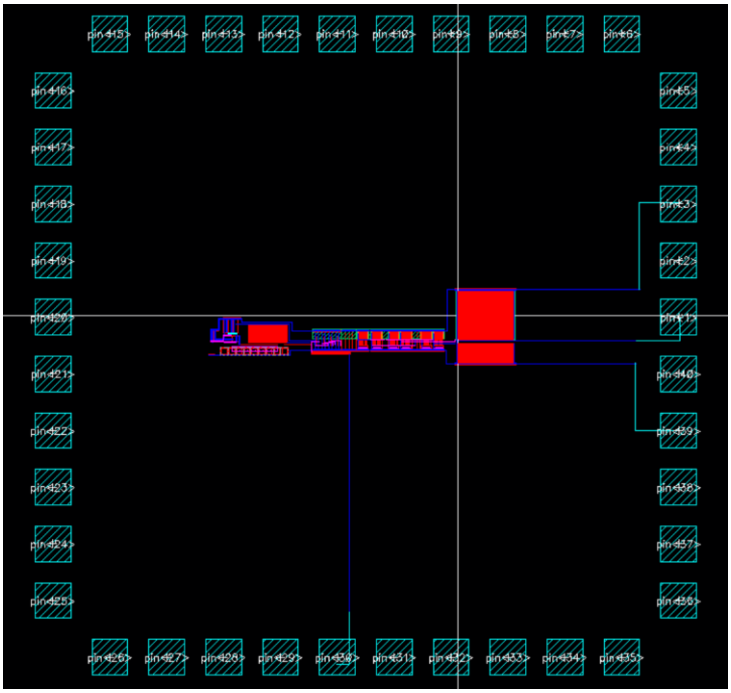
$$L = \frac{(VDD - V_{out})DT}{I_{MAX} - I_{MIN}} = \frac{(5.5 - 2.5)(0.5)\left(\frac{1}{1M}\right)}{20m} = 75uH$$

Although my calculated inductor value is 75uH I found that using a 100uH inductor with a 10uF capacitor gave me the best efficiency.

PMOS W/L/M	100.05u/0.6u/50
NMOS W/L/M	40.05u/0.6u/50

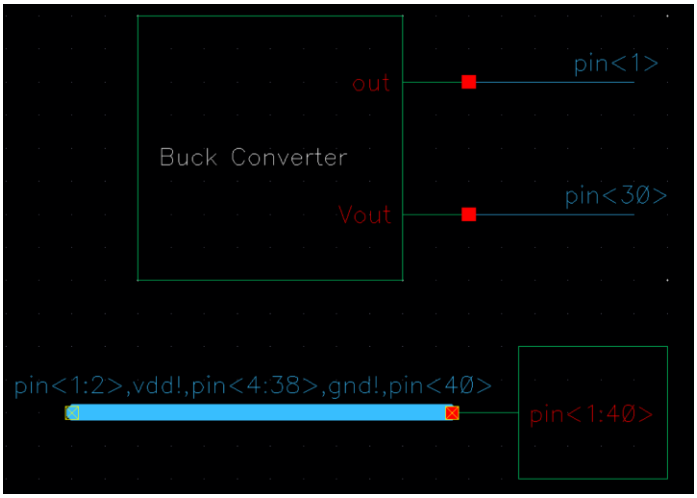
These values for my PMOS and NMOS were arbitrarily chosen and tuned to increase my efficiency and output voltage under different load currents. I found that by having my PMOS sized too wide I would get more ringing with a higher amplitude at the start of my simulations. When my NMOS was too wide I would get very little ringing at the start but my average source current increases.

Pin diagram for fabrication:



Vdd!	Pin<3>
Gnd!	Pin<39>
Out	Pin<1>
Vout	Pin<30>

Concise Schematic:



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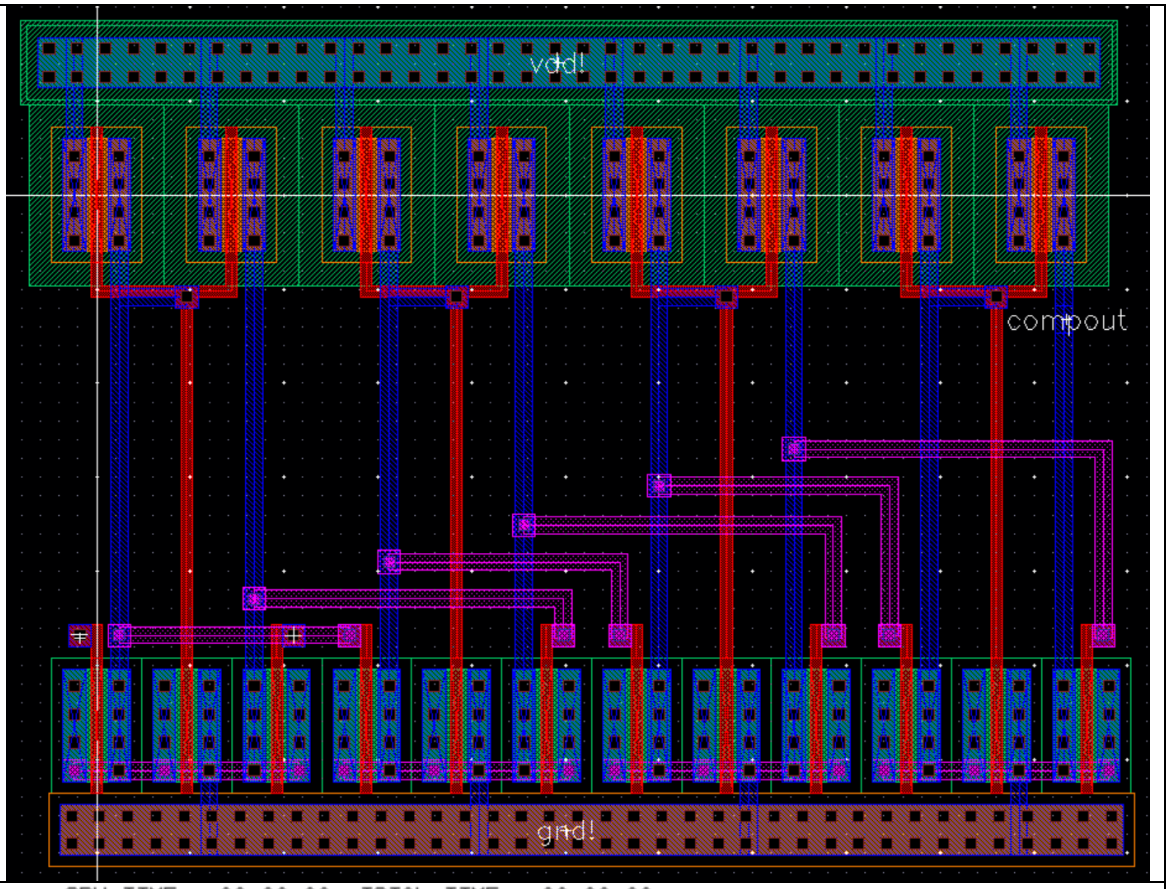
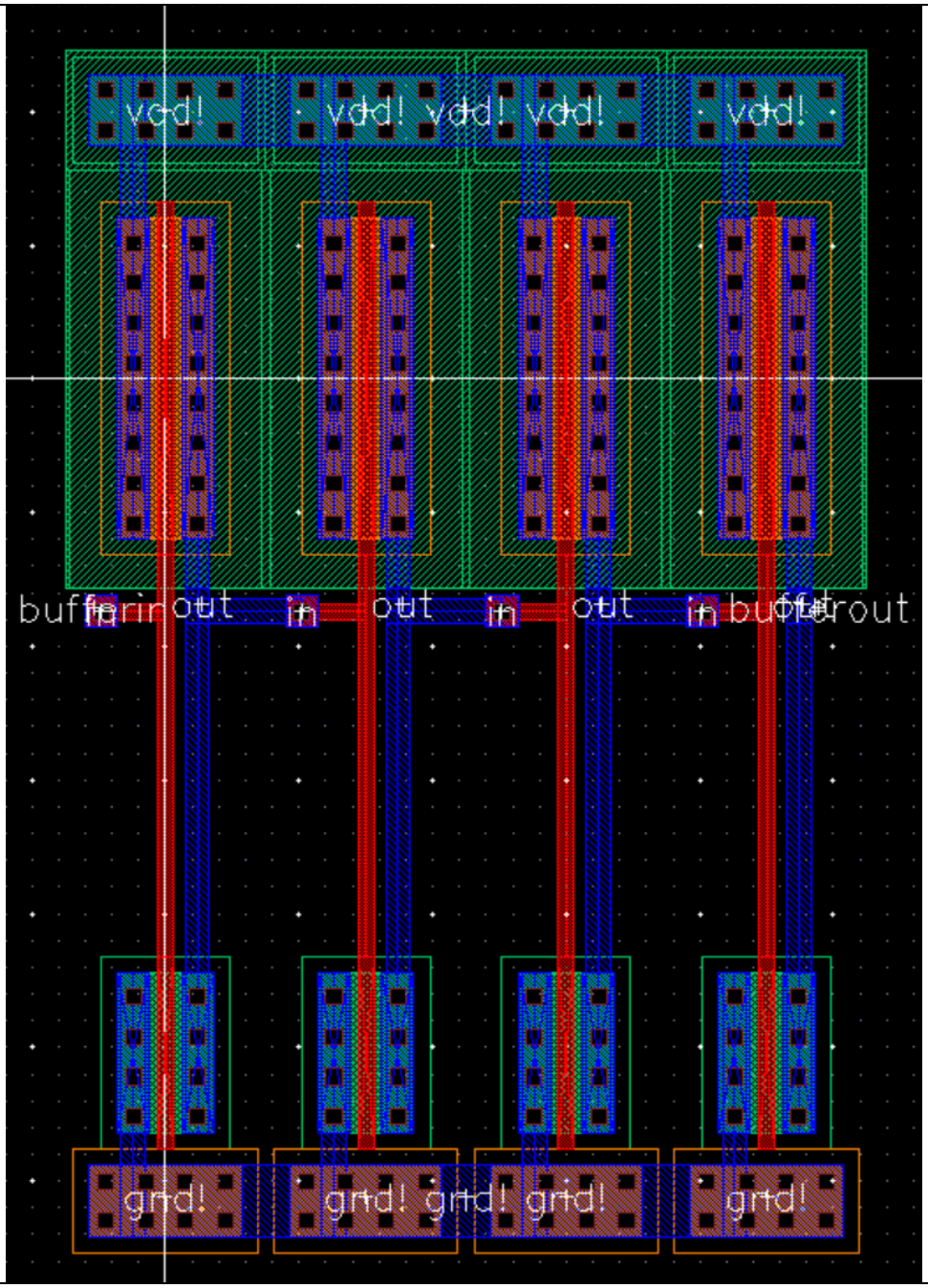
LVS:

Layouts

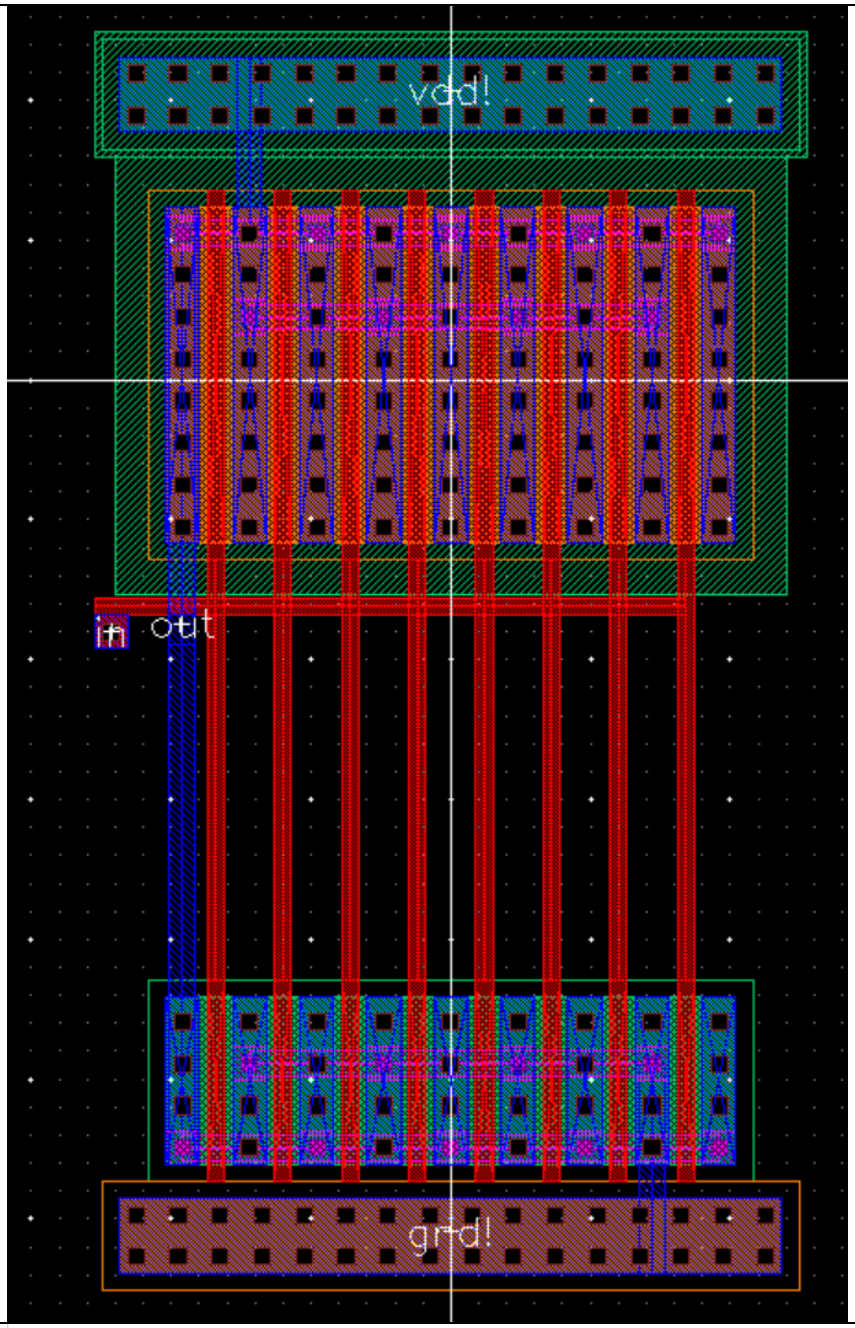
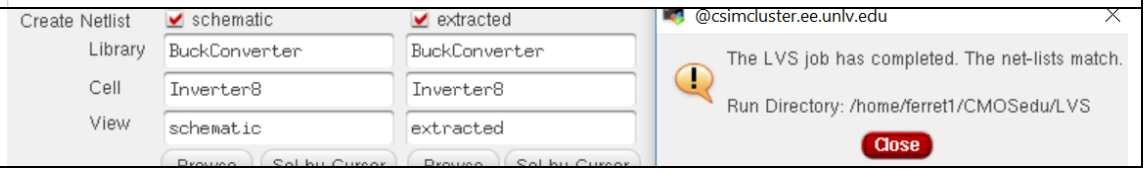
Comparator:

Layout	
DRC	CPU TIME = 00:00:00 TOTAL TIME = 00:00:00 ********* Summary of rule violations for cell "Comparator layout" ********* Total errors found: 0
LVS	

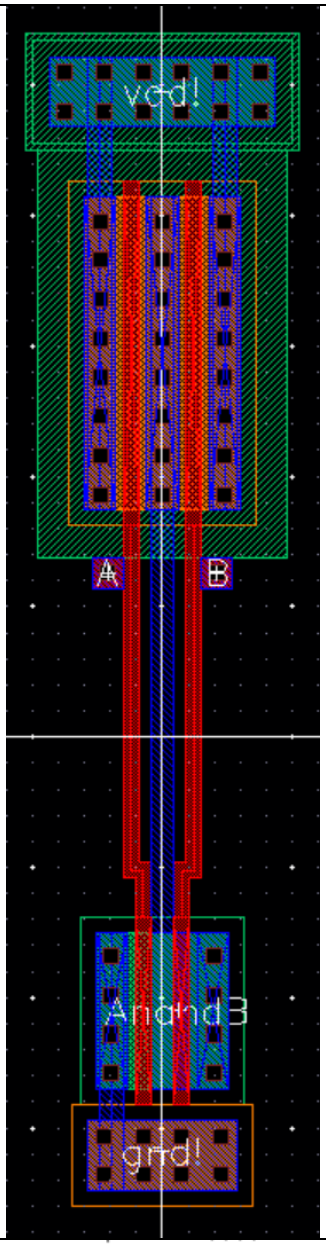
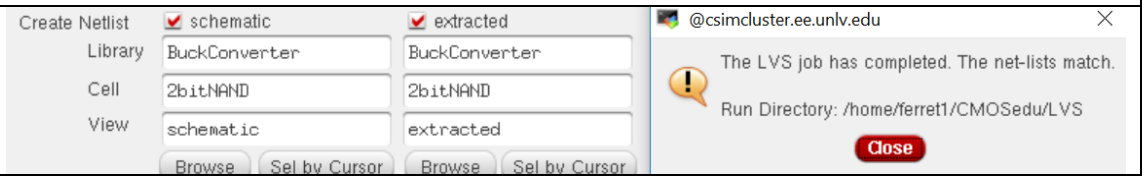
Buffer:

Layout	
DRC	********** Summary of rule violations for cell "Buffer layout" ********** Total errors found: 0
LVS	

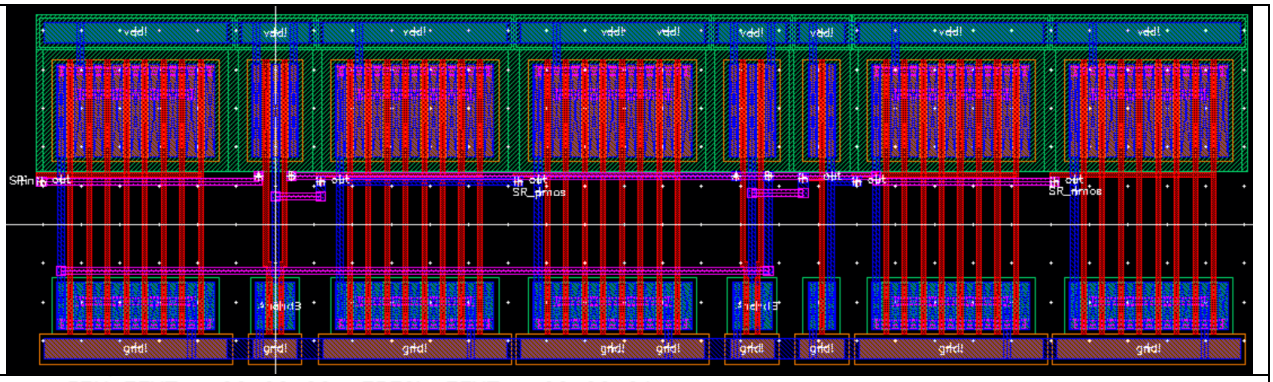
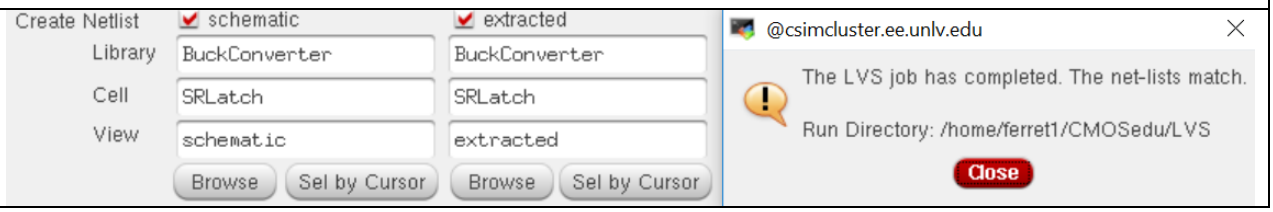
Inverter x8:

Layout	
DRC	********** Summary of rule violations for cell "Inverter8 layout" ********** Total errors found: 0
LVS	

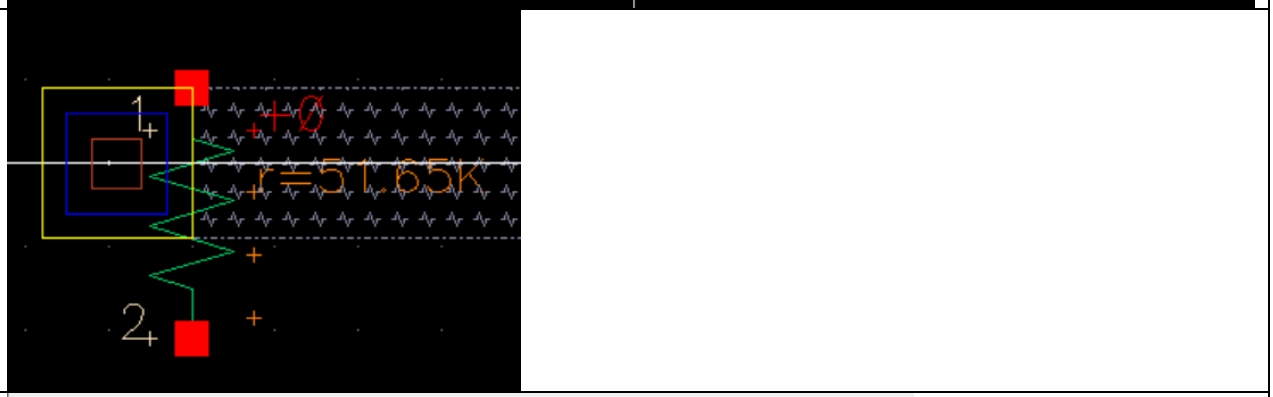
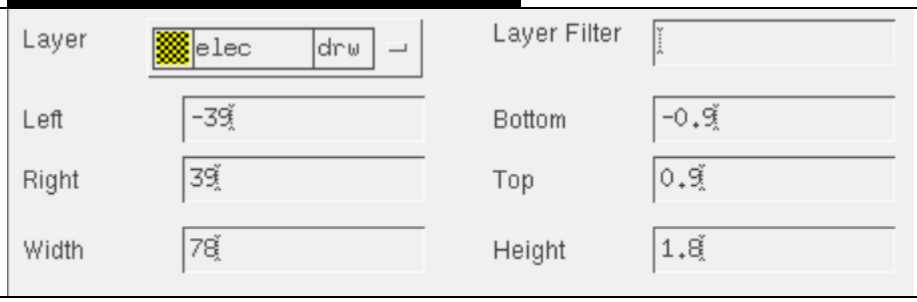
2bit NAND Gate:

Layout	
DRC	CPU TIME = 00:00:00 TOTAL TIME = 00:00:00 ********** Summary of rule violations for cell "2bitNAND layout" ********** Total errors found: 0
LVS	

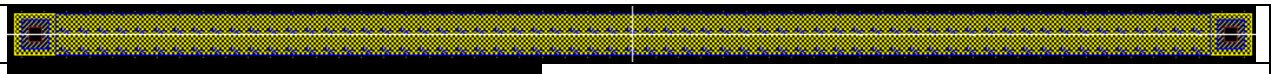
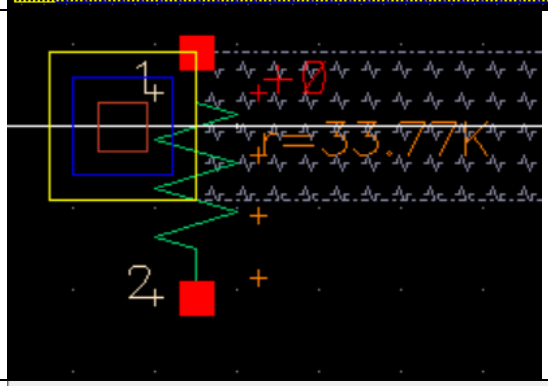
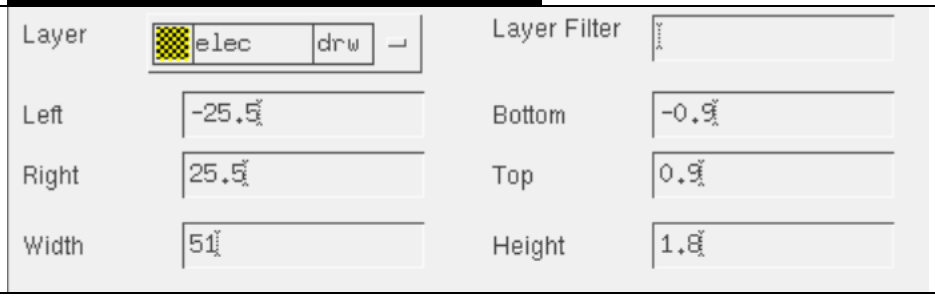
SR Latch:

Layout	
DRC	CPU TIME = 00:00:00 TOTAL TIME = 00:00:01 ********* Summary of rule violations for cell "SRLatch layout" ********* Total errors found: 0
LVS	

52K Resistor:

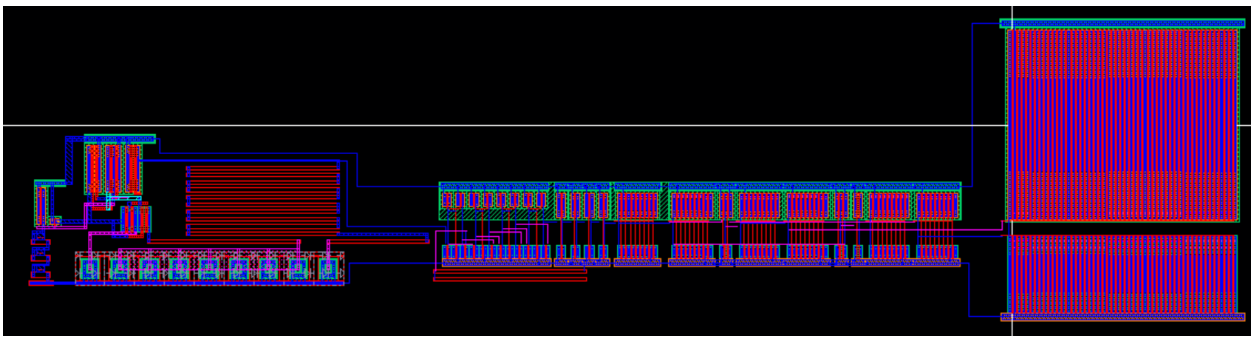
Layout	
Extracted	
Specs	

34K Resistor:

Layout	
Extracted	
Specs	

Sheet Resistance of hiRes poly	$\frac{1192\Omega}{square}$
52K Resistor W = 1.8u	$\frac{52K}{1192} * 1.8u = l = 78u$
34K Resistor W = 1.8u	$\frac{34K}{1192} * 1.8u = l = 51u$

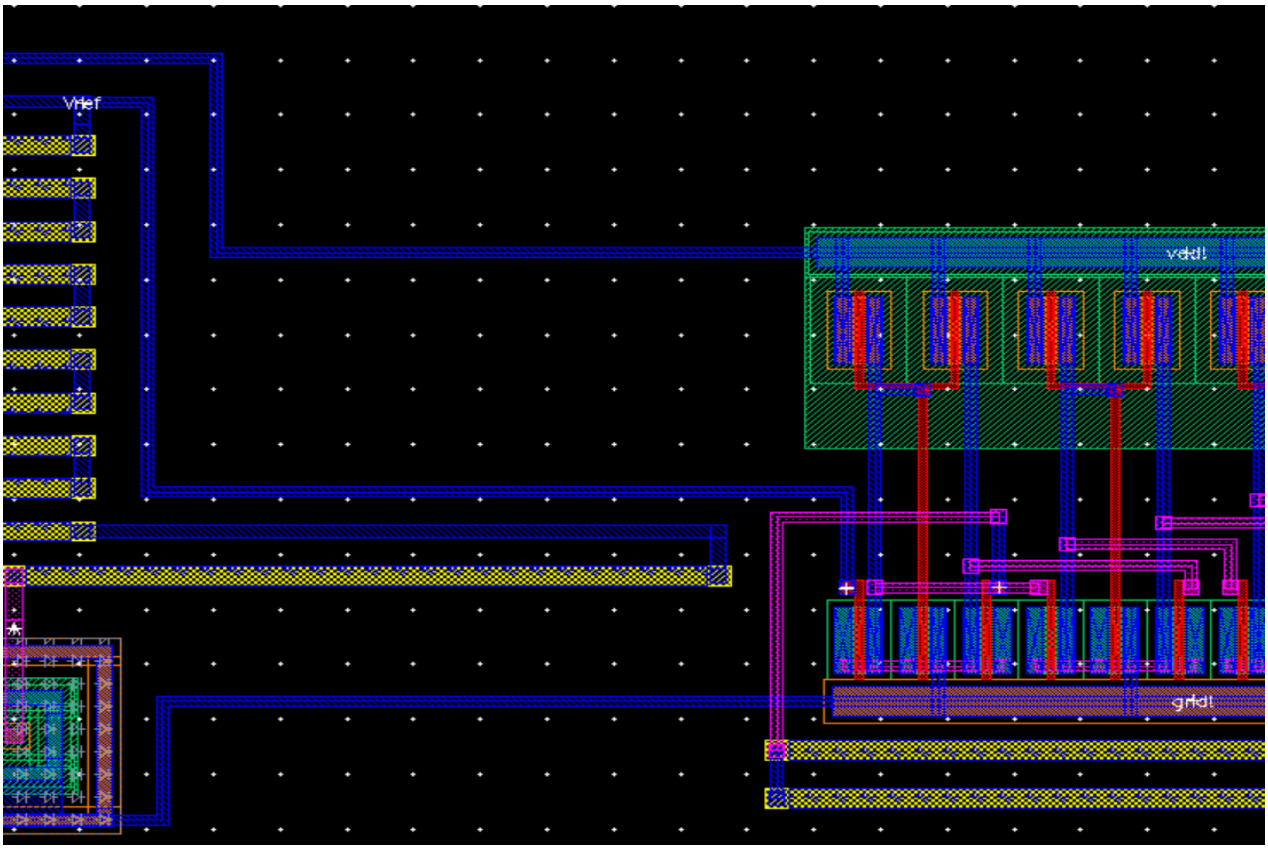
Layout of entire circuit:



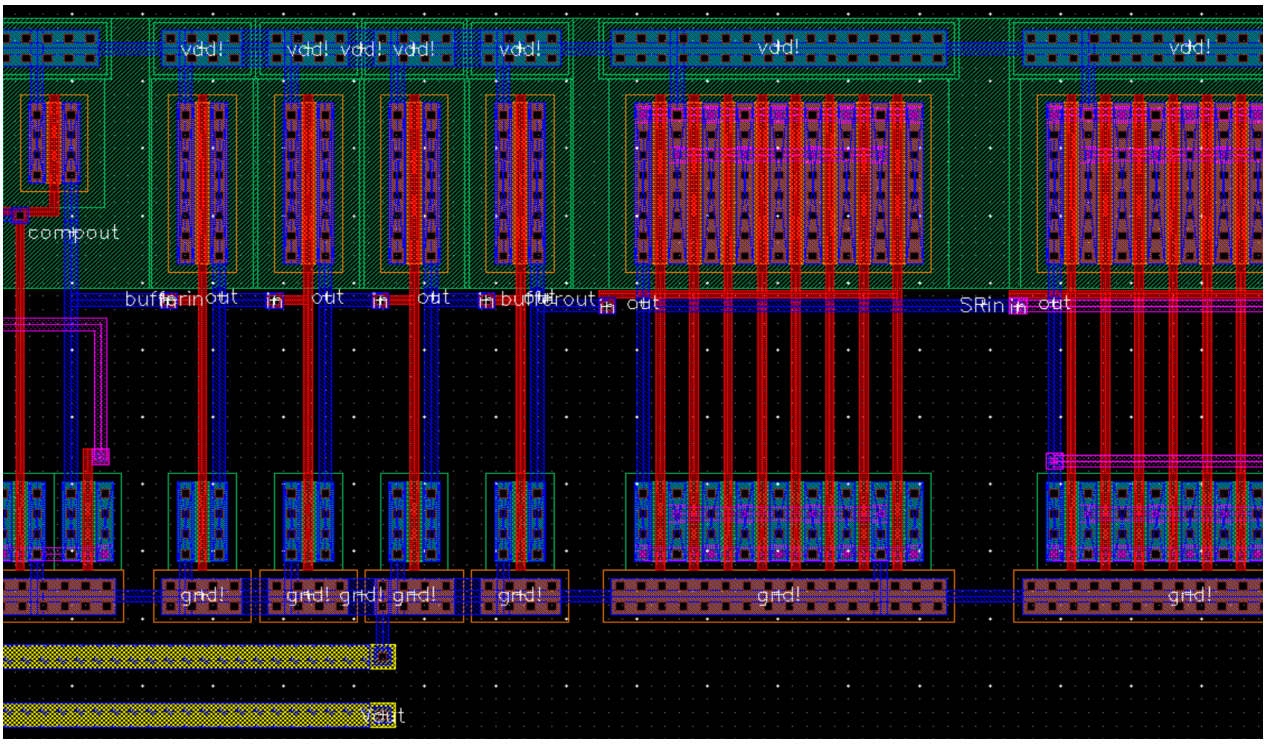
I did the layout in this fashion to understand and read the layout easier. I could have made it more compact but more difficult to understand.

Below will be zoomed in images of the connections from component to component in the layout.

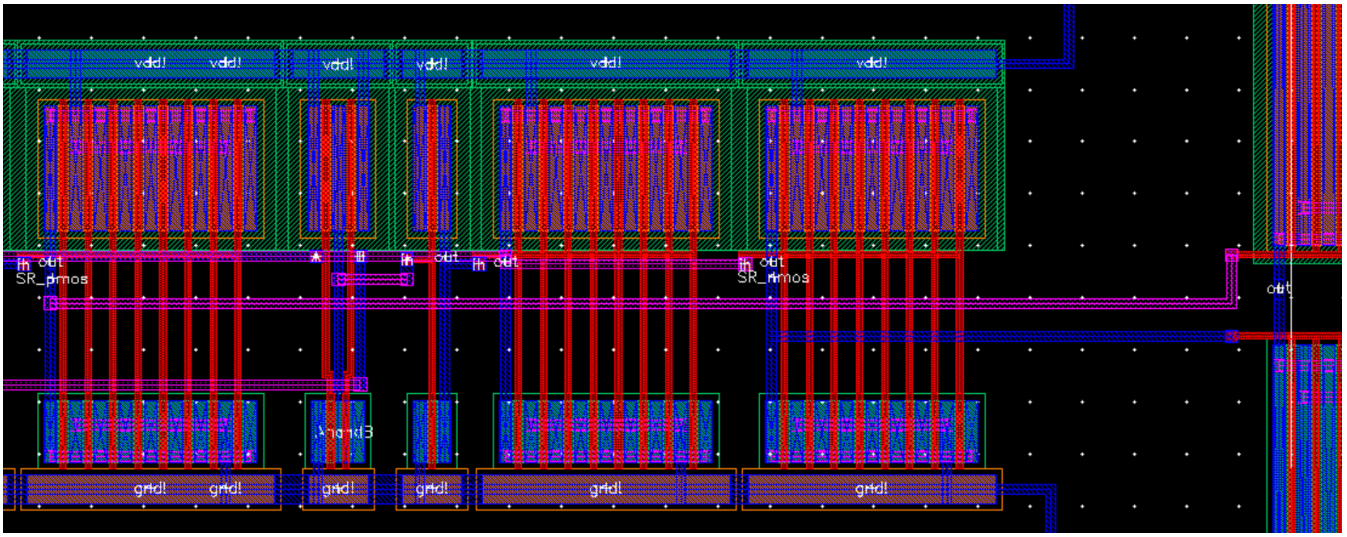
Bandgap to Comparator:



Comparator to SR Latch:



SR Latch to PMOS and NMOS:



DRC:

```
*********   Summary of rule violations for cell "Converter layout"   *********
   Total errors found: 0
```

LVS:

LVS and DRC instructions for my converter:

Cell name: Converter

Rules Library: NCSU_TechLib_ami06

> When performing verification on a different computer the rules library won't work. This needs to be changed to NCSU_TechLib_ami06. My library properties appear to have the tech library already attached but won't use the verification rules unless the rules library is changed to NCSU_TechLib_ami06.