Analog Front-End for C5 APDs

Tyler Ferreira

ECG 720

Final Project

The objective of this project is to design an analog front-end for converting current from an APD into an output voltage.

My design should be able to satisfy the following requirements:

- Total gain: First Stage – 30 $k\Omega$ and Second Stage – $10 - 20x\ V/V$
- Study of the need for inclusion of a 2nd stage
- TIA Bandwidth minimum of 250 MHz
- Input referred noise: $< 5\ pA/\sqrt{Hz}$ but preferably 1.5 $pA/\sqrt{Hz}$
- 1.5 – 2 V output swing
- 3.3 or 5 V power supply operation with less than 5 mA current consumption
- Amplifier output signal is designed to drive high impedance loads (use 1 pF)
- Slew – rate with maximum load $> 100\ V/\mu s = 100\ mV/ns$

I will use the following models for my LTspice simulations:

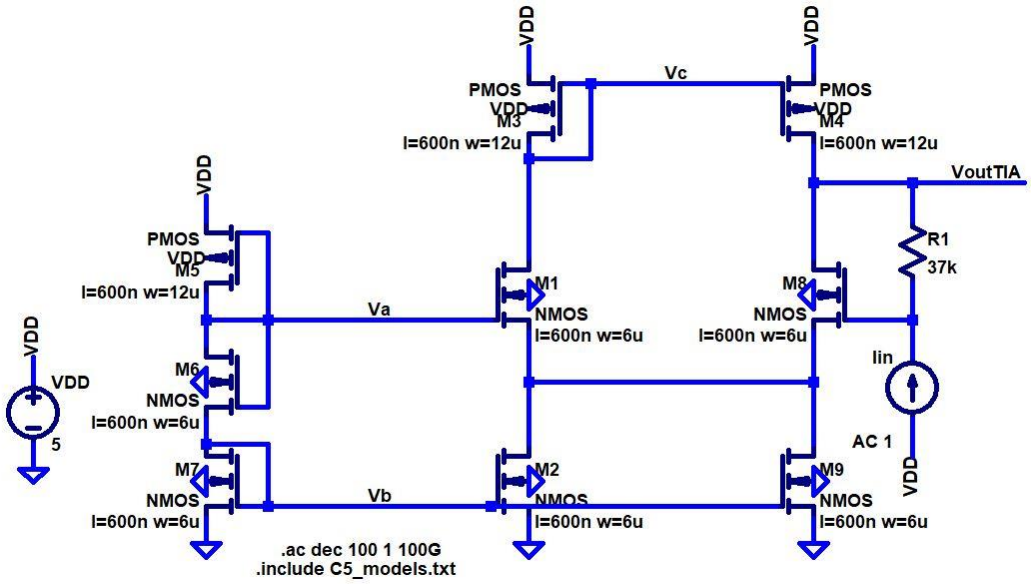
NMOS

```
.MODEL NMOS NMOS (                                  LEVEL   = 8
+VERSION = 3.1          TNOM    = 27                TOX     = 1.39E-8
+XJ      = 1.5E-7       NCH     = 1.7E17            VTH0    = 0.6696061
+K1      = 0.8351612    K2      = -0.0839158        K3      = 23.1023856
+K3B     = -7.6841108   W0      = 1E-8              NLX     = 1E-9
+DVT0W   = 0            DVT1W   = 0                 DVT2W   = 0
+DVT0    = 2.9047241    DVT1    = 0.4302695         DVT2    = -0.134857
+U0      = 458.439679   UA      = 1E-13             UB      = 1.485499E-18
+UC      = 1.629939E-11 VSAT    = 1.643993E5        A0      = 0.6103537
+AGS     = 0.1194608    B0      = 2.674756E-6       B1      = 5E-6
+KETA    = -2.640681E-3 A1      = 8.219585E-5       A2      = 0.3564792
+RDSW    = 1.387108E3   PRWG    = 0.0299916         PRWB    = 0.0363981
+WR      = 1            WINT    = 2.472348E-7       LINT    = 3.597605E-8
+XL      = 0            XW      = 0                 DWG     = -1.287163E-8
+DWB     = 5.306586E-8  VOFF    = 0                 NFACTOR = 0.8365585
+CIT     = 0            CDSC    = 2.4E-4            CDSCD   = 0
+CDSCB   = 0            ETA0    = 0.0246738         ETAB    = -1.406123E-3
+DSUB    = 0.2543458    PCLM    = 2.5945188         PDIBLC1 = -0.4282336
+PDIBLC2 = 2.311743E-3  PDIBLCB = -0.0272914        DROUT   = 0.7283566
+PSCBE1  = 5.598623E8   PSCBE2  = 5.461645E-5       PVAG    = 0
+DELTA   = 0.01         RSH     = 81.8              MOBMOD  = 1
+PRT     = 8.621        UTE     = -1                KT1     = -0.2501
+KT1L    = -2.58E-9     KT2     = 0                 UA1     = 5.4E-10
+UB1     = -4.8E-19     UC1     = -7.5E-11          AT      = 1E5
+WL      = 0            WLN     = 1                 WW      = 0
+WWN     = 1            WWL     = 0                 LL      = 0
+LLN     = 1            LW      = 0                 LWN     = 1
+LWL     = 0            CAPMOD  = 2                 XPART   = 0.5
+CGDO    = 2E-10        CGSO    = 2E-10             CGBO    = 1E-9
+CJ      = 4.197772E-4  PB      = 0.99              MJ      = 0.4515044
+CJSW    = 3.242724E-10 PBSW    = 0.1               MJSW    = 0.1153991
+CJSWG   = 1.64E-10     PBSWG   = 0.1               MJSWG   = 0.1153991
+CF      = 0            PVTH0   = 0.0585501         PRDSW   = 133.285505
+PK2     = -0.0299638   WKETA   = -0.0248758        LKETA   = 1.173187E-3
+AF      = 1            KF      = 0)
*
```

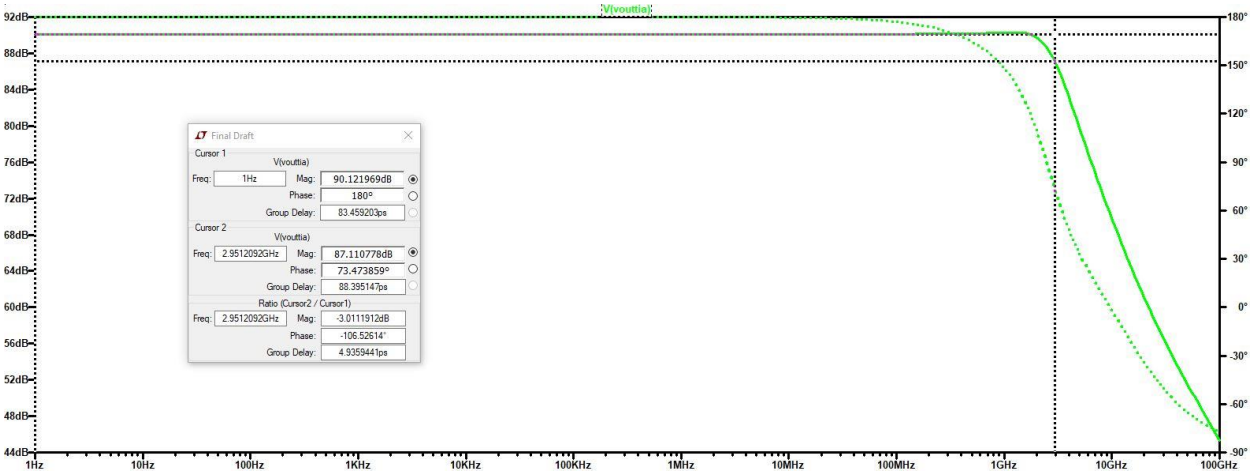
PMOS

```
.MODEL PMOS PMOS (                                  LEVEL   = 8
+VERSION = 3.1          TNOM    = 27                TOX     = 1.39E-8
+XJ      = 1.5E-7       NCH     = 1.7E17            VTH0    = -0.9214347
+K1      = 0.5553722    K2      = 8.763328E-3       K3      = 6.3063558
+K3B     = -0.6487362   W0      = 1.280703E-8       NLX     = 2.593997E-8
+DVT0W   = 0            DVT1W   = 0                 DVT2W   = 0
+DVT0    = 2.5131165    DVT1    = 0.5480536         DVT2    = -0.1186489
+U0      = 212.0166131  UA      = 2.807115E-9       UB      = 1E-21
+UC      = -5.82128E-11 VSAT    = 1.713601E5        A0      = 0.8430019
+AGS     = 0.1328608    B0      = 7.117912E-7       B1      = 5E-6
+KETA    = -3.674859E-3 A1      = 4.77502E-5        A2      = 0.3
+RDSW    = 2.837206E3   PRWG    = -0.0363908        PRWB    = -1.016722E-5
+WR      = 1            WINT    = 2.838038E-7       LINT    = 5.528807E-8
+XL      = 0            XW      = 0                 DWG     = -1.606385E-8
+DWB     = 2.266386E-8  VOFF    = -0.0558512        NFACTOR = 0.9342488
+CIT     = 0            CDSC    = 2.4E-4            CDSCD   = 0
+CDSCB   = 0            ETA0    = 0.3251882         ETAB    = -0.0580325
+DSUB    = 1            PCLM    = 2.2409567         PDIBLC1 = 0.0411445
+PDIBLC2 = 3.355575E-3  PDIBLCB = -0.0551797        DROUT   = 0.2036901
+PSCBE1  = 6.44809E9    PSCBE2  = 6.300848E-10      PVAG    = 0
+DELTA   = 0.01         RSH     = 101.6             MOBMOD  = 1
+PRT     = 59.494       UTE     = -1                KT1     = -0.2942
+KT1L    = 1.68E-9      KT2     = 0                 UA1     = 4.5E-9
+UB1     = -6.3E-18     UC1     = -1E-10            AT      = 1E3
+WL      = 0            WLN     = 1                 WW      = 0
+WWN     = 1            WWL     = 0                 LL      = 0
+LLN     = 1            LW      = 0                 LWN     = 1
+LWL     = 0            CAPMOD  = 2                 XPART   = 0.5
+CGDO    = 2.9E-10      CGSO    = 2.9E-10           CGBO    = 1E-9
+CJ      = 7.235528E-4  PB      = 0.9527355         MJ      = 0.4955293
+CJSW    = 2.692786E-10 PBSW    = 0.99              MJSW    = 0.2958392
+CJSWG   = 6.4E-11      PBSWG   = 0.99              MJSWG   = 0.2958392
+CF      = 0            PVTH0   = 5.98016E-3        PRDSW   = 14.8598424
+PK2     = 3.73981E-3   WKETA   = 5.292165E-3       LKETA   = -4.205905E-3
+AF      = 1            KF      = 0)
```

I started by designing each stage of my TIA separately and then connecting them. My first stage is a shunt – shunt amplifier with a gain of $30k\Omega$ and minimum bandwidth of 250MHz. I will test my design by running an AC response without a load because the output of this stage will connect to the second stage through the gate of an NMOS.



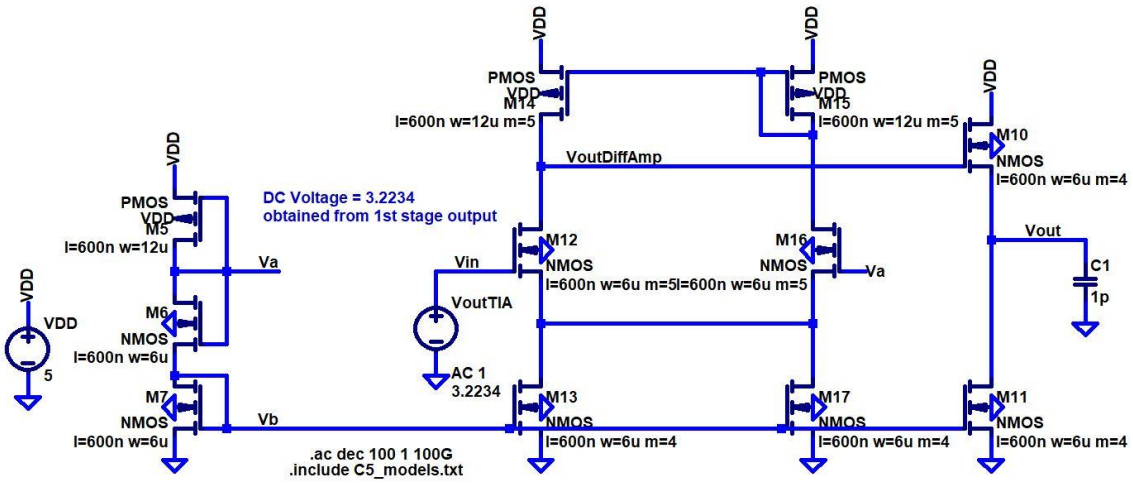
First stage of my amplifier with biasing



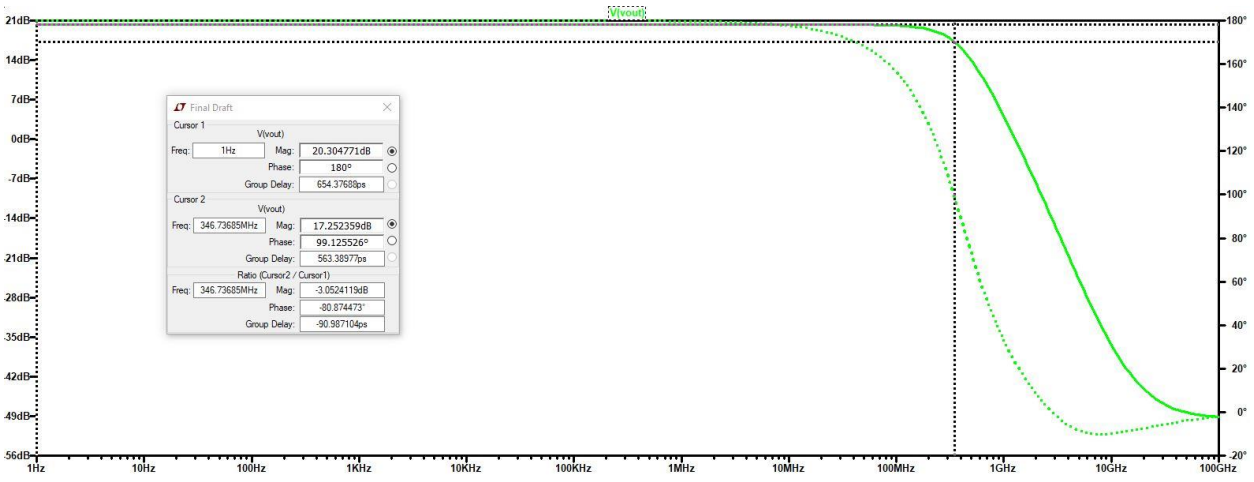
AC Response of my first stage

Gain = 90.1dB Bandwidth = 2.95GHz

My second stage is a series – shunt amplifier using a diff amp topology. I decided to use this topology because it was easy to bias and reach the desired specifications while staying within the maximum current consumption. I chose an NMOS diff amp because the DC output voltage of the first stage was at 3V and a rising input current results in a lowering output voltage. With a lower output voltage (input voltage to the second stage) the output of the second stage will increase which increases the total output voltage. This results in an increasing output voltage with an increasing input current.



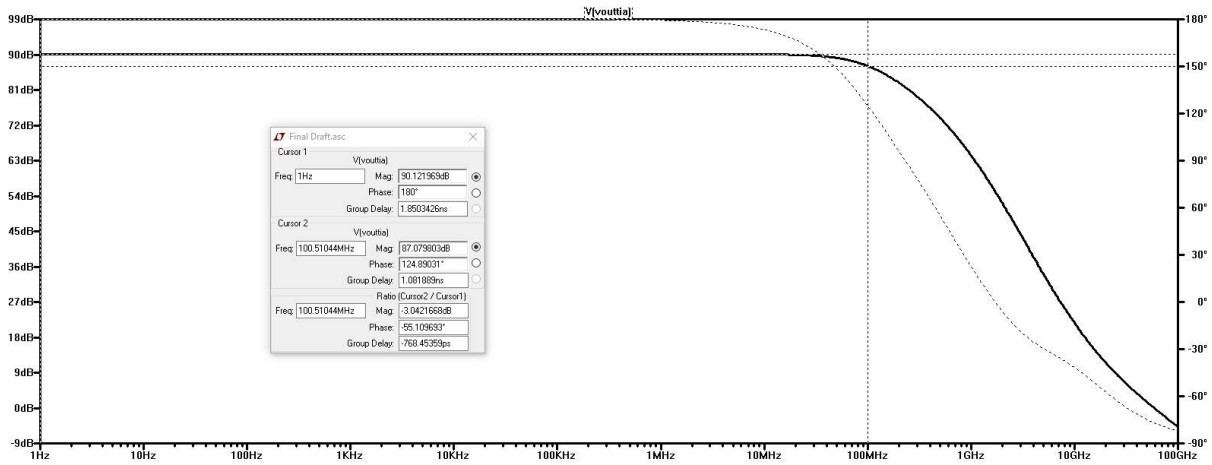
Second stage of my amplifier with biasing



AC Response of my second stage with high impedance load (1pF capacitor)

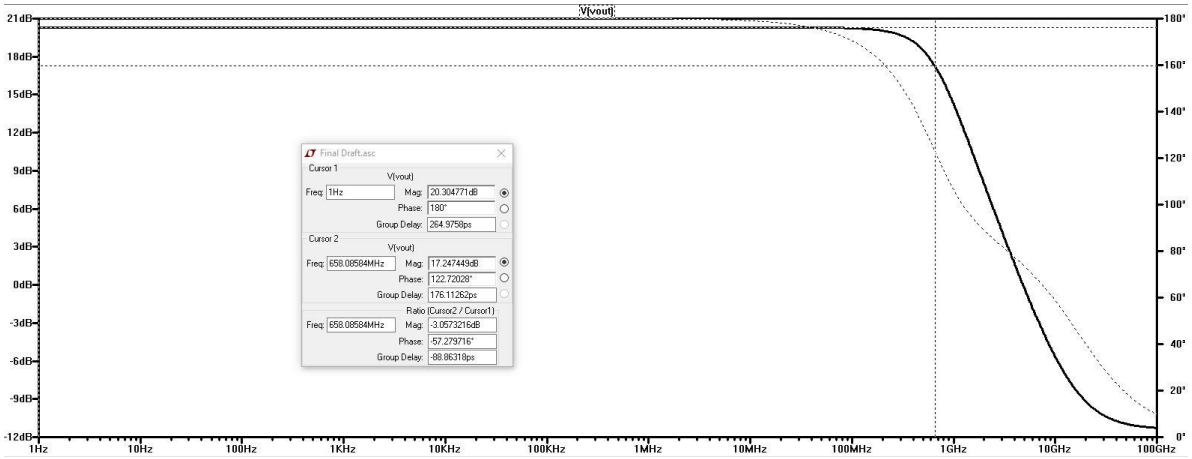
Gain = 20.3dB Bandwidth = 346.7MHz

The second stage is necessary for my design to be able to drive the high impedance load.



Simulation of my first stage with a 1pF load on the output

	Gain	**Bandwidth**
Without load	90.12 dB	2.95 GHz
With 1pF load	90.12 dB	100.5 MHz

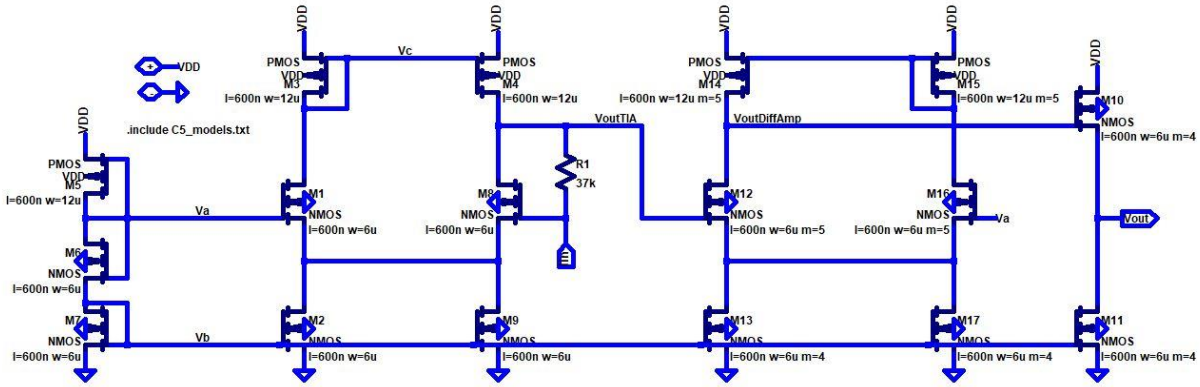


Simulation of my second stage with no load

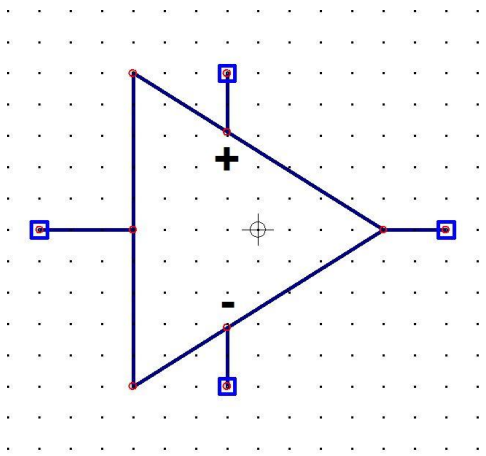
	Gain	**Bandwidth**
Without load	20.3 dB	658 MHz
With 1pF load	20.3 dB	346.7 MHz

Comparing the first stage to the second stage I noticed the bandwidth of the first stage would drop significantly compared to the second stage bandwidth. The bandwidth of the first stage with the load is reduced to 3% of the bandwidth without the load. The bandwidth of the second stage with the load is reduced to 50% of the bandwidth without the load giving a bandwidth that meets the specification. The second stage is necessary for my design in order to meet the bandwidth specification.

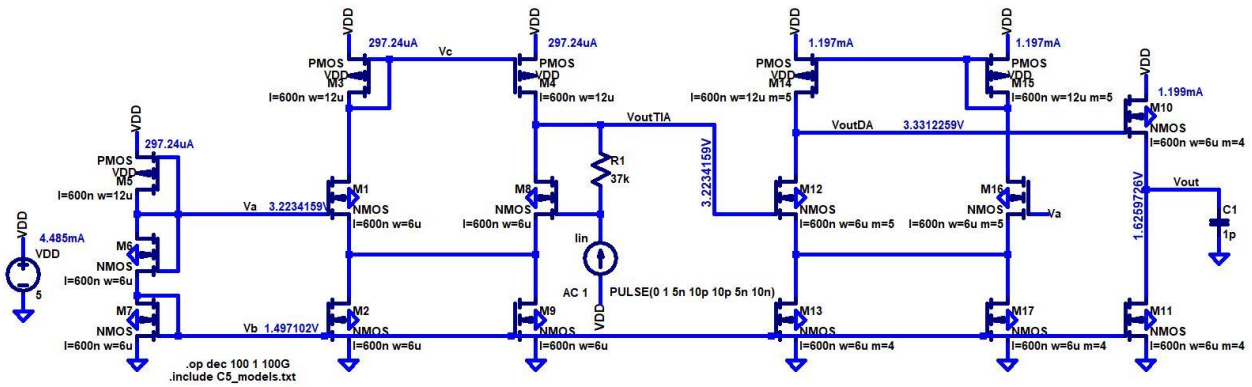
Since both stages work within specification I connected them to make the following schematic:



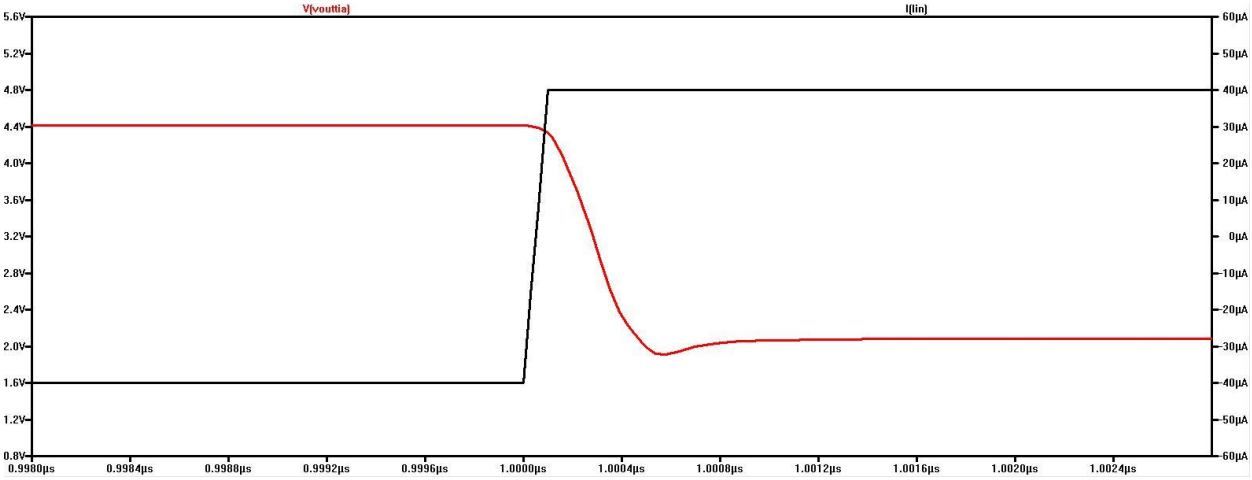
Final design schematic



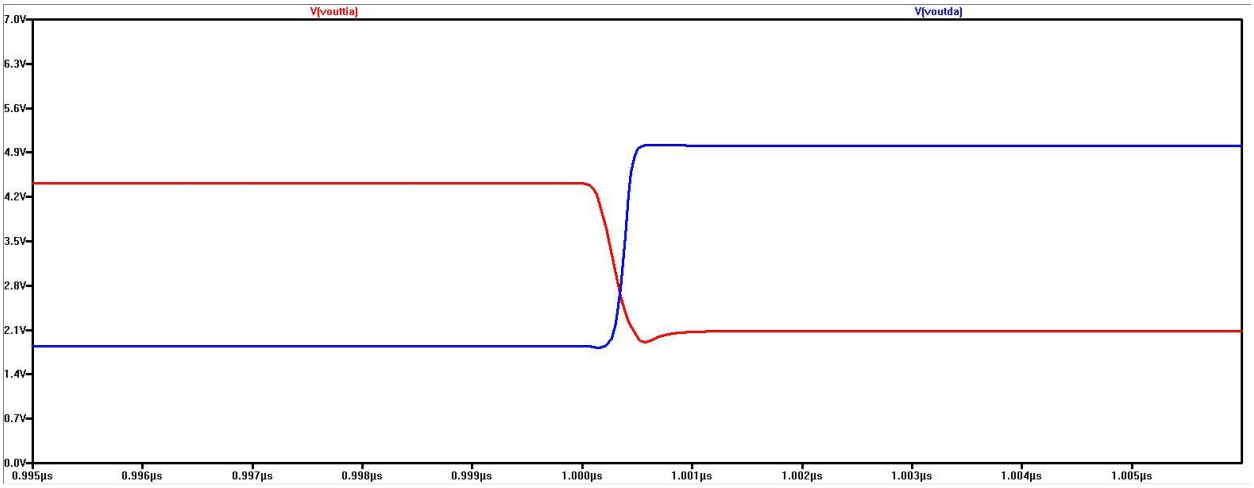
Symbol of my final design for clean schematics



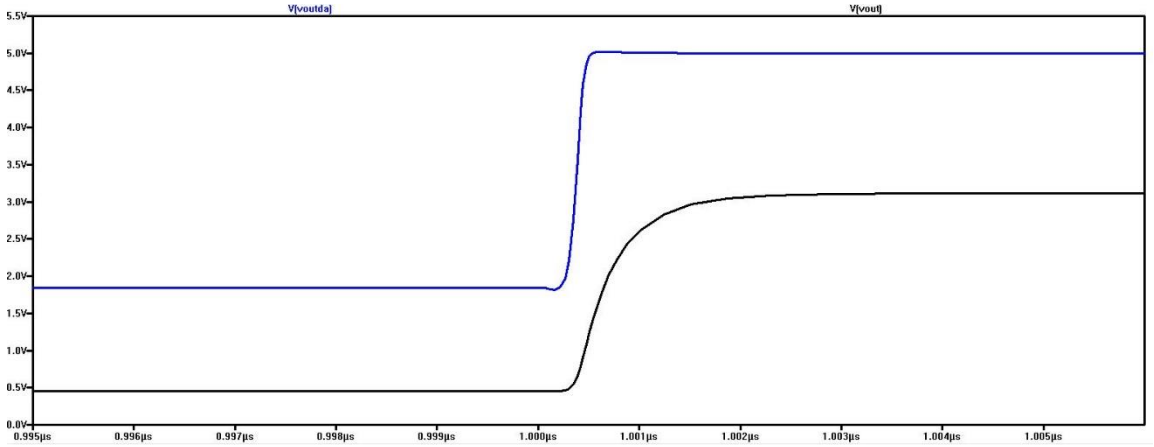
Final design with DC operating points labeled



Large signal operation from input source to first stage output

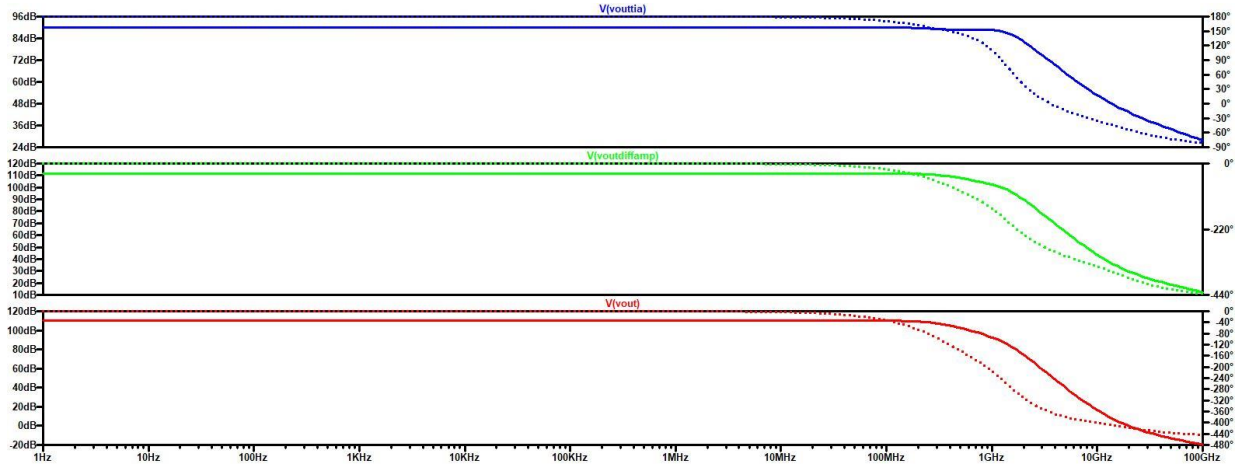


Large signal operation from output of first stage to input of second stage



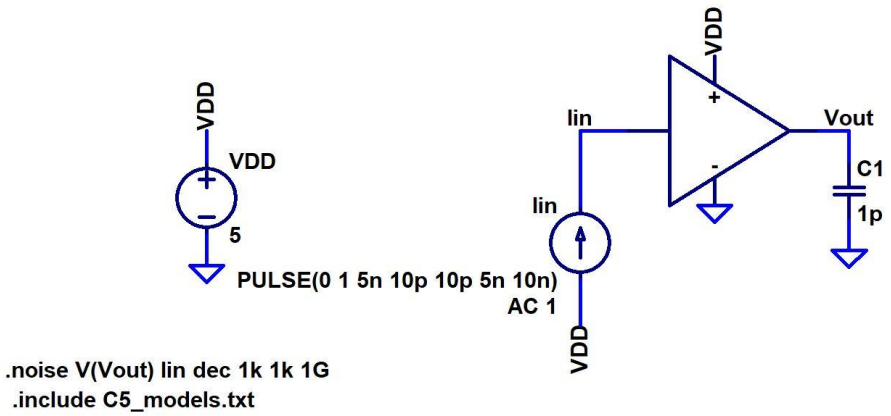
Large signal operation from input of source follower to the output of the source follower

These large signal simulations show how an increasing or decreasing input will affect the output of the corresponding stage. This is useful for deciding the topology of the following stages because I want to design the output voltage to increase with an increasing input.

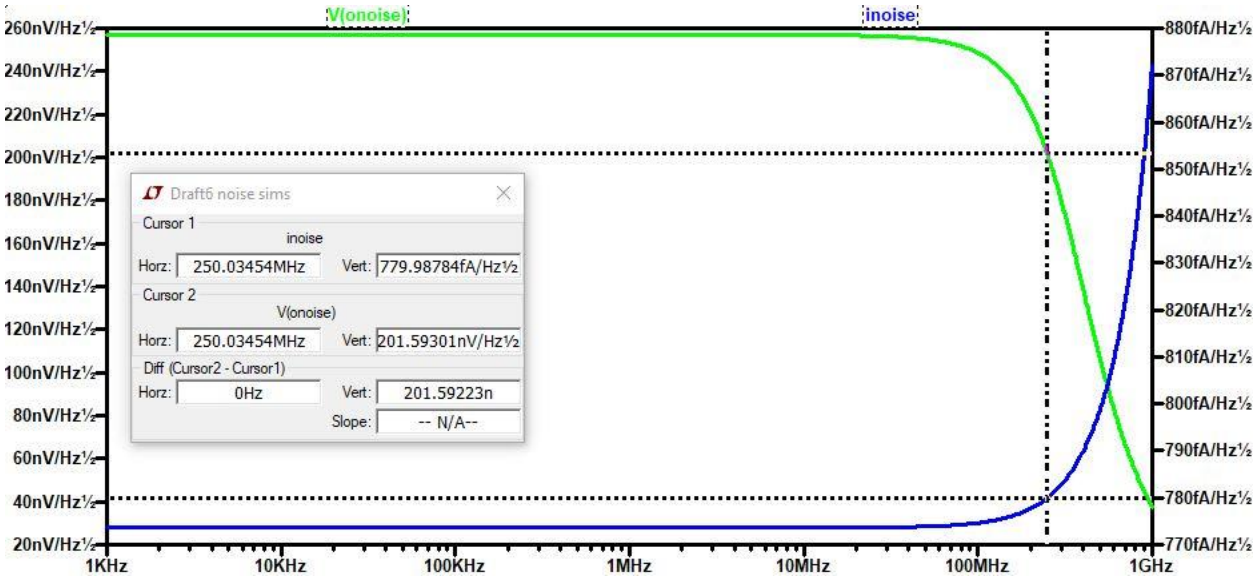


AC response of my final design probing the outputs of each stage

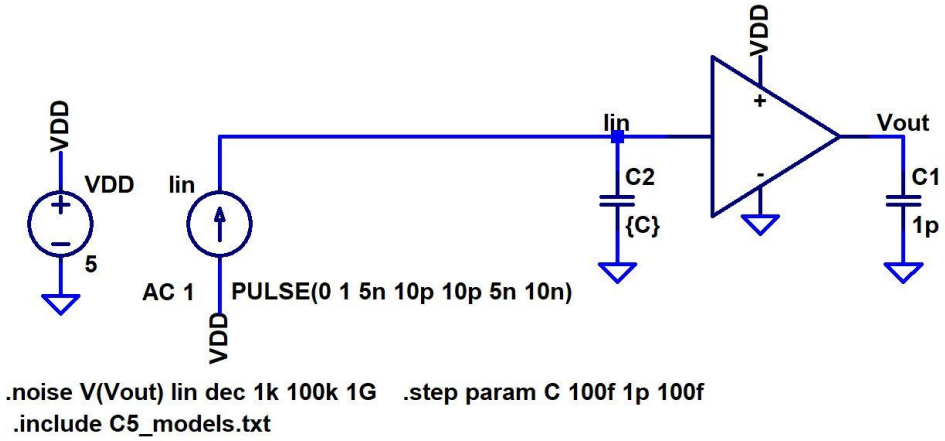
	Gain	**Bandwidth**
VoutTIA	90.1 dB	1.39 GHz
VoutDiffAmp	111.6 dB	446 MHz
Vout	110.4 dB	295 MHz



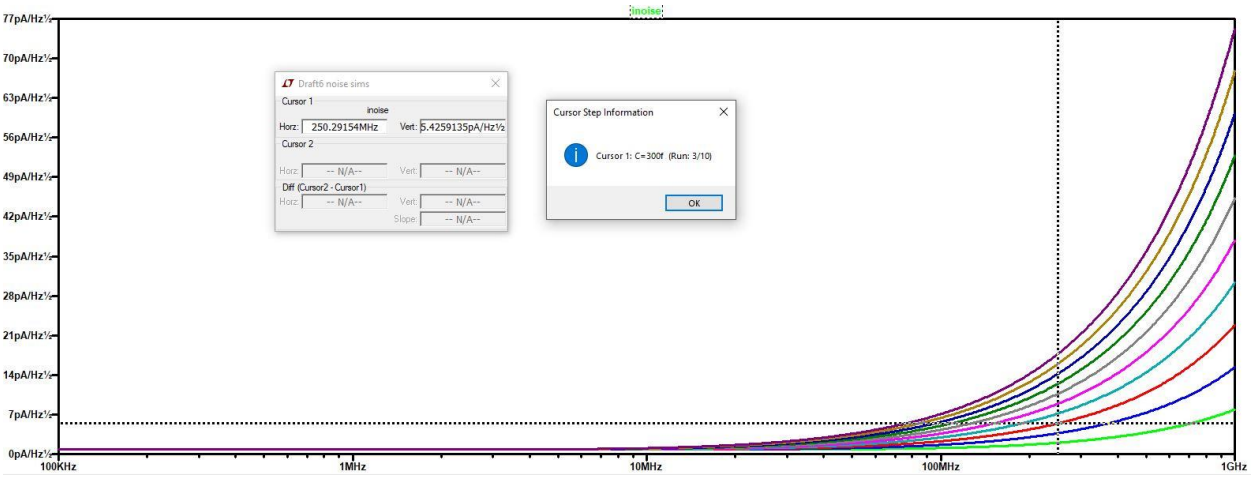
Schematic used to obtain noise performance of my design



Simulation showing my input and output referred noise



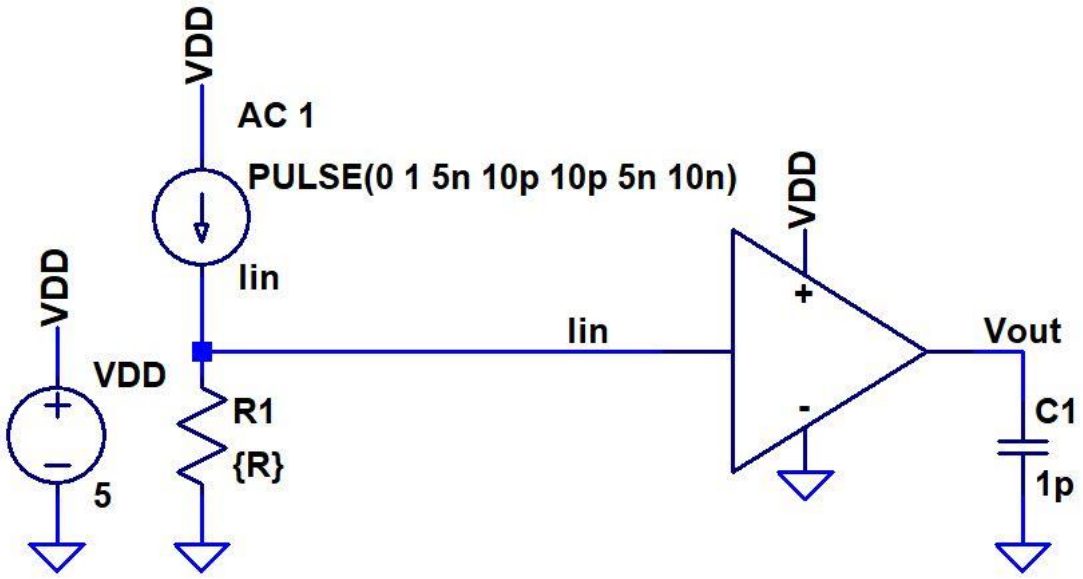
Schematic used to obtain noise performance of my design with input capacitance



Simulation showing that input capacitance becomes significant at 300fF

Capacitor	**Input noise**
100fF	2.00 $pA/\sqrt{Hz}$
200fF	3.68 $pA/\sqrt{Hz}$
300fF	5.42 $pA/\sqrt{Hz}$
400fF	7.16 $pA/\sqrt{Hz}$
500fF	8.91 $pA/\sqrt{Hz}$
600fF	10.66 $pA/\sqrt{Hz}$
700fF	12.42 $pA/\sqrt{Hz}$
800fF	14.18 $pA/\sqrt{Hz}$
900fF	15.93 $pA/\sqrt{Hz}$
1000fF	17.69 $pA/\sqrt{Hz}$

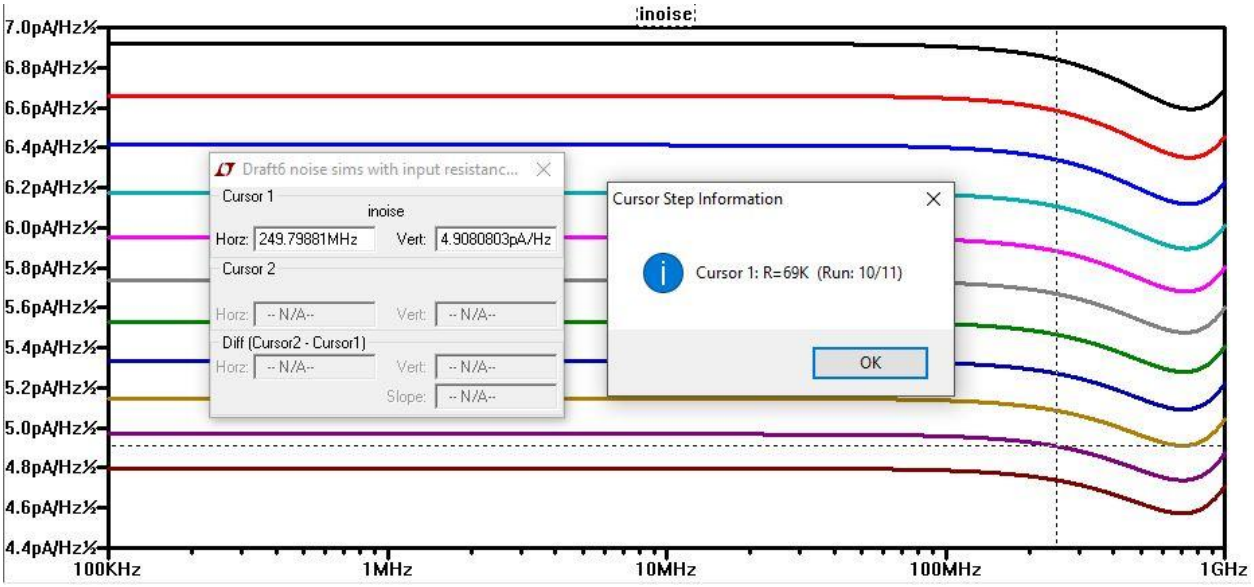
Table showing the input noise with varying input capacitance



.noise V(Vout) lin dec 1k 100k 1G .step param R 60k 70k 1k

.include C5_models.txt

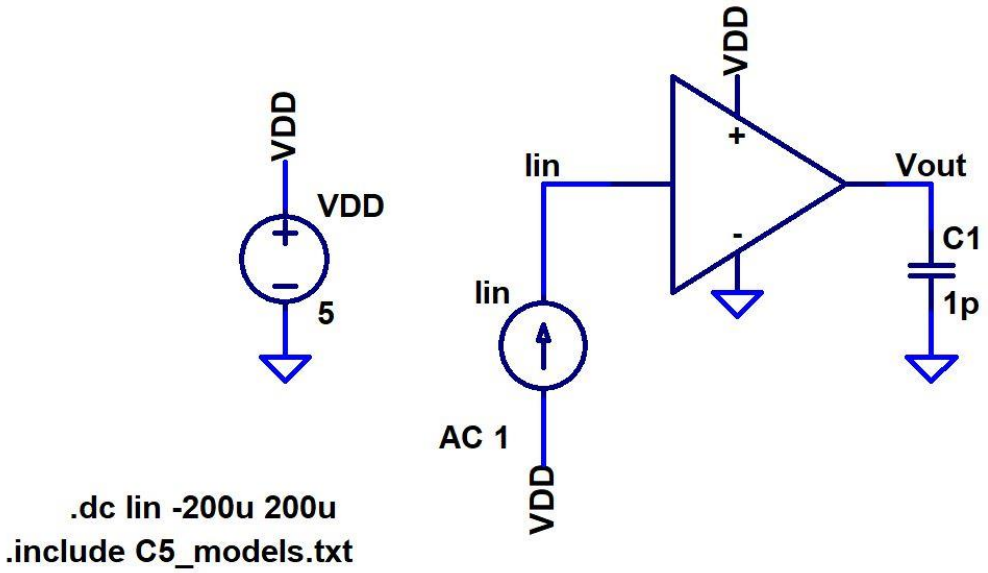
Schematic used to obtain noise performance of my design with input resistance



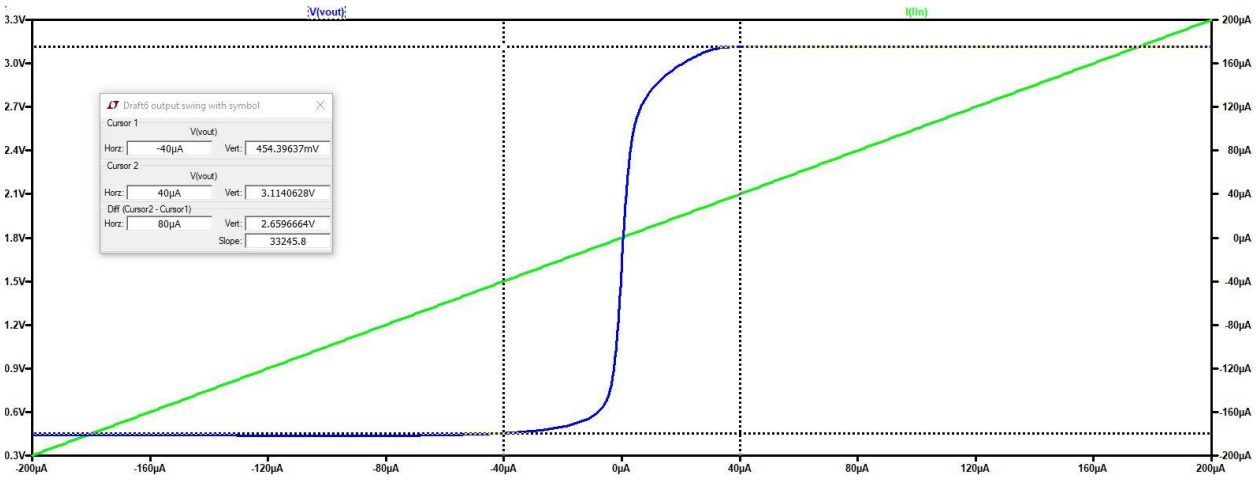
Simulation showing that input resistance needs to be at least 69k to meet the noise specification

Resistor	Input noise	DC Voltage
60k	6.84 $pA/\sqrt{Hz}$	2.81 V
61k	6.58 $pA/\sqrt{Hz}$	2.82 V
62k	6.33 $pA/\sqrt{Hz}$	2.83 V
63k	6.10 $pA/\sqrt{Hz}$	2.84 V
64k	5.88 $pA/\sqrt{Hz}$	2.85 V
65k	5.67 $pA/\sqrt{Hz}$	2.86 V
66k	5.46 $pA/\sqrt{Hz}$	2.87 V
67k	5.27 $pA/\sqrt{Hz}$	2.88 V
68k	5.08 $pA/\sqrt{Hz}$	2.89 V
69k	4.9 $pA/\sqrt{Hz}$	2.89 V
70k	4.74 $pA/\sqrt{Hz}$	2.90 V

A smaller resistor on the input will increase the amount of noise on the input and reduce the DC bias voltage. This is a problem with my design because the input of my TIA is on the gate of an NMOS device. With a 69k resistor my DC bias voltage is at 2.89V which will properly bias my diff amp. Using a larger resistor will reduce the input noise and increase the bias voltage on the gate of the NMOS which will pull the output DC voltage down. The APDs cathode should be connected to my VDD with the anode connected to the input (gate of NMOS) of the front-end and a resistor to ground. The resistor should be chosen based on the above information to bias my diff amp correctly as well as reduce the input referred noise of the circuit.



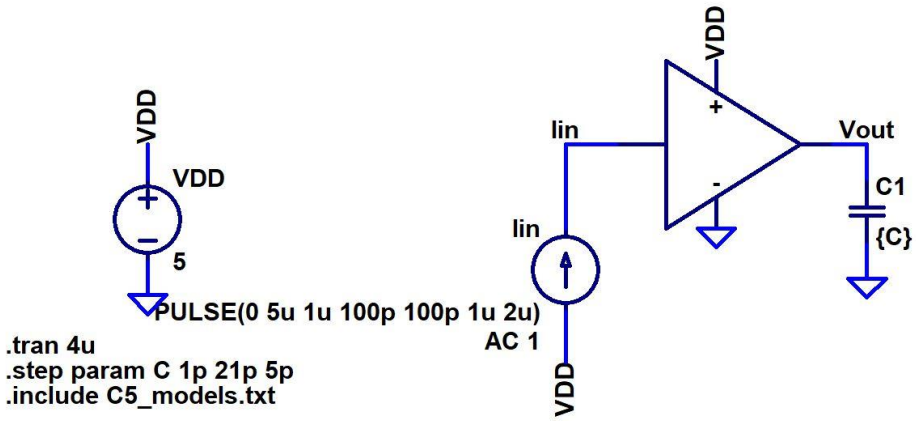
Schematic used to obtain the output swing of my design



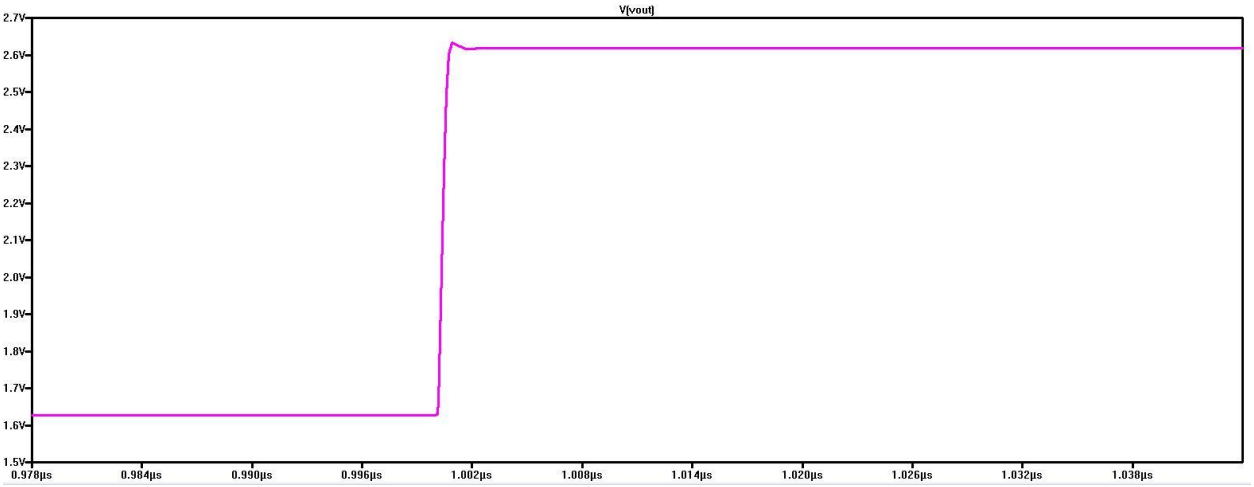
Simulation of my output swing

Operating current	**Output swing**
-40uA to 40uA	454mV to 3.11V = 2.659V

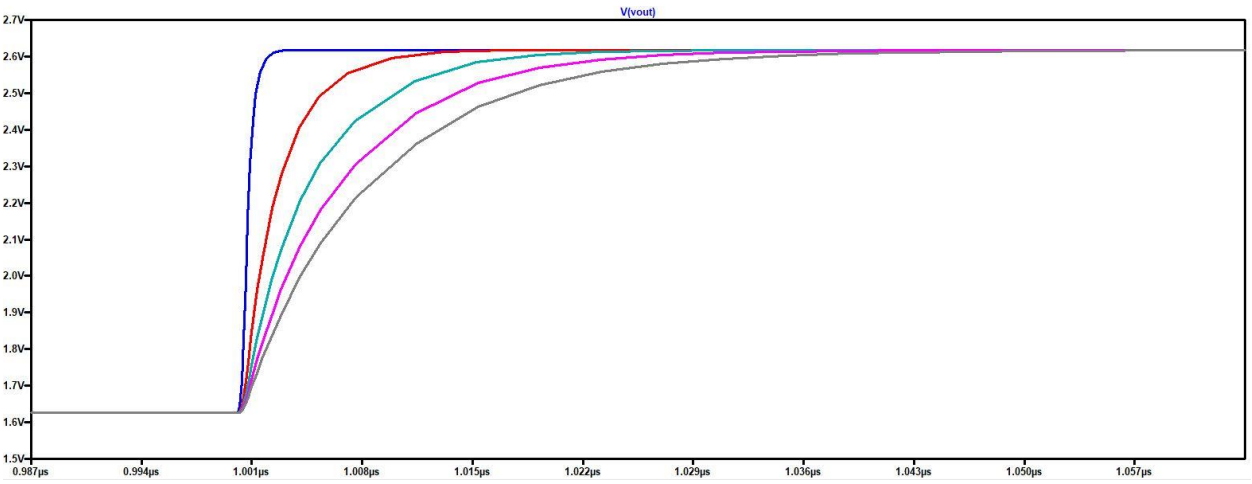
My output voltage swings from 454mV to 3.11 V centered around 1.8V.



Schematic used to obtain slew rates and settling times of my design



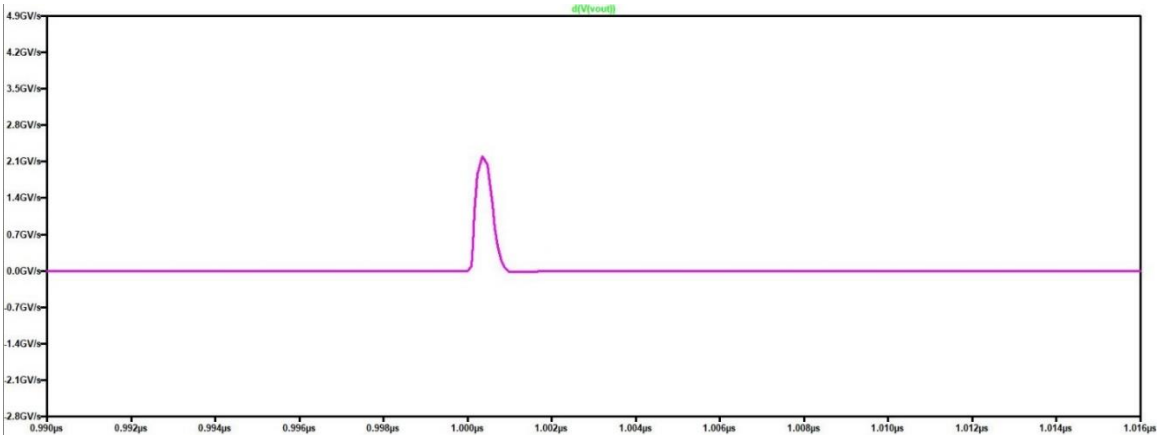
Simulation showing settling time with no load



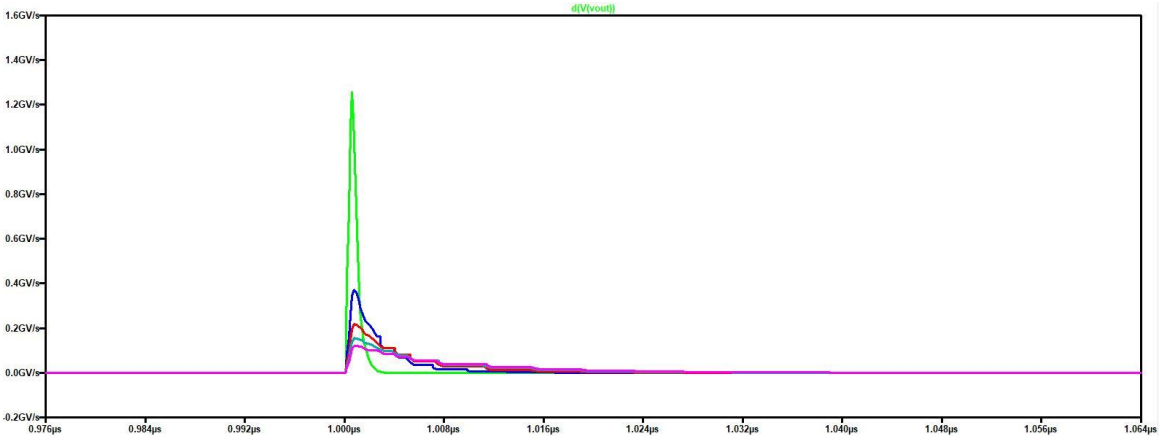
Simulation showing settling times with varying loads

Capacitive load	Peak Value	Settling Time
1 pF	2.617 V	1.205 ns
6 pF	2.617 V	5.211 ns
11 pF	2.617 V	9.706 ns
16 pF	2.617 V	13.42 ns
21 pF	2.617 V	17.03 ns
no load	2.617 V	600 ps

Settling times for varying capacitive loads



Simulation showing slew-rate with no load



Simulation showing slew-rates with varying loads

Capacitive load	Slew-Rate
1 pF	1.25 GV/s
6 pF	375 MV/s
11 pF	224 MV/s
16 pF	159 MV/s
21 pF	116 MV/s
no load	2.32 GV/s

Slew-rates for varying capacitive loads