BOISE STATE UNIVERSITY

Wide I/O DRAM Architecture Utilizing Proximity Communication

by

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Thesis Defense – October 8th, 2009

College of Engineering

Introduction

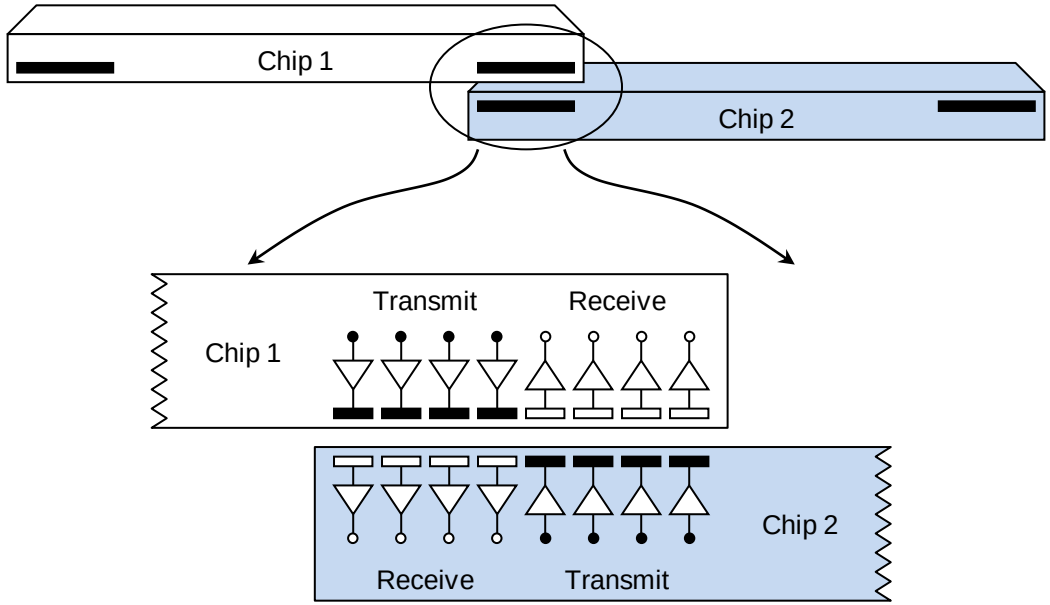
Bandwidth and power consumption of dynamic random access memory stifles computer performance scaling

- Background
- Status of Proximity Communication
- DRAM Market Analysis
- 4 Gb DRAM Architecture
- Wide I/O DRAM Architecture Utilizing Proximity Communication

Background

- Memory Gap
  - ✓ Main memory does not scale with processor performance
- Power
  - ✓ Current consumption is rising
  - ✓ Bandwidth increases power
  - ✓ Voltage scaling masks the issue
- Density
  - ✓ Memory channel loading
  - ✓ Limits bandwidth
- Proximity Communication
  - ✓ Proposed by Ivan Sutherland – US Patent #6,500,696
  - ✓ Promises to reduce power and increase bandwidth

Proximity Communication



- Capacitive Coupled Proximity Communication
  - ✓ Top metal forms the parallel plates
  - ✓ Chip-to-chip communication through coupling capacitor

Ref:[1]

Proximity Communication

- Benefits
  - ✓ Increased I/O density
  - ✓ Avoids on/off chip wires
  - ✓ Eases chip replacement at the system level
  - ✓ Enhances system level testability
  - ✓ Enables smaller chip sizes
  - ✓ Removes the need for ESD protection
- Challenges
  - ✓ Mechanical misalignment
  - ✓ Applying power to the chips
  - ✓ Thermal solution

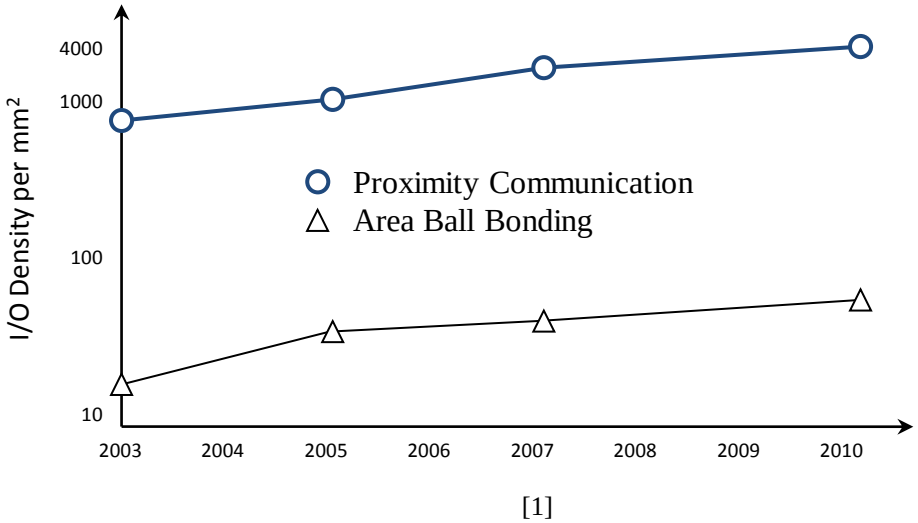
Ref:[1-5]

Proximity Communication

- Parallel Plate Capacitance

$$C = \frac{\varepsilon_0 A}{d} \qquad \varepsilon_0 = 8.9\ {}^{aF}/_{\mu m}$$

- 10 pF/mm^2
  - ✓ Chip-to-chip separation
  - ✓ d = 1 µm
- One channel
  - ✓ 50 fF
  - ✓ 200 signals/mm^2

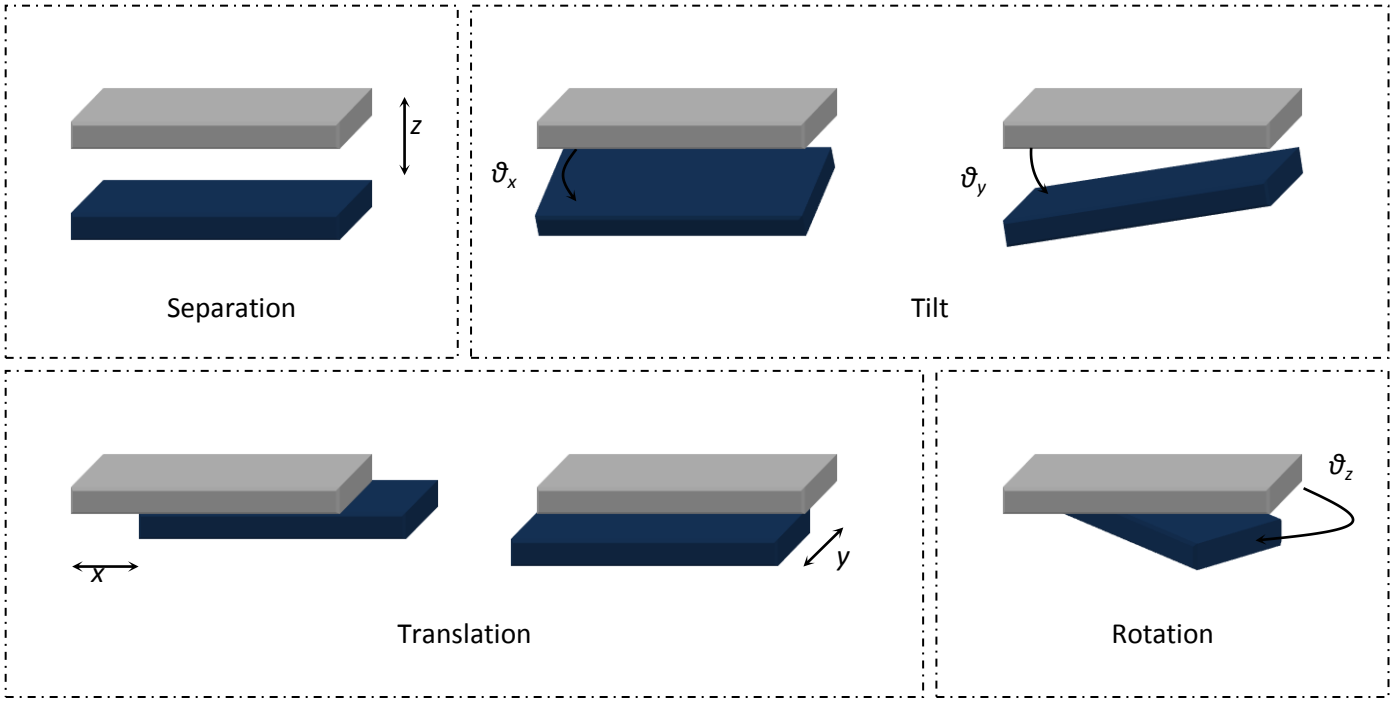


[1]

Ref:[1]

Proximity Communication

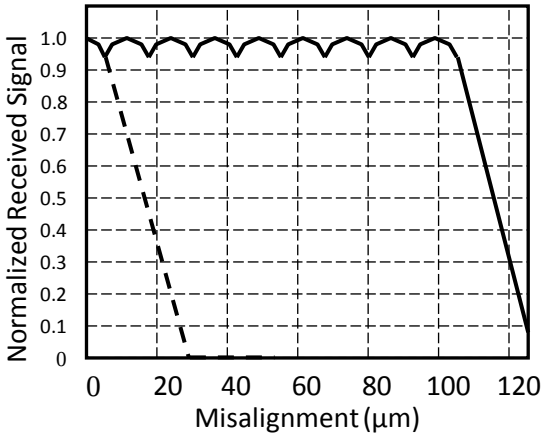
- Mechanical Misalignment
  - ✓ Six axis
  - ✓ Multiple sources

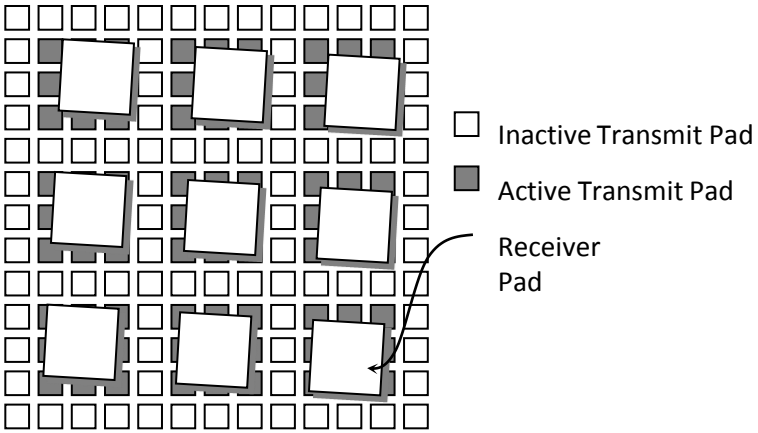


Ref:[5]

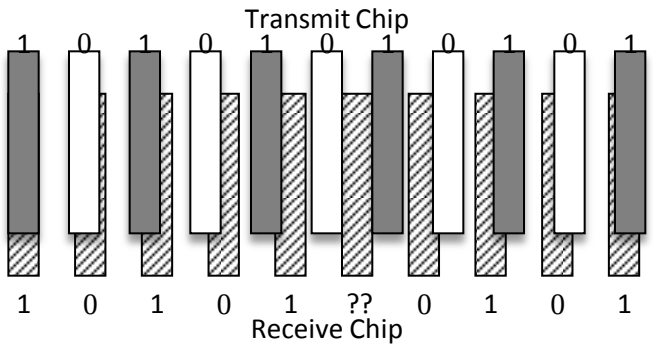
Proximity Communication

- Electronic Sensors
  - ✓ Chip-to-chip separation sensors (0.2 µm resolution)
  - ✓ Vernier scale incorporated on chip (1.0 µm resolution)
- Electrical Re-Alignment
  - ✓ Receive array
  - ✓ Micro-transmit array
  - ✓ Electronic steering circuit



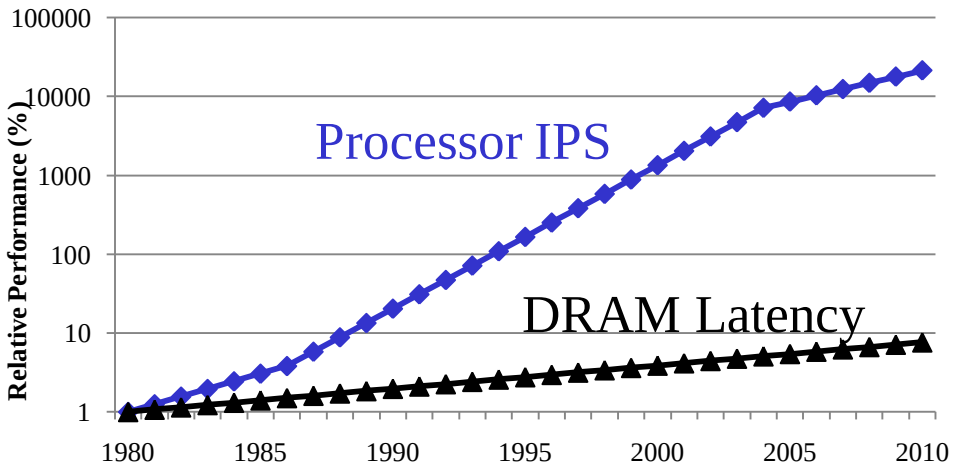


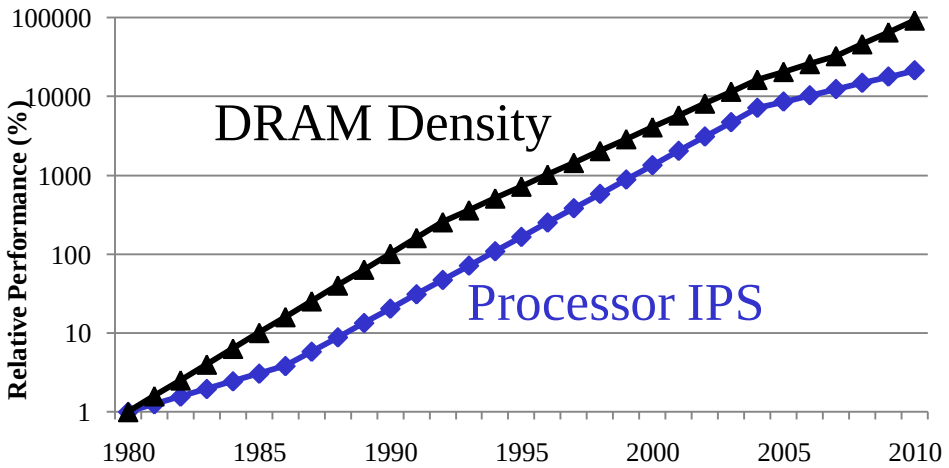
Ref:[1-5]



DRAM Market Analysis

- Revisit the Memory Gap
  - ✓ "Performance" becomes a relative term
  - ✓ Dichotomy in scaling
- Why Density?
- Why Not Latency?

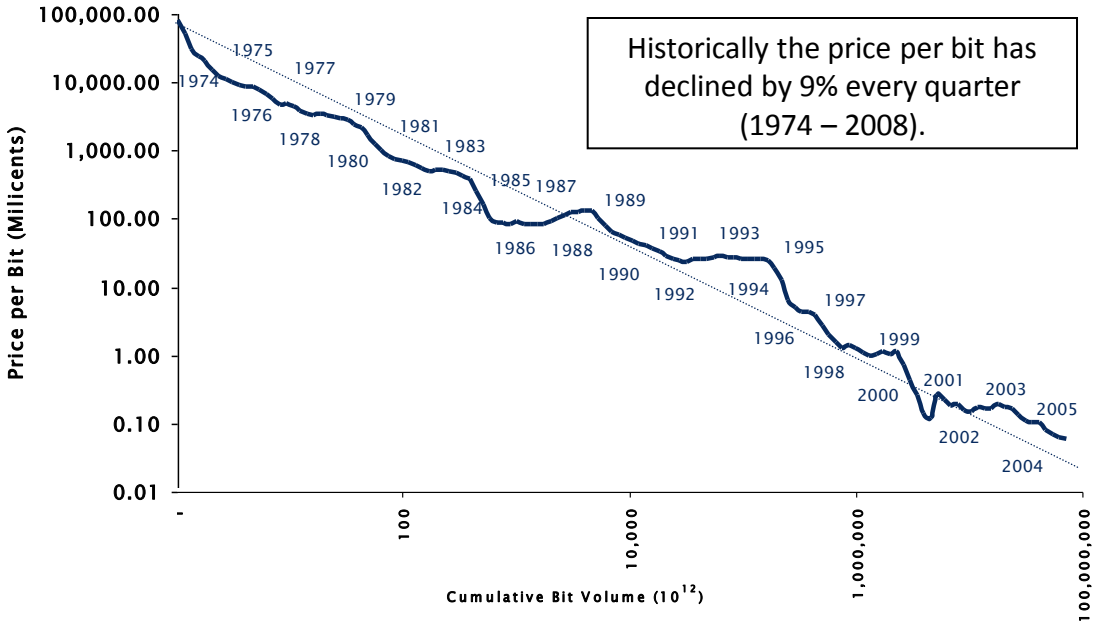




Ref:[6]

DRAM Market Analysis

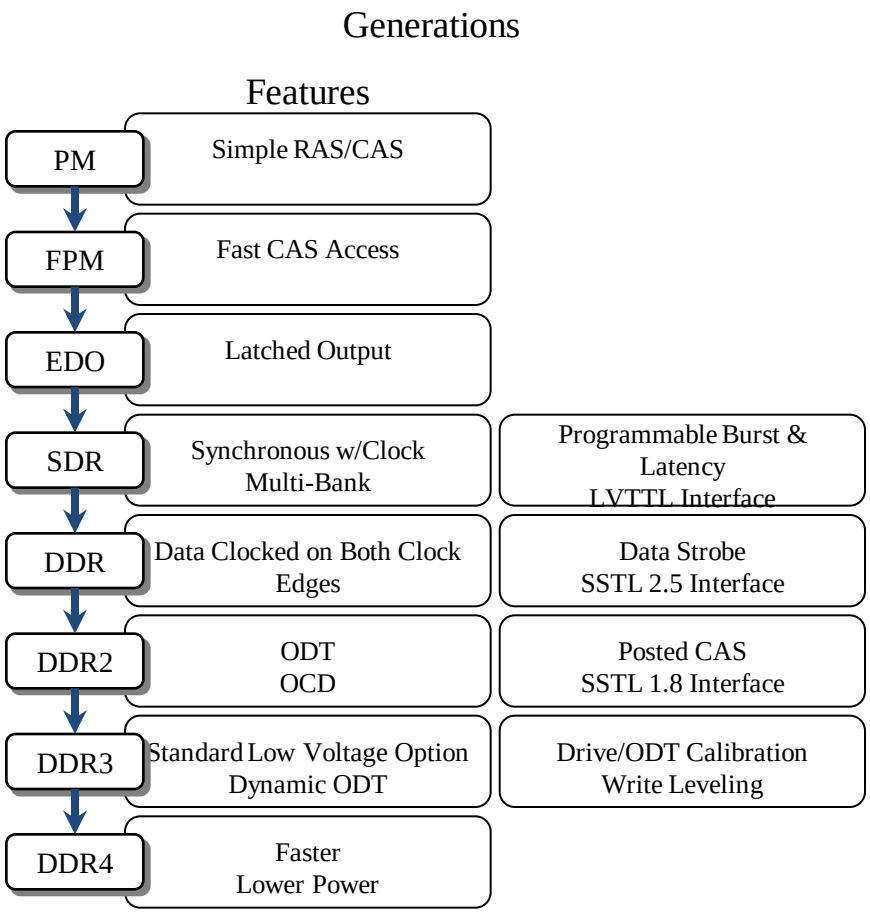
- Moore's Law
  - ✓ 41% increase in transistor count per year
- Selling Price
  - ✓ 36% historic decline per year
- Putting it into Perspective
  - ✓ 1 Gb 2009 → $2.00
  - ✓ 2 Gb 2011 → $1.64
- Density or Bust!!



Ref:[7-8]

DRAM Market Analysis

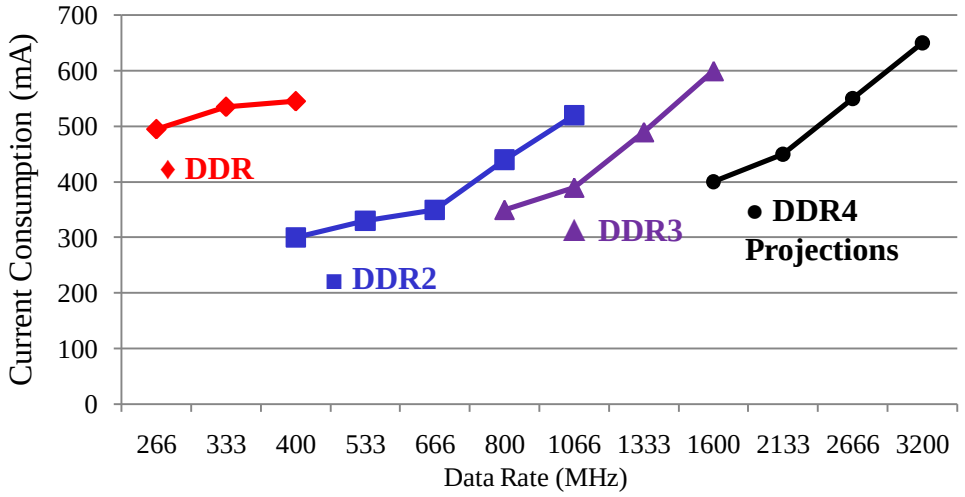
- Cost
  - ✓ Low cost manufacturing process
    - o 3 metal layers
      - Increased usage of each level
    - o Small chip size
      - Limits I/O count
- Moore's Law
  - ✓ 41% scaling per year
    - o Wordline cross sectional area
    - o Tight metal pitch
    - o Contact resistance
- Physics of Scaling
  - ✓ Latency must increase

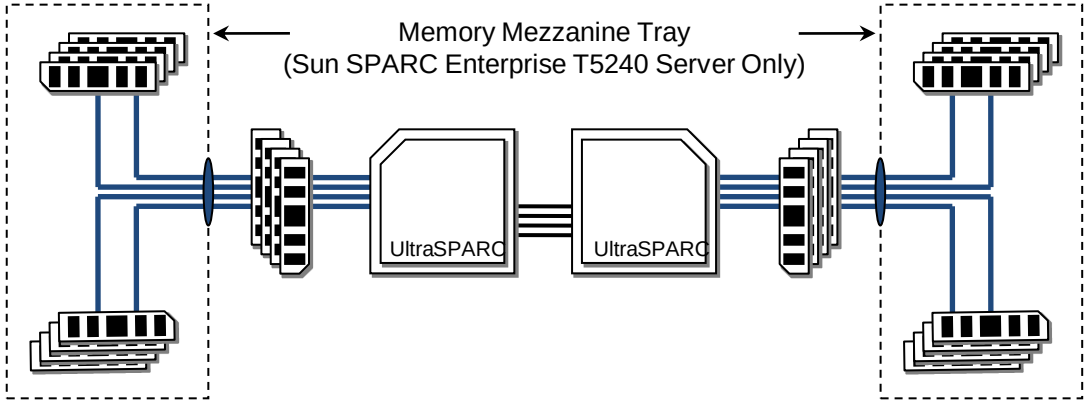


Ref:[7-8,13]

DRAM Market Analysis

- Home PC
  - ✓ Plugged into a wall
- Mobile
  - ✓ Battery life
- Server
  - ✓ Power consumption
  - ✓ Cooling
- Trending Up
  - ✓ Poor Efficiency
  - ✓ Bandwidth Driven

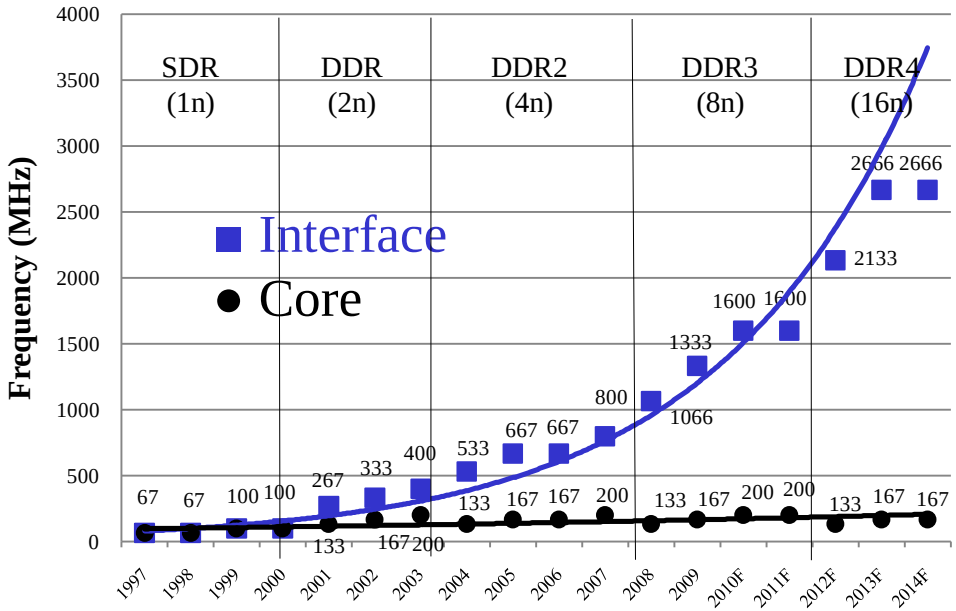


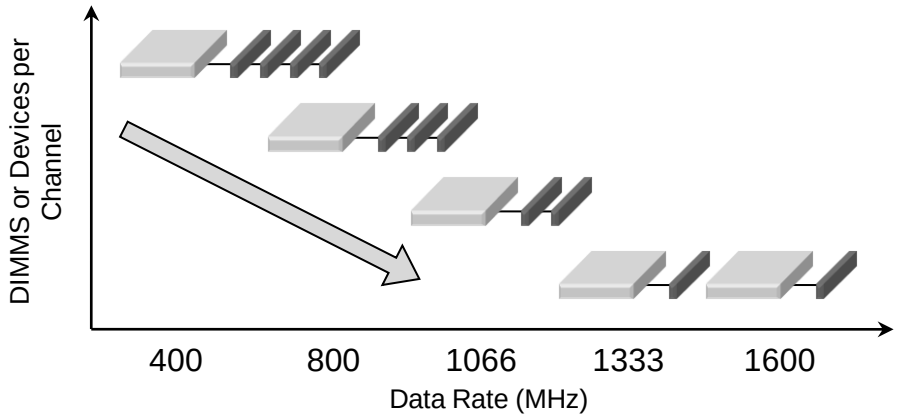


Ref:[14-17]

DRAM Market Analysis

- Interface versus Core
  - ✓ Interface bares the burden
  - ✓ Core cycles
- DRAM Pre-fetch
  - ✓ Doubles at each generation
- Density limited by bandwidth
  - ✓ SSTL loading in memory channel
  - ✓ Increase chip count per module

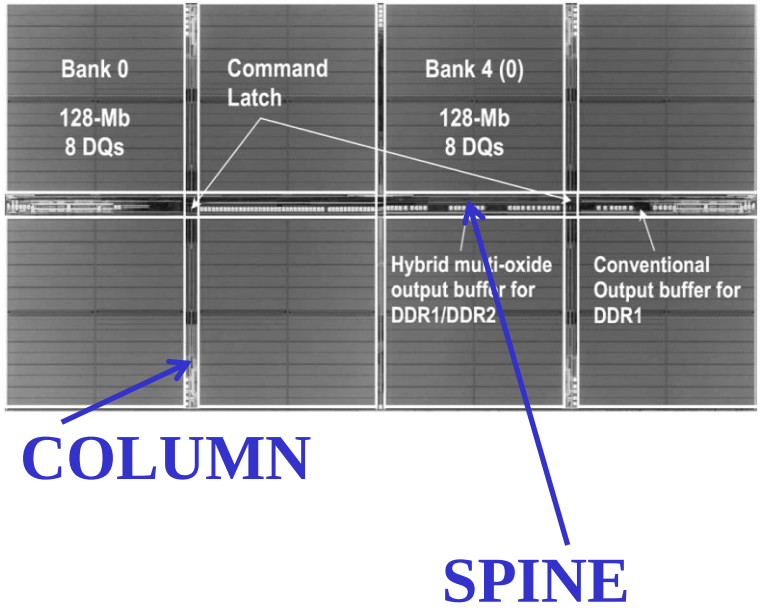


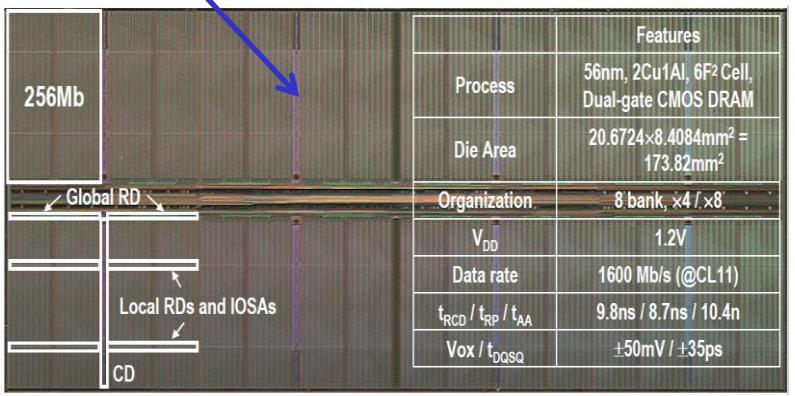


Ref:[14-17]

4 Gb DRAM Architecture

- Possible Architecture
  - ✓ Compared to ITRS
- 2012 Production Release
- 74 mm^2
- 56 % Array Efficiency
- 40 nm

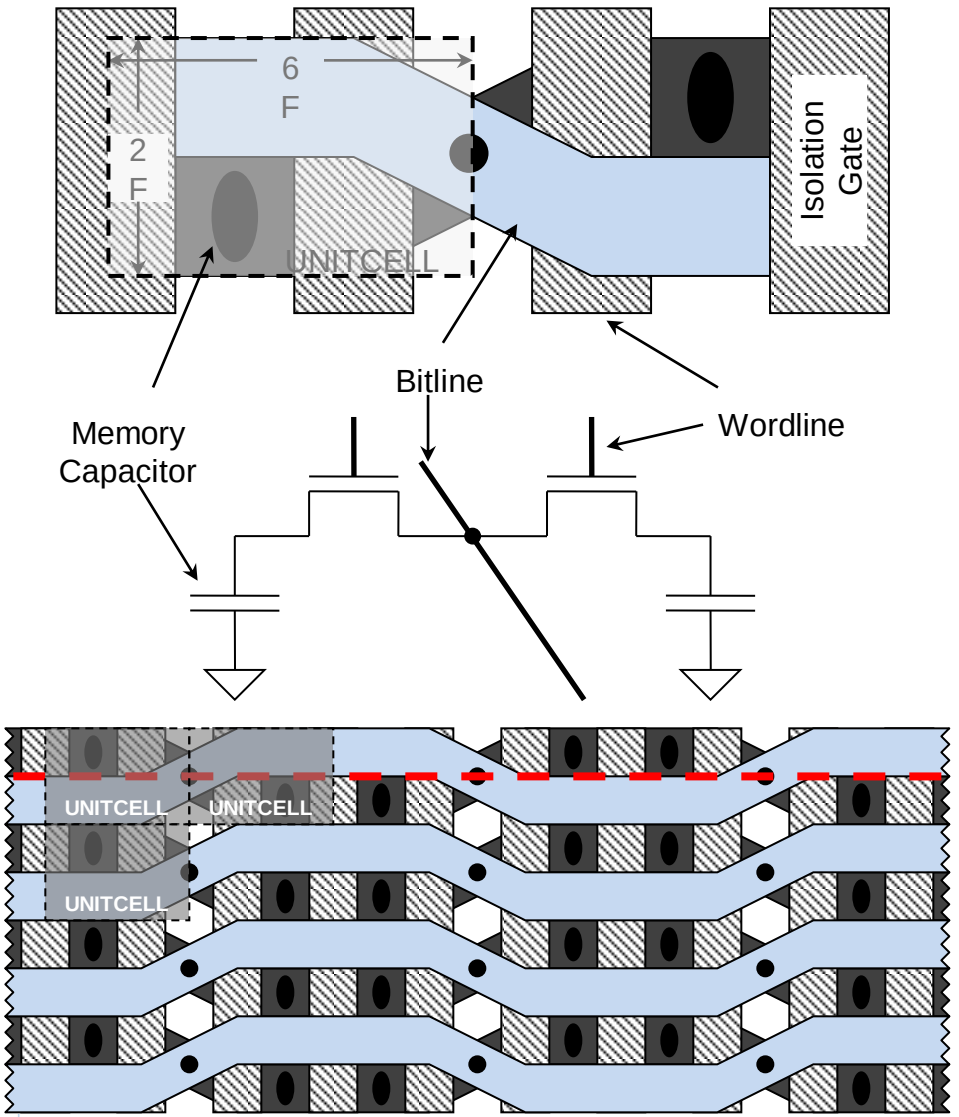




Ref:[10,12,20-24]

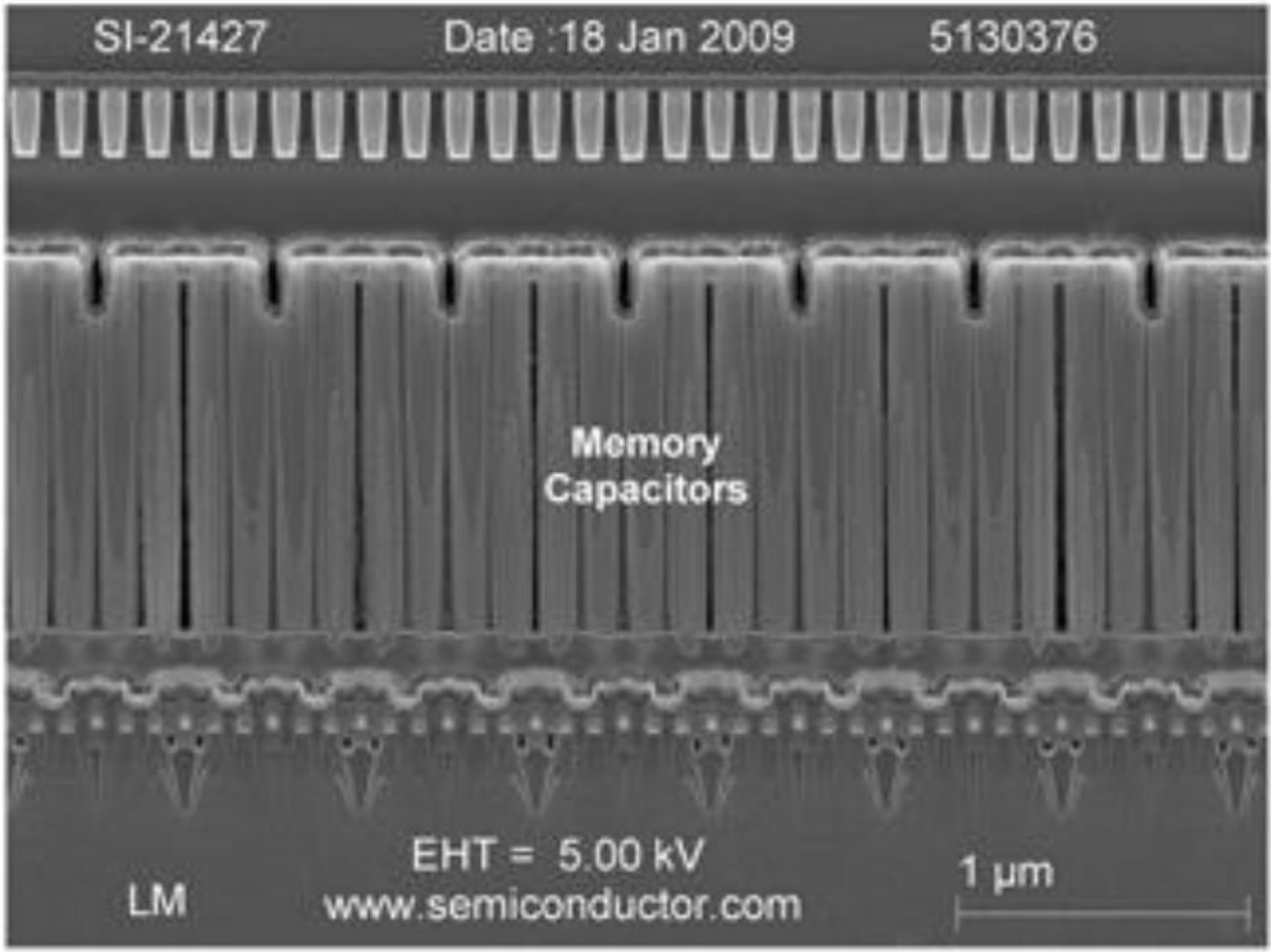
4 Gb DRAM Architecture

- $6F^2$ Memory Cell
- Feature Size = 40 nm
- Cell Area = 0.0096 μm^2
- 3F Pitch per Wordline
- 2F Pitch per Bitline
- 256 kb Array Macro
  - ✓ Core Array
  - ✓ 512 bitlines ≈ 43.6 µm
  - ✓ 512 wordlines ≈ 65.4 µm
- Periphery Circuitry
  - ✓ 4 µm space allocated



Ref:[24]

4 Gb DRAM Architecture



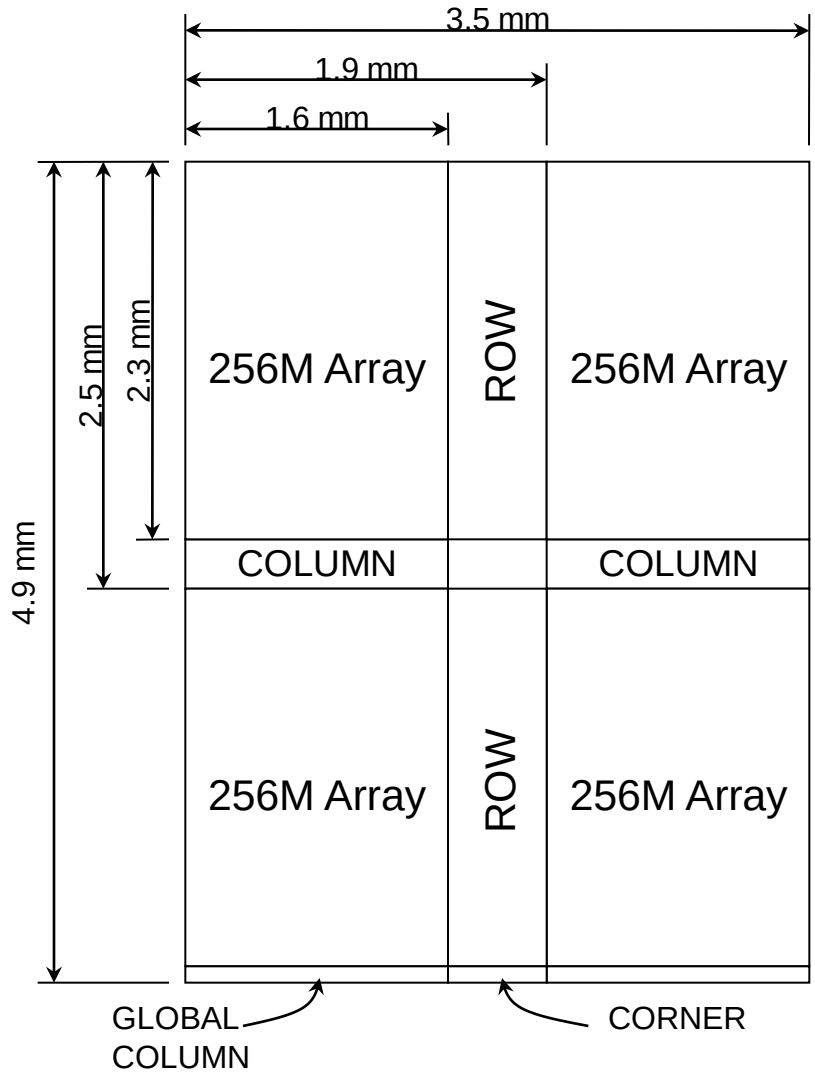
Ref:[25]

4 Gb DRAM Architecture

- 256 Mb Array
  - ✓ 32 x 32 256 kb macros

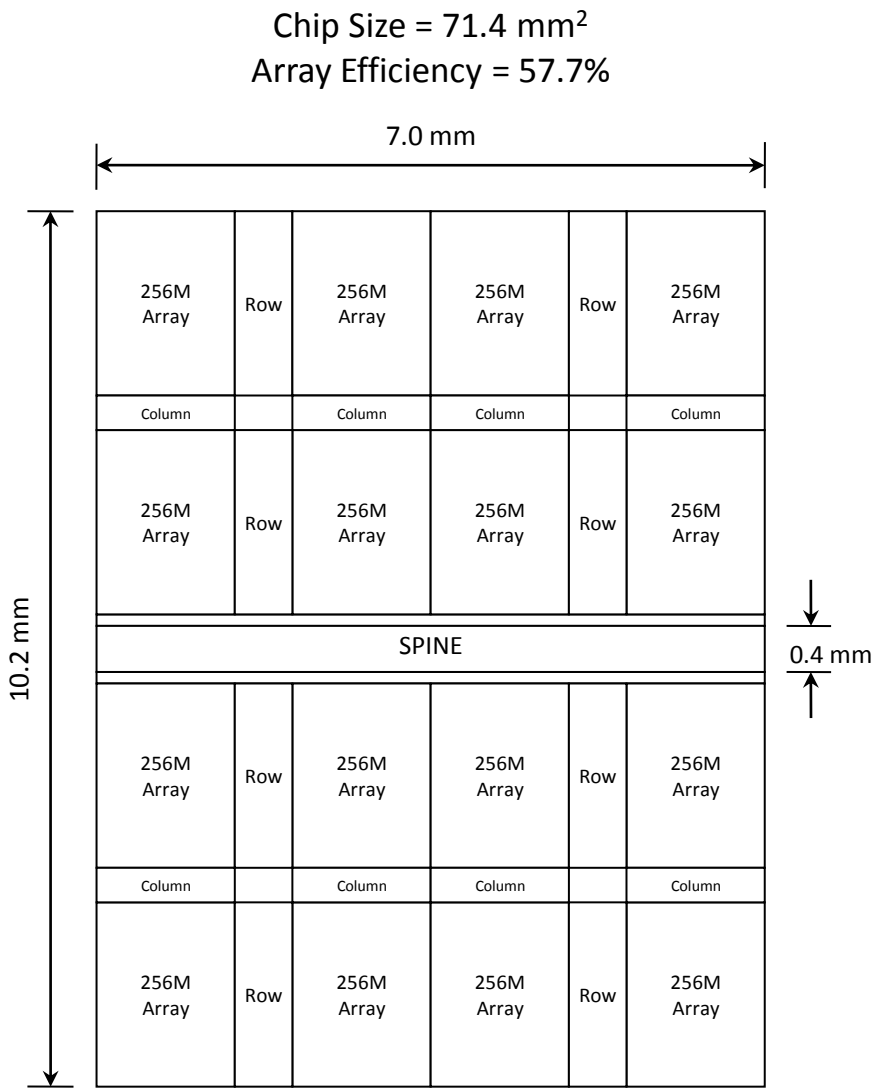
$$32 \cdot \left(43.6\,\mu m + 4\,\mu m\right) = 1.532\ mm$$

- 1 Gb Array
  - ✓ Multiple implementations



4 Gb DRAM Architecture

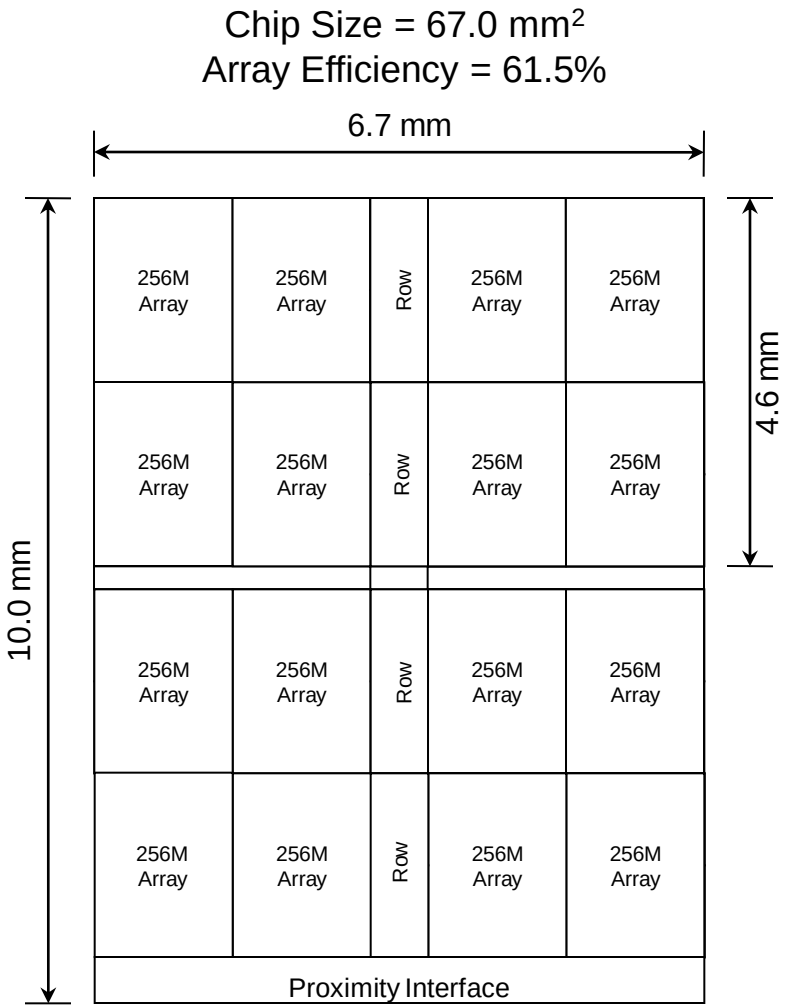
- ITRS
  - ✓ 74 mm^2
  - ✓ 56% Array Efficiency
- Wide I/O Architecture
  - ✓ Moving the pads
  - ✓ Centralized Row
  - ✓ Centralized Column



Ref:[29]

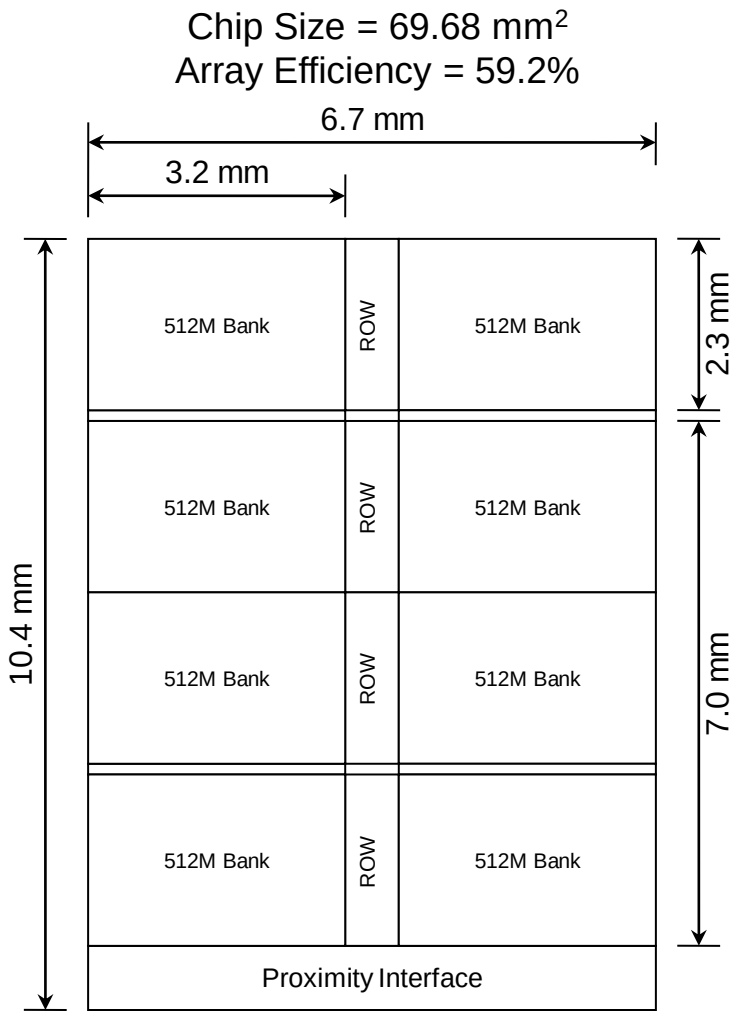
Wide I/O Chip Architecture

- 64 Bytes per Chip
- 6.2% Chip Size Reduction
- 6.6% Increase in Array Efficiency
- Challenges
  - ✓ Routing from the edge
  - ✓ Array I/O route increase
    - o 2.3 mm → 4.6 mm
  - ✓ Additional row decode
- Create Eight Internal Banks



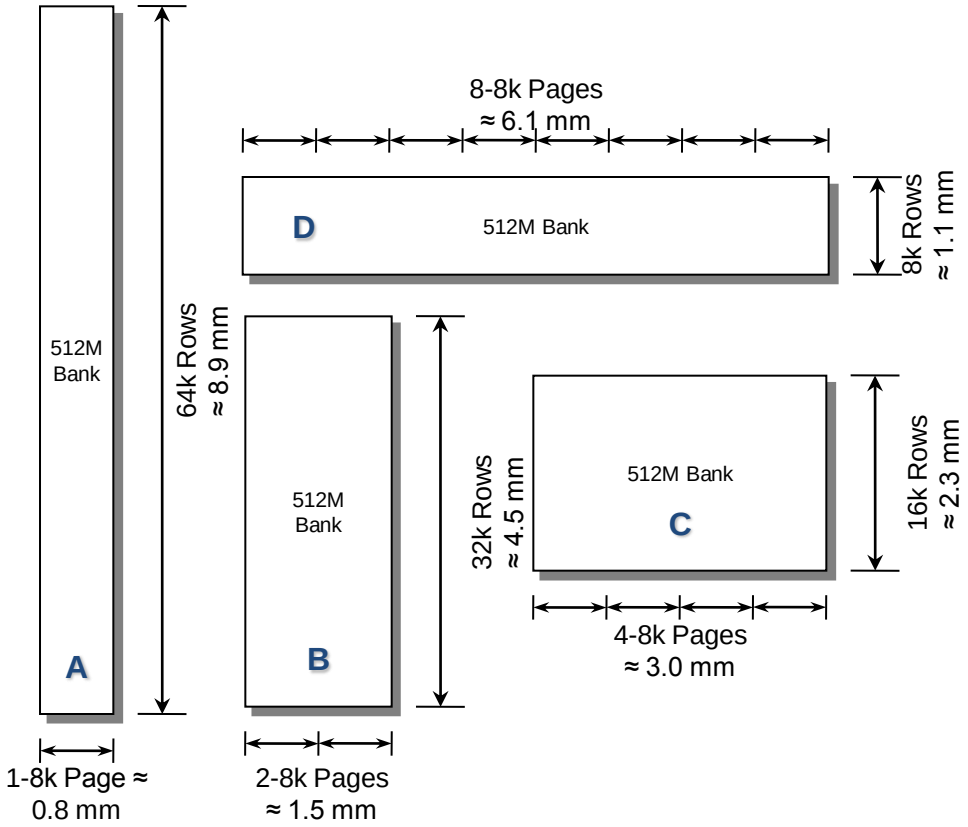
4 Gb DRAM Architecture

- 1 mm Allocation for Proximity Channel
- Buffers at the Center
  - ✓ Increase global I/O metal usage
- Array I/O Routing Reduced to 2.3 mm
- Architecture NOT Efficient for Proximity Communication
  - ✓ 6.7 mm versus 10.4 mm
  - ✓ Buffers required
  - ✓ Large metal usage



4 Gb DRAM Architecture

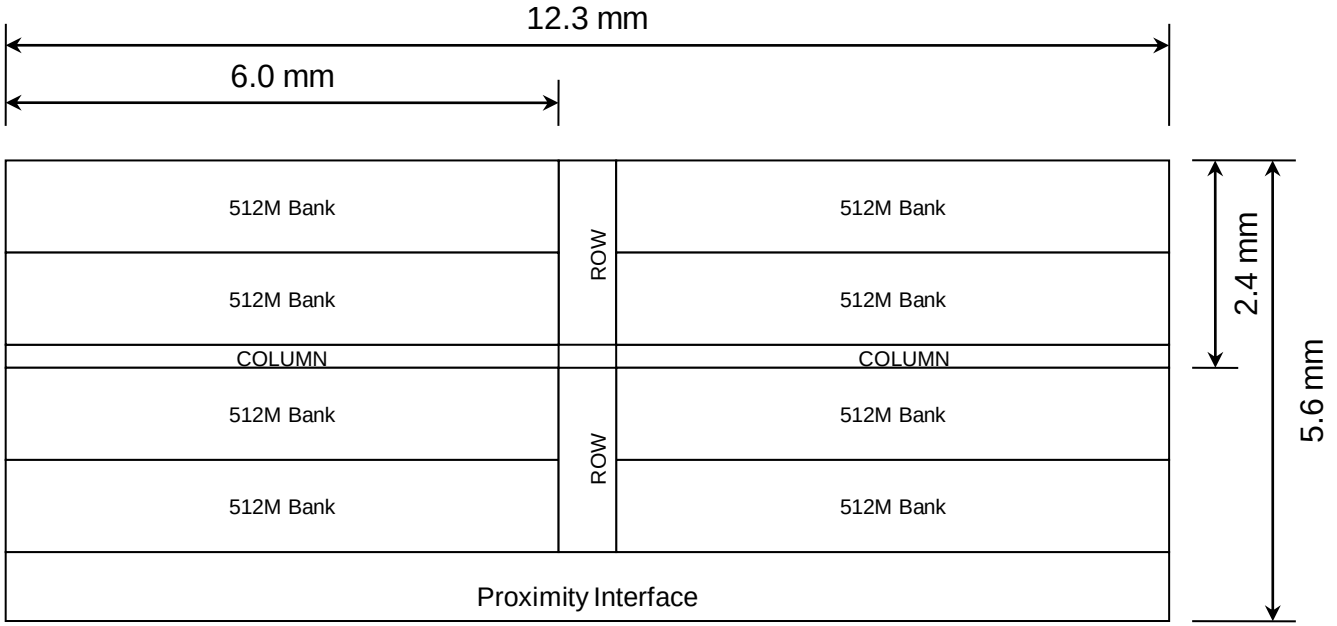
- Multiple Bank Architectures
- Page Size
  - ✓ Standard size = 8k
  - ✓ Energy efficiency
- Global Row Routing
  - ✓ ~20 ns latency
- Global Column Routing
  - ✓ ~5 ns latency
- D – Architecture
  - ✓ Page decode



Ref:[13,16,27,30,]

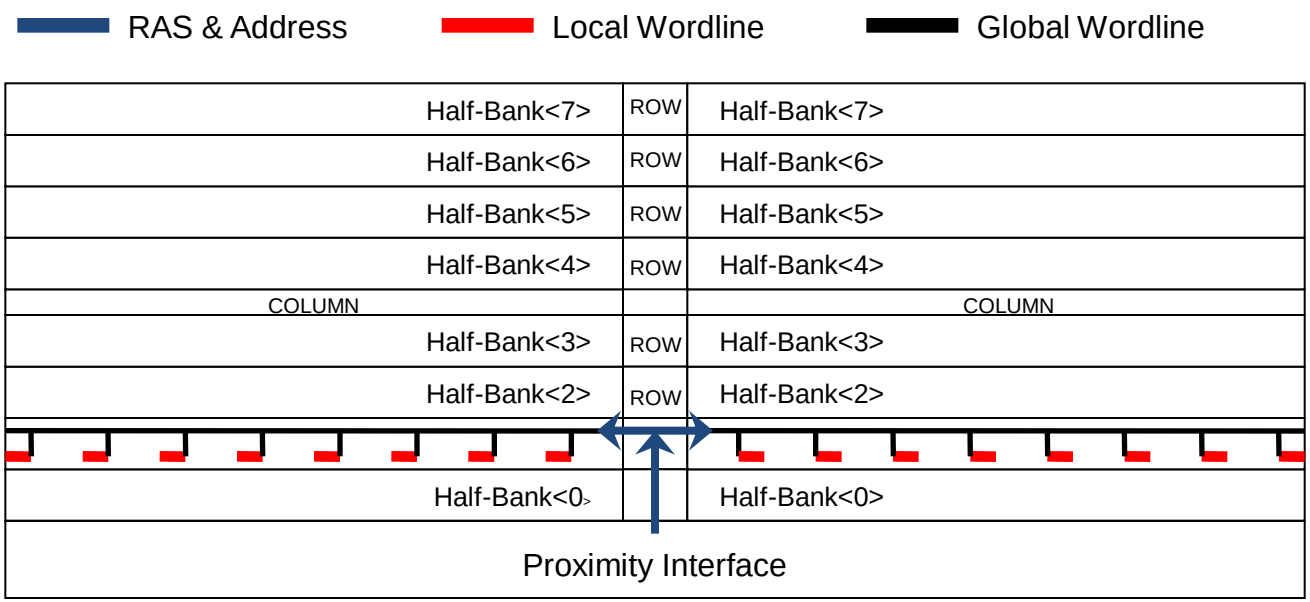
Wide I/O Chip Architecture

- Chip Size = 68.88 mm^2, Array Efficiency = 59.9%
  - ✓ Centralized row & column
  - ✓ Buffers not required
  - ✓ 12.3 mm for proximity communication
  - ✓ Enables two levels of metal



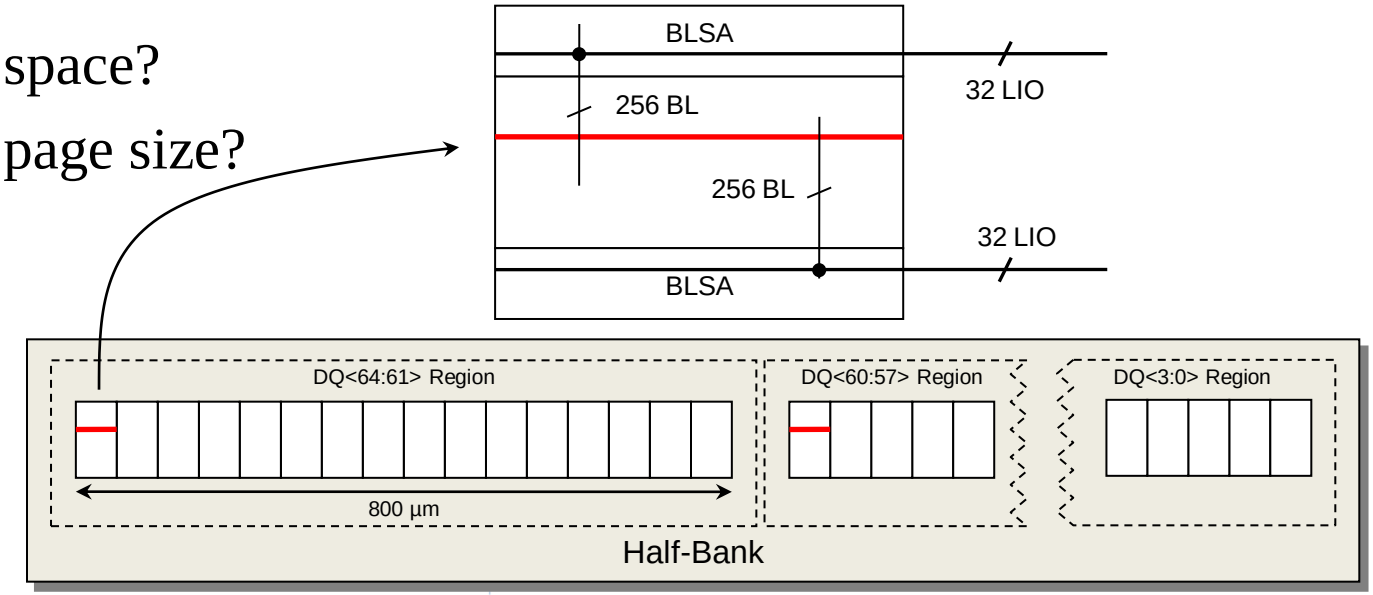
Wide I/O DRAM Architecture

- Split Bank Architecture
  - ✓ 64 bytes = 512 signals
  - ✓ 6 mm / 256 ≈ 43 µm per signal
  - ✓ 0.4 µm pitch < 1 % metal usage



Wide I/O DRAM Architecture

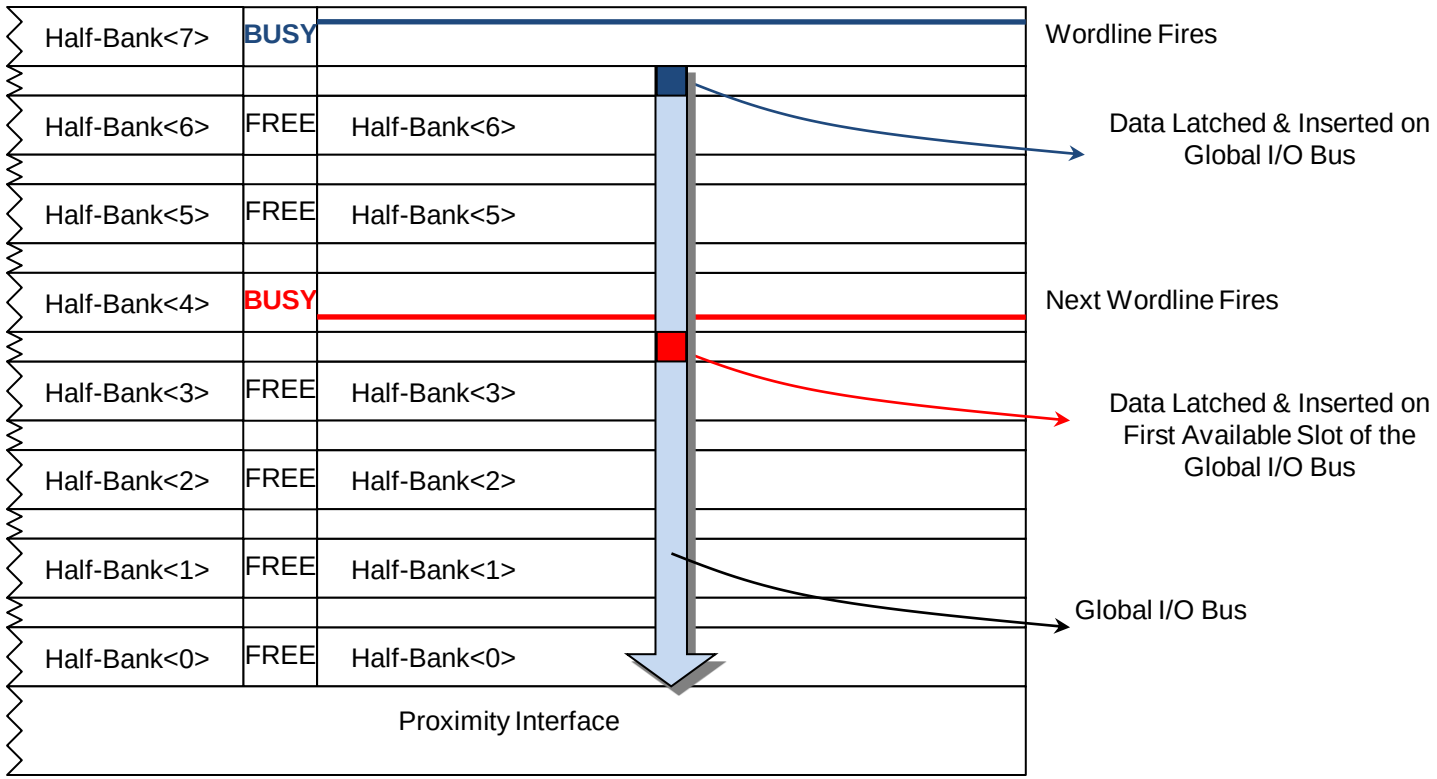
- Split Page Architecture
  - ✓ 8k page keeps current relative
  - ✓ Page decode required
  - ✓ 32 differential signals per macro
- Local I/O Routing
  - ✓ Space limited
  - ✓ Increase space?
  - ✓ Increase page size?



Ref:[12,20-24,26,28]

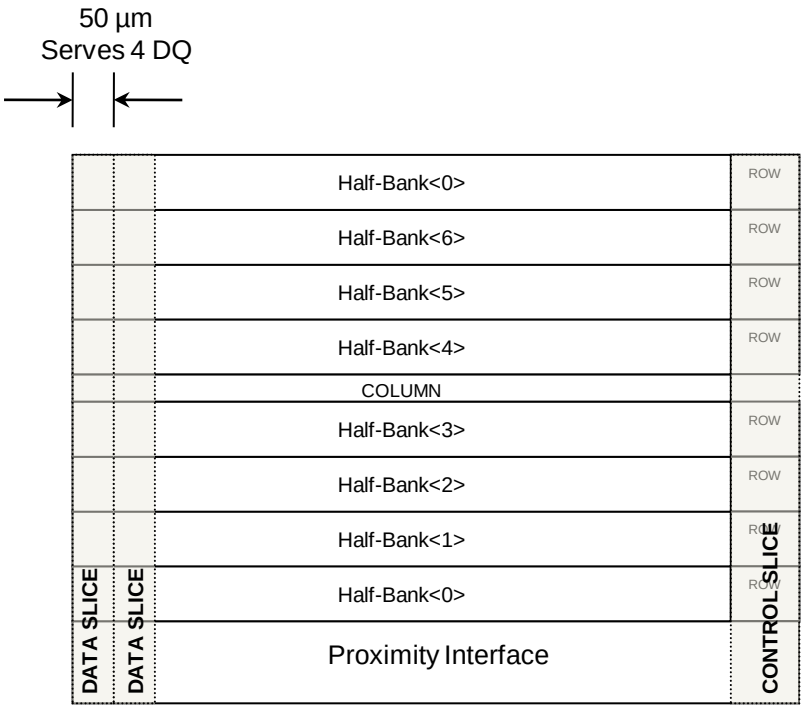
Wide I/O DRAM Architecture

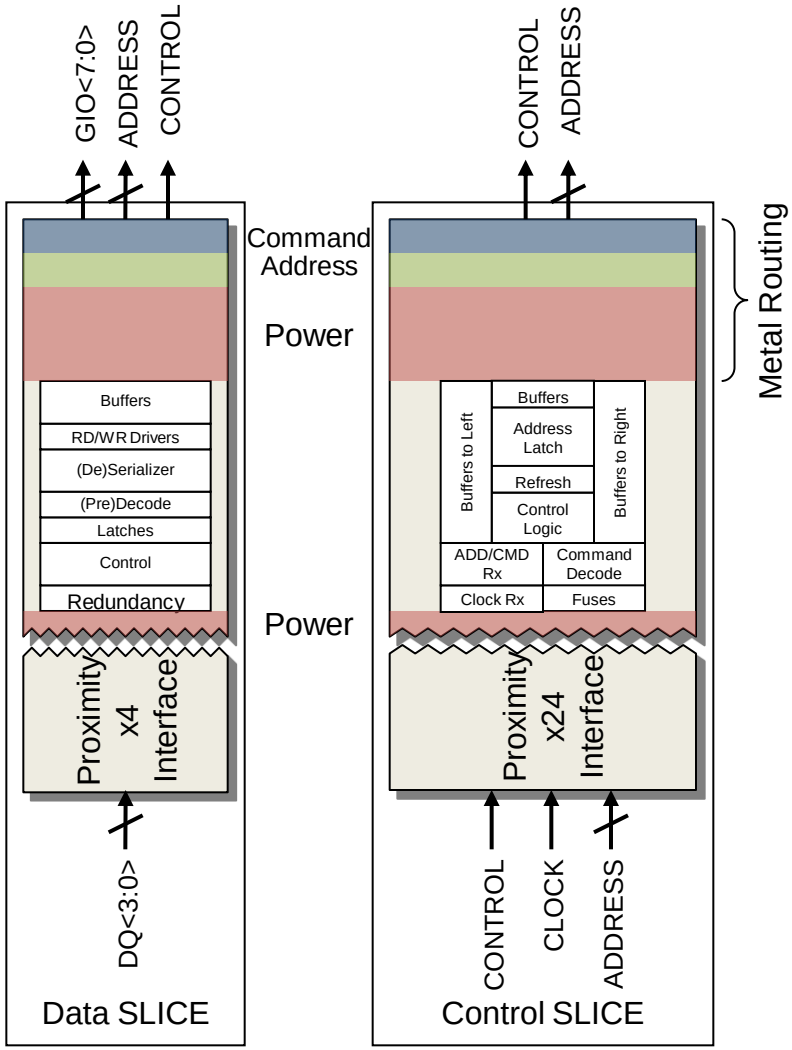
- New Column Routing
  - ✓ Global I/O operates at higher frequency
  - ✓ Protocol allows for insertion of data



Wide I/O DRAM Architecture

- Slice Architecture
  - ✓ Ease of design
    - o Uniformity, speed, verification



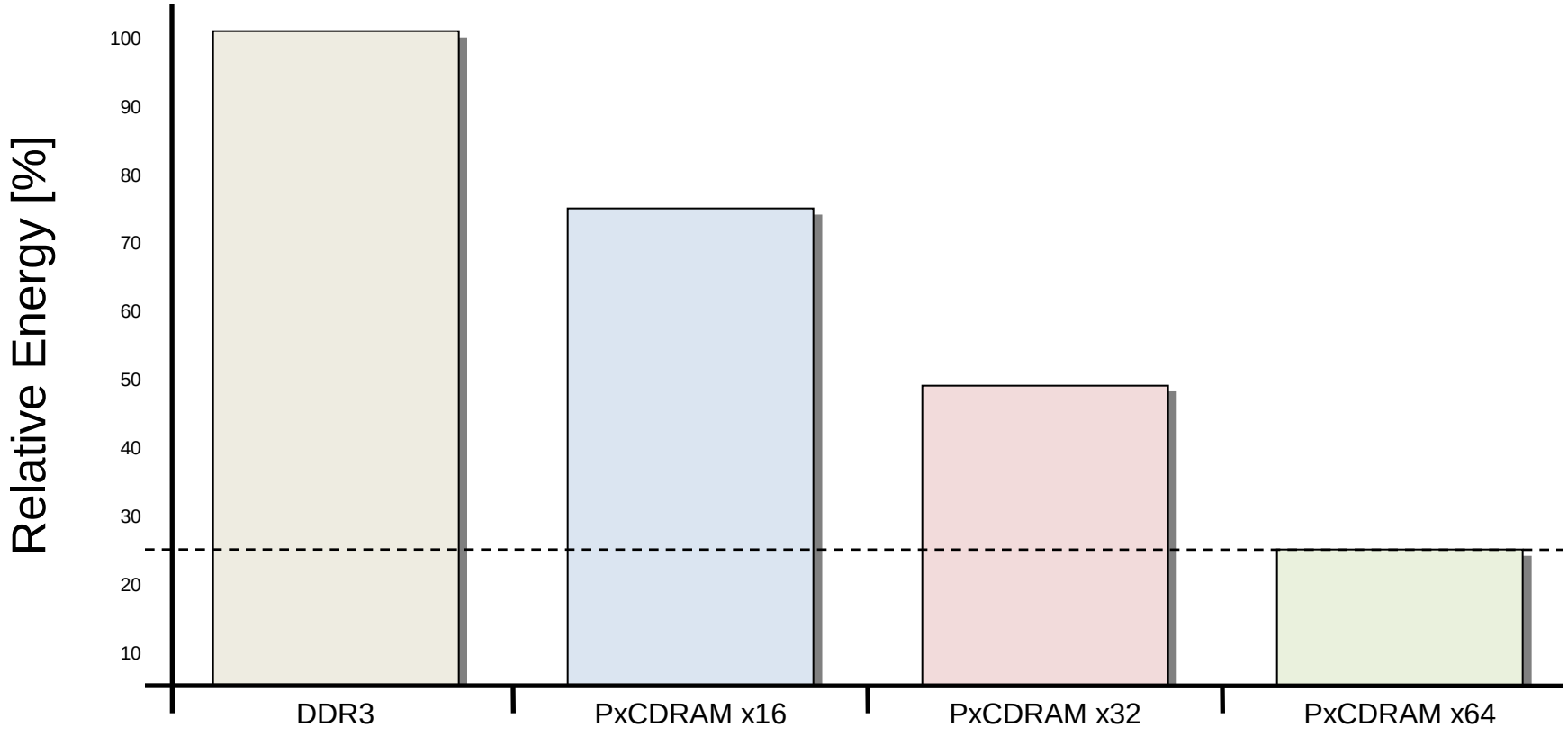


Wide I/O DRAM Architecture

- 64 Bytes per Chip
  - ✓ Significant bandwidth increase
- Power Consumption
  - ✓ Standard 8k page size
  - ✓ Split bank, split page
- Cost Performance
  - ✓ Two metals enabled for 4 Gb
  - ✓ Smaller chip size, higher array efficiency

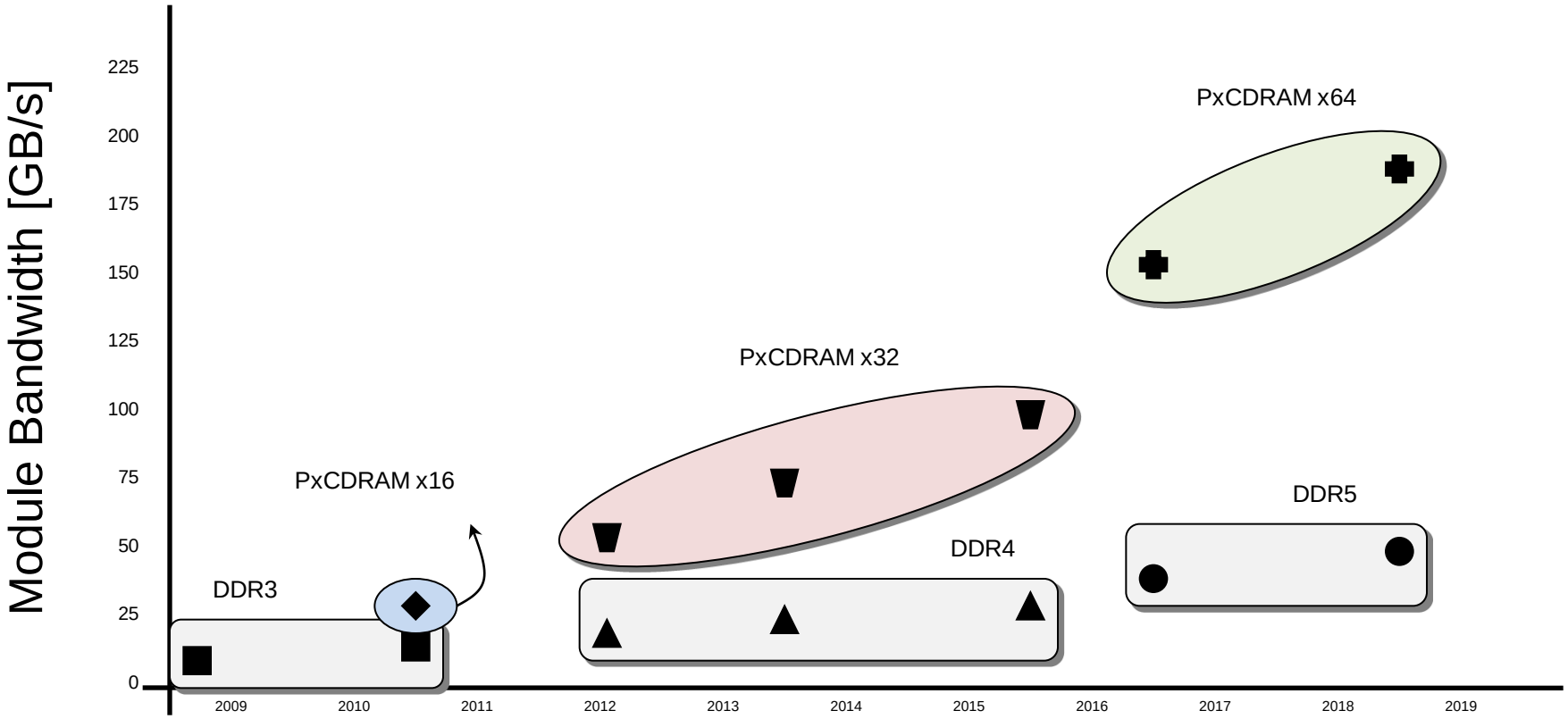
Wide I/O DRAM Architecture

- Power Consumption



Wide I/O DRAM Architecture

- Bandwidth



Future Work

- Applying Proximity Communication to New Memory Technologies
  - ✓ "High" density
  - ✓ Chalcogenide
  - ✓ Slice architecture
  - ✓ Circuit design techniques
- Local I/O Routing
  - ✓ New column global I/O structure
  - ✓ Through bitline routing
  - ✓ Novel local I/O latch

Acknowledgments

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- Ms. Donna Welch
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- Questions?

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