VARIABLE TRANSITION TIME INVERTERS IN A DIGITAL DELAY LINE WITH

ANALOG STORAGE FOR PROCESSING FAST SIGNALS AND PULSES

By

James Mellott

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University of Nevada, Las Vegas
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Department of Electrical and Computer Engineering
Howard R. Hughes College of Engineering
The Graduate College

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ABSTRACT

As the electronics industry moves forward there is an increasing need to process information faster and more accurately. High speed signals are used in scientific instrumentation, range finding devices, radar applications, and electro-optical interfaces. High-speed state of the art analog-to-digital converters are required to process these signals in real time. High frequency signals or very fast pulses are not able to be processed accurately due to either Nyquist-rate limitations or practical power consumption limits. For applications where signals are transient in nature and design size and power consumption are major factors, the proposed Variable Fast Transient Digitizer (VFTD) will be able to discretize fast signals and reproduce them with minimal signal loss. The VFTD can be coupled with micro-controllers to process these very fast signals and pulses that operate in the gigahertz (GHz) range, while minimizing static power consumption and package size [1].

The VFTD designed is an application specific integrated circuit (ASIC) that can capture and store a high-speed analog input signal at a variable rate. The stored signal can be replicated at a slower rate, also adjustable, for user specific applications. The reconstruction process is adjustable to allow for interfacing with different microprocessors that vary across a range of operating frequencies and costs. This implementation of the VFTD utilizes 256 on-chip capacitors to store the data. Experimental results show the fastest rate of capture to be roughly 3.16 GHz, or 316 ps per stage, with slower rates of capture dependent upon off-chip bias resistors values. The capture rate and number of stages determine the overall capture window. For example, with 256 stages and 316 ps per stage the total capture window is roughly 81 ns, and with 6.25 ns per stage the capture window is roughly 1.59 us. The variable control and off-chip resistor allow for user

and application specific modifications. The 256-stage VFTD can be implemented on a chip in a 0.5 mm x 1.5 mm area. The VFTD integrated circuit (IC) used for testing was fabricated by MOSIS using On Semiconductor's C5 Process.

ACKNOWLEDGEMENTS

DEDICATION

I would personally like to dedicate this Thesis to my wife Jessica Mellott. Without your love and support I would not be where I am today. The last 10 years of my accomplishments would not have been possible if I did not find you. I cannot thank you enough for all the sacrifices you have made for me. You shaped me to be the man I am today. I hope to be as good to you as you are to me. I love you Jessica.

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Chapter 1 Introduction

As circuits and components in modern electronics continue to decrease in size and subsequently increase in speed, the need to develop inexpensive, fast and efficient methods to capture and process information increases. Specifically, the ability to capture and analyze transient and high-speed analog signals is a common goal shared in a multitude of fields. These analog signals are used for a variety of applications including, but not limited to, telecommunications, electro-optics, photonics, and many application-specific integrated circuit (ASIC) designs. Typically, modern implementations that deal with such signals use high-speed analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and various filters. These components tend to be bulky, expensive, consume excessive power, or have very specific operating frequencies. Modern detection systems use thresholds to trigger an event, wherein the proposed Variable Fast Transient Digitizer (VFTD) will allow complete analyzation of the captured signal, rather than generating a pulse once a threshold has been reached.

The Fast Transient Digitizer (FTD) introduced by Buck and Baker [1] was developed to address the need for a way to efficiently capture transients or high-speed analog signals. Along with capturing these signals, the FTD can reproduce a slowed or stretched out version of the captured signal with minimal loss of the original signal. With the FTD, the captured signal can be analyzed to gain more information about what was captured. The FTD eliminated the need for ADCs, DACs, and additional filters, such as reconstruction and anti-aliasing filters. The FTD's capture sequence behaves like 128 sequential track and hold sampling circuits [2]. Consider Figure 1.1 for a brief example of the how the track and hold circuit operates.
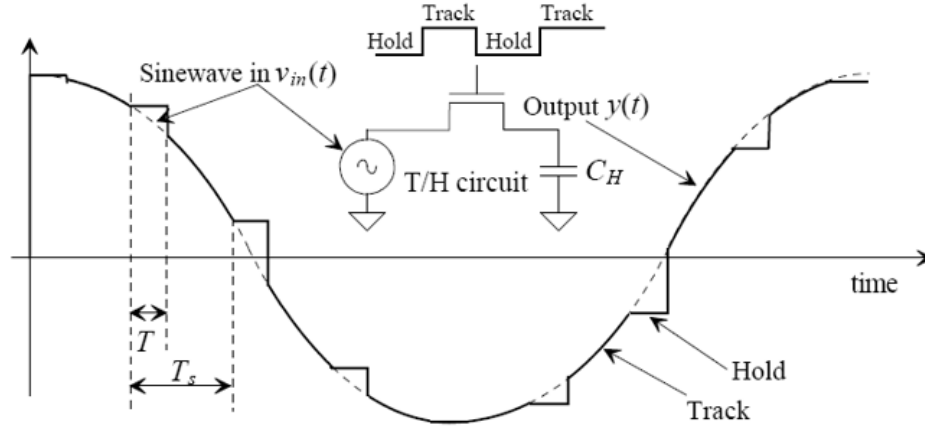
Figure 1.1: Track and Hold operation [2]

In the FTD design, N-Channel MOSFET (NMOS) devices act as switches for 128 sequential circuits controlled through a basic inverter delay line consisting of two identically sized inverters per capture stage. The amount of delay through two basic inverters in the delay line is equivalent to T_s in Figure 1.1. This time delay gives the effective sampling rate of the FTD, measured at 5 GHz using On Semiconductor's C5 process [3]. One of the major drawbacks of this implementation is the lack of variability in the capture rate that limits the number of useful applications of the design.

The proposed Variable Fast Transient Digitizer (VFTD) aims to address the need for a variable sampling rate in the FTD design by implementing a current starved inverter in place of the first basic inverter in each capture stage. The current starved inverters will be controlled with a DC bias voltage generated from an on-chip bias generator. The bias generator, a voltage-controlled beta multiplier, will be controlled via an off-chip voltage source. The voltage will adjust the time delay between 256 sequential capture stages and can be adjusted for application specific needs. The design and operation of all the components comprising the VFTD will be discussed in detail in chapter 2.

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As an example of how adding variability to the FTD will increase the number of useful applications, consider optical range finders. Used in this type of an application, the FTD will only operate in a short time window since the number of stages and the sampling rate set this range. If the sampling rate were variable, as implemented in the VFTD design, the FTD could operate over a wider time range. An optical range finder utilizing a VFTD would allow the device to capture and analyze signals at distances that would not be possible otherwise. Once the signal has been received from a far distance, the bias generator can be adjusted to a higher voltage, thus allowing the circuit to capture with high resolution for close range acquisition. Consequently, the addition of the current starved inverters increases the useful applications of the FTD. The design of the VFTD allows for capture rates between hundreds of MHz and 3 GHz, as compared to the FTD operating at the single sampling rate of 5 GHz.

The following chapters will cover the design, simulations, layout, and test results of the VFTD. Chapter 2 will go over the design of the individual components and their simulation results as well as a complete 256 capture stage design. Chapter 3 will cover the layout and design considerations of the individual components and the entire chip. Chapter 4 will discuss the PCB design and test results of the completed project. Chapter 5 will include the conclusion and future works of the VFTD. All of the layouts and simulations were generated using Cadence Electronic Design Automation (EDA) Software utilizing the On Semiconductor C5 CMOS Process Design Kit (PDK).

Chapter 2 VFTD Design Components

Chapter 2 provides a description of the function and design of the individual components constituting the VFTD design, as well as the composite 256 capture stage design. Section 2.1 discusses the bias generator circuit, Section 2.2 details the delay line unit cell, and Section 2.3 describes the capture stage unit cell. Section 2.4 combines these components into the 256 stage VFTD design and demonstrates the fundamental operation with a comparison of calculated and simulated results.

2.1 Bias Generator

The bias voltages are generated using a DC bias generator, a voltage-controlled beta multiplier voltage reference. The bias generator design, Figure 2.1, was selected due to its inherent ability to remain stable with variations in temperature. Referencing Figure 2.1, *vinvc* will set the current through NMOS, *N1*, acting as a proportional to absolute temperature reference (PTAT), while the resistor connected to the source of *N1* acts as the complementary to absolute temperature reference (CTAT). The P-Channel MOSFET PMOS, *P1*, is a gate-drain connected device, therefore the current set by *N1* flows through *P1* and is also mirrored over to *P0*. *N0* is also gate-drain connected, thus the current through *N0* will match that of *P0*. The bias voltage nodes are taken from the gates of the 0th devices, labeled *vbiasp* for the PMOS bias voltage, and *vbiasn* for the NMOS bias voltage.
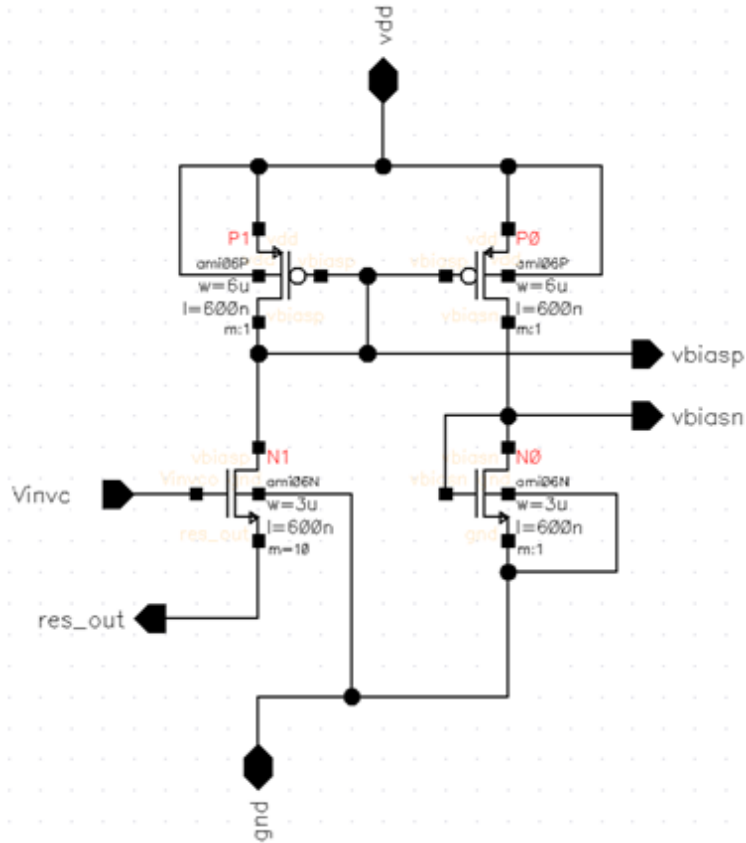
Figure 2.1 Voltage-Controlled Beta Multiplier

The simulation results seen in Figures 2.2-2.4 will demonstrate how the bias generator operates with different off-chip bias resistors, labeled *res_out* in Figure 2.1. The goal is to obtain a wide range of linearity for linear adjustments in the sampling rates, as well as the ability for the voltage reference to remain stable over a wide temperature range. First, Figure 2.2 shows the simulation results for a DC sweep of *vinvc* using a 4 kOhm resistor. As can be seen, the linear range of adjustment region is from approximately 1 Volt to 3.5 Volt.
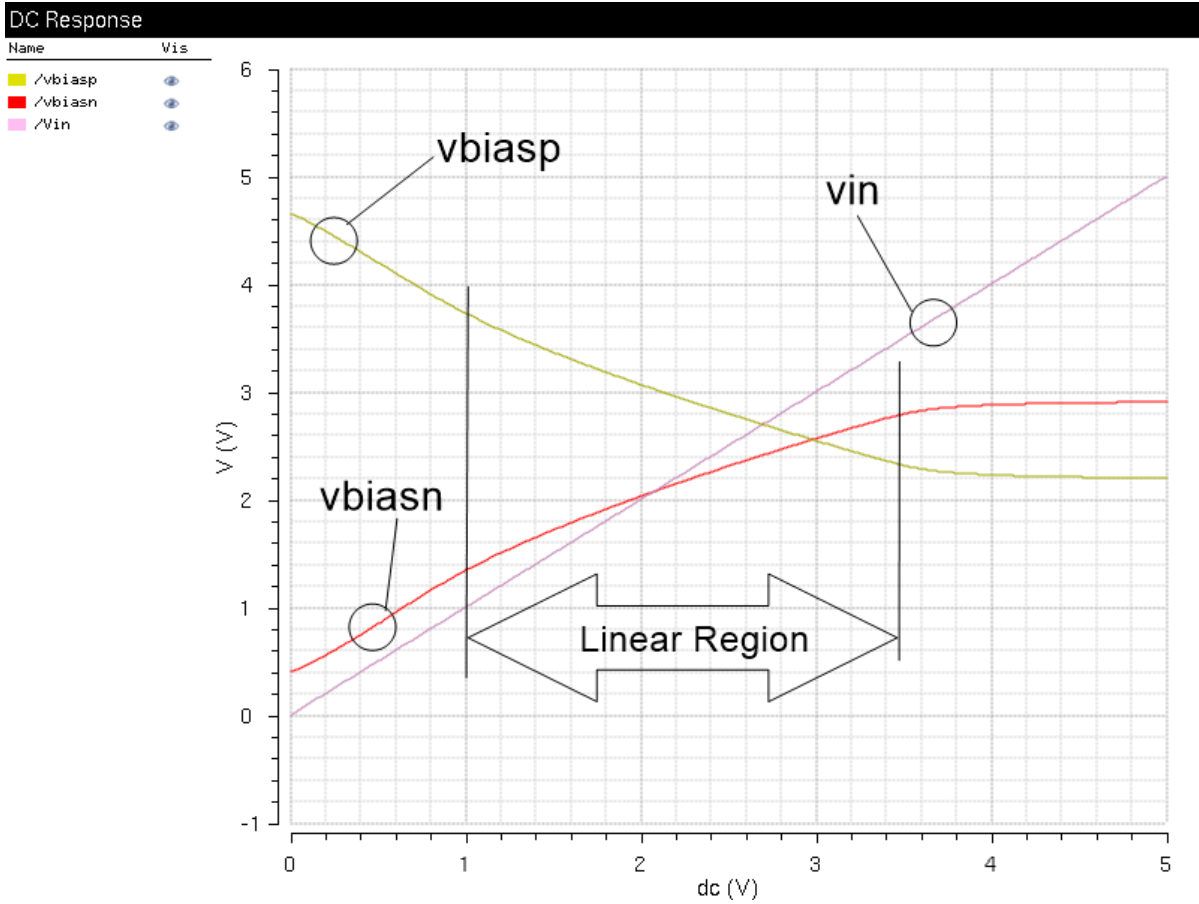
Figure 2.2 DC Sweep with 4 kOhm Resistor

Next, Figure 2.3 displays the results of the same simulation with a 2 kOhm bias resistor. The linear range of *vbiasn* and *vbiasp* is now from 1 Volt to 3 Volts. Decreasing the bias resistor value allows more current to flow and increases the bias voltage range, but the tradeoff is a reduction in the linear adjustment region when compared to the simulation results from Figure 2.2.
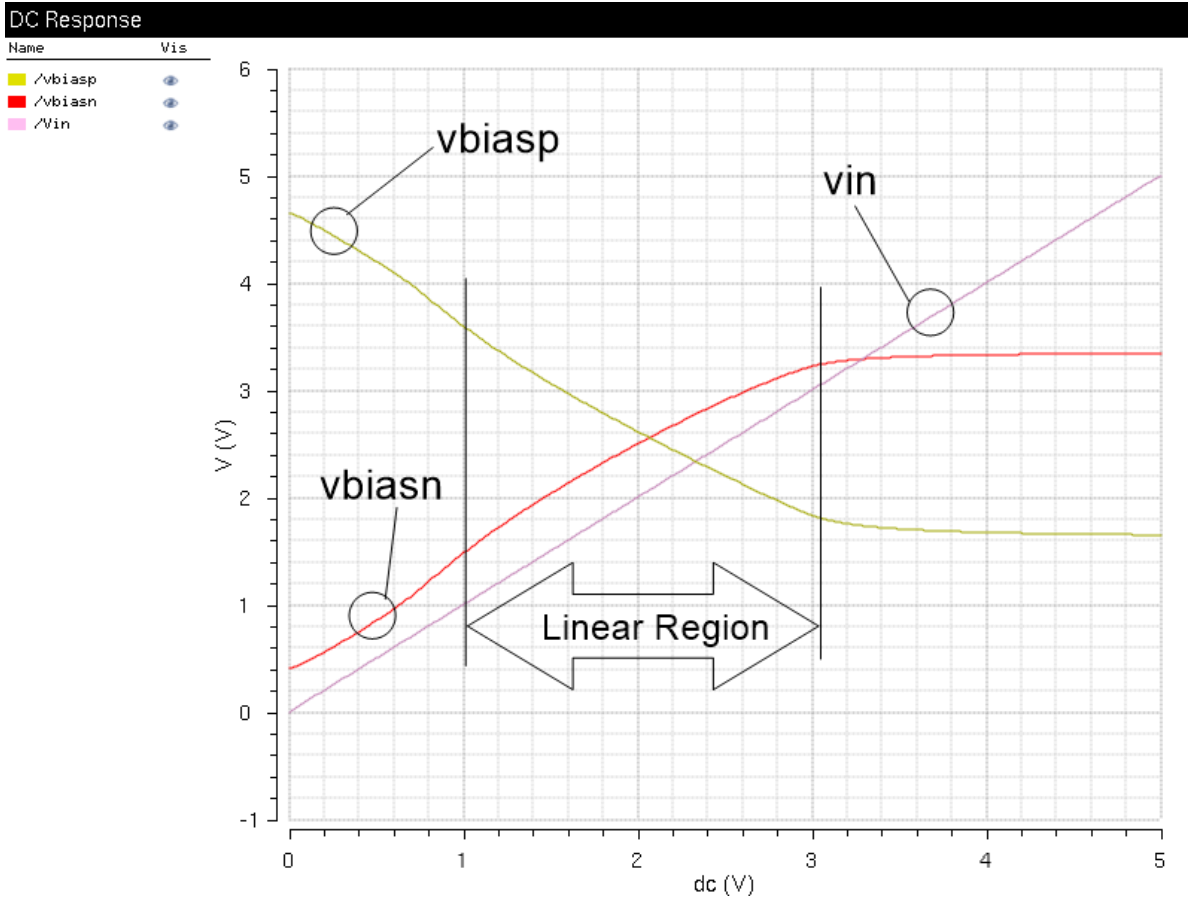
Figure 2.3 DC Sweep with 2 kOhm Resistor

The simulation to generate Figure 2.2 was performed with a temperature variation from 0 ºC to 100 ºC in 25 ºC increments. The goal is to have the current remain constant for each temperature increment. The effects of temperature on *N1*, the PTAT reference, are counteracted by the effects of temperature on the resistor, the CTAT reference. This means that as the properties of *N1* change, the resistor will keep the current flow through the device the same over varying temperatures. To clarify, as temperature changes the mobility and the threshold voltage of the MOSFETs change. For example, as temperature increases the threshold voltage of the NMOS will decrease and electron mobility increases. The PMOS has the opposite effect with increasing temperature where threshold voltage increases and hole mobility decreases. As can be seen from the simulation results in Figure 2.4, *vbiasn* remain stable across a wide range of temperature

changes due to the complementary behavior of the PTAT and CTAT references and *vbiasp* decreases, or turns on more, as temperature increases, to maintain the correct amount of current flow as temperature increases. Most importantly, the current flow in the linear adjustment region remains relatively constant.
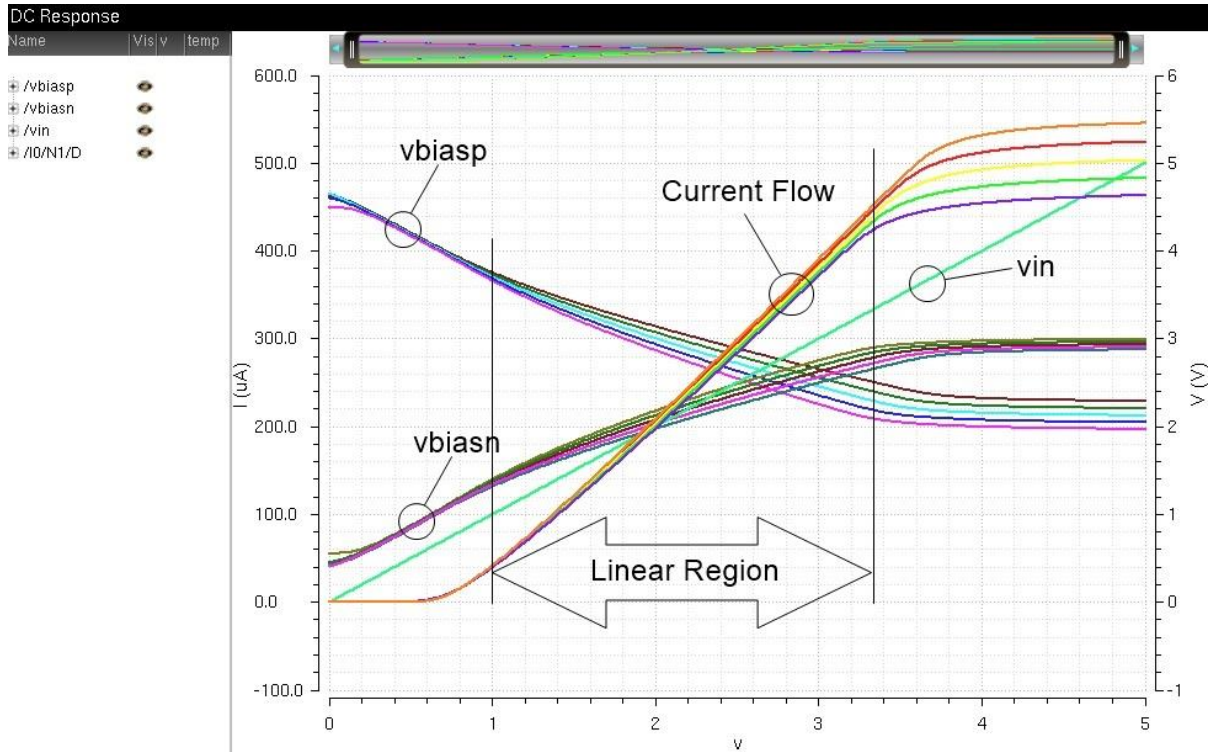
Figure 2.4 Temperature Sweep with 4 kOhm Resistor

Table 2.1 contains the consolidated bias generator results. Adjusting *vinvc* or the bias resistor impedance, or a combination of both, allow for control over the bias voltages for the current starved inverter that will be discussed in section 2.2.

Vinvc (V)	Bias Resistance (Ω)	Vbiap (V)	Vbiasn (V)
5	4k	2.20	2.90
5	2k	1.65	3.34
1	4k	3.73	1.34
1	2k	3.60	1.48

Table 2.1: Bias Generator Results Table

2.2 The Delay Line Unit cell

The VFTD delay line unit cell, referred to as 'delay element', consists of a current starved inverter followed by a basic inverter, as discussed in Chapter 1. Before explaining how a current starved inverter operates, a brief summary of the basic inverter is presented. A basic inverter consists of a PMOS and an NMOS arranged as seen in Figure 2.5(a). The current starved implementation can be seen in Figure 2.5(b). The inverter receives an input signal, either a logic 0, defined as ground, or a logic 1, defined as VDD. After some time delay, the inverter outputs the opposite of the input. For example, a logic 0 input results in a logic 1 output. The simplicity of the inverter is the time delay can be modeled as a simple RC circuit, discussed later, thus making the time delay predictable.
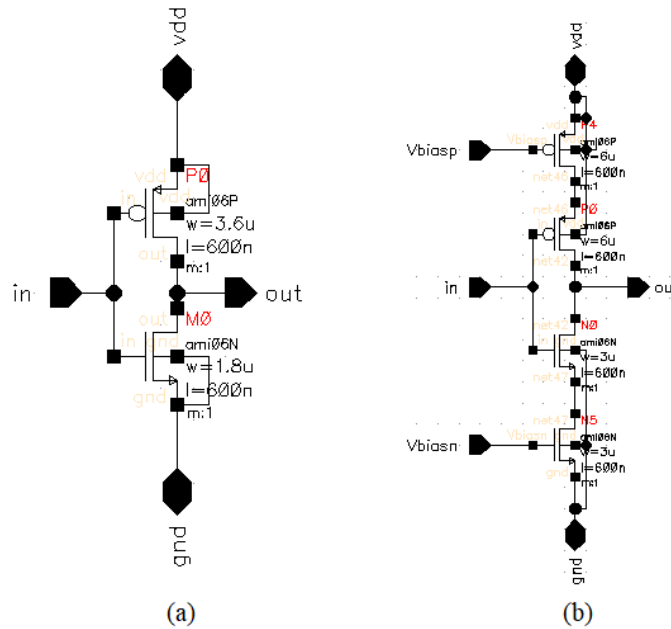
Figure 2.5 (a) Basic Inverter; (b) Current Starved Inverter

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The difference between a basic inverter and a current starved inverter is the addition of an extra NMOS and PMOS, Figure 2.5(b). The top PMOS, *P4* functions as a current source and the bottom NMOS, *N5*, acts as a current sink. The current starved inverter uses the bias voltages, *vbiasn* and *vbiasp*, generated by the bias generator. The generated bias voltages are used to limit the current flow through the inverter and that in turn sets the time delay. The delay element, Figure 2.6, uses the current starved inverter to add the desired variability followed by the basic inverter to generate a faster transitioning edge. A sharp edge is desired for more accurate control over the captured signal, as well as a sharp signal for the input to the next current starved inverter. Stringing several delay elements together comprises the voltage-controlled delay line. The time difference between the input signal and the output signal can be increased or decreased with adjustments of *vinvc* or the bias resistor. The delay element will be a component within each capture stage unit cell, discussed in Section 2.3, to control the NMOS serving as the hold capacitor's switch.
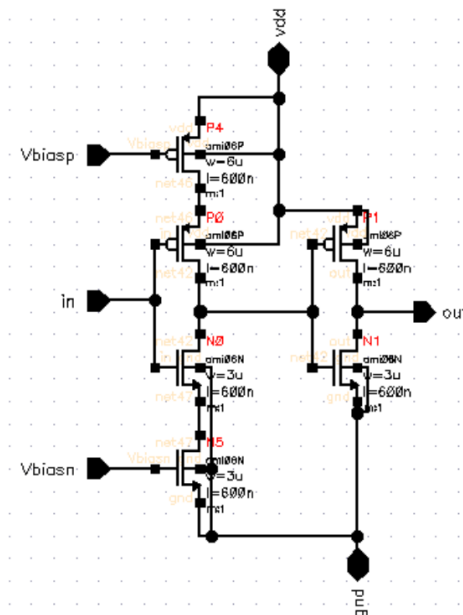
Figure 2.6 Delay Element with Current Starved Inverter

Due to the effective switching resistances, $R'_{n,p,}$ and parasitic capacitances, C_{oxn} and C_{oxp}, associated with MOSFETs, the time delay through a delay element can be modeled as a traditional RC delay defined by [4]

$$t_d = 0.693 * RC \approx 0.7RC \qquad\qquad Eq(2.1)$$

The resistance is given as [4]

$$R_{n,p} = \frac{VDD}{I_{D,sat}} = R'_{n,p}\frac{L}{W} \qquad\qquad Eq(2.2)$$

or solving for $R'_{n,p}$ [4]

$$R'_n = \frac{VDD}{I_{D,sat}} * \frac{W_n}{L_n} \text{ and } R'_p = \frac{VDD}{I_{D,sat}} * \frac{W_p}{L_p} \qquad\qquad Eq(2.3)$$

where W and L are the width and length of the devices, respectively.

The short-channel devices used in the C5 process do not follow the square-law, therefore to estimate R'_n, and R'_p Cadence simulations were performed to estimate the effective switching resistance. Setting the value on the gate of an NMOS to 5 Volts and sweeping VDD from 0 to 5 Volts, R_n can be calculated by taking the inverse of the slope of the line created between 0 and 5 Volts. Figure 2.7 shows the simulation results used for determining R_n.
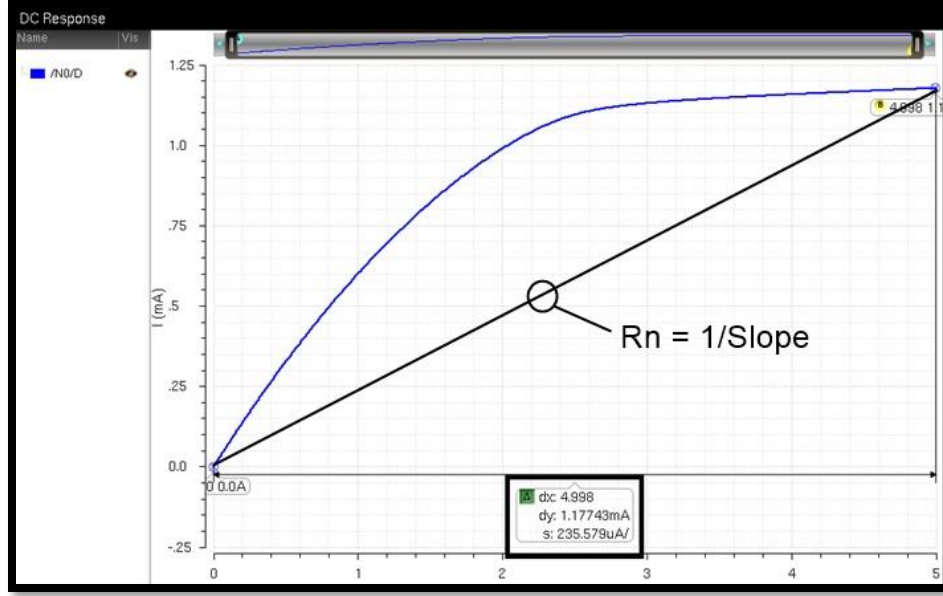
Figure 2.7 Simulation to Determine *Rn*

Therefore, R'_n can be calculated as

$$R'_n = \frac{VDD}{I_{D,sat}} * \frac{W_n}{L_n} = \frac{4.998V}{1.177mA} * \frac{3\mu m}{0.6\mu m} = 21.223k\Omega$$

In the C5 process, hole mobility is approximately half the electron mobility [3]. This requires a 2:1 ratio for a PMOS and an NMOS to have the same drain current. Therefore, using this ratio, we can approximate R'_p as

$$R'_p = 2 * R'_n = 42.447k\Omega$$

To continue building the RC model, the total capacitance, C_{total}, is defined by [5]

$$C_{tot} = \frac{3}{2} * \left(C_{oxn} + C_{oxp} \right) + C_{oxn} + C_{oxp} = \frac{5}{2} * \left(C_{oxn} + C_{oxp} \right) \qquad Eq(2.4)$$

The oxide capacitance of a MOSFET can be determined as [4]

$$C_{ox} = C'_{ox}WL \qquad\qquad Eq(2.5)$$

where C'_{ox} represents the oxide capacitance per unit area given as 2.5 fF/μm^2 in the C5 Process

[3] and t_{ox} is roughly 14nm. Using Eq. (2.5), the parasitic MOSFET capacitances, C_{oxn} and C_{oxp},

are then defined by

$$C_{oxn} = 2.5\frac{fF}{\mu m^2} * 3\mu m * 0.6\mu m \approx 4.5fF \qquad\qquad Eq(2.6)$$

$$C_{oxp} = 2.5\frac{fF}{\mu m^2} * 6\mu m * 0.6\mu m \approx 9fF \qquad\qquad Eq(2.7)$$

Using the values for C_{oxn} and C_{oxp} in Eq. (2.4) results in

$$C_{tot} = \frac{5}{2} * (4.5fF + 9fF) \approx 33.75fF$$

Now that $R'_{n,p}$ and $C_{oxn,p}$ have been determined, the time delay for the delay element can be

determined. The time the signal takes to transition from logic 0 to logic 1, low-to-high, is given

as [4]

$$t_{plh} = 0.7\, R'_p \frac{L_p}{W_p} C_{tot} \qquad\qquad Eq(2.8)$$

$$0.7 * 42.447k\Omega * \frac{0.6\mu m}{6\mu m} * 33.75fF \approx 100.28ps$$

with the transition from high-to-low given by [4]

$$t_{phl} = 0.7\, R'_n \frac{L_n}{W_n} C_{tot} \qquad\qquad Eq(2.9)$$

$$0.7 * 21.223k\Omega * \frac{0.6\mu m}{3\mu m} * 33.75fF \approx 100.28ps$$

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The total delay through an individual unit cell can be approximated as [4]

$$t_d = t_{plh} + t_{phl} \qquad\qquad Eq(2.10)$$

$$100.28ps + 100.28ps \approx 200.56ps$$

for a sampling frequency of

$$f_{sample} = \frac{1}{t_d} \qquad\qquad Eq(2.11)$$

$$\frac{1}{200.56ps} \approx 5GHz$$

Figures 2.8-2.11 show transient simulation results for the schematic in Figure 2.6 with four different bias voltages generated using the bias generator, Figure 2.1, and a 2 kOhm resistor. The goal of these simulations is to demonstrate how adjusting the voltage of the bias generator will allow for time delay adjustment through each delay element, thus varying the sampling rate of the VFTD. The red trace is the input voltage, *in*, the green trace is the voltage output of the current starved inverter, and the blue trace is the basic inverter output, *out*. The simulations all vary the input voltage to the bias generator with the input voltage *vinvc* set to 5 Volts, 3 Volts, 2 Volts, and 1 Volt, respectively. The results in Figures 2.8-2.11 demonstrate how the current starved inverter output can be controlled. Note how the basic inverter generates a sharper signal, *out,* than the current starved inverter output. This is necessary for better control over capturing the analog input signal and providing a sharp input signal, *in,* for the next delay element.

Figure 2.8 shows the simulation results for *vinvc* set to 5 Volts. Again, the red trace is the input voltage, *in*, the green trace is the voltage output of the current starved inverter, and the blue trace is the basic inverter output, *out*. As can be seen, the current starved inverter transition time, red to green, is roughly 150 ps and the inverter transition time, green to blue, is roughly 70 ps.
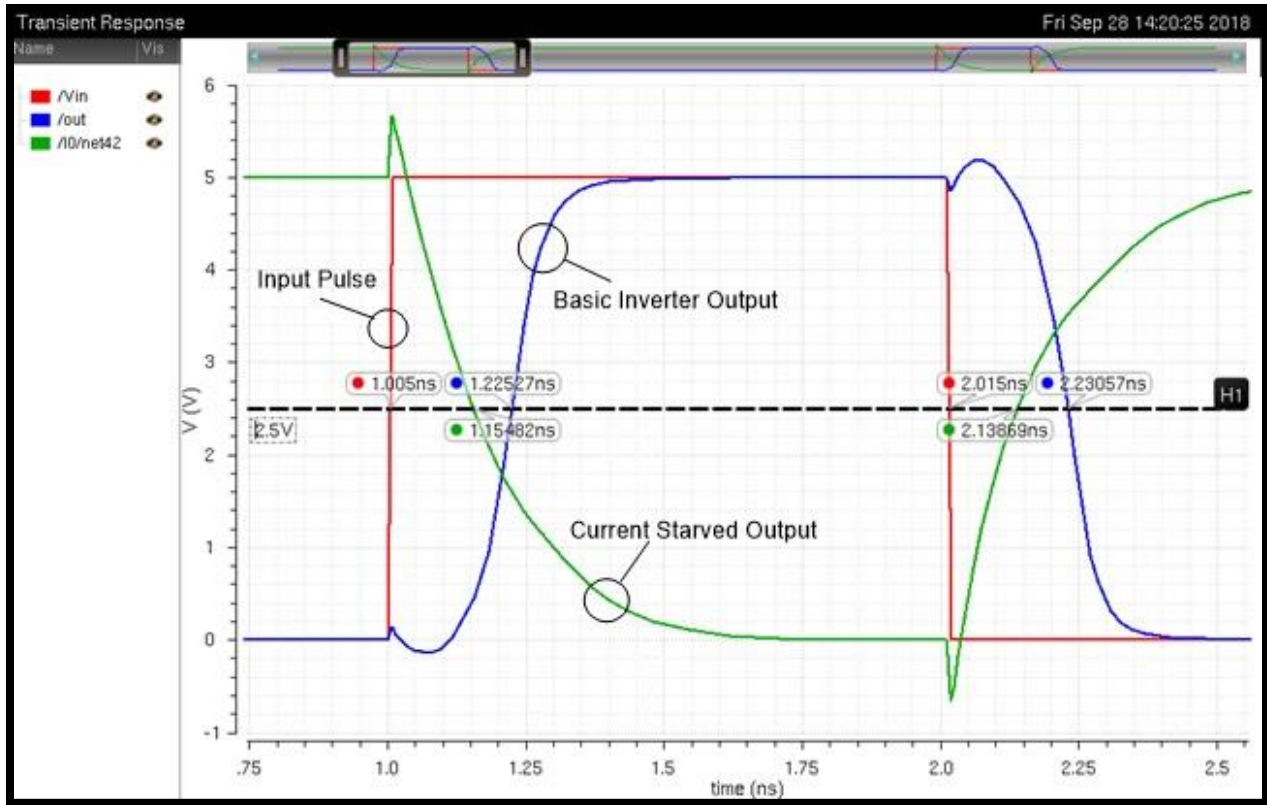
Figure 2.8 Transient Simulation of Figure 2.1 with Figure 2.6 with 5 Volts on *vinvc*

Figure 2.9 shows the simulation results for *vinvc* set to 3 Volts. As can be seen, the current starved inverter transition time, red to green, is roughly 150 ps and the inverter transition time, green to blue, is roughly 70 ps. It is also clear to see the basic inverter provides a sharper signal, the blue trace, when compared to the green trace.

Figure 2.9 Transient Simulation of Figure 2.1 with Figure 2.6 with 3 Volts on *vinvc*

Next, Figure 2.10 contains results for *vinvc* set to 2 Volts. Now, the current starved inverter transition time is roughly 200 ps and the inverter transition time is roughly 80 ps. As expected from the bias generator simulation results, adjusting *vinvc* to 3 Volts from 5 Volts has almost no impact on the transition times. Again, it is also clear to see that the inverter provides a sharper signal.
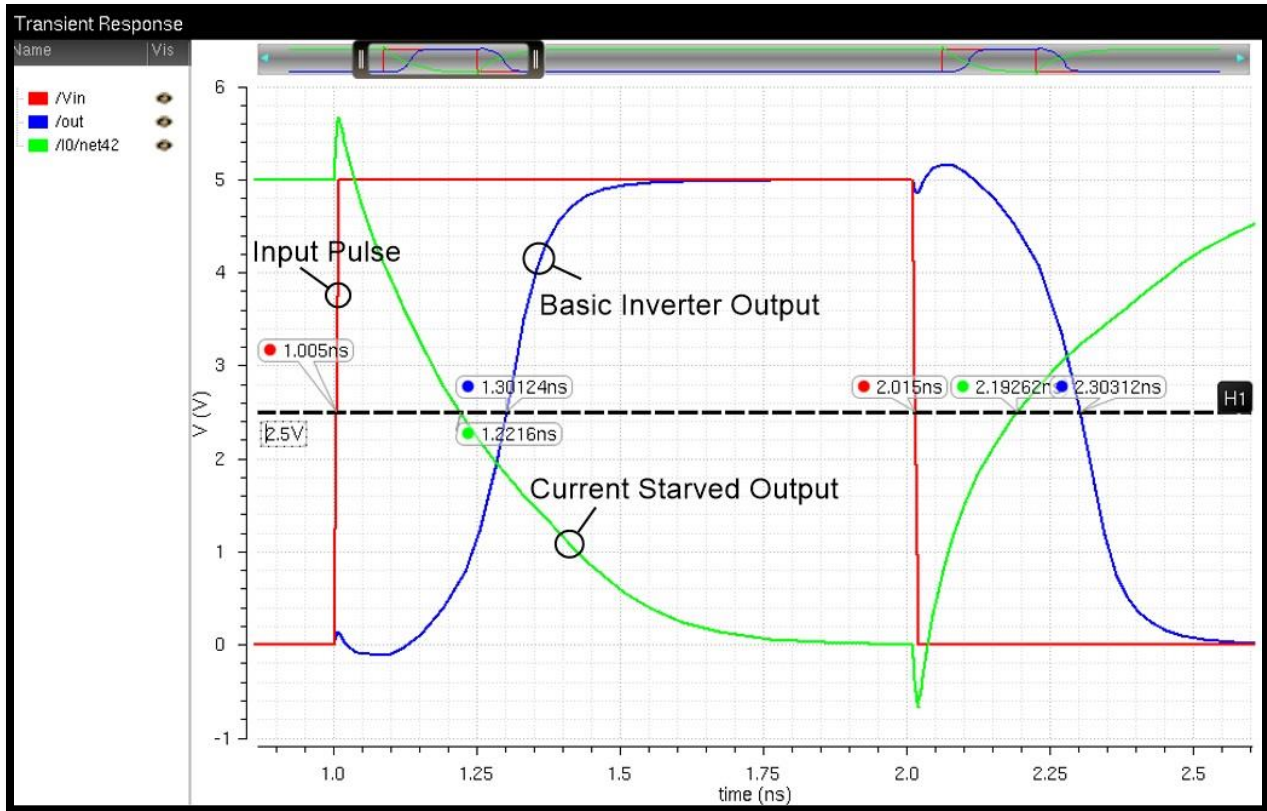
Figure 2.10 Transient Simulation of Figure 2.1 with Figure 2.6 with 2 Volts on *vinvc*

The results for *vinvc* set to 1 Volt are seen in Figure 2.11 with a current starved inverter transition time of roughly 700 ps and a basic inverter transition time of roughly 80 ps. It is also clear to see how the basic inverter still provides a sharper signal edge.
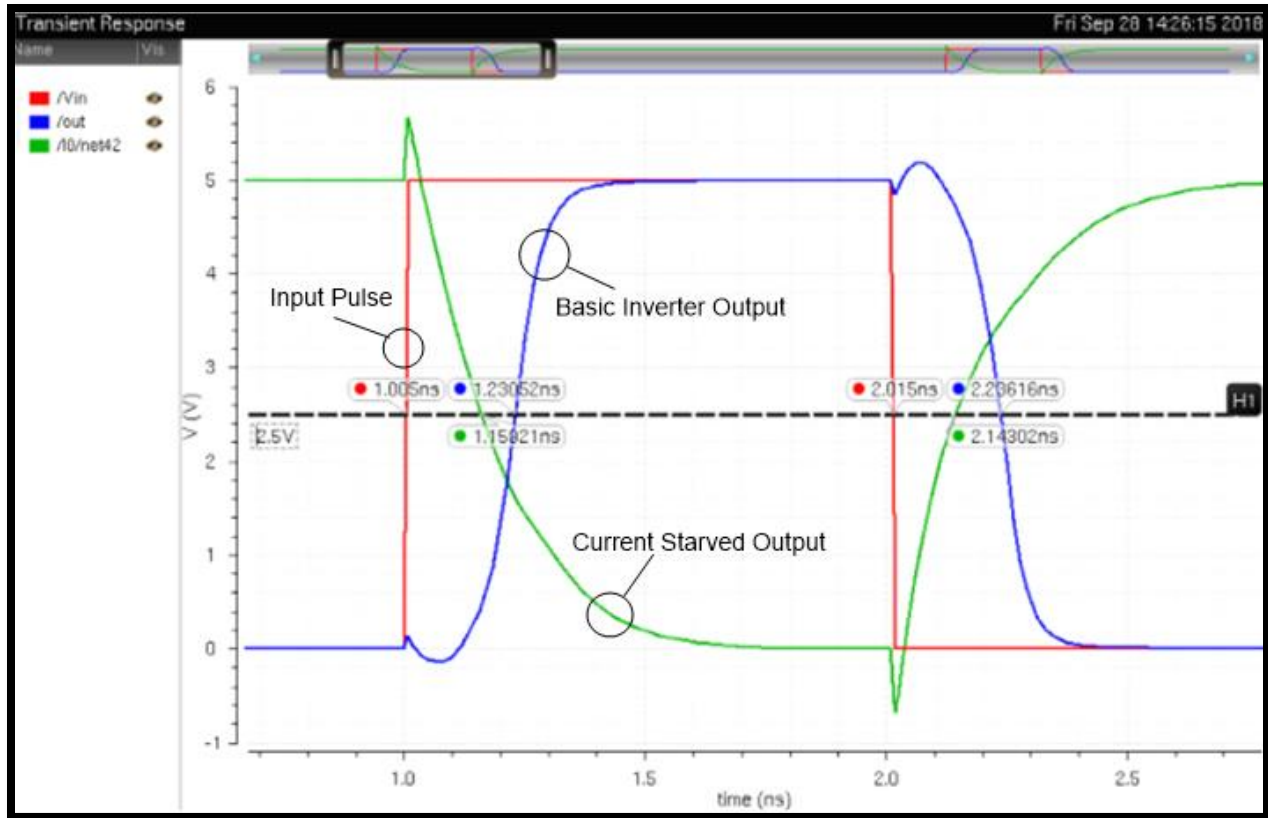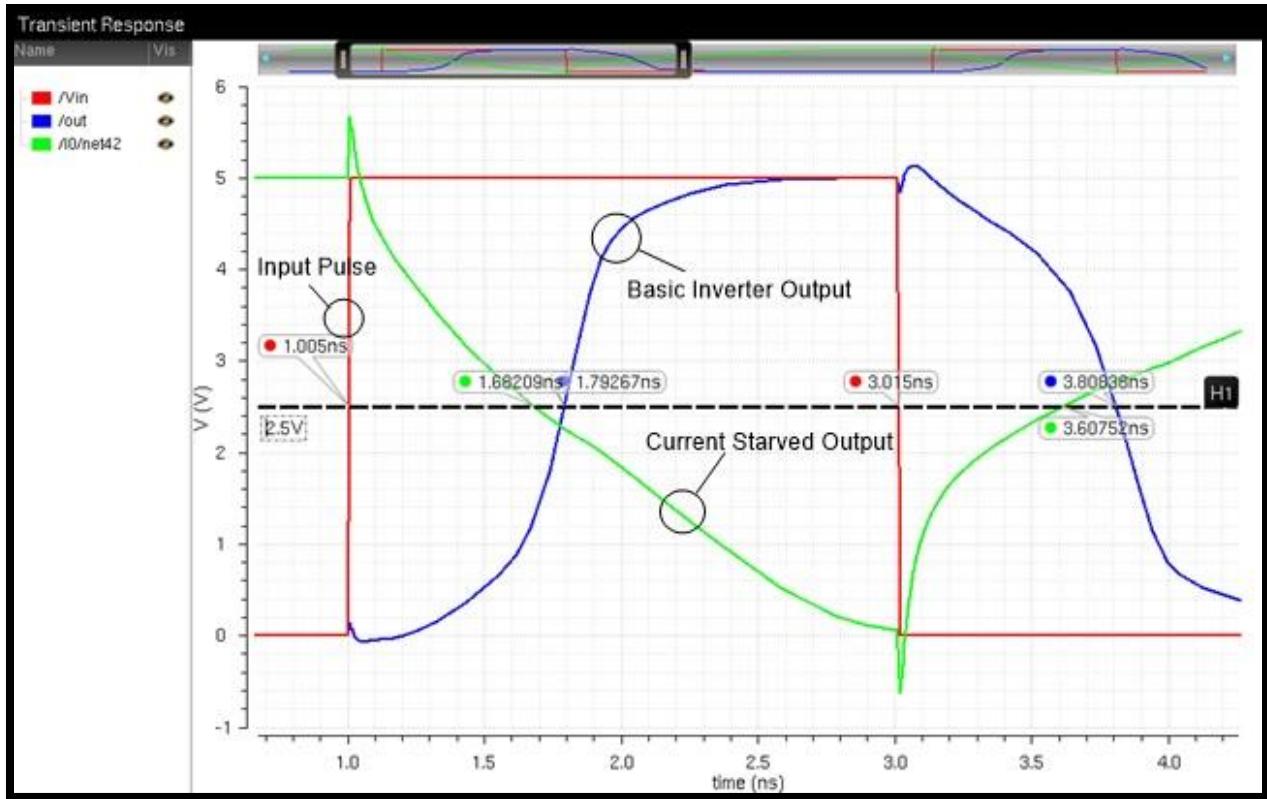
Figure 2.11 Transient Simulation of Figure 2.1 with Figure 2.6 with 1 Volt on *vinvc*

The simulation results in Figures 2.8 through 2.11 verify the variable delay element can be adjusted with the voltage-controlled beta multiplier. The time delay from each simulation ranged from 220 ps to 780 ps giving an effective sampling rate of 4.54 GHz to 1.28 GHz. In addition, adjusting the value of the bias generator's off-chip resistor increases or decreases the range of the sampling rate. For example, a larger resistor results in a slower sampling rate due to a decrease in the bias voltages and consequently, a decrease in the current through the delay element.

Vinvc (V)	Bias Resistor (kΩ)	Current Starved Time Delay (ps)	Basic Inverter Time Delay (ps)	Sampling rate (GHz)
5	2	150	70	4.54
3	2	150	70	4.54
2	2	200	80	3.57
1	2	700	80	1.28

Table 2.2 Consolidated Delay Line Results

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2.3 Stage

Figure 2.12 displays the schematic for a single capture stage unit cell. Note the delay element from Section 2.2 is included to generate the voltage-controlled delay line. The capture stage operation begins when the trigger signal, t*rig_in*, transitions from high to low and propagates through the delay element to the gate of NMOS, *N2,* causing *N2* to switch off. The analog input signal, *analog_in*, is connected to the drain of *N2* and feeding through to the hold capacitor node connected to both the source of *N2* and the gate of PMOS, *P2*. The capacitor value was chosen to accommodate for the thermal noise generated, given by kT/C, and settling time [2]. For example, the 100 fF capacitor chosen generates 200 µVolts RMS of thermal noise and takes roughly 2 ns to fully charge at 300 °K. When *N2* switches off, a sample of the signal is captured on the hold capacitor.

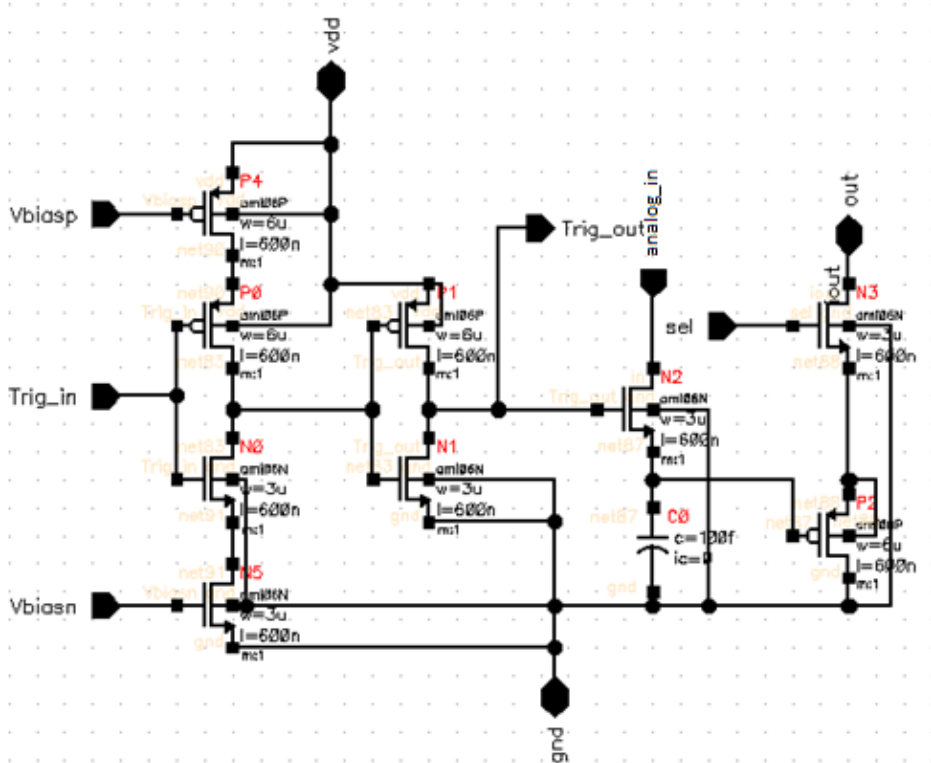Figure 2.12 Schematic of a Single Capture Stage Unit Cell with Delay element

The current flowing in *P2* is set by the voltage captured on the hold capacitor and ultimately determines the voltage on the output node. The NMOS was selected as the hold capacitor switch due to its ability to pass logic 0's well compared to PMOS devices which are able to pass logic 1's well. This is relative since it allows the range for the analog input voltage window to go down to ground and therefore bias *P2* such that it remains in saturation providing the upper range of the analog input voltage, 3 Volts, calculated using equation 2.16, is not exceeded.

Returning to Figure 2.12, *N3* is a switch activated by a logic 1 from an on-chip 8:256 decoder, connected to *sel*, during readout of the sampled signal. Recreating a slowed, or stretched out, version of *analog_in* requires the stages to be readout sequentially with only one stage active at any given time. The decoder is controlled via binary values from 0 to 255 from an off-chip counter or microcontroller and ensures only one capture stage is active at any time.

Connecting a 20 kOhm pull-up resistor from the outputs of all the capture stages to VDD allows for reconstructing the captured signal. The value of the pull-up resistor can be varied dependent upon application requirements. For example, a larger pull-up resistor will generate more swing on the output, *out* in Figure 2.12. A larger swing could be necessary if the analog input signal has little variation between successive capture stages.

As mentioned above, there are limitations on the voltage range of *analog_in* that are related to the ability of *P2* to remain in saturation. In order to create a stretched replication of *analog_in*, two conditions have to be satisfied for *P2* to remain operating in the saturation region. These two conditions are defined by [4]

$$V_{THP} \leq V_{SG} \qquad\qquad Eq(2.12)$$

and [4]

$$V_{SG} - V_{THP} \leq V_{SD} \qquad\qquad Eq(2.13)$$

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Eq. (2.12) requires *P2's* source-gate voltage to be greater than or equal to its threshold voltage, V_{THP}, to ensure *P2* is turned on. Eq. (2.13) requires the source-drain voltage to be greater than or equal to the difference between the source-gate voltage and V_{THP}. A point of note is *P2* was fabricated in its own well to eliminate body effect that would occur if the bulk was connected to VDD, thus creating a consistent V_{THP}. Referencing Figure 2.12, the maximum source voltage possible at *P2* is defined by

$$VDD - V_{THN} = V_{S,max} \qquad\qquad Eq(2.14)$$

where V_{THN} will vary due to body effect from the potential difference between the bulk and source of *N4*. To find the values of V_{THP}, V_{THN}, V_{SD}, and V_{DS}, an operating point simulation was performed on Figure 2.12 to obtain these values. The operating point results demonstrated that

$$V_{S,max} = VDD - V_{THN} = 5V - 1.271V = 3.729V \qquad\qquad Eq(2.15)$$

and using Eq. (2.12), the maximum gate voltage can be calculated as

$$V_{S,max} - V_{THP} \geq V_G \qquad\qquad Eq(2.16)$$

$$3.729V - 725.5mV \geq 3.0035V$$

Now the maximum and minimum output voltages can be determined using the following equations where the gate voltage on *P2* is 0 Volts for maximum output and 3 Volts for minimum output.

$$V_{out} = V_{SD} + V_{DS} \qquad\qquad Eq(2.17)$$

$$V_{out,max} = 1.736V + 298mV = 2.034V$$

$$V_{out,min} = 3.729V + 1.248V = 4.977V$$

The simulation results seen in Figure 2.13 verify that the hand calculations are correct. The blue trace is the *analog_in*. The red trace is the *out* voltage generated by the current set by the gate

voltage on *P2* and the 20 kOhm resistor. Figure 2.13 also demonstrates the level shift caused by

the PMOS and the linearity of the output signal *out*.
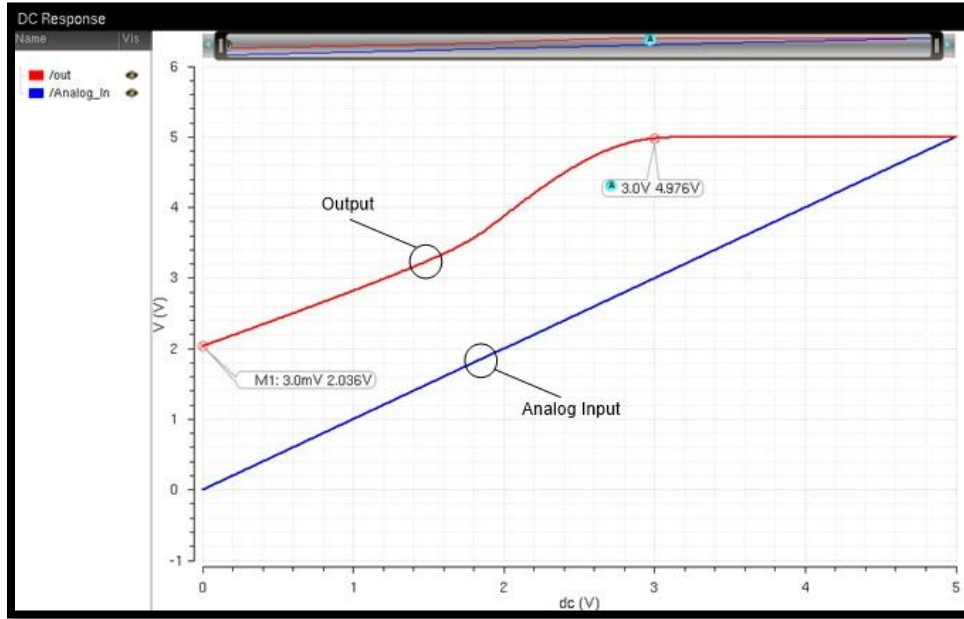
Figure 2.13 Stage DC Sweep

2.4 Variable Fast Transient Digitizer

Now that the capture stage unit cell operation has been explained and approximations for

the time delay through each stage have been determined, the next step is to demonstrate how the

unit cells are arranged sequentially to enable the trigger signal to propagate throughout the VFTD.

Figure 2.14 shows the schematic view of two sequential capture stage unit cells. Note the trigger

signal propagates from the input of the first current starved inverter to the input of the basic inverter

and then to the input of the NMOS, *N2,* acting as the hold capacitor switch. The input of *N2* is

also the same node as the input to the current starved inverter in the next sequential capture stage

unit cell. This is the manner in which the trigger signal serves to both capture the analog input

signal and propagate through all 256 capture stages.
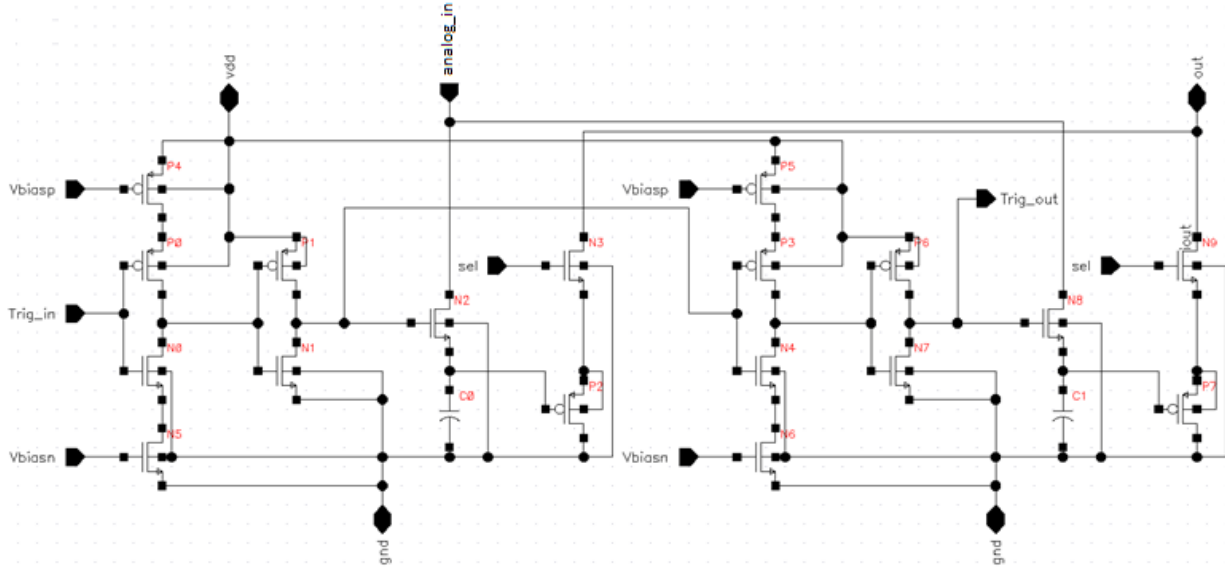
Figure 2.14 Two Sequential Stages

To confirm the time delay approximations derived in Section 2.2, the 256 stage VFTD was simulated using the schematic displayed in Figure 2.16. However, referencing Figure 2.14, an additional time delay needs to be added to the delay derived in Eq. (2.10) to accurately model the parasitics associated with $N2$ in each capture stage unit cell. This additional delay is modeled by

$$t_{n,stage} = 0.7\, R'_n \frac{L_n}{W_n} * \frac{3}{2}\, C_{oxn} \qquad\qquad Eq(2.18)$$

$$0.7 * 21.223k\Omega * \frac{0.6\mu m}{3\mu m} * \frac{3}{2} 4.5fF = 20ps$$

resulting in a more precise time delay of

$$t_d = t_{plh} + t_{phl} + t_{n,stage} \qquad\qquad Eq(2.19)$$

$$100.28ps + 100.28ps + 20ps \approx 220.56ps$$

The time delay calculated above reflects the optimal delay, however another delay element needs to be addressed before the theoretical sampling frequency can be calculated. The bias generator does not generate rail to rail bias voltages, therefore the current is limited through the current starved inverter. The expected consequence of reduced current is a slower time delay than the optimal value calculated above. The result is the maximum effective sampling frequency of the VFTD is slightly reduced when compared to the FTD. However, this is a reasonable tradeoff for increased applicability. Figure 2.15 displays the simulation results for three sequential stages biased with the bias generator to determine the actual time delay through each delay element.

Figure 2.15 Time Delay Through Three Sequential Stages
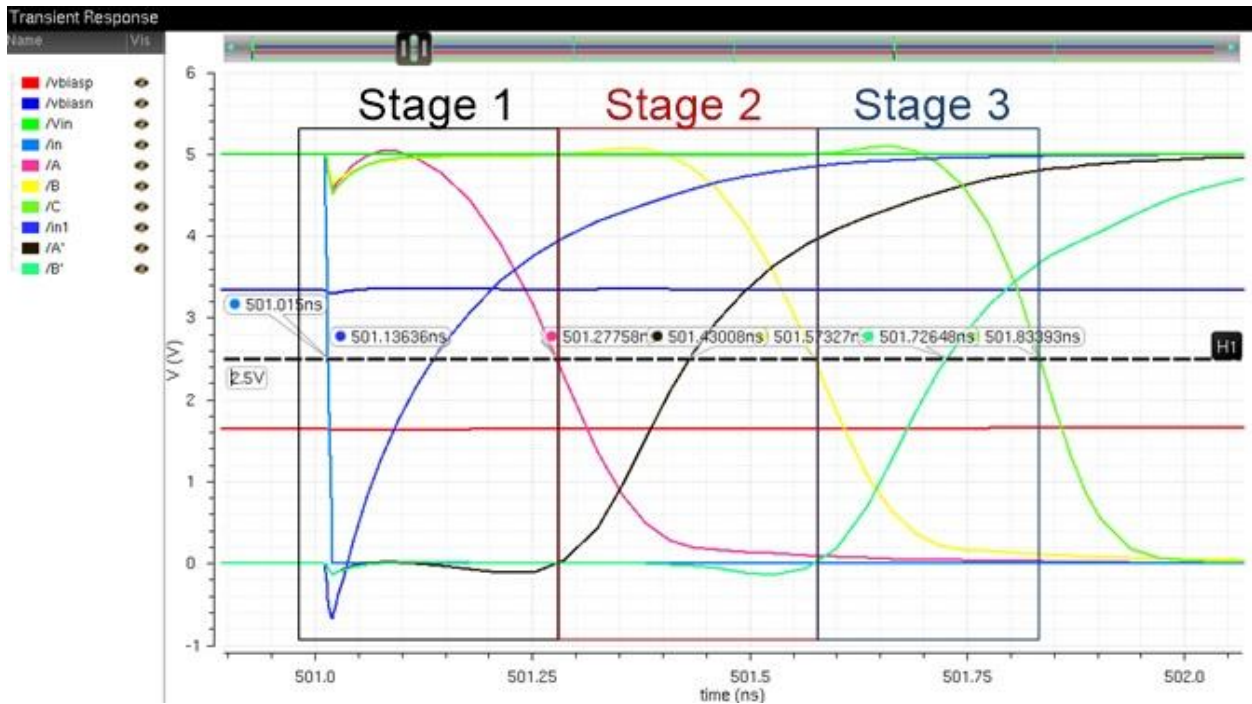
Figure 2.15 demonstrates the extra delay added due to the limited current driving the inverters for each transition. To determine an accurate time delay the middle stage, denoted by stage 2 in Figure 2.15, will be used to find the high-to-low and low-to-high time delay. The pink trace to the black trace is the high-to-low time delay of 152.5 ps and the black trace to the yellow

trace is the low-to-high time delay of 141.22 ps. This leads to the total time delay through one delay element as

$$152.5ps + 141.22ps \approx 293.72ps$$

The simulation results account for both the additional delay element from the bias generator and the extra parasitics introduced from NMOS, *N2*. This gives a more accurate sampling rate that is calculated using Eq. (2.11).

$$f_{sample} = \frac{1}{293.72ps} \approx 3.40GHz$$

After accounting for the extra delays, the entire 256 stage design was simulated to confirm the calculations. Recall, Figure 2.16 is the schematic used to simulate a 256 stage VFTD. The bias generator control voltage, *vinvc*, was set to 5 Volts to demonstrate the fastest capture rate. Inputs *A0* through *A7* are voltage sources acting as the off-chip counter that will access each stage via the on-chip 8:256 decoder discussed earlier. The input signal *Ve* enables the decoder, *trig_in* serves as the trigger, and *Vin* is the analog input signal.
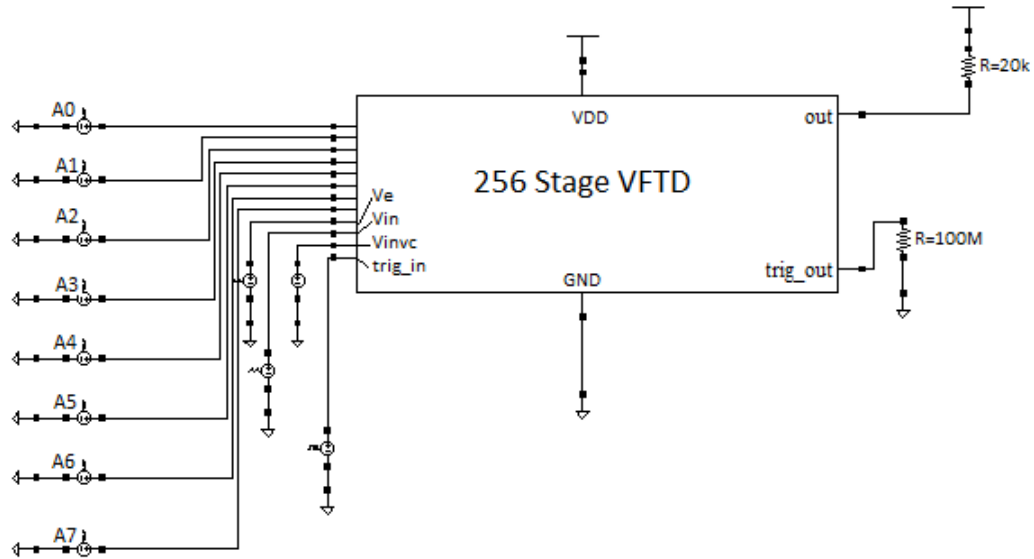
Figure 2.16 256 Stage Simulation Schematic

The simulation results from Figure 2.17 can be used to determine the effective sampling rate.
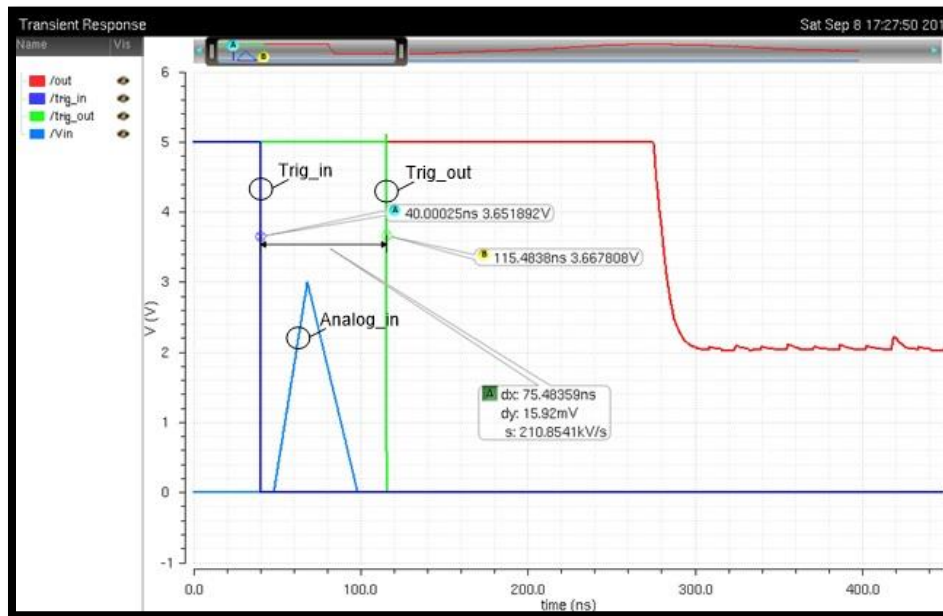

Figure 2.17 256 Stage Simulation Results

As can be seen, the time between *trig_in* and *trig_out* is 75.48 ns. Using this result, the

sampling rate can be calculated using Eq. (2.11) as

$$\frac{75.48 ns}{256 \ stages} = \frac{294.85 ps}{stage}$$

$$fs = \frac{1}{294.85 ps} = 3.39 \ GHz$$

Now that the sampling frequency has been calculated and simulated, the capturing and readout operation will be demonstrated using Figure 2.16. The analog input signal *Vin* is a piecewise linear function with a fast rising edge and a comparatively slow falling edge. The rising edge extends from 0 Volts to 3 Volts over 20 ns and the falling edge returns from 3 Volts to 0 Volts over 30 ns. Referring to Figure 2.17, the light blue trace is the analog input signal. Figure 2.18 shows the stretched-out, captured signal represented over a longer time period as the red trace.
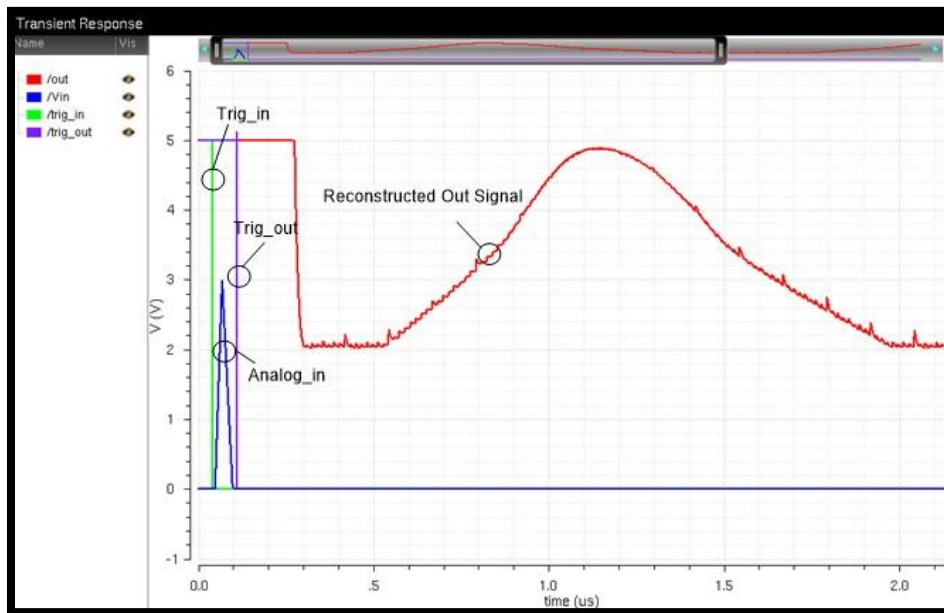

Figure 2.2.18 256 Stage VFTD Output

As can be seen, the VFTD receives the *trig_in* signal, green, at 45 ns followed immediately after by the 50 ns analog input signal. At roughly 115 ns, the *trig_out* signal exits the last capture stage indicating the analog input signal has been sampled by the VFTD. Next, the counter begins

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decoding the sampled signal at 275 ns and reconstructing the analog input signal over 1.5 us. The

initial rising edge of 20 ns is now stretched to roughly 700 ns and the initial falling edge of 30 ns

is stretched to roughly 800 ns. A key point to remember is the reconstruction rate is set by the

speed of the off-chip counter tied to the on-chip decoder. Therefore, the reconstruction rate can

be adjusted by changing the speed of the counter. It is also worth mentioning that the amplitude

of the reconstructed output signal is dependent upon the value of the pull-up resistor.

Now that the fastest speed of the VFTD has been simulated and verified, a slower speed

will be tested to demonstrate the variability of the design. For this simulation, *vinvc* is set to 1

Volt, just above the 800 millivolt threshold voltage of NMOS, *N1*. Figure 2.19 shows the

simulation results demonstrating a much larger capture window of 266.83 ns.
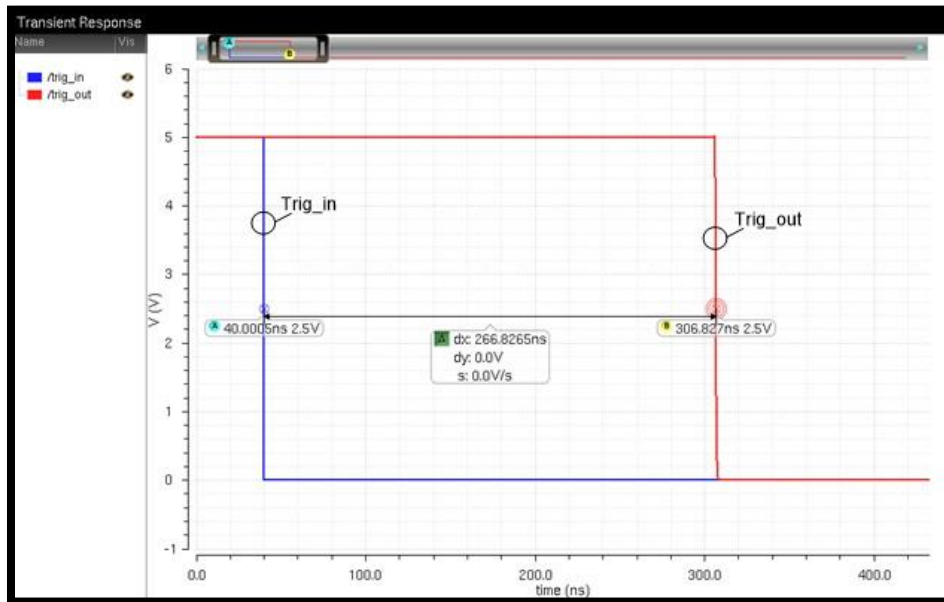

Figure 2.19 Large Capture Window

This means the single delay element of each stage now has a delay of 1.04 ns versus 294.85 ps

when *vinvc* was set to 5 Volts. Using Eq. (2.11) again, the new sampling frequency is calculated

as

$$f_{sample} = \frac{1}{1.04ns} = 959.41\ MHz$$

The result is the VFTD simulations demonstrate a capture rate range from roughly 960 MHz to 3.4 GHz for *vinvc* between 1 Volt and 5 Volts, respectively. Note, this range is also dependent upon the value of the resistor used in the bias generator. Changing the bias resistor value alters *vbiasp* and *vbiasn*, and therefore the speed and range of operation for the VFTD. For example, using a larger value resistor will further limit the current in the bias generator, and subsequently increase the time delay per stage.

It is important to provide simulation results that can later be compared to the VFTD experimental results detailed in Chapter 4. The laboratory equipment used for testing is limited to a maximum frequency of 25 MHz. For this purpose, the next simulation performed used a sinusoid with a frequency of 25 MHz and a 1.5 Volts amplitude with a 1.5 Volts DC offset to span the full range of the analog input signal. To account for the scaling difference between the high frequency sinusoid and its stretched reconstruction, the results are shown separately in Figures 2.20 and 2.21, respectively. Figure 2.20 shows an expanded view of *trig_in*, *trig_out*, and the analog input sinusoid while Figure 2.21 shows the stretched reconstruction of the sinusoid.
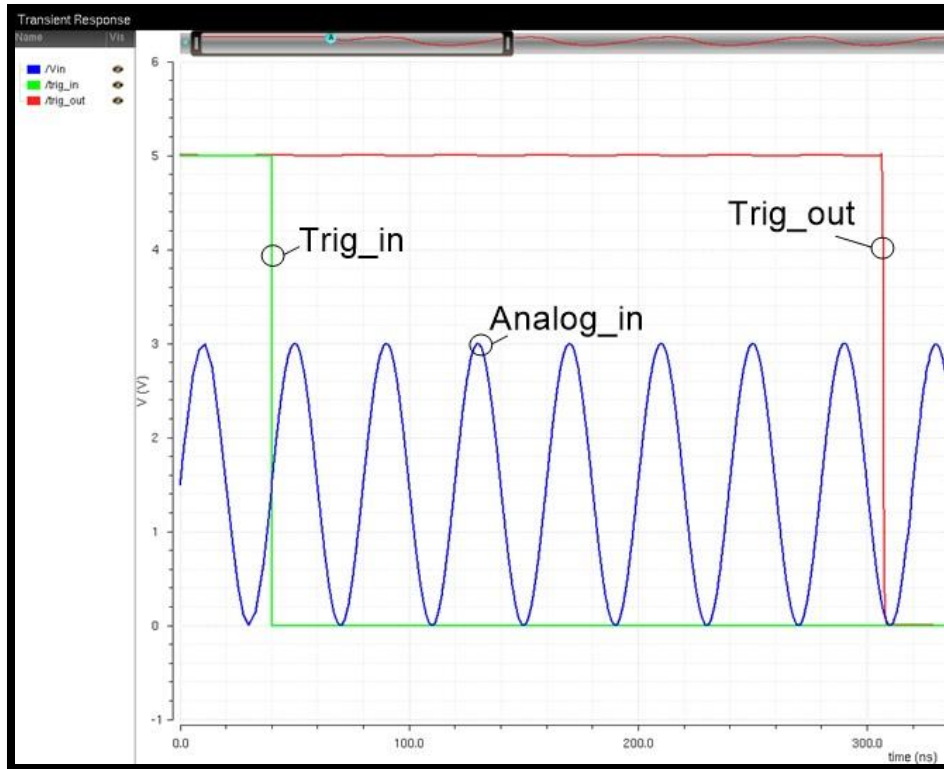
Figure 2.20 Large Capture Window with Analog Input Signal

Referencing Figure 2.20, the VFTD is triggered at roughly 40 ns and the *trig_out* signal falls at roughly 330 ns for a 290 ns capture window. Note there are approximately 6.5 cycles of the input signal within the capture window. Now referencing Fig. 2.21, the decoders begin reconstructing the signal at approximately 275 ns and finish at approximately 2.3 us. The VFTD reconstructs the original 290 ns signal over a period of 2 us with all 6.5 cycles present in the reconstruction. At 2.3 us the counter once again starts counting from 0, thus the break in the reproduction of the signal.
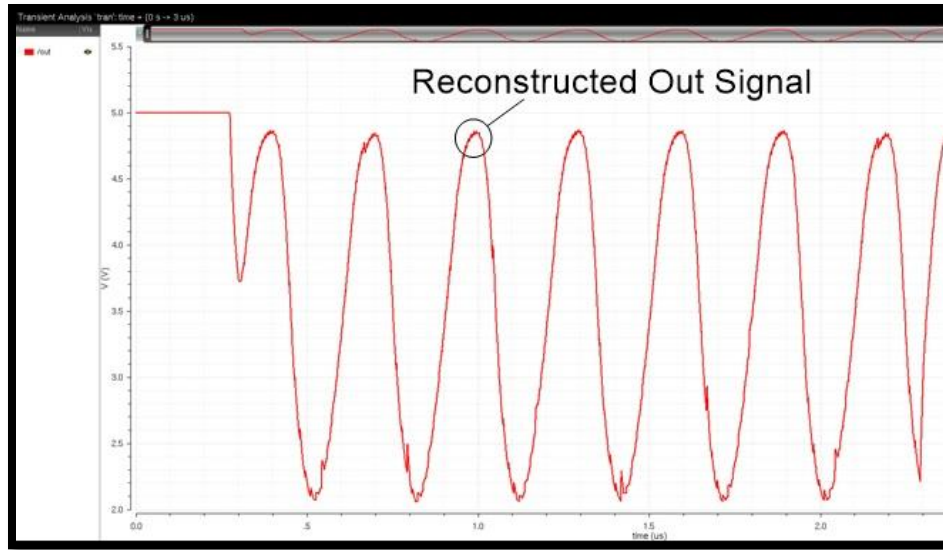
Figure 2.21 Reconstructed Captured Signal from Figure 2.20

The simulation results from Figures 2.18 and 2.21 demonstrate the VFTD can capture signals and reconstruct them at a slower rate for analysis at speeds modern processors can accommodate. The simulations also demonstrate that the capture window can vary for user specific applications. Figure 2.22 shows simulation result with the value of the bias resistor increased to 4 kOhms to demonstrate that the capture window can be adjusted with two variables, *vinvc* and the bias resistor.
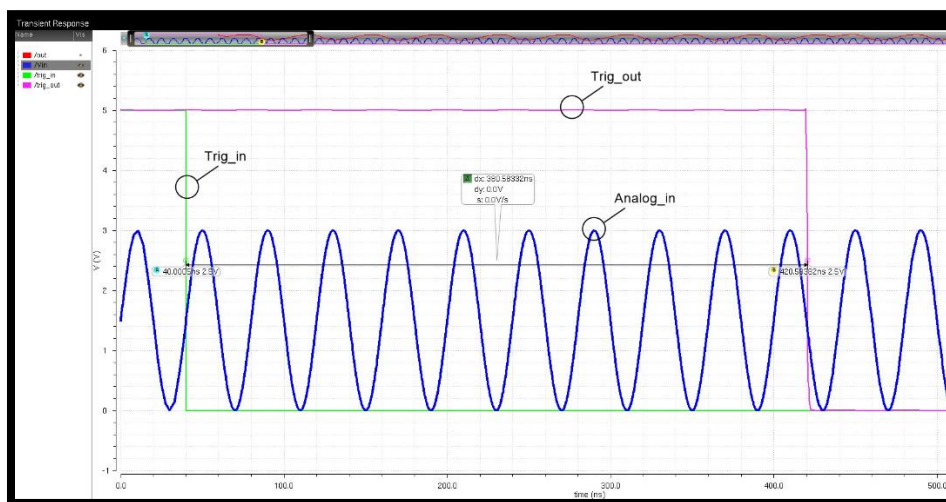
Figure 2.22 Larger Capture Window with Analog Input Signal

As can be seen the capture window has increased to roughly 380 ns yielding an effective sampling rate of 670 MHz. Figure 2.23 will demonstrate the reconstruction of the captured signal seen in Figure 2.22.
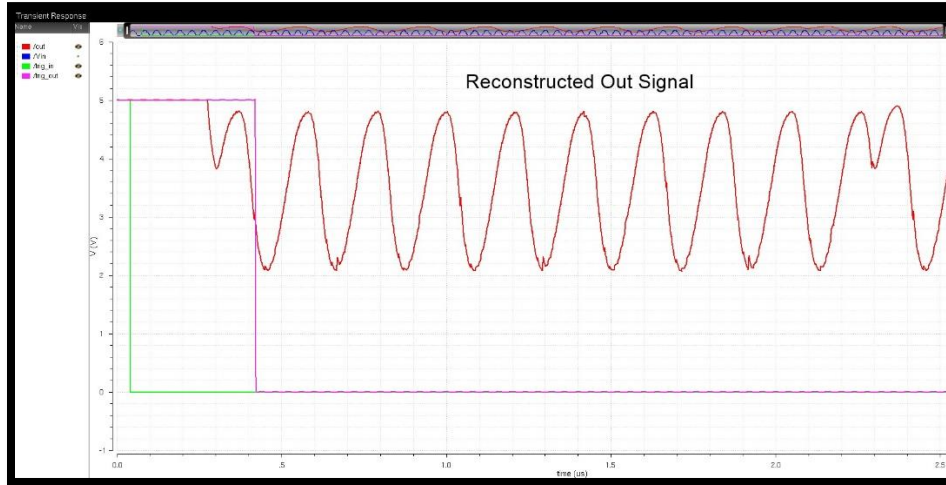
Figure 2.23 Reconstructed Captured Signal from Figure 2.22

Figure 2.22 shows there are roughly 9.5 cycles of the analog input sinewave between the trigger input and trigger output signals. Figure 2.23 confirms that roughly 9.5 cycles were captured by the VFTD.

Vinvc (V)	Bias Resistor (kΩ)	Capture window (ns)	Sampling rate
5	2	75.48	3.39 GHz
1	2	294.85	949 MHz
1	4	380.58	672 MHz

Table 2.3 Consolidated 256 Stage Simulation Results

Chapter 3 Chip and Layout Design

Chapter 3 covers the layout and design considerations of the 256 stage VFTD with the decoder and pad frame. Section 3.1 will cover the bias generator layout, Section 3.2 will discuss the stage layout, and Section 3.3 will explain the decoder operation and layout. Section 3.4 combines each component into an array of cells to complete the 256 stage VFTD and Section 3.5 details the manufacturing of the chip. Prior to performing a layout, multiple potential issues need to be addressed to ensure proper functionality of the design. Primary among these concerns are capacitive coupling, noise reduction, and signal flow for all of the layouts in this design.

3.1 Bias Generator Layout

The bias generator layout, Figure 3.1, consumes a very small portion of the 2mm x 2mm integrated circuit (IC). The trace labeled *res_out* ultimately connects to an Electrostatic Discharge (ESD) pad that in turn connects to the off-chip bias resistor. The traces labeled *vbiasn* and *vbiasp* set the DC bias voltages for the current starved inverters and route to every current starved inverter on the chip. The control voltage *vinvc* is routed to another ESD pad. The voltages produced by the bias generator are all DC in nature, therefore, issues such as capacitive coupling and signal flow are not taken into consideration when placing the components that makeup the bias generator.
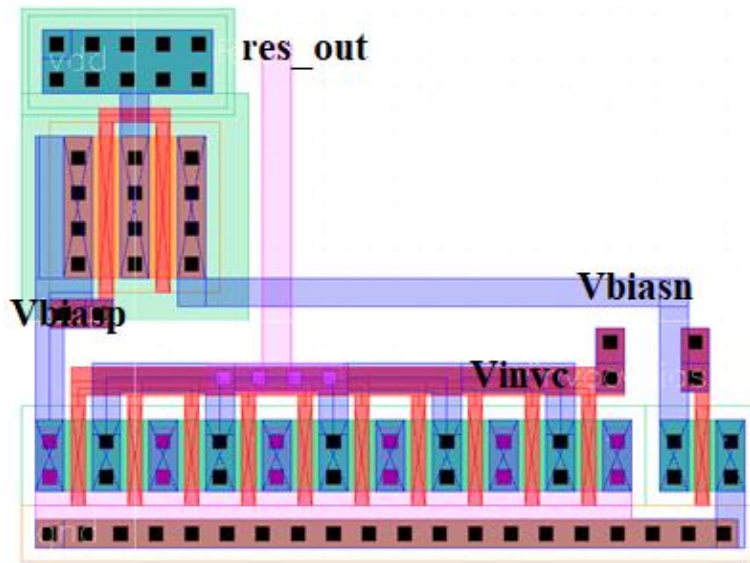
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Figure 3.1 Bias Generator Layout

3.2 Stage Layout

The stage layout seen in Figure 3.2 was designed for optimal signal flow and separation of the analog input and output signals. The stage cell was designed so that any number of cells can be placed in an array and all of the signal paths will tie together. The metal traces for the analog input and output signals are routed away from each other and from high speed signal lines to limit the capacitive coupling error that could be introduced. Capacitive coupling occurs when transient signals from one signal path affect the signal on other signal paths within close proximity. The hold capacitor has ground rails on both the top and bottom to help reduce unwanted signals from impacting the analog signal that is being stored on the hold capacitor. The pitch of the layout, a term describing the spacing between similar points within an array, was also taken into consideration so that minimum routing is needed for stage selection from the decoder.
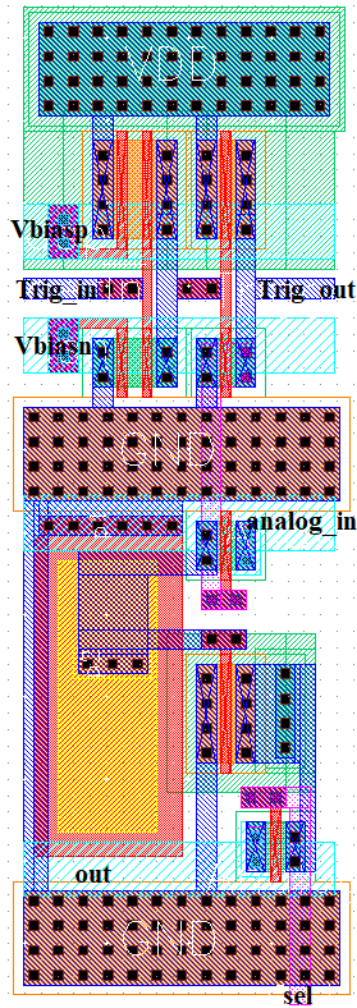
Figure 3.2 Stage Layout

3.3 Decoder Layout

The 4:16 decoder layout seen in Figure 3.3 uses four inverters and sixteen 5-input NAND gates that are followed by an inverter to create a 5-input AND gate to allow access to one stage at a time. To decode 256 stages requires the use of sixteen 4:16 decoders. The decoder is operated via a 4-bit binary input received from the off-chip counter with each bit inverted to provide all the logic required to decode 16 stages. The first four inputs to the AND gate, layout seen in Figure 3.4, are routed using the logic from the off-chip counter with the fifth input of the decoder used as an enable signal. The 4:16 decoder was designed in tandem with the stage layout in Figure 3.2 to

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have the same pitch as the stage, thus allowing for simplified array implementation. If the pitch

of either of these components did not match, then additional routing would be needed to connect

the outputs to each stage. Finally, an additional 4:16 decoder is implemented with its outputs

connected to the fifth input of the 4:16 decoders. These inputs serve as the enable signals for the

sixteen 4:16 decoders that access the individual stages. This gives a total of 8 bits that access 256
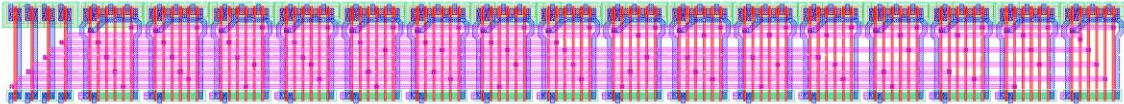
stages, effectively an 8:256 decoder.
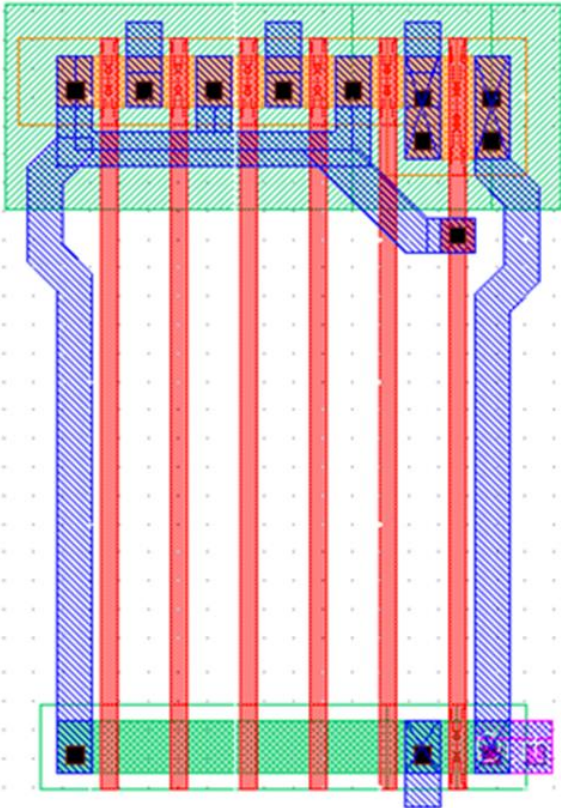

Figure 3.3 5 4:16 Decoder

Figure 3.4 5-Input AND Gate Followed by an Inverter

3.4 256 Stage Layout with Decoder and ESD Pad Frame

Figure 3.5 is an array of 16 stages including a 4:16 decoder. The trigger signal will travel through the array from left to right. The output of each AND gate is connected to a specific stage and routed so the binary input 0000 results in the 0th stage being selected for readout, the input 0001 results in the next stage being selected, and so on.
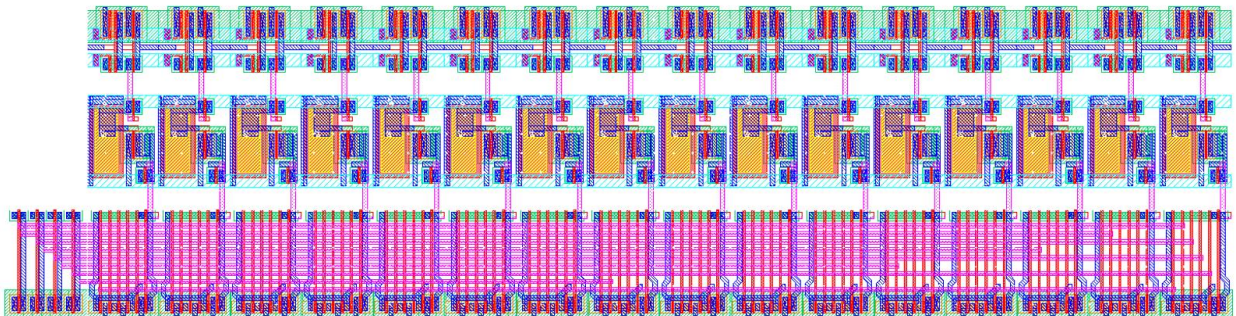
Figure 3.5 16 Stage Array with 4:16 Decoder

Figure 3.6 is an array of 32 stages where the 16 stages and decoder from Figure 3.5 are mirrored and placed above the first 16 stages. The signals *vbiasp, vbiasn, analog_in,* and *out* are routed on the sides to tie them together and maintain sequential order. The trigger signal is routed with minimal length from the 16th stage to the 17th so that the rate of capture is not influenced. A longer path would result in more parasitics, increasing the time delay between the 16th and 17th capture.

Figure 3.6 32 Stages and 2 Decoders

256 stages are obtained by implementing 8 arrays of Figure 3.6. The signals mentioned above are implemented using a tree routing technique. The tree routing technique is used when a signal path goes to several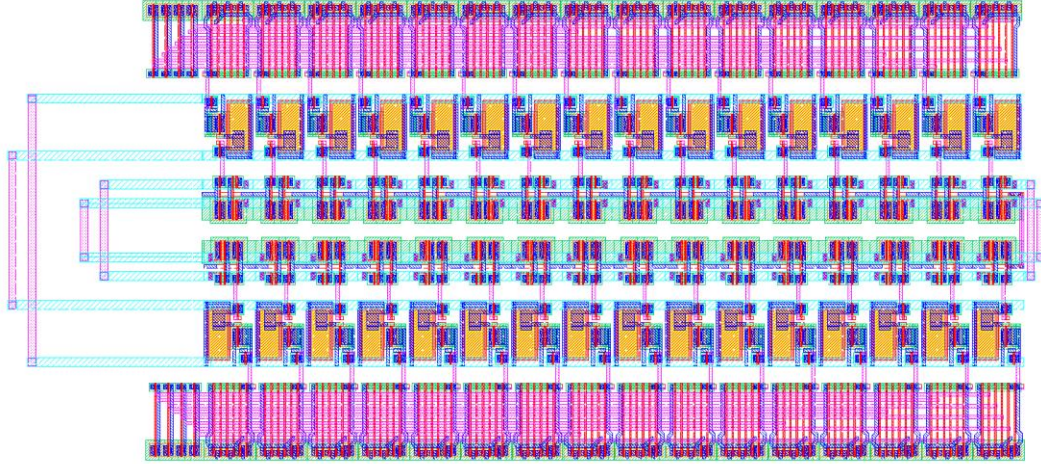 locations and the length of each path needs to be identical. The length of the path is especially important for the analog input and output signals in this design. This technique helps ensure that the analog input signal reaches the beginning of each 32-stage array at the same time. As the stages capture the analog input signal sequentially, the path of the analog input signal needs to be considered so that the signal is sampled properly. For example, if the signal path is too long to one bank, that bank could capture the signal that another bank has already captured and introduce an error during reconstruction. Each signal path is separated by a grounded trace at the same level to further limit capacitive coupling. Once the 256 stages were placed and routing was completed, a 40-pin ESD pad frame with a large decoupling capacitor between VDD and ground was designed as seen in Figure 3.7. The decoupling capacitor is intended to act as a large bucket of charge for the transistors. This helps maintain VDD at a fixed voltage while the VFTD is under operation. As can be seen in Figure 3.7, there is enough room and enough open

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pads to accommodate 2 separate 256-stage VFTDs on one 2 mm x 2 mm chip. Half of the chip was left open for other student projects.
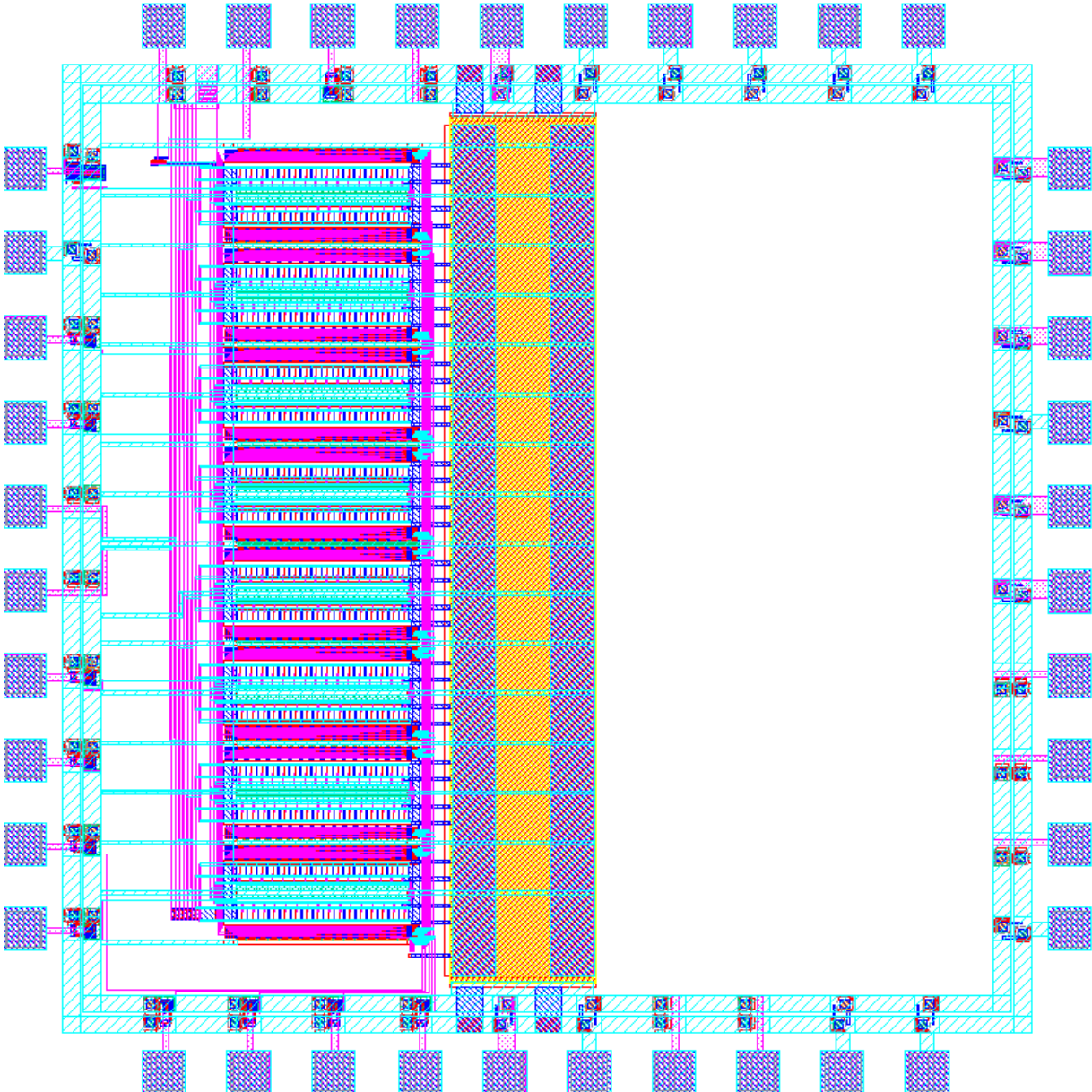
Figure 3.7 256 Stage VFTD with 40 Pin ESD Pad Frame

3.5 Manufactured Chip

Once the chip design and layout was complete, the project was sent to MOSIS for fabrication. After receiving the chip, it was wire bonded by the author at one of UNLV's

laboratories to a package in preparation for testing. Figure 3.8 is the picture of the wire bonded chip. The package is a 28-pin carrier for the chip that can be seen with the mounted and wire bonded chip in Figure 3.9.

Figure 3.8 Wire Bonded Manufactured Chip

Figure 3.9 Wire Bonded Manufactured Chip in a 28-Pin Package

Chapter 4 PCB and Test Results

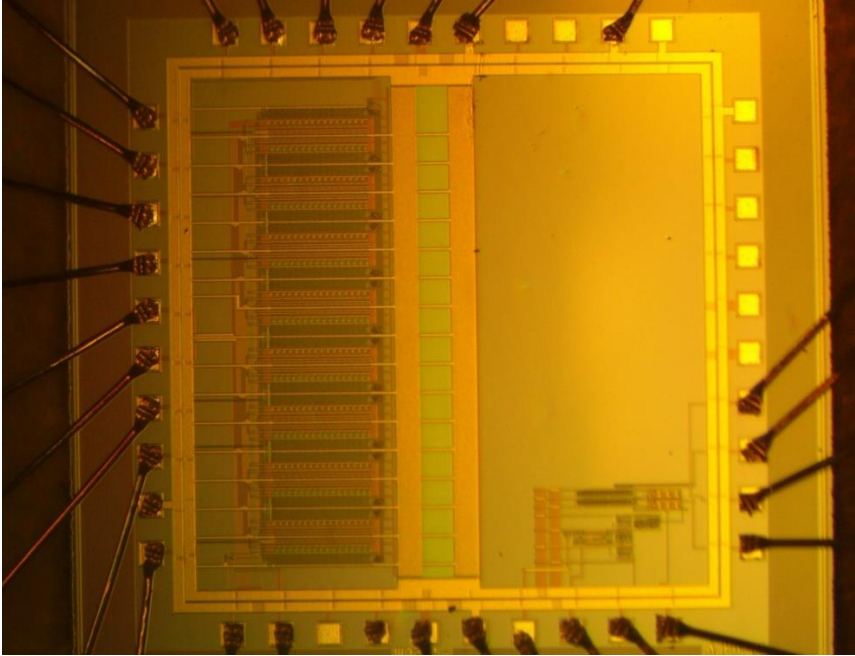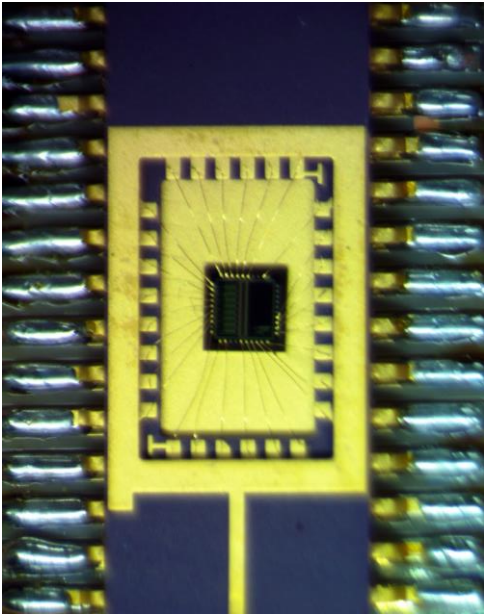Chapter 4 covers the design of the printed circuit board (PCB) used for testing and the test results. Section 4.1 will cover the PCB board and Section 4.2 will discuss the test results. The PCB design was completed using DipTrace Schematic and PCB Design Software and fabricated by Gold Phoenix. The test results were obtained using the following equipment:

- Power Supplies: Keithley 2450 Source Meter, Instek GPS-3303

- Function Generator: Instek AFG-2225

- Oscilloscope: Siglent SDS 2304X

4.1 PCB

Figure 4.1 is the top and bottom view of the PCB layout. An Arduino Uno was used to generate the control logic required to activate the counter and the trigger signals. An on/off switch was used to initiate the capture and reconstruction of the VFTD, however a common issue with switches is they suffer from a phenomenon known as switch bounce. When a switch is toggled, mechanical elements within the switch physically move to new positions with a resulting 'bounce' that can cause the switch to open and close several times before settling into position. To counteract switch bounce, a debouncing circuit was implemented in order to generate a clean signal for initiating the capture sequence and reconstruction phase of the VFTD with the Arduino. An off-chip 8-bit counter was used to access the stages for the reconstruction event. The Arduino code consists of an IF statement to control the trigger input to the VFTD and initiate the counter. The code is included in the Appendix.

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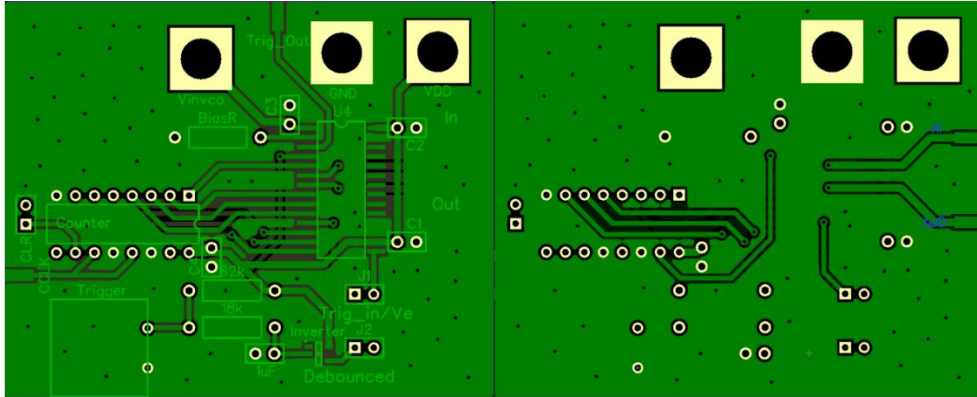
Figure 4.1 PCB Design Top and Bottom Layer

Figure 4.2 is the populated PCB that was used to generate the test results discussed later in this section. The pushbutton switch is in the lower left corner, the counter is directly above the switch, and the packaged VFTD IC is to the right of the counter.

Figure 4.2 Populated PCB Board

4.2 Test Results

The testing of the VFTD consisted of variations of both *vinvc* and the bias resistor. The signals that will be captured are as follows: *trigger_in, trigger_out, analog_in,* and *out*. For the

purposes of comparison and simplicity, the same *analog_in* signal will be used for all variations

of *vinvc* and the bias resistor. Also, since the functionality of the circuit has already been proven

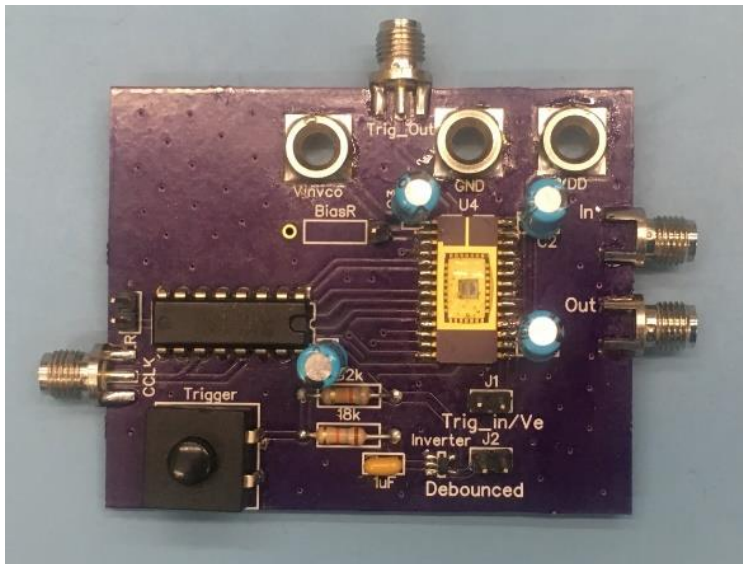in Buck and Baker's design the tests focus on the variability of the circuit. The *analog_in* signal

used was a 20 MHz sine wave with 3 Volts Peak to Peak (VPP) and a 1.5 Volt DC offset. The

blue trace in each figure represents the *trigger_in* signal, the green trace is the *trigger_out* signal,

the red trace is the *analog_in* signal, and the purple trace is the *out* signal. The off-chip counter

used to access the stages to reconstruct the captured signal was set to count at a rate of 25 MHz

using the Instek AFG-2225 function generator. The upper limit of the function generator used for

testing is 25 MHz, therefore this prevents testing of the upper limits of the VFTD. At 40 ns per

bit by 256 bits, it takes roughly 10 us to read out the captured signal. The following pairs of figures

will first demonstrate the capture window and captured signal followed in the next figure by the

reconstructed signal. Figure 4.3 demonstrates the fastest speed, or smallest capture window, of

the VFTD. To generate the test results in Figures 4.3 and 4.4, *vinvc* was set to 5 Volts and the bias

resistor was set to zero Ohms. Figure 4.3 will also show the capture window, the time between

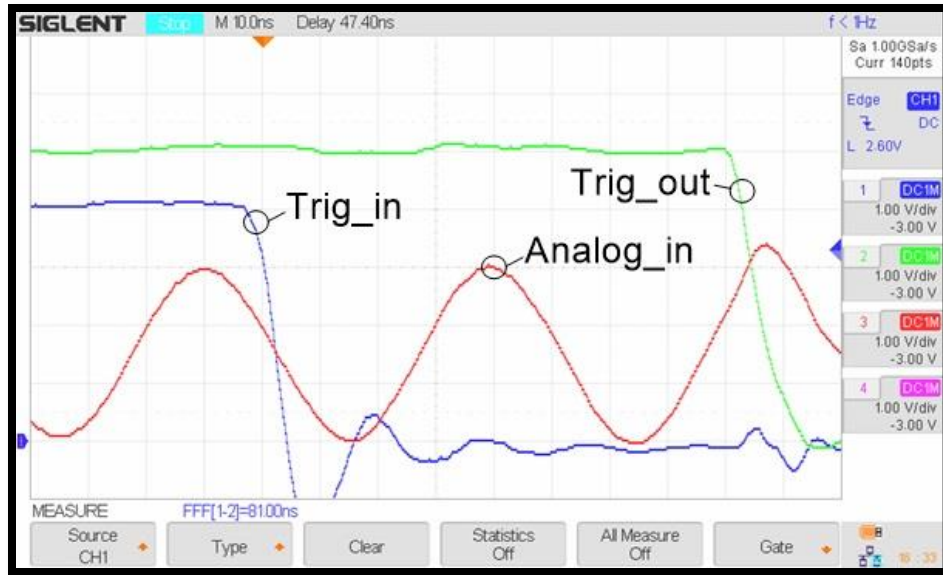*trigger_in* and *trigger_out* signals denoted by FFF(1-2).

Figure 4.3 Capture Window with 5 Volts on *vinvc* and 0 Ohm Bias Resistor

From Figure 4.3, the time delay between the *trigger_in* and *trigger_out* signal, 81 ns, will be used to calculate the effective sampling rate. Knowing there are 256 stages results in an effective sampling rate of 3.16 GHz. Also, note that the signal captured is slightly over 1.5 cycles of the 20 MHz input signal. Figure 4.4 demonstrates that the reconstruction of the captured signal, 1.5 cycles of a 20 MHz sinewave, takes approximately 10 us as estimated. This means that the VFTD took a signal at 20 MHz and stretched it out to be a 153 kHz signal. Again, this reconstruction rate can be adjusted by increasing or decreasing the rate at which the stages are accessed via the off-chip counter.

Figure 4.4 Reconstructed Captured Signal from Figure 4.3

Figures 4.5 and 4.6 repeat the test process with *vinvc* set to 1 Volt and the bias resistor set to 2 kOhms to demonstrate the variable capture window. From Figure 4.5, the capture window has increased to 384 ns. Again, knowing there are 256 stages, the effective sampling rate can be calculated to be 666.66 MHz. Note that roughly 7.5 cycles of the 20 MHz sinewave is within the capture window.

Figure 4.5 Capture Window with 1 Volt on *vinvc* and a 2 kOhm Bias Resistor

Figure 4.6 shows that 7.5 cycles of the captured signal have been recreated over 10 us. Consequently, the 20 MHz input signal has been stretched and reconstructed as an approximately 769 MHz signal.
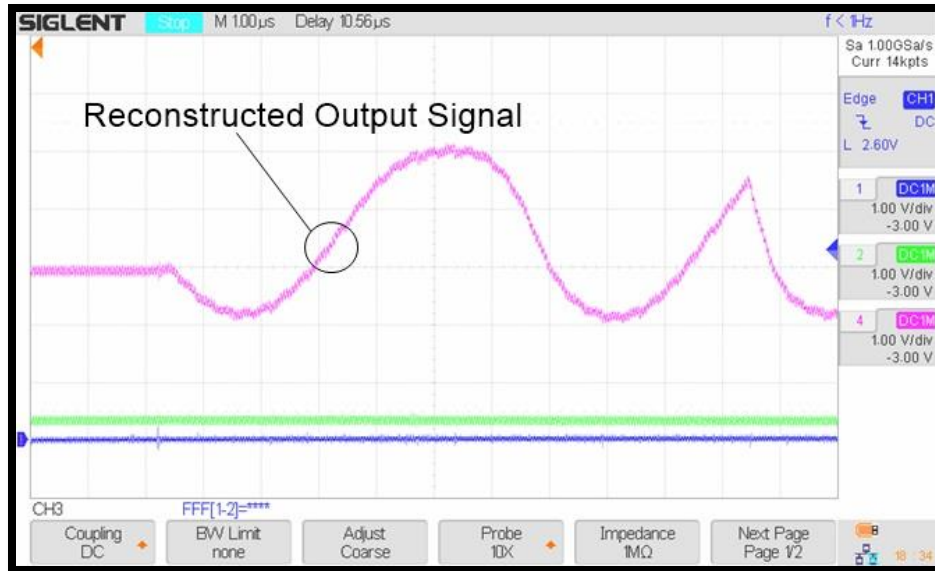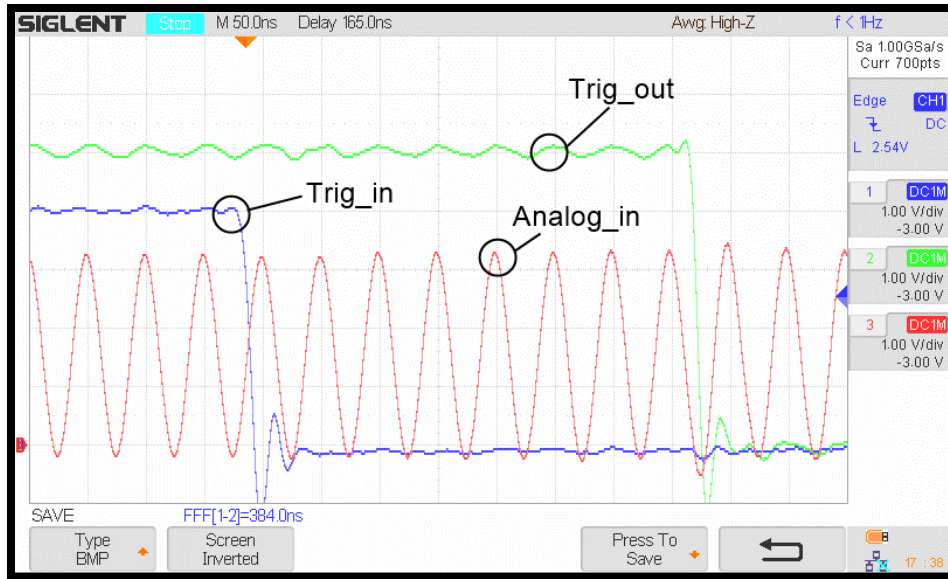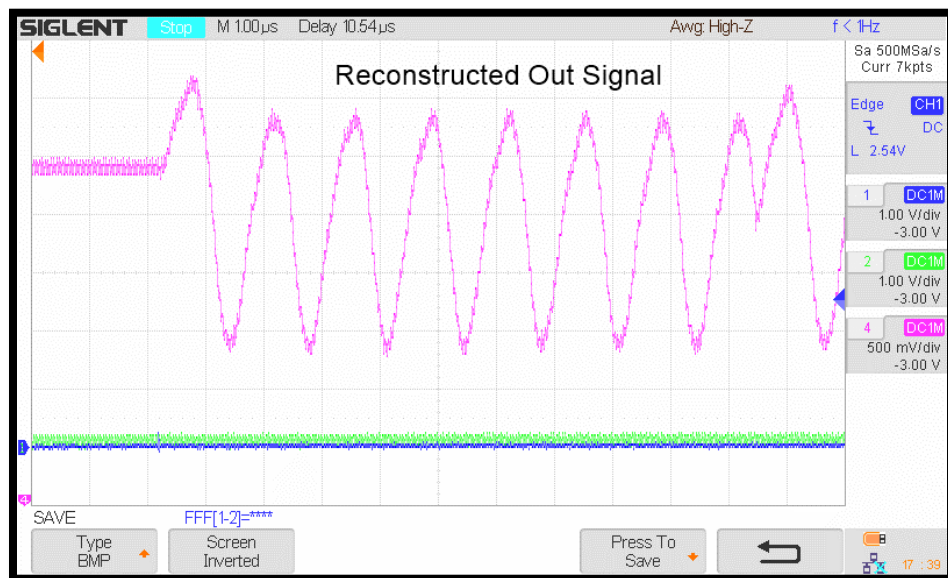

Figure 4.6 Reconstructed Captured Signal from Figure 4.5

Figures 4.7 and 4.8 repeat the test process with *vinvc* set to 1 Volt and the bias resistor set to 4 kOhms to demonstrate an even larger capture window. From Figure 4.7, the capture window has increased to 542 ns. Again, knowing there are 256 stages, the effective sampling rate can be calculated to be 472.32 MHz. Note that roughly 10.5 cycles of the 20 MHz sinewave is within the capture window.

Figure 4.7 Capture Window with 1 Volt on *vinvc* and a 4 kOhm Bias Resistor

Figure 4.8 shows that 10.5 cycles of the captured signal have been reproduced over 10 us effectively giving a 1 MHz signal.

Figure 4.8 Reconstructed Captured Signal from Figure 4.7

It is worth noting that the amplitude of the reconstructed signal is set by the value of the pull-up resistor, as discussed in Chapter 2. A side by side comparison of the experimenta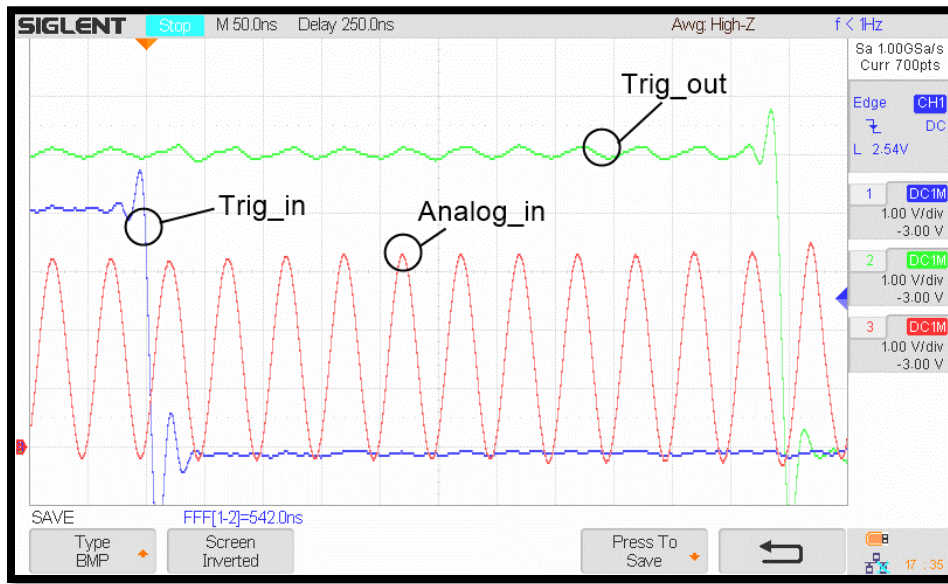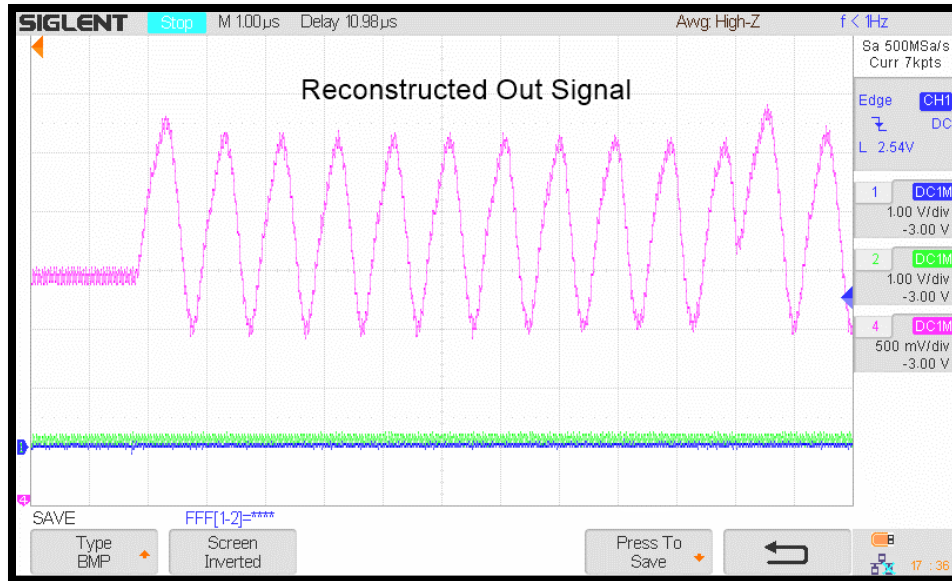l results and simulation results are provided in Table 4.1. Note the slight variations from the experimental and simulated results previously summarized in Table 2.3. These variations are probably due to the extra parasitics associated with the PCB traces, layout routing, the on-chip pads, and the package. For example, the simulations do not account for the extra parasitic capacitances associated with the bonding pads or the inductive parasitics associated with the wire bonds connecting the IC to the package. Additionally, the impedance of the bias resistor will have variance. These parasitics, albeit small, will affect the test results. The ability to vary the ASIC's sampling rate allows for compensation of the parasitics in any application. The system the VFTD will be utilized should include a feedback look that will monitor the size of the capture window and adjust *vinvc* accordingly. As an example, an application requiring a specific capture window may require a 1 GHz sampling rate. Based upon simulations, *vinvc* would be roughly 1 Volt and a 2 kOhm bias resistor would be used. However, the experimental results demonstrate how

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parasitics may reduce expectations by almost 50 %. This issue can be solved simply by adjusting

vinvc and/or the bias resistor.

Test	*Vinvc* (V)	Bias Resistor (kΩ)	Capture Window (ns)	Sampling rate
Experimental	5	2	81	3.16 GHz
Experimental	1	2	384	666.66 MHz
Experimental	1	4	542	472.32 MHz
Simulated	5	2	75.48	3.39 GHz
Simulated	1	2	294.85	949 MHz
Simulated	1	4	380.58	672 MHz

Table 4.1 Consolidated Testing Results

Chapter 5 Conclusion

The VFTD design goal was to increase the number of useful applications of the FTD designed by Buck and Baker. The addition of current starved inverters and a voltage-controlled bias generator to the capture stage from the original FTD created a voltage-controlled variable delay line that utilizes on chip capacitors for capturing and storing fast analog signals and pulses. The test results verify the VFTD operates within design goal objectives by demonstrating the ability to capture and recreate signals at a slower rate with a variable capture window. However, the available test equipment was insufficient to test the VFTD to the upper limits.

The Nyquist Sampling Theorem requires signals to be sampled at a minimum of twice their frequency to prevent the loss of signal. Based upon the experimentally determined maximum sampling rate of 3.16 GHz, the VFTD can theoretically sample frequencies up to 1.58 GHz. Redesigning the bias generator such that the bias voltages approach the rail voltages could increase the sampling frequency up to 5 GHz. The redesign could theoretically result in a new maximum input frequency of 2.5 GHz.

Referring to the capture stage unit cell in Figure 2.12, future work could include removing the lower NMOS, *N5*, from the current starved inverter as the time it takes for the NMOS, *N2*, to turn on does not need to be limited. Removing *N5* allows *N2* to turn on at the fastest possible rate, wherein *N2* can still turn off at a variable rate due to PMOS *P5*. This would eliminate one NMOS from each capture stage cell, equating to a reduction in MOSFET devices equal to the number of capture stages implemented for user specific applications. This would also allow for a more linear bias generator to be designed resulting in a single bias voltage, *vbiasp*, that approaches the rail voltages. Another benefit would be a reduction in trace routing during layout due to not needing *vbiasn*.

Another possible improvement would be to attempt to increase the overall sampling rate of the VFTD by using multiple interleaved banks of unit cells. Using interleaving could effectively increase the sampling by a rate equivalent to the number of banks. However, interleaving would require the creation of separate triggers for each bank separated in time by a delay equivalent to the time delay through a single capture stage divided by the number of banks.

References

[1] K. Buck and R. J. Baker, "Fast Transient Digitizer Chip for Capturing Signle-Shot Events," in *12th IEEE Dallas Circuits and Systems Conference*, Dallas, 2016.

[2] R. J. Baker, CMOS Mixed Signal Circuit Design, 2nd ed., Hoboken, NJ: Wiley, 2009.

[3] MOSIS, "C5 Process: ON Semiconductor 0.50 μm," [Online]. Available: https://www.mosis.com/vendors/view/on-semiconductor/c5. [Accessed 2018].

[4] R. J. Baker, CMOS Circuit Design, Layout, and Simulation, 3rd ed., Hoboken, NJ: Wiley, 2010.

[5] A. S. Sedra and K. C. Smith, Microelectronic Circuits, 6th ed., Oxford, England: Oxford University Press, 2009.

Appendix

Arduino Code

```
const int buttonPin1 = 2;    //Input pin for output triggers

const int pin1 = 10;  //Function generator Trigger

const int pin2 = 11;  //FTD Trigger

const int pin3 = 12;  //V enable for counter/decoder

int buttonState1;


void setup()

{

 pinMode(buttonPin1, INPUT);

 pinMode(pin1, OUTPUT);

 pinMode(pin2, OUTPUT);

 pinMode(pin3, OUTPUT);

}


void loop()                // run over and over again

{

 int reading = digitalRead(buttonPin1);

   buttonState1 = reading;

  delay(250);


   if (buttonState1 == HIGH) {
```

```
    digitalWrite (pin1, HIGH);

    //delay(0);

    digitalWrite (pin2, LOW);

    digitalWrite (pin3, HIGH);

  } else {

    digitalWrite (pin1, LOW);

    digitalWrite (pin2, HIGH);

    digitalWrite (pin3, LOW);

  }

}

//Pin 10 output to trigger the function generator

//Pin 11 output to trigger FTD

//Pin 12 out to enable the counter/decoder of FTD

//Pin 2 input trigger to start output triggers
```

CURRICULUM VITAE

Graduate College

University of Nevada, Las Vegas

James Mellott

Degree:

Bachelor of Science, Electrical and Computer Engineering, 2017

University of Nevada, Las Vegas

Employment:

Vorpal Research Systems Inc. 2018 - Present

University of Nevada, Las Vegas (UNLV) 2017 - Present

Thesis Title:

Variable Transition Time Inverters in a Digital Delay Line with Analog Storage for

Processing Fast Signals and Pulses

Awards:

Spring 2017 Senior Design Competition: Grand Prize, Sustainability