USING DELTA-SIGMA MODULATION FOR SENSING IN A CMOS IMAGER

by

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The project presented by Dennis Glen Montierth entitled USING DELTA-SIGMA MODULATION FOR SENSING IN A CMOS IMAGER is hereby approved:

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I would also like to thank my family for their patience and help. In particular, I would like to thank my wife, Shawnee, for her love and support during all of the hectic times. To my eldest son, Dustin, thanks for taking the time to help me collect data on the test chip.

ABSTRACT

CMOS Image Sensors are used in a wide variety of applications today, including digital still cameras, video cameras, cellular phones, applications for car sensors (including back up cameras), and many other products. The majority of CMOS image sensors use a pipeline analog-to-digital converter (ADC) to turn an analog voltage, produced from light incident on a pixel, into a digital signal. This research explores the benefits of using delta-sigma modulation for column parallel sensing in lieu of a traditional analog scheme using a pipeline ADC. The benefits include an increase in signal to noise ratio (SNR), low power circuits, a small layout area, fast design times, and circuits that are easy to design for higher speeds. Results, obtained from a test chip fabricated using the AMI 500 nm process, are presented. Running at a clock rate of 100 MHz with a 20 us row sense time gives a resolution of 10 Bits. At this rate, a 2000 column imager will output a pixel every 10 ns.

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LIST OF ABBREVIATIONS

ADC	Analog-to-Digital Converter
APS	Active Pixel Sensor
CMOS	Complementary Metal-Oxide Semiconductor
DAC	Digital-to-Analog Converter
DSM	Delta-Sigma Modulator
FPN	Fixed Pattern Noise
FPS	Frames per Second
LSB	Least Significant Bit
SNR	Signal to Noise Ratio
TSPC	True Single Phase Clock

CHAPTER 1 – INTRODUCTION

1.1 Motivation

Today's CMOS image sensors primarily use pipeline ADC's to convert voltages produced by pixel integration to a digital output. Different regions or color planes often have separate ADC's. Multiple columns are output onto a shared ADC. As demand for larger array sizes increase, issues with routing the pixel outputs while minimizing variation and noise to a shared ADC becomes a challenge.

Engineers are always trying to reduce power consumption on imager designs for low power applications, such as cell phones. The analog circuitry for signal gain and pipeline ADC's contribute to the majority of the power consumption in a CMOS imager. The analog devices are specific to process and the design consumes significant engineering time.

Noise is important in imager designs because it leads to noise in the image. This is especially the case with low light/greater gain because with lower signal amplitudes there is a corresponding reduction in signal-to-noise ratio (SNR). Flicker and thermal noise are the largest contributors to noise in CMOS imager design.

Smaller designs lead to a decrease in overall cost. This is also important for applications that require a small package size for sleek compact designs. Using a smaller

area for periphery also allows more area for pixel size based on a particular die size target. Larger pixels result in a higher quality image [1].

Depending on the application, speed can also be an issue in imager design. The pixels integrate and output a row at a time for a CMOS imager. The slower the clock rate, the more time an image will move during the capture. This results in image skew. Pipeline ADC and gain stages become tougher to design with increasing speed. A faster clock rate also requires additional power consumption for the analog devices in the design.

The imager ADC and gain stage using delta-sigma modulation presented in this research will address all of these issues. Routing issues, which get worse with increased array size, are no longer a concern since each column line uses a separate DSM ADC. Averaging thermal noise leads to an increase in SNR. The DSM ADC's are low power circuits that contribute to a decrease in overall power consumption. Increasing speed on these designs is much simpler. The gain stages and Pipeline ADC's on conventional designs require significant layout space. The DSM ADC presented in this design has a very small footprint. The DSM ADC is also able to amplify the signal using a reference voltage supplied to the ADC optimizing the dynamic range based on the range of the input. Using a DAC and a register, different reference voltages supplied to the DSM ADC amplify the signal prior to converting to a digital value. This results in a large decrease in layout area since traditional gain stages can take up a lot of space. Design times will decrease since this topology will scale where the Pipeline ADC's do not and the design is very simple [2].

1.2 CMOS Image Sensor Pixel

One version of the Active Pixel Sensor (APS) consists of a photodiode, a source follower, and a reset device as shown in Figure 1.2.1.

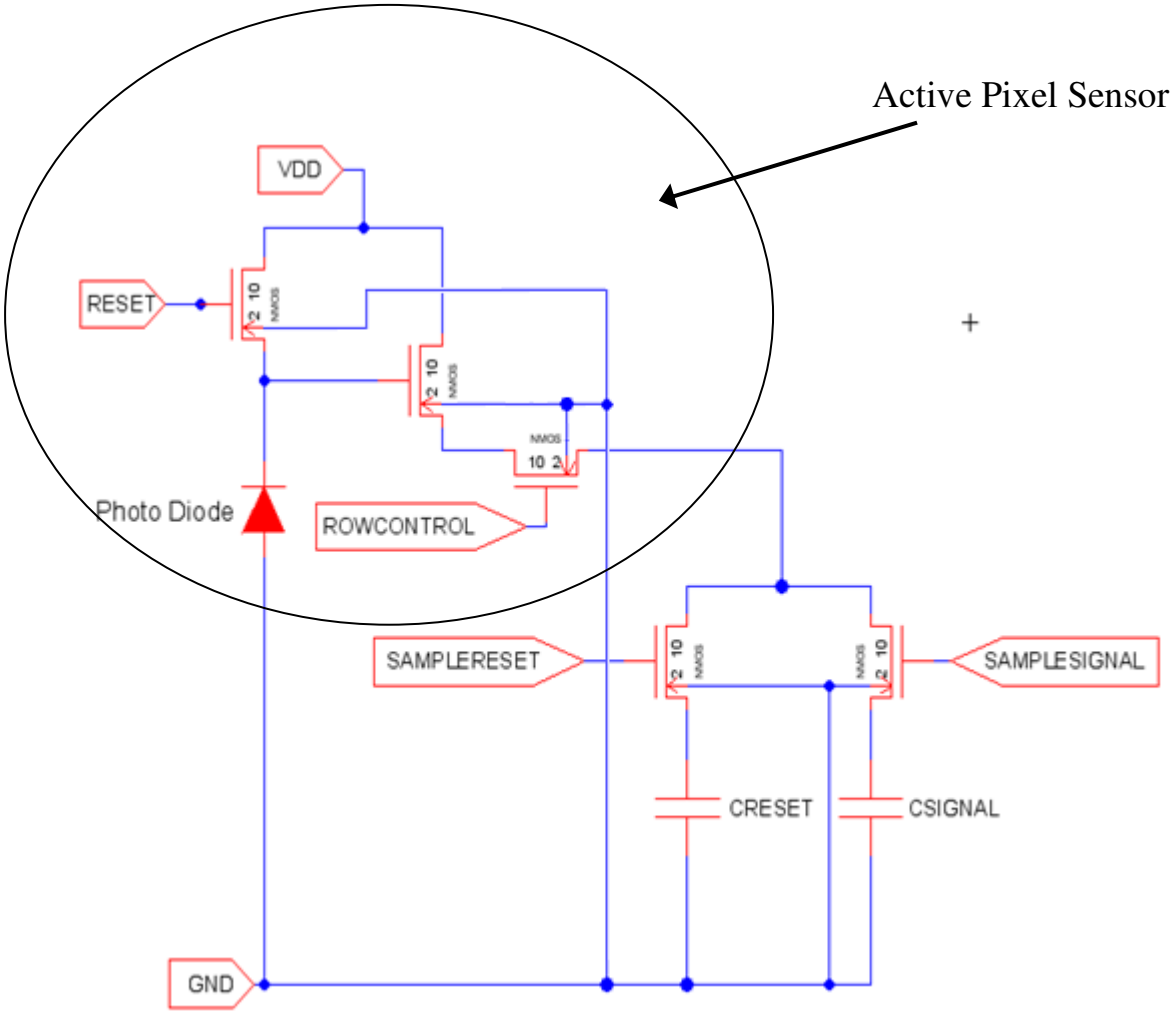

Figure 1.2.1 – APS connected to a column that reads out reference and signal voltages onto storage nodes for sensing.

The operation of the APS starts out with the RESET signal going high in order to charge the storage node (This is the node connected to the cathode of the photo diode in

Figure 1.2.1). The ROWCONTROL signal also needs to go high in order to access one pixel per column line. The source follower input is charged to a threshold voltage below V_{AA}. SAMPLERESET will then pulse high and the reset voltage will get stored on C_{RESET}. Next, with the RESET signal low, the storage node will discharge at a rate proportional to the amount of light incident on the photodiode. A constant integration time is allowed to pass followed by the output being stored on the C_{SIGNAL} capacitor by pulsing SAMPLESIGNAL high. The reset voltage stored on C_{RESET} is necessary for correlated double sampling (CDS). CDS involves storing the reset and signal voltages on different capacitors and using them as a differential input. The time between storing the reset and signal voltage needs to be minimized. This reduces fixed pattern noise (FPN) from pixel device variation and helps to eliminate flicker noise. At this point, there is a need to amplify the differential signal and convert the analog representation into digital one. This is the area that this research is focused on which is being referred to as *sensing*. The differential output of the active pixel sensor (APS) has, ideally, a linear relationship to the voltage on the input of the source follower [1][3].

1.3 Thesis Contribution

This thesis looks at advantages of the DSM ADC. Comparison to the pipeline ADC, which is the topology most widely used at the time of this writing, is examined. The operation of the DSM ADC is covered. Special attention to techniques used to reduce FPN and increase the ADC dynamic range based on the differential input are included.

CHAPTER 2 – IMAGER ADC USING DELTA-SIGMA MODULATION

2.1 CMOS Imager DSM Circuit Operation

The differential output voltage stored on the reset and signal capacitors, as pointed out in Section 1.2, are output to high impedance gates as shown in Figure 2.1.1 (V_{RESET} and V_{SIGNAL} voltages). The reset path mirrors the current to the signal path. The current difference between the reset and signal paths charge flows to C_4 (V_{BUCKI}).

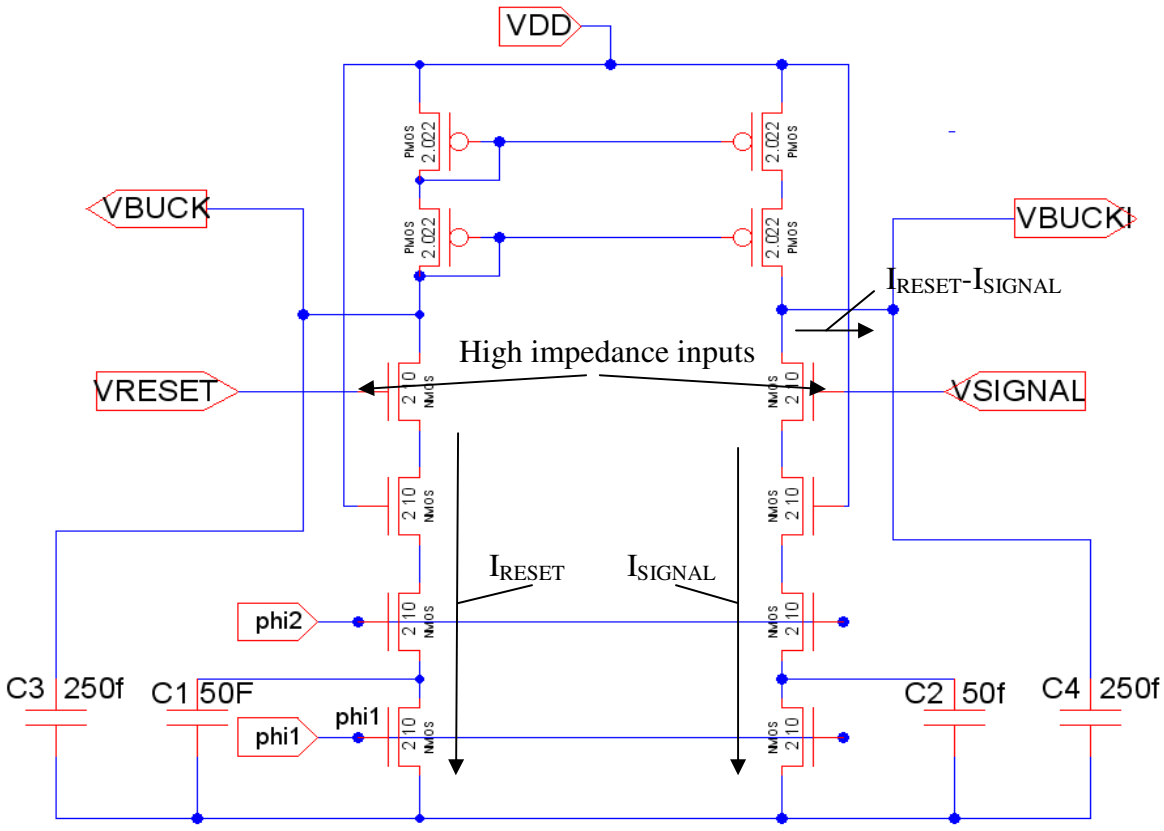

Figure 2.1.1 - DSM circuit without the comparator or difference path.

Switch capacitor resistors are used with non-overlapping clocks, phi1 and phi2 (shown in Figure 2.1.2), controlling the charge transfer.

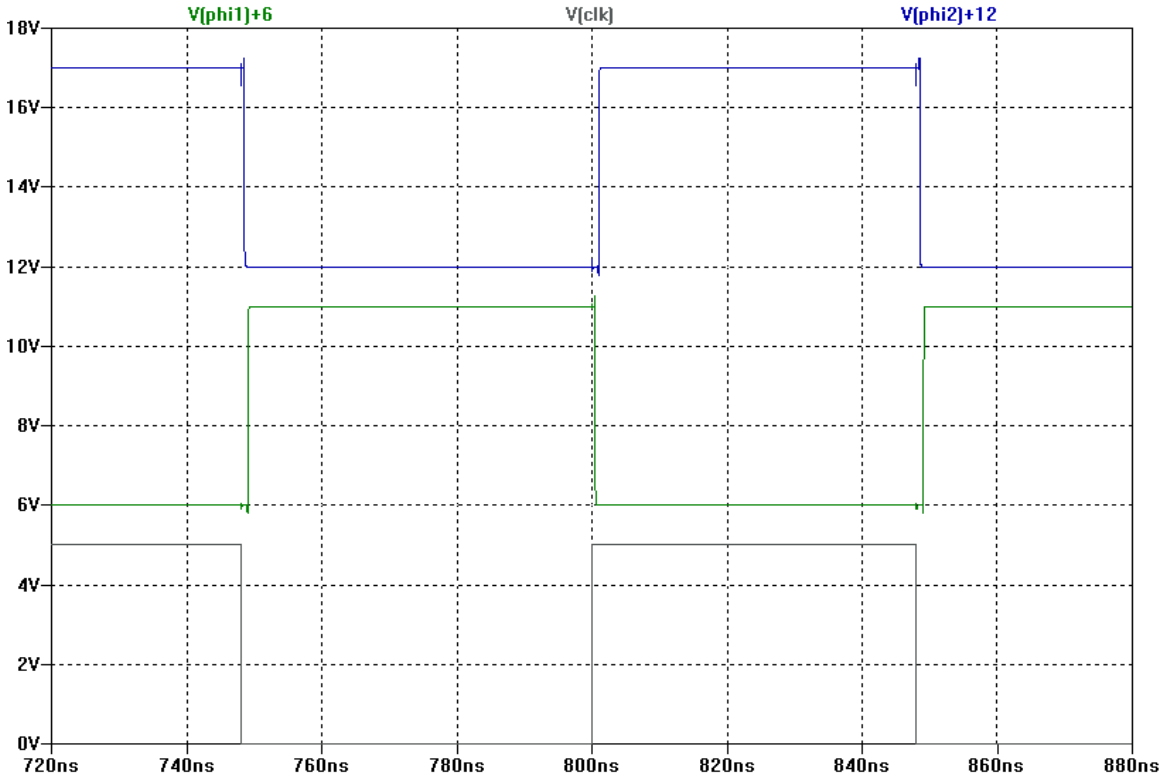

Figure 2.1.2 – Simulation of the clock generator at 10MHz. An offset voltage was added to phi1 and phi2 for display purposes. Looking closely you can see that phi1 and phi2 are non-overlapping clocks.

This topology allows for variation in the reset and signal capacitances (C_{RESET} and C_{SIGNAL}) without creating column FPN because there is no charge sharing when the sense occurs. V_{BUCK} and V_{BUCKI} signals route to a comparator that feeds back to Q. When V_{BUCKI} becomes larger than V_{BUCK}, Q turns on removing a fixed amount of charger per cycle that it is high. The control gates for the signal and reset paths are tied to VDD.

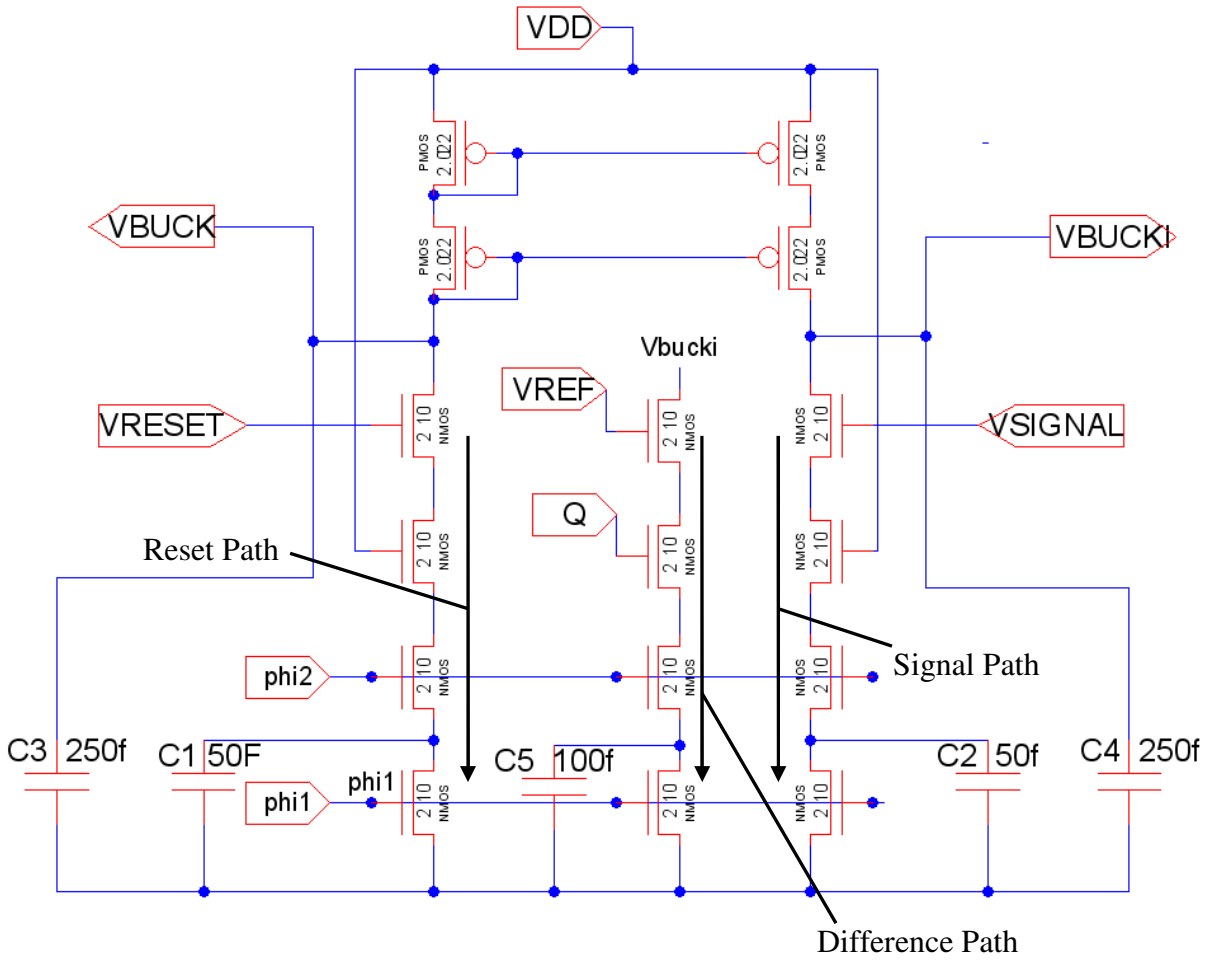

Figure 2.1.3 – DSM circuit without the comparator or path switching circuits. V_{BUCK} and V_{BUCKI} outputs connect to a comparator. This provides feedback through control signal Q.

Shown in Figure 2.1.4, signal Q (signal_q) goes high when V_{BUCKI} is greater than V_{BUCK}. The number of times that the signal Q has to go high relates to the differential voltage applied to V_{RESET} and V_{SIGNAL}.

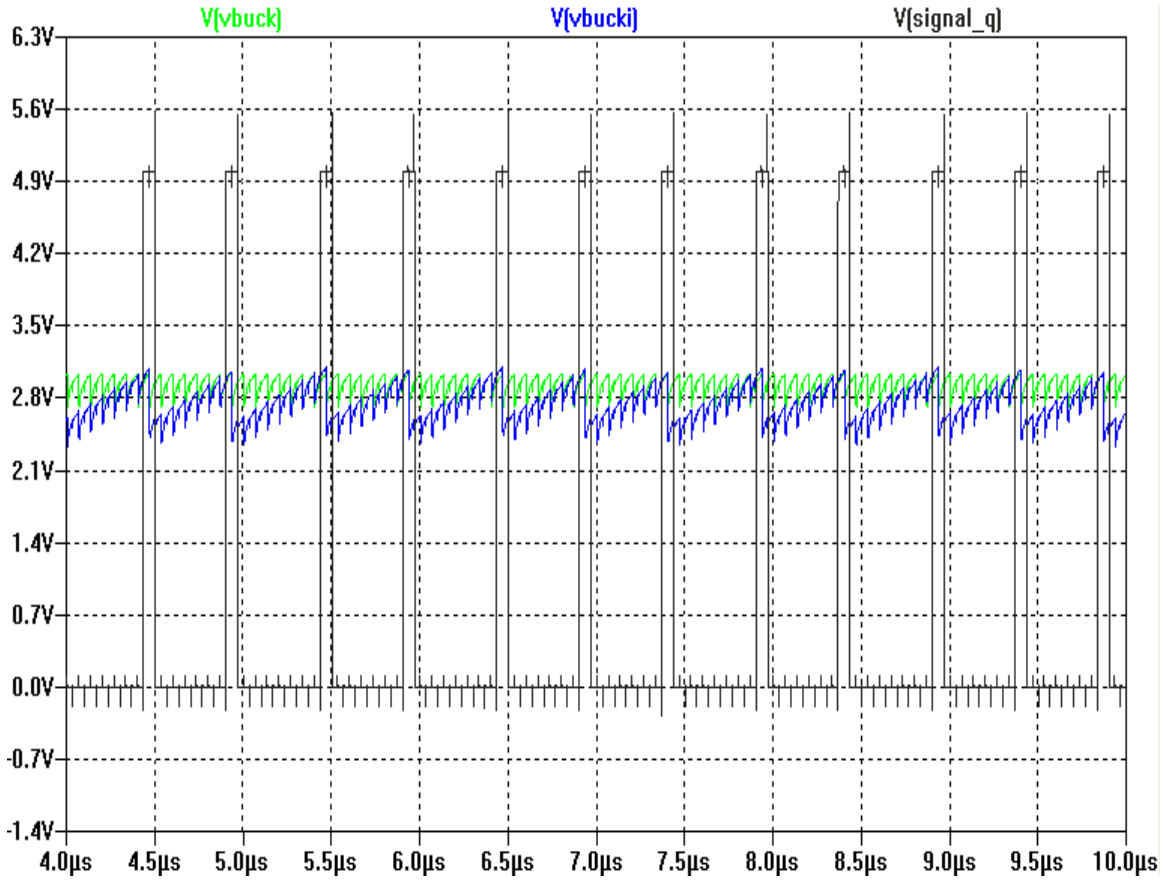

Figure 2.1.4 – Simulation showing when V_{BUCKI} is larger than V_{BUCK} signal, Q turns on pulling additional charge off the V_{BUCKI} capacitor.

The idea is that the amount of current through the difference and signal path equals the amount of current through the reset path, as the sense time gets long. Q keeps track of the current difference between the reset and signal paths. The signal Q is output to a low pass filter, a counter, to obtain a digital output.

$$I_{RESET} = I_{SIGNAL} + I_{DIFFERENCE} \tag{2-1}$$

Equation 2-1 is true over time. Quantized values substituted later in this equation give a solution for the total count. Equation 2-1 can be written in terms of the reset and signal voltages. This equation was simplified given the fact that $R_R = R_I$.

$$V_R - V_I = \left(V_{REF} - V_{THN}\right) \cdot \frac{R_{I,R}}{R_Q} \tag{2-2}$$

Using the equation the equation for a switched-capacitor resistor [3] of

$$R = \frac{\mathrm{N}}{Ccup \cdot f \cdot M} \tag{2-3}$$

N is the number of clocks and M is the number of clock cycles in which the Switch Capacitor Circuit is enabled. Combining Equation 2-2 and Equation 2-3 then solving for the number of counts when Q is enabled you obtain the following equation (M needs to be rounded down to the nearest integer):

$$M = \frac{\left(V_R - V_I\right)}{\left(V_{REF} - V_{THN}\right)} \cdot \frac{C_{1,2}}{C_5} \cdot N \tag{2-4}$$

Signal Q is output to a counter used as a low pass filter for an image sensor design to obtain M. One thing to pay attention to in Equation 2-4 is that it does not make sense for M to be greater than N. At the point where M = N, the difference in charge moving onto V_{BUCKI} is larger than the amount of charge that is removed with Q enabled. The result will always be the maximum count N because Q is always on.

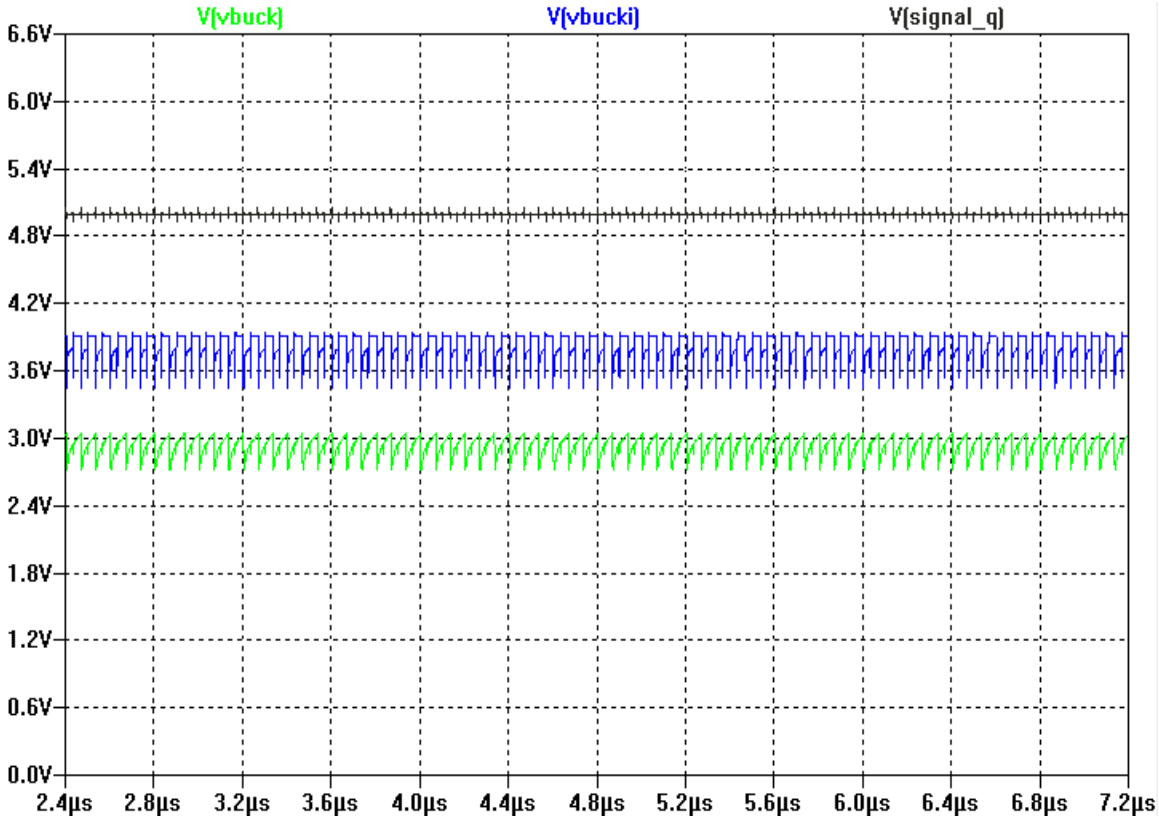

Figure 2.1.5 – Signal Q is always on because the differential difference is so large that the difference path removes less charge than the amount added to V_{BUCKI} during each clock cycle.

The important aspect for Equation 2-4 is the linear dependence based on the difference between V_R and V_I. There is no frequency dependence in the final equation. The switched-capacitor resistor equation assumes that the circuit is operating in a frequency range where the capacitor charges or discharges fully [3].

2.2 Resolution and Input Range

Since the output of the ADC is digital, the smallest nonzero count possible is a digital one. Setting M to a one in Equation 2-4 provides the smallest difference that can be resolved (Equation 2-5). The resolution increases as the number of samples increase. Also shown later is the fact that a larger sample size will decrease the impact of thermal noise.

$$Resolution = \left(V_{REF} - V_{THN}\right) \cdot \frac{C_5}{C_{1,2}} \cdot \frac{1}{N} \tag{2-5}$$

Solving for the resolution using V_{REF} of 1.9V, capacitances from the test chip design, and a 100MHz clock running for 20uS, results in a resolution of 1.2 mV. This resolution would require ten bits of output and would be in line with an ADC input range of 2.25V. This is approximately the linear range of the source follower in Figure 1.1.2 (Around 250 mV of margin ensures operation in the linear region of the APS pixel).

For a CMOS image sensor design, the minimum amount of total counts N is equal to the number of columns because the previous row would be clocking out while the next row is sensing. Using a clock multiplier to increase the DSM ADC speed relative to the master clock would increase resolution by a factor of the multiplier.

$$Resolution = \left(V_{REF} - V_{THN}\right) \cdot \frac{C_5}{C_{1,2}} \cdot \frac{1}{Columns \cdot Multiplier} \tag{2-6}$$

The dynamic range is limited either by the input to the ADC or the number of clock cycles. The total number of output bits must correspond to the maximum output. The input range of the ADC is obtained using equation 2-4 and setting M equal to N.

$$ADC\ Input\ Range = \left(V_{REF} - V_{THN}\right) \cdot \frac{C_5}{C_{1,2}} \tag{2-7}$$

For the chip fabricated for this thesis, the capacitance ratio in Equation 2-7 is two. The output of the source follower from Figure 1.2.1 is linear from around 1V to 3.5V. The ADC Input range would need to be 2.5V in the case that the APS outputs were utilizing the full output range. As calculated earlier using a V_{REF} value of 1.9 mV we get an ADC input range of 2.25V. In order to allow the largest range of amplification, use capacitance values that would put V_{REF} at the highest possible value when the ADC input range is equal to the full range of the APS. Section 2.4 will cover V_{REF} limitations.

2.3 Test Chip and Simulation Results

Test chip results, simulation, and calculated values match very closely. Figure 2.3.1 shows data points taken at 10 mV intervals for both the actual test chip and calculations.

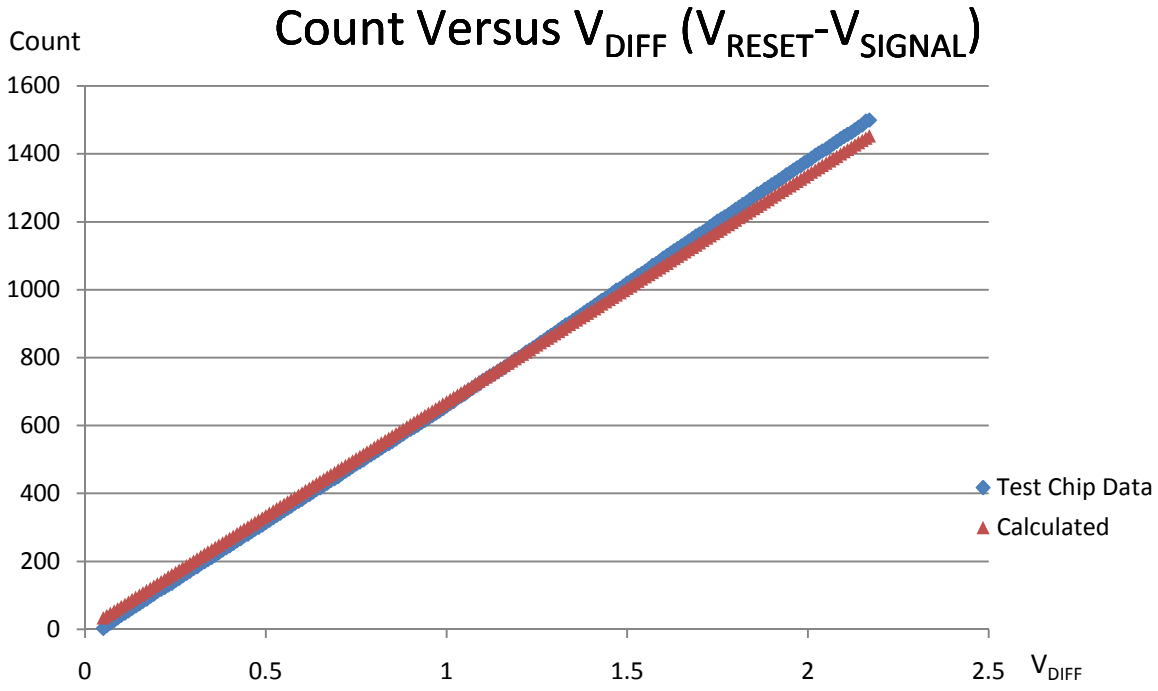

Figure 2.3.1 – Calculated and test chip values for 15MHz with a sense time of 100us and V_{REF} at 1.9V. The data points shown were taken at 10 mV increments. Calculated values are from Equation 2-4.

At an increment of 10 mV, the average step size is seven counts. In order to get an idea of the differential non-linearity, the count for every 10 mV increment is compared to the average count per 10 mV increment. The resolution of the voltage supply is 10 mV so the accuracy of this is not perfect but demonstrates that the differential non-linearity (DNL) looks very good. The 10 mV limit in resolution on the supply did not allow testing of a single LSB step size.

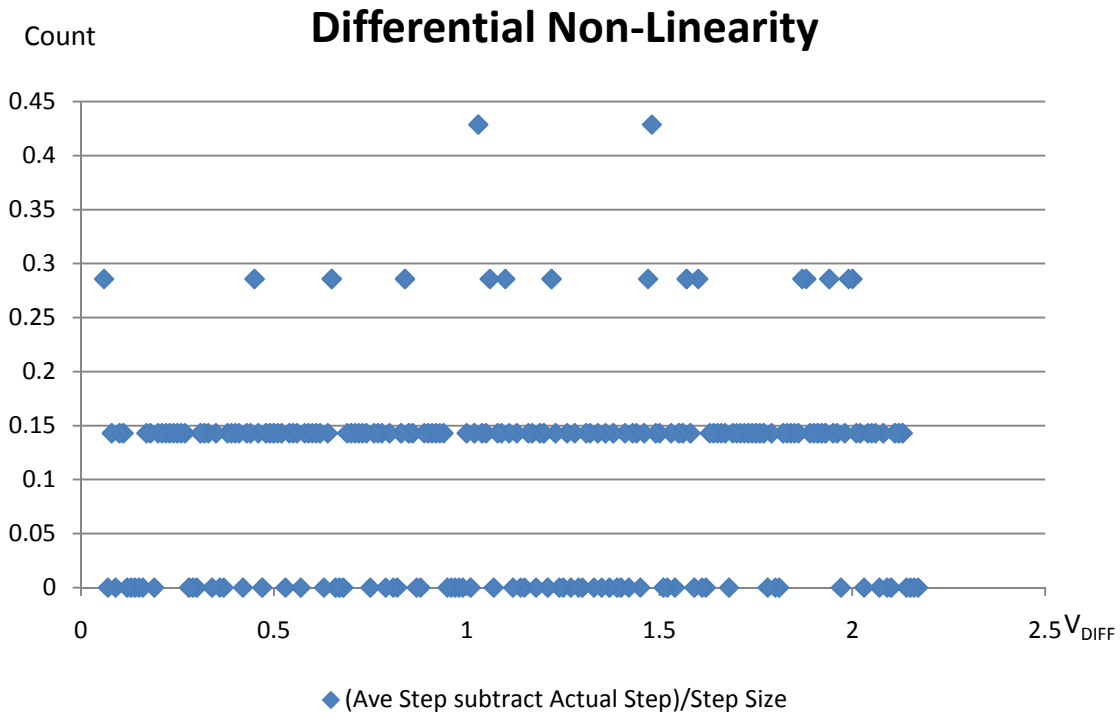

Figure 2.3.2 – DNL of the test chip based on the lowest step size being 7 counts. The dependant variable is equal to (Ave step Size of 10 mV – Actual step size at a particular V_{DIFF}) / (Average Step Size).

For the integral non-linearity (INL), a best fit line was compared with the actual count at each point of the differential voltage. The integral non-linearity is impressive; however, DNL is more of a concern for a quality imager. The other real important thing is column variation resulting in column FPN. This will be covered in Chapter Three.

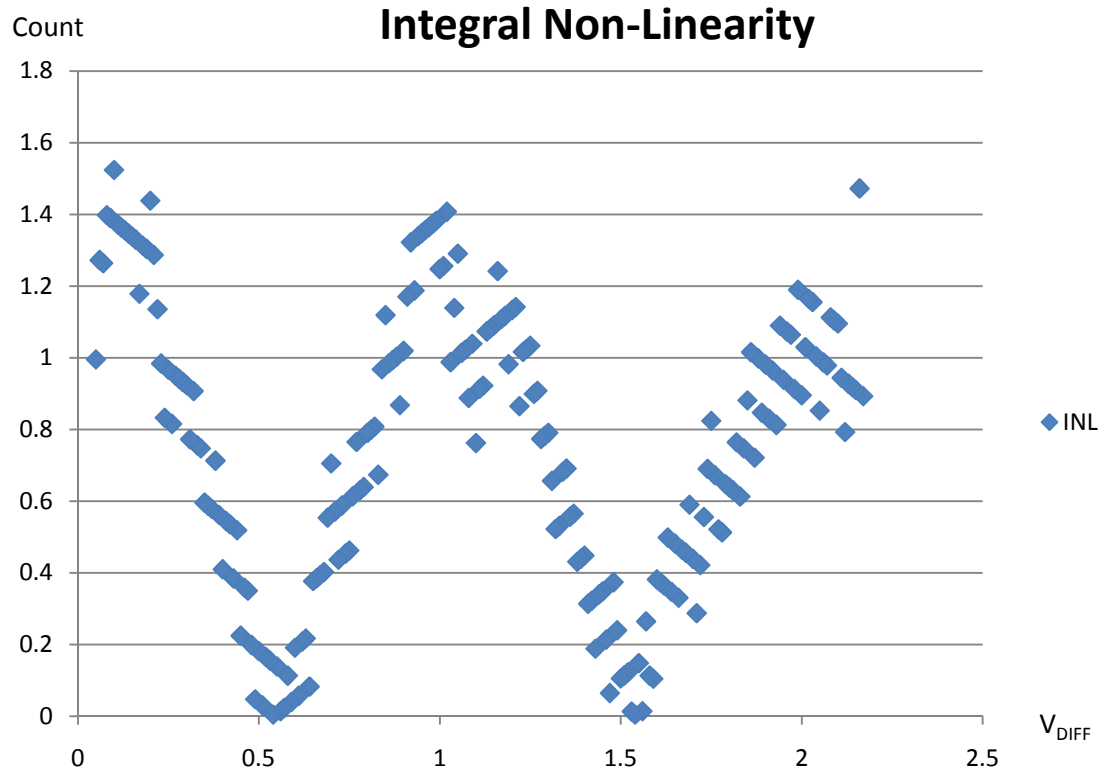

Figure 2.3.3 – Integral non-linearity. The actual count at each voltage point compared to a best fit line through the data points.

2.4 Maximizing the Dynamic Range of the ADC

The output of the APS source follower is dependent on the pixel integration time and amount of light incident on the pixel. In low light conditions, the output signal needs to increase by amplifying the signal in order to maximize the dynamic range of the ADC or suffer from long integration times. There is also a need to have control over the gain for other functions, such as white balancing (white balancing needs control of gain by

color). Signal gain is applied digitally after the DSM ADC, by utilizing features of the DSM ADC, or more than likely, by both methods.

One method of increasing the gain would be to increase the number of clock cycles per sense. However, there is a trade off. The speed of the imager, measured in frames per second (FPS), would decrease unless a higher frequency, using a multiplier, is used. Other methods of amplification would be a digital gain or by changing the V_{REF} voltage level on the ADC. The problem with applying digital gain is that the resolution is not increasing. In equation 2-7, a smaller V_{REF} will decrease the ADC input range for a given ADC output (an increase in signal gain because the output is larger for a smaller input difference). This is ideal since the output of the APS has a lower range. This effectively increases or maximizes the dynamic range of the ADC for the given input range (we are increasing our resolution within a smaller input range).

The advantage of using the V_{REF} voltage for gain control is that it is a common signal to all of the ADC's and by lowering it you are increasing your pixel resolution. A digital-to-analog converter (DAC), which will take up a very small amount of silicon, implements the gain control. V_{REF} control implemented for each color allows for functions, such as white balancing. V_{REF} signals route to the DSM circuit based on the bayer pattern as shown in Figure 2.4.1.

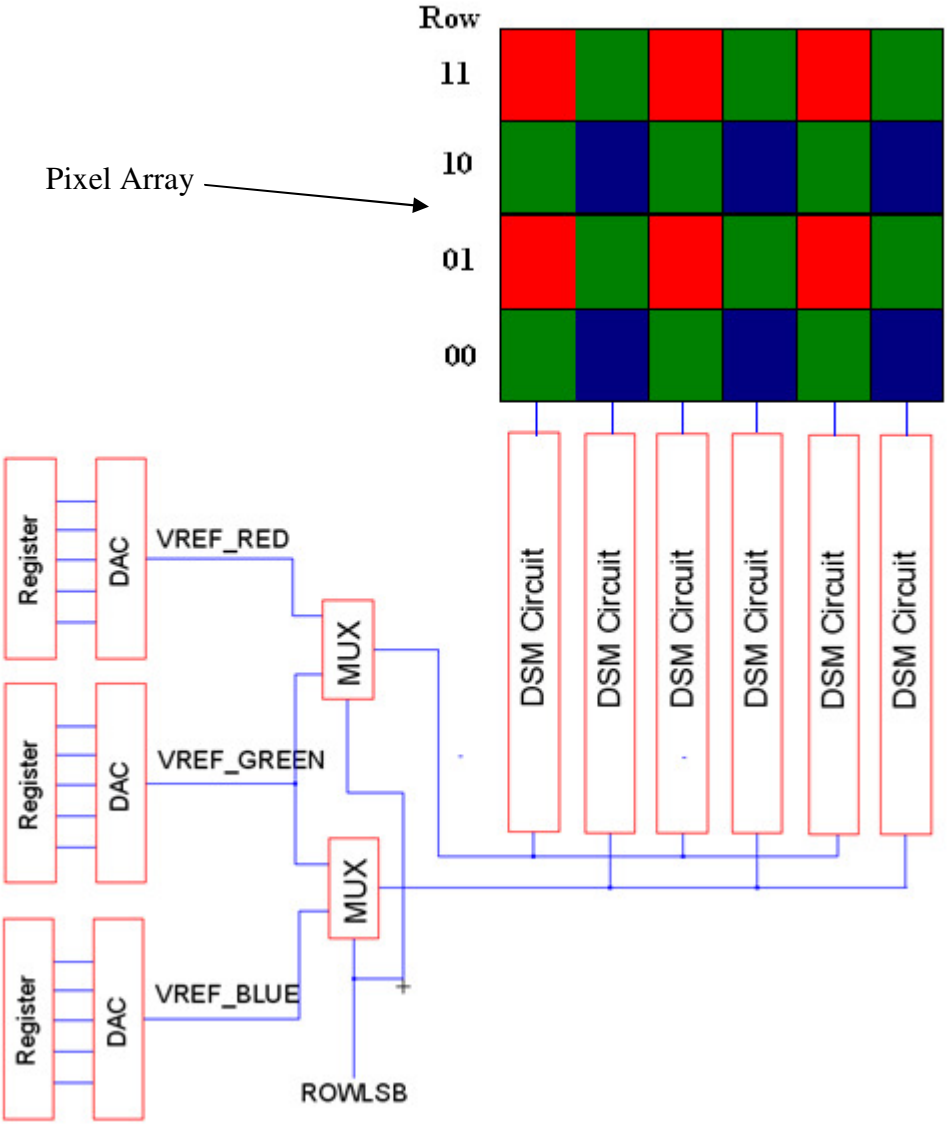

Figure 2.4.1 – V_{REF} control by using a register and a DAC. V_{REF} routes to the correct DSM circuit based on the bayer pattern and the row being output.

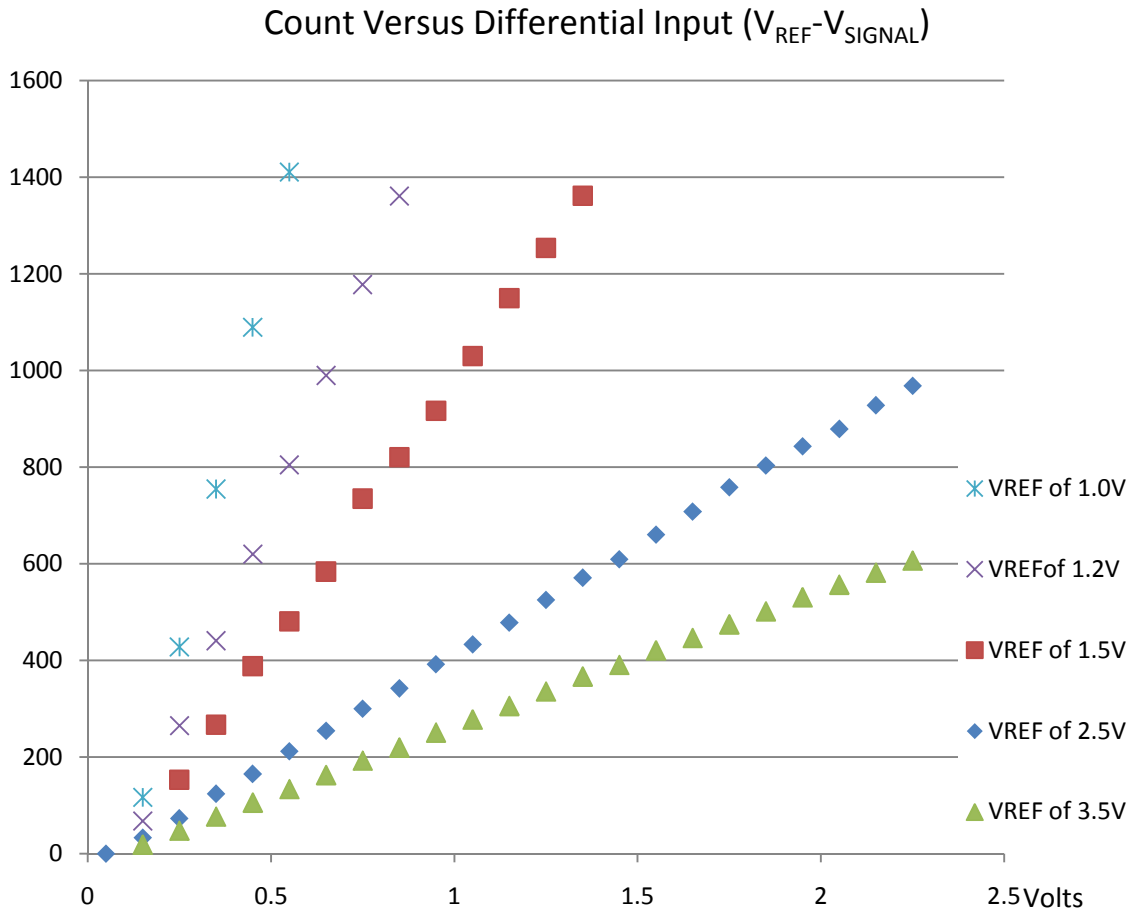

Figure 2.4.2 – Test chip results. 15MHz, 100uS with various V_{REF} values.

The amount of gain control relates to the ratio of the maximum and minimum V_{REF} values for the design as shown in Equation 2-8. For the test chip design, a maximum gain of 12.36 using V_{REFMAX} of 3.5V and V_{REFMIN} of 1V was calculated. Figure 2.4.1 shows that this closely matches the actual chip results.

$$Max\ Gain = \frac{(V_{REFMAX} - V_{THN})}{(V_{REFMIN} - V_{THN})} \tag{2-8}$$

If V_{REFMAX} is picked so the voltage on C_4 in Figure 2.1.1 does not drop below V_{REFMAX} minus a threshold voltage, the amount of charge that is removed by the difference path is fixed based on V_{REFMAX}. Once V_{REF} reaches the point where V_{REF} minus a threshold is larger than the minimum voltage on C_4, then the charge removed by the difference path will not increase with increasing V_{REF}. The V_{REF} voltage needs to be lower than this value. If the amount of charge removed is determined by the V_{BUCKI} voltage level rather than V_{REF}, offsets in the comparator will cause variation resulting in column FPN. For the test chip design, V_{REF} of 3.5V minus a threshold gives a voltage of around 2.7V to charge onto the capacitor before the transistor turns off. Based on simulation, a V_{REF} voltage of 3.5V will result in the minimum voltage on C_4 being 2.6V (this is the maximum value that can be charge onto the capacitor in the difference path). This means that increasing V_{REF} is no longer decreasing the gain. The maximum V_{REF} that should be used in this design is somewhere between 3.3V and 3.5V.

The source of column FPN resulting from a problem in the difference path can be narrowed down by taking a data point with a mid range V_{REF} and one where V_{REF} is large. The V_{REF} large data point will not suffer from an offset on the NMOS device and can be used as a reference point. (This is because the amount of charged dumped onto the capacitor in the difference path is based on the V_{BUCKI} voltage and not V_{REF}). If the column to column output differences show up with V_{REF} large and look to be due to the difference path (looks like a slope problem and not an offset difference), then it is probably caused by variation in the capacitance and not a mismatch on the device.

The minimum V_{REF} value of 1.0V, picked to illustrate test results versus theory when calculating the gain of 12.36, was the lowest value tested. The only restriction on the minimum V_{REF} value is that it needs to be larger than the threshold voltage. This allows for very large gains. However, variation in the threshold voltage from column to column will equate to a larger amount of column FPN as V_{REF} minimum approaches the threshold. More variation and noise at high gain is common to imager design; with increased gain more column FPN will be present in any topology. The ability to have so much gain control with such a small amount of extra silicon dedicated to this purpose is very exciting for this design.

Another method to increase gain would be to put an adjustable capacitance in place of C_5 in Figure 2.1.2 by switching in different size capacitors. One major disadvantage to this is that adding complexity to this part of the circuit can lead to a higher level of FPN as well as the fact that it takes up a lot of additional silicon.

2.5 Testing at Higher Frequencies

This design had a target frequency of 15MHz. This is a reasonable frequency for the AMI 500 nm process. Higher frequencies were tested to determine the limits of the test chip design.

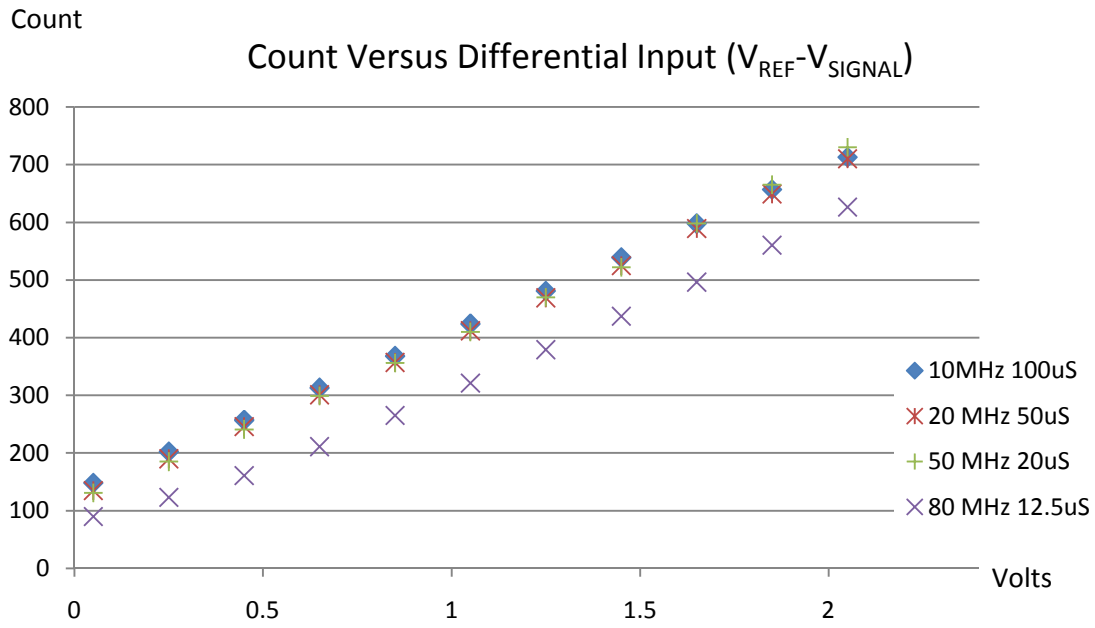

Figure 2.5.1 – Various frequencies with the sense time set so the counts should match. V_{REF} is at 2.5V.

As stated in Section 2.1, the count should be independent of frequency. In Figure 2.5.1 data at 80 MHz shows a count which is considerably lower than at other frequencies. This relates to not giving enough time for capacitors C_1, C_2, and C_5 to charge adequately. Using larger devices would allow for higher frequencies by decreasing the time constant. The issue becomes more apparent as the differential input gets larger. This relates to the reset (or reference) capacitor (C_1 in Figure 2.1.2) not charging as close to its full level compared to the signal capacitor (C_2 in Figure 2.1.2). The signal capacitor does not have to charge to near as high a voltage level because of the large differential input. This is apparent in simulations that ran at 100 MHz on the chip layout.

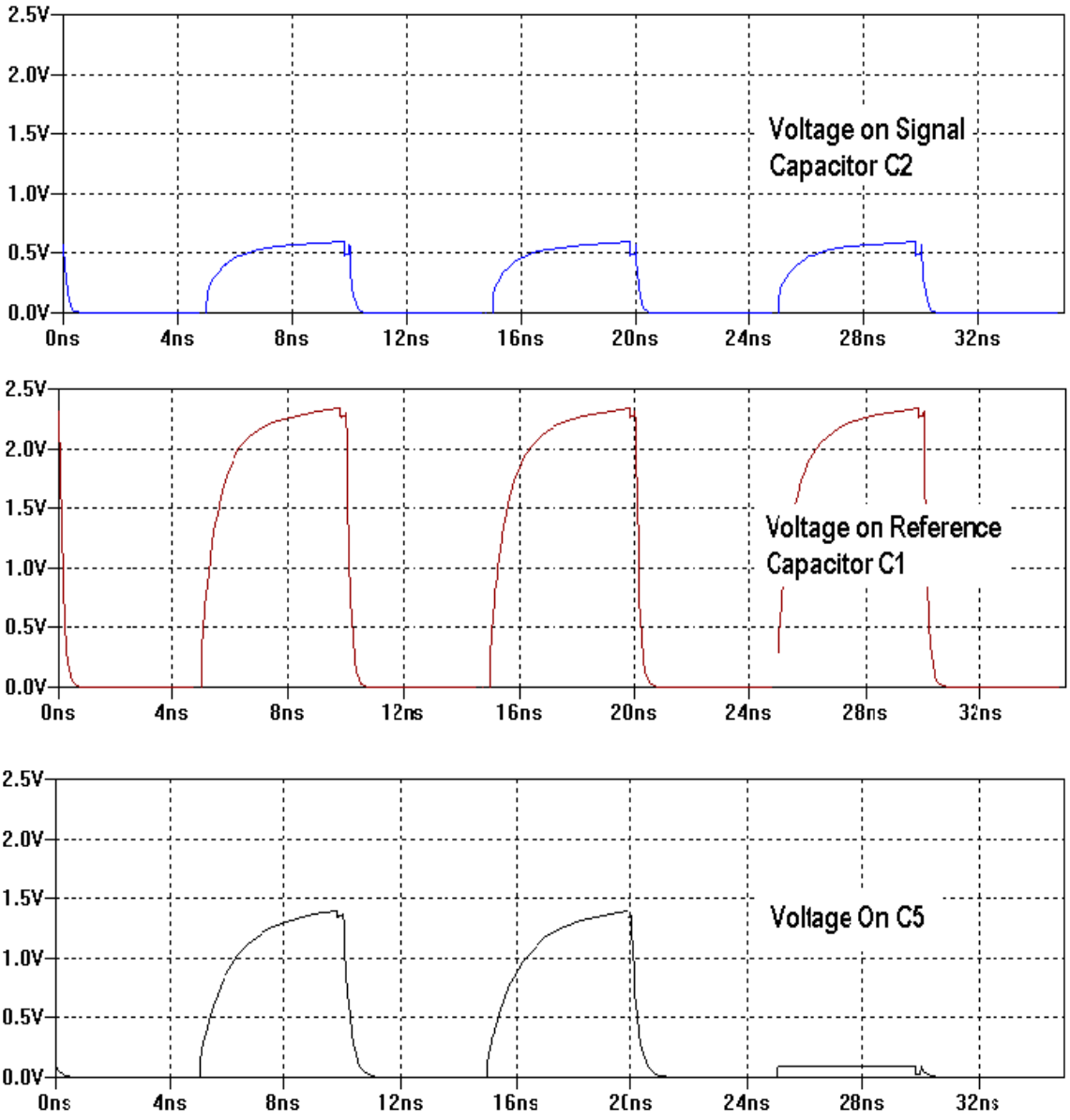

Figure 2.5.2 – Simulations performed on the layout of the test chip to show that all of the capacitors are not fully charging at 100 MHz because of the RC time constant. Notice the missing pulse on the Voltage on C5. This is because Q is not on for that cycle.

CHAPTER 3 – NOISE CONSIDERATIONS

3.1 FPN from DSM Signal Paths and Device Mismatch

Offset differences in the signal and reset paths and differences in the signal versus reset devices of the DSM will result in fixed pattern column noise. The error in count due to an offset on the ADC input is derived using equation 2-4.

The offset can be the result of path differences between V_{RESET} and V_{SIGNAL} or device mismatch. As shown in Equation 3-1, the offset has no dependence on the actual signal and reset voltages. A difference in the capacitance of C_1 and C_2 can also cause a difference in count leading to column FPN.

$$Offset\ Count = \frac{C_{1,2}}{C_5} \cdot \frac{V_{OFFSET}}{\left(V_{REF} - V_{THN}\right)} \cdot N \tag{3-1}$$

Adding circuitry to swap paths at the midpoint during the sense will address these differences. This can be accomplished by adding a few routing transistors as shown in Figure 3.1.1, which will switch the circuitry used for outputs to the comparator and the inputs to the reset and signal inputs. The select signal (SL) is held high during the first half of the sense then low during the second.

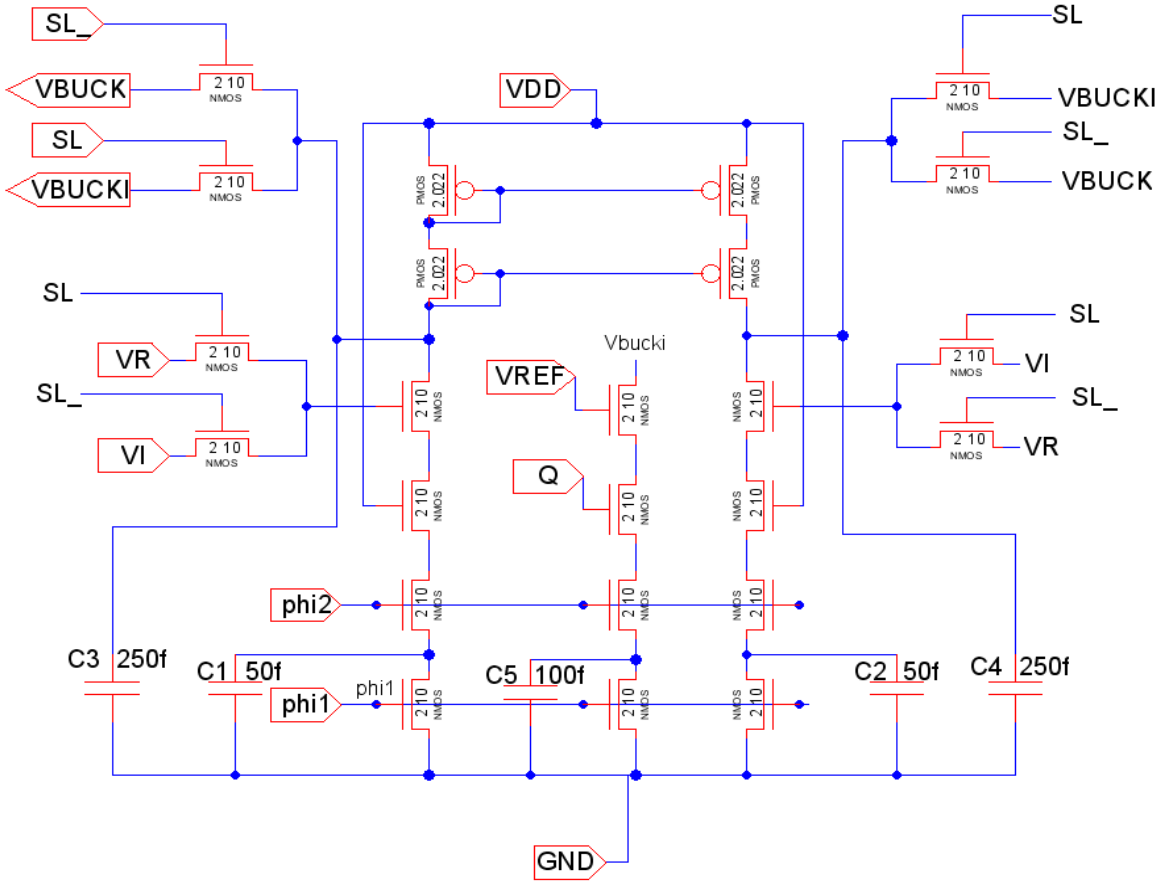

FIGURE 3.1.1 – SL and SL_ switch paths at the sensing midpoint to average out the offset.

The idea is to switch the signal paths midway through the sense in order to cancel out the effects of device mismatches, path differences, and differences in capacitance between C_1 and C_2 (If the C_1 and C_2 differences do not average to the ideal values they will still introduce column FPN. This will be shown, later, when difference path noise is examined). A 75 mV offset was used during the simulation to show how the offset is removed by using this topology.

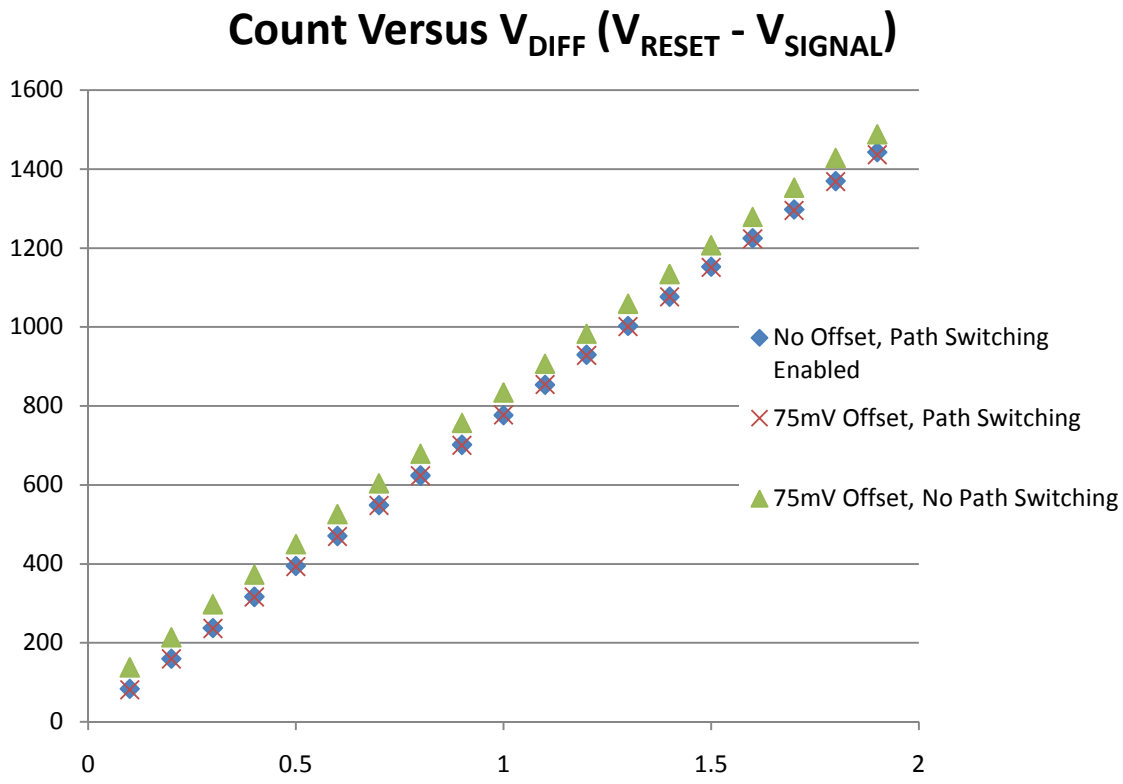

Figure 3.1.2 – Simulation ran to show the effects of path switching on a signal or reset offset.

The test chip design used near minimum device sizes. This is ideal for demonstrating offset cancellation because these devices are likely to have larger offsets. Looking at test chip data shown in Figure 3.1.3, the offset is equal to the point where the graph crosses the x-axis. Data collected on six outputs shows an offset as large as 150 mV. The other thing to pay special attention to is that the slope of OUTPUT #1 looks noticeably different. Variation in the difference path is the most likely suspect for a difference in the slope. The magnitude of output differences (column variation) in Figure 3.1.3 would result in a large amount of column FPN in an image.

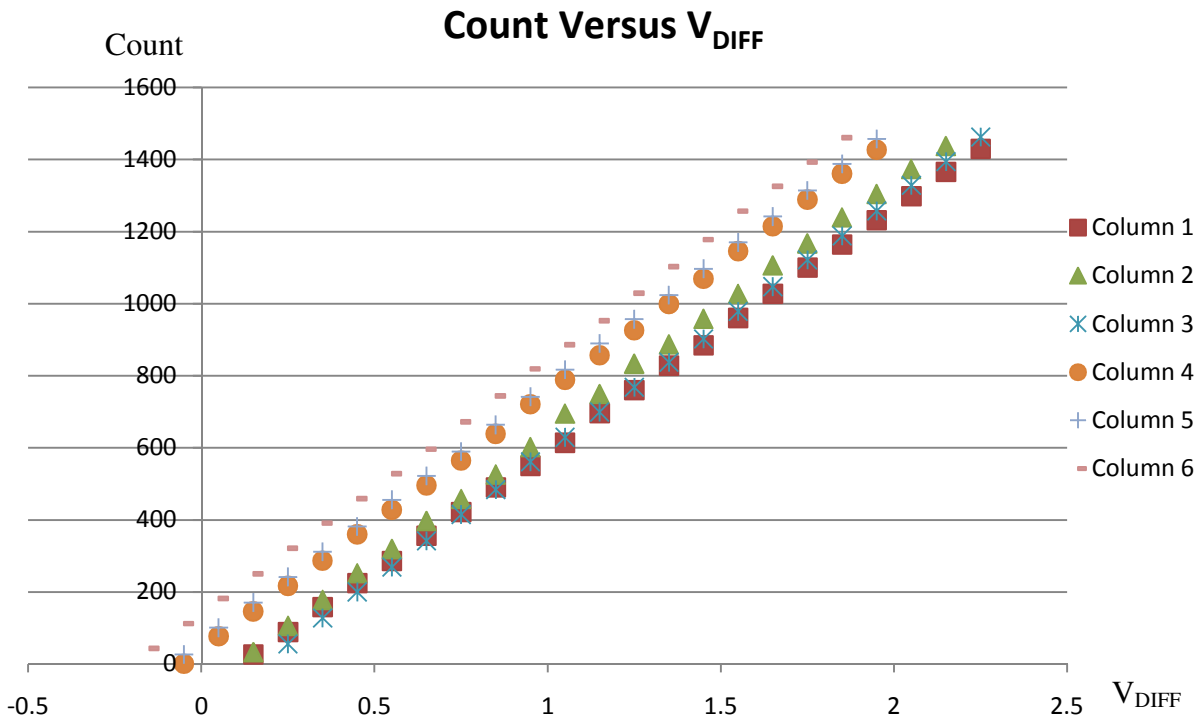

Figure 3.1.3 – Showing the error due to different offsets from 6 different outputs. Some offsets are as large as 150 mV. SL in Figure 2.1.1 is low in this case.

To illustrate how path switching averages out offset differences data was taken with the path switching signal, SL, low and high (Figure 3.1.3 is the SL low data). Figure 3.1.4 shows data points from SL high and SL low averaged together. It is evident that this greatly reduces the amount of difference between the outputs.

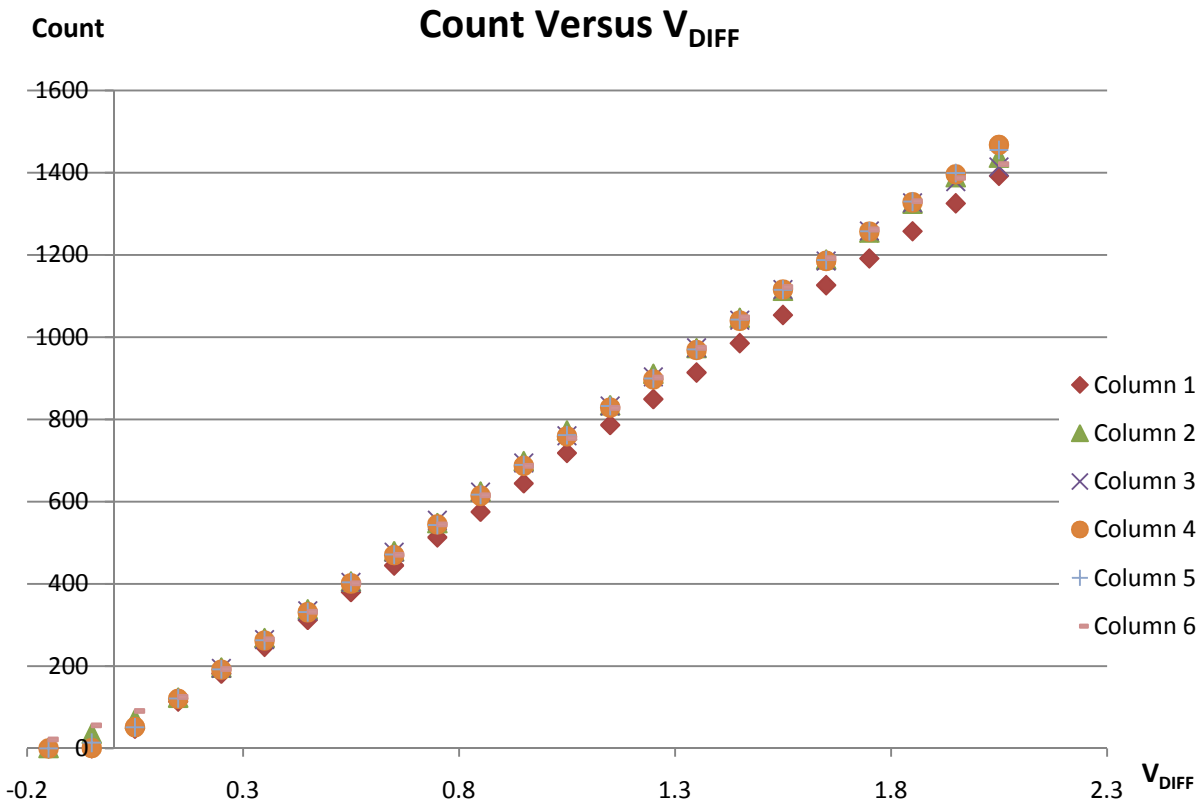

Figure 3.1.4 – Averaging the values from SL high and SL low to switch the paths causes most of the offset to cancel out.

There are a few things to address in Figure 3.1.4. The endpoints of the graph show non-linearity. This is because the count cannot be lower than zero or above the number of total possible counts (1500 in this case). To allow the endpoints to average correctly, one of the path outputs would have to go lower than zero or higher than 1500, which is not possible. Figure 3.1.5 also illustrates this point by taking a closer look at what occurs when the count should reach zero on the y-axis.

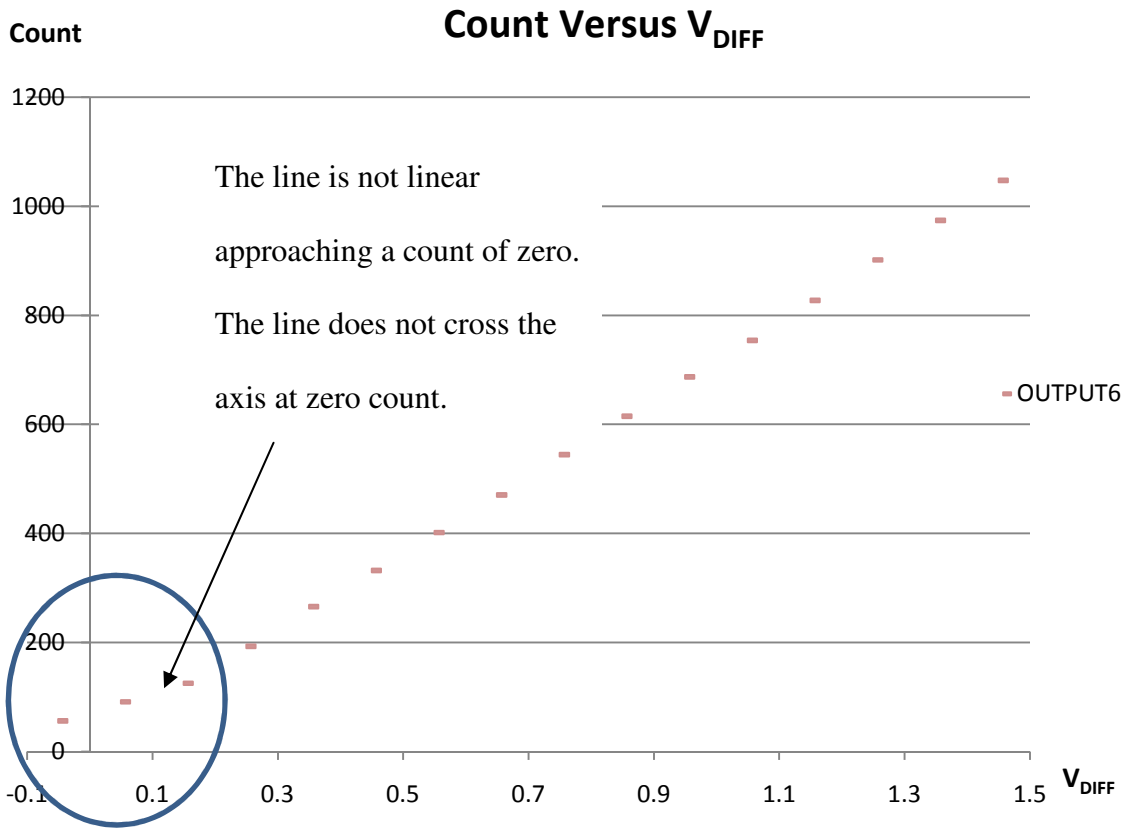

Figure 3.1.5 – Non-linearity is present when the count approaches zero. Device mismatch and path offset are the culprits. Non-linearity will occur for the width of the offset looking at the V_{DIFF} axis.

To remove non-linearity near the zero point, subtract the number of counts associated with the maximum allowable offset from the count. This just moves the zero point up to the linear range and would not have an adverse affect for a typical magnitude of offset in a production design. To remove non-linearity near the maximum count, increase the total count N while maintaining the same maximum count. For example, if targeting a maximum count of 2048 you could clock the circuit 2068 times but allow the

counter to max out at 2048. Twenty additional counts is an arbitrary pick for this example. The number of additional clock cycles can be calculated based on a typical offset.

Another thing shown clearly in Figure 3.1.4 is the fact that OUTPUT #1 has a different slope. This can be due to an offset in the difference path or a variation of capacitance on C_5. For the test chip, this is likely caused by an offset on the NMOS transistor in the difference path having V_{REF} applied to its gate since the design is using near minimum size devices. An offset in the difference path device is of concern because the path switching topology shown in Section 3.1 will not correct the issue. The table in Table 3.1.6 gives a better idea of the exact differences.

Table 3.1.6 – Output values nearing the maximum differential input. Note that output #1 likely has device variation in the reference path.

	Output #1	Output #2	Output #3	Output #4	Output #5	Output #6
Count @2.05V	1392	1437	1414	1467	1454	1420
Count @1.95V	1325	1389	1379	1396	1399	1387
Count @1.85V	1257	1325	1327	1328	1329	1330
Count @ 1.80V	1191	1255	1258	1257	1257	1261
Count @1.85V	1126	1189	1186	1185	1187	1192

As mentioned previously, the large deviation at the endpoints is due to offset or device mismatch where the count goes to maximum or zero for one of the paths. Figure 3.1.6 shows that the outputs are close together until you get to a differential voltage of 1.95V. Using different ADC's per column, output matching is critical to reduce column FPN in this design.

3.2 FPN from the Difference Path

Path switching has no effect on threshold voltage or capacitance variation in the difference path. The C_1 and C_2 capacitances affect the signal gain (amount of charge that is removed when Q is high) so the path switching method in Section 3.2 does not remove all the error from variation in these capacitances (If the capacitances average out to the ideal value then the path switching will remove the mismatch. Otherwise, it will result in some amount of column FPN). These differences will result in column FPN in the test chip design.

To address the mismatch in the difference path, a topology that would add six additional transistors per column ADC and require three non-overlapping clock cycles instead of two was developed. The idea is to remove the device mismatch by switching paths midway through the sense similar to the path switching added for the signal and reset paths. Two source follower paths are used; one sets a low voltage point, the other sets a high voltage point. The level of charge removed from C_4 (in the case of SL high) relates to the difference of these voltage levels. Reversing the roles of each source follower midway through the sense subtracts out mismatch.

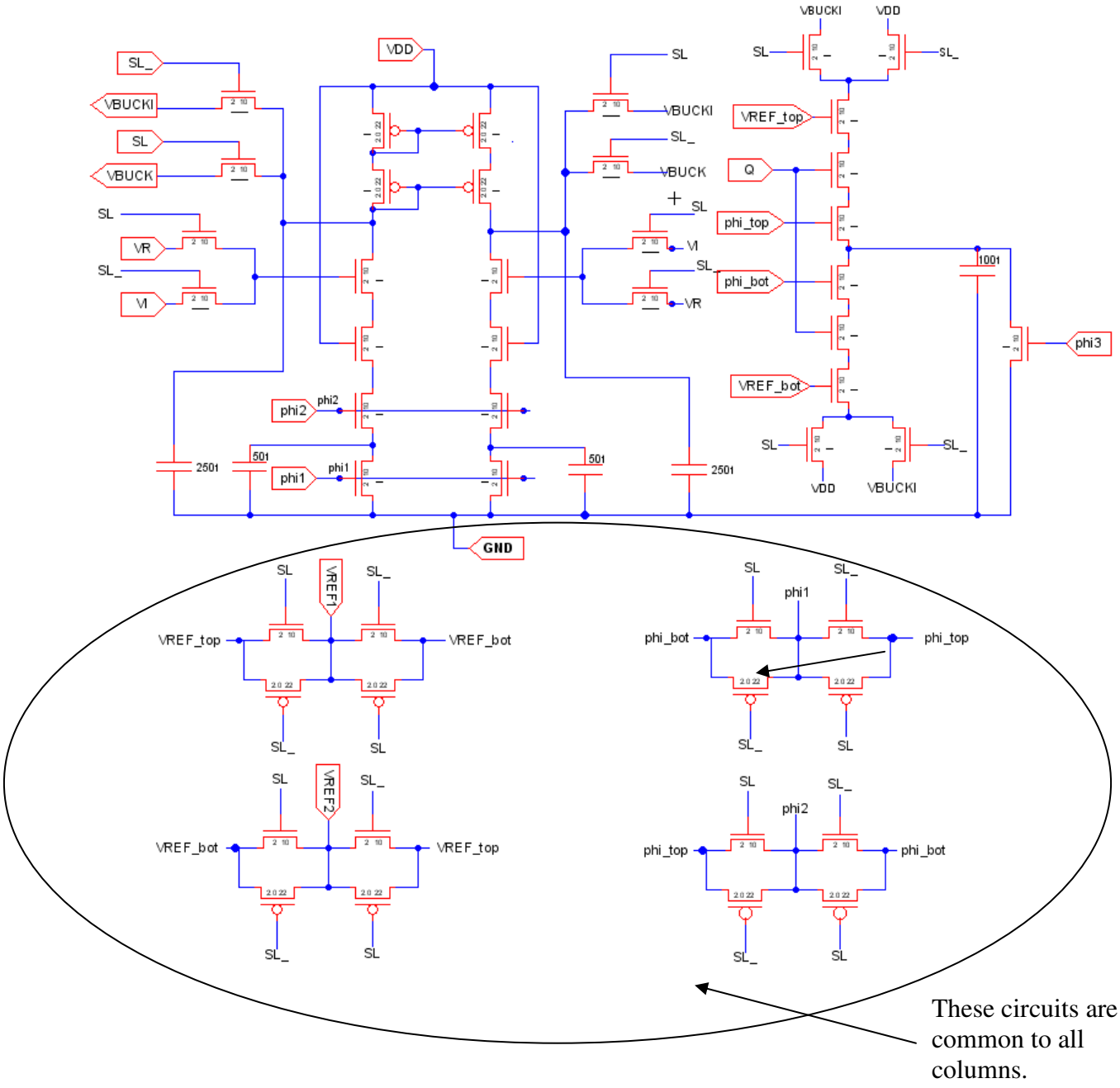

Figure 3.2.1 - DSM ADC without the comparator; including the circuitry to subtract out the device mismatch in the difference path.

In order to set the low voltage reference onto C_5 using one of the source followers, phi3 needs to turn on pulling off the charge from the previous cycle because

the voltage needs to be at a lower potential than the output of the source follower. This requires three non-overlapping clock phases. The disadvantage to requiring three clock phases is that each phase now has less time to transfer charge. Increasing the width of phi2 compared to phi1 and phi3, since it needs to charge to a larger potential, will help. The width of phi3 is not critical since capacitor C_5 is connected to ground directly through a pass transistor when phi3 is high. The phi3 pulse width could be considerably shorter.

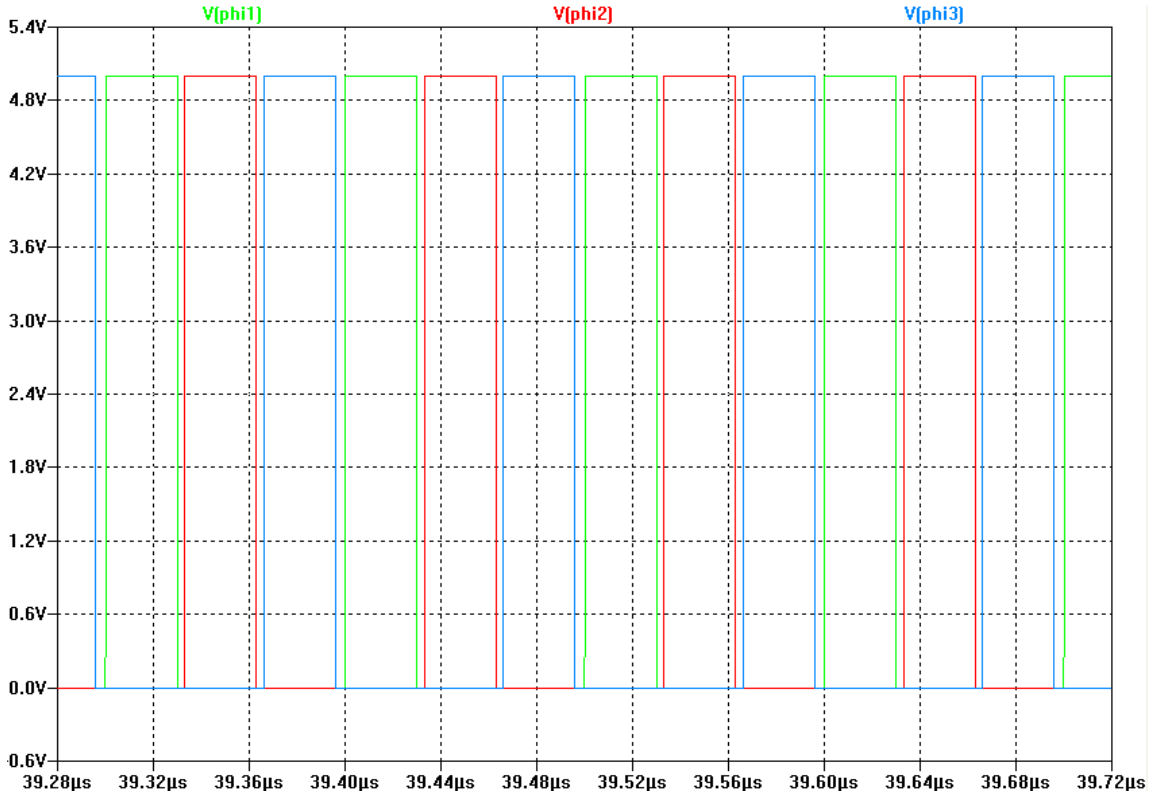

Figure 3.2.2 – Three non-overlapping clocks used in the simulation of Figure 3.2.1.

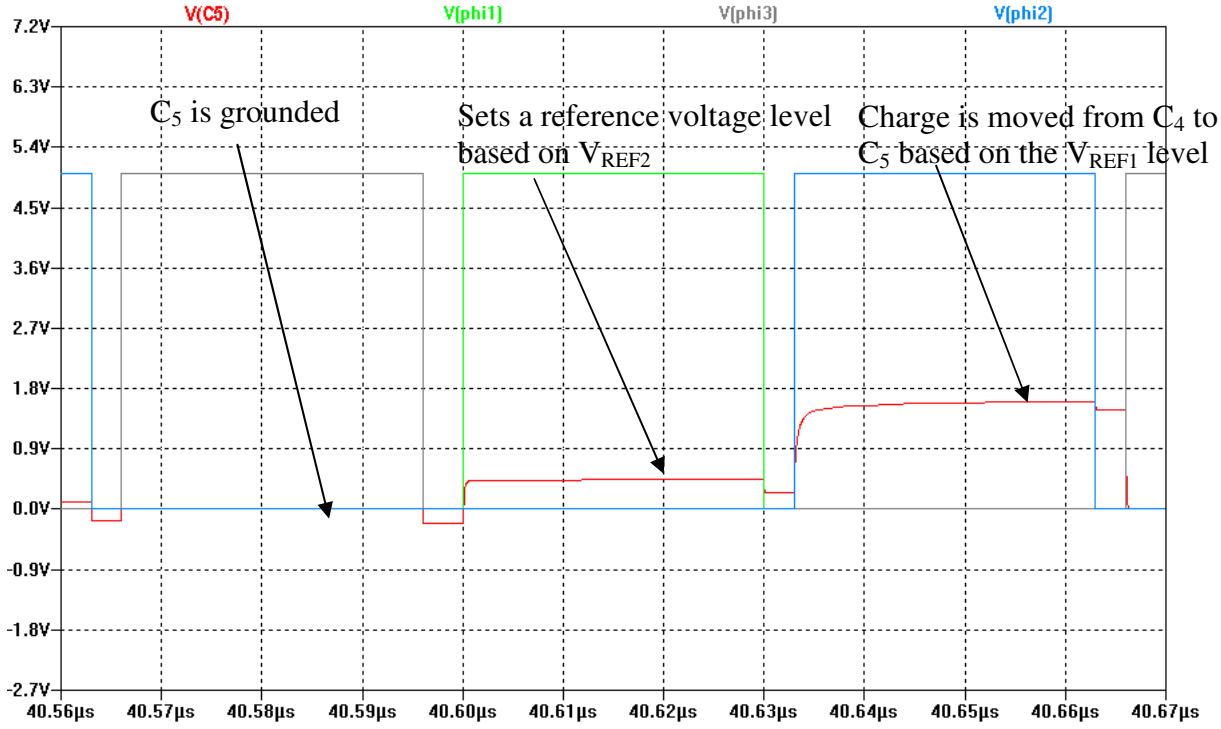

Figure 3.2.3 – When phi3 is high, C_5 is pulled to ground. Clock phase phi1 going high sets a reference voltage on C_5 based on V_{REF2}. Clock phase phi2 going high removes charge from the C_4 capacitor onto C_5, which charges to a voltage level based on V_{REF1}.

To show the removal of device mismatch, the charge transfer during one cycle with SL high and one cycle with SL low are examined. Q is high for both cases. The charge removed from C_4 relates to the final voltage on C_5 compared to the reference voltage. Equation 3-1 shows the charge removed when SL is high.

$$Q(\text{SL High}) = C_5 \cdot \left(\left(V_{REF1} - V_{THN1} \right) - \left(V_{REF2} - V_{THN2} \right) \right) \tag{3-2}$$

With SL low the amount of charge removed is shown in equation 3-2.

$$Q(\text{SL Low}) = C_5 \cdot \left(\left(V_{REF1} - V_{THN2} \right) - \left(V_{REF2} - V_{THN1} \right) \right) \tag{3-3}$$

Adding together the charge transferred during each cycle results in the cancellation of the threshold voltages. In this example, if there was mismatch due to variation in threshold voltage, it is removed.

$$Q(\text{SL High}) + Q(\text{SL Low}) = 2 \cdot C_5 \cdot \left(V_{REF1} - V_{REF2}\right) \tag{3-4}$$

This idea will not remove all the affects of the threshold or offset difference. Since there is a difference in the charge removed with each cycle the difference path is enabled, the counts will be different for the first and second half of the sense. Therefore, you will not have an equal number of charge transfers for a complete cancellation. However, this still has a very large impact on the amount of error due to threshold mismatch. The error in the difference path is greater when approaching higher counts because it relates to the slope of the line. This is a good thing because it is easier to see variation in a dark portion of an image. Equation 3-4 shows the solution for the count when implementing the circuit in Figure 3.2.1.

$$M = \frac{\left(V_R - V_I\right)\left(V_{REF1} - V_{REF2}\right)}{\left(V_{REF1}^2 + V_{REF2}^2 - 2 \cdot V_{REF1} \cdot V_{REF2} - OFFSET^2\right)} \cdot \frac{C_{1,2}}{C_5} \cdot N \tag{3-5}$$

If there is no offset the solution of Equation 3-4 reduces to the following:

$$M = \frac{\left(V_R - V_I\right)}{\left(V_{REF1} - V_{REF2}\right)} \cdot \frac{C_{1,2}}{C_5} \cdot N \tag{3-6}$$

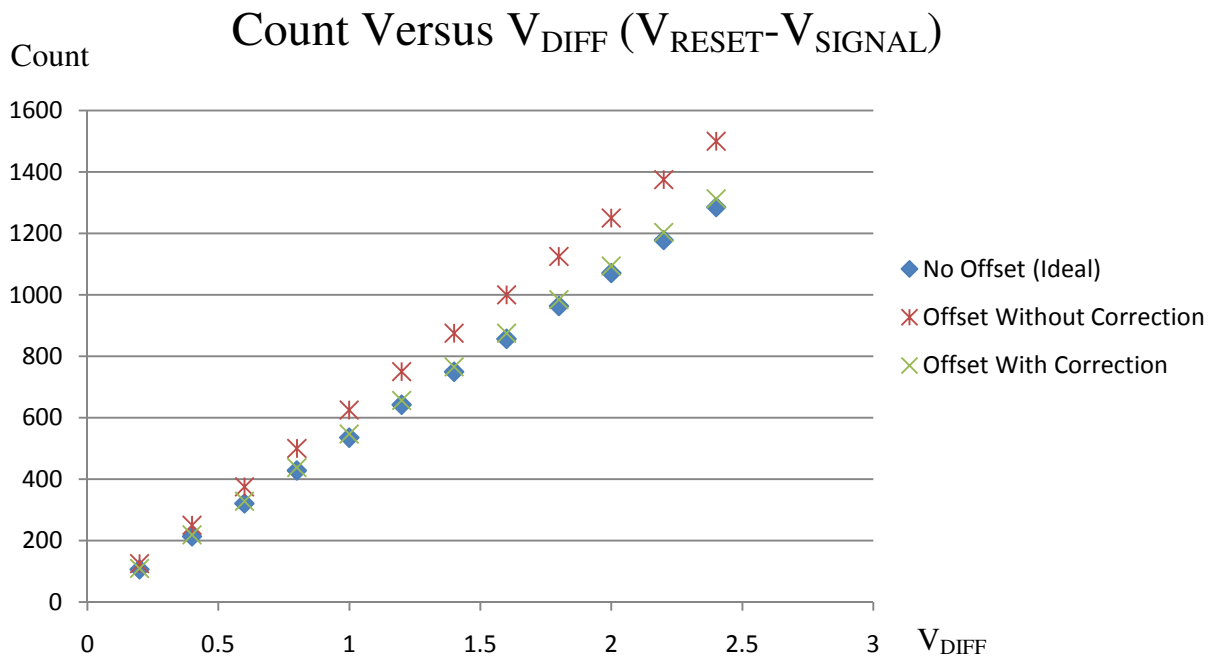

Figure 3.2.4 – Calculated values for showing improvement from differential offset correction (200 mV offset).

V_{REF2} needs to be greater than the maximum expected offset voltage plus the threshold. Additional margin, added to avoid non-linearity issues when operating just above the threshold, will result in more immunity to mismatch. Making V_{REF2} larger requires a larger capacitance to remove the same amount of charge. Simulations ran, with V_{REF1} at 2.5, V_{REF2} at 1.1, and an offset at 200 mV, produced excellent results.

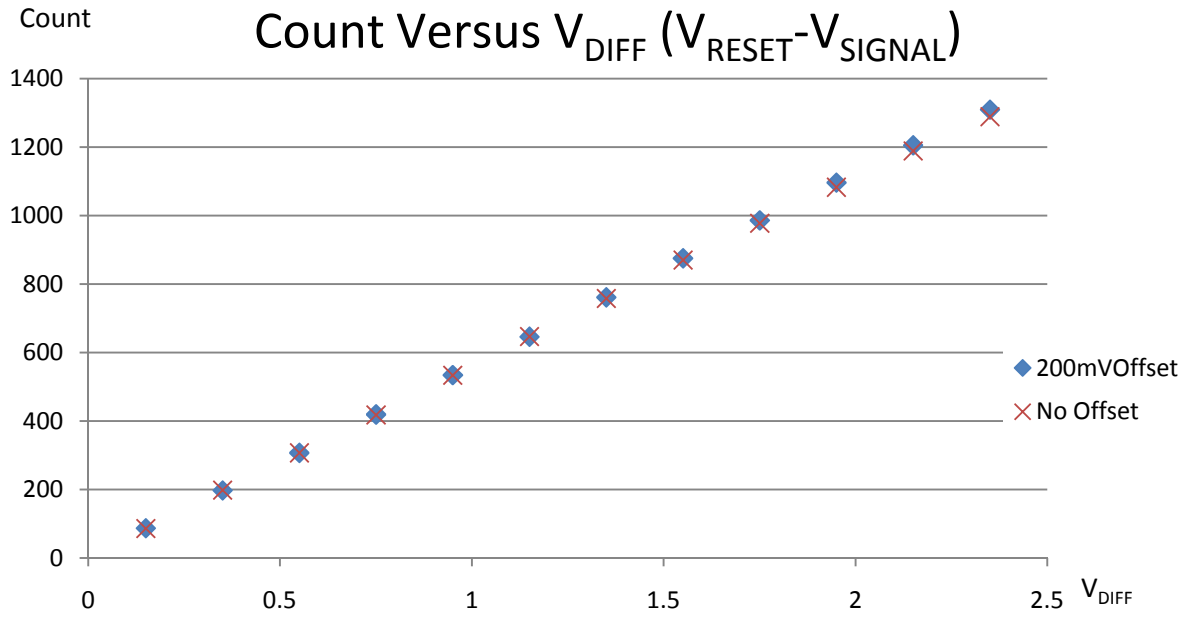

Figure 3.2.5 – Simulation data showing the results from applying a 200 mV offset to the differential path.

3.3 Thermal Noise

Thermal noise is a very good topic for DSM's. Because of averaging, the capacitors used in this topology have a lower RMS voltage for a given capacitance.

$$V_{ONOISE,RMS} = \sqrt{\frac{kT}{NC}} \tag{3-7}$$

Because of the decrease in thermal noise, smaller capacitors can be used for the DSM circuit allowing for a smaller footprint. The reset and signal capacitors still need to be comparable to that used with the pipeline ADC topology. To measure the immunity of the DSM ADC to thermal noise, a source was added to V_{SIGNAL} with a magnitude as large

as 1V peak to peak. V_{SIGNAL} and V_{RESET} voltages are directly ran from the test chip output pins to the input gates on the ADC.

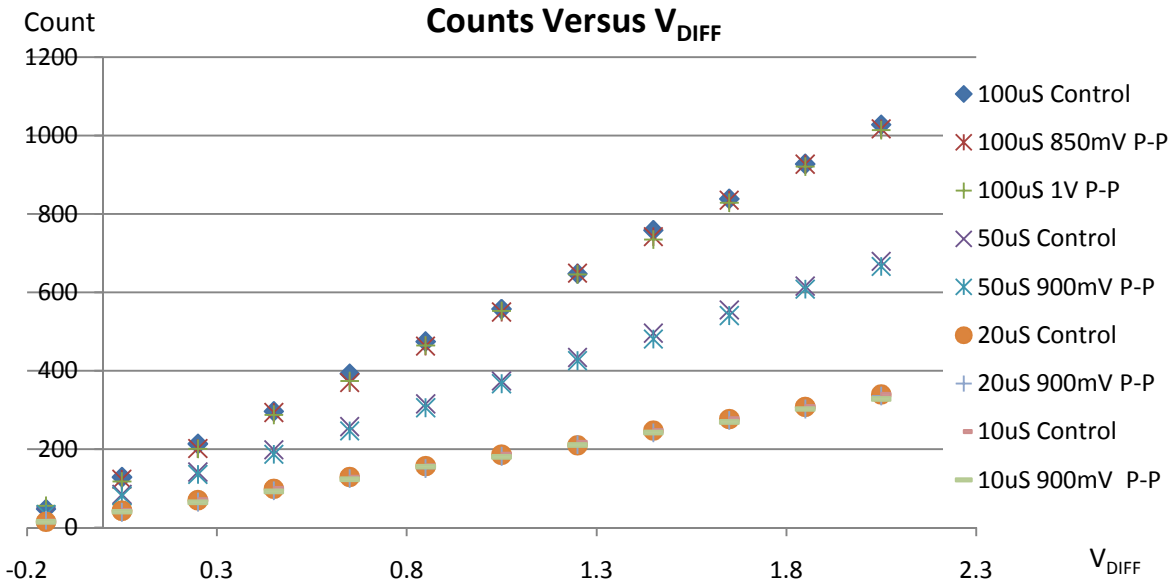

Figure 3.3.1 – Noise applied to V_{SIGNAL} versus control groups on our test chip.

In Figure 3.3.1, the data points with large amplitudes of white noise line up very well with the control groups. The variation in some of the data points looks to be the result of the noise signal having an average lower signal.

CHAPTER 4 – DSM VERSUS PIPELINE ADC'S FOR CMOS IMAGERS

4.1 Noise

As explained in Chapter 1, V_{RESET} and V_{SIGNAL} voltages sampled onto capacitors provide a differential input. This is a measure of how much light was incident on the photo diode during a fixed integration time. Thermal noise will affect the final voltage that gets stored on the capacitor based on the equation kT/C for both topologies. For a pipeline ADC, this will be followed by gain stages in order to increase the dynamic range of the ADC based on the range of the APS pixel output. These gain stages can introduce column FPN.

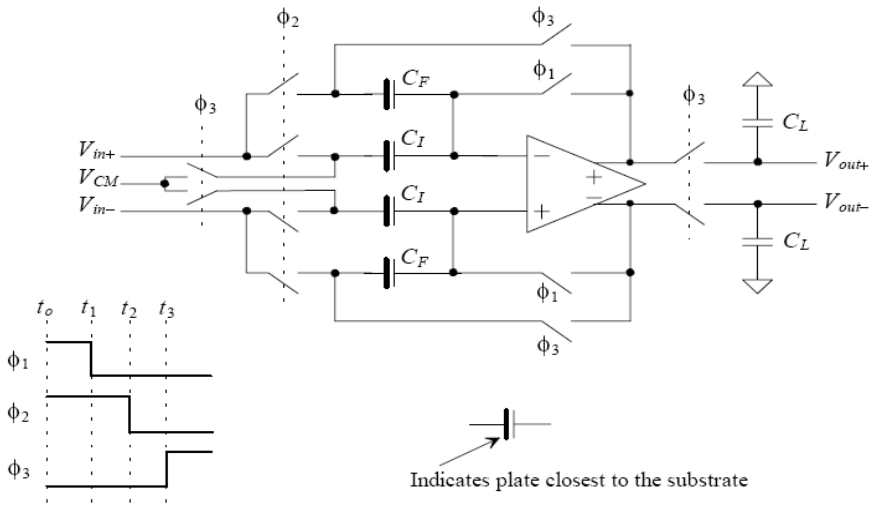

Figure 4.1.1 – Example of a topology used for a gain stage. (Taken from [4], p.343, Figure 34.20).

The column FPN is a result of differences in capacitance values or related to the metal line busing, which connects the capacitors to the amplifier. The metal line busing even becomes a larger problem as the size of the array increases. Adding additional pipeline ADC's by region can address this issue. However, this allows for variation issues between regions, especially when multiple ADC's share the same color plane.

In Figure 4.1.1, the C_I capacitors (labeled C_{RESET} and C_{SIGNAL} in Figure 1.2.1) are used to store V_{RESET} and V_{SIGNAL} voltages at the bottom or top of each column of the pixel array for a pipeline ADC. These signals are bused to the inputs of the shared gain stage amplifier. All columns share the feedback capacitors C_F. For this topology, the gain relates to the capacitance ratio of the reset and signal capacitors to the feedback capacitance. Charge sharing occurs when the phi2 signal goes high to produce the differential output (V_{OUT+} and V_{OUT-}).

$$V_{OUT} = V_{OUT+} - V_{OUT-} = \left(1 + \frac{C_I}{C_F}\right) \cdot \left(V_{RESET} - V_{SIGNAL}\right) \tag{4-1}$$

Looking at the last equation and knowing the C_I capacitors are unique to each column, it is evident that column variation occurs if the capacitance values vary or there are differences due to busing.

The DSM ADC does not suffer from reasonable differences in the reset and signal capacitances. The reset and signal capacitors are used to hold a voltage on a high impedance gate. There is no charge sharing to worry about. The DSM ADC's are local to each column, eliminating problems with busing analog signals. Variation in the

difference path capacitor or with C_1 and C_2 in Figure 2.1.1 will cause column FPN as shown in Section 3.2.

The main advantage of the pipeline ADC is that after the sample and reset capacitors and metal busing, all columns share the remaining gain and ADC stages (although multiple ADC's could be used for groups of columns creating variation from ADC to ADC which becomes a bigger issue if they share the same color plane). Any offset or mismatch in the rest of the circuitry is common to all columns. Dark row readout allows feedback to remove offsets common to all columns in the analog chain.

Another difference between the topologies is that the thermal noise associated with the reset and signal capacitances, and the many other capacitors used in the pipeline ADC relates to kT/C. As shown in Section 4.2, the thermal noise in the DSM ADC also relates to the number of clocks cycles during the sense, kT/NC (the final voltage on reset and signal relate to kT/C for both topologies but the error during sensing of the final voltage for the DSM ADC is kT/NC). The DSM ADC is a much simpler design with a fewer number of capacitors where thermal noise can be added to the output.

4.2 Layout

The DSM ADC is very competitive with the pipeline ADC regarding layout size. The analog circuits in the pipeline ADC take up a lot of space. This can consist of multiple gain stages to increase the ADC dynamic range, a pipeline ADC requiring an amplifier and comparator along with other circuitry for each bit of resolution, circuitry

for reference voltages and biasing, a DAC used to apply an analog feedback voltage to cancel out common offsets, etc.

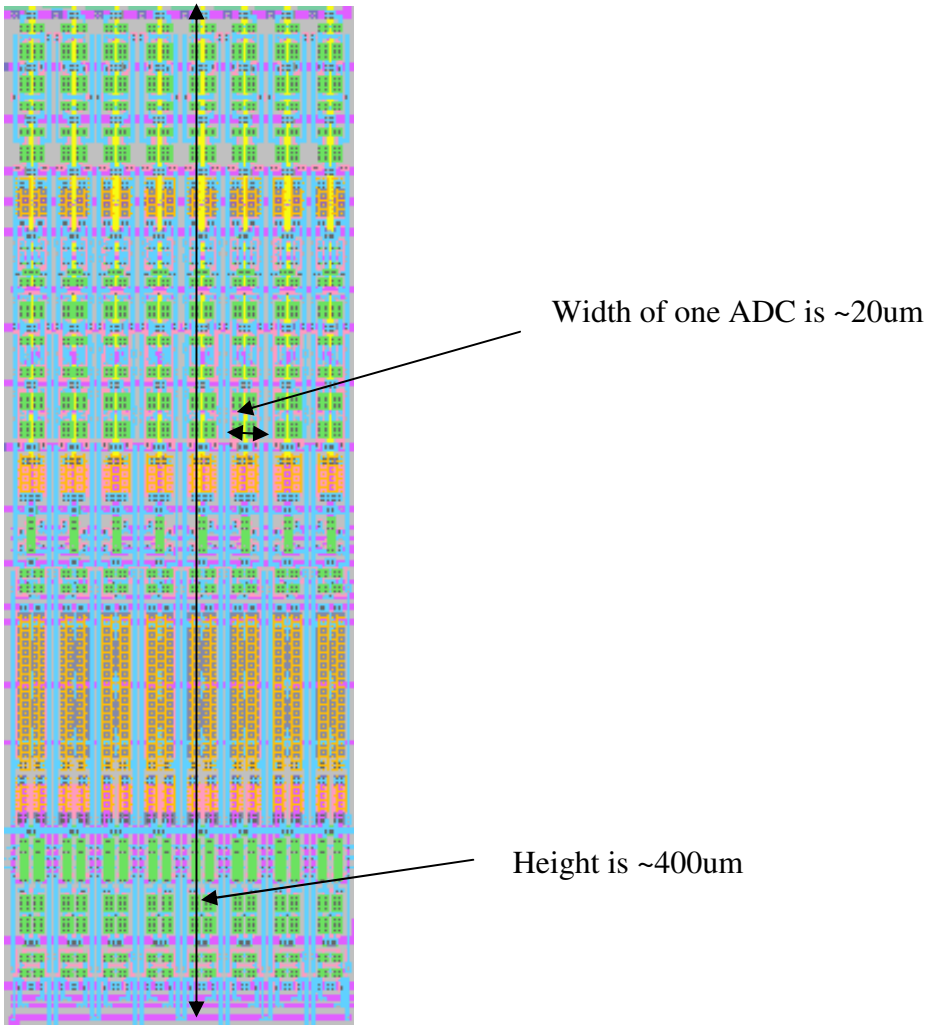

Figure 4.2.1 – 8 DSM ADC circuits side by side for the test chip on the AMI 500nm process. *Electric* was used for the layout.

For a DSM design with a 1600w x 1200h pixel array, using the AMI 500 nm process, with an estimate pixel size of 18 um x 18 um, the array would require an area of

28.8 mm x 21.6 mm. The DSM's would require an area of 28.8 mm x 400 um**.** Each column requires a counter used as a low pass filter. A TSCP counter designed for this research was not included in the layout. Calculating the counter layout area, based on the number of transistors and other reasonable considerations, gave a dimension of 1.36 um x 28.8 mm. Other circuits, including a shared clock generator, a DAC with a register to supply V_{REF} for each color, and a control signal to switch paths midway through the sense, would be required but take up a very small amount of space.

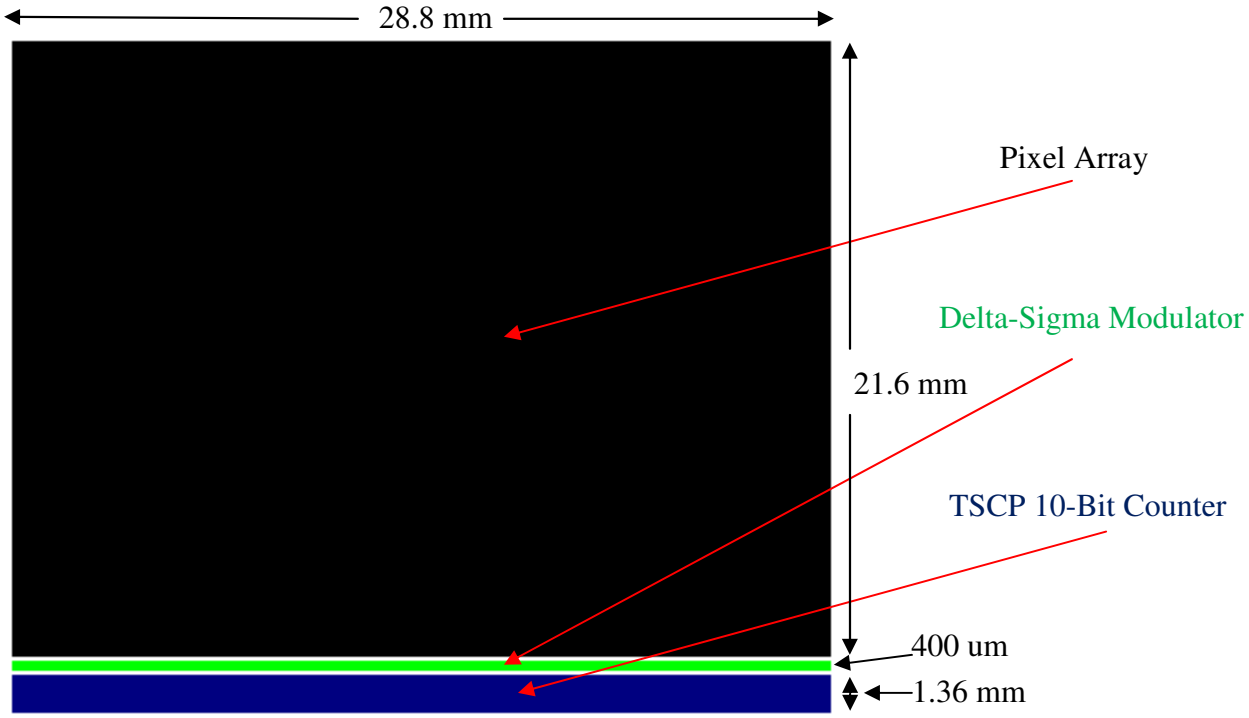

Figure 4.2.2 – Diagram showing layout scale for an image sensor using delta-sigma modulation for sensing using the AMI 500 nm process.

The test chip used minimum device sizes, allowing a good look at how offsets really affect the design. For a production design, using larger devices would minimize

offset and allow for faster frequencies. This would result in a little larger layout but the amount of silicon consumed would still be very reasonable.

4.3 Power Consumption

CMOS Image sensors are used in a variety of applications where low power is a big concern. This is a big advantage of using CMOS over CCD sensors. There is also an advantage in using DSM ADC's compared to pipeline ADC's. Pipeline ADC's are relatively high power circuits. With the DSM ADC topology, you will consume less power. Based on simulations on the test chip, the current average is around 20 uA per ADC. If a CMOS Imager was built using the AMI 500 nm process, 1000 ADC's would consume around 20 mA of current, which is very low for the process (A counter for each column would also need to be built and used as a low pass filter but the benefit would still be large). The test chip supplied current is under 3 mA for all circuits (the VDD supply is common to all circuits).

4.4 Other

The circuits presented in this research are very simple and will scale between processes. Another advantage of the DSM ADC is speed. The pipeline ADC designs get challenging with increasing frequency. The frequency limitations on the DSM ADC are based on the RC time constants associated with the switch mode capacitors. Larger devices and/or smaller capacitors will allow greater frequencies. With minimum device sizes, the test chip was able to function properly at frequencies as high as 50MHz. Faster frequencies will be easy to achieve using this design.

CHAPTER 5 – TEST CHIP DESIGN, LAYOUT, AND TESTING

5.1 General Test Chip Information

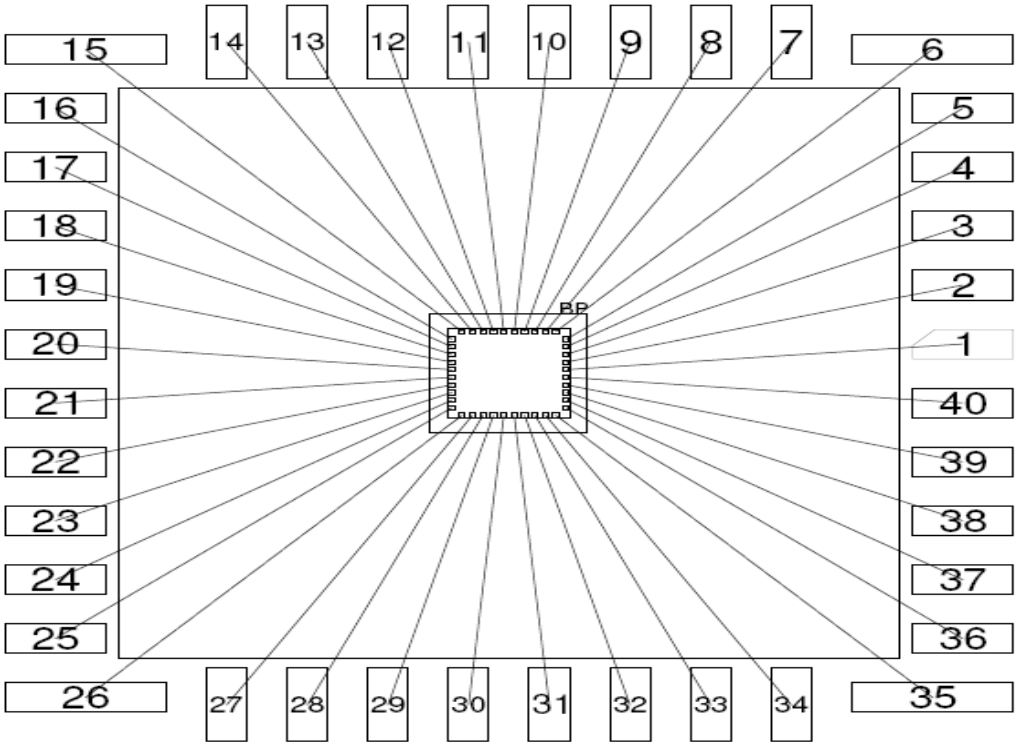

Figure 5.1.1 – Bonding diagram for test chip provided by MOSIS.

Table 5.1.2 – Pin descriptions

Pin Number	Pin Type	Pin Description
3,13,16,35,40	Supply	VDD Supply. These pins are tied together on chip.
1,6,8,9,25,37	Supply	Ground. Ground signals are tied together on chip.
5,27-34	Input	ADC signal inputs. There is a separate signal input for each DSM ADC.
4,26	Input	Reset Inputs. There is a single reset input for the 8 DSM ADC's as well as the single DSM ADC.
39	Input	Positive input to comparator
40	Input	Negative input to comparator
7,12	Input	$V_{REFERENCE}$ input. There is a single V_{REF} input for the 8 DSM ADC's as well as the single DSM ADC.
10,14	Input	Path select. There is a single select input for the 8 DSM ADC's as well as the single DSM ADC.
2,17-24	Output	These are the outputs for the DSM ADC's. There is a single output per DSM. The output is referred to as Q in this thesis.
36	Output	This is the output for the comparator.
11, 15	CLK	A separate clock is used for the 8 DSM ADC's. The other is used for the single ADC and the stand alone comparator.

5.2 Layout

The test chip consists of 9 DSM ADC's; one of which is separated from the rest with a clock generator that it shares with a comparator. The comparator, which is used in the DSM ADC design, was also included in the lay out for direct testing.

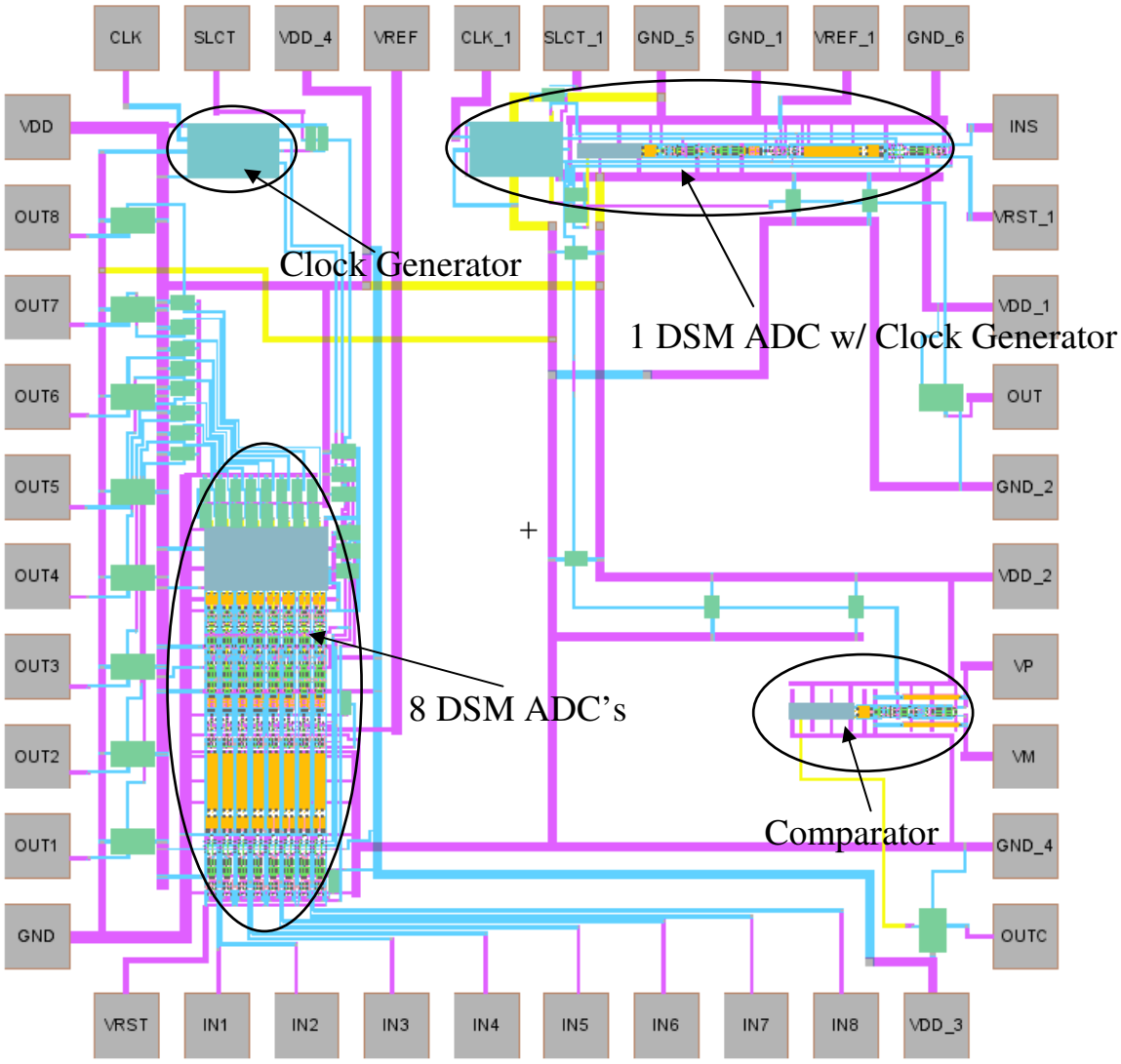

Figure 5.2.1 – Test chip full layout.

The digital and analog supply voltages are tied together for a single voltage supply. These voltages are separate in a production imager design. Separating them on the test chip would have had very little effect on the results.

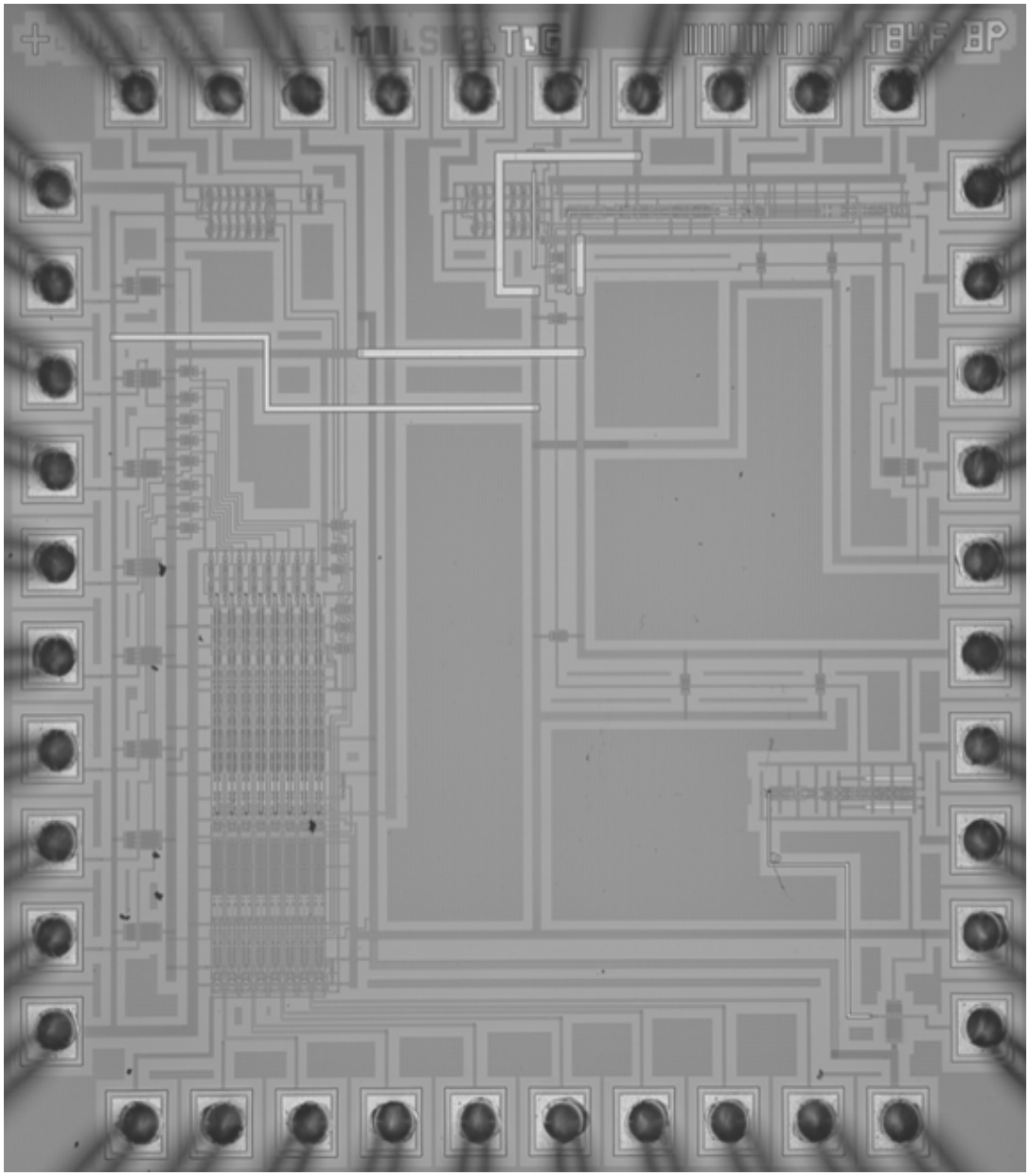

Figure 5.2.2 – Microscope image of test chip.

For matching consideration, the common centroid method was used. Matching is very important for this design to reduce column FPN. Special consideration needs to be

applied to the difference path because it is the area that will be most susceptible to causing column FPN.

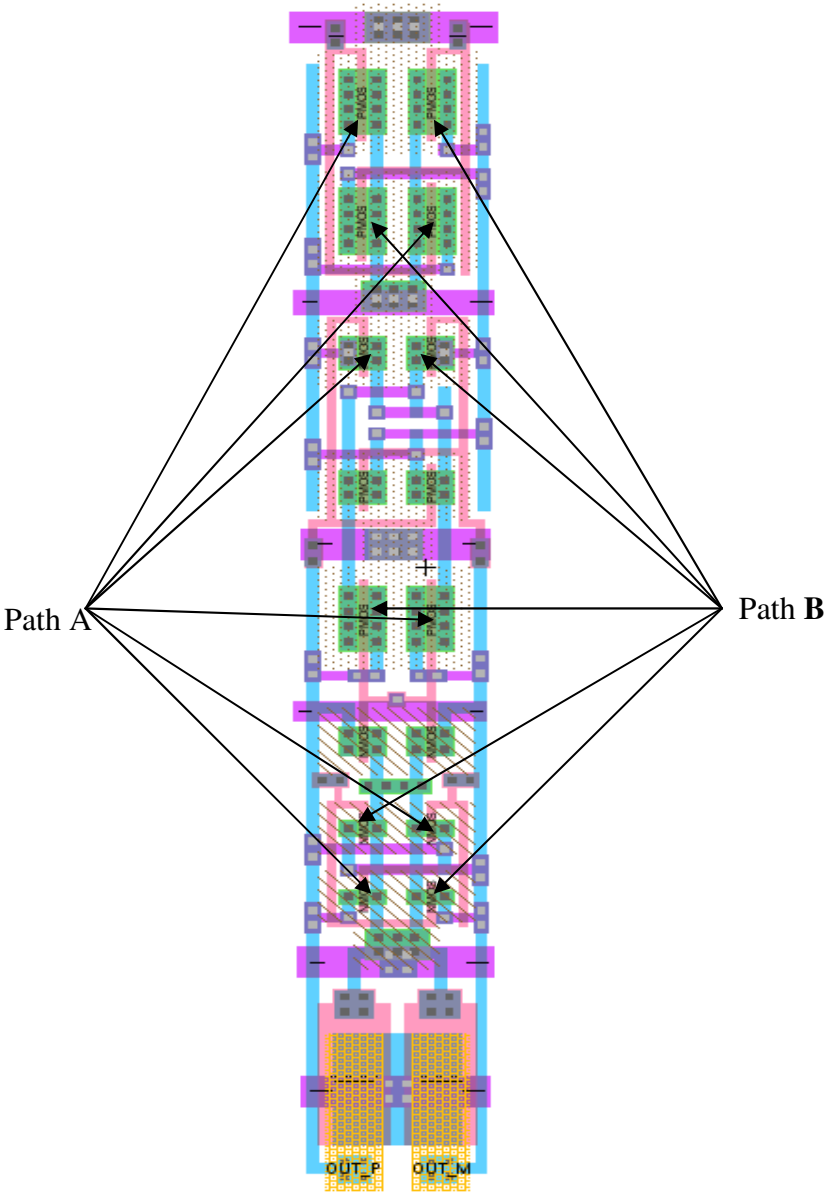

Figure 5.2.3 – Comparator layout as an example of using the common centroid method.

5.3 Testing

Separate HP E3631AC power supplies were used for the supply and input voltages. An Agilent waveform generator supplied the clock pulse. Outputs connected to an oscilloscope allowed the waveform capture. Voltage versus time data, captured on the oscilloscope, was sent to a Perl program written to count the number of pulses. Data was obtained for different frequencies, VREF values, etc. over a range of differential inputs.

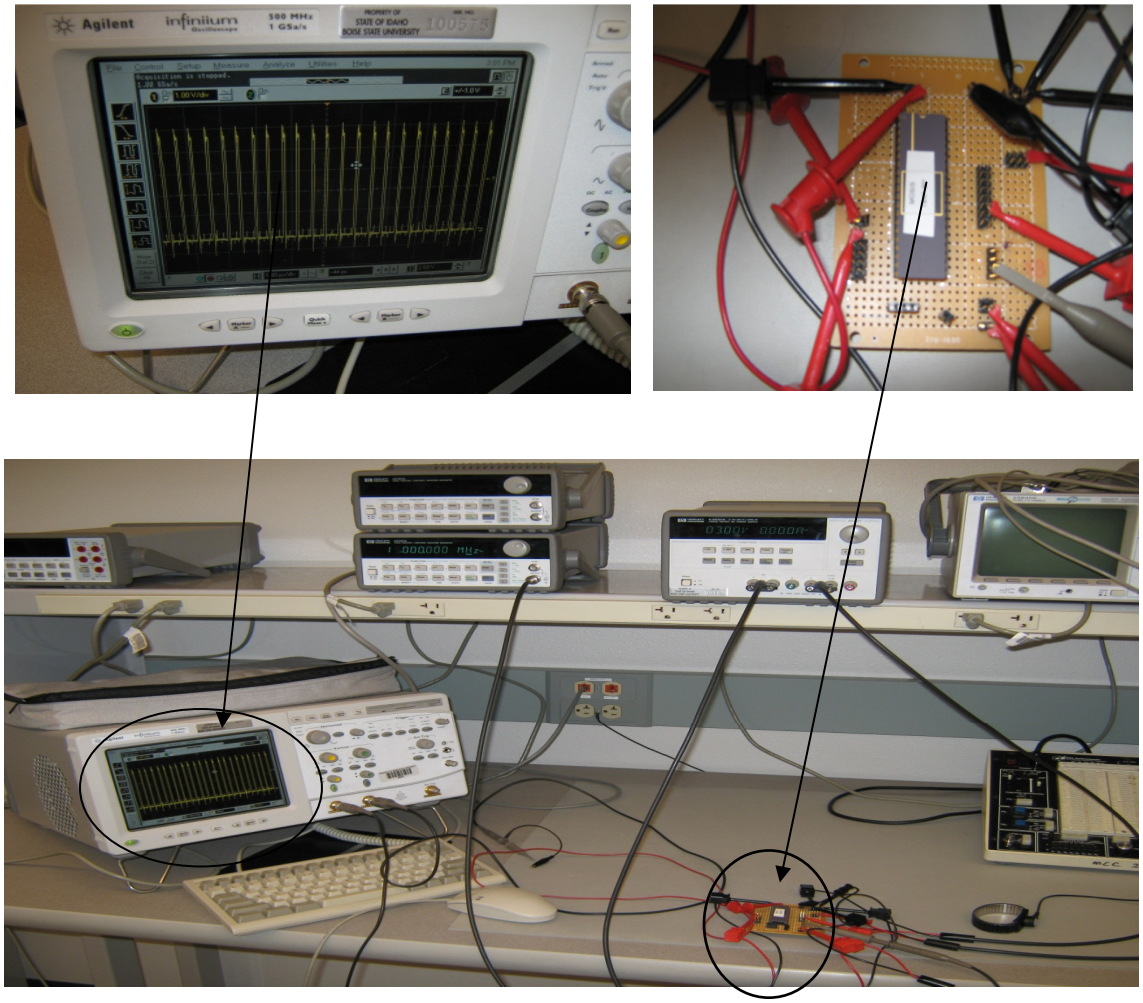

Figure 5.3.1 – Test setup used to collect test chip data.

CHAPTER 6 – CONCLUSION AND FUTURE WORK

6.1 Conclusion

This work involved the design and testing of a DSM circuit for analog-to-digital conversion and gain in a CMOS Imager. It was shown that this design has many benefits over the tradition Pipeline ADC topology. Noise, power, layout size, and speed were among the features compared.

To address noise issues due to device mismatch in the reset and signal path devices, path switching was added to the circuit. Minimum device sizes were used in the design, which were ideal to show how device mismatch can be removed. These devices were also ideal for showing other design limitations. A topology was introduced to remove device mismatch in the difference path. This topology was thought of after the test chip design and was only simulated. The DSM ADC design presented in this thesis has been shown to be very tolerant and would work well in a production design.

6.2 Future Work

Future work could include implementing the suggested topology to remove mismatch in the difference path on a test chip. Larger devices could also be used to minimize offsets and show how robust this design is. The devices could also be optimized for faster frequencies to show the effectiveness of this design in high speed applications.

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APPENDIX A

Key Design Schematics

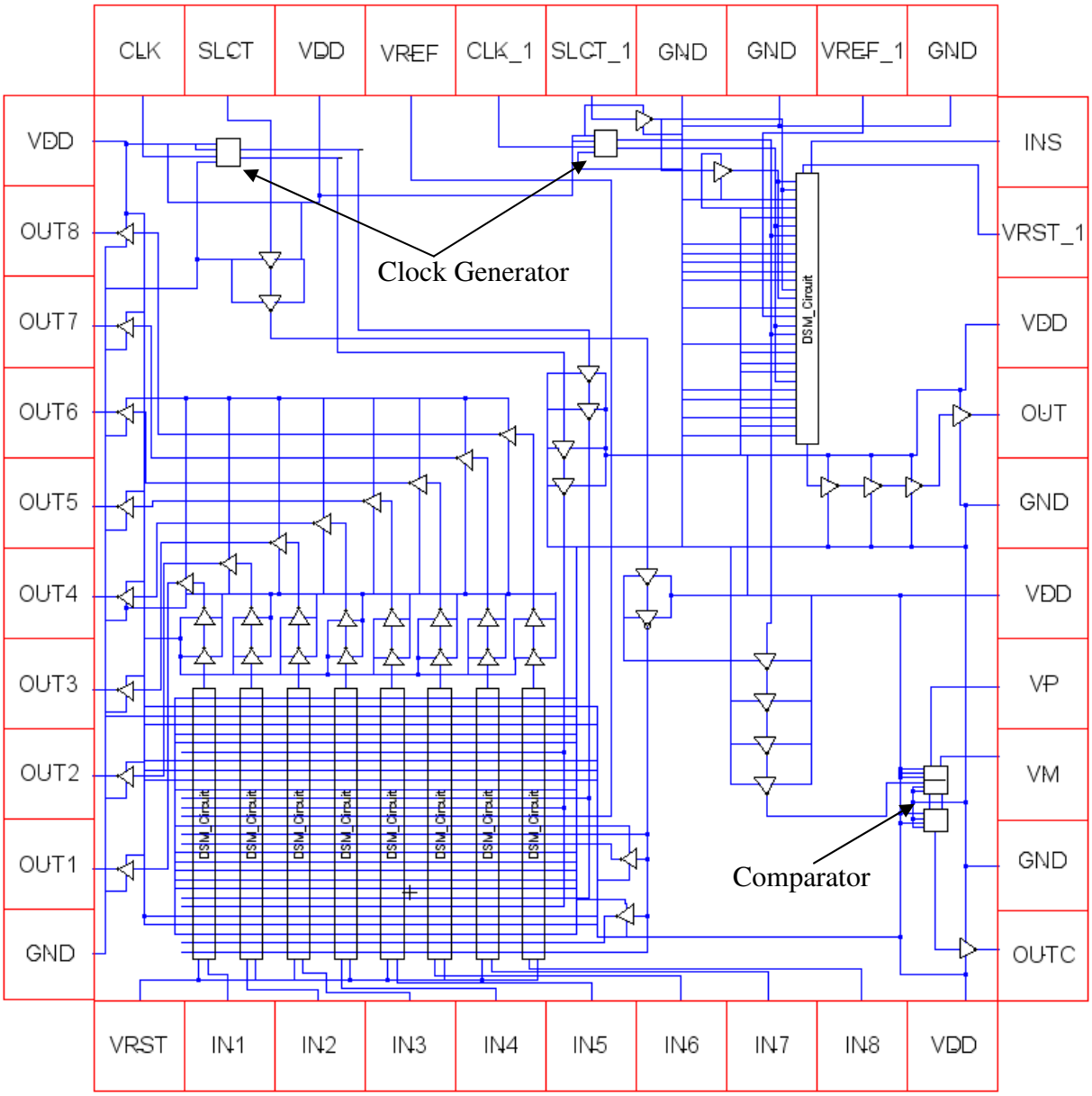

Figure A.1 – Schematic of test chip

Figure A.2 – Full DSM circuit (DSM_Circuit)

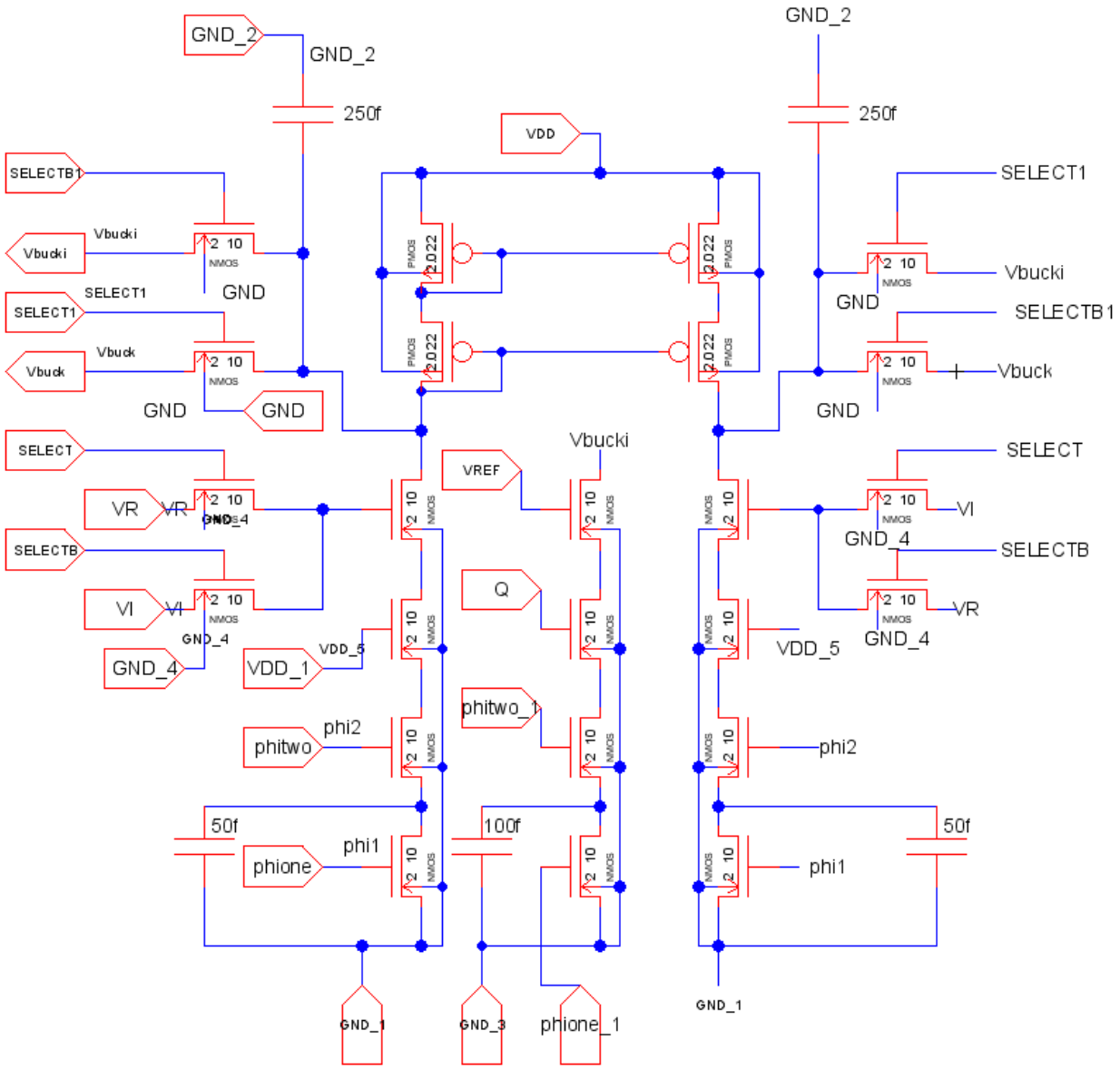

Figure A.3 – Test chip DSM circuit without the comparator and output (DSM_ADC_W_OFF)

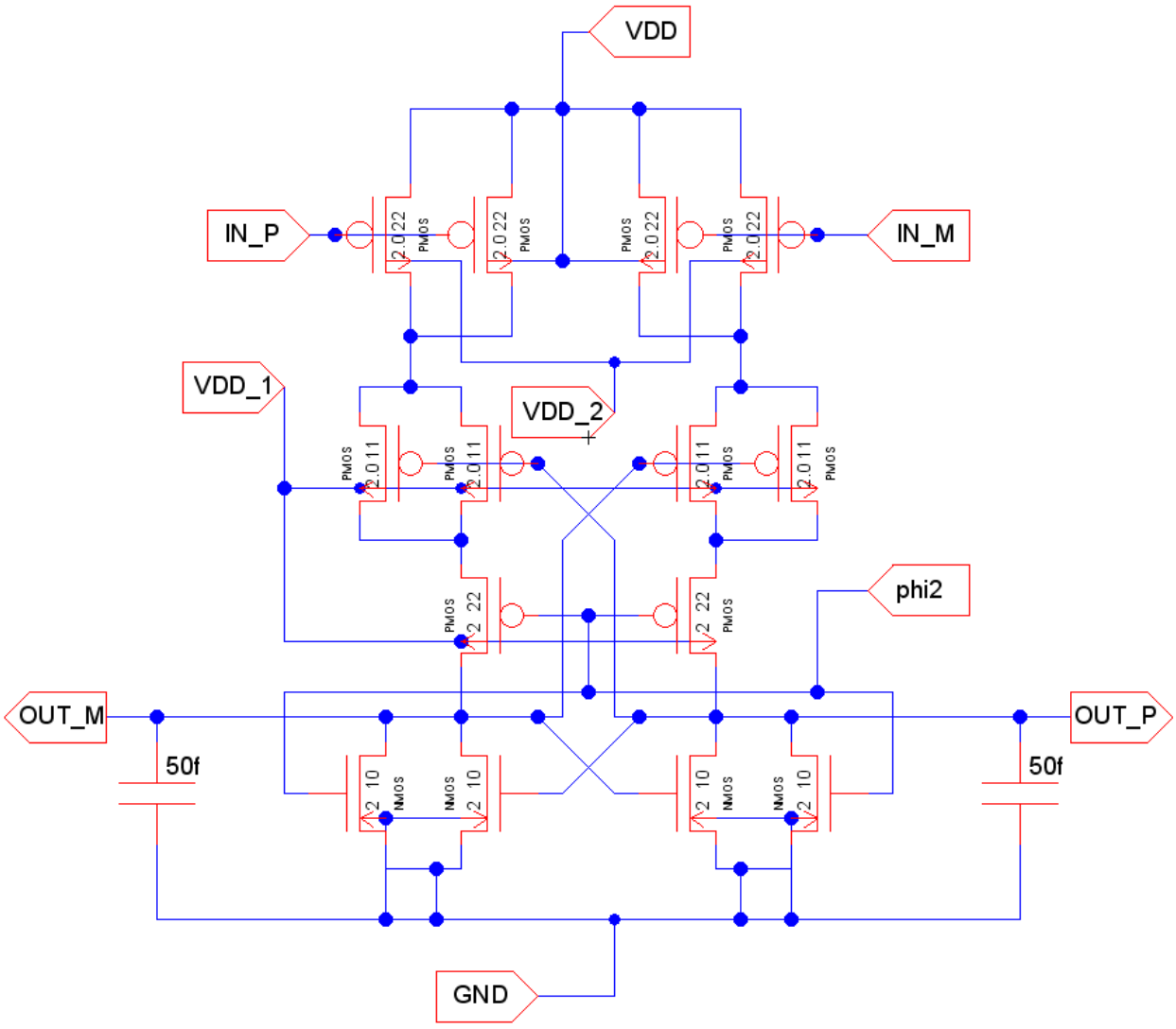

Figure A.4 – Comparator

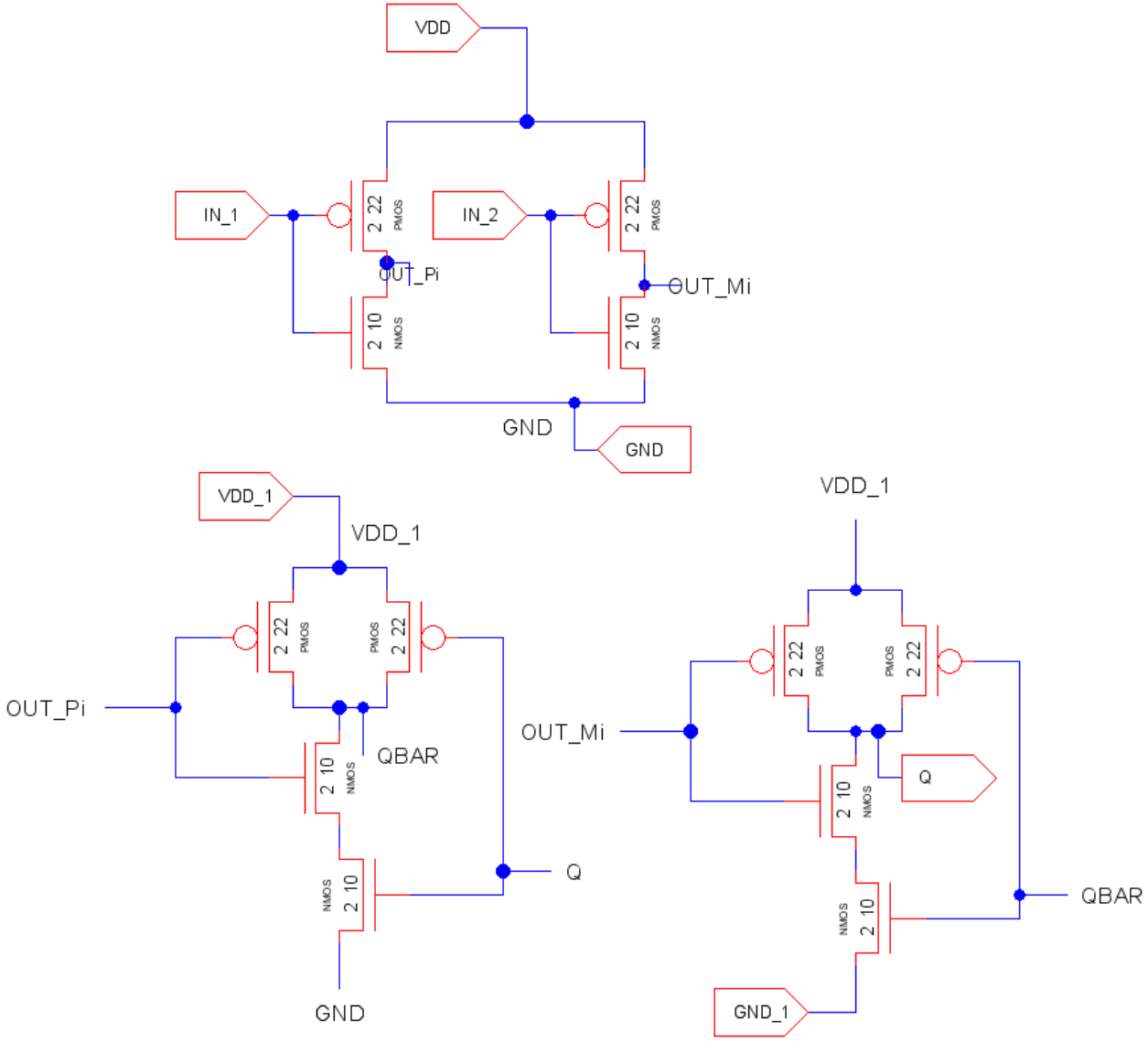

Figure A.5 – Digital output (digital circuit for comparator output)

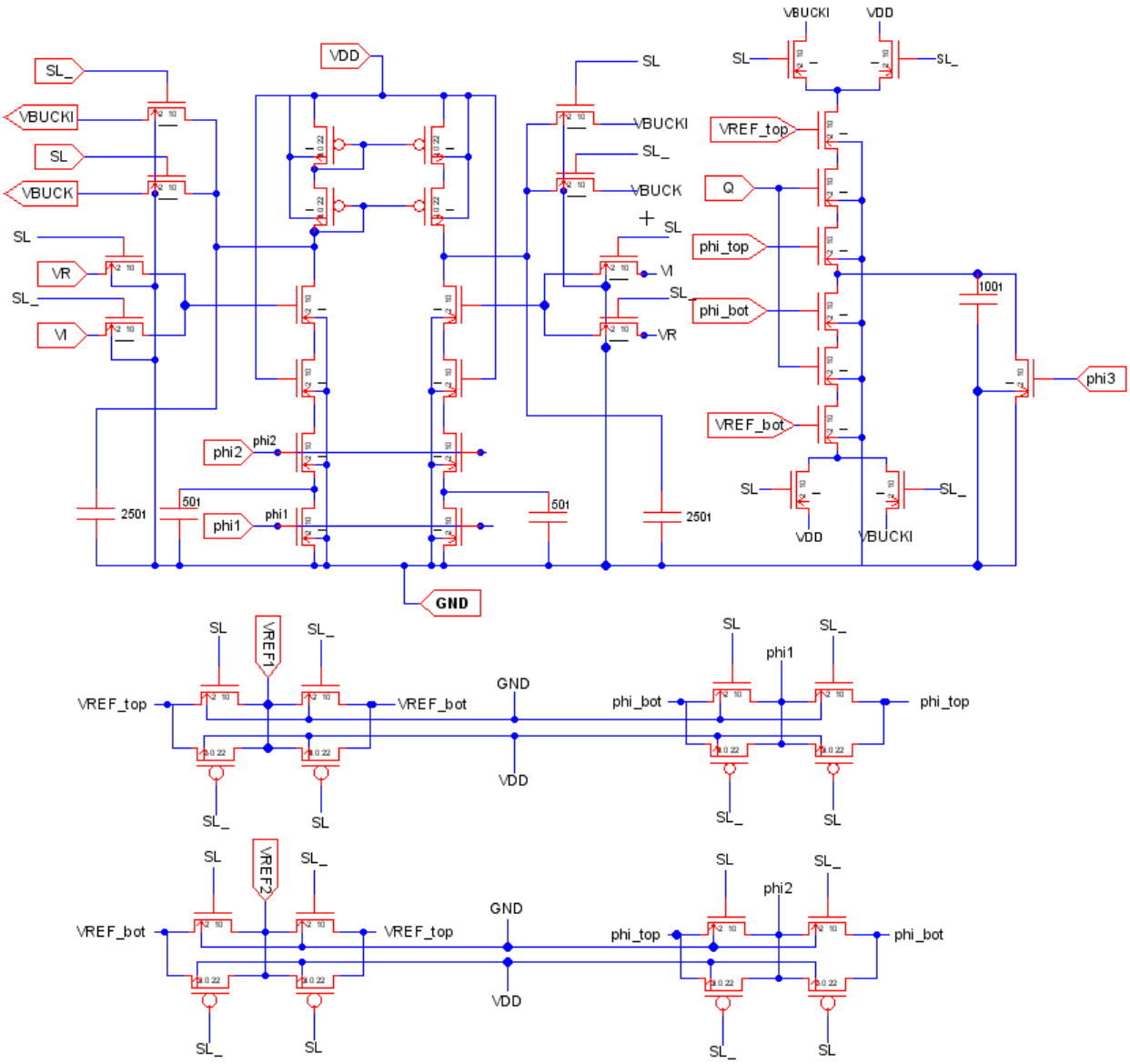

Figure A.6 –DSM circuit without comparator with additional circuitry to correct for device mismatch in the difference path

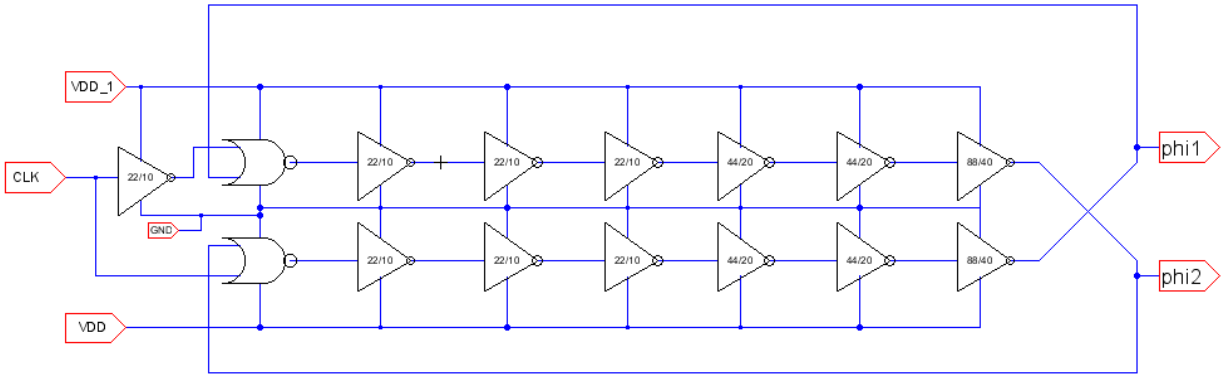

Figure A.7 –Clock generator