TMOS: A NOVEL DESIGN FOR MOSFET TECHNOLOGY

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Douglas R. Hackler Sr.

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Major Professor: R. Jacob Baker, Ph.D.

AUTHORIZATION TO SUBMIT

THESIS

This thesis of Douglas R. Hackler Sr., submitted for the degree of Master of Science with a major in Electrical Engineering and titled "TMOS: A NOVEL DESIGN FOR MOSFET TECHNOLOGY," has been reviewed in final form, as indicated by the signatures and dates given below. Permission is now granted to submit final copies to the College of Graduate Studies for approval.

Major Professor _____ Date 12/3/99
R. Jacob Baker

Committee Members _____ Date 12/09/99
Harry W. Li

_____ Date 12/3/99
Stephen Parke

Department Administrator _____ Date 12-9-99
David Egolf

Discipline's College Dean _____ Date 12/10/99
David Thompson

Final Approval and Acceptance by the College of Graduate Studies

_____ Date 12/21/99
Jean'ne M. Shreeve

ABSTRACT

"TMOS: A NOVEL DESIGN FOR MOSFET TECHNOLOGY"

by Douglas R. Hackler Sr.

MOSFET design has changed little throughout the history of microelectronics. New process technology used to optimize performance and allow this evolution could be applied to create an entirely new MOSFET structure. A Damascene device can make use of materials that have not been allowed in standard MOSFET devices. This thesis presents the simulation results for such a device. The Trench MOSFET (TMOS) device and process are defined. Two 0.1um device structures, the standard and TMOS, are simulated using Silvaco Athena and Atlas tools. Process development, flow and optimization are presented. Common DC parameters of merit and AC frequency response are used to evaluate the new design and compare it to a standard structure.

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INTRODUCTION

The MOSFET is the basic building block for the majority of integrated circuits throughout microelectronics history. It has been studied, modeled, optimized, shrunk and manufactured in efforts to continuously improve it's performance. However, the basic design of the device has changed little. Engineers have learned to accommodate the MOSFET's "non-idealities" at every level of the design process and new technologies have been developed to ameliorate it's shortcomings. In general, the MOSFET is a tried and true device that has worked very well.

However, what if a new device structure was developed that did not have the short channel problems, parasitic issues, limited poly level routing, complex patterning requirements and vast capital equipment investments required for today's electronic devices? What if a device was available that provided higher current, less leakage, lower power and smaller layouts without a major change in capital tooling? Perhaps the answer is that additional steps in microelectronics evolution could be much more easily, and quickly, achieved. The search for a device in the spirit of these "what-ifs" is the basis for this work.

Microelectronics fabrication techniques have developed rapidly to address the performance requirements for the evolution of the shrinking MOSFET. Improvements in optical lithography are advancing patterning technology to 0.1 micron (100nm) minimum feature size and beyond. [1] Resolution enhancement technology (RET) including phase shift masks (PSM) and optical proximity correction (OPC) combined with optical wavelengths as low as 157 nm make standard MOSFET structures production worthy at 100 nm. However, these

new optical systems are extremely expensive. A new MOSFET structure designed to be more forgiving to optical lithography could allow this expenditure to be delayed, or avoided, if it would allow existing 248nm systems to produce devices with area and performance comparable to standard 0.1um MOSFETs.

Minimum image resolution with coherent illumination is defined by the Rayleigh criterion as:

$$R = 0.5\frac{\lambda}{NA}$$

where lambda is wavelength and NA is numerical aperture. Complementary to this criterion, a second Rayleigh formula defines an expression for the depth of focus (DOF):

$$DOF = k_2 \frac{\lambda}{NA^2}$$

The proportionality constant k_2 depends on criteria for acceptable imaging and on the type of feature being imaged. A rule of thumb is k_2=0.8 for the total depth of focus for a mix of different feature types.[2] If the available wavelength is 248nm and 0.1um resolution is required, then the NA must be 1.24, which is non-sensically high, and would results in a DOF requirement of 1.29um! If resist thickness is assumed to be 1.0um, this demands a surface with practically no variation in topology. However, it also implies that extremely small features can be printed without moving to advanced lithography if a planar surface is provided!

Recent patterning process improvements involve technology that combines traditional lithography with chemical mechanical polishing (CMP). [3] This new Damascene approach has been applied to interconnect fabrication and allows metals such as Copper, Tungsten and

Tantalum to be used, some of which have been too difficult to etch or resulted in undesirable reliability prior to this technique.[4] Application of damascene processing to MOSFET gate structures could allow the use of these materials for standard MOSFET fabrication. This then allows for gate "workfunction engineering". Natural setting of V_{th}, no gate depletion and no dopant contamination of the gate oxide.

Shrinking lateral dimensions for any FET requires the oxide equivalent thickness to be reduced proportionally.[5] Deposited nitrided SiO_2 or Ta_2O_5 gate dielectrics combined with rapid thermal processing (RTP) allow for oxide thickness equivalent to the ultrathin requirements for sub-100 nm devices.[6]

RTP also supports other key technology issues associated with MOS junction and contact processes. The required ultra-shallow, heavily doped junctions can only be achieved by some type of short time thermal process. High doping densities require high annealing temperatures while ultra shallow junctions require short times and/or low temperatures.[7] RTP now provides process alternatives to achieve both of these constraints.

Process technology developments can be applied to manufacture alternative device structures not feasible for early or standard MOSFETs. Alternative FET structures requiring shallow source drain junctions were proposed as early as 1988 utilizing trench or "grooved gate" architecture to suppress short channel effects. [8] In 1993, this approach was

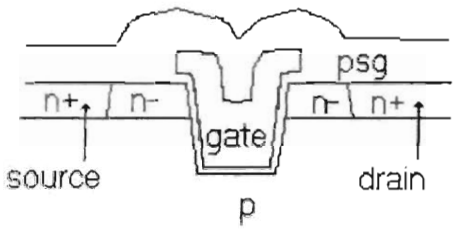


Figure 1: Grooved Gate MOSFET

demonstrated at the 0.1um level.[9] Simulations of this structure provide insight into the basis for the improved short channel behavior. [10] The electric fields for this structure do not support punchthrough. Short-channel effects are caused by drain potential extension into the source region, resulting in barrier lowering. [11] But inthis device, there is little, if any, lateral potential field generated below the channel. However, fabrication of the grooved-gate MOSFET is at least as difficult as that of the traditional MOSFET.

Alternative development of a similar structure was proposed and simulated in early 1998 in a senior design project using damascene techniques to simplify processing and relax photolithography requirements.[12] An unassociated effort published in December 1998 showed development and fabrication of a damascene gate process.[13] This structure with the benefit of CMP, damascene and a metal gate was shown to offer some reliability improvements, but the paper did not address short-channel issues other than those improvements from the metal gate.

After reviewing advanced microfabrication techniques, grooved gate structures and damascene device fabrication, a new structure was envisioned. The primary requirements for the device are suppressed short channel effects, low power, low leakage, high drain current and high frequency operation compared to a standard MOSFET of similar channel length. Additionally, the device must be no more difficult to fabricate than a standard MOSFET and also lend itself to CMOS processing.

PROBLEM DEFINITION

Design a deep sub-micron device (~0.1um) that takes advantage of advances in fabrication technology and device physics to overcome the short-channel performance penalties and fabrication complexities inherent to standard MOSFET production.

CREATION OF A BASELINE

The approach to this effort requires a baseline to compare the new device performance to. MOSFET models of devices less than 180 nm are still new enough that they are not readily available to many researchers and silicon implementations are exceedingly few. A 0.1 um, LDD MOSFET was designed as a baseline for this work, and is referred to as the "standard" process, or STD device. The experimental TMOS device was developed around the same critical geometry. Both of the designs were done using the simulation software package from Silvaco International. The Athena (Suprem) portion of the package was used for process and structure models. Device performance was simulated with the Atlas (Pisces) portion. (See Appendices A and B)

The standard LDD device process simulation for an n-type transistor is defined in process steps similar to the process flow that is required in actual fabrication.

STANDARD 0.1 um PROCESS

Standard 0.1 um MOSFET Process Flow

Wafer Start - Substrate: 100 p-type Silicon boron doped at 1e16.

Thermal Oxidation - This step is included to insure that the surface of the wafer is clean. Any contamination on the silicon surface is oxidized.

Punchthrough and Vt Adjustment Implant - This step increases the doping between the source and drain in order to control the lateral potential fields and eliminate punchthrough. This process also utilized the straggle of the Punchthrough implant to set the correct doping of the channel for the desired Vt characteristic. The Vt for this process is set to match that of the experimental device at 0.40 V.

Thermal Oxide Removal - The thermal oxide is stripped to remove any impurities and create a pristine surface for the gate oxide.

Gate Oxidation - A 20 angstrom strengthened oxide is deposited. This would typically be a nitrided oxide, or even possibly tantalum pentoxide. However, the oxide in the model is ideal and specified at the desired thickness. The strengthened oxides would be much thicker physically, but have the characteristics of a 20 angstrom SiO_2.

Poly Deposition - The gate structure for the 0.1 micron structure is the critical defining geometry for this device. Polysilicon is used because of its ability to be easily patterned. The polysilicon in this simulation is idealized with a boron doping concentration of $1e20/cm^3$. Considerable argument could be made for the feasibility of this in production. The doping would be required via ion implantation and some poisoning of the gate oxide would result. The simulator maintains an ideal doping uniformity of the poly and does not reflect the degradation of the gate oxide quality. Wherever possible, ideal performance has been included in the standard process to create an aggressive baseline for comparison of the experimental structure.

1st Mask - Gate Photolithography - At this point the gate is defined. 100 nm geometry can be optically achieved with phase-shift technology. The availability of this technology is critical for this design effort. The nature of photo processing requires tradeoffs between depth of focus and minimum feature size. The poly structure in this device is close to ideal, however in a typical CMOS process, non uniform surface conditions such as field oxide result in a loss of planarity.

Poly Oxidation - A thin oxide is grown to protect the poly and enhance the implantation of the LDD regions.

LDD Implantation - Lightly dope the source and drain with a phosphorous dose of $1e13/cm^2$.

Spacer Oxide Deposition and etchback - Deposit and etch an oxide to create spacers on either side of the poly to protect the lightly doped regions from the N+ source/drain implant.

Source Drain Implant - Implant the source and drain area with an arsenic dose of 1e14/cm^2, then anneal the wafer to repair all implant damage and set the junction depth.

Contact Deposition - Deposit Aluminum

Mask - Define the source and drain contacts and interconnects.

Process Complete

TMOS PROCESS DEVELOPMENT

Three performance issues were of primary importance for the development of this technology. First, the device was desired to be self-planarizing and capable of fabrication with non-traditional gate materials. Secondly, short channel effects (SCE) and device parasitic issues were to be reduced or eliminated with device geometry or additional non-traditional materials. Third, the device must work well at 0.1 um with better short-channel behavior than the standard MOSFET.

The SPD structure [12] was used as a starting point for the device because it already met the requirement for a better gate material (tungsten) and, with it's damascene architecture, it was planar in nature. The literature suggested that the size and shape of the channel corners could be used to control short-channel effects. "Inside" versus "outside" corners of the gate trench could dissipate electric fields to reduce SCE. The length of the sidewall, clip or rounding of the corner and flatness of the bottom are all Leff variables.

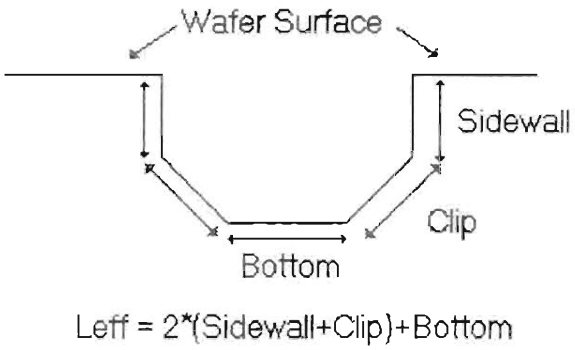


Figure 2: Damascene Channel Cross-section

The SPD design was modified to include Tungsten interconnects to reduce the non-idealities and limitations associated with poly-silicon and to reduce series resistance. Fabrication of the first interconnect layer had to be considered in order to avoid increasing the manufacturing complexity. The Damascene process was modified to a Dual Damascene approach so that first level interconnects could be patterned when the source and drain areas were defined. The Damascene process extensively utilizes chemical mechanical polishing (CMP). However, the CMP simulator was not licensed by BSU at the time of this work. The Silvaco deck was modified with a series of planarizing etch steps whenever CMP was required.

Previous research has suggested that drain current in this type of structure is only 50% of that achieved in STD devices due to the potential barrier created by the grooved gate structure. [10] However, simulations of alternative source and drain formations were shown to improve this to within 6% of the STD device. Reduction of series resistance was the approach used for this performance improvement. An Ohmic contact is required and does not allow the metal to be placed immediately on the lightly doped substrate. Traditional implant methods

were evaluated and rejected due to their propensity to diffuse into the channel and to create larger junction depths. The alternative developed for the TMOS process utilizes the Damascene structure to align a poly doping source to the source and drain regions. This is capped with tungsten, then annealed to form an Ohmic contact with a very shallow junction. This process was further improved after results by etching away the poly prior to tungsten deposition, further reducing series resistance and improving Idmax. Junction depths can be compared on the plots provided in the appendices.

The use of tungsten for both first level interconnects and gates has several benefits other than reduced resistance. Standard devices using doped polysilicon are subject to the doping of the poly, usually boron, diffusing into and degrading the gate oxide. Tungsten gates eliminate this issue entirely, but require the avoidance of high temperature processing after deposition. Threshold is another consideration. Polysilicon gate work functions require that the channel doping be modified for 1e16 boron doped silicon in order to generate the target Vt of 0.4V. Tungsten has a work function of 0.455 eV. This results in a natural device threshold voltage of ~0.4V. (See Appendix C) Note: CMOS processing would require characterization of this material and additional doping considerations for fabrication of PMOS devices.

TMOS 0.1 um PROCESS

TMOS 0.1 um MOSFET Process Flow

Wafer Start - Substrate: 100 p-type Silicon boron doped at 1e16

Thermal Oxidation - This step is included to insure that the surface of the wafer is clean. Any contamination on the silicon surface is oxidized. An alternative that could be used for this process is an SC1 portion of an RCA clean. [14] This process also removes a small amount of silicon from the wafer surface, and associated contaminants. The benefit is that the RCA clean actually reduces surface roughness. Roughness can be transferred into the trench and channel in the etch process.

STI - Shallow trench isolation was used for this device consistent with the demand for a planar architecture. A deposited dielectric is used for this simulation, however, a thermal oxide could be used. Modification of this step must also be used to provide the isolation channels for the source, drain and gate interconnects. (Note: STI structures are 0.1 X 0.1 um. Careful examination of simulation output scaling is required when referring to structures in the appendices)

S/D Trench Etch - A trench for the entire device is fabricated at this step. S/D formation is typically been done post gate processing. However, it is done early for TMOS to simplify the process (self-aligns all critical structures), provide for the use of tungsten interconnects (creates Damascene processing for the metal) and contribute to maintaining planarity of the silicon surface for critical geometry patterning.

Barrier/Tungsten S/D Deposition - The formation of the source and drain regions is done by depositing a thin film of highly doped poly-silicon followed by a tungsten deposition to fill the trench. Thermal activation of this structure results in a very shallow junction diffused from the arsenic doped poly into the boron doped silicon. This process significantly reduces series

resistance and results in improved Idmax. The shallow junction also insures that significant lateral or vertical diffusion into the channel region does not occur.

1st CMP - This step is used to planarize the surface of the MOSFET prior to gate photolithography. The poly and tungsten are removed at the wafer surface. This creates the first level interconnects and source/drain contacts.

Gate Photo Mask 3 - The critical geometry gate length, the minimum size feature of the technology is defined at this step. The complete planarity of the device structure and wafer surface results in relaxing DOF requirements to their optimum. The gate is patterned in the middle of the S/D trench structure. This allows for maximum tolerance of overlay because of the non-critical relationship of marginally different source and drain lengths. Further, overlap parasitics of the gate beyond the width of the channel are eliminated due to the placement of the STI definition of the device width. The DC simulations in this thesis were run for this structure. However, concern for Gate to Drain capacitance and tungsten patterning were considered versus this simplest process flow. The alternative is to add an additional mask/damascene step

for the tungsten source, drain and interconnects as the last step in the process. The tungsten deposited prior to gate formation being replaced with oxide. This results in the spacer ox structure shown in the appendix.

Gate Etch - A variety of channel depths and corner shapes were simulated at this step. Leff is computed by determining the channel length from junction to junction between the source and drain. Unlike the baseline device, the channel length is composed of vertical and horizontal components. In the simplest structure, L is equal to the critical geometry plus 2 times the

distance from the bottom of the gate trench to the S/D junction. A flat junction device was fabricated by etching the gate trench just slightly past the S/D junction.

Punchthrough and Vt Adjustment Implant - Additional boron doping is NOT required in this process. Reduction of doping in the channel is desirable to improve mobility. The Vt of the device using the described substrate doping and the tungsten gate is ~ 0.4 V (comparable to the baseline device). A punchthrough implant is not required because of the potential field management provided by the device geometry. Examination of the potential simulations for any TMOS structure in the appendices illustrates that unlike the standard Mosfet, the TMOS device potential field primarily propagates in the vertical with little lateral behavior, thus significantly limiting punchthrough and SCE.

Gate Oxide Deposition - A deposited oxide was selected for this device in order to meet requirements for conformance and low temperature (post-metal) processing. Further, a deposited oxide met the requirements for oxide integrity concerns raised from utilizing a channel that had exposure to the significant processing (possible contamination) required for this structure. A variety of deposited oxides have been demonstrated with performance comparable to thermal oxides. [15]

Tungsten Gate Deposition - Tungsten is used as the gate material and easily patterned in this technology through the use of the damascene structure.

Tungsten Gate CMP - The final step of the TMOS fabrication defines the gate, gate interconnects and planarizes the surface of the wafer for ideal multiple metal layer processing.

Alternative S/D Processing - Contacts are defined through the oxide to the poly-silicon. Damascene processing is then used to finish the application of the final tungsten layer.

This results in a substantial oxide thickness between the S/D and the Gate and reduces $C_{gs,d}$ to only that which is contributed by the gate to poly overlap. DC simulations of this structure indicate that DC characteristics for the device are unchanged by this process variation.

ATHENA PROCESS SIMULATION DECK

To simulate the device fabrication process in Silvaco, a process "deck", or list of commands, must be specified. The decks developed for the Standard and TMOS structures (See Appendix A and B) are input to Athena which simulates and defines the structure that is passed to ATLAS for DC and AC simulations. In addition to providing the basis for ATLAS simulations, ATHENA provides process details such as potential fields, electron and hole concentrations, doping profiles and material orientations.

ATLAS DC SIMULATION

The parameters extracted from the DC simulations are:

DIBL - Drain Induced Barrier Lowering, The change in Vg to drive Id = 1e-4 A with Vd varying from 1.5 to 2.5 V.

Idmin - Sub-threshold leakage current

Idmax - Maximum drain current attained at Vdd = 1.5 V

Threshold Voltage - The applied gate voltage where Id = 1.0 um

Sub-threshold Swing - Volts/Decade required to move Id from Idmin to 1.0 uA

Transconductance - dId/dVg

ro - Output resistance, dVd/dId at 1.4 t0 1.5 V

ATLAS AC SIMULATION

Frequency Response modeling was done using Atlas small signal analysis applied to the Athena model developed for DC simulations. The set-up for the simulation is shown below.

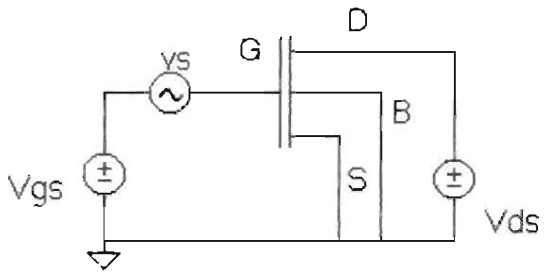


Figure 3: AC Simulation Circuit

The gate and the drain are set to 1.5 Volts, the design voltage for the process. The small signal is applied in series with the gate voltage supply. Source and bulk are grounded.

The frequency response, or "speed" of the device is defined as the unity current gain, f_T. [16] The unity gain frequency is,

$$f_T = \frac{KP \cdot W(V_{GS} - V_{THN})}{2\pi L(C_{gb} + C_{gs} + C_{gd})} \approx \frac{KP \cdot W}{2\pi L C_{gs}}(V_{gs} - V_{THN})$$

Additionally, since the potential across C_{db} and C_{sb} is fixed, they can be eliminated and it can easily be seen that f_T must scale as,

$$\frac{\mu}{L^2}$$

Specifically, to improve the speed of a MOSFET, mobility must be increased relative to the square of the channel length.

STANDARD VERSUS TMOS PROCESS DIFFICULTY COMPARISON

A primary requirement for a feasible device alternative is that it must be no more difficult to fabricate than a conventional MOSFET. The two processes are displayed simultaneously below for comparison.

STANDARD FLOW	TMOS FLOW
Implant 1 - Vt Adjust	Mask 1 - STI
Ox 1 - Gate Ox	Ox 1 - STI
Poly Dep	Mask 2 - Trench Etch
Mask 1 - Gate	Implant 1
Ox 2 - Poly Ox	Poly Dep
Implant 2 - LDD	Metal 1 - S/D
Ox 3 - Spacer	CMP - 1
Mask 2 - S/D	Mask 3 - Gate
Implant 3 - S/D	Ox 2 - Gate
Mask 3 - Contact	Metal - 2
Metal 1 - S/D	CMP - 2
Mask 4 - Pattern Metal	

Table 1: Standard versus TMOS Process Flow

The most obvious difference in the two is the reduced mask content for the TMOS flow. This is even a greater advantage than first observed, because an additional mask would be required to provide STI for the standard flow.

The TMOS flow has two primary advantages beyond the reduced mask count. #1. The damascene process allows metal to be used for all gate, source and drain interconnects without etch concerns and with maximum utilization of photolithography equipment from optimum planarity. #2. Only one implant and one anneal step is required, significantly simplifying management of the thermal budget.

STANDARD VERSUS TMOS SIMULATION COMPARISONS

The TMOS process flow has been shown to be at least no more difficult, and in many ways much easier to manufacture than the conventional flow used for the standard MOSFET. However, the performance of the fabricated devices ultimately determines the structure best suited to circuit applications. Atlas simulations were run to provide a comparison of device performance expectations. A number of DC parameters were evaluated, including short channel behavior. Additionally, small signal AC simulations were run to compare the expected device speeds.

	TMOS Flat Junction	TMOS Flat Junction with Spacer Ox	TMOS Shallow Junction Round Corner	TMOS Shallow Junction Clipped Corner	TMOS Shallow Junction Square Corner
Leff (um)	0.1	0.1	0.1+	0.101	0.104
DIBL (V/V)	0.0147	0.0271	0.0128	0.0124	0.0123
Idmin A/um	1.80E-11	4.26E-11	1.58E-11	1.28E-11	1.26E-11
Swing ST	0.085	0.09	0.085	0.084	0.084
Vt (V)	0.41	0.39	0.4	0.42	0.41
Idmax(uA/um	921	508	728	814	798
ro (Ohm/um)	22100	36200	38700	25500	25700

	Standard LDD MOSFET	TMOS Deep Junction Round Corner	TMOS Deep Junction Clipped Corner	TMOS Deep Junction Square Corner
Leff (um)	0.076	0.101	0.107	0.108
DIBL (V/V)	0.0372	0.0332	0.0161	0.0164
Idmin A/um	4.56E-11	7.54E-12	5.71E-12	5.60E-12
Swing ST	0.092	0.082	0.081	0.081
Vt (V)	0.4	0.42	0.42	0.43
Idmax(uA/um	979	769	757	727
ro (Ohm/um)	7970	39600	24600	27300

Table 2: 0.1 um MOSFET DC Simulation Data

Leff was measured for the different structures tested. The comparison of device performance was done without adjusting all devices to the same channel length. This approach was taken due to all structures running in Athena with the same minimum feature size. These results indicate a reasonable comparison for devices that could be fabricated within the context of a standard installed equipment base for 0.1 um minimum feature photolithography.

The STD device actually developed a Drain Current that was over 6% greater than that demonstrated by any of the TMOS devices with a Leff that was 24% smaller due to lateral diffusion. However, due to the comparison guidelines, the advantage of current per channel length of the TMOS device is discounted because it would not be a manufacturable advantage.

Drain induced barrier lowering (DIBL) is a significant concern for continued migration to shorter channel lengths. Extreme cases of DIBL can actually result in punchthrough. DIBL was shown to be much less for the TMOS device than the STD, generally reduced by more than 50%. This is due to the field management that is possible in the TMOS structure. E-fields propagate vertically and laterally under the source and drain regions of the STD device. Lateral propagation results in loss of gate control. The TMOS device virtually eliminates lateral propagation. This effect is clearly shown in the potential contour plots for the devices in the appendices.

Leakage current (Idmin) of the TMOS device is highly dependent on the trench geometry. However, it was also generally better than that of the STD device. Additional simulation of this parameter was done with the model enhanced for impact ionization consideration. Leakage through the substrate ground was observed in both devices as Vdrain increased. The TMOS device performance was worse than that of the STD up to Vdrain = 2V. For Vdrain above 2V, avalanche breakdown was observed in the STD device. However, even with the

higher substrate current, the short-channel characteristic of the TMOS device was much better.

Sub-Threshold Swing (SwingST) was better in the TMOS structures than in the STD device with a value of 81mV/dec versus 92mV/dec.

The threshold voltages (Vt) for the simulation were targeted at 0.4V. The STD device required higher channel doping to achieve this due to the poly-silicon gate. The TMOS device achieved this naturally with the use of the Tungsten gate.
Maximum drain current (Idmax) was greatest for the STD device. However, this advantage is negated by the DIBL and short-channel behavior.

Output resistance was several times greater for the TMOS structure, regardless of geometry, over the STD. This is a clear demonstration of the improved short channel performance of the TMOS device. The TMOS structure clearly demonstrates better gate control of drain current.

Short channel behavior can be shown with Vt plotted against channel length (Vt Roll-Off). The figure below clearly illustrates TMOS superiority in this area.

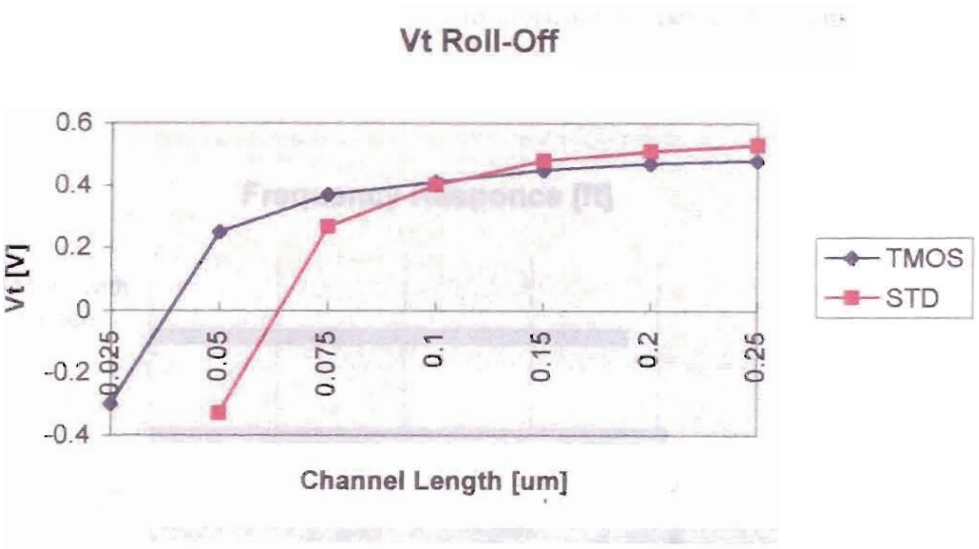


Figure 4: TMOS versus STD Vt Roll-Off

Good DC characteristics are required for any device and AC performance is becoming more important for high speed processing. Speed is an important factor. Small signal modeling was performed in Atlas to compare the frequency response of the different structures. The major concern for the TMOS device was the larger parallel plate capacitors formed on either side of the gate due to the close proximity of the source and drain electrodes.

The TMOS device was slower than the STD, 81.4 versus 99.9 GHz. An attempt was made to modify the TMOS structure by adding additional oxide on either side of the gate. This approach did not resolve the performance issue and actually made it worse by significantly reducing Idmax. On first inspection, this might appear to indicate that the TMOS device cannot match the speed of the STD structure. However, the damascene process allowed for the complete replacement of all polysilicon with Tungsten. In circuit applications, parasitic capacitance of the interconnect network limits the true speed. Speed is forecast as a major

advantage of TMOS because of the ability to fabricate all metal interconnects inside oxide insulated trenches.

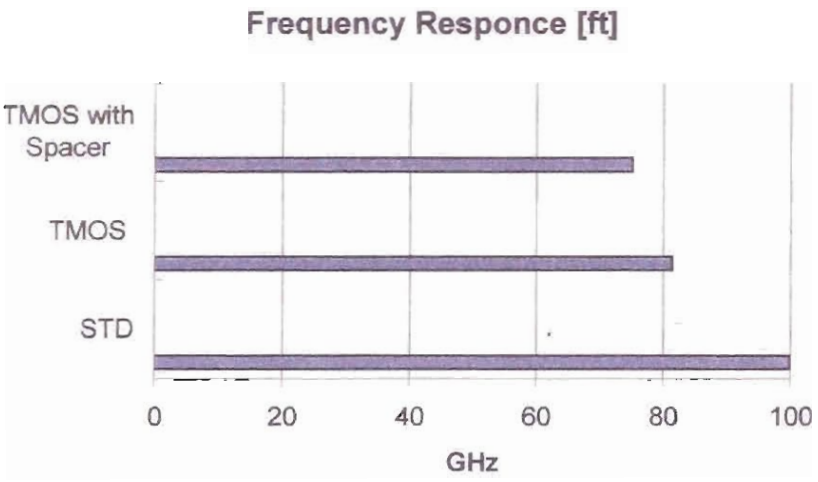


Figure 5: Frequency Response

FIRST PASS DESIGN IMPROVEMENT OF TMOS

Standard MOSFET architecture has evolved through decades of technology evolution. The structure has been constantly improved. A first pass attempt to improve the TMOS design yields additional benefits for the application of new process technology to the novel design. A rapid thermal anneal (RTA) followed by the removal of the poly-silicon applied prior to S/D tungsten depostion further improves TMOS performance. This structure was modeled with consideration for impact ionization. The flat gate option was evaluated with this technique (TMOS_Id_ RTP3.log in Appendix N) and then compared to the performance of :

The Standard Device (STDmos_Id_STD3.log)

TMOS with poly and Flat Junction (TMOS_Id_FLAT3.log)

TMOS with poly and Deep Junction (TMOS_Id_DEEP.log)

The IV curves show that this one improvement reduces substrate leakage, improves Idmax, improves SwingST, and maintains short channel performance.

CONCLUSION

The novel architecture of the TMOS device utilizes current technology to address short channel problems facing continued channel length reductions. The ability to utilize metal without patterning problems, control potential fields, reduce the thermal budget and maximize capital equipment life through planarity demonstrates the ability of new structures to better address technology migration than that of conventional MOSFET structures. Additionally, the future technologies currently in development such as SOI and 3-D devices will need to make use of non-traditional techniques like these in order to become feasible mainstays for legitimate manufacturing solutions.

Appendix A. Silvaco Deck for Standard Baseline Process

```
# Doug Hackler - TMOS Design Project
#
# STANDARD 0.1 um MOSFET Athena Deck

go athena

#
line x loc=0.0 spac=0.02
line x loc=0.102 spac=0.001
line x loc=0.142 spac=0.001
line x loc=0.182 spac=0.002
#
line y loc=0.0 spac=0.0004
line y loc=0.08 spac=0.005
line y loc=0.1 spac=0.01
line y loc=0.15 spac=0.03

#

init orientation=100 c.boron=1e16 space.mul=2
#
#_____

#
#Vt ADJUST
implant boron dose=0.92e12 energy=13 pearson

#_____

#GATE OX

deposit oxide thick=.002 DIV=5

# Extract a design parameter
extract name="gateox" thickness oxide mat.occno=1 x.val=0.05

#_____

#POLY DEPOSITION

method poly.diff
deposit poly thick=0.05 c.boron=1.0e20 divi=10

#PATTERN POLY

etch poly left p1.x=0.132

#
structure outfile=1_gate.str
tonyplot  1_gate.str
#_____

#GROW AN OXIDE
method fermi compress
diffuse time=1.0 temp=900 weto2 press=1.0

structure outfile=ox.str
tonyplot  ox.str
#_____
```

```
#LDD (Phos) IMPLANT

#Protect the doped poly from phos implant.
deposit oxide thick=.1
etch oxide start    x=0       y=-.16
etch       continue x=.12743 y=-.16
etch       continue x=.12743 y=-.0035
etch       done     x=0       y=-.0035

#Lightly dope the source and drain
implant phosphor dose=1.0e13 energy=5 pearson

etch oxide above p1.y=-.05655

structure outfile=2_LDD.str
tonyplot  2_LDD.str
#_____________________________________________________________

#SPACER OXIDE

depo oxide thick=0.02 divisions=8

etch oxide dry thick=0.02

structure outfile=3_spaceox.str
tonyplot  3_spaceox.str
#_____________________________________________________________


#S/D IMPLANT

implant arsenic dose=1.0e14 energy=10 pearson

method fermi compress
diffuse time=0.25 temp=900 nitro press=1.0

structure outfile=4_SDimp.str
tonyplot 4_SDimp.str
#_____________________________________________________________


#S/D METALIZATION

etch oxide left p1.x=0.104
deposit alumin thick=0.05 divi=5
etch alumin right p1.x=0.1
etch alumin above p1.y=-0.049
#
structure outfile=STDfinal.str
tonyplot  STDfinal.str
#_____________________________________________________________


# Extract design parameters

# extract final S/D Xj
extract name="nxj" xj silicon mat.occno=1 x.val=0.05 junc.occno=1

# extract the N++ regions sheet resistance
```

```
extract name="n++ sheet rho" sheet.res material="Silicon" mat.occno=1 x.val=0.025 region.occno=1

# extract the sheet rho under the spacer, of the LDD region
extract name="ldd sheet rho" sheet.res material="Silicon" \
        mat.occno=1 x.val=0.15 region.occno=1

# extract the surface conc under the channel.
extract name="chan surf conc" surf.conc impurity="Net Doping" \
        material="Silicon" mat.occno=1 x.val=0.18

# extract a curve of conductance versus bias.
extract start material="Polysilicon" mat.occno=1 \
        bias=0.0 bias.step=0.2 bias.stop=2 x.val=0.18
extract done name="sheet cond v bias" \
        curve(bias,1dn.conduct material="Silicon" mat.occno=1  region.occno=1)\
        outfile="extract.dat"

# extract the long chan Vt
extract name="nldvt" ldvt ntype vb=0.0 qss=1e10 x.val=0.18


structure mirror right

electrode name=gate x=0.2 y=0.1
electrode name=source x=0.05
electrode name=drain x=0.35
electrode name=substrate backside

structure outfile=STD_Mosfet.str

# plot the structure
tonyplot  STD_Mosfet.str

#_____________________________________________________________
```

```
##################################################################
#                                                                #
#                   DIBL SIMULATION (Id/Vgs)                     #
#                                                                #
#                   (vgate=1.5, vdrain=1.5)                      #
#             Vt Test : Returns Vt, Beta and Theta               #
#                                                                #
##################################################################

go atlas

# set material models
models cvt srh print

contact name=gate n.poly
interface qf=1e10

method gummel newton
solve init

# Bias the drain
solve vdrain=0.1 outf=solve_tmp1
solve vdrain=1.5 outf=solve_tmp2
solve vdrain=2.0 outf=solve_tmp3
solve vdrain=2.5 outf=solve_tmp4

#Load in temporary files and Ramp the gate

load infile=solve_tmp1
log outf=STDmos10.log
solve vgate=0 vstep=0.1 vfinal=1.5 name=gate

load infile=solve_tmp2
log outf=STDmos15.log
solve vgate=0 vstep=0.1 vfinal=1.5 name=gate

load infile=solve_tmp3
log outf=STDmos20.log
solve vgate=0 vstep=0.1 vfinal=1.5 name=gate

load infile=solve_tmp4
log outf=STDmos25.log
solve vgate=0 vstep=0.1 vfinal=1.5 name=gate

# plot results
tonyplot  -overlay STDmos10.log STDmos15.log STDmos20.log STDmos25.log
#tonyplot STDmos15.log

# extract device parameters
extract name="nvt" (xintercept(maxslope(curve(abs(v."gate"),abs(i."drain")))) \
        - abs(ave(v."drain"))/2.0)
extract name="nbeta" slope(maxslope(curve(abs(v."gate"),abs(i."drain")))) \
        * (1.0/abs(ave(v."drain")))
extract name="ntheta" ((max(abs(v."drain")) * $"nbeta")/max(abs(i."drain"))) \
        - (1.0 / (max(abs(v."gate")) - ($"nvt")))

#_____________________________________________________________
```

```
############################################################
#                                                          #
#              SIMULATE Divice Field Contour               #
#                                                          #
#                   (vgate=1.5, vdrain=1.5)                #
#                                                          #
############################################################

go atlas

# set material models
models cvt srh print

contact name=gate n.poly
interface qf=1e10

method gummel newton
solve init

# Bias the drain
solve vdrain=1.5
solve vgate=0
save outf=STDmos0.str
tonyploy STDmos0.str

# Ramp the gate
log outf=STDmos.log master
solve vgate=0 vstep=0.1 vfinal=1.5 name=gate
save outf=STDmos15.str
tonyplot STDmos15.str
#_____________________________________________________________

#################################################################
#                                                               #
#    SIMULATE DRAIN CURRENT AT 0.5, 1.0 and 1.5 VOLTS.          #
#                                                               #
#  (Id curve simulation as shown in Example: moslex09.in)       #
#                                                               #
#################################################################

go atlas2

# define the Gate workfunction
contact name=gate n.poly

# Define the Gate Qss
interface qf=1e10

# Use the cvt mobility model for MOS
models cvt srh

# set gate biases with Vds=0.0
solve init
solve vgate=.5 outf=solve_tmp1
solve vgate=1.0 outf=solve_tmp2
solve vgate=1.5 outf=solve_tmp3

#load in temporary files and ramp Vds

load infile=solve_tmp1
```

```
log outf=STDmos_Id_1.log
solve name=drain vdrain=0 vfinal=1.5 vstep=0.1

load infile=solve_tmp2
log outf=STDmos_Id_2.log
solve name=drain vdrain=0 vfinal=1.5 vstep=0.1

load infile=solve_tmp3
log outf=STDmos_Id_3.log
solve name=drain vdrain=0 vfinal=1.5 vstep=0.1

# extract max current and saturation slope
extract name="pidsmax" max(abs(i."drain"))
extract name="p_sat_slope" slope(minslope(curve(abs(v."drain"),abs(i."drain"))))

tonyplot -overlay STDmos_Id_1.log STDmos_Id_2.log STDmos_Id_3.log
#tonyplot STDmos_Id_3.log

#_____________________________________________________

quit
```

Appendix B. Silvaco Deck for TMOS Process

```
# Doug Hackler - TMOS Design Project

# TMOS Design Model and Simulation Deck

go athena

# Set up a mesh
#
#
#
line x loc=0.00  spac=0.01
line x loc=0.01  spac=0.005
line x loc=0.17  spac=0.001
line x loc=0.25  spac=0.00024
line x loc=0.2512 spac=0.00024
line x loc=0.3   spac=0.001

#
line y loc=0.00  spac=0.01

line y loc=0.0538  spac=0.00024
line y loc=0.055  spac=0.00024

#y=.052 for shallow junction

line y loc=0.07  spac=0.001
line y loc=0.10  spac=0.001
line y loc=0.15  spac=0.002
#
#_____________________________________________________

#STEP 1

# Starting Material

     init orientation=100 c.boron=1e16 space.mul=2
#_____________________________________________________

#STEP 2

# Initial Oxidation

#     Thermal oxidation for surface cleaning.

#_____________________________________________________

#STEP 3
################## STI PHOTO - MASK 1 ####################
#_____________________________________________________

#STEP 4

# STI TRENCH ETCH

     #STI Trench (Square corner)
     etch silicon start    x=.05    y=0
     etch          continue x=.15    y=0
     etch          continue x=.15    y=.1
     etch          done     x=.05    y=.1
```

```
#    PLOT STI Trench Etch
#     structure outfile=4_STItrench.str
#tonyplot 4_STItrench.str
#_____________________________________________________

#STEP 5

# Second Oxidation

     deposit oxide thick=.15 DIV=6

#    PLOT Second Oxidation
#     structure outfile=5_2nd_Ox.str
#tonyplot 5_2nd_Ox.str
#_____________________________________________________

#STEP 6
################## S/D PHOTO - MASK 2 ##################
#_____________________________________________________

#STEP 7

#  S/D ETCH

     #Etch Oxide for S/D
     etch oxide   start    x=.15  y=-.2
     etch         continue x=.3   y=-.2
     etch         continue x=.3   y=0.0
     etch         done     x=.15  y=0.0

#    PLOT S/D Etch
#     structure outfile=7_SD_Etch.str
#tonyplot 7_SD_Etch.str
#_____________________________________________________

#STEP 8

#  S/D TRENCH ETCH

     #Etch Silicon Trench (Square corner)
     etch silicon start    x=.15   y=0
     etch         continue x=.3    y=0
     etch         continue x=.3    y=.05
     etch         done     x=.15   y=.05

#    PLOT 1st Trench Etch
#     structure outfile=8_SDtrench.str
#tonyplot 8_SDtrench.str
#_____________________________________________________
#
#STEP 9

# Barrier/Tungsten S/D Deposition

#
     # Diffusion Barrier DepositioN
     deposit poly thick=0.01 c.arsenic=1.0e20 divi=3


     # Tungsten Deposition
```

```
     deposit tungsten thick=0.1 divi=10

#      structure outfile=9_SD.str
#tonyplot 9_SD.str


#_____________________________________________________________

#STEP 10

# 1st CMP (Use etch to simulate CMP)

     etch tungsten above p1.y=0.0
     etch poly  above p1.y=0.00
     etch oxide     above p1.y=0.00

#     PLOT 1st CMP
#      structure outfile=10_1stCMP.str
#tonyplot 10_1stCMP.str
#_____________________________________________________________

#STEP 11
################ GATE PHOTO - MASK 3 ######################
#_____________________________________________________________

#STEP 12 - 4 Process variations are defined here.

#Flat Junction no corner
# Channel Trench Etch

     # Etch the channel in the silicon
#     etch tungsten start    x=.25  y=.0
#     etch          continue x=.3   y=.0
#     etch          continue x=.3   y=.041
#     etch          done     x=.25  y=.041

     # Etch the channel in the silicon
#     etch poly     start    x=.25  y=.0
#     etch          continue x=.3   y=.0
#     etch          continue x=.3   y=.051
#     etch          done     x=.25  y=.051

    # Etch the channel in the silicon - required due to shallow
    # doping from the polysilicon

#     etch silicon  start    x=.25  y=.0
#     etch          continue x=.3   y=.0
#     etch          continue x=.3   y=.0508
#     etch          done     x=.25  y=.0508


#Shallow junction square corner
# Channel Trench Etch

     # Etch the channel in the silicon
#     etch tungsten start    x=.25  y=.0
#     etch          continue x=.3   y=.0
#     etch          continue x=.3   y=.041
#     etch          done     x=.25  y=.041
```

```
     # Etch the channel in the silicon
#     etch poly      start    x=.25  y=.0
#     etch           continue x=.3   y=.0
#     etch           continue x=.3   y=.051
#     etch           done     x=.25  y=.051

     # Etch the channel in the silicon
#     etch silicon   start    x=.25  y=.0
#     etch           continue x=.3   y=.0
#     etch           continue x=.3   y=.052
#     etch           done     x=.25  y=.052


#Deep junction square corner
# Channel Trench Etch

     # Etch the channel in the silicon
#     etch tungsten start    x=.25  y=.0
#     etch           continue x=.3   y=.0
#     etch           continue x=.3   y=.041
#     etch           done     x=.25  y=.041

     # Etch the channel in the silicon
#     etch poly      start    x=.25  y=.0
#     etch           continue x=.3   y=.0
#     etch           continue x=.3   y=.051
#     etch           done     x=.25  y=.051

     # Etch the channel in the silicon
#     etch silicon   start    x=.25  y=.0
#     etch           continue x=.3   y=.0
#     etch           continue x=.3   y=.055
#     etch           done     x=.25  y=.055

#Deep junction clipped corner
# Channel Trench Etch

     # Etch the channel in the silicon
     etch tungsten start    x=.25  y=.0
     etch           continue x=.3   y=.0
     etch           continue x=.3   y=.041
     etch           done     x=.25  y=.041

     # Etch the channel in the silicon
     etch poly      start    x=.25  y=.0
     etch           continue x=.3   y=.0
     etch           continue x=.3   y=.051
     etch           done     x=.25  y=.051

     # Etch the channel in the silicon
     etch silicon   start    x=.25    y=.0
     etch           continue x=.3     y=.0
     etch           continue x=.3     y=.055
     etch           continue x=.2512  y=.055
     etch           done     x=.25    y=.0538

     # Etch the channel in the silicon
     etch silicon   start    x=.25    y=.0
     etch           continue x=.3     y=.0
     etch           continue x=.3     y=.055
```

```
    etch          continue x=.2512  y=.055
    etch          done     x=.25    y=.0538

#Deep junction round corner
# Channel Trench Etch

    # Etch the channel in the silicon
#    etch tungsten start    x=.25  y=.0
#    etch          continue x=.3   y=.0
#    etch          continue x=.3   y=.041
#    etch          done     x=.25  y=.041

    # Etch the channel in the silicon
#    etch poly     start    x=.25  y=.0
#    etch          continue x=.3   y=.0
#    etch          continue x=.3   y=.051
#    etch          done     x=.25  y=.051

    # Etch the channel in the silicon
#    etch silicon  start    x=.25    y=.0
#    etch          continue x=.3     y=.0
#    etch          continue x=.3     y=.055
#    etch          continue x=.275   y=.055
#    etch          continue x=.256   y=.0542
#    etch          done     x=.25    y=.05182

    # Etch the channel in the silicon
#    etch silicon  start    x=.25    y=.0
#    etch          continue x=.3     y=.0
#    etch          continue x=.3     y=.055
#    etch          continue x=.275   y=.055
#    etch          continue x=.256   y=.0542
#    etch          done     x=.25    y=.05182

#Shallow junction round corner
# Channel Trench Etch

    # Etch the channel in the silicon
#    etch tungsten start    x=.25  y=.0
#    etch          continue x=.3   y=.0
#    etch          continue x=.3   y=.041
#    etch          done     x=.25  y=.041

    # Etch the channel in the silicon
#    etch poly     start    x=.25  y=.0
#    etch          continue x=.3   y=.0
#    etch          continue x=.3   y=.051
#    etch          done     x=.25  y=.051

    # Etch the channel in the silicon
#    etch silicon  start    x=.25  y=.05
#    etch          continue x=.3   y=.05
#    etch          continue x=.3   y=.052
#    etch          continue x=.2512  y=.052
#    etch          done     x=.25  y=.0508

    # Etch the channel in the silicon
#    etch silicon  start    x=.25  y=.05
#    etch          continue x=.3   y=.05
#    etch          continue x=.3   y=.052
```

```
#     etch          continue x=.2512  y=.052
#     etch          done     x=.25  y=.0508

#Shallow junction Clipped corner
# Channel Trench Etch

     # Etch the channel in the silicon
#     etch tungsten start    x=.25  y=.0
#     etch          continue x=.3   y=.0
#     etch          continue x=.3   y=.041
#     etch          done     x=.25  y=.041

     # Etch the channel in the silicon
#     etch poly     start    x=.25  y=.0
#     etch          continue x=.3   y=.0
#     etch          continue x=.3   y=.051
#     etch          done     x=.25  y=.051

#     etch silicon  start    x=.25  y=.05
#     etch          continue x=.3   y=.05
#     etch          continue x=.3   y=.052
#     etch          continue x=.2512  y=.052
#     etch          done     x=.25  y=.0508

#   etch silicon  start    x=.25  y=.05
#   etch          continue x=.3   y=.05
#   etch          continue x=.3   y=.052
#   etch          continue x=.2512  y=.052
#   etch          done     x=.25  y=.0508

#    PLOT 2nd Trench
     structure outfile=12_ChanTrenEt.str
tonyplot 12_ChanTrenEt.str

#_____________________________________________________________

#STEP 13 Gate Oxide Deposition

     # Deposit Gate Ox
    deposit oxide thick=.002 DIV=5

#    PLOT Gate Oxide Dep
#     structure outfile=17_Gate_Ox.str
#tonyplot 13_Gate_Ox.str
#_____________________________________________________________


#STEP 14 Tungsten 1 - Gate Deposition

     # Tungsten Deposition
   deposit tungsten thick=0.1 divi=10

#    PLOT Tungsten Gate Deposition
#     structure outfile=14_T1Gatedep.str
#tonyplot  14_T1Gatedep.str
#_____________________________________________________________

#STEP 15 Tungsten Gate CMP

     etch tungsten above p1.y=0.00
```

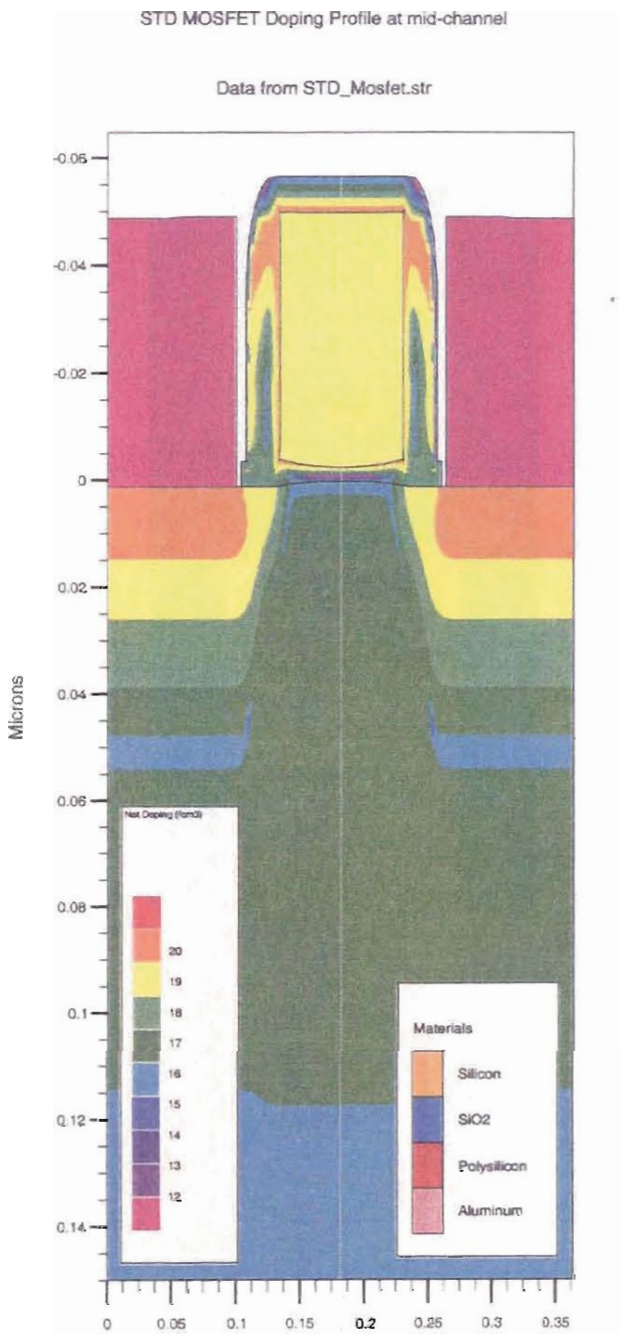
```
     etch oxide above p1.y=0.00

#    PLOT Gate_Et
#     structure outfile=15_Gate_Et.str
#tonyplot  15_Gate_Et.str
#_____________________________________________________

#SHOW COMPLETE DEVICE and assign electrodes

structure mirror right

electrode name=gate   x=0.3  y=0.0
electrode name=source x=0.2  y=0.0
electrode name=drain  x=0.4  y=0.0
electrode name=substrate backside

# plot the TMOS structure
structure outfile=TMOS.str
tonyplot  TMOS.str

#_____________________________________________________
```

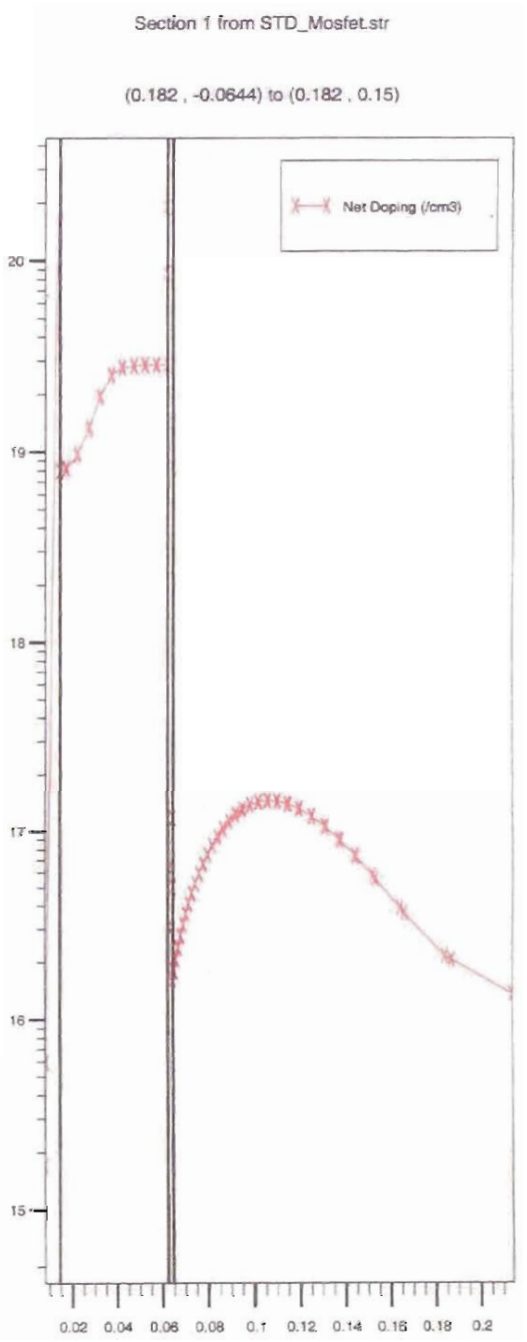
```
##############################################################
#                                                            #
#                     SIMULATE Id/Vgs                        #
#                                                            #
#                  (vgate=1.5, vdrain=1.5)                   #
#             Vt Test : Returns Vt, Beta and Theta           #
#                                                            #
##############################################################

go atlas

# set material models
models cvt srh print

contact name=gate tungsten
interface qf=1e10

method gummel newton
solve init

# Bias the drain
solve vdrain=0.1 outf=solve_tmp1
solve vdrain=1.5 outf=solve_tmp2
solve vdrain=2.0 outf=solve_tmp3
solve vdrain=2.5 outf=solve_tmp4


# Load in temporary files and Ramp the gate

load infile=solve_tmp1
log outf=TDIBL_01.log
solve vgate=0 vstep=0.15 vfinal=1.5 name=gate


load infile=solve_tmp2
log outf=TDIBL_15.log
solve vgate=0 vstep=0.15 vfinal=1.5 name=gate


load infile=solve_tmp3
log outf=TDIBL_20.log
solve vgate=0 vstep=0.15 vfinal=1.5 name=gate


load infile=solve_tmp4
log outf=TDIBL_25.log
solve vgate=0 vstep=0.15 vfinal=1.5 name=gate


# plot results
tonyplot  -overlay TDIBL_01.log  TDIBL_15.log TDIBL_20.log TDIBL_25.log

# extract device parameters
extract name="nvt" (xintercept(maxslope(curve(abs(v."gate"),abs(i."drain")))) \
```

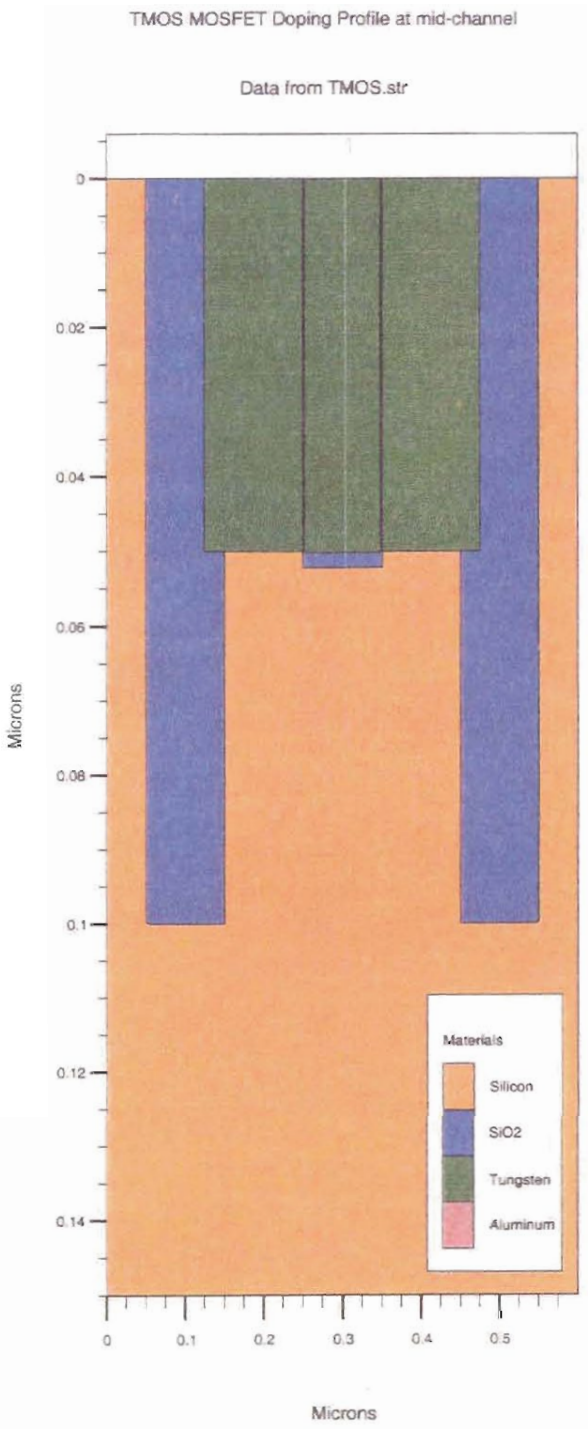
```
        - abs(ave(v."drain"))/2.0)
extract name="nbeta" slope(maxslope(curve(abs(v."gate"),abs(i."drain")))) \
        * (1.0/abs(ave(v."drain")))
extract name="ntheta" ((max(abs(v."drain")) * $"nbeta")/max(abs(i."drain"))) \
        - (1.0 / (max(abs(v."gate")) - ($"nvt")))

#_____________________________________________________

##############################################################
#                                                            #
#              SIMULATE Divice Field Contour                 #
#                                                            #
#                   (vgate=1.5, vdrain=1.5)                  #
#                                                            #
##############################################################

go atlas

# set material models
models cvt srh print

contact name=gate tungsten
interface qf=1e10

method gummel newton
solve init

# Bias the drain
solve vdrain=1.5
solve vgate=0
save outf=TMOS0.str
tonyplot TMOS0.str

# Ramp the gate
log outf=TMOS.log master
solve vgate=0 vstep=0.1 vfinal=1.5 name=gate
save outf=TMOS15.str
tonyplot TMOS15.str
#_____________________________________________________

##############################################################
#                                                            #
#    SIMULATE Sub-Threshold CURRENT, Max Gate Volts=0.3      #
#                                                            #
#         (SubVt Test : Returns PSubVt Parameter)            #
#                                                            #
##############################################################

go atlas

# set material models
models cvt srh print
contact name=tungsten
interface qf=1e10

# get initial solution

solve init

method  newton trap
```

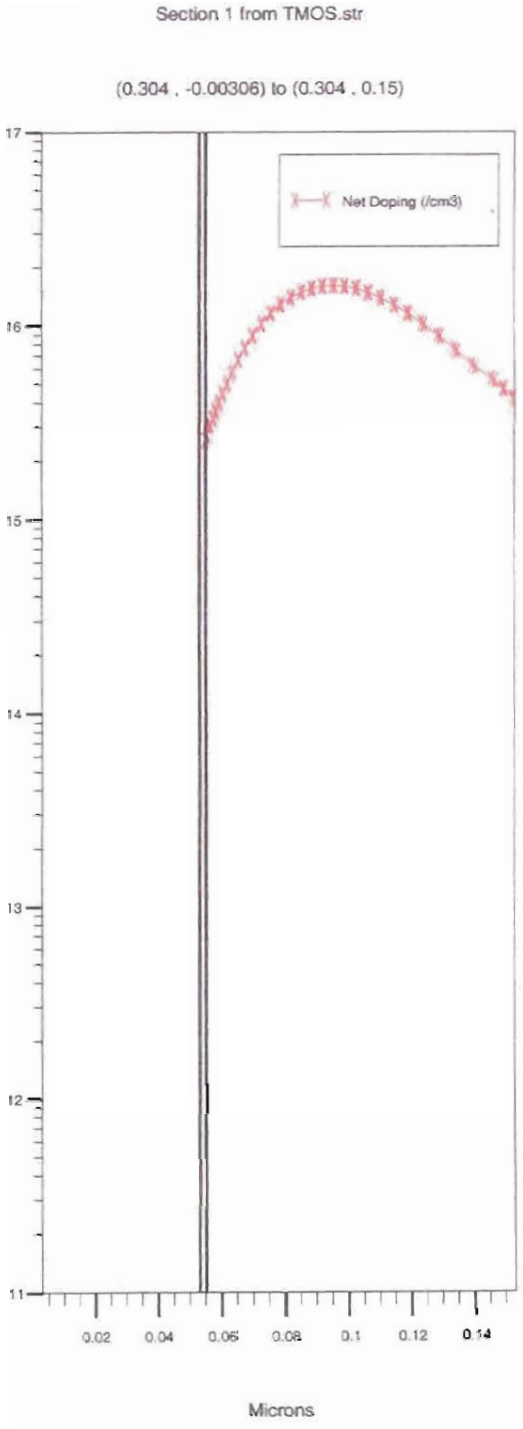
```
solve prev

# Bias the drain a bit...
solve vdrain=0.001 vstep=0.1 vfinal=1.5 name=drain
# Ramp the gate to a volt...
log outf=TMOS_Sub.log master
solve vgate=0 vstep=0.1 vfinal=1.5 name=gate


# extract the device parameter SubVt...
extract init inf="TMOS_Sub.log"
extract name="npubvt" 1.0/slope(maxslope(curve(abs(v."gate"),log10(abs(i."drain")))))

tonyplot TMOS_Sub.log

#_____


##############################################################
#                                                            #
#    SIMULATE DRAIN CURRENT AT 0.5, 1.0 and 1.5 VOLTS.       #
#                                                            #
#  (Id curve simulation as shown in Example: mos1ex09.in)    #
#                                                            #
##############################################################

go atlas2

# define the Gate workfunction
contact name=gate tungsten

# Define the Gate Qss
interface qf=1e10

# Use the cvt mobility model for MOS
models cvt srh

# set gate biases with Vds=0.0
solve init
solve vgate=.5 outf=solve_tmp1
solve vgate=1.0 outf=solve_tmp2
solve vgate=1.5 outf=solve_tmp3

#load in temporary files and ramp Vds

load infile=solve_tmp1
log outf=TMOS_Id_1.log
solve name=drain vdrain=0 vfinal=1.5 vstep=0.1

load infile=solve_tmp2
log outf=TMOS_Id_2.log
solve name=drain vdrain=0 vfinal=1.5 vstep=0.1

load infile=solve_tmp3
log outf=TMOS_Id_3.log
solve name=drain vdrain=0 vfinal=1.5 vstep=0.1

# extract max current and saturation slope
```

Appendix C. Typical Doping Profiles

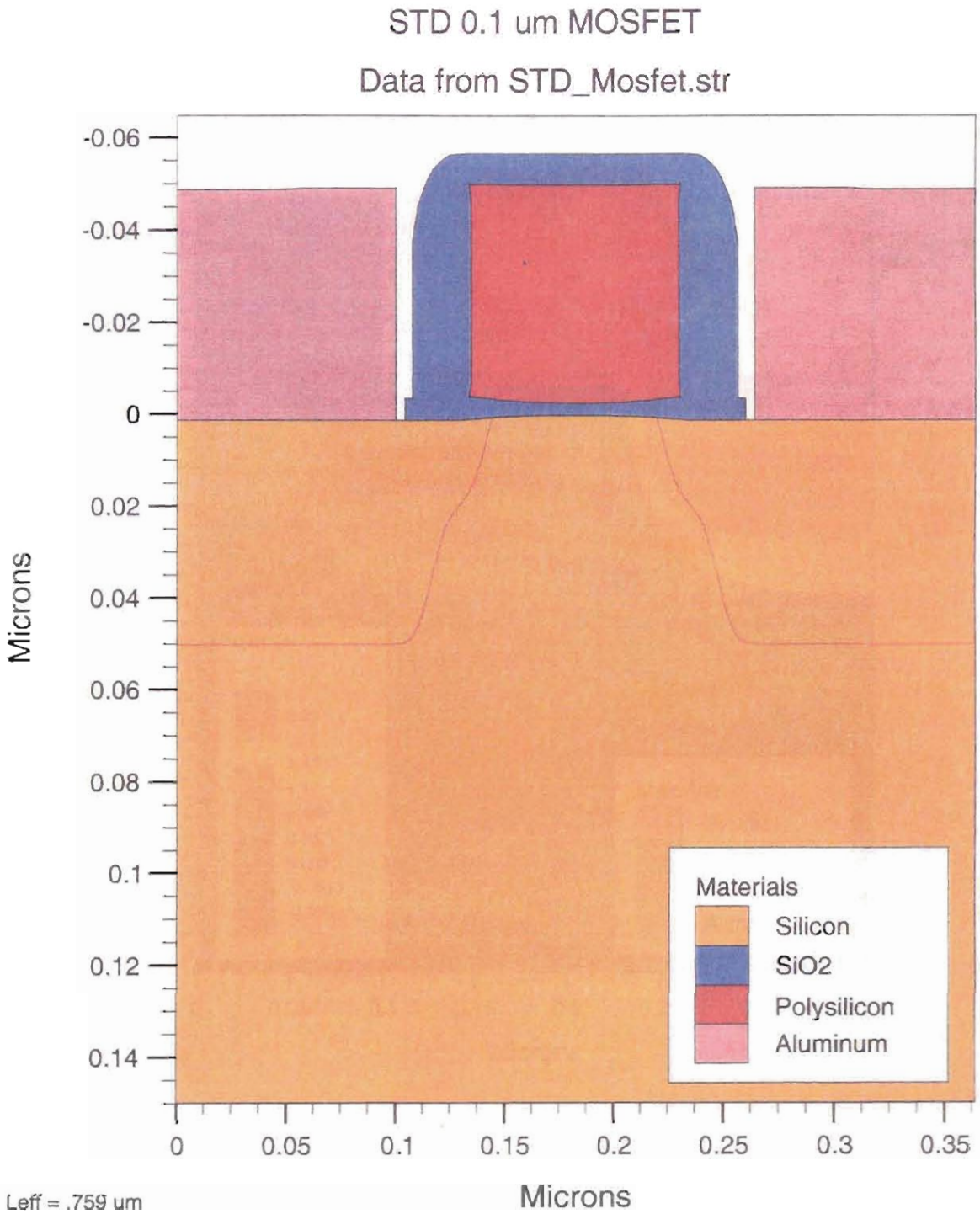

STD MOSFET Doping Profile at mid-channel
Data from STD_Mosfet.str
Microns
Microns
Net Doping (/cm3)
20
19
18
17
16
15
14
13
12
Materials
Silicon
SiO2
Polysilicon
Aluminum

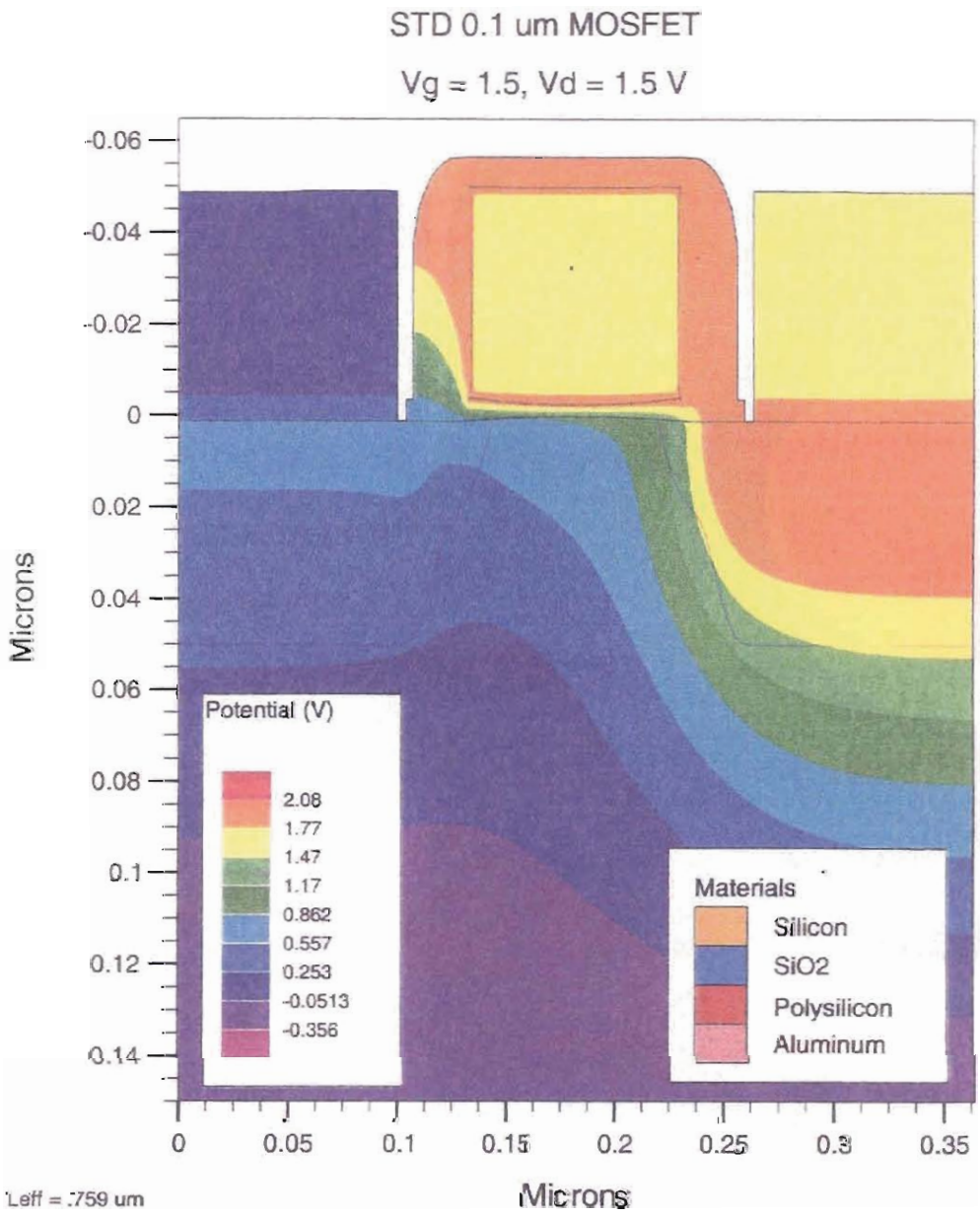

Section 1 from STD_Mosfet.str
(0.182 , -0.0644) to (0.182 , 0.15)
Net Doping (/cm3)
Microns

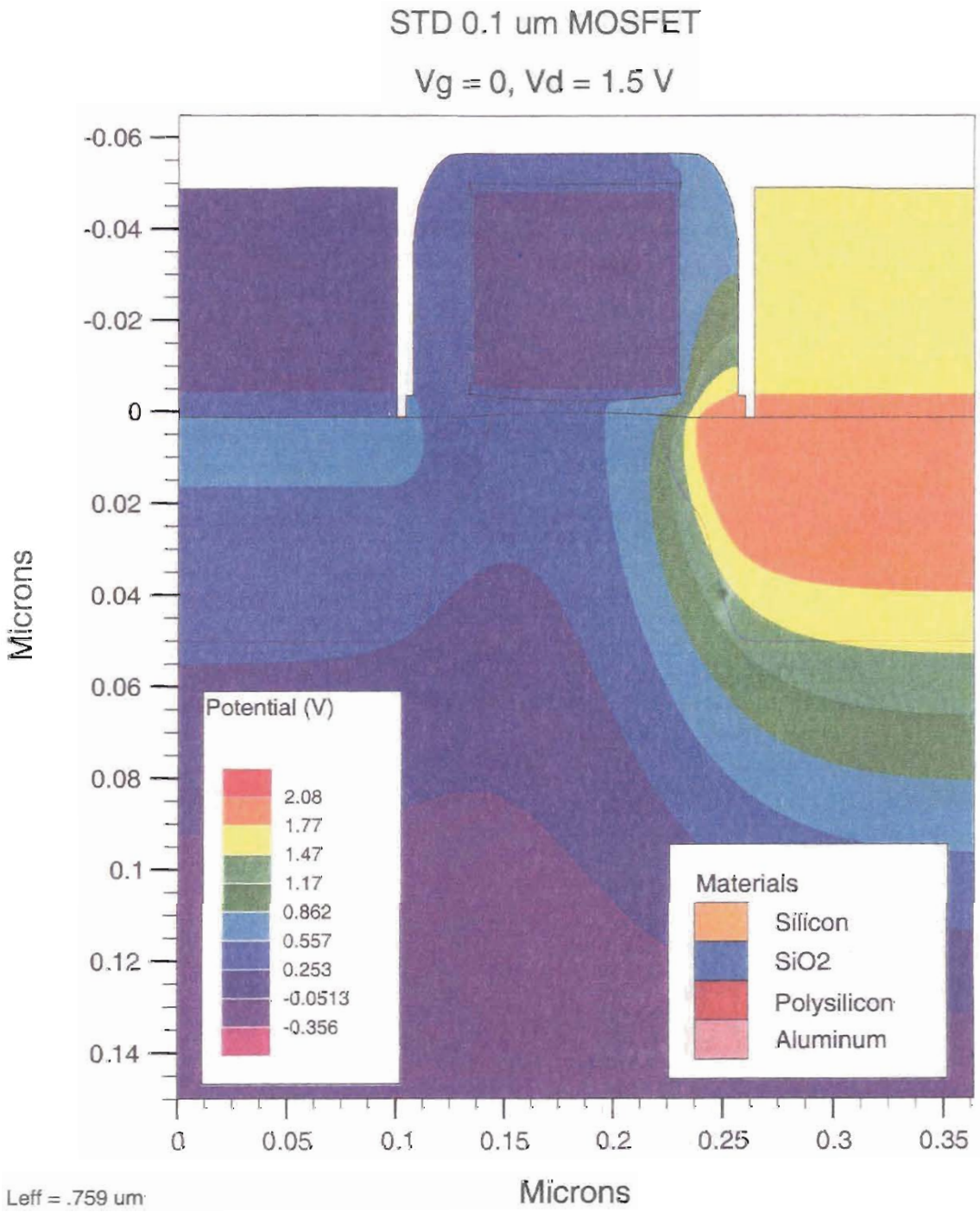

TMOS MOSFET Doping Profile at mid-channel
Data from TMOS.str
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0
0.1
0.2
0.3
0.4
0.5
Microns
Materials
Silicon
SiO2
Tungsten
Aluminum

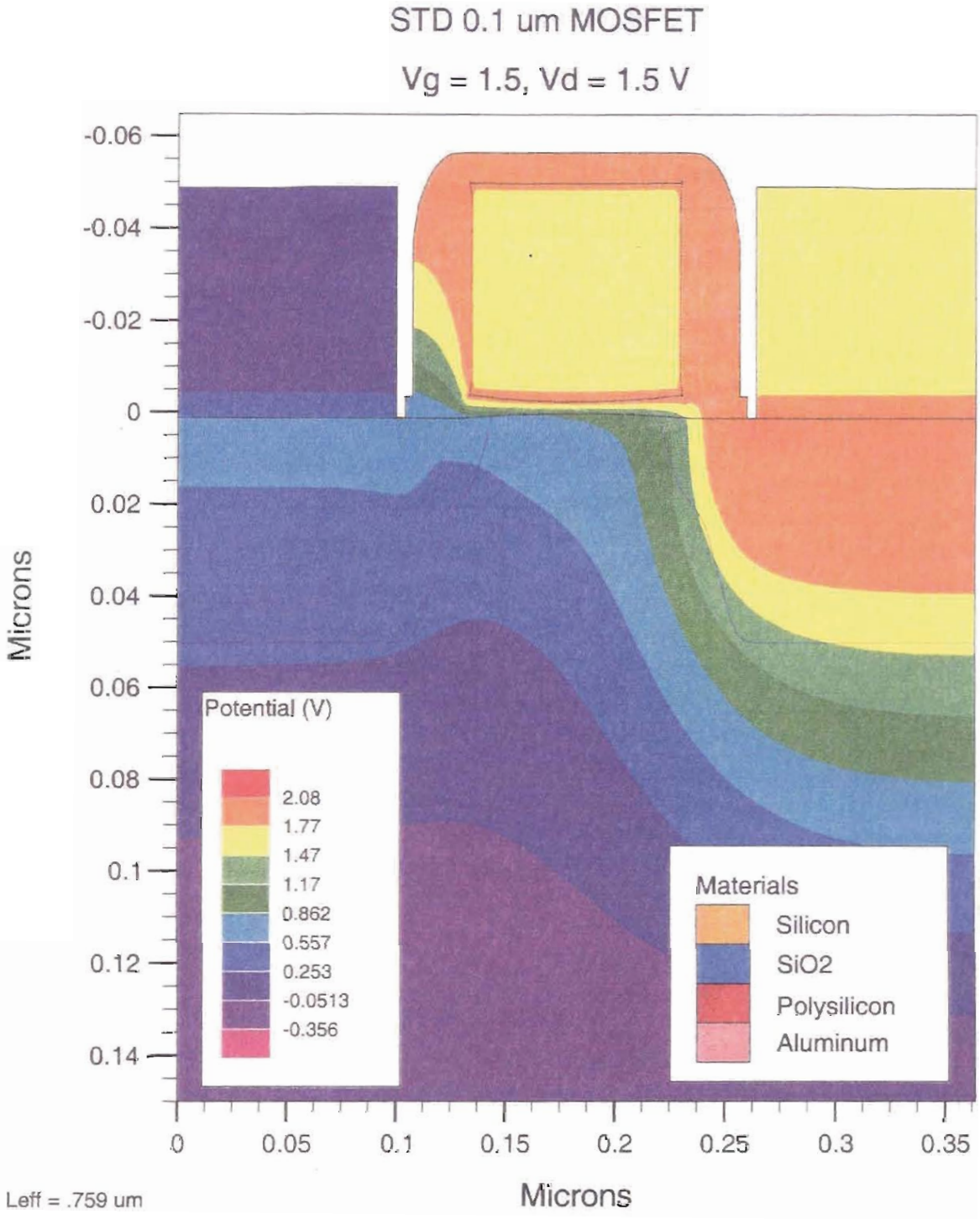

Section 1 from TMOS.str
(0.304 , -0.00306) to (0.304 , 0.15)
Net Doping (/cm3)
17
16
15
14
13
12
11
0.02
0.04
0.06
0.08
0.1
0.12
0.14
Microns

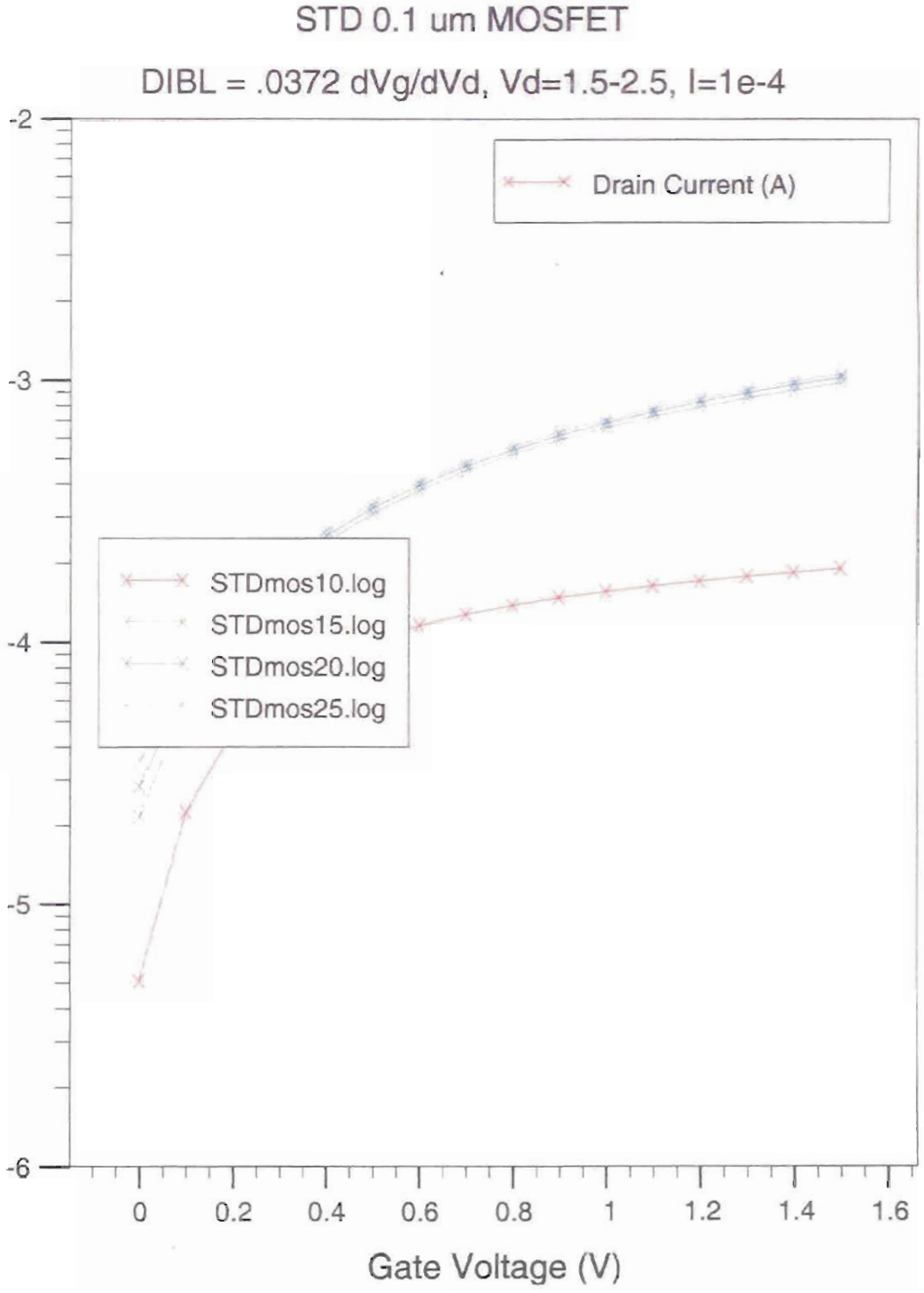
Appendix D. STD 0.1um MOSFET

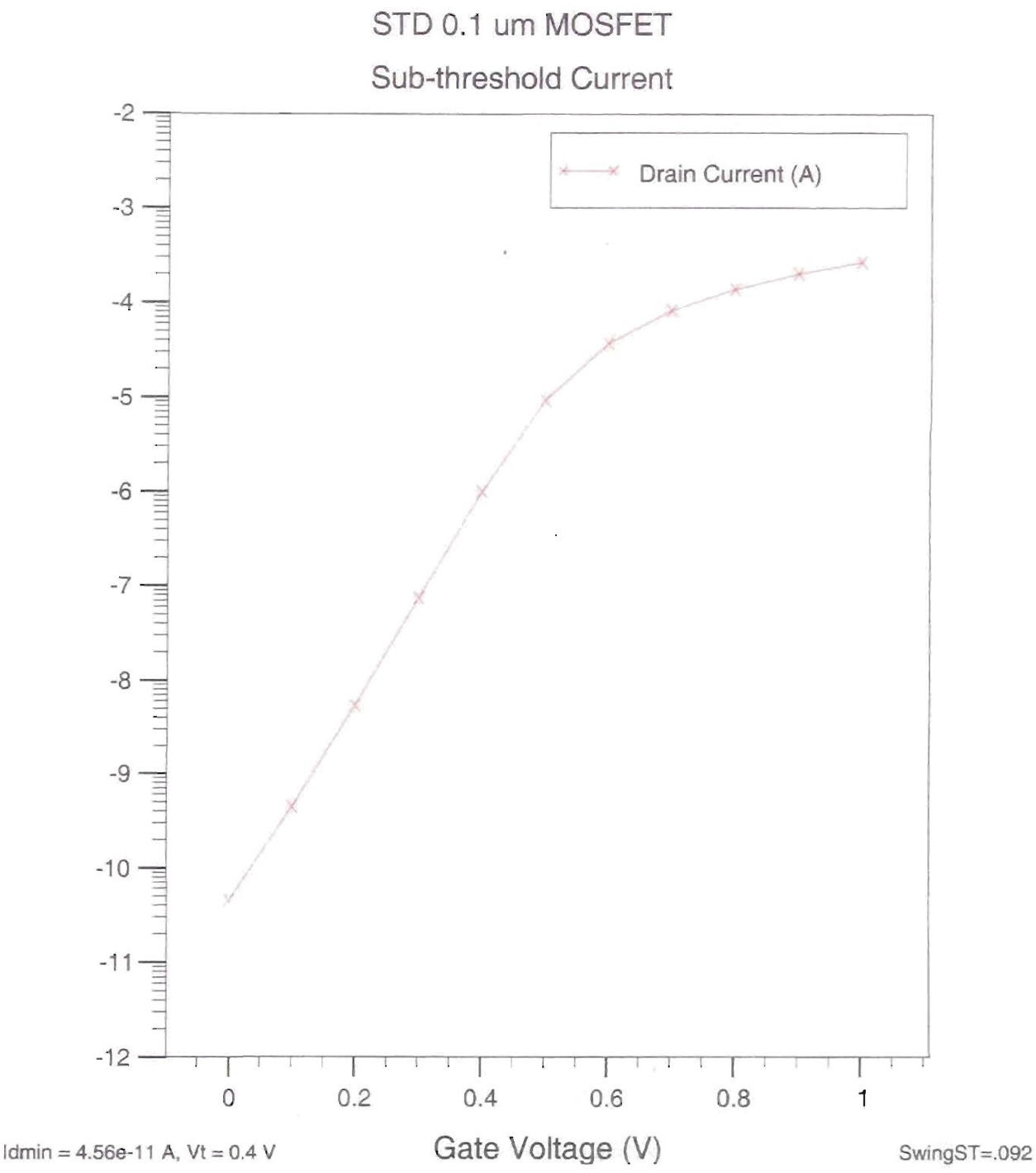

STD 0.1 um MOSFET
Data from STD_Mosfet.str
-0.06
-0.04
-0.02
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
Microns
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
Microns
Materials
Silicon
SiO2
Polysilicon
Aluminum
Leff = .759 um

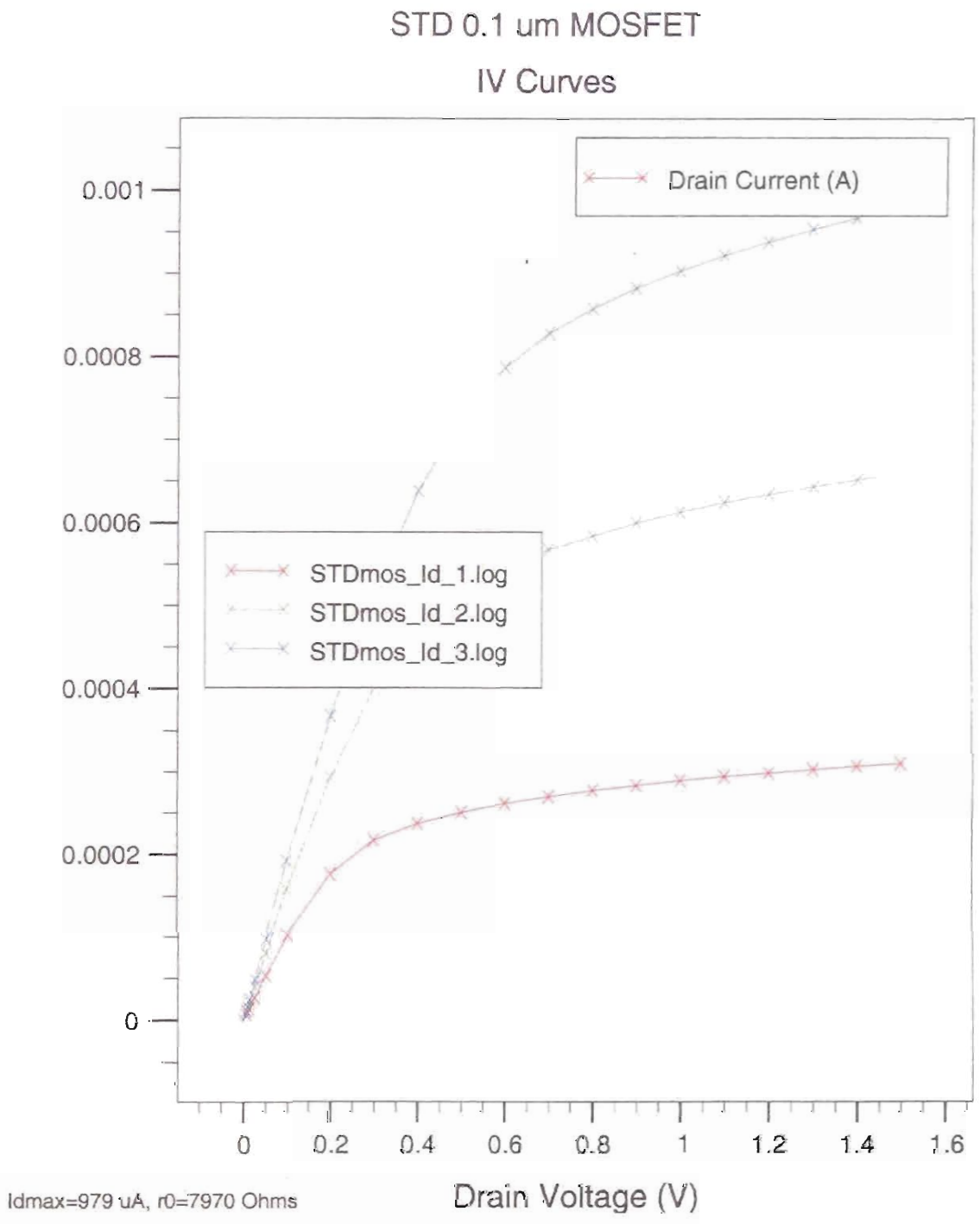

STD 0.1 um MOSFET
Vg = 1.5, Vd = 1.5 V
-0.06
-0.04
-0.02
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
Microns
Potential (V)
2.08
1.77
1.47
1.17
0.862
0.557
0.253
-0.0513
-0.356
Materials
Silicon
SiO2
Polysilicon
Aluminum
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
Microns
Leff = .759 um


STD 0.1 um MOSFET
Vg = 0, Vd = 1.5 V
-0.06
-0.04
-0.02
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
Microns
Potential (V)
2.08
1.77
1.47
1.17
0.862
0.557
0.253
-0.0513
-0.356
Materials
Silicon
SiO2
Polysilicon
Aluminum
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
Microns
Leff = .759 um

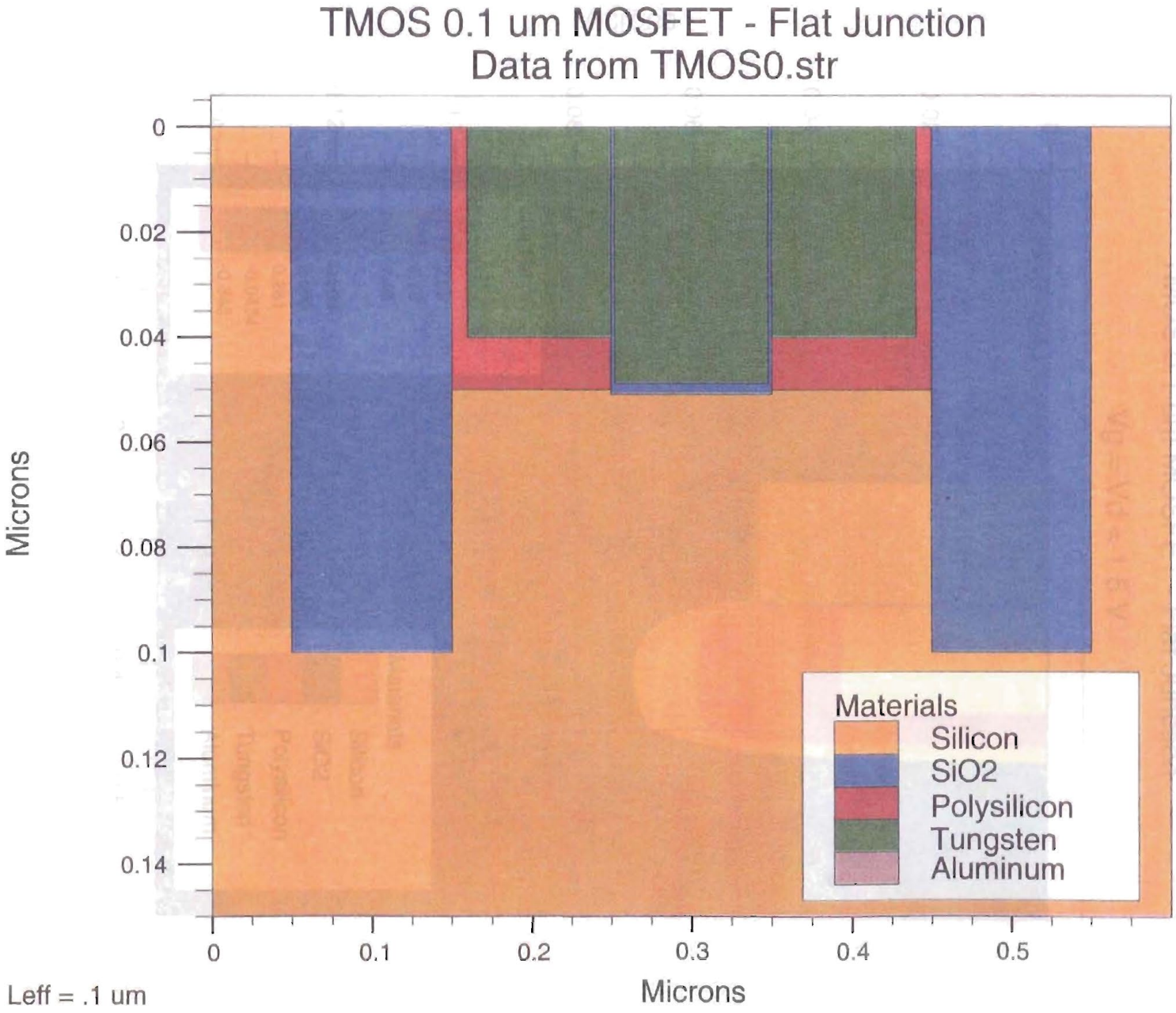

STD 0.1 um MOSFET
Vg = 1.5, Vd = 1.5 V
-0.06
-0.04
-0.02
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
Microns
Potential (V)
2.08
1.77
1.47
1.17
0.862
0.557
0.253
-0.0513
-0.356
Materials
Silicon
SiO2
Polysilicon
Aluminum
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
Microns
Leff = .759 um

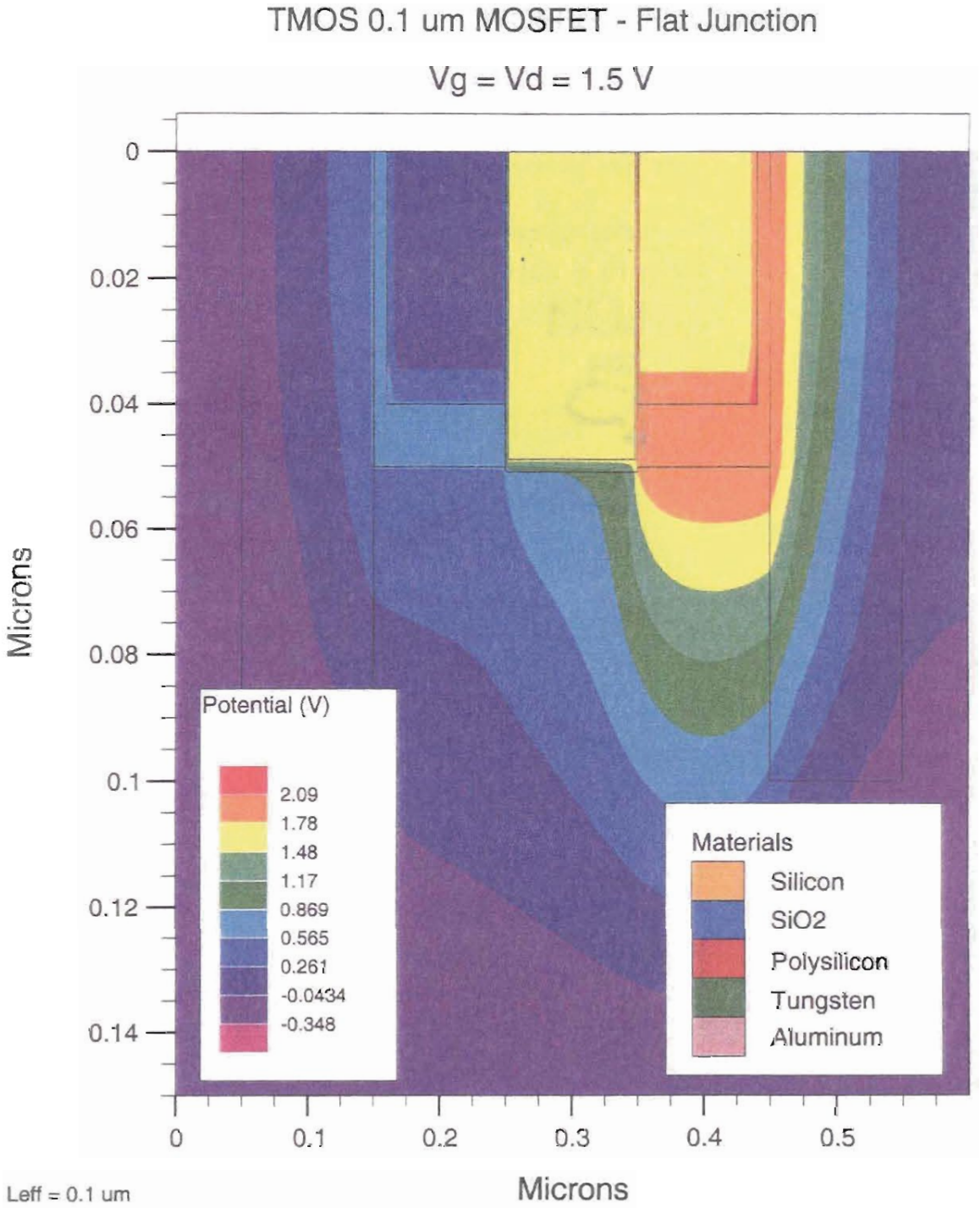

STD 0.1 um MOSFET
DIBL = .0372 dVg/dVd, Vd=1.5-2.5, I=1e-4
Drain Current (A)
STDmos10.log
STDmos15.log
STDmos20.log
STDmos25.log
-2
-3
-4
-5
-6
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Gate Voltage (V)

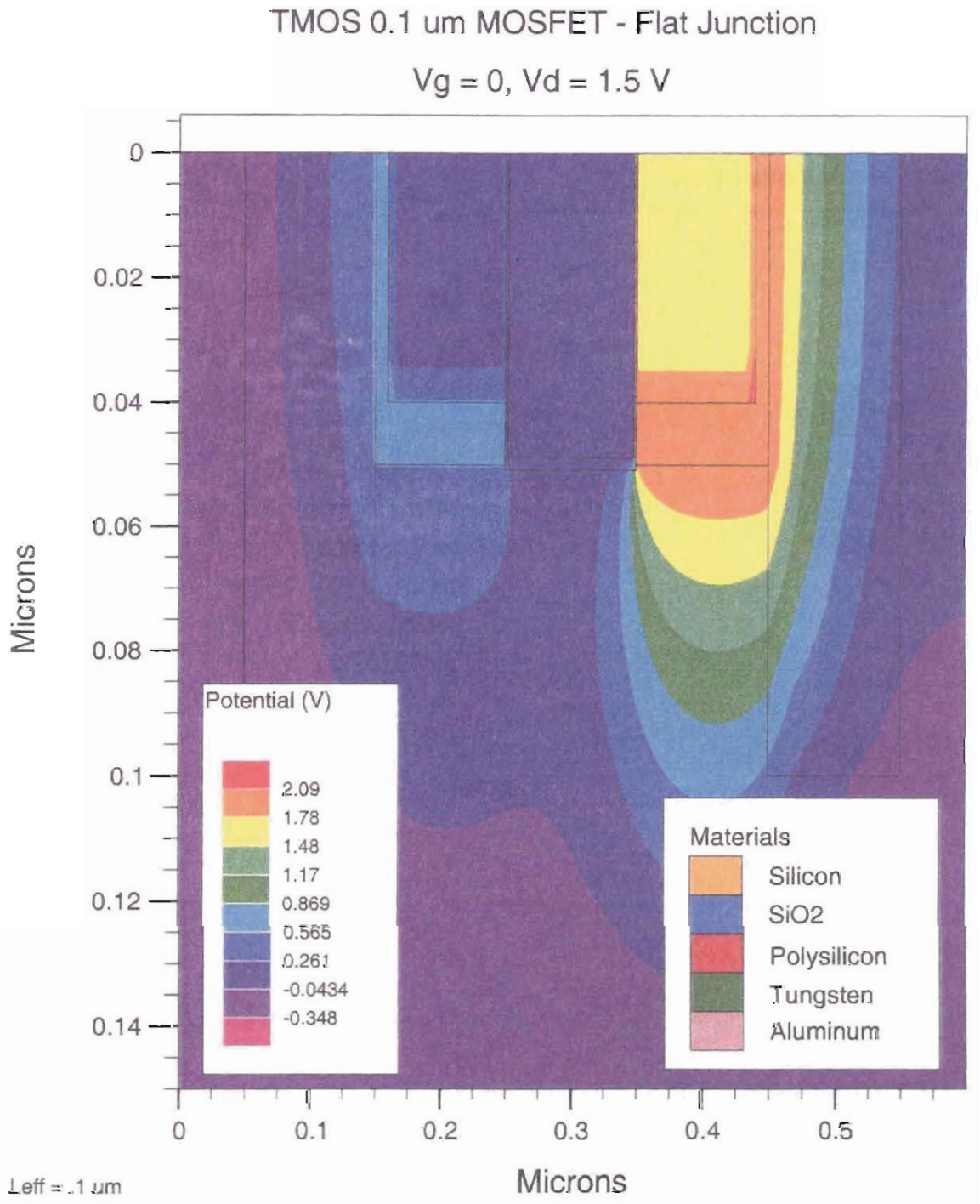

STD 0.1 um MOSFET
Sub-threshold Current
Drain Current (A)
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
0
0.2
0.4
0.6
0.8
1
Gate Voltage (V)
Idmin = 4.56e-11 A, Vt = 0.4 V
SwingST=.092

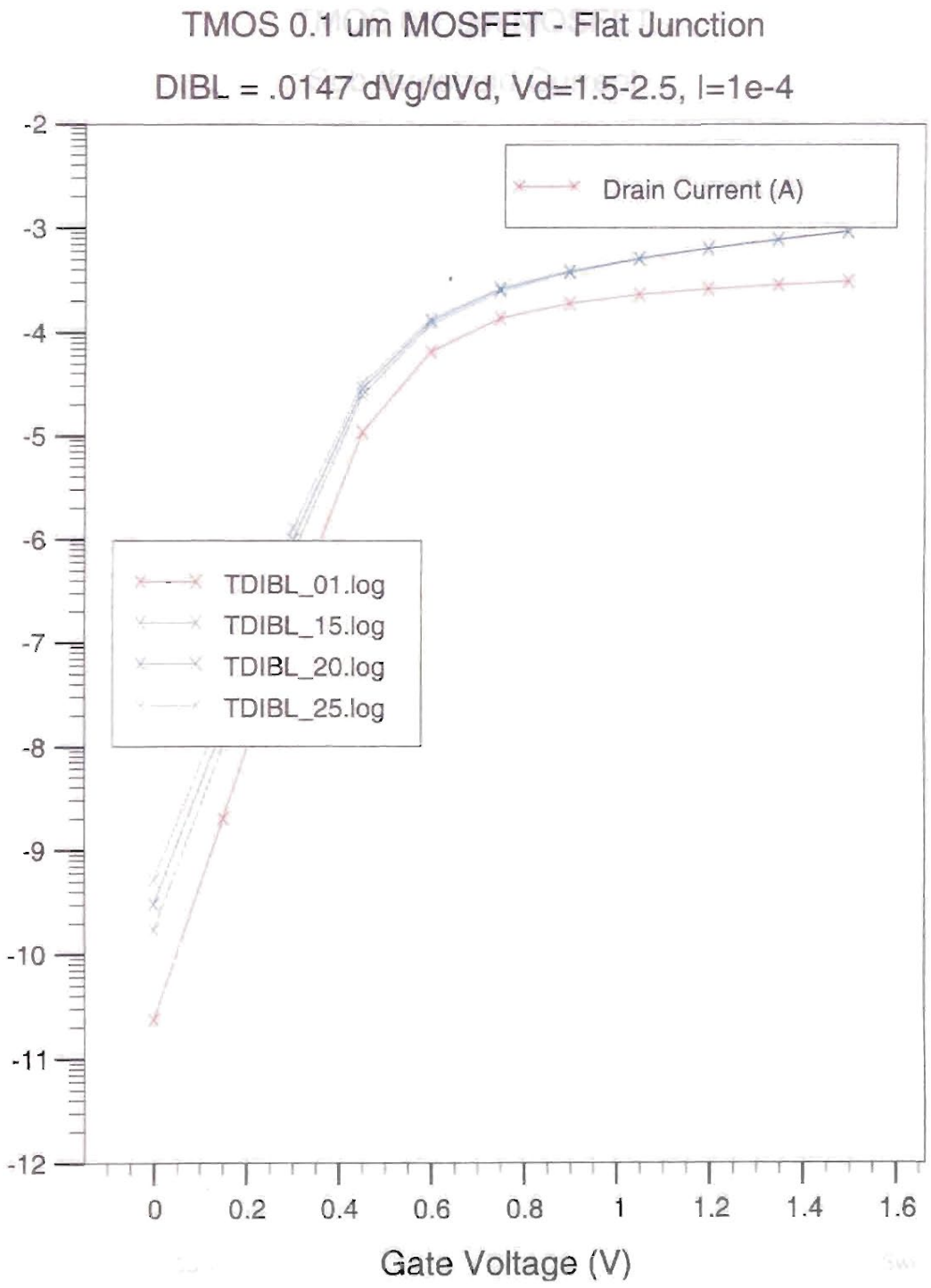

STD 0.1 um MOSFET
IV Curves
Drain Current (A)
STDmos_Id_1.log
STDmos_Id_2.log
STDmos_Id_3.log
0.001
0.0008
0.0006
0.0004
0.0002
0
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Idmax=979 uA, r0=7970 Ohms
Drain Voltage (V)

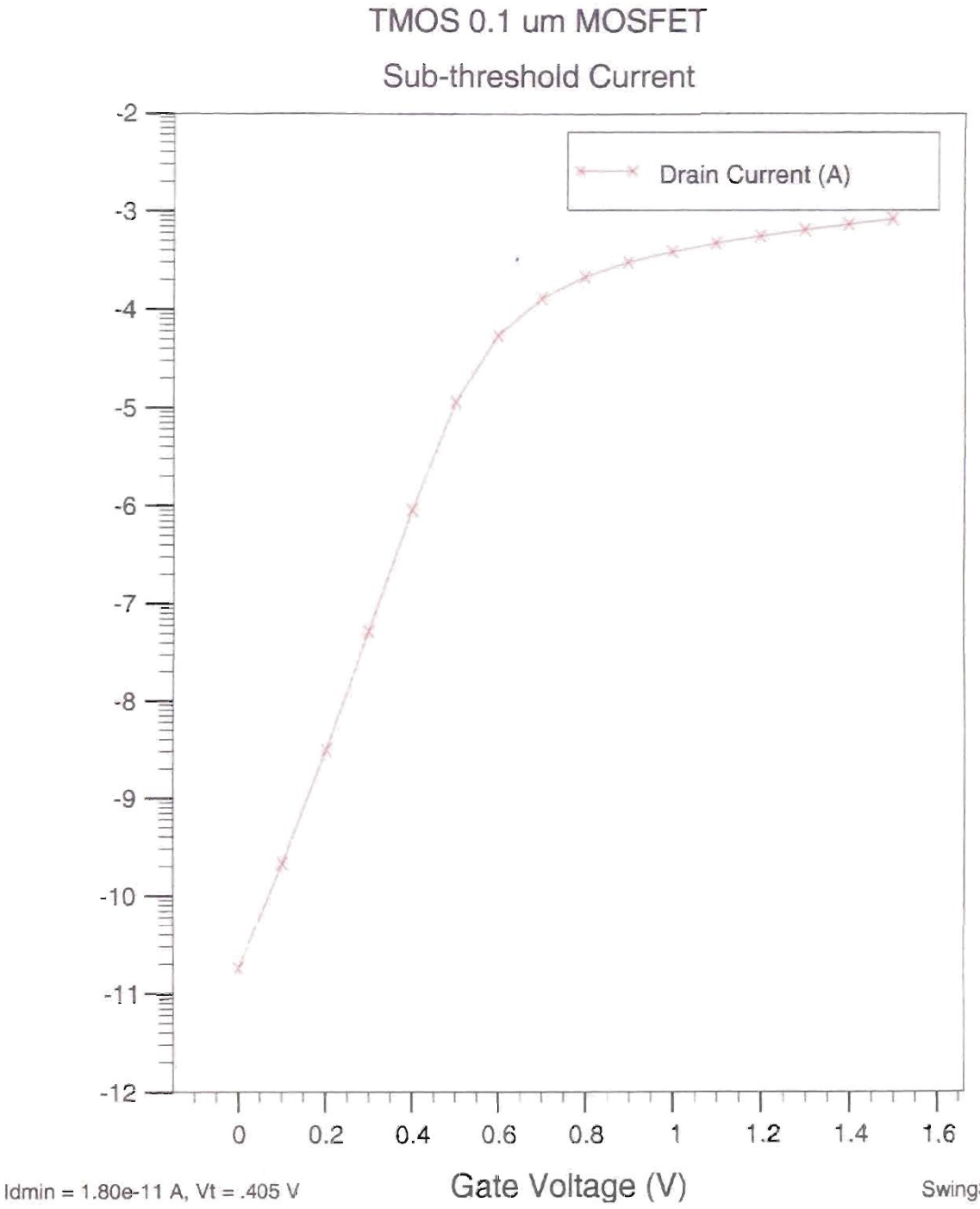
Appendix E. TMOS 0.1 um MOSFET - Flat Junction

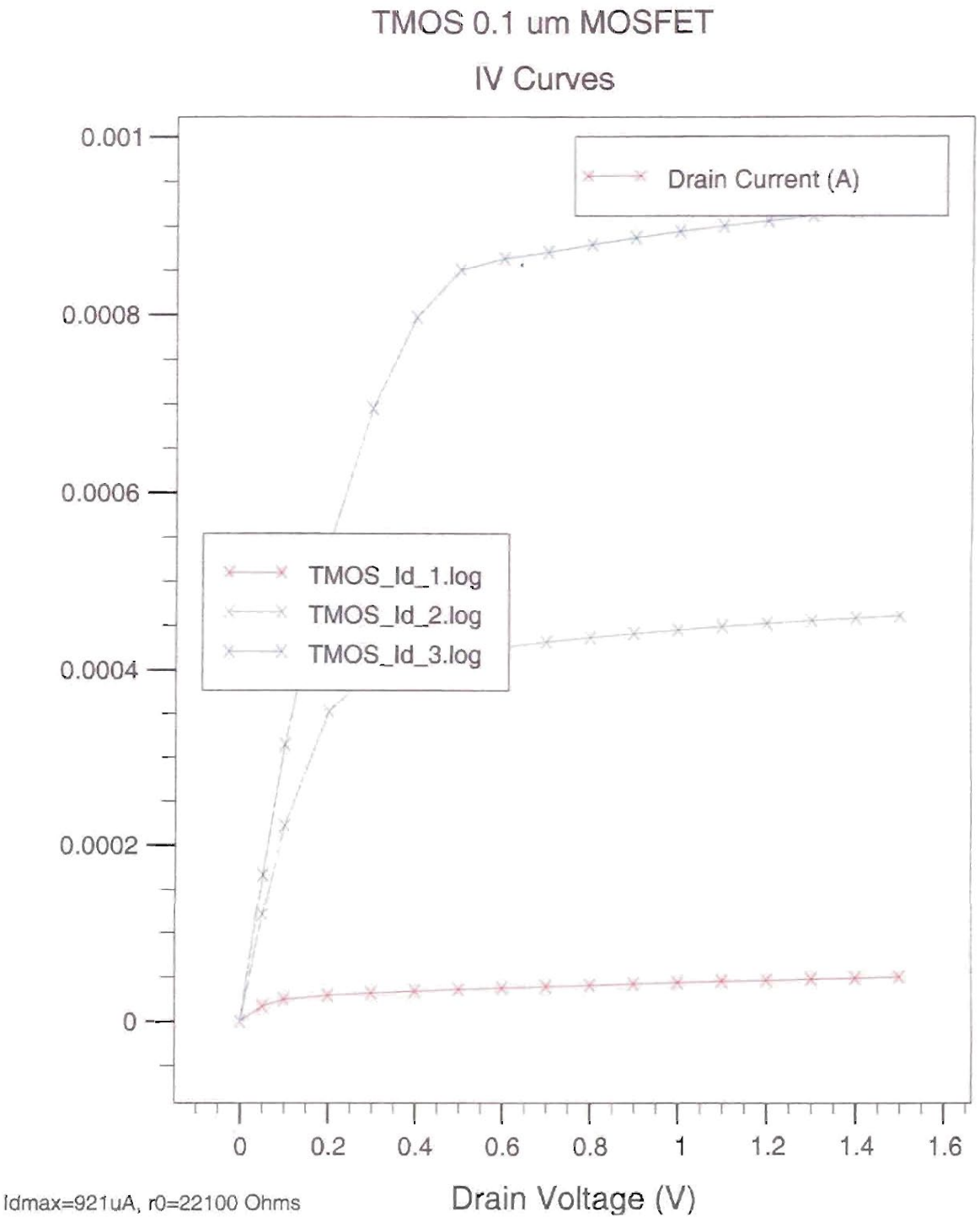

TMOS 0.1 um MOSFET - Flat Junction
Data from TMOS0.str
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0
0.1
0.2
0.3
0.4
0.5
Microns
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum
Leff = .1 um


TMOS 0.1 um MOSFET - Flat Junction
Vg = Vd = 1.5 V
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
Potential (V)
2.09
1.78
1.48
1.17
0.869
0.565
0.261
-0.0434
-0.348
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum
0
0.1
0.2
0.3
0.4
0.5
Microns
Leff = 0.1 um

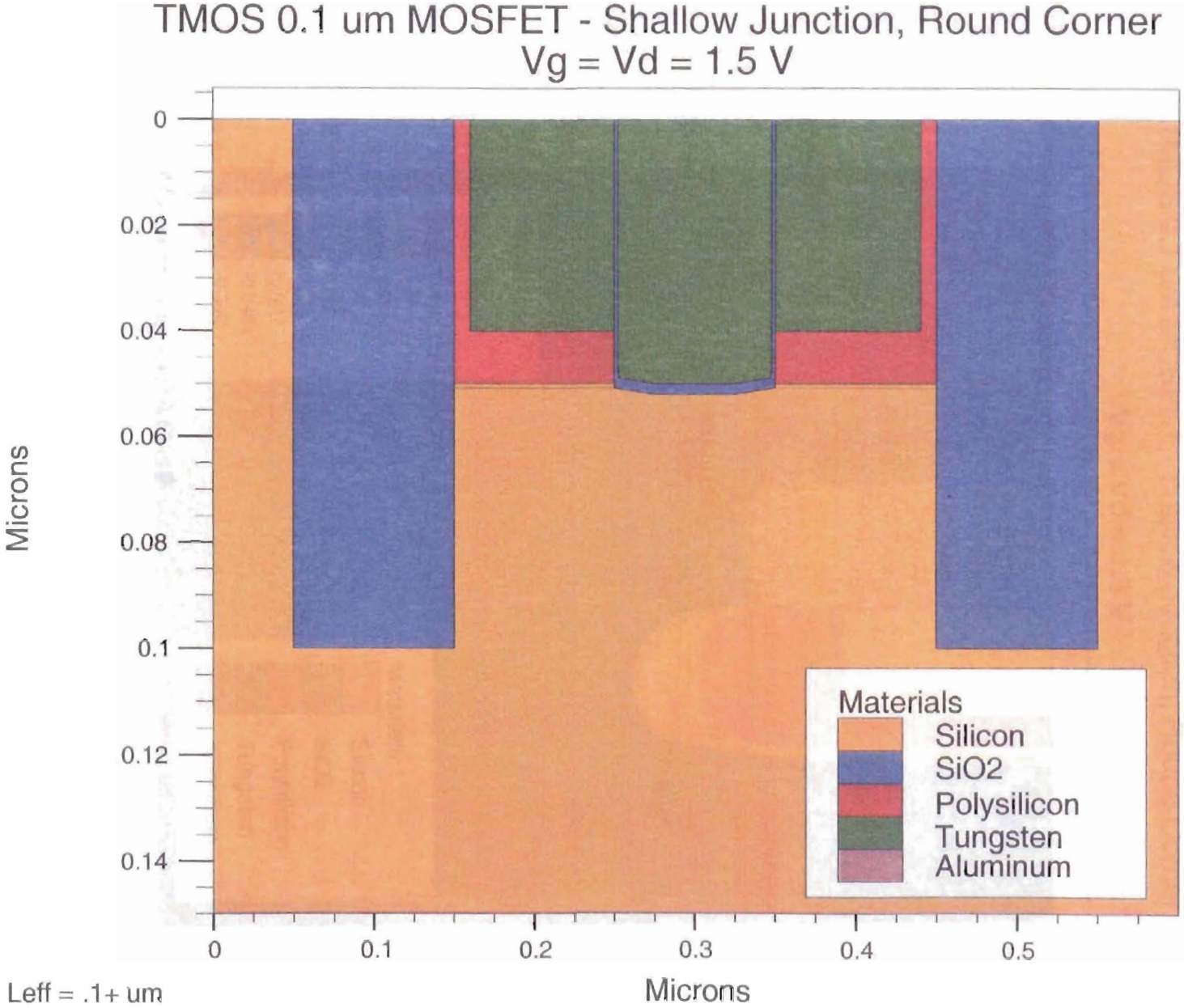

TMOS 0.1 um MOSFET - Flat Junction
Vg = 0, Vd = 1.5 V
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0
0.1
0.2
0.3
0.4
0.5
Microns
Potential (V)
2.09
1.78
1.48
1.17
0.869
0.565
0.261
-0.0434
-0.348
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum
Leff = .1 um

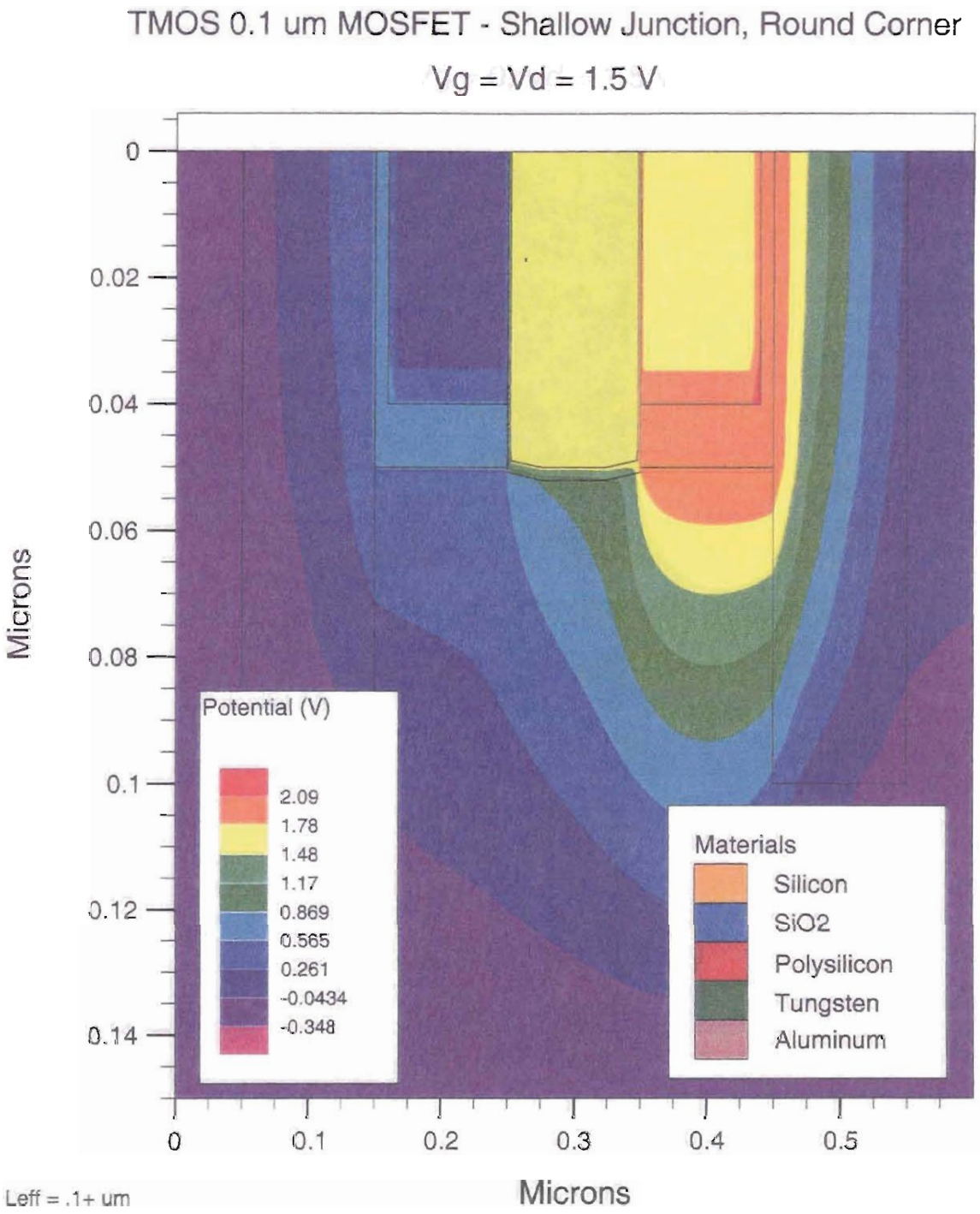

TMOS 0.1 um MOSFET - Flat Junction
DIBL = .0147 dVg/dVd, Vd=1.5-2.5, I=1e-4
Drain Current (A)
TDIBL_01.log
TDIBL_15.log
TDIBL_20.log
TDIBL_25.log
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Gate Voltage (V)

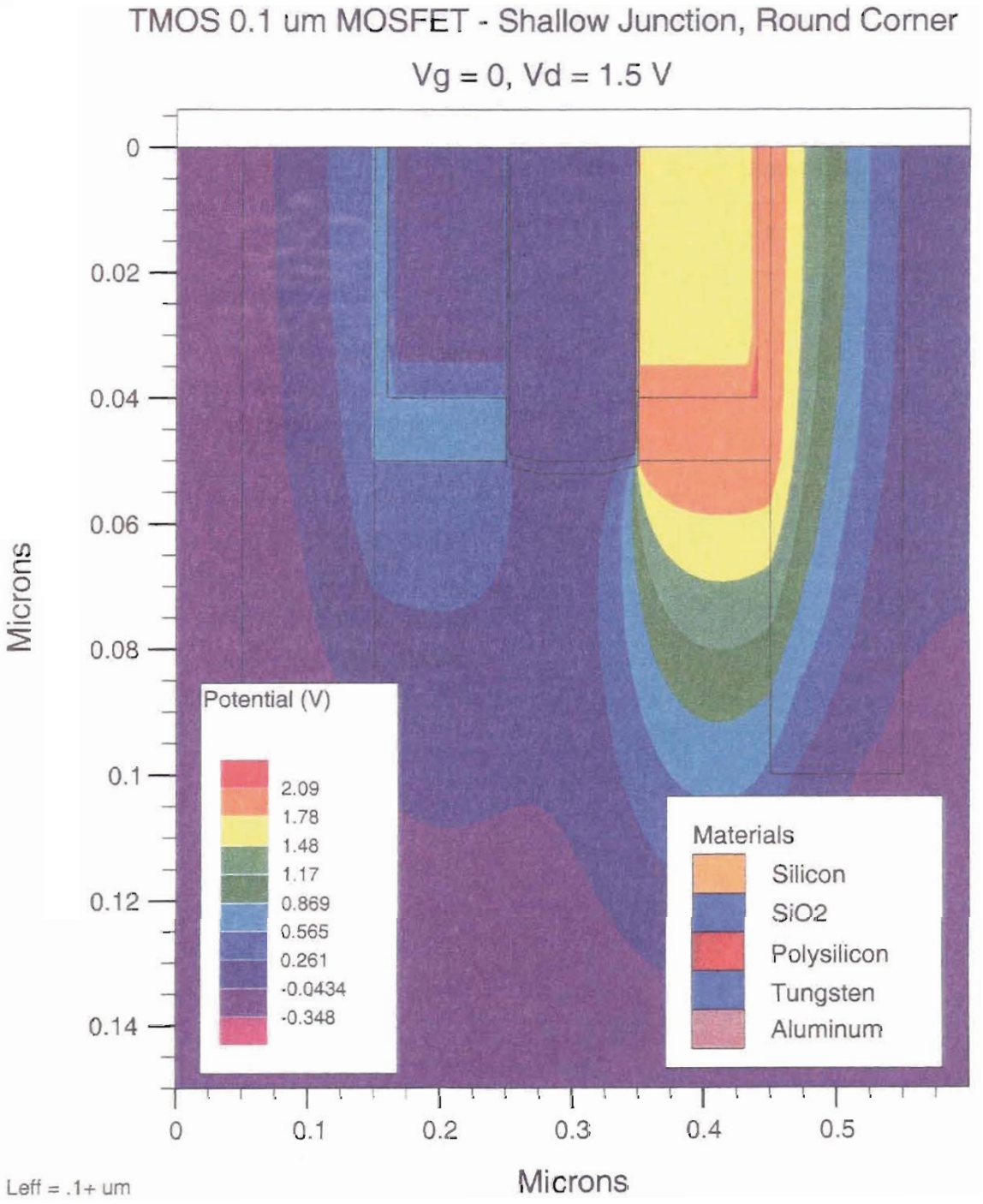

TMOS 0.1 um MOSFET
Sub-threshold Current
Drain Current (A)
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Gate Voltage (V)
Idmin = 1.80e-11 A, Vt = .405 V
SwingST = .085

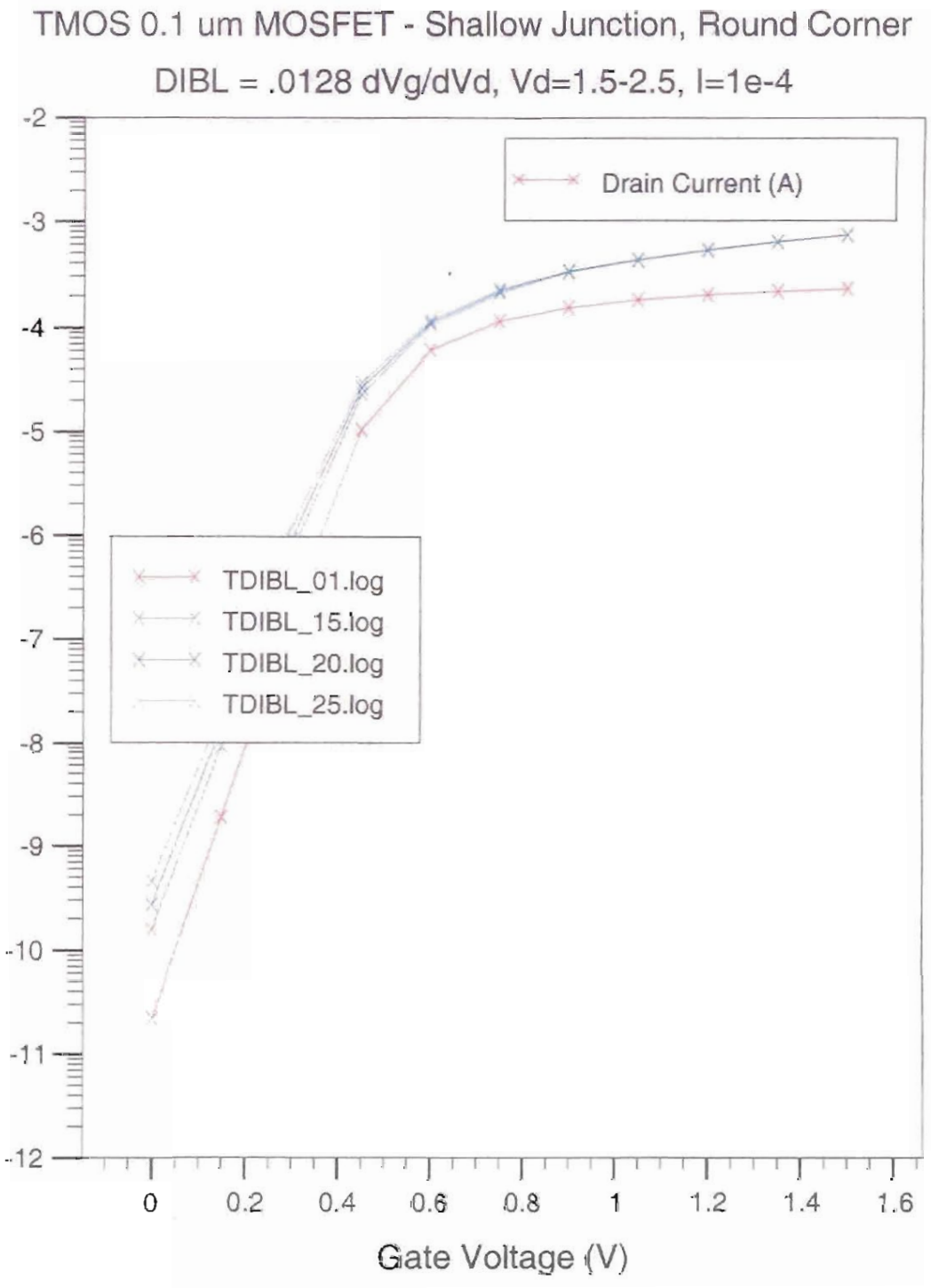

TMOS 0.1 um MOSFET
IV Curves
0.001
0.0008
0.0006
0.0004
0.0002
0
Drain Current (A)
TMOS_Id_1.log
TMOS_Id_2.log
TMOS_Id_3.log
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Drain Voltage (V)
Idmax=921uA, r0=22100 Ohms

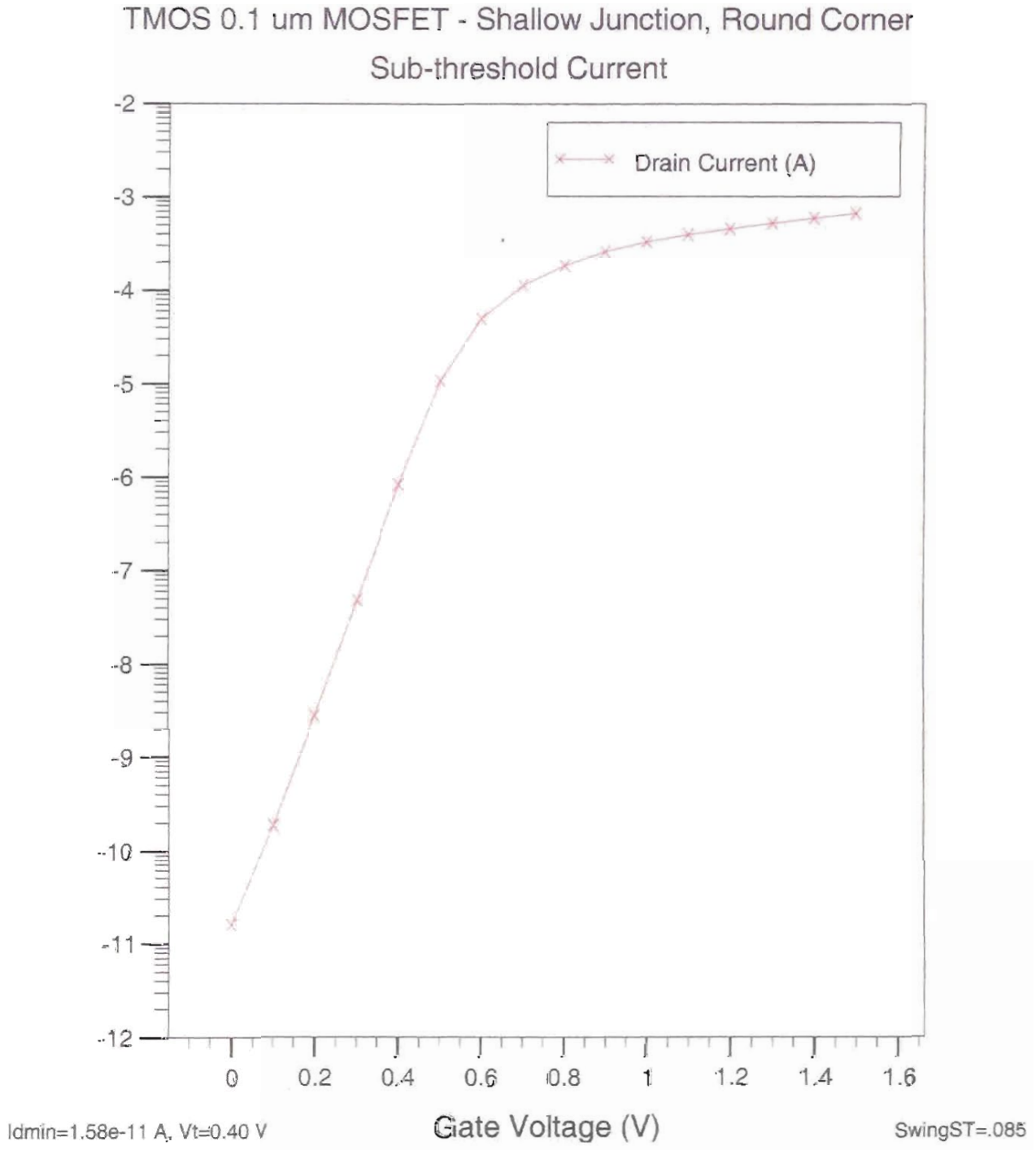
Appendix F. TMOS 0.1 um MOSFET - Shallow Junction, Round Corner

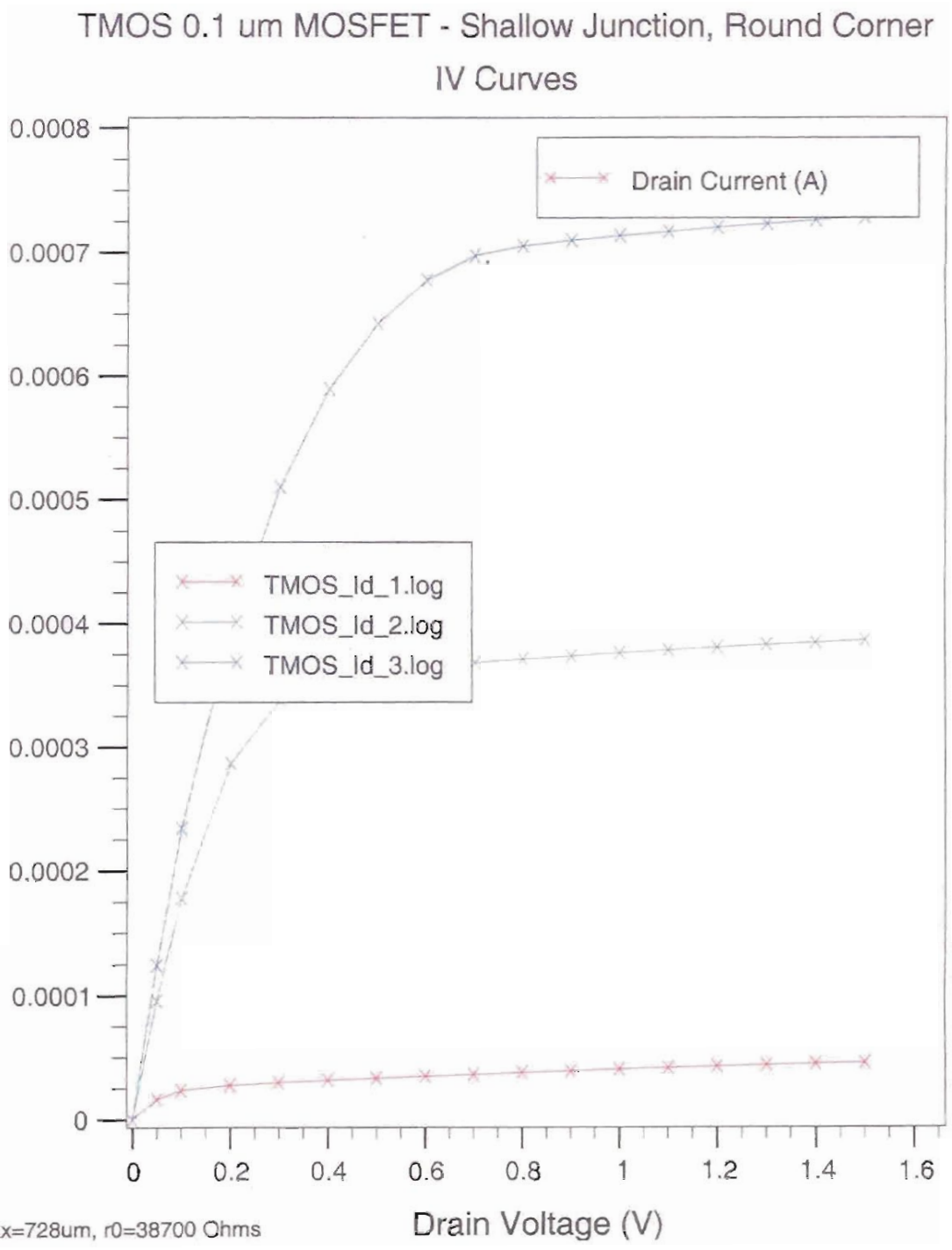

TMOS 0.1 um MOSFET - Shallow Junction, Round Corner
Vg = Vd = 1.5 V
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0
0.1
0.2
0.3
0.4
0.5
Microns
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum
Leff = .1+ um


TMOS 0.1 um MOSFET - Shallow Junction, Round Corner
Vg = Vd = 1.5 V
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
Potential (V)
2.09
1.78
1.48
1.17
0.869
0.565
0.261
-0.0434
-0.348
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum
0
0.1
0.2
0.3
0.4
0.5
Microns
Leff = .1+ um

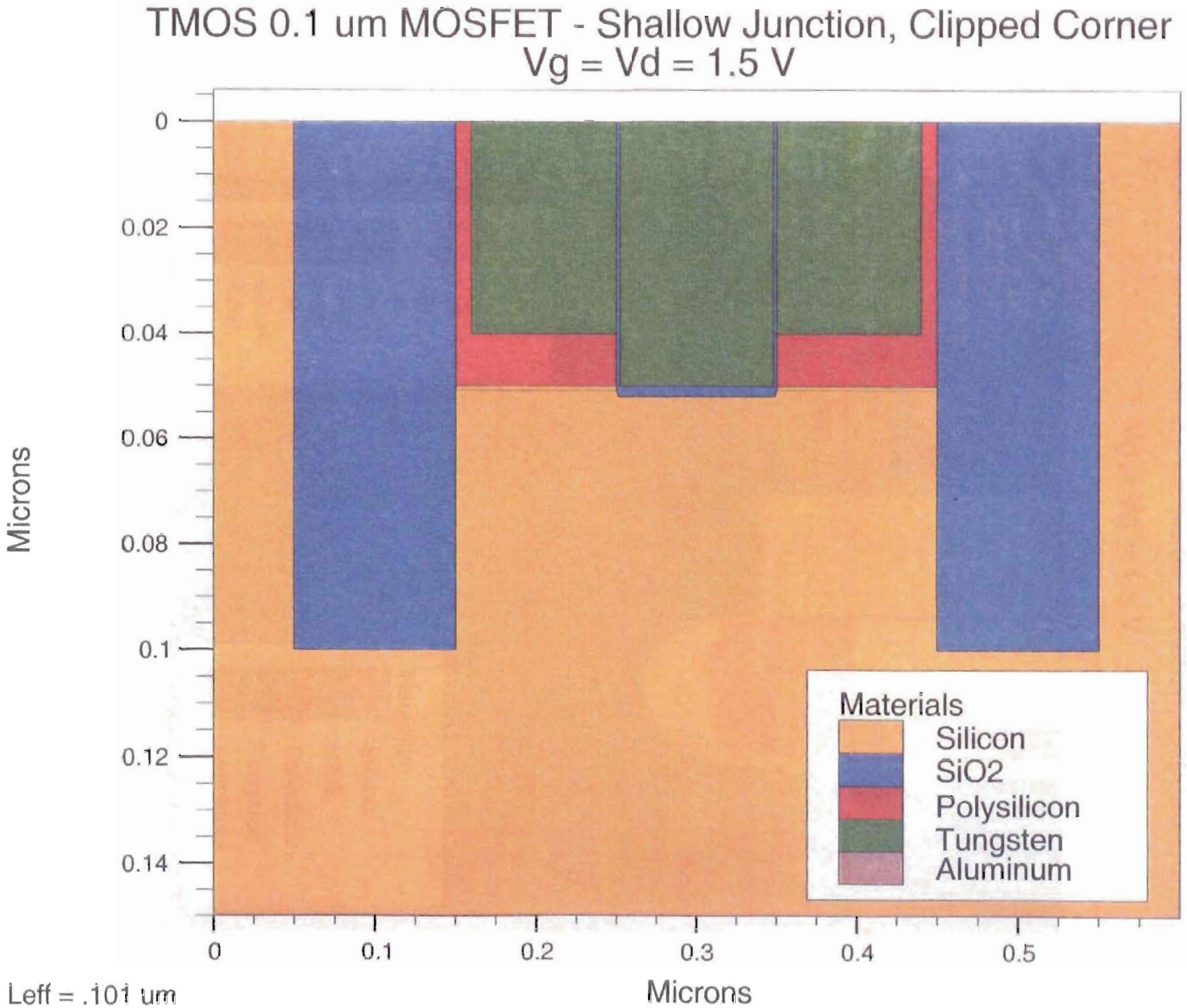

TMOS 0.1 um MOSFET - Shallow Junction, Round Corner
Vg = 0, Vd = 1.5 V
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0
0.1
0.2
0.3
0.4
0.5
Microns
Potential (V)
2.09
1.78
1.48
1.17
0.869
0.565
0.261
-0.0434
-0.348
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum
Leff = .1+ um

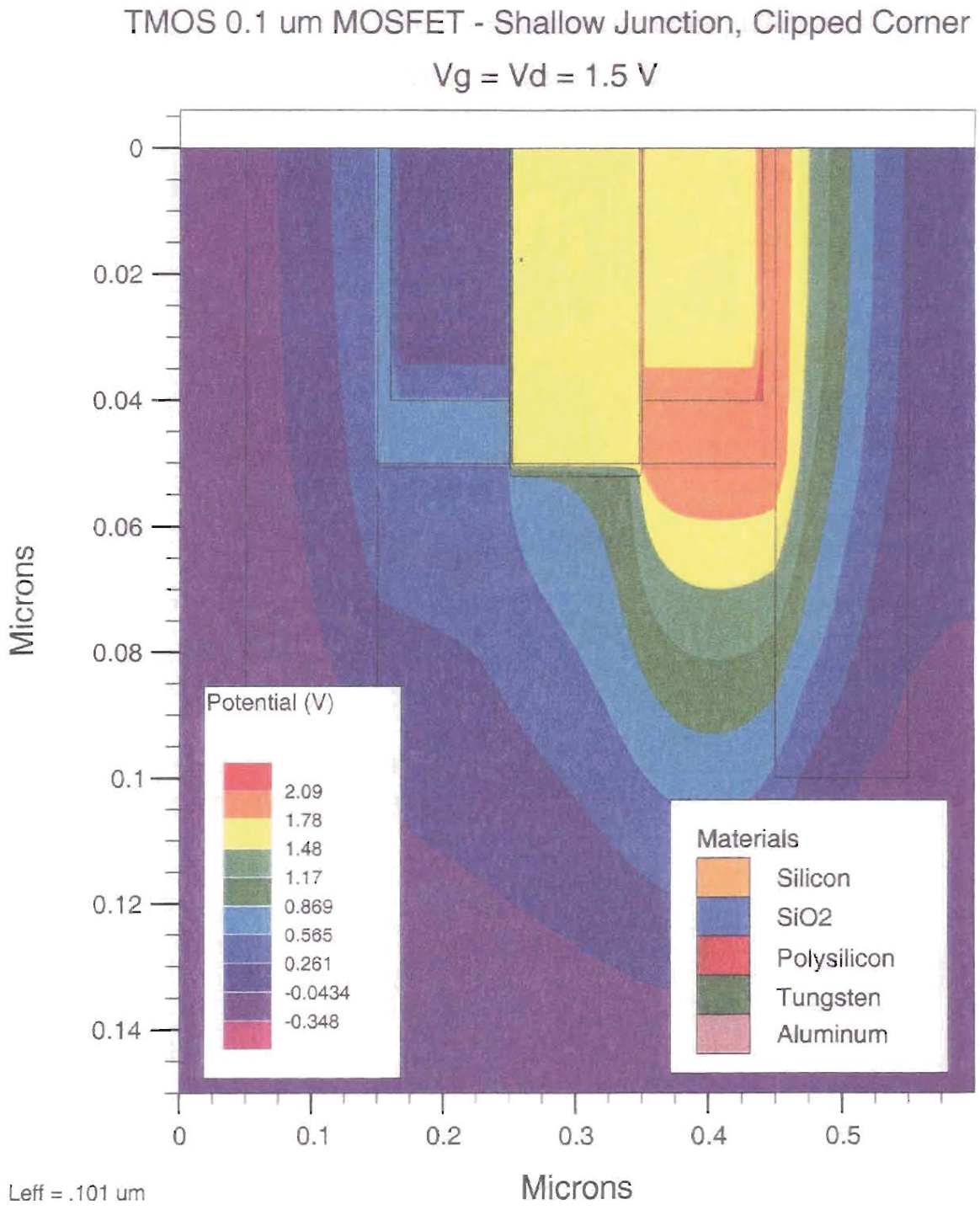

TMOS 0.1 um MOSFET - Shallow Junction, Round Corner
DIBL = .0128 dVg/dVd, Vd=1.5-2.5, I=1e-4
Drain Current (A)
TDIBL_01.log
TDIBL_15.log
TDIBL_20.log
TDIBL_25.log
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Gate Voltage (V)

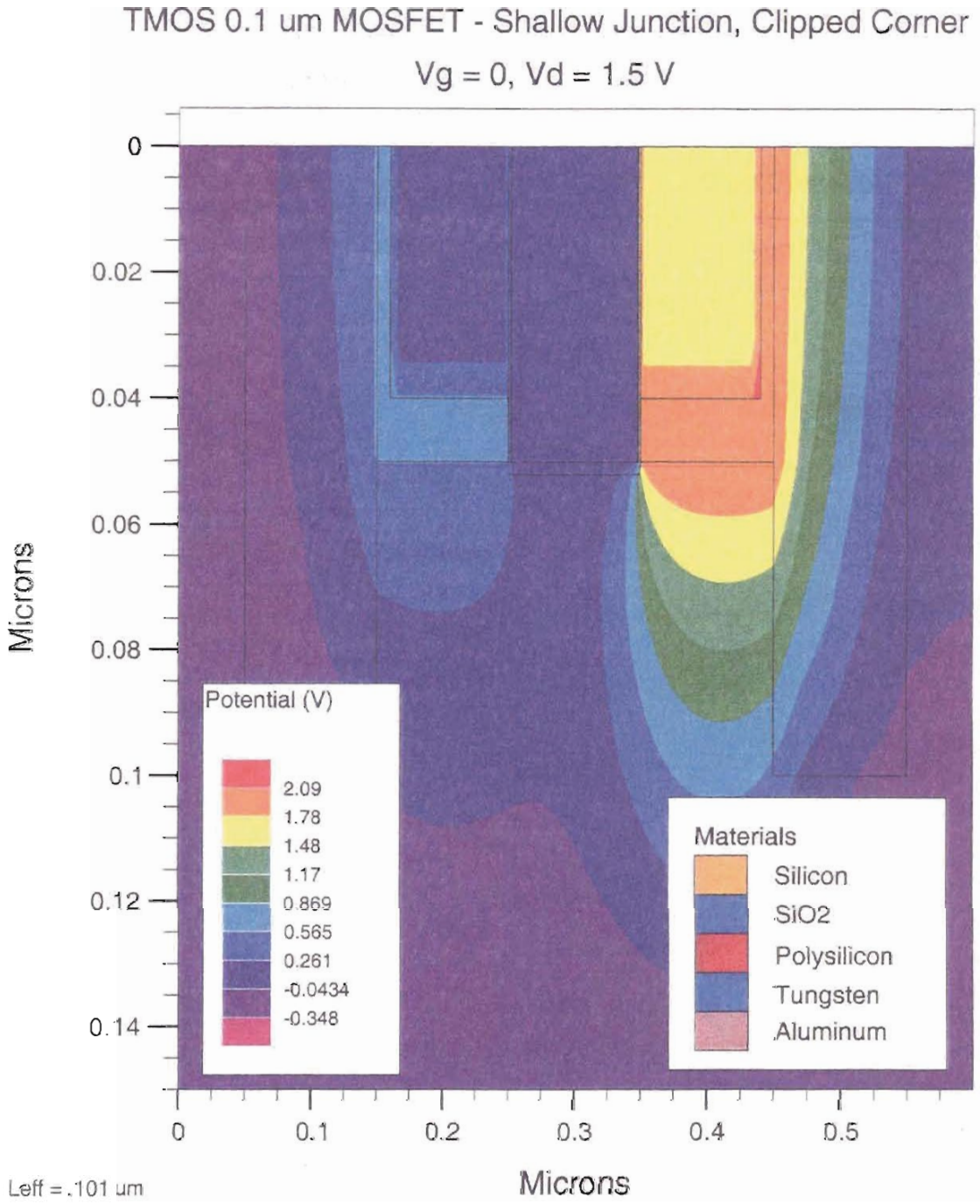

TMOS 0.1 um MOSFET - Shallow Junction, Round Corner
Sub-threshold Current
Drain Current (A)
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Gate Voltage (V)
Idmin=1.58e-11 A, Vt=0.40 V
SwingST=.085

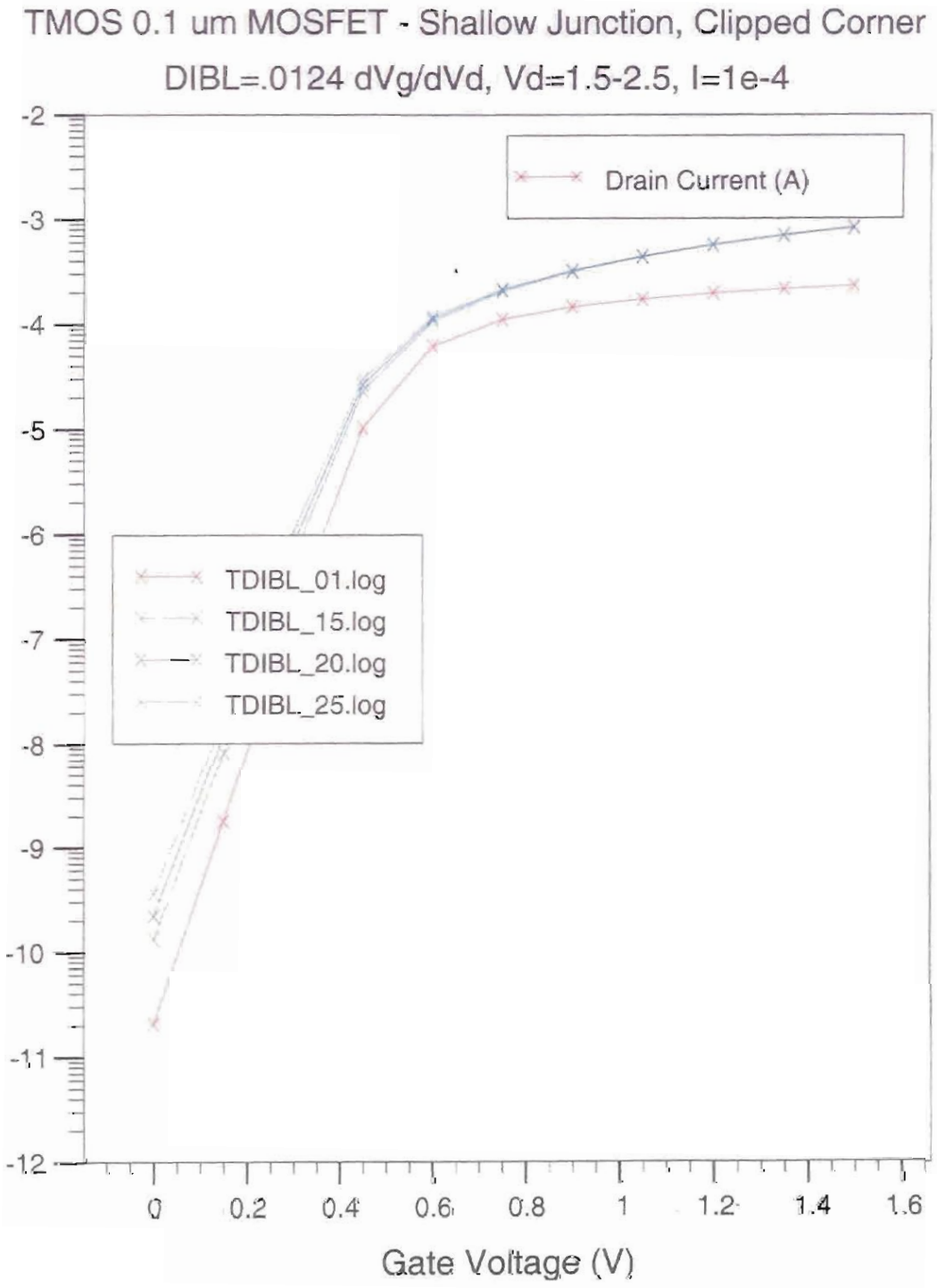

TMOS 0.1 um MOSFET - Shallow Junction, Round Corner
IV Curves
0.0008
0.0007
0.0006
0.0005
0.0004
0.0003
0.0002
0.0001
0
Drain Current (A)
TMOS_Id_1.log
TMOS_Id_2.log
TMOS_Id_3.log
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Drain Voltage (V)
Idmax=728um, r0=38700 Ohms

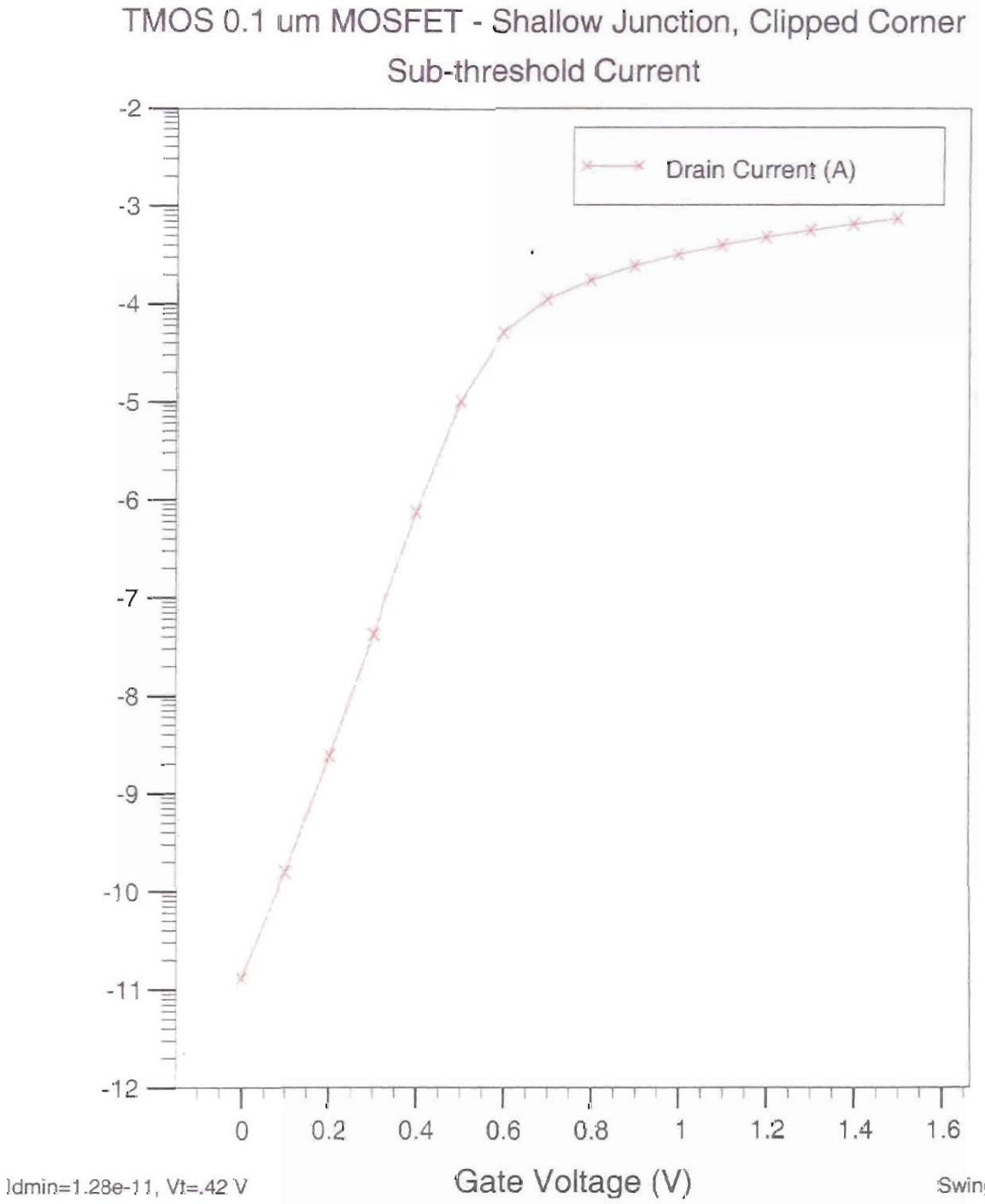
Appendix G. TMOS 0.1 um MOSFET - Shallow Junction, Clipped Corner

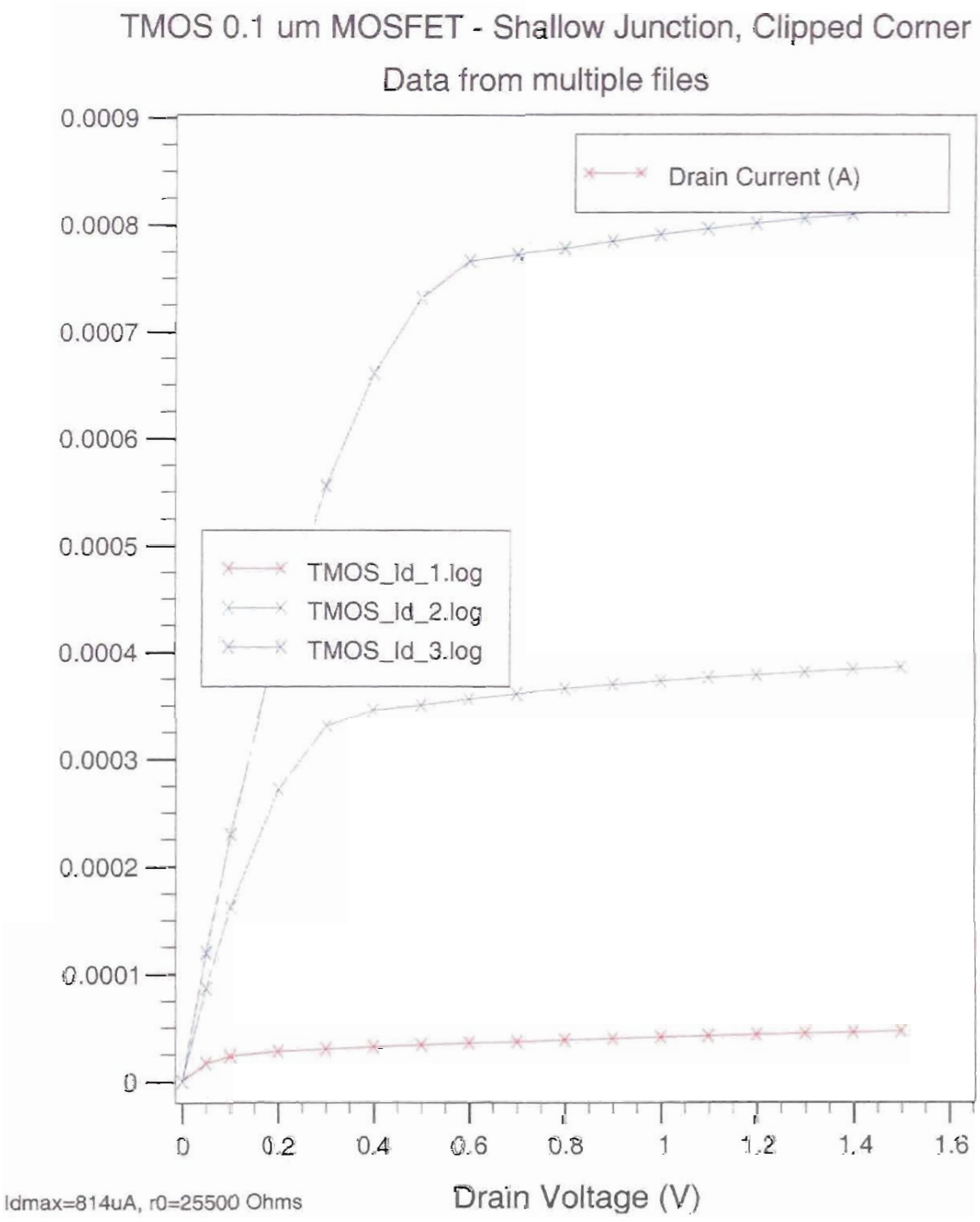

TMOS 0.1 um MOSFET - Shallow Junction, Clipped Corner
Vg = Vd = 1.5 V
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0
0.1
0.2
0.3
0.4
0.5
Microns
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum
Leff = .101 um


TMOS 0.1 um MOSFET - Shallow Junction, Clipped Corner
Vg = Vd = 1.5 V
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0
0.1
0.2
0.3
0.4
0.5
Microns
Potential (V)
2.09
1.78
1.48
1.17
0.869
0.565
0.261
-0.0434
-0.348
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum
Leff = .101 um

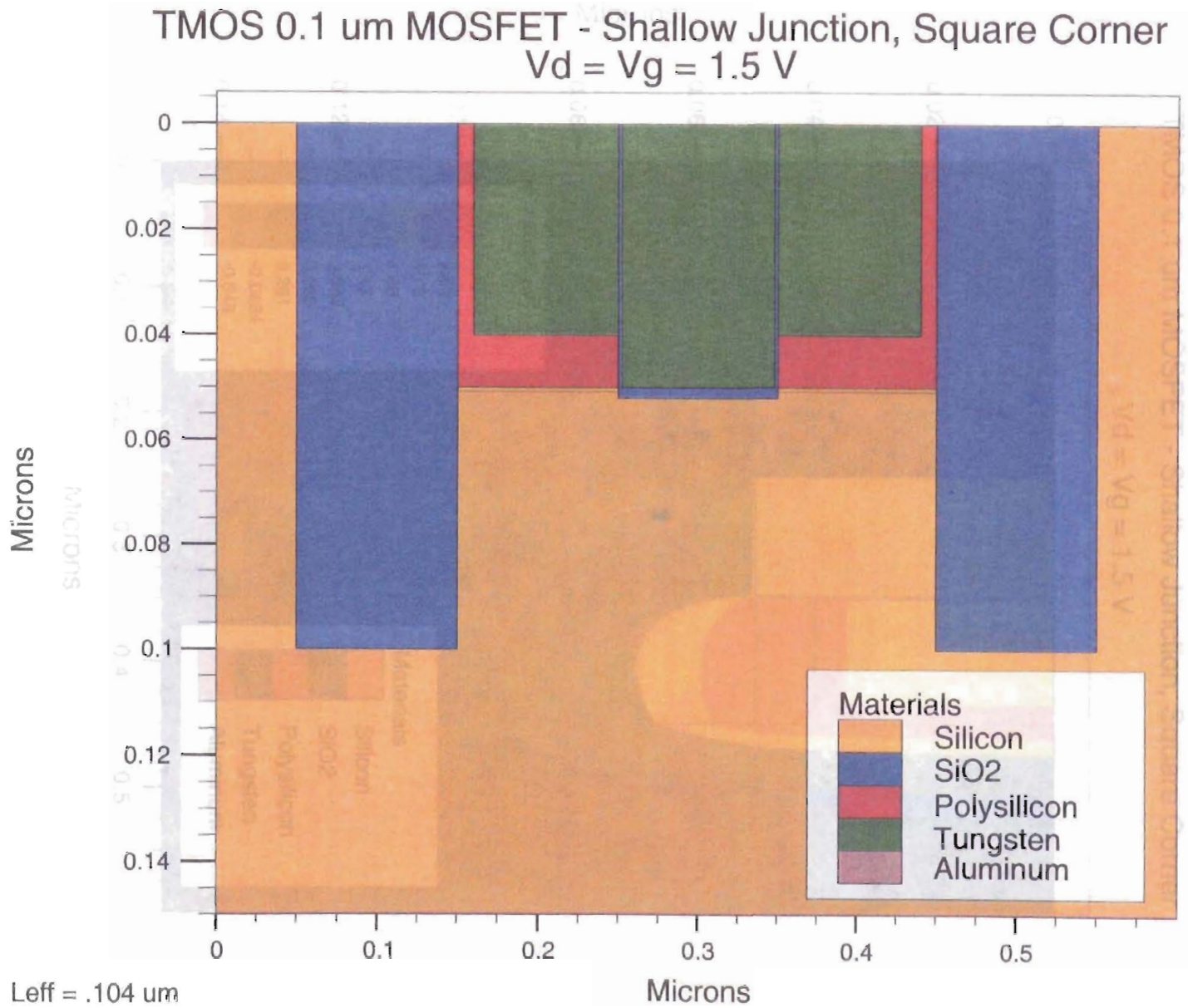

TMOS 0.1 um MOSFET - Shallow Junction, Clipped Corner
Vg = 0, Vd = 1.5 V
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0
0.1
0.2
0.3
0.4
0.5
Microns
Potential (V)
2.09
1.78
1.48
1.17
0.869
0.565
0.261
-0.0434
-0.348
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum
Leff = .101 um

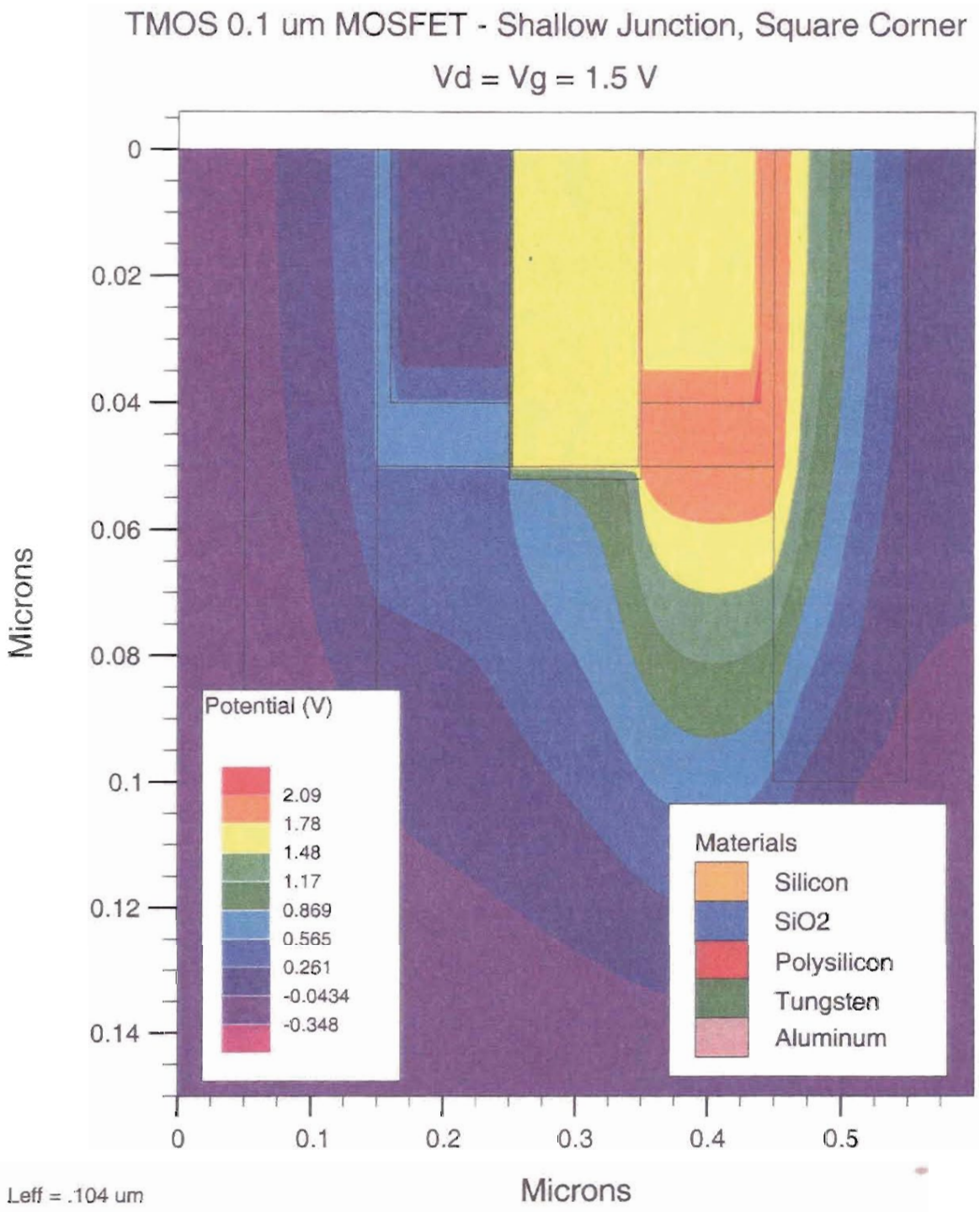

TMOS 0.1 um MOSFET - Shallow Junction, Clipped Corner
DIBL=.0124 dVg/dVd, Vd=1.5-2.5, I=1e-4
Drain Current (A)
TDIBL_01.log
TDIBL_15.log
TDIBL_20.log
TDIBL_25.log
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Gate Voltage (V)

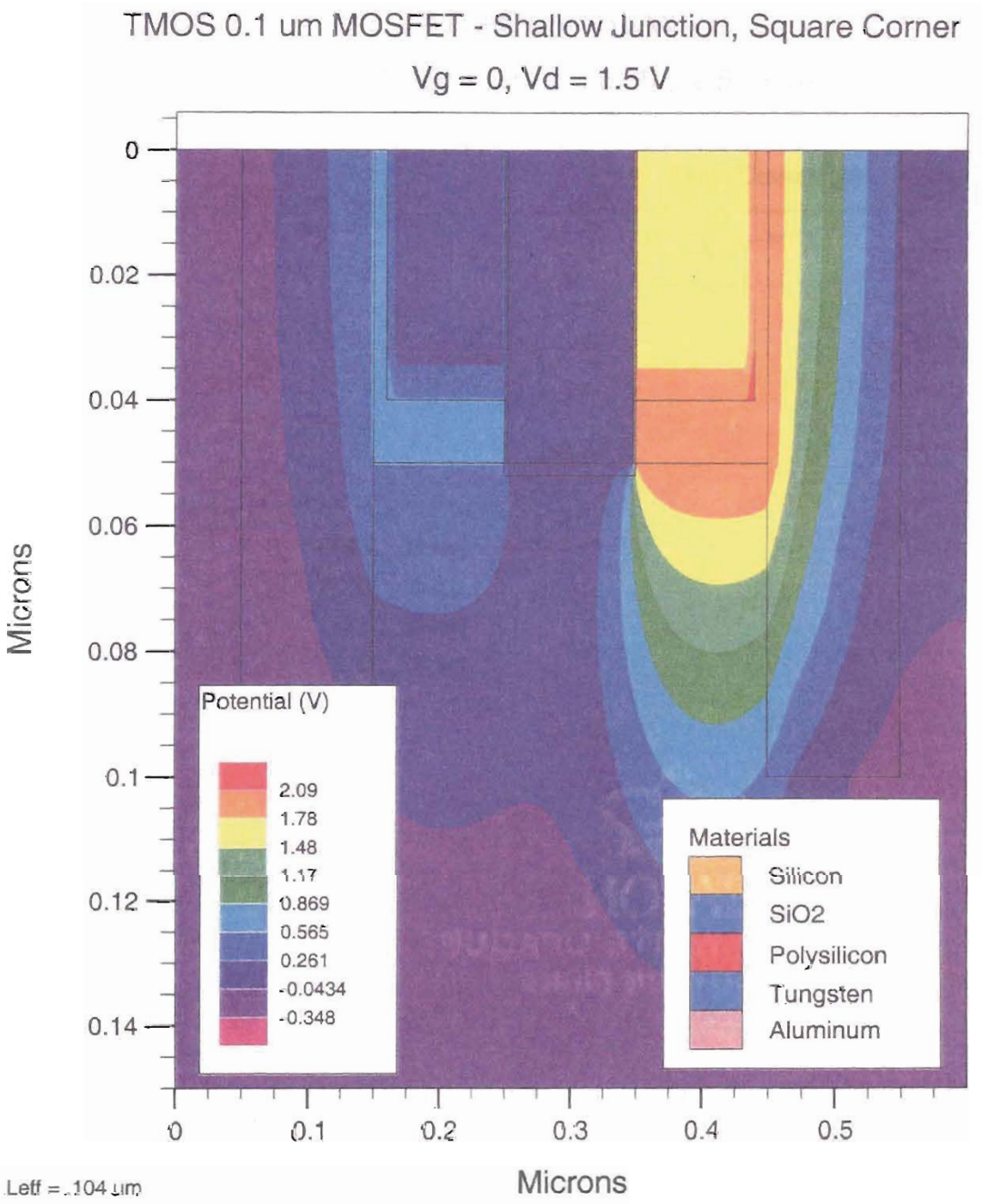

TMOS 0.1 um MOSFET - Shallow Junction, Clipped Corner
Sub-threshold Current
Drain Current (A)
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Gate Voltage (V)
Idmin=1.28e-11, Vt=.42 V
SwingST=.084

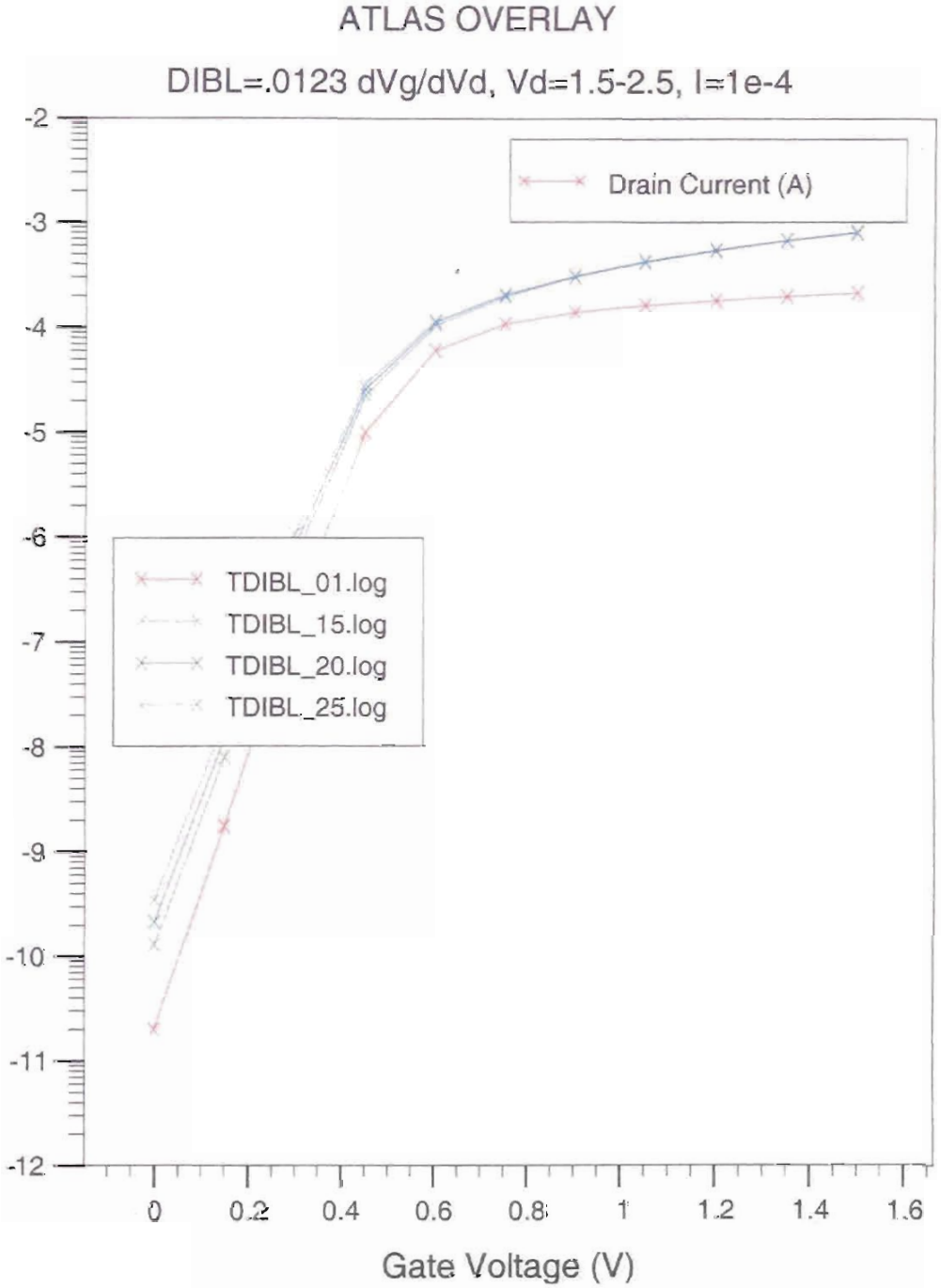

TMOS 0.1 um MOSFET - Shallow Junction, Clipped Corner
Data from multiple files
Drain Current (A)
TMOS_Id_1.log
TMOS_Id_2.log
TMOS_Id_3.log
0.0009
0.0008
0.0007
0.0006
0.0005
0.0004
0.0003
0.0002
0.0001
0
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Idmax=814uA, r0=25500 Ohms
Drain Voltage (V)

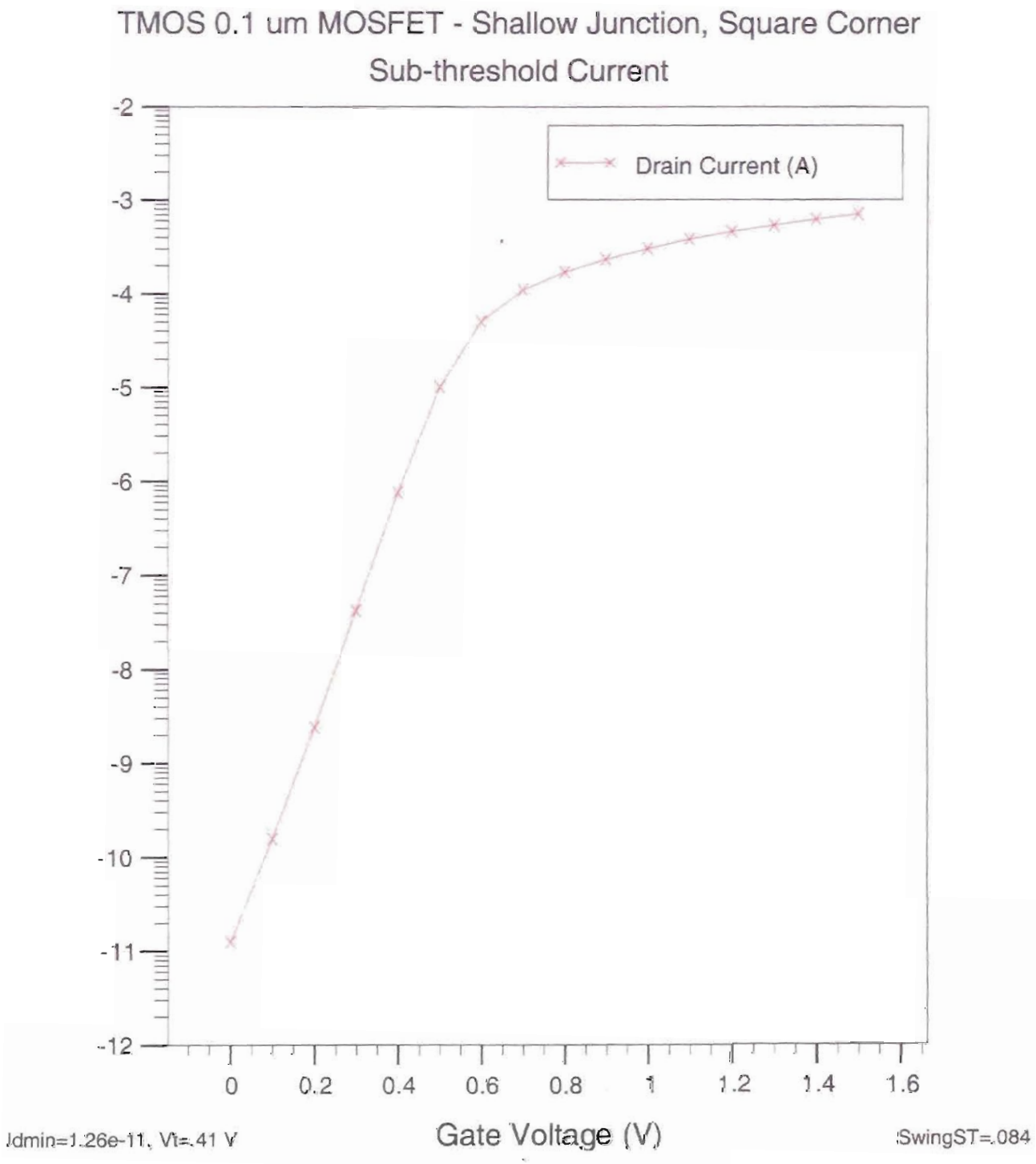
Appendix H. TMOS 0.1 um MOSFET - Shallow Junction, Square Corner

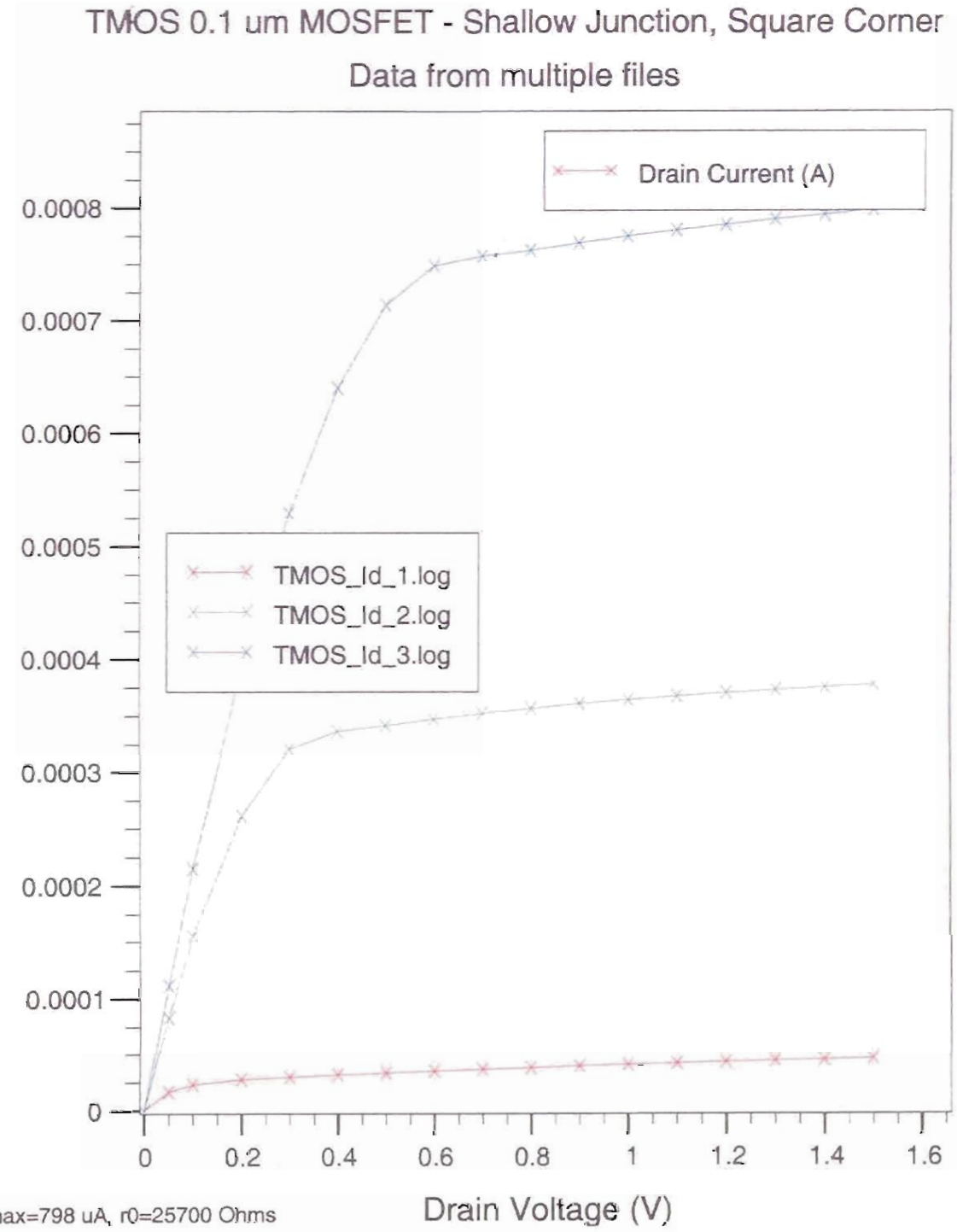

TMOS 0.1 um MOSFET - Shallow Junction, Square Corner
Vd = Vg = 1.5 V
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0
0.1
0.2
0.3
0.4
0.5
Microns
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum
Leff = .104 um


TMOS 0.1 um MOSFET - Shallow Junction, Square Corner
Vd = Vg = 1.5 V
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0
0.1
0.2
0.3
0.4
0.5
Microns
Potential (V)
2.09
1.78
1.48
1.17
0.869
0.565
0.261
-0.0434
-0.348
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum
Leff = .104 um

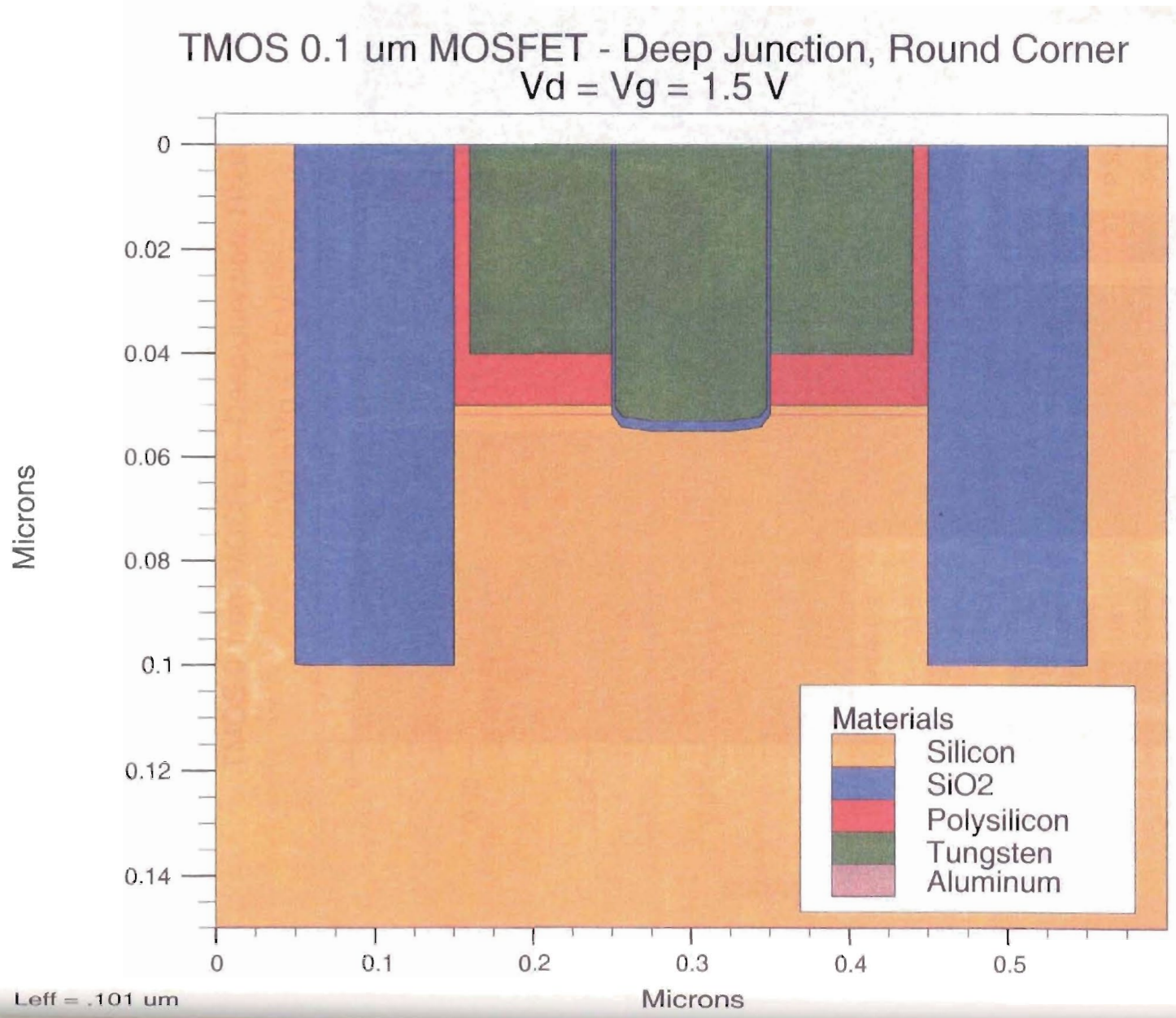

TMOS 0.1 um MOSFET - Shallow Junction, Square Corner
Vg = 0, Vd = 1.5 V
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0
0.1
0.2
0.3
0.4
0.5
Microns
Potential (V)
2.09
1.78
1.48
1.17
0.869
0.565
0.261
-0.0434
-0.348
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum
Leff = .104 um

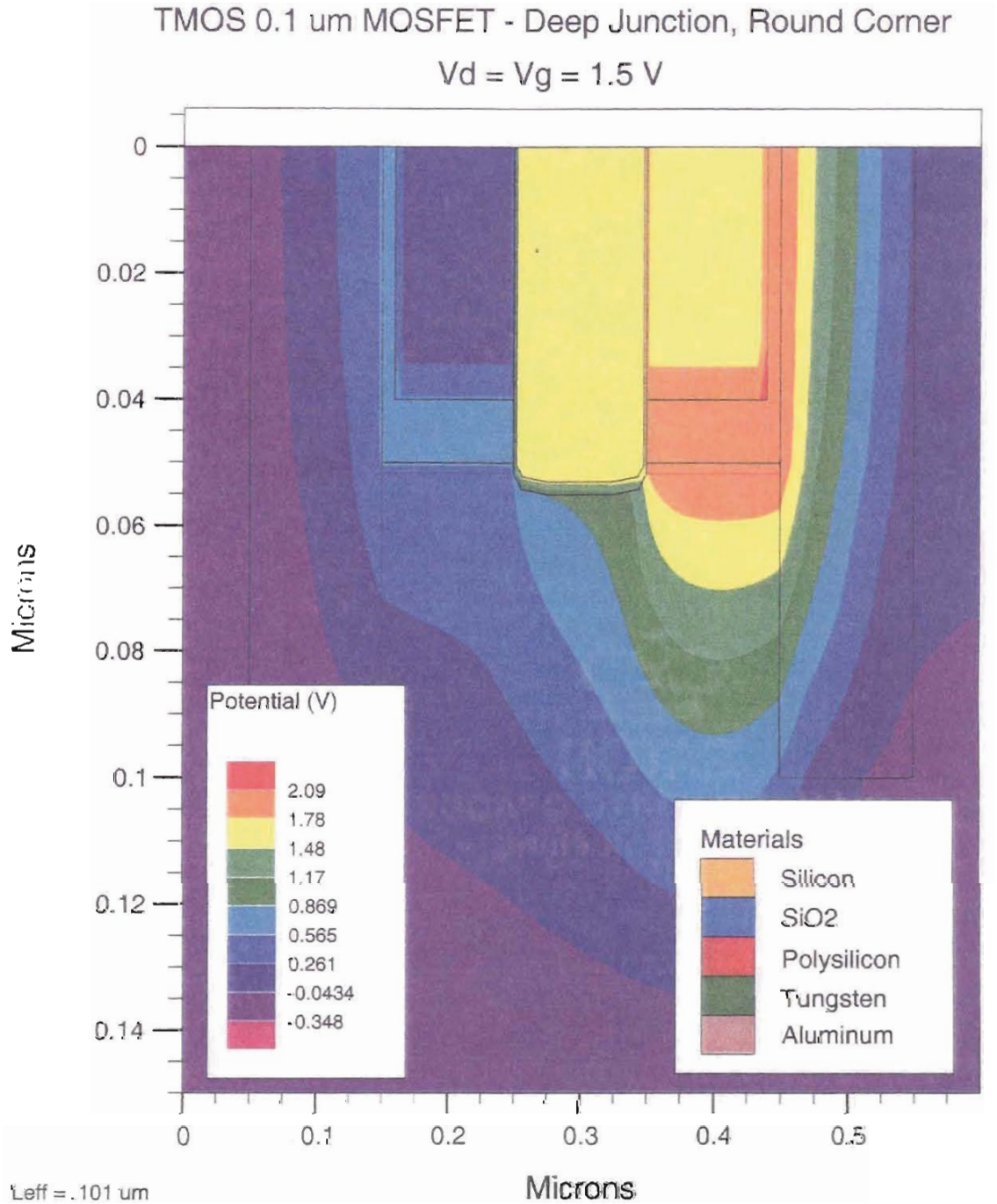

ATLAS OVERLAY
DIBL=.0123 dVg/dVd, Vd=1.5-2.5, I=1e-4
Drain Current (A)
TDIBL_01.log
TDIBL_15.log
TDIBL_20.log
TDIBL_25.log
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Gate Voltage (V)

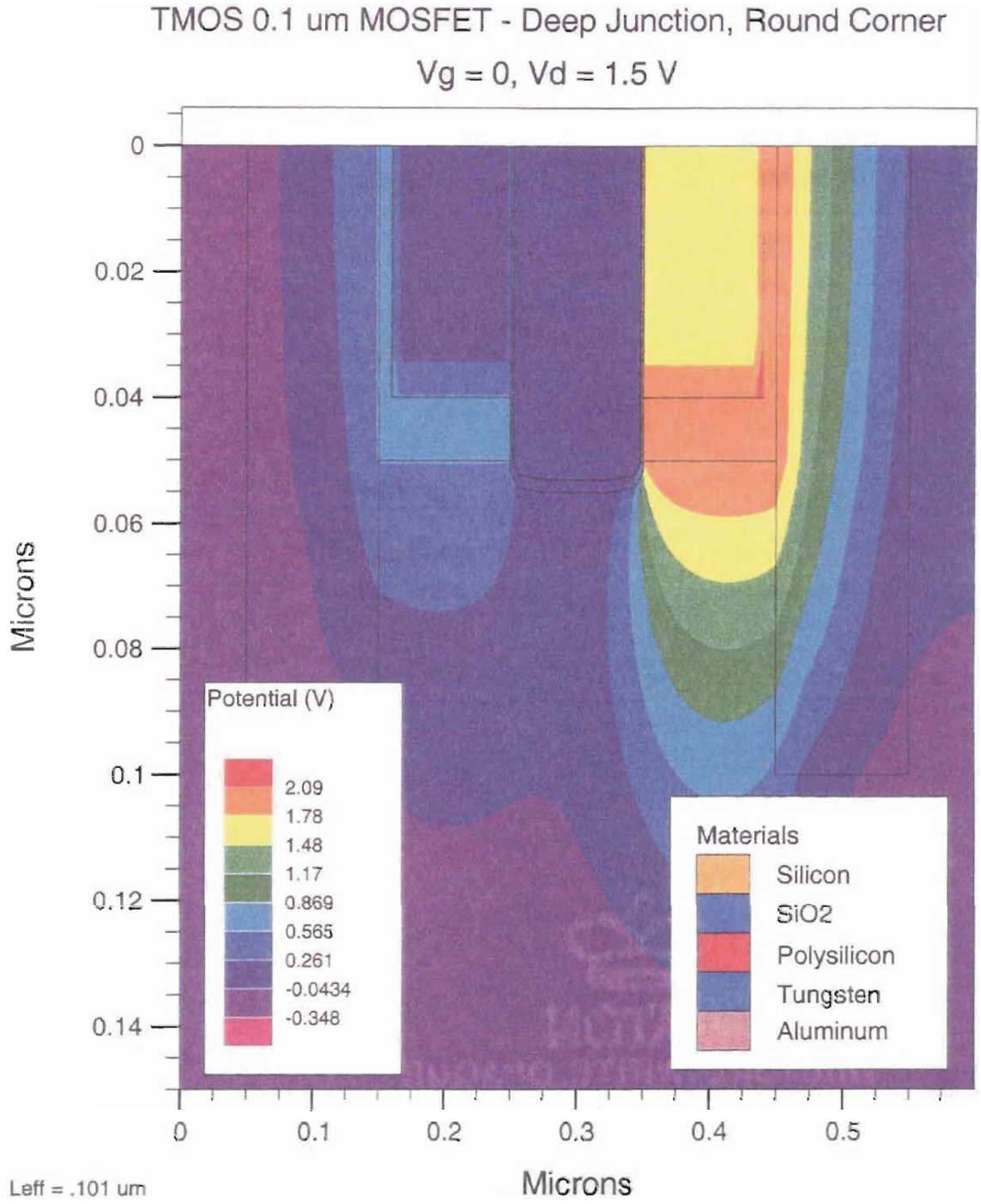

TMOS 0.1 um MOSFET - Shallow Junction, Square Corner
Sub-threshold Current
Drain Current (A)
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Gate Voltage (V)
Idmin=1.26e-11, Vt=.41 V
SwingST=.084

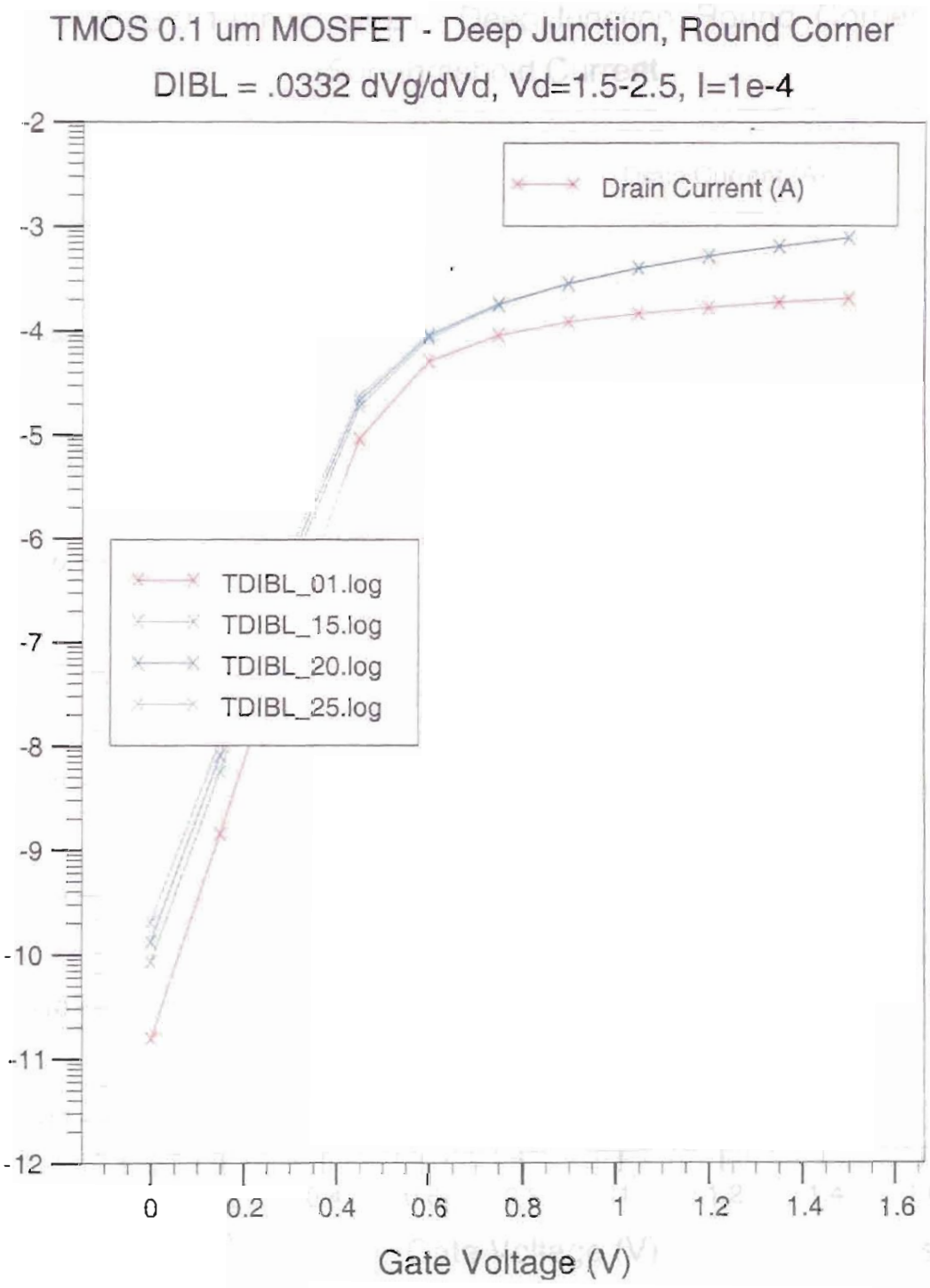

TMOS 0.1 um MOSFET - Shallow Junction, Square Corner
Data from multiple files
Drain Current (A)
TMOS_Id_1.log
TMOS_Id_2.log
TMOS_Id_3.log
0.0008
0.0007
0.0006
0.0005
0.0004
0.0003
0.0002
0.0001
0
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Drain Voltage (V)
Idmax=798 uA, r0=25700 Ohms

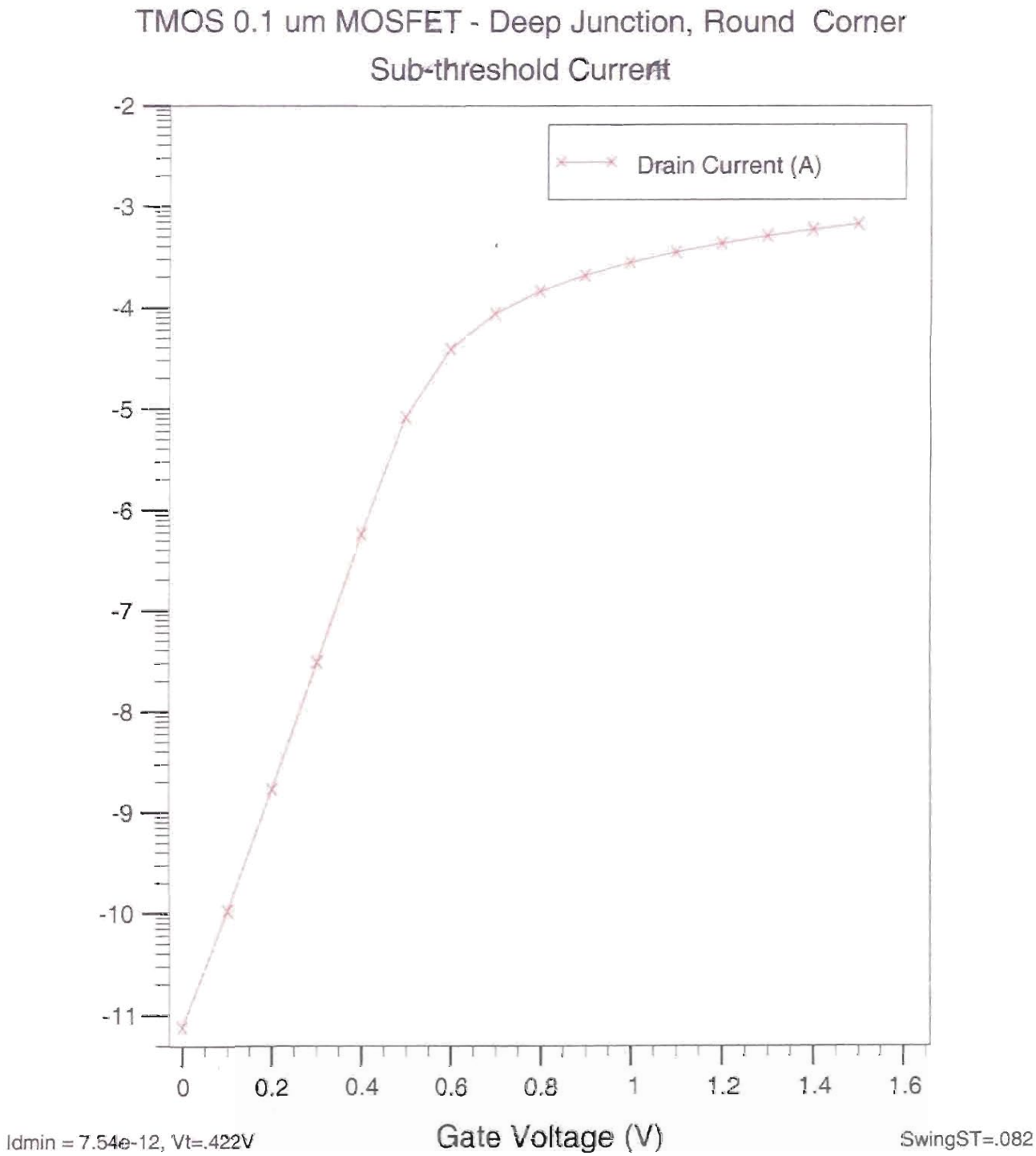
Appendix I. TMOS 0.1 um MOSFET - Deep Junction, Round Corner

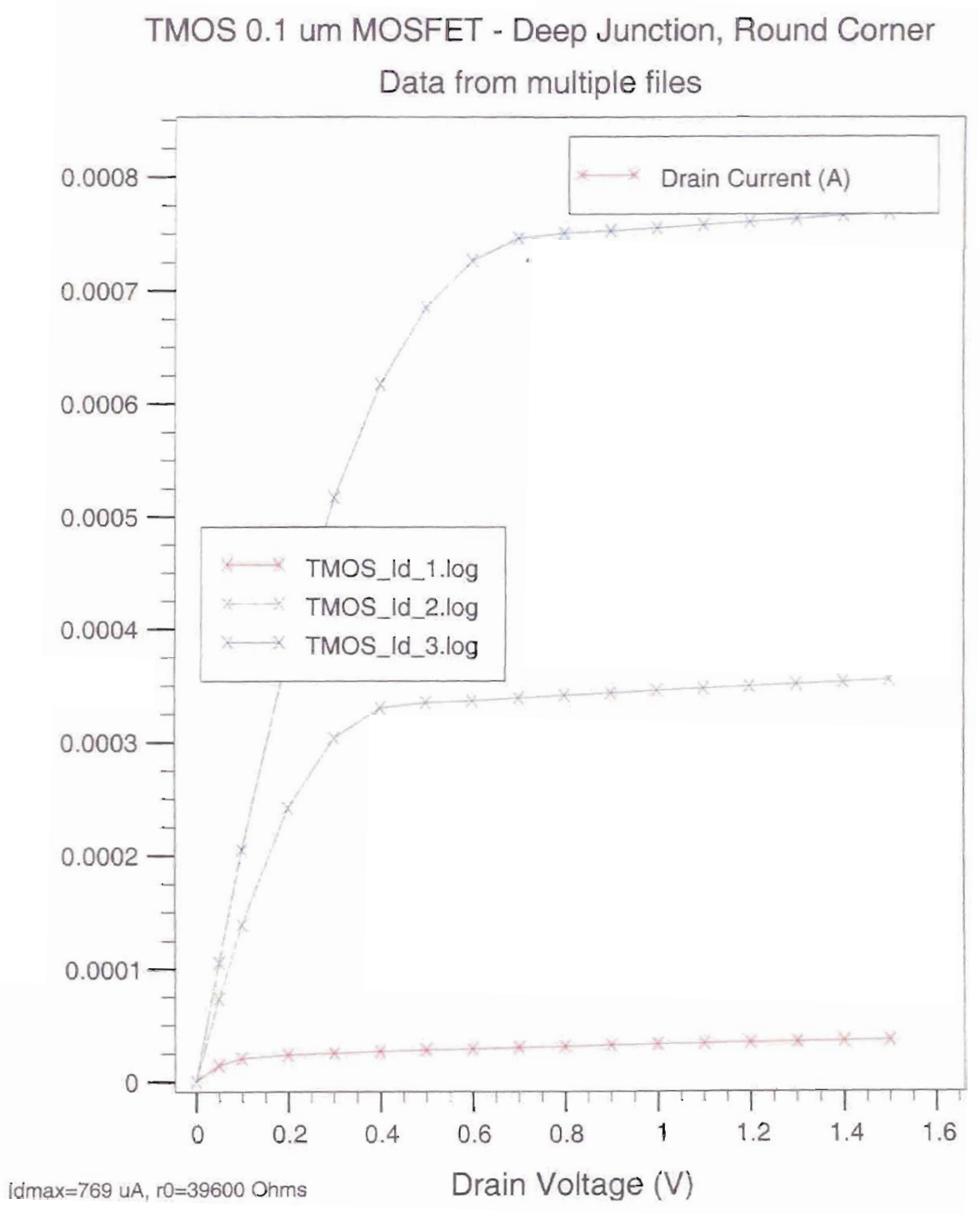

TMOS 0.1 um MOSFET - Deep Junction, Round Corner
Vd = Vg = 1.5 V
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0
0.1
0.2
0.3
0.4
0.5
Microns
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum
Leff = .101 um


TMOS 0.1 um MOSFET - Deep Junction, Round Corner
Vd = Vg = 1.5 V
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
Potential (V)
2.09
1.78
1.48
1.17
0.869
0.565
0.261
-0.0434
-0.348
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum
0
0.1
0.2
0.3
0.4
0.5
Microns
Leff = .101 um

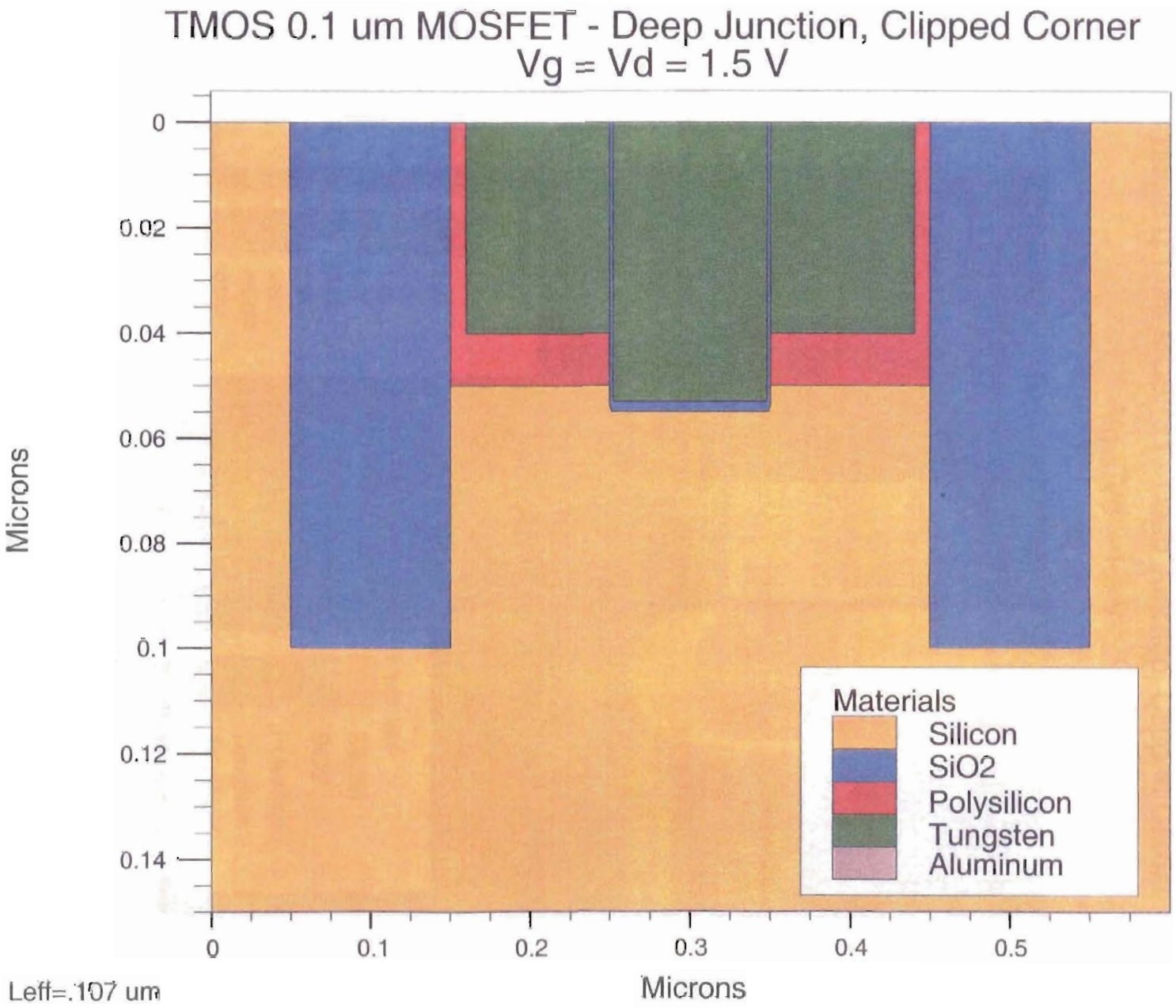

TMOS 0.1 um MOSFET - Deep Junction, Round Corner
Vg = 0, Vd = 1.5 V
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
Potential (V)
2.09
1.78
1.48
1.17
0.869
0.565
0.261
-0.0434
-0.348
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum
0
0.1
0.2
0.3
0.4
0.5
Microns
Leff = .101 um

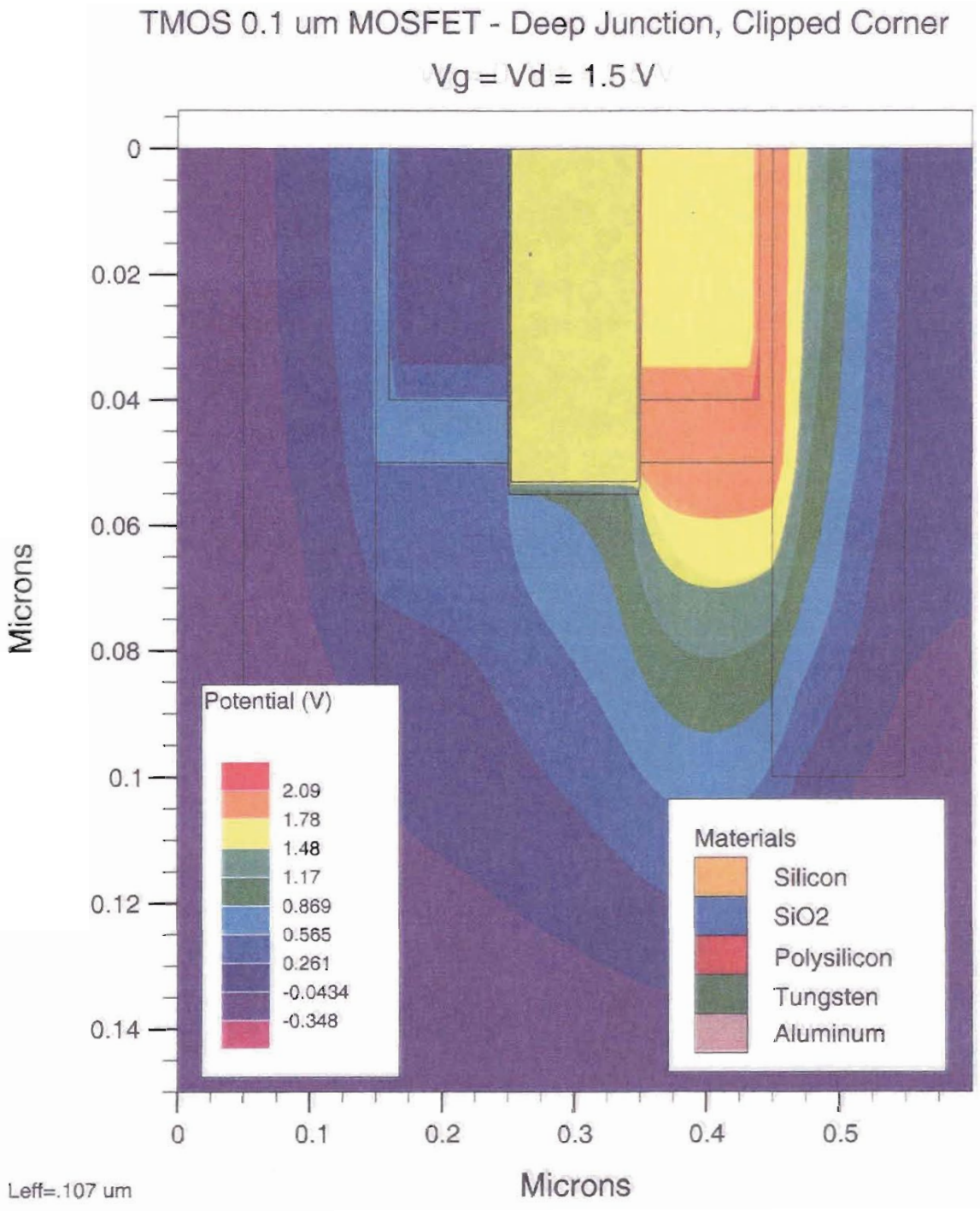

TMOS 0.1 um MOSFET - Deep Junction, Round Corner
DIBL = .0332 dVg/dVd, Vd=1.5-2.5, I=1e-4
Drain Current (A)
TDIBL_01.log
TDIBL_15.log
TDIBL_20.log
TDIBL_25.log
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Gate Voltage (V)

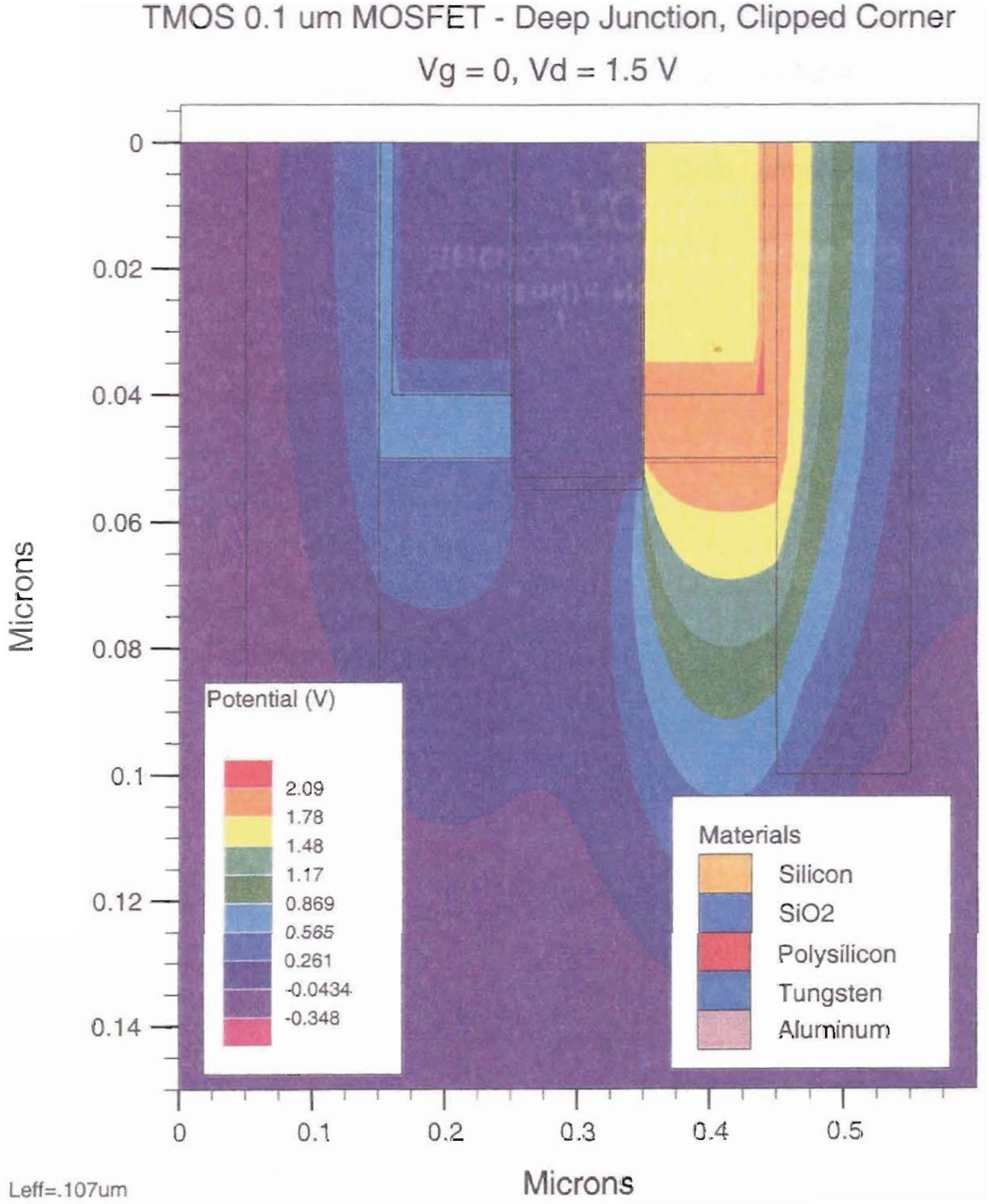

TMOS 0.1 um MOSFET - Deep Junction, Round Corner
Sub-threshold Current
Drain Current (A)
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Gate Voltage (V)
Idmin = 7.54e-12, Vt=.422V
SwingST=.082

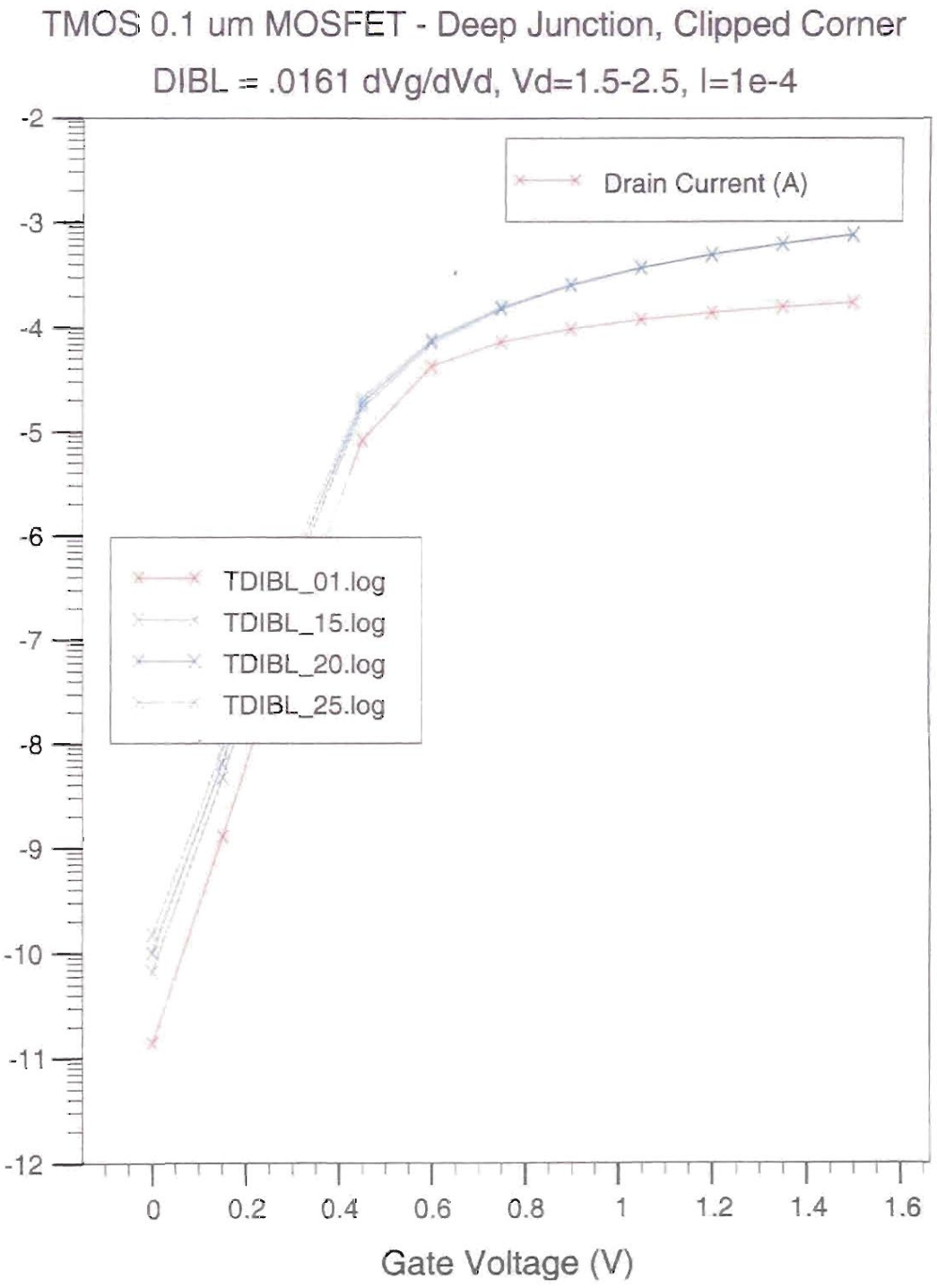

TMOS 0.1 um MOSFET - Deep Junction, Round Corner
Data from multiple files
Drain Current (A)
TMOS_Id_1.log
TMOS_Id_2.log
TMOS_Id_3.log
0.0008
0.0007
0.0006
0.0005
0.0004
0.0003
0.0002
0.0001
0
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Idmax=769 uA, r0=39600 Ohms
Drain Voltage (V)

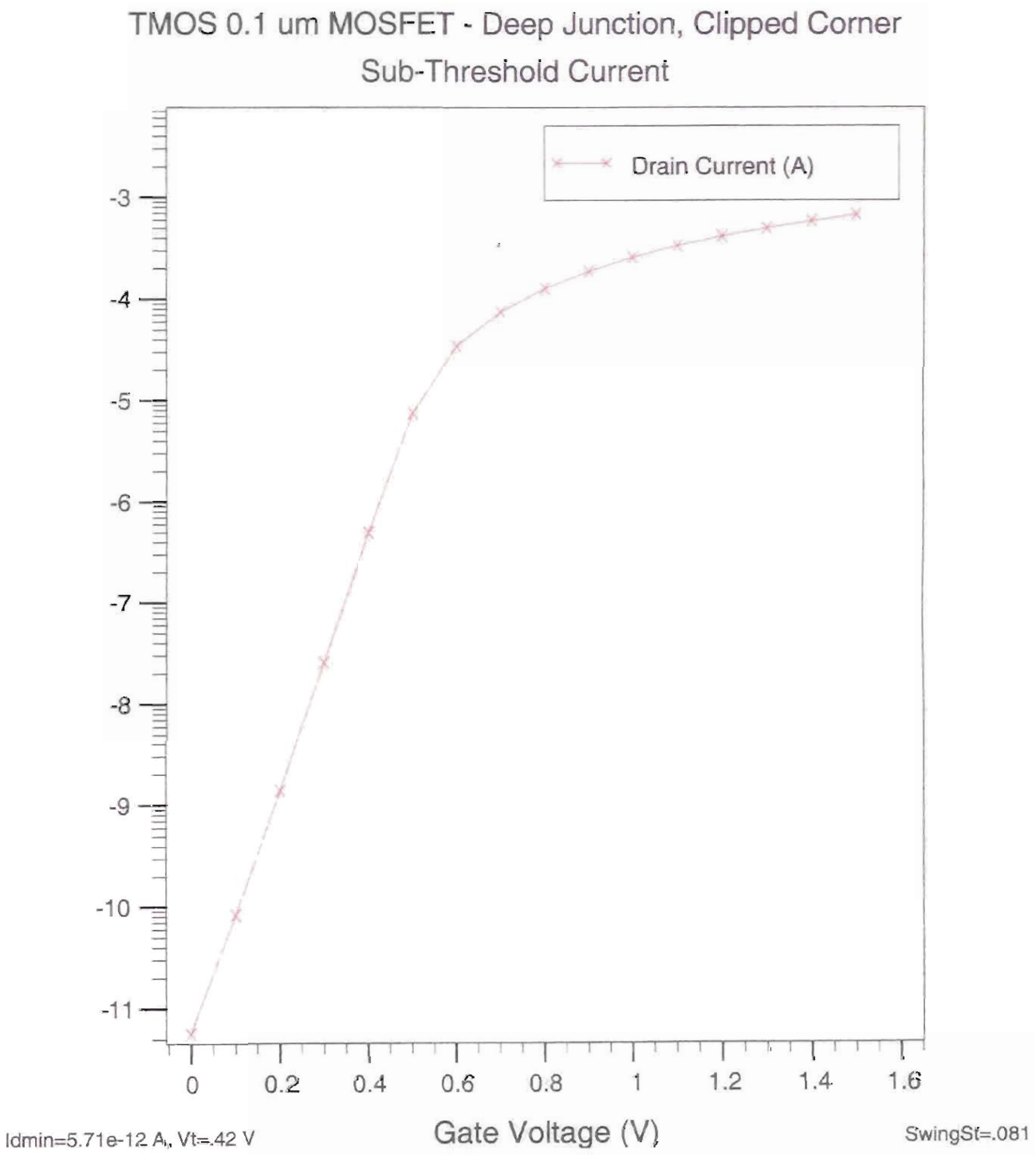
Appendix J. TMOS 0.1 um MOSFET - Deep Junction, Clipped Corner

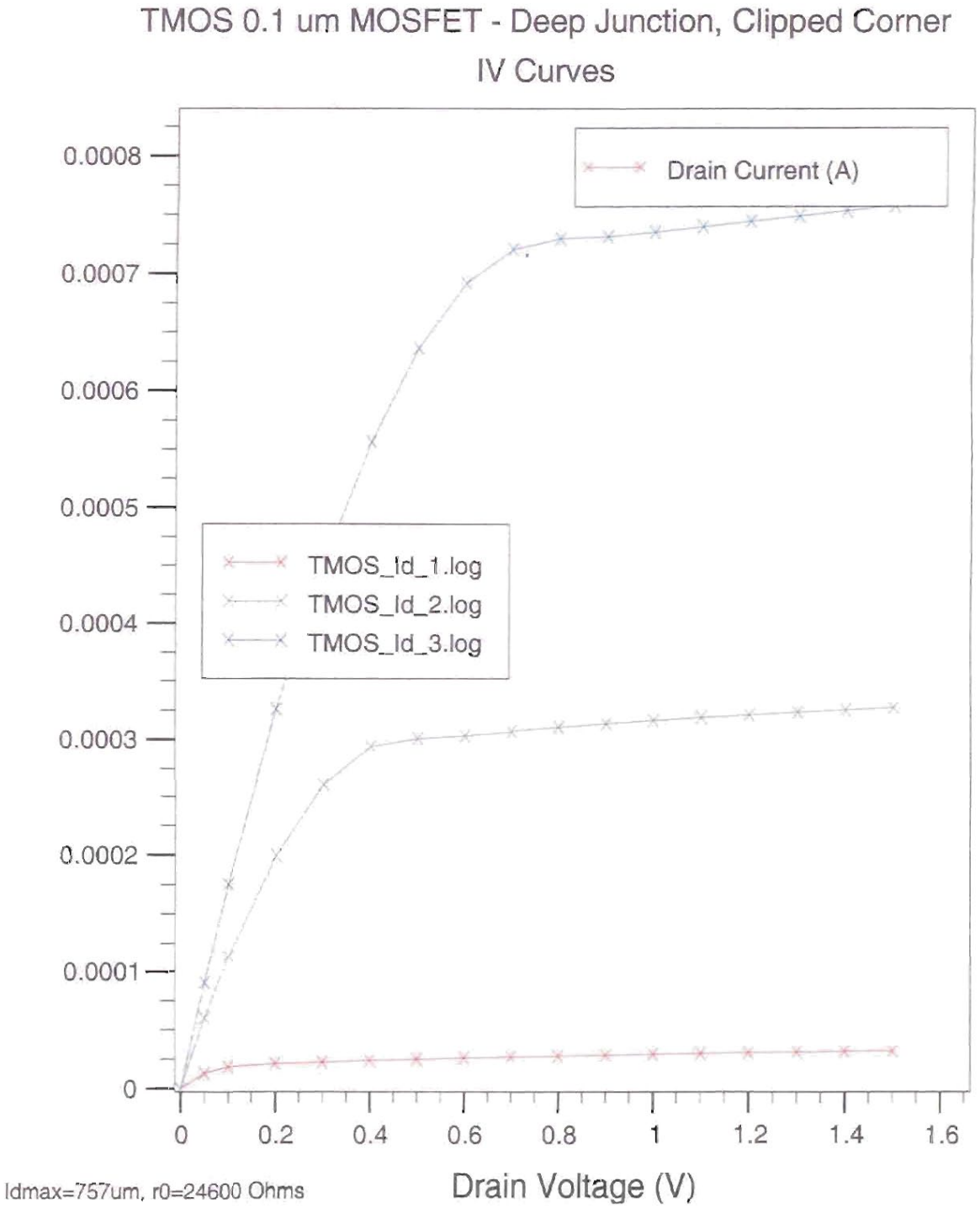

TMOS 0.1 um MOSFET - Deep Junction, Clipped Corner
Vg = Vd = 1.5 V
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0
0.1
0.2
0.3
0.4
0.5
Microns
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum
Leff=.107 um


TMOS 0.1 um MOSFET - Deep Junction, Clipped Corner
Vg = Vd = 1.5 V
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0
0.1
0.2
0.3
0.4
0.5
Microns
Potential (V)
2.09
1.78
1.48
1.17
0.869
0.565
0.261
-0.0434
-0.348
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum
Leff=.107 um

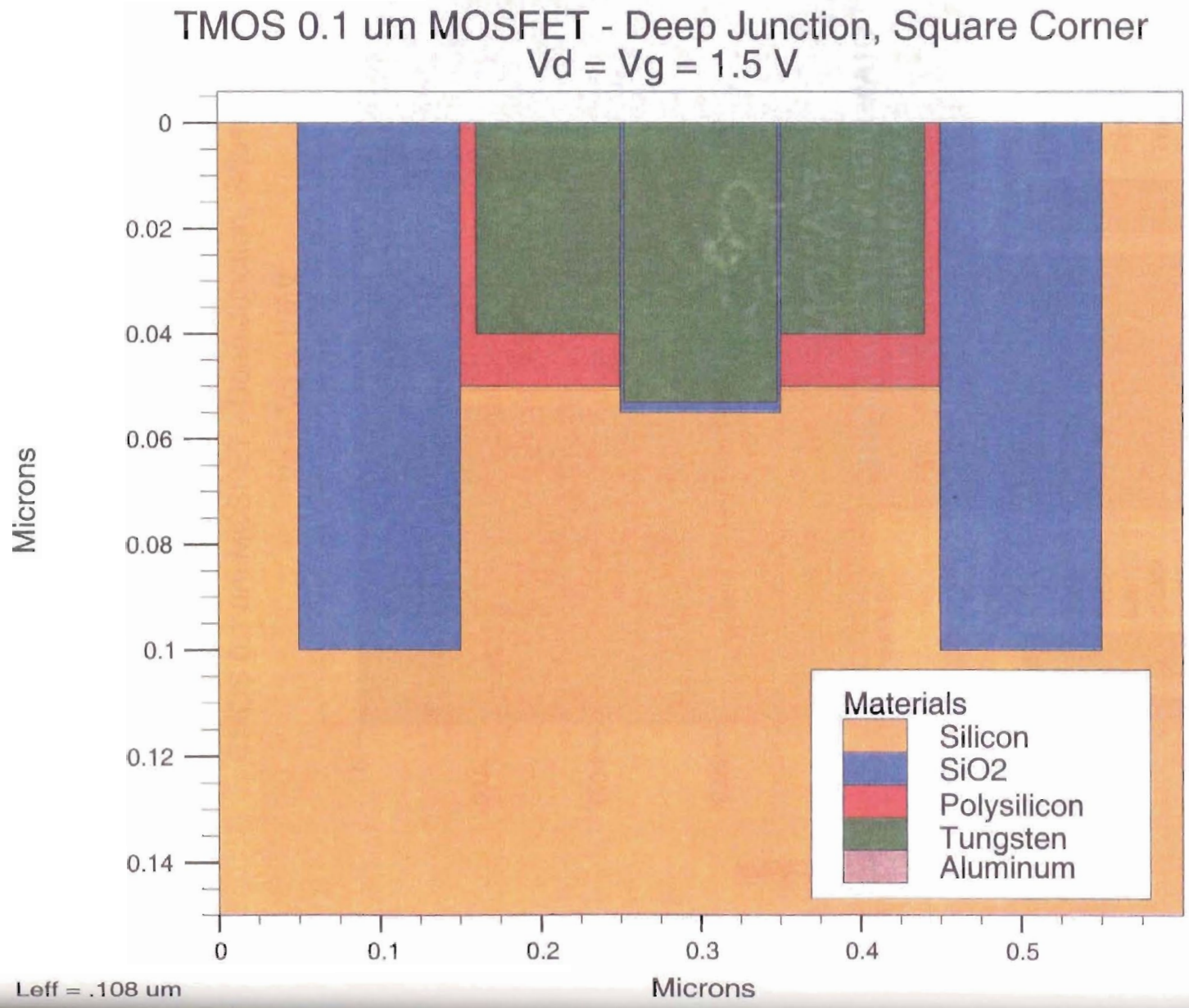

TMOS 0.1 um MOSFET - Deep Junction, Clipped Corner
Vg = 0, Vd = 1.5 V
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
Potential (V)
2.09
1.78
1.48
1.17
0.869
0.565
0.261
-0.0434
-0.348
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum
0
0.1
0.2
0.3
0.4
0.5
Microns
Leff=.107um

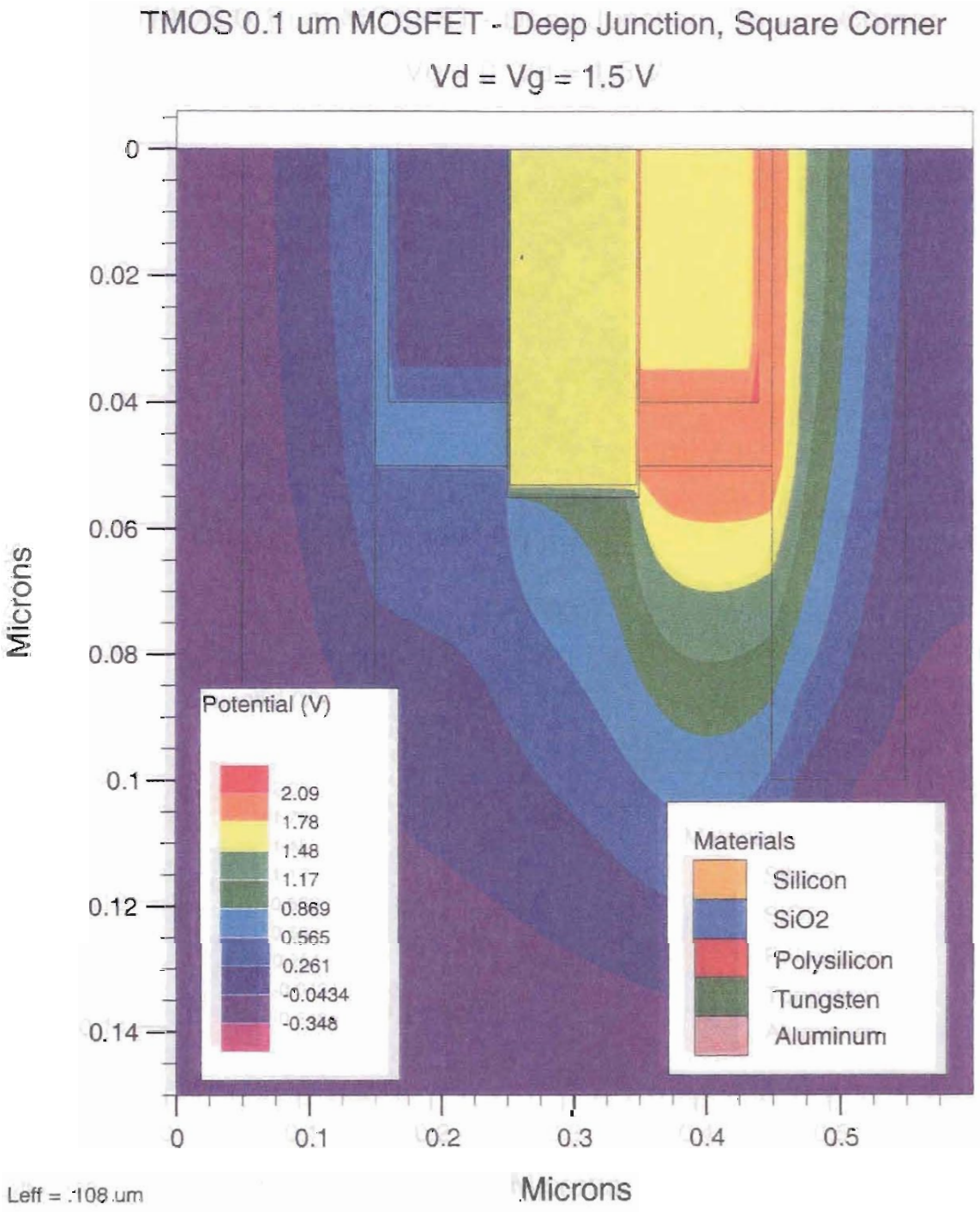

TMOS 0.1 um MOSFET - Deep Junction, Clipped Corner
DIBL = .0161 dVg/dVd, Vd=1.5-2.5, I=1e-4
Drain Current (A)
TDIBL_01.log
TDIBL_15.log
TDIBL_20.log
TDIBL_25.log
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Gate Voltage (V)

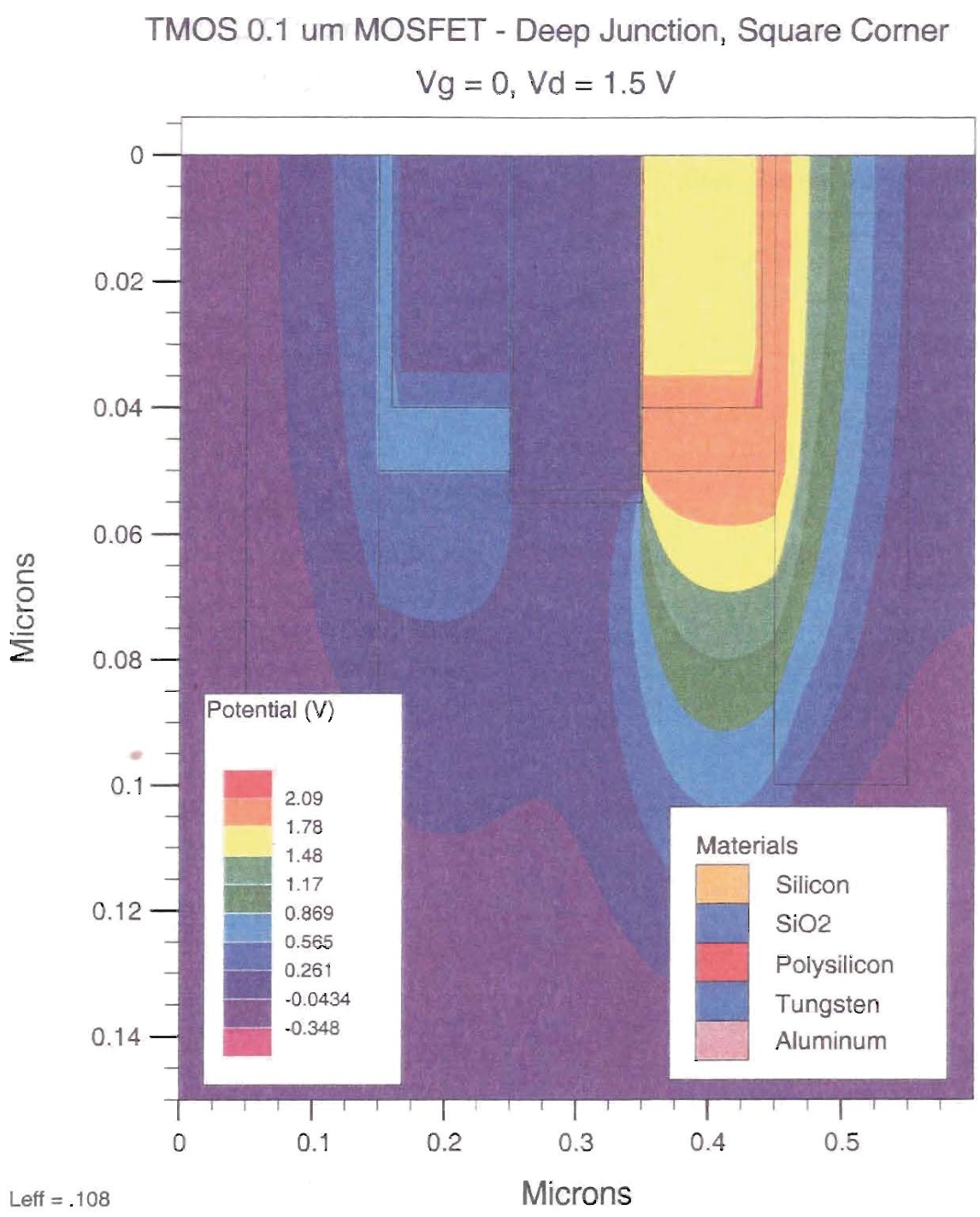

TMOS 0.1 um MOSFET - Deep Junction, Clipped Corner
Sub-Threshold Current
Drain Current (A)
-3
-4
-5
-6
-7
-8
-9
-10
-11
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Gate Voltage (V)
Idmin=5.71e-12 A, Vt=.42 V
SwingSt=.081

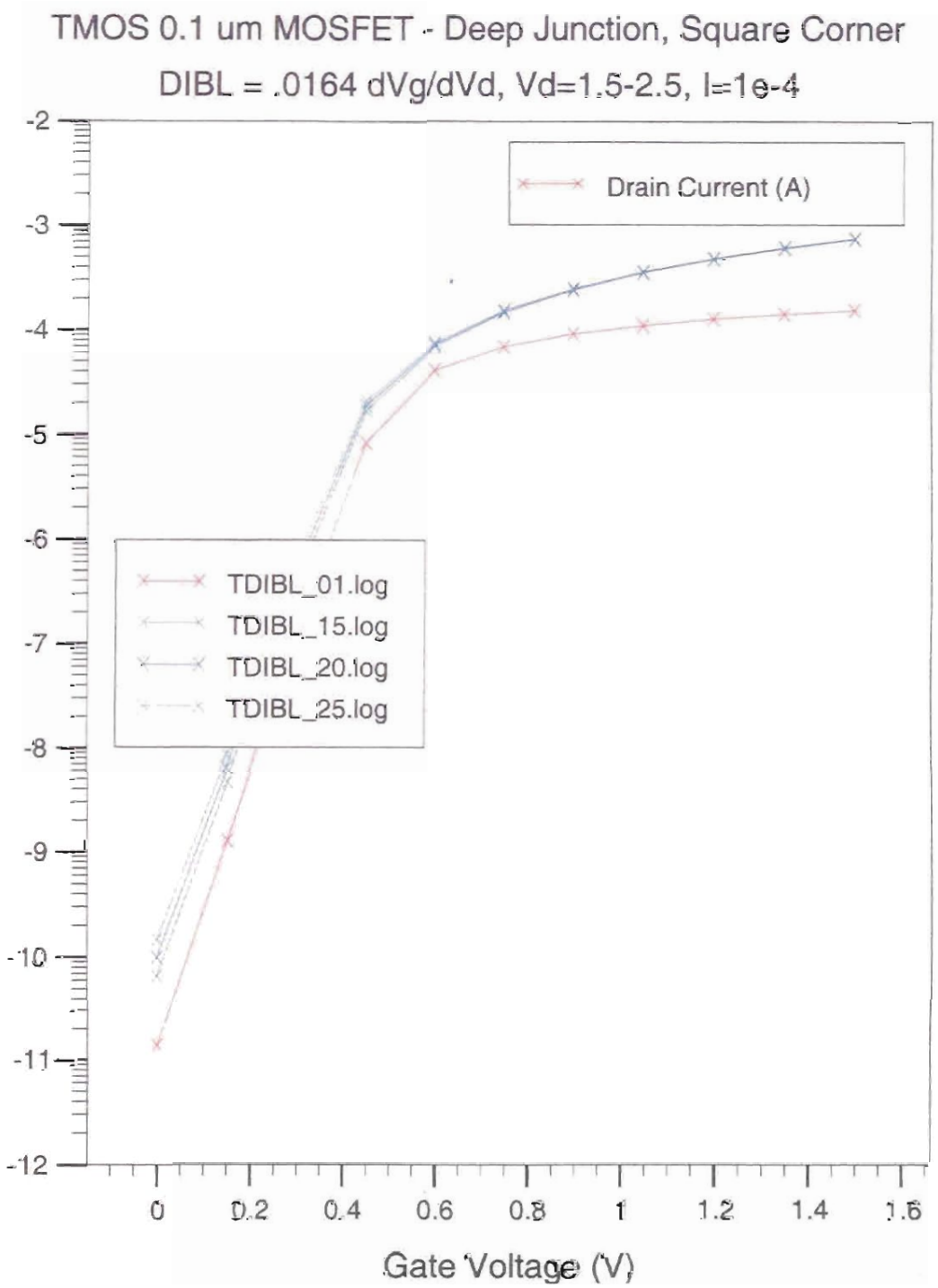

TMOS 0.1 um MOSFET - Deep Junction, Clipped Corner
IV Curves
Drain Current (A)
TMOS_Id_1.log
TMOS_Id_2.log
TMOS_Id_3.log
0.0008
0.0007
0.0006
0.0005
0.0004
0.0003
0.0002
0.0001
0
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Drain Voltage (V)
Idmax=757um, r0=24600 Ohms

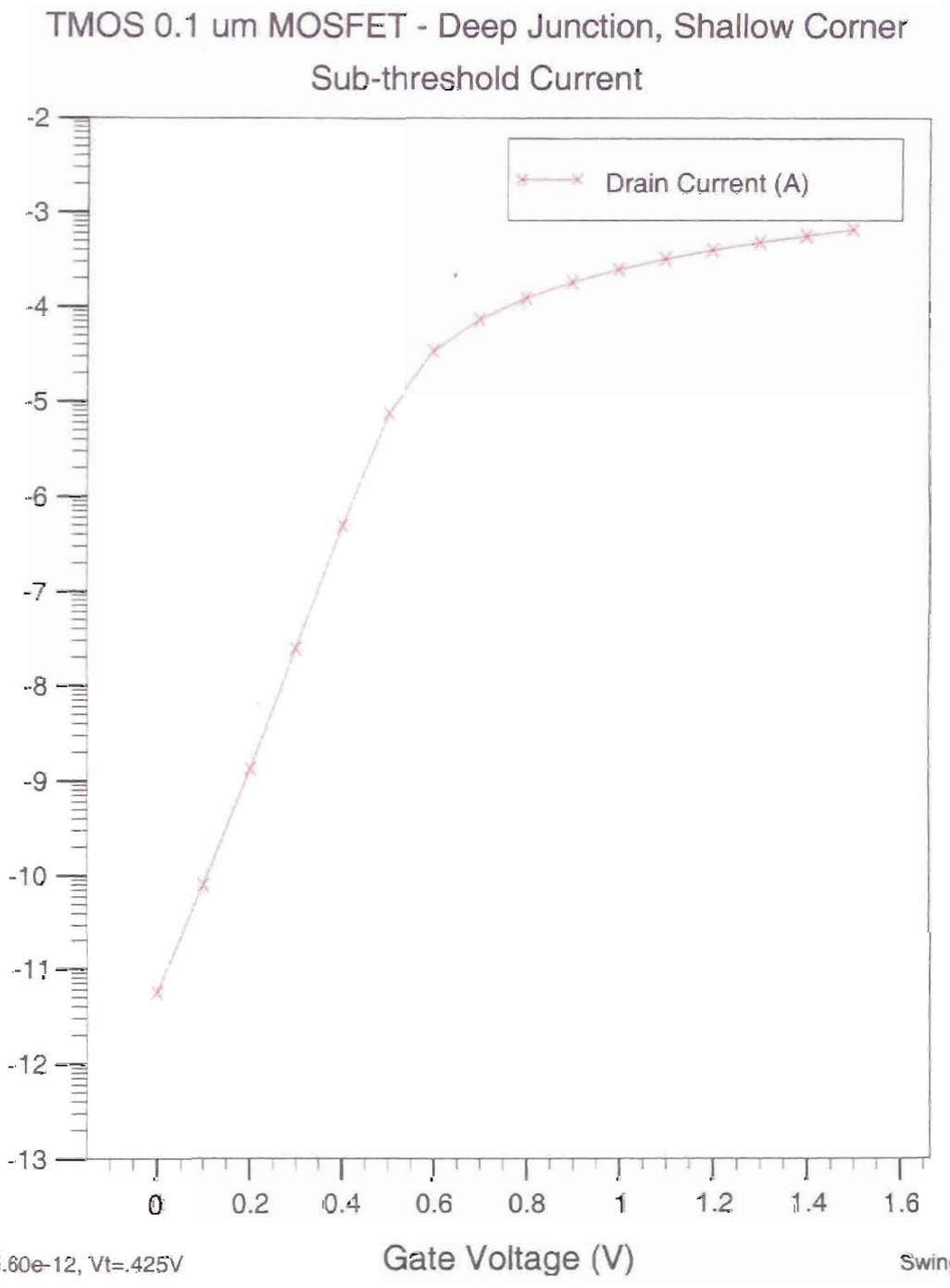
Appendix K. TMOS 0.1 um MOSFET - Deep Junction, Square Corner

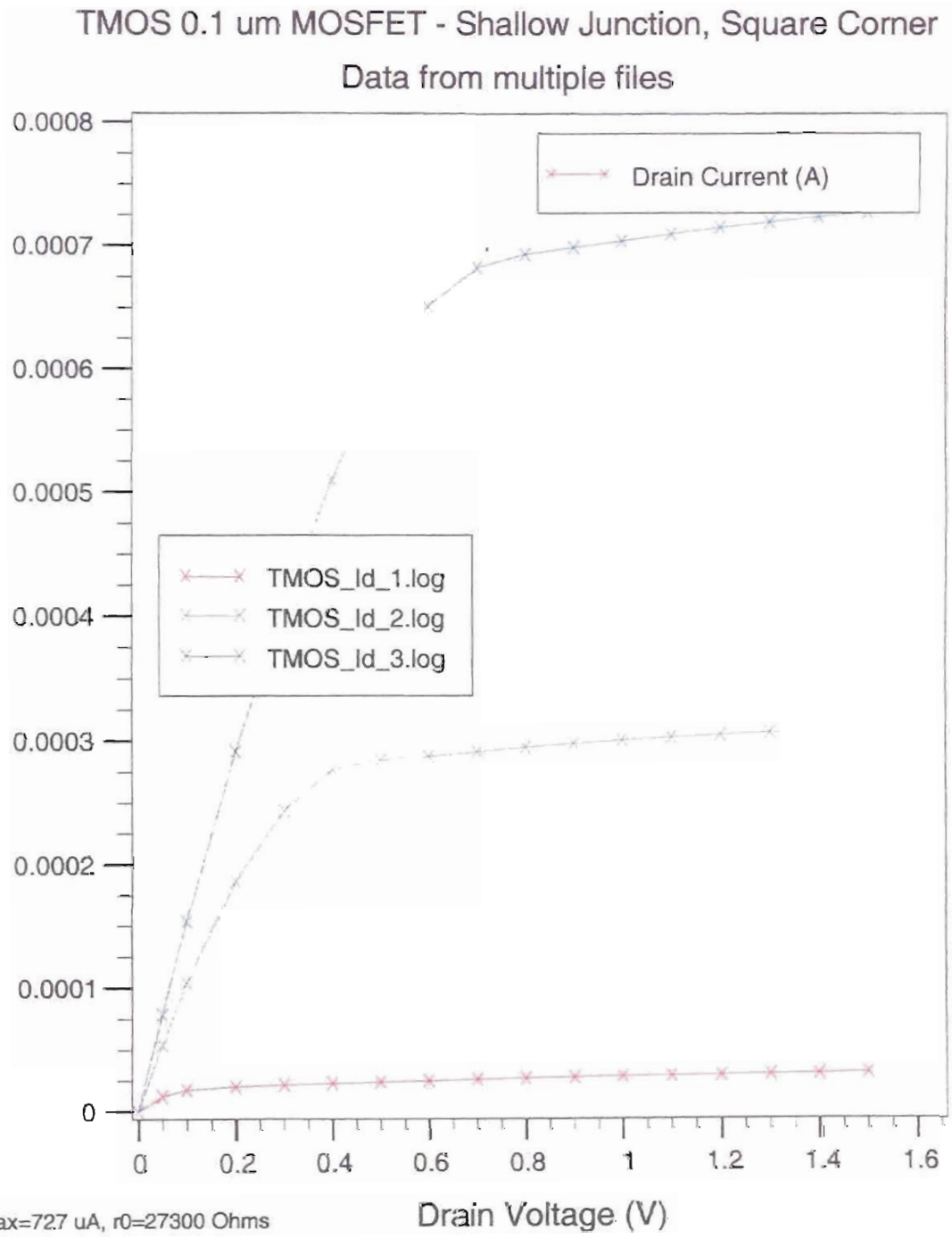

TMOS 0.1 um MOSFET - Deep Junction, Square Corner
Vd = Vg = 1.5 V
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0
0.1
0.2
0.3
0.4
0.5
Microns
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum
Leff = .108 um


TMOS 0.1 um MOSFET - Deep Junction, Square Corner
Vd = Vg = 1.5 V
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
Potential (V)
2.09
1.78
1.48
1.17
0.869
0.565
0.261
-0.0434
-0.348
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum
0
0.1
0.2
0.3
0.4
0.5
Microns
Leff = .108 um

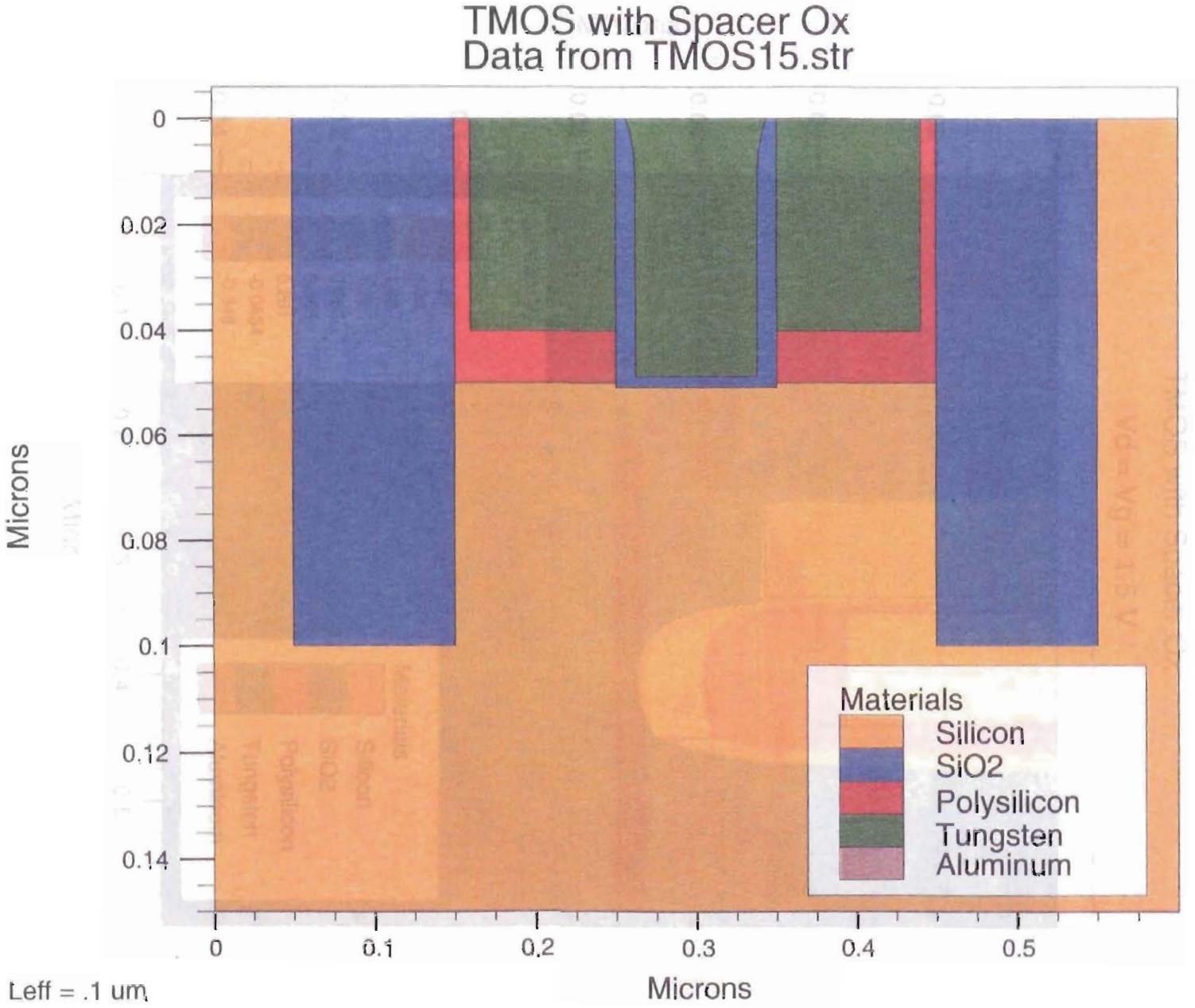

TMOS 0.1 um MOSFET - Deep Junction, Square Corner
Vg = 0, Vd = 1.5 V
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0
0.1
0.2
0.3
0.4
0.5
Microns
Potential (V)
2.09
1.78
1.48
1.17
0.869
0.565
0.261
-0.0434
-0.348
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum
Leff = .108


TMOS 0.1 um MOSFET - Deep Junction, Square Corner
DIBL = .0164 dVg/dVd, Vd=1.5-2.5, I=1e-4
Drain Current (A)
TDIBL_01.log
TDIBL_15.log
TDIBL_20.log
TDIBL_25.log
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Gate Voltage (V)

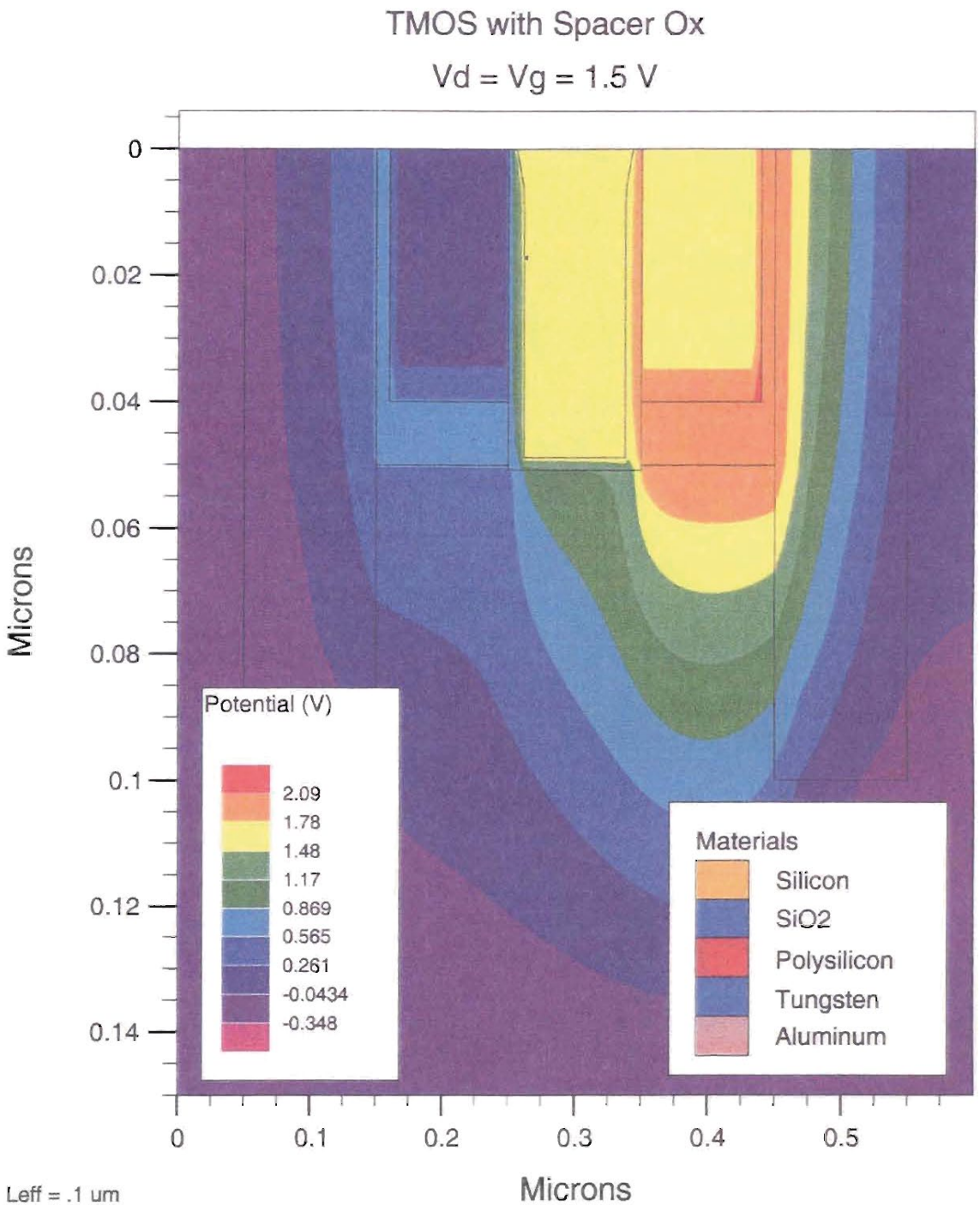

TMOS 0.1 um MOSFET - Deep Junction, Shallow Corner
Sub-threshold Current
Drain Current (A)
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
-13
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Idmin = 5.60e-12, Vt=.425V
Gate Voltage (V)
SwingST=.081

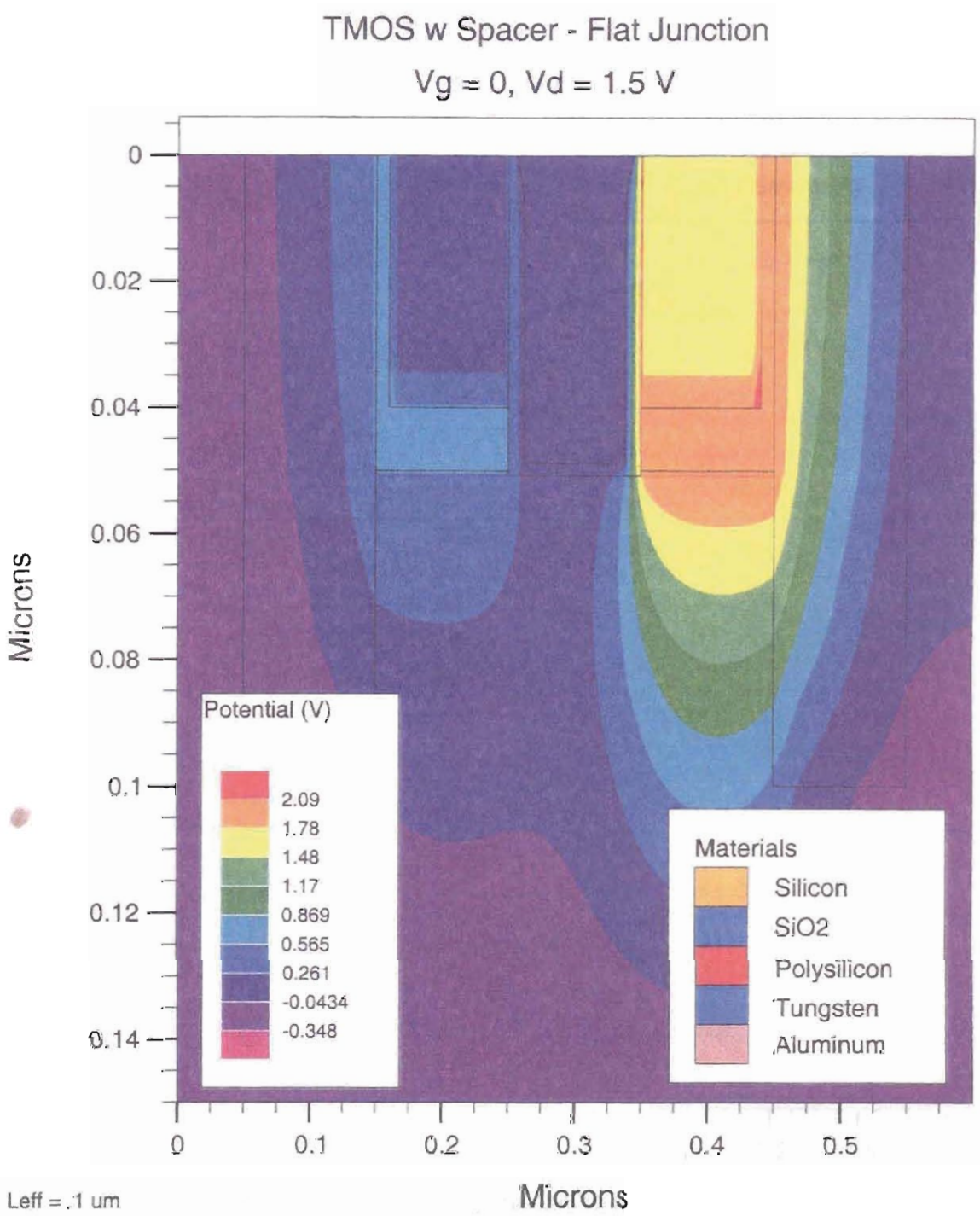

TMOS 0.1 um MOSFET - Shallow Junction, Square Corner
Data from multiple files
0.0008
0.0007
0.0006
0.0005
0.0004
0.0003
0.0002
0.0001
0
Drain Current (A)
TMOS_Id_1.log
TMOS_Id_2.log
TMOS_Id_3.log
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Idmax=727 uA, r0=27300 Ohms
Drain Voltage (V)

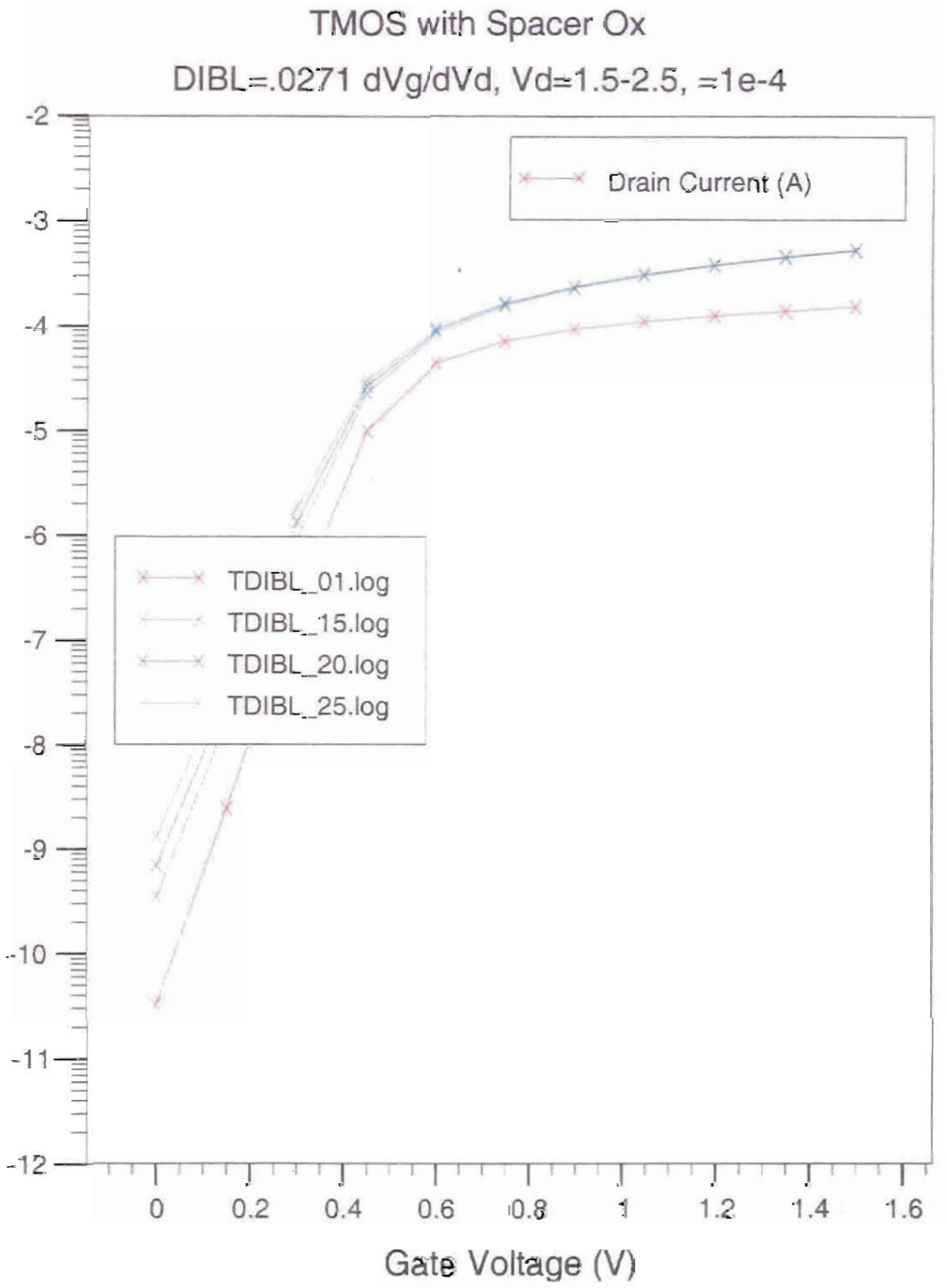
Appendix L. TMOS with Spacer Ox

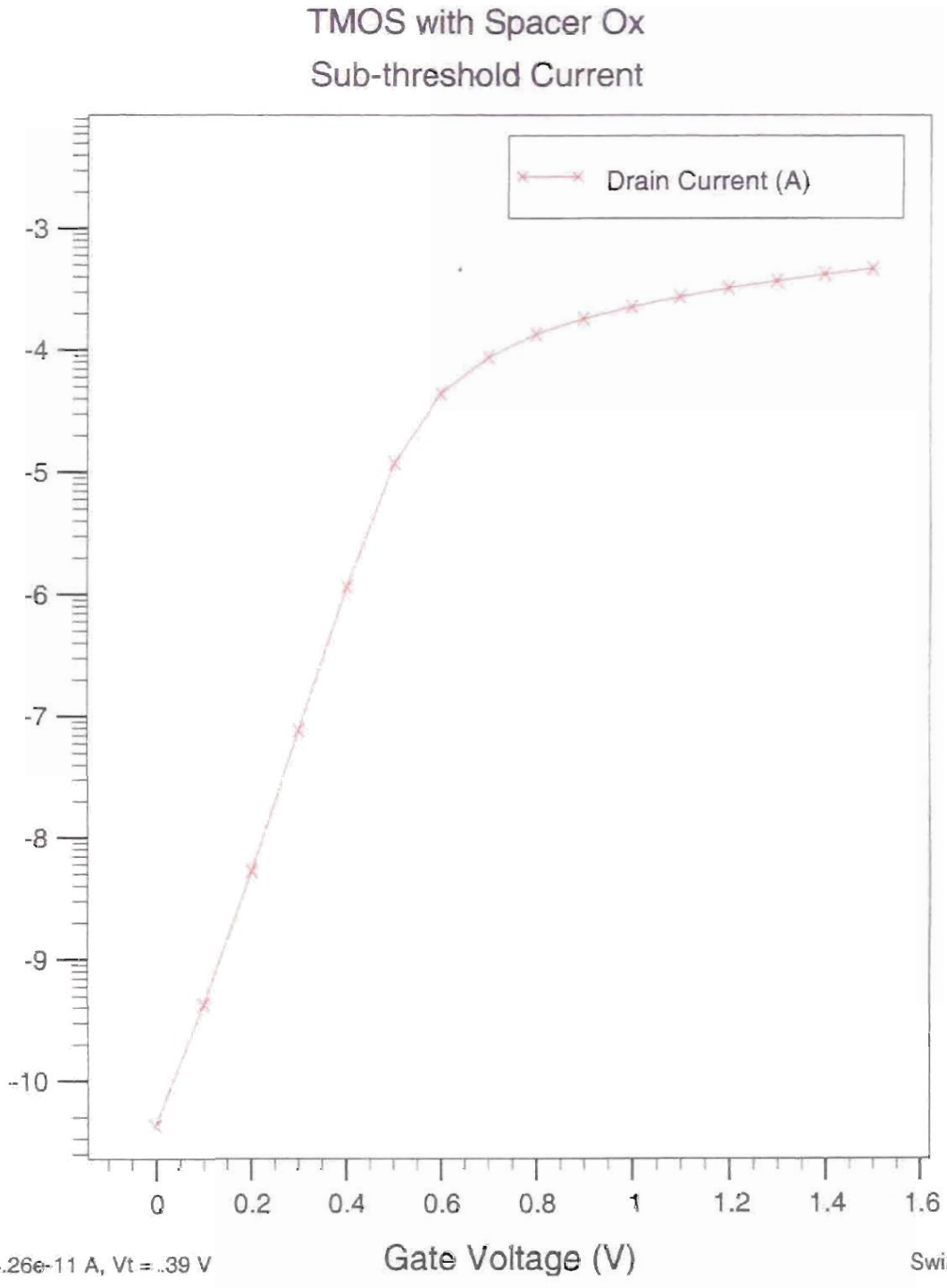

TMOS with Spacer Ox
Data from TMOS15.str
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0
0.1
0.2
0.3
0.4
0.5
Microns
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum

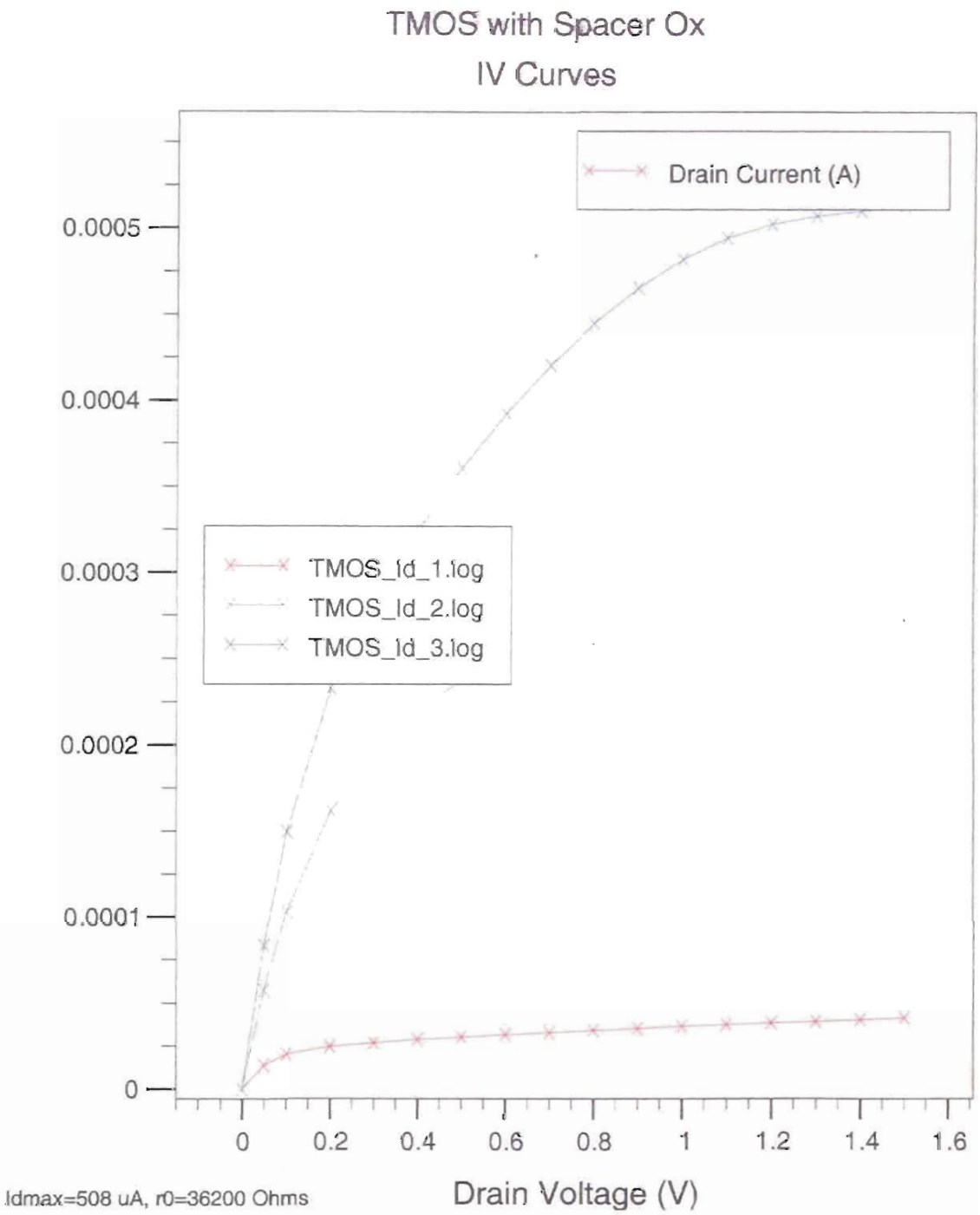
Leff = .1 um


TMOS with Spacer Ox
Vd = Vg = 1.5 V
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0
0.1
0.2
0.3
0.4
0.5
Microns
Potential (V)
2.09
1.78
1.48
1.17
0.869
0.565
0.261
-0.0434
-0.348
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum
Leff = .1 um

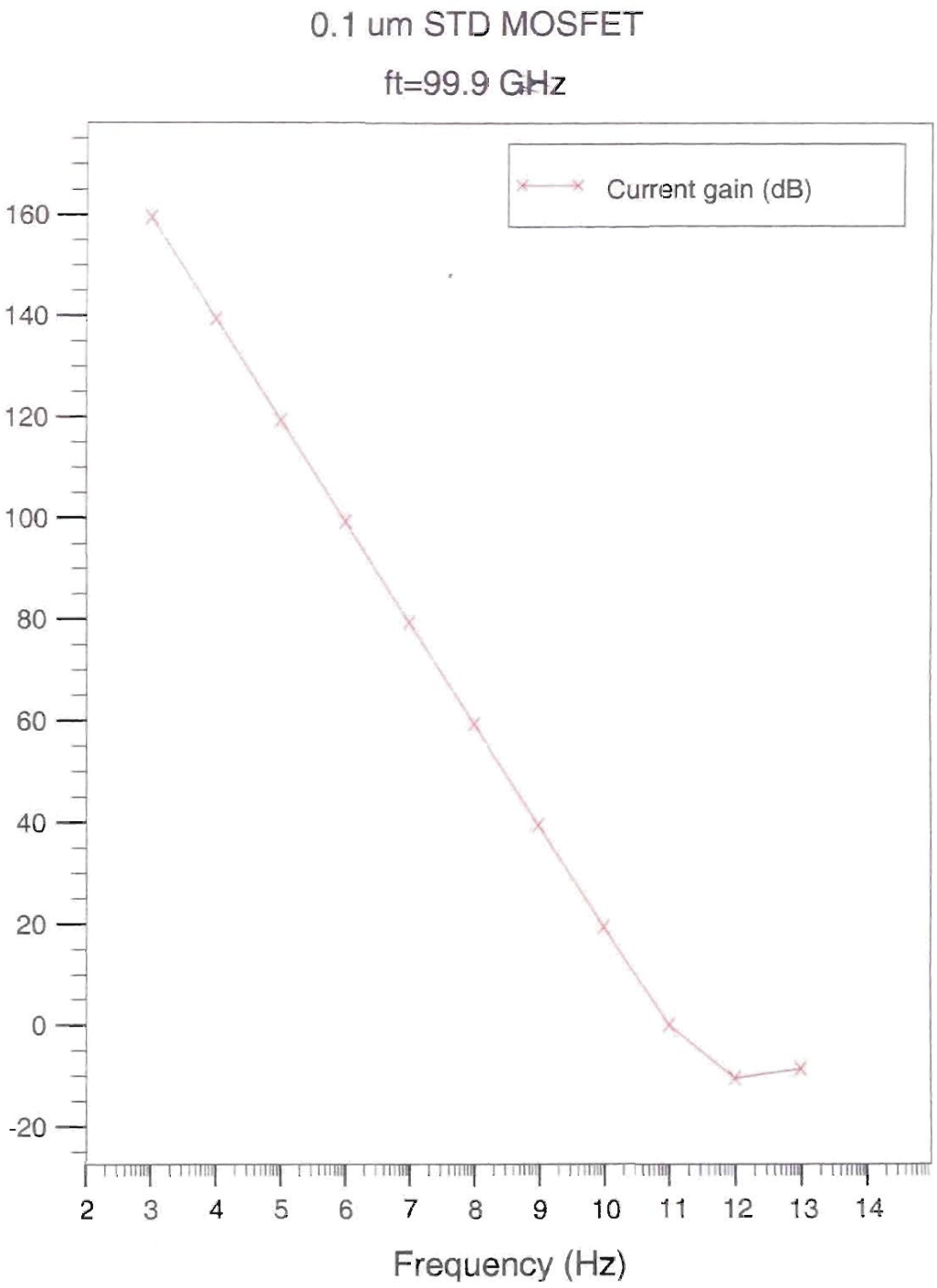

TMOS w Spacer - Flat Junction
Vg = 0, Vd = 1.5 V
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0
0.1
0.2
0.3
0.4
0.5
Microns
Potential (V)
2.09
1.78
1.48
1.17
0.869
0.565
0.261
-0.0434
-0.348
Materials
Silicon
SiO2
Polysilicon
Tungsten
Aluminum
Leff = .1 um

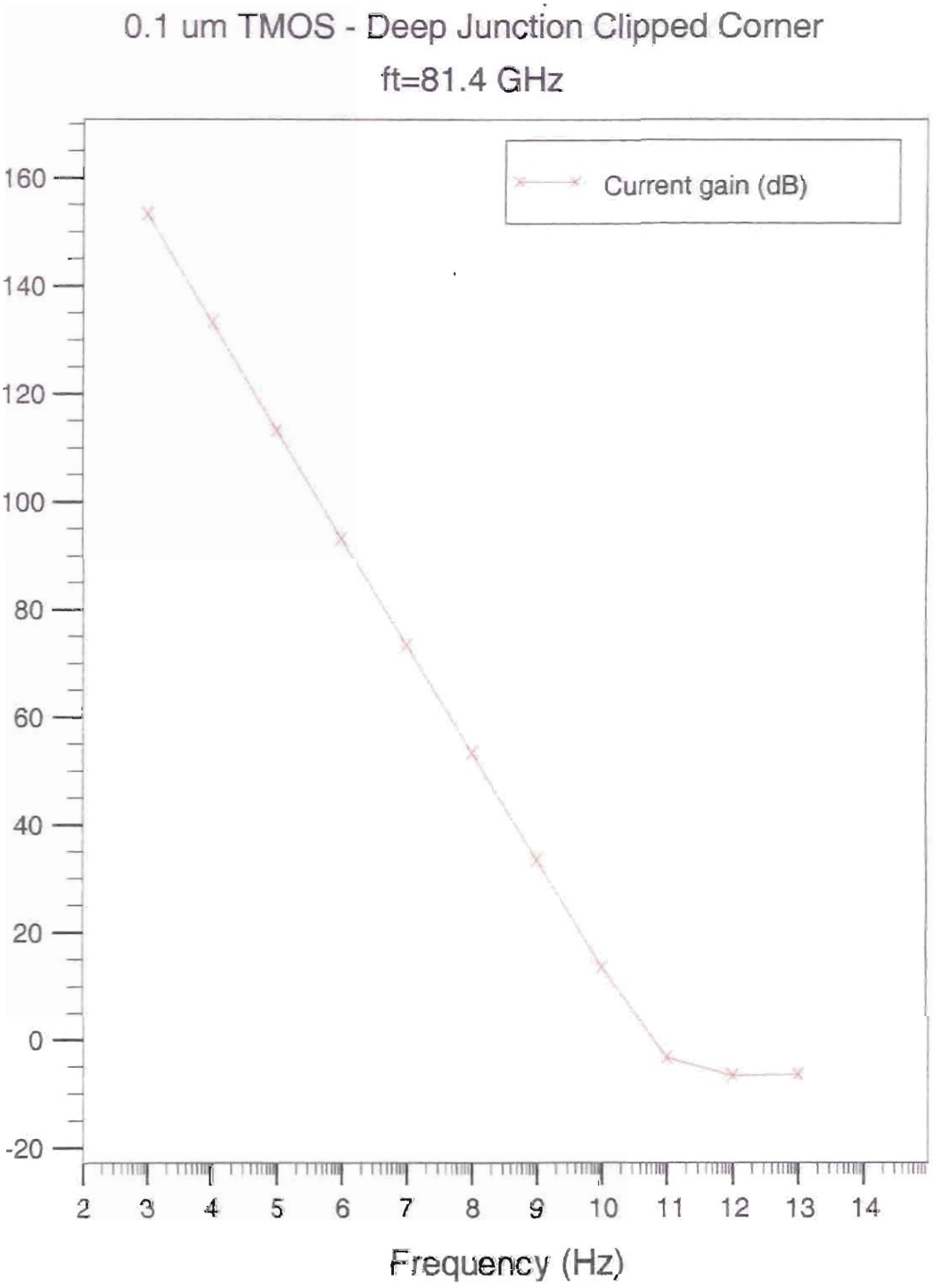

TMOS with Spacer Ox
DIBL=.0271 dVg/dVd, Vd=1.5-2.5, =1e-4
Drain Current (A)
TDIBL_01.log
TDIBL_15.log
TDIBL_20.log
TDIBL_25.log
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Gate Voltage (V)

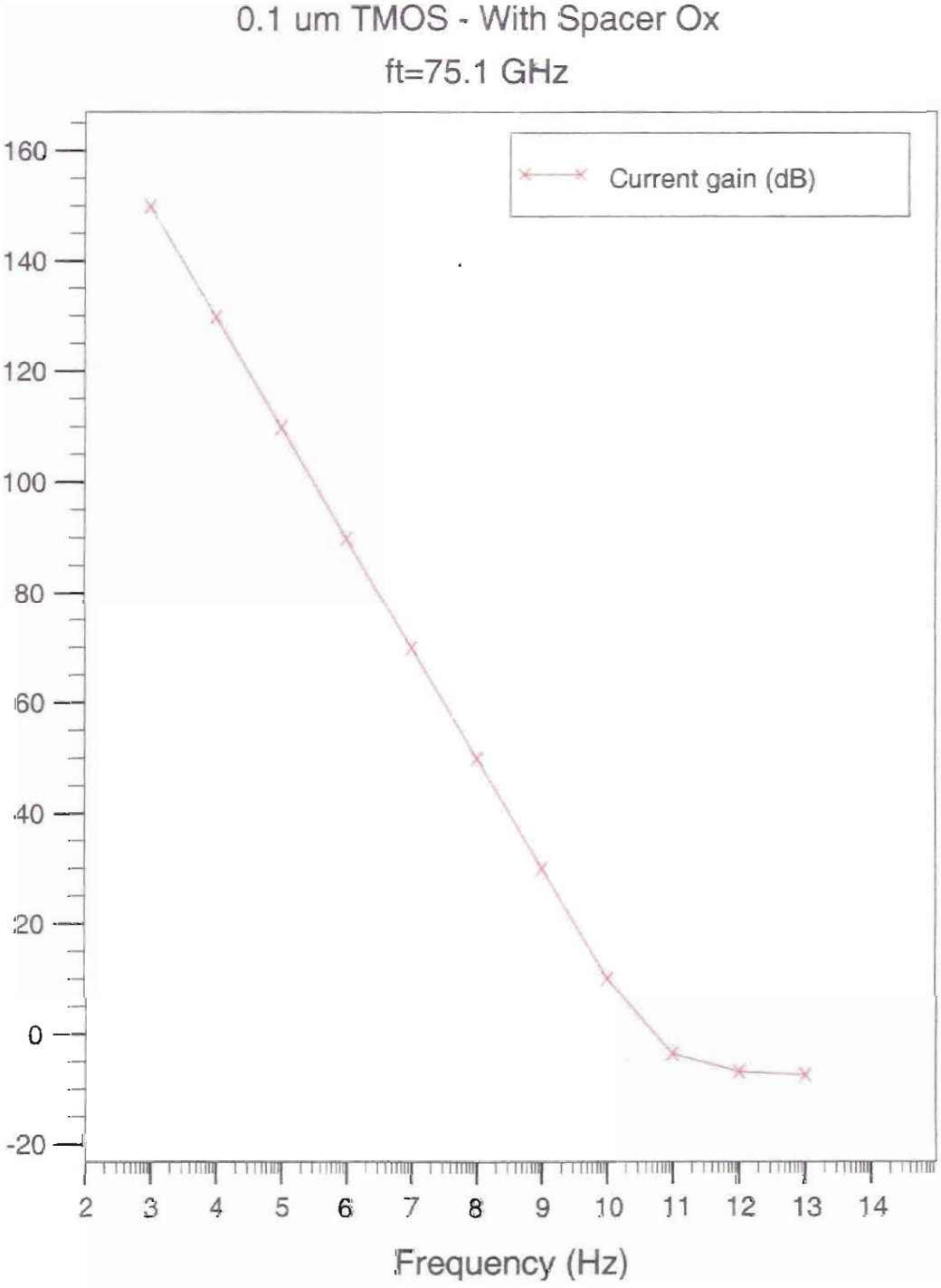

TMOS with Spacer Ox
Sub-threshold Current
Drain Current (A)
-3
-4
-5
-6
-7
-8
-9
-10
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Gate Voltage (V)
Idmin = 4.26e-11 A, Vt = .39 V
SwingST=.09


TMOS with Spacer Ox
IV Curves
Drain Current (A)
TMOS_Id_1.log
TMOS_Id_2.log
TMOS_Id_3.log
0.0005
0.0004
0.0003
0.0002
0.0001
0
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Drain Voltage (V)
Idmax=508 uA, r0=36200 Ohms

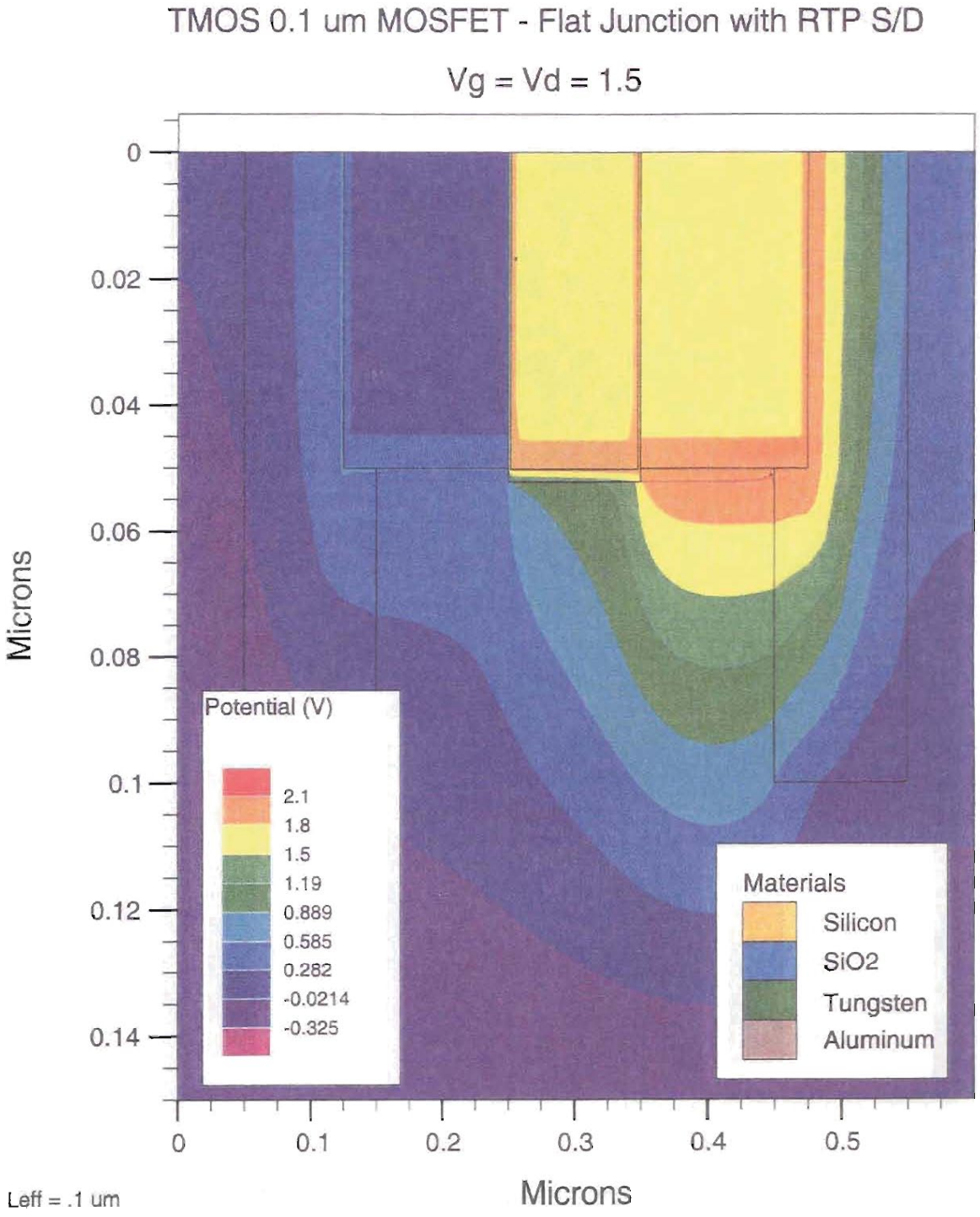
Appendix M. AC Simulations

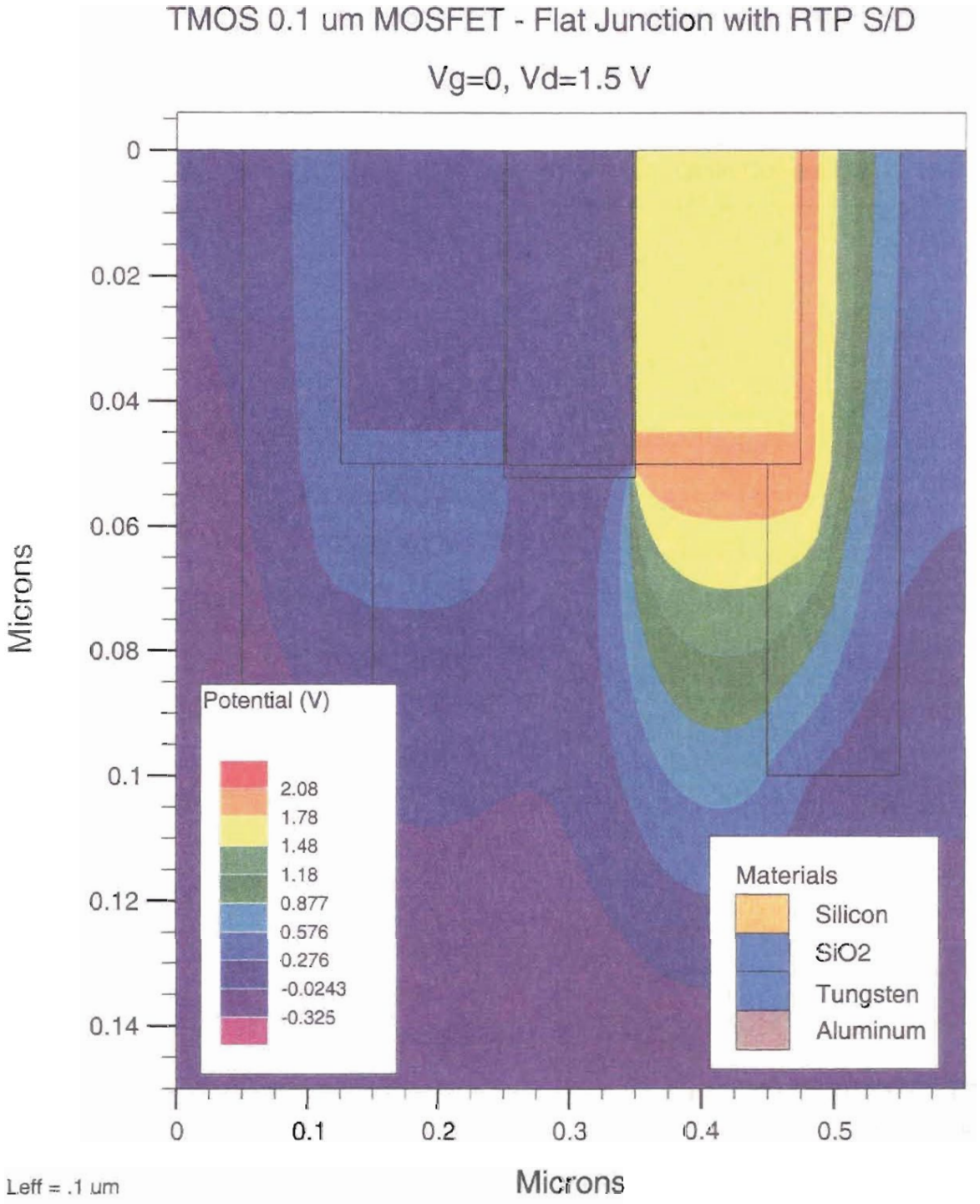

0.1 um STD MOSFET
ft=99.9 GHz
Current gain (dB)
160
140
120
100
80
60
40
20
0
-20
2
3
4
5
6
7
8
9
10
11
12
13
14
Frequency (Hz)

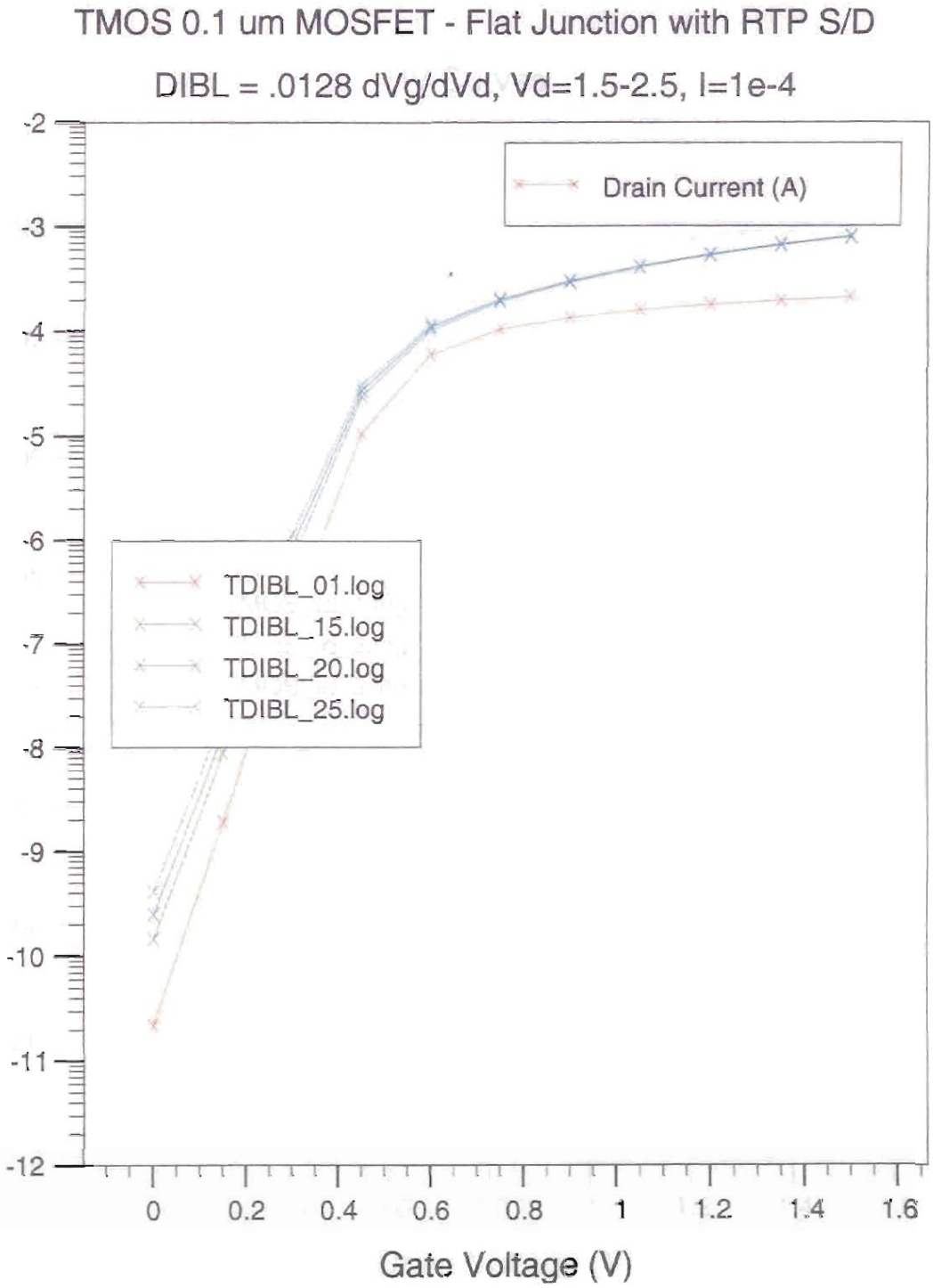

0.1 um TMOS - Deep Junction Clipped Corner
ft=81.4 GHz
Current gain (dB)
160
140
120
100
80
60
40
20
0
-20
2
3
4
5
6
7
8
9
10
11
12
13
14
Frequency (Hz)

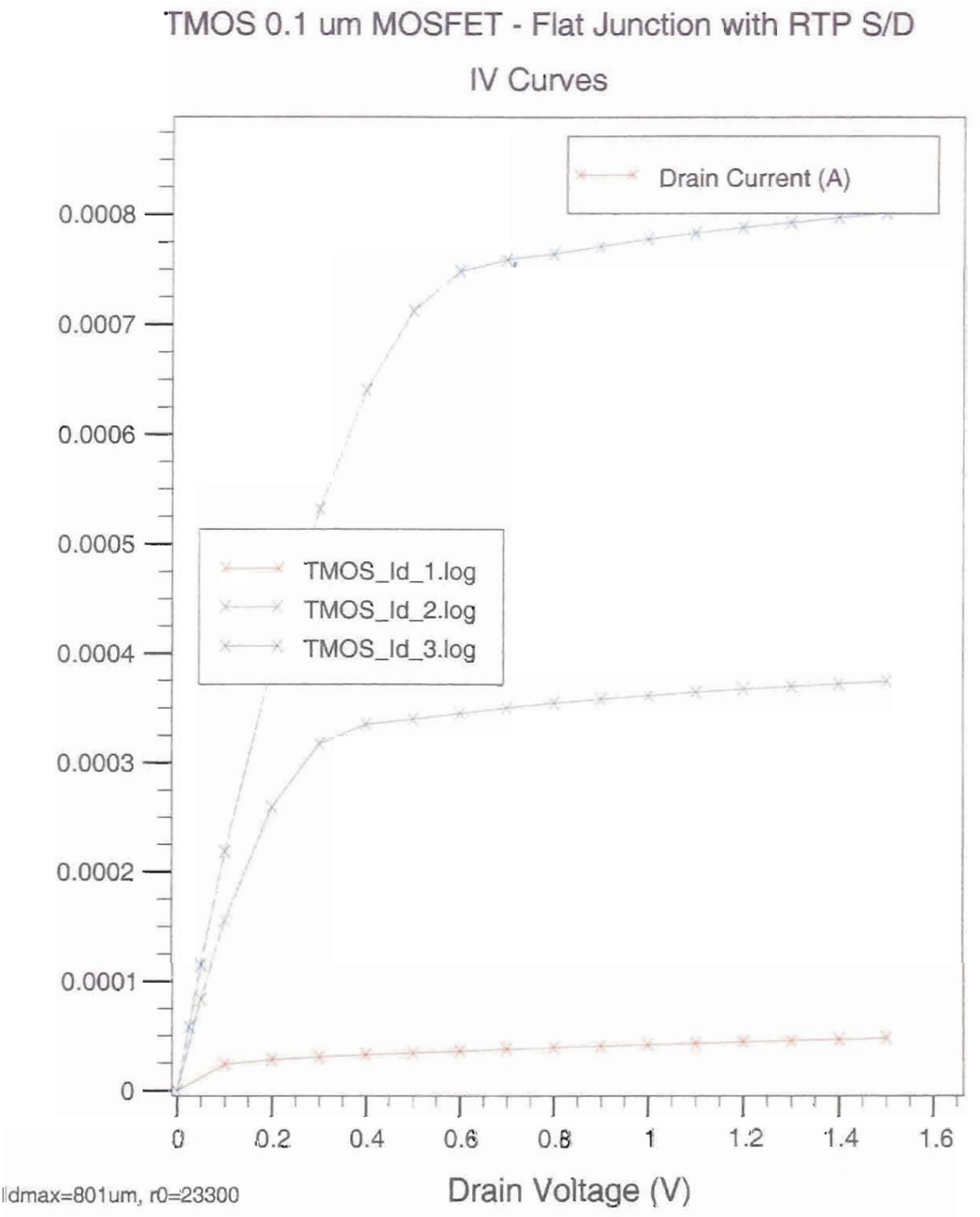

0.1 um TMOS - With Spacer Ox
ft=75.1 GHz
Current gain (dB)
160
140
120
100
80
60
40
20
0
-20
2
3
4
5
6
7
8
9
10
11
12
13
14
Frequency (Hz)

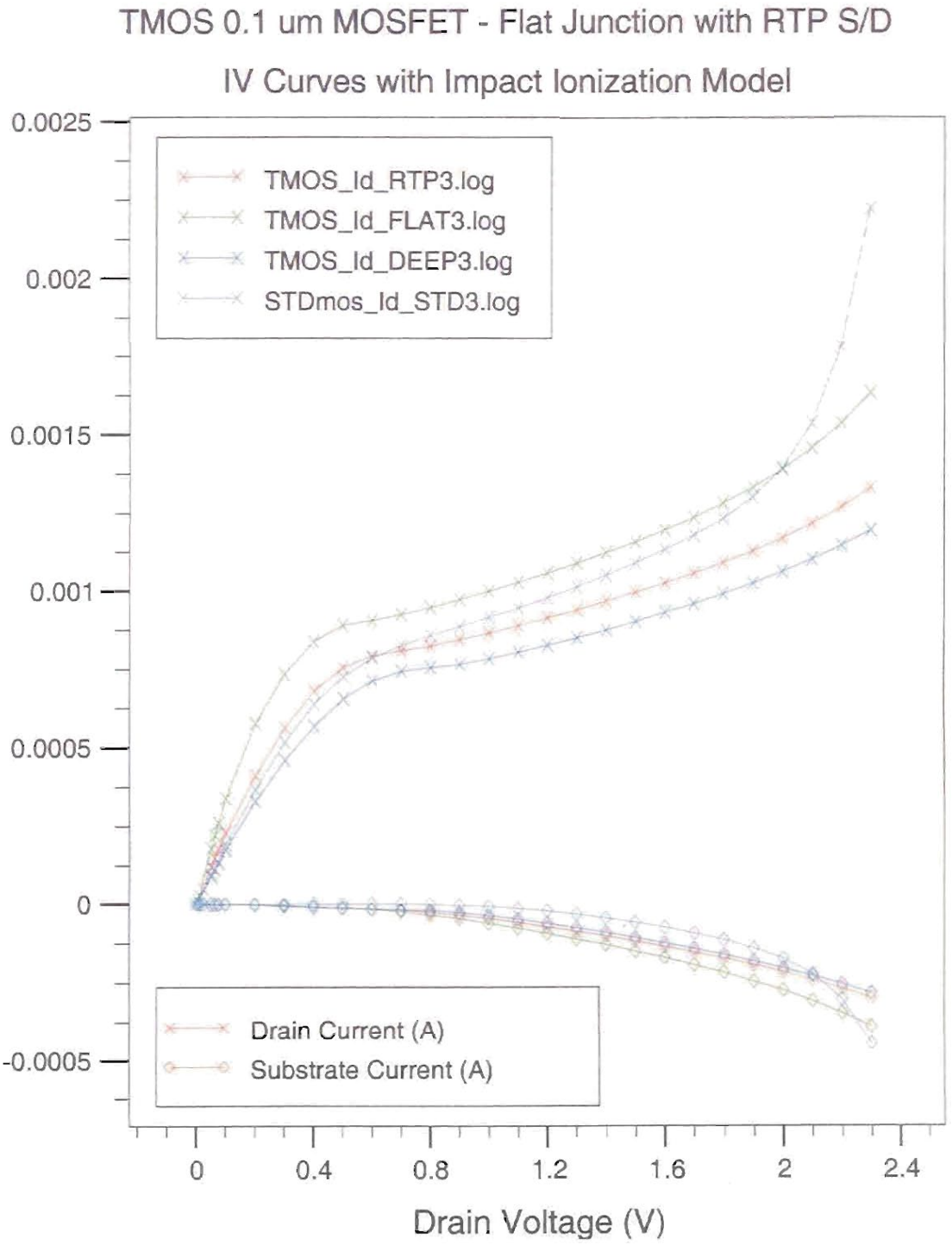
Appendix N. TMOS with RTP Junction (No Poly) .


TMOS 0.1 um MOSFET - Flat Junction with RTP S/D
Vg = Vd = 1.5
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
0
0.1
0.2
0.3
0.4
0.5
Microns
Potential (V)
2.1
1.8
1.5
1.19
0.889
0.585
0.282
-0.0214
-0.325
Materials
Silicon
SiO2
Tungsten
Aluminum
Leff = .1 um


TMOS 0.1 um MOSFET - Flat Junction with RTP S/D
Vg=0, Vd=1.5 V
Microns
0
0.02
0.04
0.06
0.08
0.1
0.12
0.14
Potential (V)
2.08
1.78
1.48
1.18
0.877
0.576
0.276
-0.0243
-0.325
Materials
Silicon
SiO2
Tungsten
Aluminum
0
0.1
0.2
0.3
0.4
0.5
Microns
Leff = .1 um


TMOS 0.1 um MOSFET - Flat Junction with RTP S/D
DIBL = .0128 dVg/dVd, Vd=1.5-2.5, I=1e-4
Drain Current (A)
TDIBL_01.log
TDIBL_15.log
TDIBL_20.log
TDIBL_25.log
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
-12
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Gate Voltage (V)


TMOS 0.1 um MOSFET - Flat Junction with RTP S/D
IV Curves
Drain Current (A)
TMOS_Id_1.log
TMOS_Id_2.log
TMOS_Id_3.log
0.0008
0.0007
0.0006
0.0005
0.0004
0.0003
0.0002
0.0001
0
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Drain Voltage (V)
Idmax=801um, r0=23300


TMOS 0.1 um MOSFET - Flat Junction with RTP S/D
IV Curves with Impact Ionization Model
TMOS_Id_RTP3.log
TMOS_Id_FLAT3.log
TMOS_Id_DEEP3.log
STDmos_Id_STD3.log
Drain Current (A)
Substrate Current (A)
0.0025
0.002
0.0015
0.001
0.0005
0
-0.0005
0
0.4
0.8
1.2
1.6
2
2.4
Drain Voltage (V)