METHODS AND CONSIDERATIONS FOR TESTING RESISTIVE MEMORIES

by

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ABSTRACT

Resistive random access memory (RRAM) has been the topic of many research papers in recent years, as companies begin to look for non-volatile alternatives to NAND Flash. The standard testing methodologies for single devices do not work for most of the RRAM technologies, so new methods must be developed. Parasitic capacitance will destroy the device under test without current compliance circuitry. A test structure with the capability to apply current compliance in either direction was designed, simulated, and tested with electrical results. Pulses greater than 4.0 V were delivered with 100 μA current compliance, and parasitic capacitance was kept below 50 fF.

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CHAPTER ONE – INTRODUCTION

1.1 NAND Background

Flash memory has been the mainstream non-volatile memory for several decades. Considered highly reliable, it has been used for non-archival storage for code and data. Flash memory gained adoption starting with the NOR architecture flash (NOR flash), which is optimized for random access suited for applications like code storage. NOR flash is used widely for computer basic input/output system (BIOS), cell phones, set top boxes, and other embedded applications that utilize its execute in place (XIP) capability. In recent years, NAND architecture flash (NAND flash) has become the dominant form of flash memory, with an architecture that is best suited for large amounts of data. With long access times and large data pages, NAND flash is not adept at XIP applications, but excels at mass storage applications such as solid state disk drives (SSD), USB drives, and memory cards. The low power per bit required for programming and erase enables NAND flash to support page sizes up to 8 kB, which allows high data throughput despite long access latencies.

Recent consumer demand for increasing storage in music players, smart phones, tablet computers, as well as beginning adoption of SSD's in notebook computers have all increased the market for NAND flash memory. Recent iSuppli data shows the NAND flash market to be a $22 *B* market for 2011, and projected to be a $25 *B* market by 2014 [1].

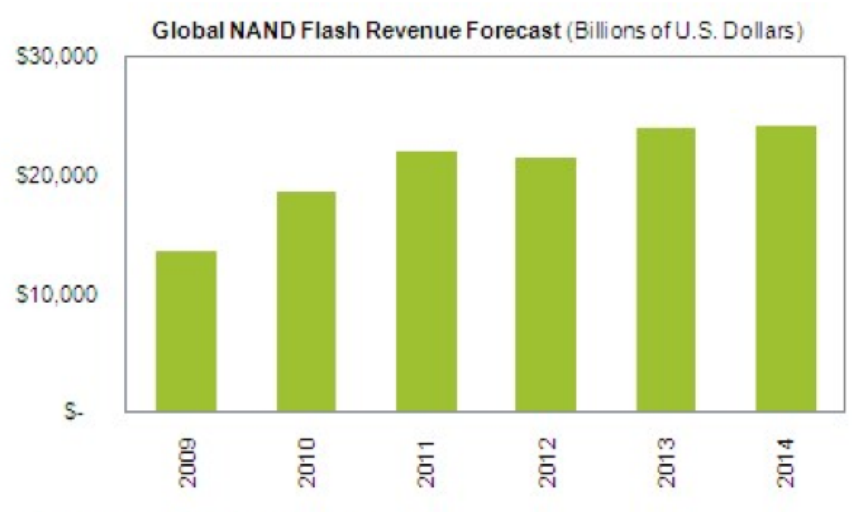


Figure 1 NAND Market for 2009-2014 [1]

Low cost per bit has long been the advantage of NAND flash over NOR flash. Starting with the architecture, NOR requires a contact per 2 bits, which requires more area. Memory cell area is usually given in terms of "features size" (F), where the feature size is half of the pitch that is supported by the most advanced masking layer (typically the bitline pitch). This allows a comparison of different technologies to give a relative cost potential, with the most cost effective memory having a lower feature squared area (F^2). NOR has a cell size of ~8 F^2 (Figure 2(b)), where NAND is ~4.5 F^2 (Figure 2(c)). The "ideal" memory has a cell area of 4 F^2, which is essentially a wordline (WL) crossing a bitline (BL) per cell, and is shown in Figure 2(a). Most memories today are comprised of a single layer, but some new memories can be built in multiple layers, one on top of another, allowing less than 4 F^2 per bit, by stacking multiple bits in the same silicon area. Multi level cell technology (MLC) enables NAND flash to store up to 4 bits of logical data in 1 physical cell, enabling even lower cost per bit [2, 3]. Aggressive pitch multiplication techniques [4] enable further cost reductions, by scaling the cell faster than direct print photolithography equipment allows. In 1965, Intel's Gordon Moore observed

what has come to be known in the industry as "Moore's law," that the number of transistors on an integrated circuit will double approximately every 18 to 24 months [5]. This was first applied to logic chips, and later extended to memories, as doubling in density every 18 months due to the very periodic and dense nature of memory arrays. The combination of the previously mentioned techniques allows NAND flash to scale much faster than other memory and logic devices, with a doubling of density every 12 months. The President and CEO of Samsung's Memory Division observed this fact and called for a new memory growth model for the highest density memories like NAND [6].

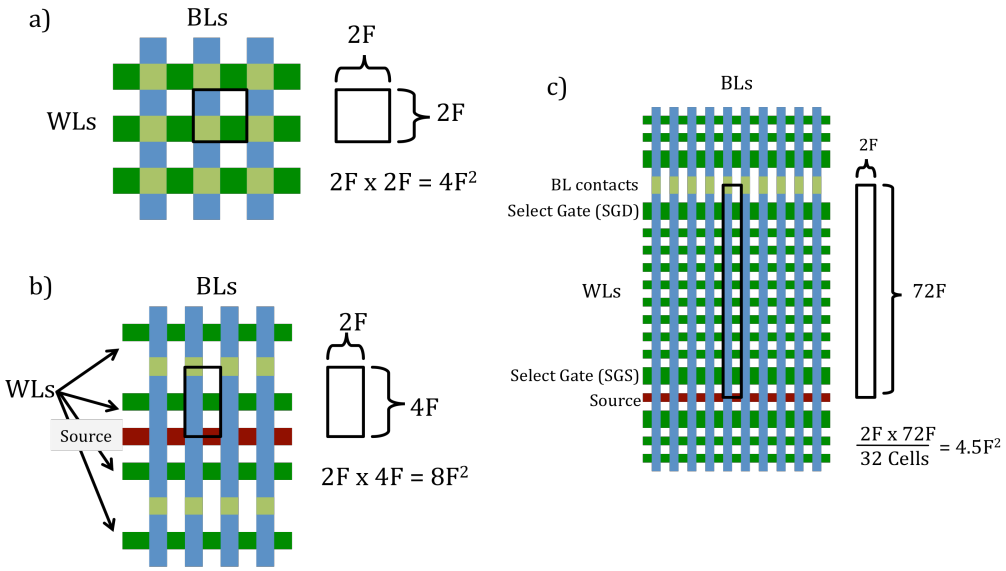


Figure 2 Array Architectures in Terms of Feature Size

Because of this aggressive scaling of NAND flash, there are many challenges that must be overcome. Tunnel oxide thickness is essentially constant, so programming and erase voltages do not scale with the cell size. As the cell gets smaller, so does the distance between cells. With > 20 *V* required for programming, a 20 *nm* cell/space will have > 10 *MV/cm* across it, causing near instantaneous breakdown, so care must be taken never to allow full programming potential across lines at the smallest dimension. Even

the charge stored on the floating gate (FG) of one cell is close enough to the neighbor cell to cause significant interference. This effect called FG-FG interference was observed at the 72 *nm* node, and has required many innovations to successfully mitigate its effects [7]. Other effects, such as random telegraph noise (RTN), program verify sigma (PVS) and others continue to have an increasingly significant impact on operating window with each successive generation [7].

The cumulative effect of the scaling challenges in conjunction with the accelerated scaling path is that NAND flash is fast approaching the scaling limit of the present floating gate technology. Future generations of NAND will likely see some evolutionary changes in the NAND flash architecture. The industry is planning a change from a planar NAND device to a vertical NAND string, a so-called "3D" NAND flash, one example of which is shown in Figure 3 [8]. However, such efforts are likely to be short lived, as the vertical string requires high aspect ratios and additional processing cost per wafer, which eventually makes adding layers non-cost competitive. In the next 5-10 years, we are likely to see NAND flash stop scaling at least at the historical rate, and see another type of memory emerge as the non-volatile memory of choice.

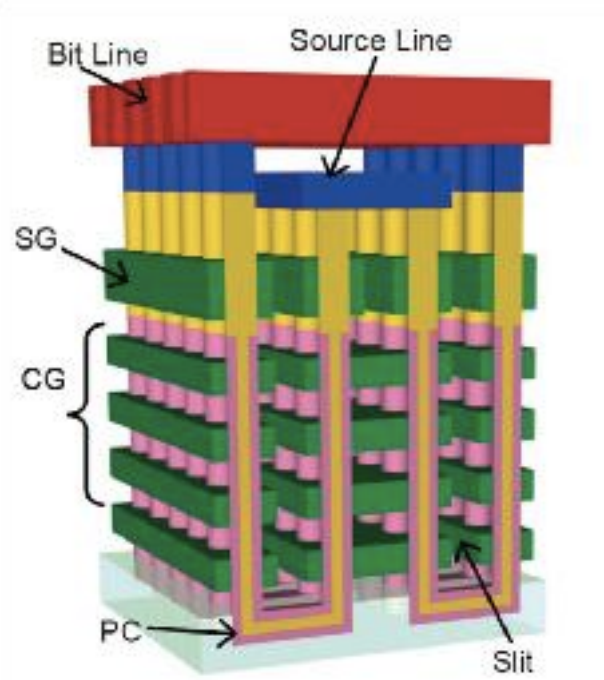


Figure 3 Toshiba P-BICS 3D-NAND Technology [8]

1.2 RRAM

One such class of memory is the resistive random access memory element, or RRAM. RRAM is not a specific memory technology, and has been used by many people to discuss emerging technologies with various different definitions. For the purpose of this work, the RRAM definition will be a class of 2 terminal devices that change resistance according to various stimuli applied to those terminals. By classifying RRAM so broadly, one can encompass a wide range of devices driven by a variety of physical mechanisms. In testing these devices, similar considerations must be taken, so it is useful and appropriate here to make such a broad classification. This work will attempt to classify the various RRAM devices seen in the literature by their physical mechanisms, where such information is known. The reader who is familiar with the subject will recognize that in many cases there is some ambiguity surrounding the exact physical

mechanism and model, so although the categorization will be imprecise, it is still useful for discussion. A summary table of the characteristics of the different RRAM options is shown below in Table 1.

1.3 Definitions

All the RRAM devices discussed in this work are capable of the most basic requirement of a memory, the ability to change the resistance of the material between two states. The more conductive state is called the low resistance state (LRS), and the less conductive state is called the high resistance state (HRS). The initial state of the device as it is fabricated before any electrical stimulus may be in the LRS or HRS, or somewhere in between depending on a variety of factors. Some devices require electrical stimulus called "forming" before they will switch reliably between states. Other devices do not require forming, but can begin switching immediately after they are fabricated.

Switching states in an RRAM device requires different terminology than is presently used on NAND floating gate devices. Floating gate devices have an erased state, which is achieved by an erase operation, and a programmed state, which is achieved by a program operation. The erased state is the higher conductive state (or lower V_{TH}), and a "1" is read out of the memory by convention, indicating current flow greater than the threshold of the sense amplifier. The programmed state is the lower conductive state (or higher V_{TH}), and a "0" is read out of the memory for this state. The floating gate in a NAND device is used to store electrons, and during the programming operation, additional electrons are added to the floating gate, increasing the Vth. During the erase operation, those electrons are removed from the floating gate, lowering the Vth.

The convention for switching an RRAM device has been carried over from phase change memory (PCM), and this work will use the same definitions. Switching from a HRS to LRS is called SET, and switching from the LRS to HRS is called RESET.

Although the physical mechanism of switching between states varies for different RRAM devices, switching must be accomplished by applying either a positive bias to the terminals, or a negative bias to the terminals. Those devices that switch between states by applying positive and negative bias are called "bipolar", while those devices that require only one bias are called "unipolar". As will be seen later, bipolar devices are more difficult to integrate into dense arrays.

As with NAND, the read operation of an RRAM device is non-destructive, as long as proper biasing is applied. That means that the state of the memory cell is preserved from read to read, so data does not need to be written back into the cell, like a DRAM requires. Read is accomplished by biasing the device at a lower voltage than SET and RESET and measuring the current. If the read bias is too high, a disturb to the SET or RESET state can occur, so proper biasing is critical during the read of an RRAM device.

1.4 Cell Options

1.4.1 PCM

The most mature RRAM technology to date is phase change memory (PCM). Companies such as Samsung, Hynix, and Micron have announced they are selling memories based on this technology, albeit in limited quantities. The structure of the device is a chalcogenide such as $Ge_2Sb_2Te_5$ (GST) that changes phase from amorphous to crystalline. In the crystalline state, the more ordered structure of the material has less

resistance to electron flow, and so has a lower resistance (LRS). In the amorphous state, the material is less conductive, and so has a higher resistance (HRS). A high resistance state (HRS) PCM bit is shown in Figure 4. The physical mechanism has been studied extensively and is well known. PCM is one of the few unipolar memories, which requires bias in only one direction for both SET and RESET. Both SET and RESET operations begin the same way, by biasing the device and passing enough current to melt the phase change (i.e. GST) material. The phase change material is typically deposited over a heater that is responsible for generating the heat to melt the material. Once melted, a slow cooling will produce a crystalline dome over the heater during the SET operation. A fast quench from the melted state will return the material to an amorphous state during the RESET operation. The initial state of the material as it is fabricated is the LRS, since the GST comes out of the fab in the crystalline state [9, 10].

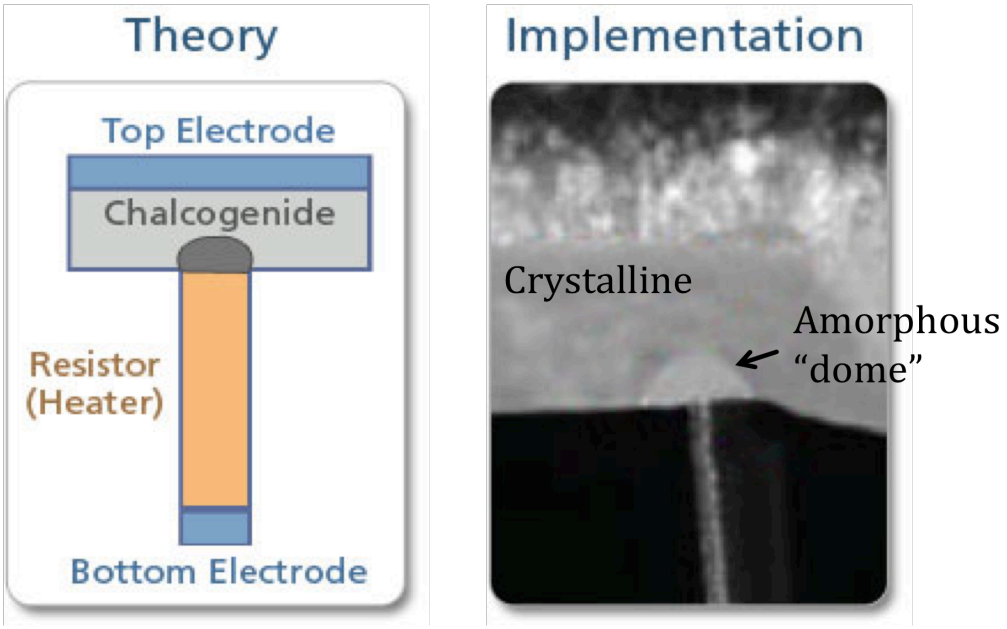


Figure 4 PCM Bit in the Amorphous State [11]

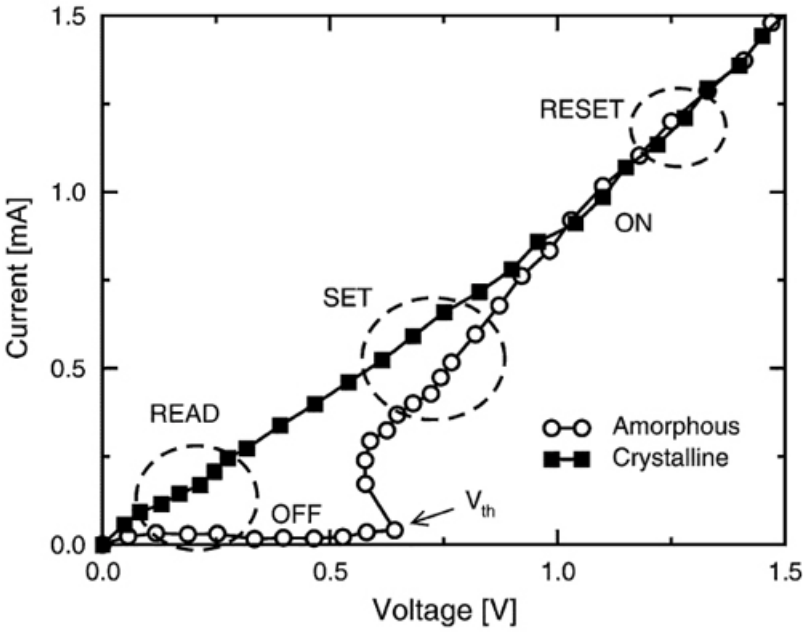


Figure 5 PCM DC I-V [12]

1.4.2 CBRAM

Another widely explored category of device is the conductive bridge RAM, or CBRAM. This category includes work done by Kozicki (called "programmable metallization cell", PMC) at Arizona State Univeristy, as well as companies like Qimonda, and Sony [13, 14]. A PMC cell drawing is shown in Figure 6 and the corresponding DC I-V charateristic sweep is found in Figure 7. Each cell may have some differences, but also some commonalities. These devices have a conductive, mobile metal, such as silver or copper over an insulator. In the case of Kozicki and Qimonda, silver is placed over amorphous GST. In the case of Sony, copper in the form of copper telluride (CuTe) is placed over gadolinium oxide (GdO). Initially, the device is in the HRS, since the metal is present only in a layer above the insulator, and little current flows. Forming bias is required on these cells to move the metal ions from the layer above the insulator down in the insulator itself to form a conductive bridge (or filament)

through the insulator. After forming, the device is in the LRS, and can be RESET to the HRS by applying a reverse bias, generally at a very low voltage to partially dissolve the conductive bridge and move the metal ions back into the metal layer. A subsequent SET operation will bias the cell in the forward direction, and re-build the bridge to put the cell in the LRS. The SET operation is in the same direction as forming, but is done at a lower voltage, since the initial bridge is only partially dissolved by the RESET operation. During the forming and SET operations, some form of limiting the current is essential. When the conductive bridge forms, the diameter of the bridge is determined by the current flow through the bridge. As the diameter of the bridge increases, the resistance of the bridge decreases, and more current flows, causing a positive feedback. Without the limiting of current, the bridge will be burned up by the excessive current flow [15].

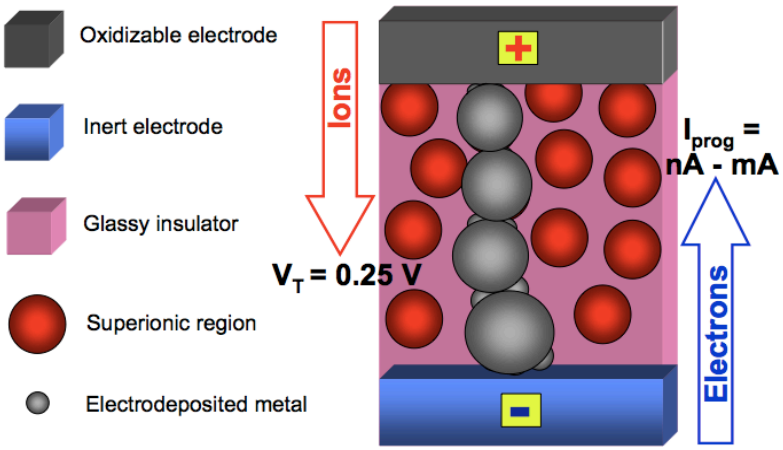


Figure 6 CBRAM Memory Cell (PMC) [14]

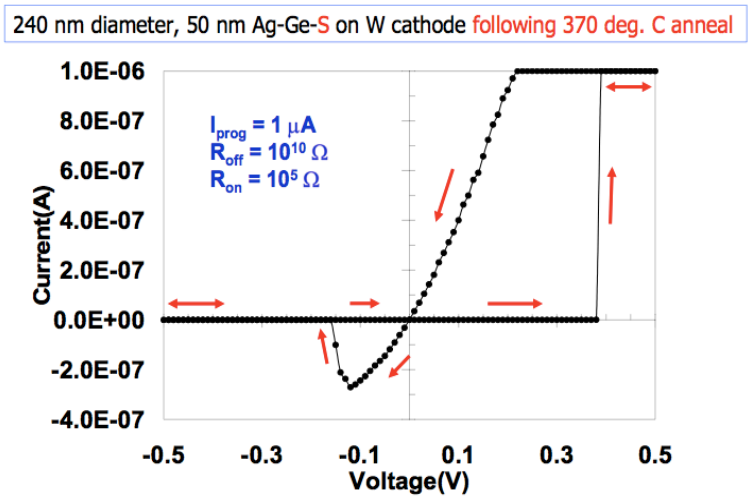


Figure 7 CBRAM DC I-V Characteristic (PMC) [14]

1.4.3 Binary Oxide RAM

One of the most common classes of RRAM is the binary oxide. A binary oxide is a two-part oxide, generally of a transition metal and oxygen. These are by far the easiest to create and look at, since simple oxidation of a metal is all that is required, and many metals that are commonly used in modern processes have switching characteristics. There is much literature on these binary oxides, studying various degrees of operation. Common binary oxides are HfOx, TiOx, TiON, ZrOx, etc. There has been much excitement in some circles about the work that HP is doing on memristors, work being done on a titanium dioxide cell [16]. Initially, the binary oxide is insulating, so the cell is in the HRS state. The switching mechanism for the binary oxides is filament formation, which is driven by a combination of field, current and heat. Typically, the oxygen ions in the oxide re-arrange to form a string of oxygen vacancies, which then changes the cell to a LRS. The characteristic curve of a binary oxide cell indicates that it is similar to the CBRAM, where a conductive filament is created and dissolved. Binary oxides require a

forming step, where a filament is first created. The subsequent RESET operation will dissolve a portion of the filament to return the device to a HRS. The SET operation re-forms the filament returning the device to the LRS. Like CBRAM, binary oxides require current compliance on the forming and SET operations, since they have similar positive feedback mechanisms. Most binary oxides can function in bipolar operation, although some have the unique property of being able to function as both a bipolar and unipolar device. The unipolar operation uses a lower voltage longer pulse to SET the device and form the filament, and a short higher voltage (and current) pulse to burn out a section of the filament and RESET the device.

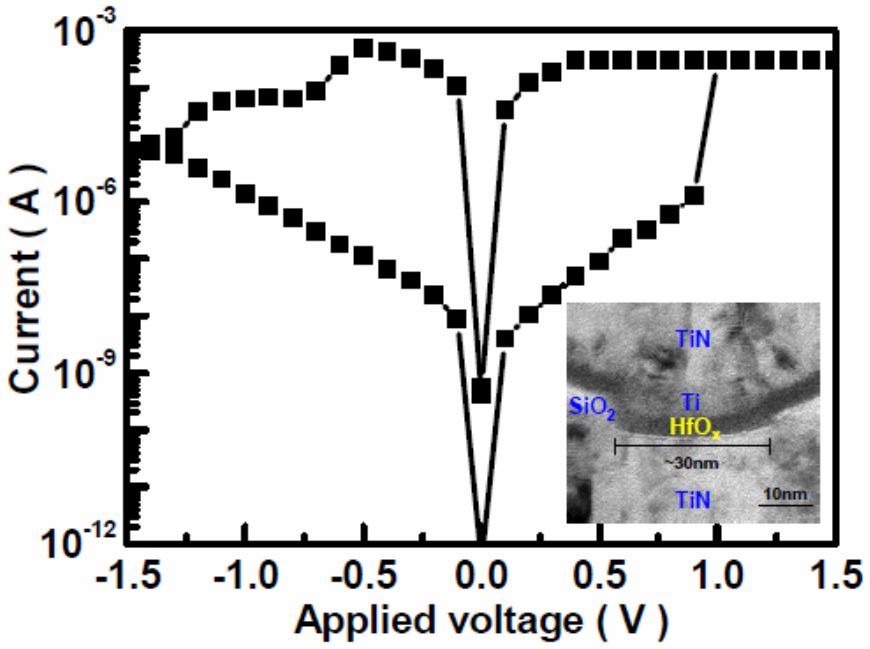


Figure 8 Binary Oxide DC I-V and Cell (inset) [17]

1.4.4 MVO

Another interesting category of RRAM is the multi-valence oxide (MVO). These oxides allow the movement of oxygen under an electrical bias, and therefore take or give up oxygen ions and change valence states. The makeup of the oxide determines its electrical conductivity. One such common oxide is a perovskite called PrCaMnO (PCMO). Note that although PCMO shares several letters with PCM, phase change memory, they are completely unrelated. Several startup companies such as 4DS, Adesto, Unity Semiconductor, as well as research institues like GIST, have investigated the use of MVO's as memories [18]. Although all use a multi-valence oxide, the memory mechanism may be unique to each case. Some have claimed an oxidation-reduction of a reactive electrode like aluminum, while others talk about the conductivity of the MVO itself changing. Unity has a unique approach, using a conductive metal oxide (CMO) and an insulating metal oxide (IMO) layered device that moves oxygen ions into and out of the IMO, changing the barrier height, and therefore the conductivity of the device. For these devices, no forming appears to be necessary. The presence of a forward bias moves oxygen in one direction for a SET. The reverse bias moves oxygen in the other direction for a RESET. The MVO devices all function in a bipolar manner, since an electric field is required in both directions.

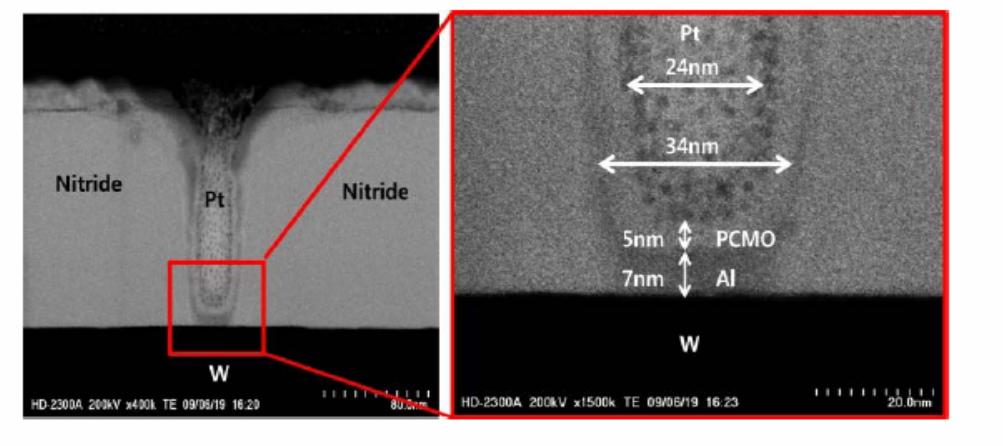


Figure 9 MVO Cell (PCMO) [18]

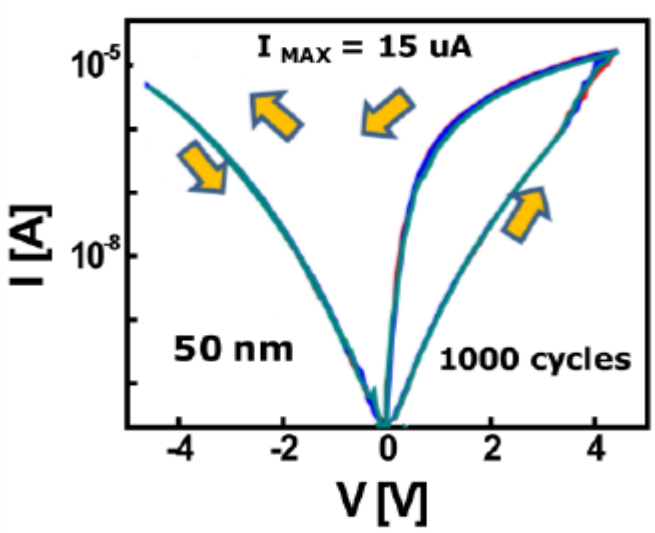


Figure 10 MVO DC I-V (PCMO) [18]

1.4.5 STTRAM

The last class of RRAM that will be discussed is one that is generally categorized on it's own, not as an RRAM. The class of magnetic random access memories, or MRAM is broad, and is also very mature with varying companies offering products based on magnetic memories. Recently, one variation that is most suitable as an emerging technology has begun to gain ground. Spin-torque transfer RAM, or STTRAM is a magnetic memory that uses the spin of electrons to change a magnetic layer in the device,

allowing a change of resistance [19]. STTRAM devices are composed of multiple layers, with a fixed magnetic layer, and a free magnetic layer that can change magnetic field orientation. When the fixed and free magnetic layers have magnetic fields oriented in the same direction (parallel), the device is in the LRS, and conducts the most current. When the fixed and free magnetic layers have magnetic fields oriented in opposite directions (anti-parallel), the device is in the HRS, and conducts less current. Initially, the devices are generally in the LRS, since the magnetic material is annealed in a magnetic field, aligning the internal fields. No forming is needed for STTRAM devices. A SET operation will pass current through the fixed magnetic layer, which acts as a filter to only allow electrons with a certain spin to pass through. The spin of these electrons hitting the free magnetic layer exerts a torque on that layer, causing it to flip magnetic field direction. The fixed and free magnetic layers have magnetic fields that are in the same direction, changing the device to the LRS. A RESET operation reverses the current flow, and the backup of electrons of the wrong spin polarity exert a torque on the free layer which then causes it to flip magnetic field direction so that the fixed and free magnetic layers are in opposite directions, changing the device to the HRS [20].

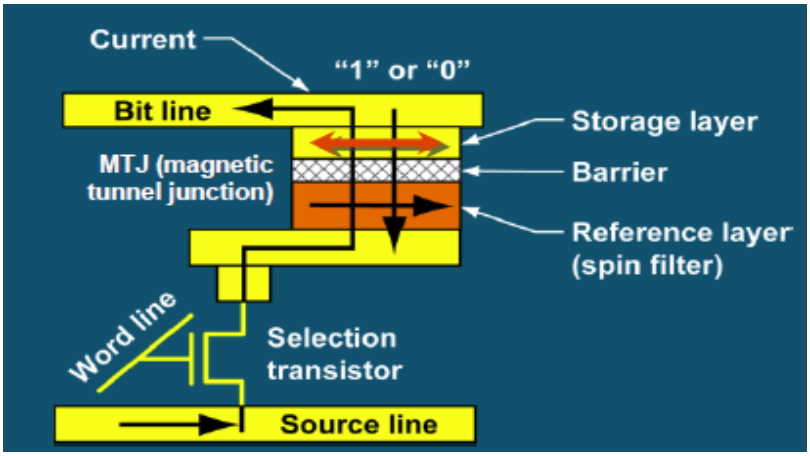


Figure 11 STTRAM Cell [19]

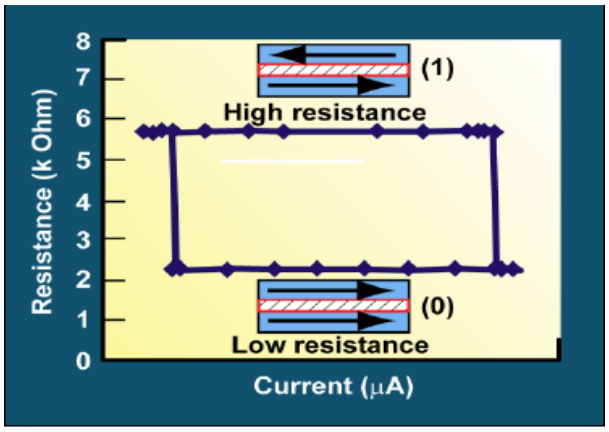


Figure 12 STTRAM DC I-V [19]

	PCM	CBRAM	Binary Oxide	MVO	STTRAM
Polarity	Unipolar	Bipolar	Bipolar/ Unipolar	Bipolar	Bipolar
V/I Driven Mechanism	Current (Temperature)	Voltage	Voltage	Voltage	Current
Forming Required?	No	Yes*	Yes*	No*	No
Abrupt Transition?	Yes	Yes	Yes	No	Yes
Self Limiting?	Yes	No	No	Yes	Yes
Requires Compliance?	No	Yes	Yes	No	No

* Usually, although some cases may show the contrary

Table 1 RRAM Cell Characteristics

1.5 Testing

In semiconductor memory development, memory cells are tested individually in test structures that connect metal pads to the terminals of the memory device. For a flash cell, for instance, the 4 terminals of the transistor would be connected to metal pads, the gate, drain, source, and bulk. This allows the cell to be programmed, erased, and read

without the effects of the memory array, or the need for any other circuits. Eventually, the memory cell must be integrated into a full array with a full supporting chip design, but the initial step is often the memory cell alone. Although the memory cell is tested alone, it is rarely an isolated structure. Isolated structures suffer from many issues, including feature sizes that print differently than dense arrays, and chemical mechanical polishing (CMP) that polish at different rates for isolated structures compared to dense arrays. To resolve such issues in a test structure, the memory cell of interest (the "live" cell) is usually placed in an array of dummy cell elements, with only the one cell of interest electrically connected. The rest of the cells are present, but not connected to help resolve some of the topological issues associated with an isolated structure. This configuration is shown in Figure 13.

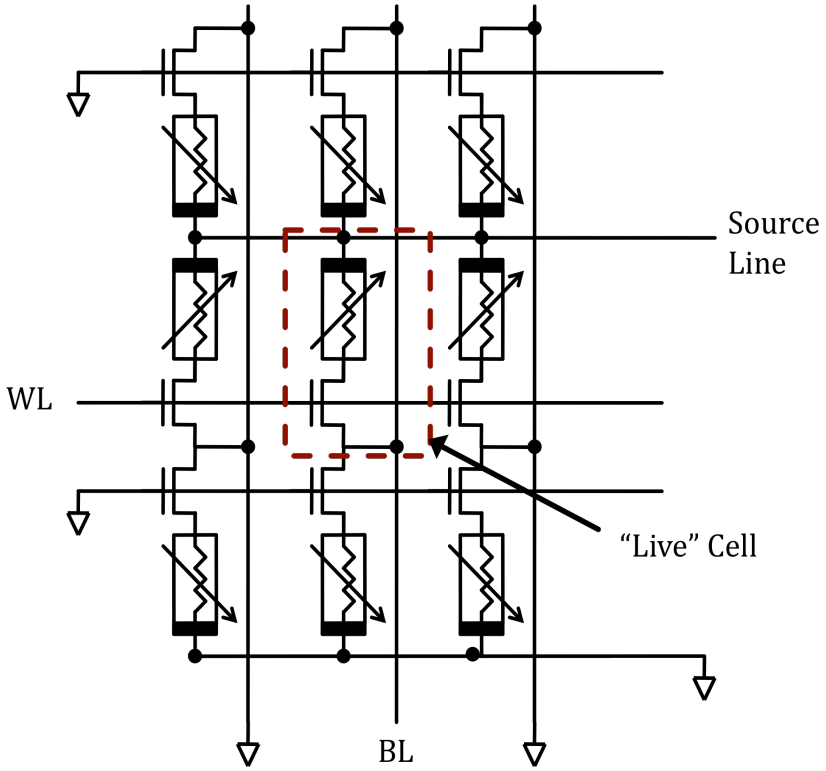


Figure 13 Test Structure Connecting to Single "Live" Cell

In an RRAM device, there are only 2 terminals to the memory cell, the top electrode (TE) and bottom electrode (BE). These electrodes are connected to metal pads on the wafer, which are then contacted with a probe card, shown in Figure 14. The probe card positions tungsten needles to make contact to the metal pads on the wafer. The probe card then connects through cables to the parametric tester. The parametric tester is capable of forcing a DC voltage and measuring current, or forcing a DC current and measuring voltage. Parametric testers can also generate voltage pulses of fixed amplitude and duration, frequently with programmable slew rates.

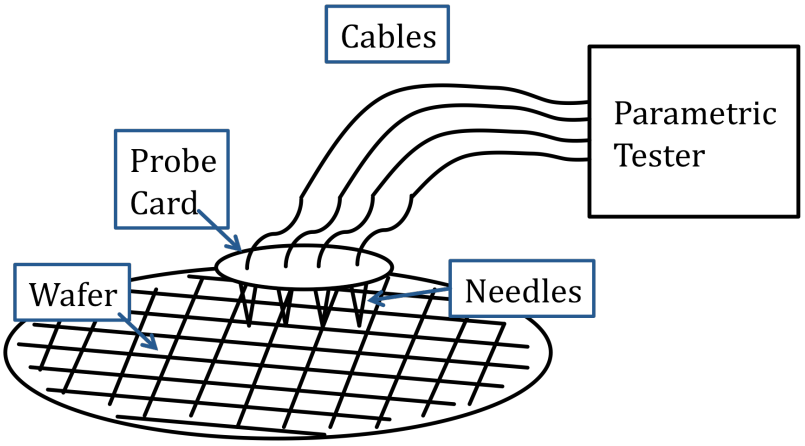


Figure 14 Parametric Test Setup

Some typical measurements for an RRAM device are discussed below. The first is a current versus voltage (DC I-V) sweep. Using the parametric tester, voltage is applied across the device in a stepped ramp. At each voltage step, the current through the device is measured and plotted on a graph. In a bipolar RRAM device, the voltage must be swept positive and then reversed and swept negative to SET and RESET the device. The DC I-V sweep for a CBRAM device is shown in Figure 15. The sweep starts at 0 *V* and sweeps in the positive direction (path 1). As the voltage increases, current increases linearly, showing the HRS. The voltage continues to increase and the current jumps

abruptly, indicating a switching event where the device changes to the LRS (SET operation). At this point, the current does not continue to increase in the device as the voltage increases. This is not a function of the device, but a feature of the parametric tester that limits the current. This limiting of the current is called current compliance, and as discussed previously, is critical to the successful operation of any CBRAM or binary oxide device. When the current is sensed to be greater than the allowed compliance, the voltage is reduced until the current is at the compliance value. The effect on the device being tested is that as the voltage steps, once compliance is hit, no further voltage stepping occurs. Once the maximum voltage is achieved, the voltage ramp reverses and proceeds to 0 *V* (path 2). The current follows the compliance limit until the voltage gets low enough to follow the LRS resistance linearly back to 0 *V*.

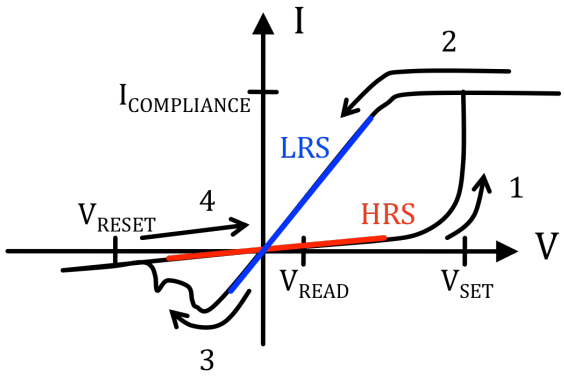


Figure 15 RRAM DC-IV

The next part of the sweep is in the negative direction (path 3). Again voltage is applied in a stepped ramp with current measurements at each step. As the voltage goes negative, the device changes from the LRS to the HRS (RESET operation). Note that this transition is more gradual, with multiple steps causing a "ragged" appearance as the cell changes resistance, and does not require such high current as the SET operation.

Since it is a gradual transition, no compliance is needed. The voltage continues to sweep to the maximum negative voltage and returns to 0 *V* on the HRS resistance curve (path 4).

Another typical measurement is pulsed cycling. In this measurement, the parametric tester applies a voltage pulse across the device at the V_{SET} bias for the SET operation, or the V_{RESET} bias for the RESET operation. After each SET or RESET operation, the current through the device is measured with a lower V_{READ} bias. The resultant waveform might look like Figure 16. Read currents after the SET and RESET pulses are then plotted vs. cycle number to show the behavior of cycling. Figure 17 shows the read values for a CBRAM cell vs. cycle number. Note that the device state after the SET operation (LRS) and the RESET operation (HRS) are determined by a single point measurement at 100 *mV*. Parametric testers do not have the ability to limit current during the pulses, which can be a big problem for CBRAM and binary oxide device. Often a resistor is placed in series between the parametric tester and the device to offer some protection against destruction of the device during the SET pulses. This type of current limiting is crude, but can be effective in some cases.

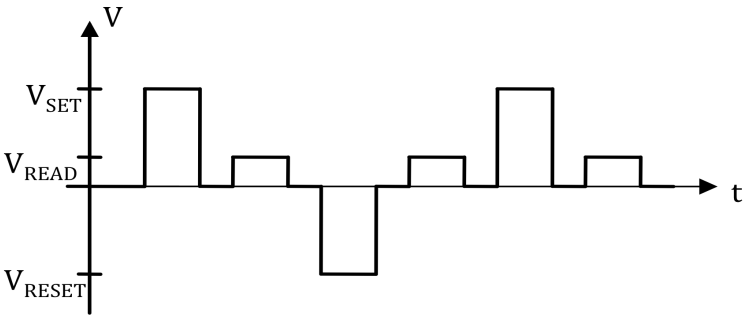


Figure 16 RRAM Pulse Waveform

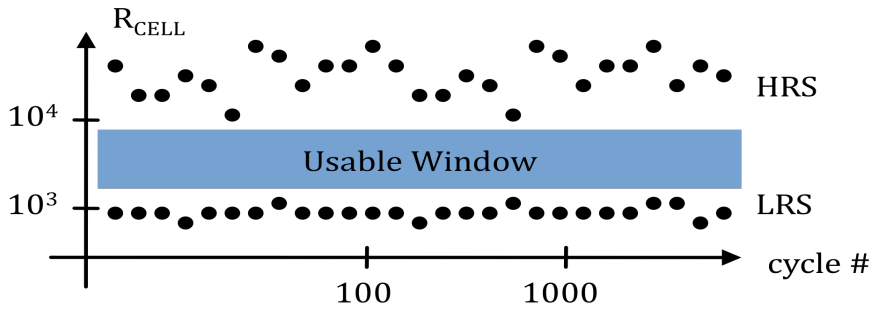


Figure 17 RRAM Resistances vs. Cycle

1.6 Parasitic Capacitance

Standard test methodologies have worked well for NAND, NOR, and DRAM devices, but the dynamic nature of RRAM device switching requires some special considerations. One issue that requires some scrutiny is parasitic capacitance of the connected lines. Typically, parametric test connections are 50 Ω impedance matched. This generally means that co-axial cable is used to connect probe card to the parametric tester. Standard 50 Ω co-axial cable has a capacitance of 30 *pF* per foot, so with a standard setup using 4-6 foot cables, the parasitic capacitance of any connection can easily be 150 – 200 *pF*.

As previously discussed, the CBRAM and binary oxide devices require current compliance to prevent damage to the conducting bridge/filament. The parasitic capacitance between the device and the compliance circuitry will change the amount of current that flows during a switching event. An example circuit is shown in Figure 18. The voltage pulse on the V_{TE} electrode pulses from 0 *V* to 3 *V*, and will flow current through the RRAM device. With the ideal current compliance connected at the bottom electrode, V_{BE} will be 0 *V* until the current limit is reached, then V_{BE} will increase to maintain current at the current limit level. The parasitic capacitance, C_{PAR}, will allow

additional current to flow through the RRAM device as V_{BE} rises. The additional charge, $\Delta Q = C_{PAR} \cdot \left(V_{Final} - V_{Initial}\right)$, is required to charge up the V_{BE} node, and dissipates additional energy into the RRAM device. For large capacitance such as the external pad and cable capacitance, this additional energy can destroy the RRAM device. For smaller capacitances, the additional energy may not destroy the device, but might change its LRS resistance, since the LRS resistance is related to the energy or current during the forming or SET operation [21].

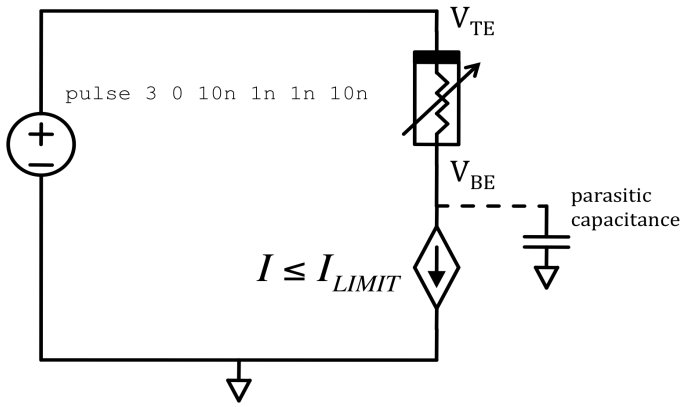


Figure 18 Current Compliance Circuit

1.7 Array Architectures

RRAM devices have been proposed in a number of array architectures. The simplest architecture, Figure 19, is to have a single RRAM device attached to a bitline on one end (the top electrode), and connected to a transistor on the other end (the bottom electrode). The gate of the transistor is connected to the wordline, and the source of the transistor is connected to the source plate. This configuration is called a ”1T1R” array because the memory cell consists of a transistor access device (the 1 T), and a resistive device (the 1 R). The circuit for this configuration is shown in Figure 19.

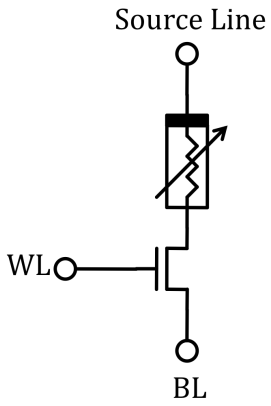


Figure 19 1T1R Array Architecture

A more complicated array architecture is to have the RRAM device connected to the bitline on one end (the top electrode), and to a wordline on the other end (the bottom electrode). Alternatively, there may also be a two terminal select device between the RRAM device and the wordline. This approach is called a "crosspoint" array because wherever the wordlines and bitlines cross, a bit in the array is formed at the intersection. This architecture is shown in Figure 20. This is the most efficient array, with a memory cell size of 4 F^2. The complication in this architecture is that there is no isolation from one cell to another. As one cell is selected, there are sneak paths that allow additional current to flow on the bitline during sensing from other unselected cells. The addition of a select device can help with the isolation, but there is a limit to how large of an array can be accessed in a crosspoint configuration. The solution to this problem is generally that the array is broken up into tiles of a certain size. The tiles are isolated from each other with transistors, and each tile is arranged in a crosspoint configuration. This allows a high density with good isolation. Crosspoint RRAM memories are also desirable because multiple layers can be stacked on top of one another. In a 1T1R, the transistor must be fabricated in the silicon substrate of the wafer, preventing the use of multiple layers. The

crosspoint array forms the RRAM device between two metal layers, so this can be repeated for additional memory layers. The result is a very dense array that can compete with NAND array density.

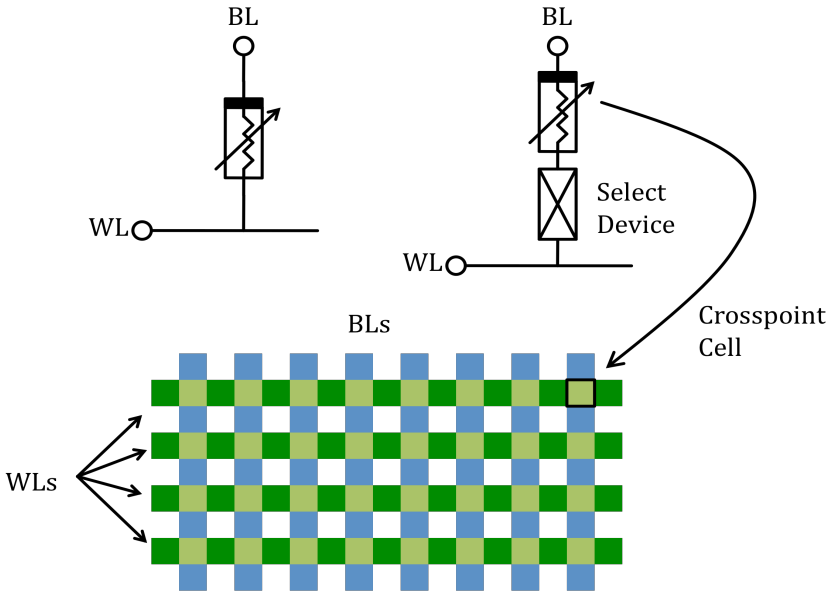


Figure 20 Crosspoint Array Architecture

A natural two-terminal select device for a crosspoint array would be a diode. In one direction, current flows, and in the other, no current flows, so biasing can be such that desired selection can be done with a diode. However, since the diode only flows current in one direction, this only works for unipolar devices. For the vast majority of RRAM devices that are bipolar in nature, a good select device is still being sought after.

CHAPTER TWO – IDEAL CHARACTERIZATION VEHICLE

As previously discussed, present test methodologies for NAND devices, and circuit elements are not adequate for basic characterization of RRAM devices. There is a need for a more comprehensive approach to test structures that will allow protection of devices and still enable simple operation. This work details some of the options and considerations, as well as one implementation of such a characterization vehicle.

Starting from the basic test structure in Figure 21(a), the parasitic capacitance of the pads and connections will be added in and shown in (b). A pad is connected to each end of the device, one to the top electrode, and one to the bottom electrode. For a bipolar device, a SET operation will be done biasing the device in one polarity, and a RESET operation will be done biasing the device in the opposite polarity. This can be done by holding one terminal at ground and biasing the other terminal positive (for a SET) or negative (for a RESET). The same biasing of the RRAM device can be performed without negative voltages by applying a positive SET bias on one terminal while grounding the other, and a positive RESET bias on the other terminal while grounding the one. The two options are shown in Figure 22.

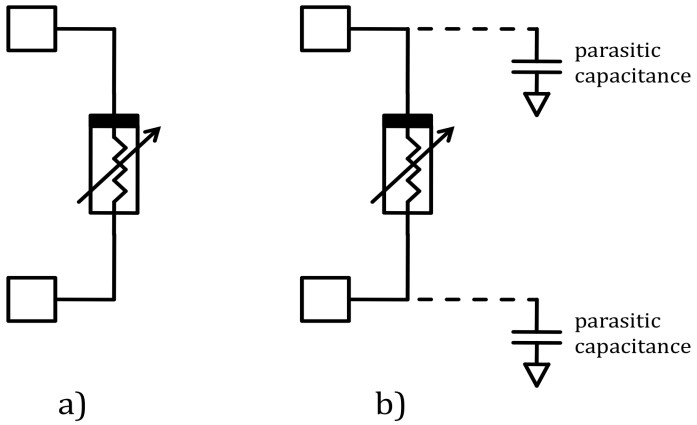


Figure 21 Parasitic Capacitance

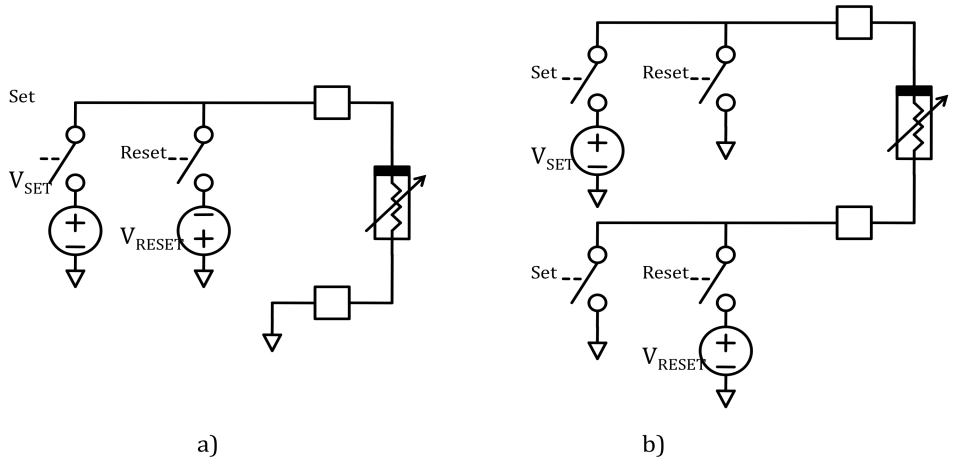


Figure 22 RRAM SET/RESET Biasing Options

2.1 Compliance Placement

There are many ways that current compliance can be represented and implemented in a circuit simluation. First, a current limited voltage source can be used to supply a voltage below a certain current limit, and once the current is exceeded, the voltage is reduced to maintain the current below the current limit. Another option is to use a current source with the magnitude of the current limit, then limit the voltage across it to ≥ 0 *V* to prevent it from going negative when the current required is less than the limit. A third option is to use a switch with a current limit. This option allows

connection to a voltage source, but will not allow more than a certain current limit to flow, with the voltage across the switch increasing to maintain the current at the current limit. For this discussion, a 0 V voltage source with a current limit of $I \leq I_{LIMIT}$ will be used to indicate the current compliance unit.

Figure 23 shows different placement of the current compliance unit, either above or below the RRAM device with respect to the positive voltage source. If a voltage is applied to the top of the circuit, when the RRAM device tries to draw more than the compliance current, the compliance circuit will adjust the voltage across itself to maintain the current at the current limit. For the bottom compliance configuration (a), the compliance circuit is located between the RRAM device and ground. In this configuration, the node between the RRAM device and the compliance circuit will start at 0 V, and when the compliance current is reached, the voltage will increase to maintain the current at the I_{LIMIT} value.

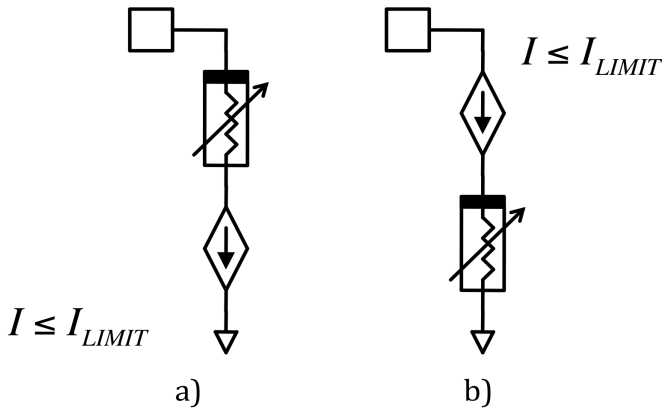


Figure 23 Current Compliance Placement Options

For the top compliance configuration (b), the compliance circuit is located between the positive voltage source and the RRAM device. The node between the RRAM device and the compliance circuit will follow the voltage source until the

compliance current is reached. If the compliance current is reached during the ramp, the voltage will simply stop increasing. If the voltage on the supply reaches a high voltage and then a switching event in the RRAM device causes the current to increase so that compliance is reached, then the voltage between the compliance circuit and the RRAM device will decrease so that the current is limited at the compliance level.

2.2 Compliance Options

There are several simple options for compliance. The ideal current limit would drop 0 V across it until the current reached the current limit, and then would allow the voltage to drop across it so that $I \leq I_{LIMIT}$. The circuit and the I-V response for the ideal current compliance circuit are shown in Figure 24.

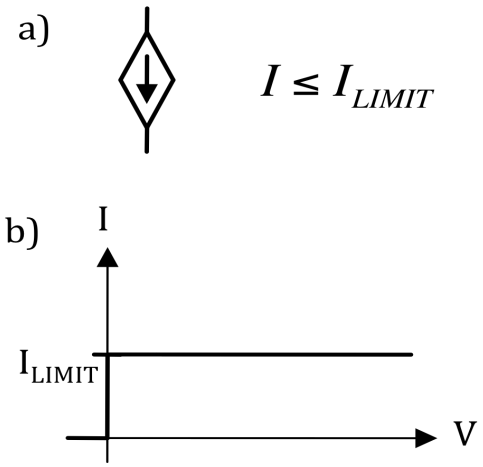


Figure 24 Ideal Compliance I-V Response

As already discussed, a simple series resistor provides some compliance to current, but will continue to drop voltage as the current increases. If the characteristics of the cell are not well known, it is likely that the voltage waveform actually delivered to the cell is much different than what was intended, distorting the results. The circuit and I-V response for the resistor compliance circuit can be seen in Figure 25. The I-V response

can be seen to be a simple line, with the slope of 1/R, which is not very close to the ideal compliance I-V repsonse. In fact, there is only a single point where I = I_{LIMIT}, at a single voltage. To ensure that the current never exceeds I_{LIMIT}, the voltage applied must be less than or equal to V_{LIMIT}. In most cases, the actual current through the RRAM device is significantly less than I_{LIMIT}, since some of the applied voltage is dropped across the RRAM device, leaving less voltage, and therefore less current, across the resistor current limiter.

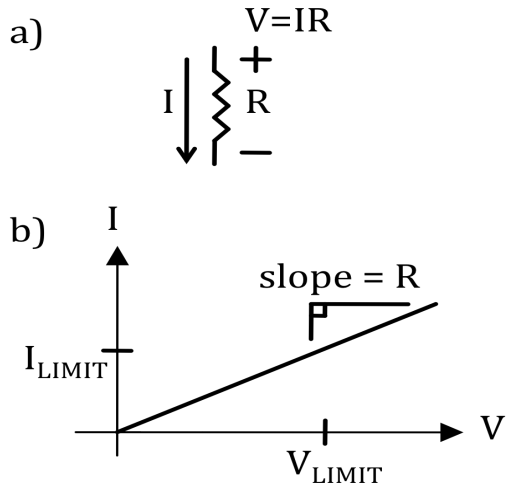


Figure 25 Resistor Compliance I-V Response

One improvement to the simple resistor is to use a MOSFET to provide compliance. This option is essentially the same as the "1T1R" array option discussed above. The circuit and I-V response for the MOSFET compliance circuit can be seen in Figure 26. Figure 26(a) & (b) shows the MOSFET on the ground side of the RRAM cell. Figure 26(c) & (d) shows the MOSFET on the high side of the RRAM cell. The I-V responses are dramatically different between the two, with the top I-V response looking much closer to the ideal case. Since RRAM cells are much more sensitive to the SET direction, it is desirable to have the best compliance and place the MOSFET so that it is

between the RRAM cell and ground during the SET operation. During the SET operation, a low, fixed gate voltage (V_G) is applied to the MOSFET, giving a constant V_{GS}. A larger width MOSFET will have a higher transconductance (gm), and therefore will have a smaller triode region (for a given V_{DD}), and a more ideal compliance characteristic. However, such a device will then be very sensitive to the gate voltage, with very small changes in V_G giving large changes in I_{DS}. Also, a large MOSFET device will have larger parasitic capacitance from the junction and gate overlap. During the RESET operation, the I-V response looks much more like the resistor, which as previously discussed, is not a good compliance device. Although the NMOS device is shown in the schematics, the MOSFET devices can be either NMOS or PMOS, which allows either top compliance or bottom compliance options.

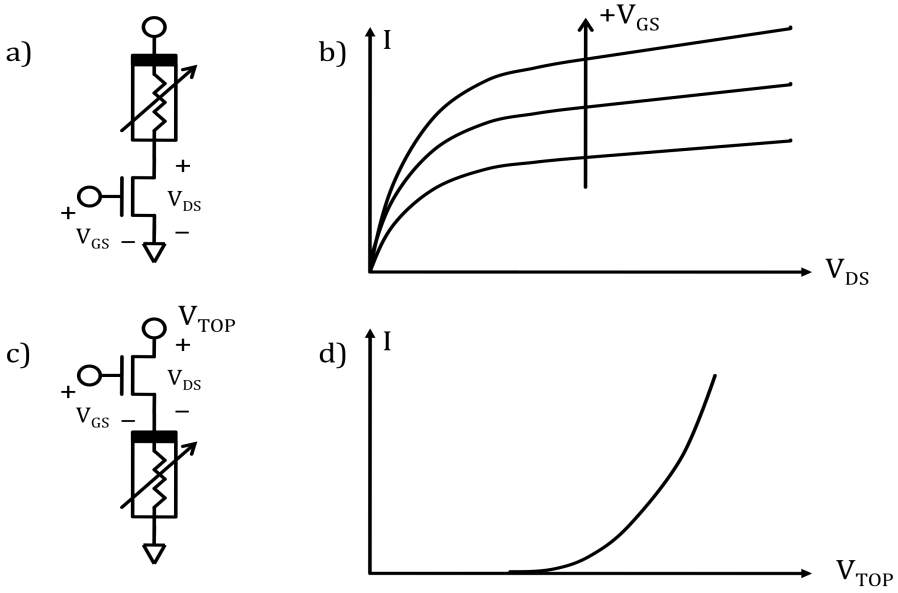


Figure 26 MOSFET Compliance I-V Response

A further improvement, and one that will be used in this work, is to use a current mirror to establish a very precise current compliance. The circuit and I-V response for the MOSFET current mirror circuit can be seen in Figure 27. One additional improvement is

to add a cascode device to further improve the I-V response characteristic. Since the voltage for the mirror is generated on chip using a matched device, much finer control of the current compliance can be realized.

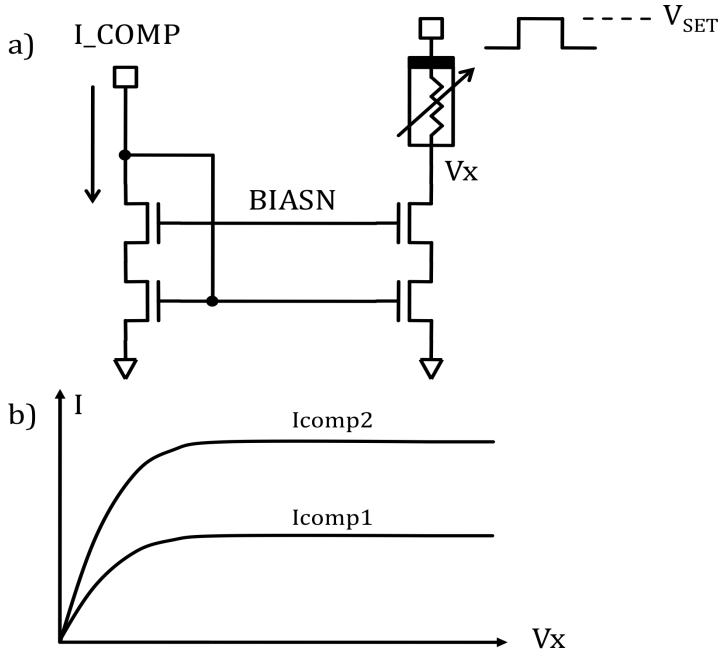


Figure 27 Current Mirror Compliance I-V Response

2.3 SET/RESET Compliance

As previously discussed, the transition from the HRS to the LRS during the SET operation requires current compliance to prevent destruction. The voltage applied across a cell during a SET pulse will break down the cell, causing current to flow. As the current flows, the resistance is reduced in the cell. As the resistance is reduced, more current flows (since the voltage is held constant across the cell). This positive feedback mechanism causes large currents to flow, which likely causes a thermal event, which redistributes the materials of the cell, causing a permanently open or shorted cell. Therefore, current compliance in the SET direction is a requirement.

For most cells, there isn't a requirement for compliance in the RESET direction. The voltage applied across the cell during a RESET operation causes current to flow according to the voltage applied and the resistance of the cell. As the current flows, the resistance of the cell increases, causing current to reduce. Therefore, the RESET operation is a negative feedback mechanism.

Even though current compliance isn't required in the RESET operation, there are other considerations that might make it desirable. Having compliance in the RESET direction allows an upper limit to be placed on the amount of current delivered to the cell, which enables characterization of the RESET current required. This information can be useful when sizing an access device for a 1T1R architecture, or determining current requirements for a crosspoint select device.

2.4 Pulsing Options

The traditional method of pulsing the RRAM cell to switch states is to apply a positive voltage pulse to one side and ground the other side for a SET pulse, and to switch the biases for a RESET pulse. Another approach is to hold one terminal and pulse the other high or low for SET and RESET. Either of these techniques is equivalent to the cell, but may require additional options for the test chip. For instance if one side of the cell is grounded, and the other side goes positive for SET and negative for RESET, the negative voltage requires the well of the NMOS devices to be separate from the substrate connection.

With the addition of a current compliance circuit using MOSFETs, a third option is available. The voltages across the RRAM and MOSFET can be applied, and then the gate of the MOSFET can be switched to define the SET or RESET pulse. The drawback

of this approach is driving the gate voltage very accurately and fast without causing overshoot, which would interfere with the current compliance.

With some additional CMOS transmission gates, the pulse can instead be applied through control signals. One such configuration is shown in Figure 28. This approach allows the voltage V_{SET} to be applied as a static voltage, and a voltage pulse applied to the control signal V_{PULSE}. One possible drawback to this approach is that it does not actively discharge the potential across the RRAM cell, but charge is trapped after the transmission gate is turned off, leaving a residual voltage across the cell. It is unclear if this is an issue or not. For a LRS state, the terminals will come to equilibrium through the RRAM cell itself. For the HRS state, the RRAM cell can be on the order of several G Ω, so it is likely any trapped charge will eventually leak off through junction leakage. Obviously there is no current available with the trapped charge, so for RRAM technologies that have current driven mechanisms, there should be no problem. For RRAM technologies that have a voltage driven mechanism, however, we must consider that charge trapped on the terminals of the RRAM cell in the HRS state could cause the state of the cell to be disturbed.

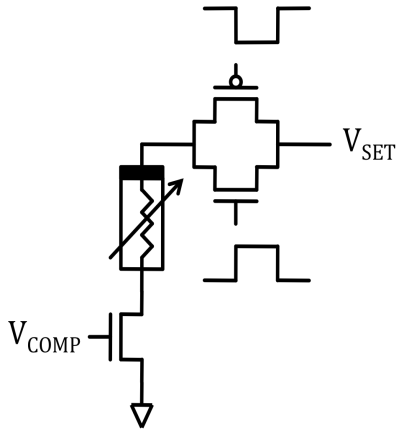


Figure 28 Pulsed CMOS Transmission Gate

2.5 Cell Polarity

Another aspect to consider is the polarity of the cell. Consider a new material set that hasn't been characterized well in the literature. It's not always known which direction of bias will cause a cell to SET to the LRS. Even when the direction is known, it's not always an option to be able to flip the terminals/materials to put the cell in the desired direction. Therefore, it's necessary to be able to apply the SET bias in either direction, with compliance.

2.6 Design Choices

The focus of this work is to allow for accurate characterization of multiple RRAM memory cells, while giving flexibility in the fabrication process. In order to accurately characterize the RRAM cell, it is necessary to minimize the parasitic capacitances. The CMOS transistor performance was partly unknown, so in the design process, simulation was used as a guide, with final performance to be assessed on actual silicon. Given the reality of varying transistor performance, choices were made in the design to maintain flexibility.

The completed circuit for the "Ideal RRAM Characterization Vehicle" (IRCV) is shown in Figure 29. In the center of the schematic is the RRAM cell. Voltages are applied to the V_TOP pad at the top of the circuit. Current flows through the memory cell and into the current mirror to ground.

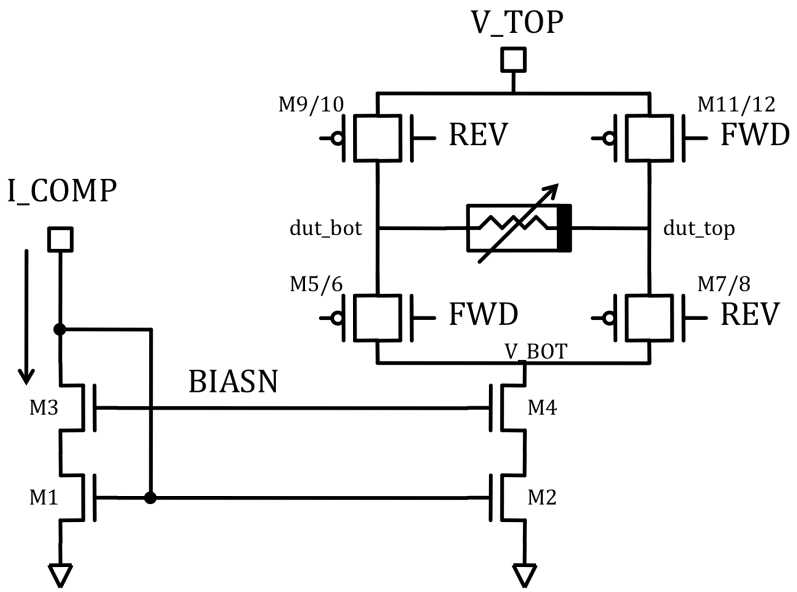


Figure 29 Ideal RRAM Characterization Vehicle

There are two control signals, FWD and REV. The FWD signal and its complement, open the transmission gate (made up of M11 and M12), to connect the V_TOP voltage to the top electrode of the RRAM cell. It also opens the transmission gate (made up of M5 and M6) to connect the bottom electrode of the RRAM cell to the current mirror. This direction is defined as the "forward" direction, since the positive voltage is applied to the top of the cell, and the bottom of the cell is connected to ground.

The REV control signal reverses the direction of the cell so that the positive voltage is connected to the bottom electrode through transmission gate M9/M10, and the current mirror connects the top electrode to ground through transmission gate M7/M8. This direction is defined as the "reverse" direction.

Either the FWD or REV direction can give a SET or RESET operation, depending on the characteristics of the cell. While most RRAM cells have one specific direction for SET, there are some RRAM cells that can be SET equally well in either the FWD or REV direction. In the case of the latter cell, the "forming" (initial SET) direction determines

that subsequent SET operations will be done in that same direction, and that RESET operations will be done in the opposite direction.

Note that the transmission gates form a tri-state mux that allows the cell to be SET with compliance in either direction. This enables flexibility on the process side to build the cell in the easiest way, and then decide through cell characterization which direction is best for SET and RESET.

Transmission gates were chosen for their voltage passing capability. This allows for the maximum voltage range to be passed for a given transistor specification, since the full V_{DD} can be passed through the switch. Use of NMOS pass gates was considered, but was rejected due to the fact that only $V_{DD} - V_{THN}$ can be passed through these switches. One impact to this choice is the additional junction capacitance that comes from the PMOS device, which can impact the RRAM cell.

During the SET operation (shown in Figure 30(a)), the desired current compliance is applied to the I_COMP pad. This current is then passed through M1, and is mirrored to M2/M4, which act as a current source. The M2 device provides 0 *V* to the V_BOT node, which is connected to the bottom of the memory cell through the transmission gate M5/M6. The V_{SET} voltage is applied to the V_TOP pad, and connected to the top of the memory cell through the transmission gate M11/M12. When the current through the RRAM cell exceeds the compliance current, the V_BOT node rises until the current through the RRAM cell equals the compliance current.

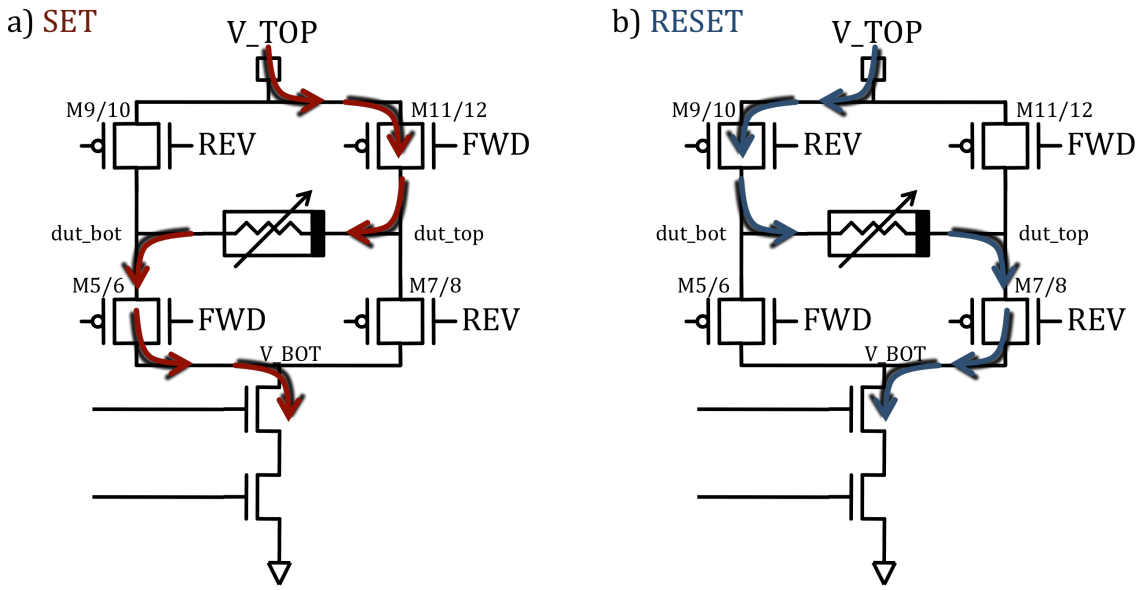


Figure 30 SET and RESET Operations

Similarly, during the RESET operation (shown in Figure 30(b)), the desired compliance current is applied to the I_COMP pad, and mirrored through M2/M4. 0 *V* is applied to the top of the memory cell through the transmission gate M7/M8. V_{RESET} is applied at V_TOP, and connected to the bottom of the memory cell through the transmission gate M9/M10. The current is normally the highest at the start of RESET, and so as the voltage pulse is applied to V_TOP, the V_BOT node rises to limit the current, if necessary. As current flows through the memory cell, the cell becomes higher resistance, and current limits, causing the V_BOT node to drop.

The current mirror is a standard NMOS cascoded current mirror. The bias for the cascode device is applied through the BIASN pad. The bias voltage could have been generated on-chip through a beta-multiplier reference, or even a simple resistor divider, but given the need for flexibility, an off-chip voltage supply was chosen. This allows biasing to be selected based on the actual transistor parameters, to give the widest

operating range of the current mirror. In general, the bias to be applied on BIASN is V_{GS} + $V_{DS,sat}$.

2.7 Operation

The operation of the IRCV is discussed below. Voltages for SET, RESET, and Read operations are always applied to the V_TOP pad. The direction of the current flow is determined by the FWD and REV pads, switching the top of the cell to V_TOP, and the bottom of the cell to the compliance circuit, or the bottom of the cell to V_TOP, and the top of the cell to the compliance circuit respectively. In addition, if both FWD and REV are low, the cell is floating.

The desired compliance current is applied on the I_COMP pad, and is setup before the switching of other signals to ensure that the gate voltages on M1 and M2 are constant before switching occurs. For read, a higher I_COMP may be applied to ensure that there is little voltage dropped across M2 and M4 so that the real resistance of the RRAM cell can be measured. During reads, a low bias is placed across the cell, so switching will not occur, and so compliance is not necessary.

Figure 31 shows all the primary operations and the two methods for applying pulses. The primary modes of operation are SET, RESET, Read FWD, and Read REV. The last two operations are reading with current flow from top to bottom of the RRAM cell (forward), and reading with current flowing from bottom to top (reverse).

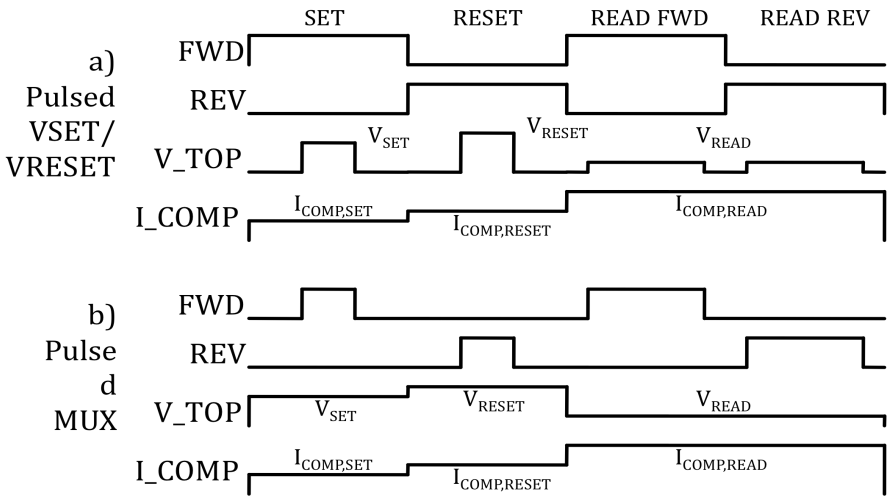


Figure 31 Primary Operation Waveforms for IRCV

For pulsed V_{SET} and pulsed V_{RESET} operation, the sequence of applied signals can be seen in Figure 31(a). BIASN is held steady at the desired voltage, I_COMP is applied for the appropriate operation, and the mux signals FWD and REV are held to provide the correct direction. After the previous signals are setup, the V_TOP voltage is pulsed to V_{SET}, V_{RESET}, or V_{READ}, depending on the operation. The time allowed for the SET or RESET operation is defined by the width of the pulse applied to V_TOP.

For pulsed mux operation, the sequence of applied signals can be seen in Figure 31(b). BIASN and I_COMP are held to the correct biases as described in the pulsed V_{SET}/V_{RESET} above. V_TOP is also held at the correct voltage, V_{SET}, V_{RESET}, or V_{READ}, depending on the operation. One of the mux signals is held at 0 *V* (either REV or FWD depending on operation), and the other mux signal (FWD or REV) is pulsed to V_{DD}. The time allowed for the SET or RESET operation is defined by the width of the pulse applied to FWD or REV.

During the READ operation, the current from the V_{READ} supply applied to V_TOP is measured. Typically, this measurement will take several milliseconds to complete, so

V_{READ} is applied for a long time. The SET and RESET operations, by contrast, can be very short. Some RRAM cells switch in less than 1 *ns*, where others require 10's of nanoseconds, or microseconds. When fast pulses are applied during SET and RESET, the current can't be measured.

2.8 Parasitic Capacitance

As previously discussed, if the parasitic capacitance at the terminals of the cell, or in the testing setup is too large, the cell can be destroyed by a SET operation. However, even smaller amounts of parasitic capacitance can affect the operation of the RRAM cell. Many papers talk about the resistance of the LRS state being related to the compliance current during the SET operation. In the ideal case, the maximum current in the cell would be only what the compliance current allowed. In practice, the parasitic capacitance has an impact on the actual maximum current through the cell. The maximum current depends on the transition properties of the cell and the amount of parasitic capacitance, as well as the compliance current applied. The parasitic capacitance of concern is located on the V_BOT node, which must move in order to limit the current through the changing cell. Additional capacitance on the V_TOP node is not a concern, since that will be driven by a voltage source, and will not be a source of additional current flow through the RRAM cell.

The parasitic capacitance on V_BOT is comprised of the capacitance from the cell itself, the FWD/REV mux, and the current mirror. The capacitance of the RRAM cell varies greatly depending on the oxide thickness, the oxide material (many are high-K materials like HfOx), and the cell area, and can be represented by $C_{RRAM} = \frac{\varepsilon_{RRAM}}{t_{OX}} \cdot Area$.

The capacitance of the FWD/REV mux is determined by the one "on" mux, and the two "off" muxes. The "on" mux has both transistors in triode, so will be $C_{ON} = C'_{OX} \cdot \left(W_P \cdot L_P + W_N \cdot L_N\right)$ and each "off" mux will be $C_{OFF} = CGD0 \cdot \left(W_P + W_N\right)$. The total capacitance of the mux is:

$$C_{MUX} = C_{ON} + 2 \cdot C_{OFF} = C'_{OX} \cdot \left(W_P \cdot L_P + W_N \cdot L_N\right) + 2 \cdot CGD0 \cdot \left(W_P + W_N\right)$$

To the first order, only the drain capacitance of M4 counts as the capacitance of the current mirror, since the M3 capacitance is hidden by the cascode configuration. Since the cascode device is in saturation, the capacitance of the current mirror is $C_{MIRROR} = CGD0 \cdot W_N$ [22].

The total parasitic capacitance is given by

$$C_{PARA} = C_{RRAM} + C_{MUX} + C_{MIRROR}$$

$$C_{PARA} = \frac{\varepsilon_{RRAM}}{t_{OX}} \cdot Area + C'_{OX} \cdot \left(W_P \cdot L_P + W_N \cdot L_N\right) + 2 \cdot CGD0 \cdot \left(W_P + W_N\right) + CGD0 \cdot W_N$$

An estimation of the components for a cell requiring 100 *uA* of switching capability for a 5 *nm* thick 100 *nm* cell, using HfOx as a RRAM cell would yield the following.

$$C_{PARA} = 350\ aF\ (C_{RRAM}) + 9.9\ fF\ (C_{MUX}) + 1\ fF\ (C_{MIRROR})$$

$$C_{PARA} = 11.25\ fF$$

Although parasitic capacitance has been much reduced from the original 2 terminal setup, there must still be a balance between the need for flexibility, (using the mux, etc.) performance (sizing to reduce voltage drops), and parasitic capacitance. This design attempted to keep the capacitance below 50 *fF* as a target.

CHAPTER THREE – SIMULATION RESULTS

The IRCV was fabricated in an in-house low cost 0.18 μm, 3.3 V CMOS process, derived from a NAND process flow. Although the process is rated for 3.3 V for production devices, operations up to 5.0 V for short times were permitted for this test chip. Simulations were performed with HSpice, and reported below.

The completed IRCV schematic circuit is shown in Figure 32. There are 5 inputs to the circuit besides V_{DD} and ground. I_COMP and BIASN control the compliance mirror, with the compliance current forced into the I_COMP input, and the voltage desired on the gate of the cascode device in the compliance mirror forced on the BIASN input.

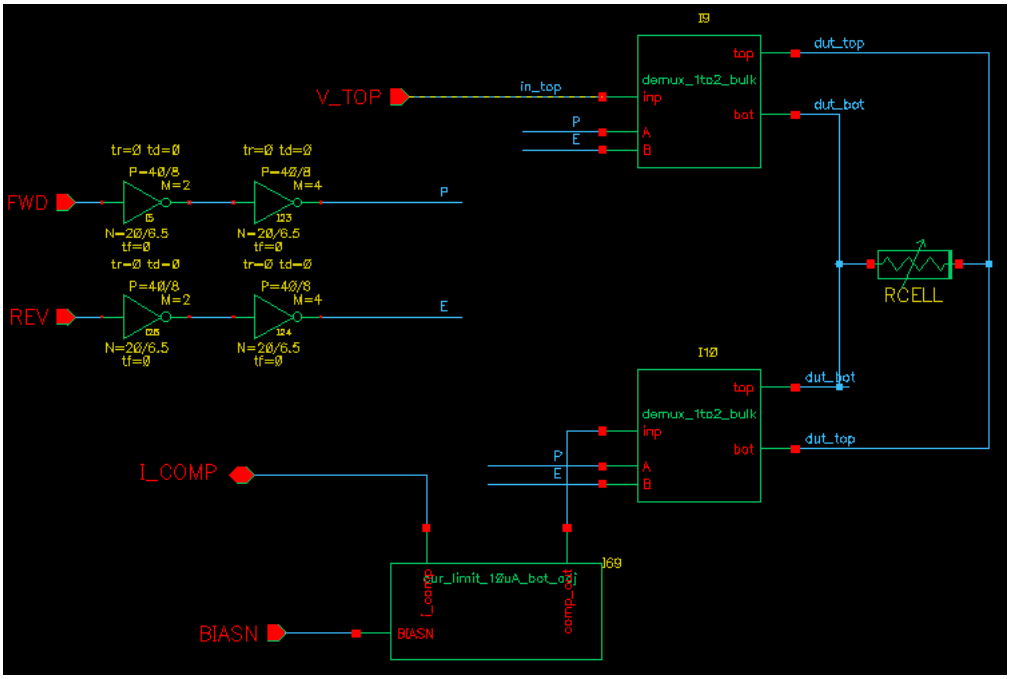


Figure 32 Complete IRCV Schematic

The FWD and REV inputs control the mux that determines the direction of current flow through the RRAM cell. As discussed above, there are 4 useful states that result in the combination of these two inputs. The truth table for the different states is

shown in Table 2. V_TOP is the input that supplies V_{SET}, V_{RESET}, or V_{READ} for the SET, RESET or READ operations.

FWD	REV	Operation
0	0	Float Cell
1	0	Connect V_TOP to dut_top, Compliance mirror to dut_bot
0	1	Connect V_TOP to dut_top, Compliance mirror to dut_bot
1	1	Char compliance mirror (Connect V_TOP, dut_top, Compliance mirror, dut_bot)

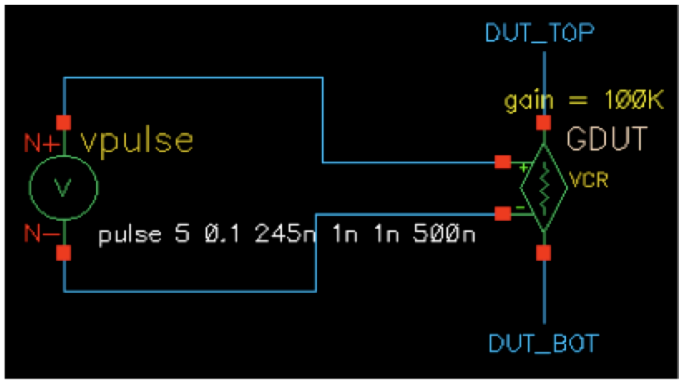
Table 2 Truth Table for IRCV Control Signals

3.1 RRAM Cell Model

There are many theories on how each of the cell options operates, and some fairly computation-intensive models to match. Many models exist, and have been proposed for switching behavior and resistance in academic, and industry papers. Most of these models are physics based, and so are difficult to implement in SPICE without significant effort. However, for the IRCV, it wasn't necessary to model the exact switching characteristics of any specific RRAM cell, since it is intended to be a generic vehicle. So since our concern is accurate compliance, it is necessary to consider the worst case RRAM cell model, which would be one that had instantaneous switching. It was decided to use a simple RRAM cell model using standard SPICE components, which could accomplish the goals of "instantaneous" switching and not be computationally intensive, or have issues of convergence.

The RRAM cell model is shown in Figure 33. The model is extremely simple, with a voltage-controlled resistor (VCR) being the central element. In HSPICE, the VCR

is implemented as a "G" element, although it can be implemented with other versions of spice with a combination of current and voltage sources. There is no feedback in the circuit to change the resistance based on voltages applied to the cell. To switch the state of the cell, the input voltage of the VCR is changed abruptly using a standard pulsed voltage source, and the resistance of the cell changes abruptly as well.




```
*DUT Model
vpulse vpulse 0 pulse 5 0.1 245n 1n 1n 500n
gdut dut_top dut_bot VCR vpulse 0 100K
```

Figure 33 RRAM Cell Model, HSPICE Code and Symbol

3.2 Compliance Mirror

The current mirror shown in Figure 34 is the completed schematic of the compliance circuit. The current mirror was designed for up to 100 μA compliance operation, with the minimum transistor size to reduce the associated parasitic capacitances. A size of 4 μm/.5 μm (40/10 with M = 2 shown, 0.05 scale factor) was chosen despite the rather high V_{THN} = 1.25 V for a 100 μA current. Note that the minimum L for this process is 0.18 μm, and minimum W of 0.5 μm, so a larger than minimum L and W were chosen for matching purposes.

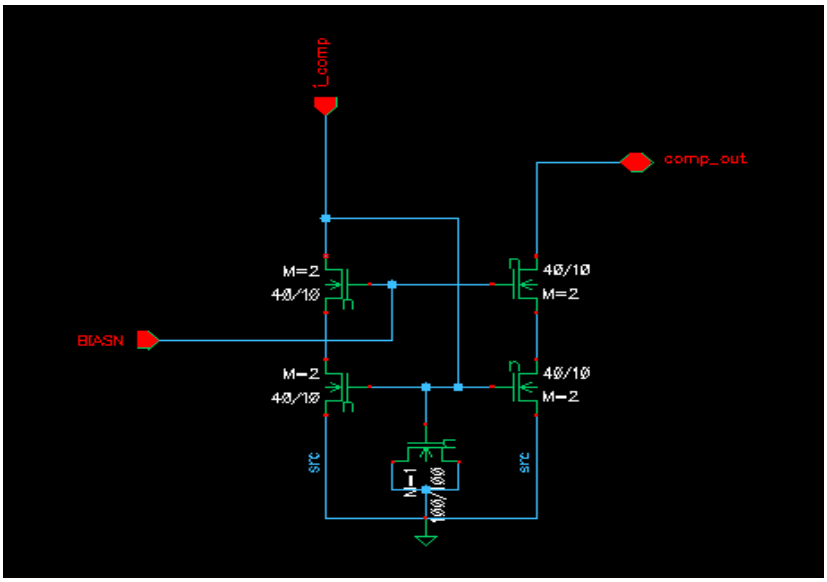


Figure 34 Compliance Mirror Schematic

The I-V plots of the current mirror are shown in Figure 35 and Figure 36. The I-V's are shown in log and linear scale to show different features. First, from the log plot, it can be seen that the current mirror works well over a large range, from 1 μA up to 100 μA. Second, as can be seen clearly in the linear plot, the current increases above 3.5 V V_{DS} when the mirror is biased at 100 μA. A solution to this problem is discussed below.

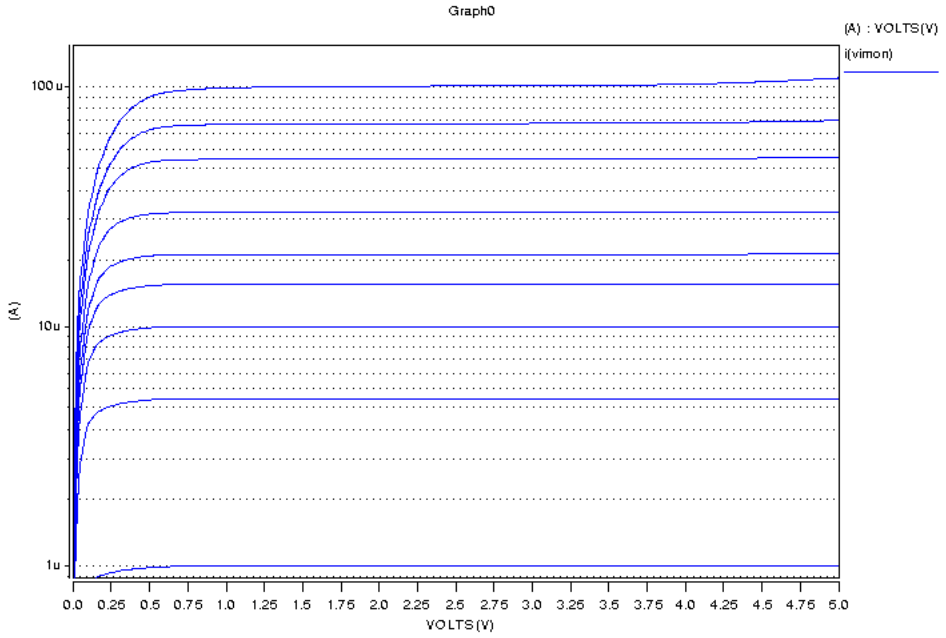


Figure 35 Compliance IDS vs. VDS, Log Scale

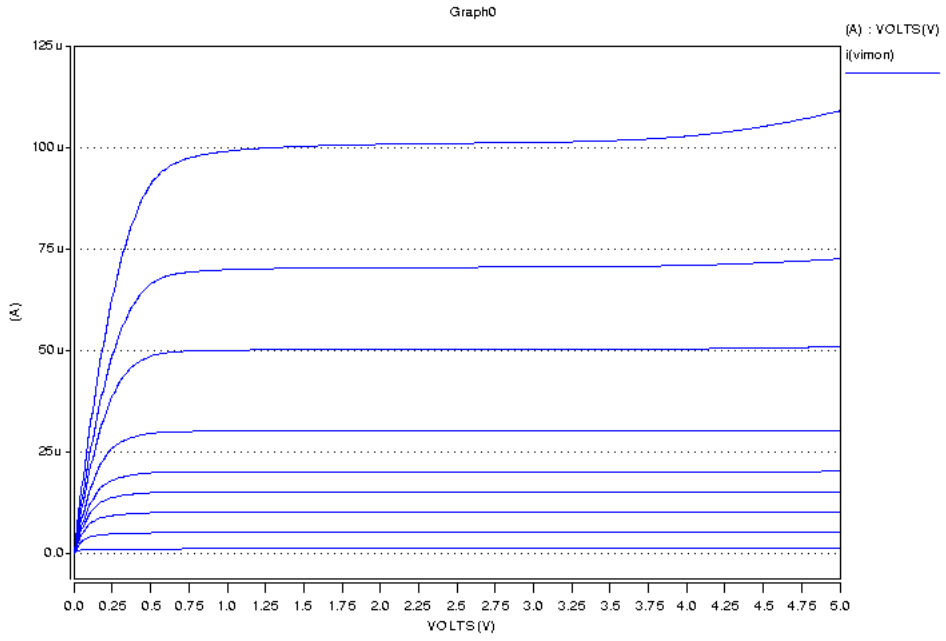


Figure 36 Compliance IDS vs. VDS, Linear Scale

The importance of flexibility in biasing the gate of the cascode device can be seen in Figure 37. Biasing the gate of the cascode (BIASN) too low in (b) and (c) shows that the mirror current is not constant with changing V_{DS} voltage. In the case of the higher 100

μA compliance current, too low of BIASN voltage limits V_{DS} on M2 and prevents it from operating in saturation. This changes the output resistance of the mirror, causing the increase in current at high cell voltages. As can be seen in (a), the proper BIASN shows that there is a fairly high $V_{DS,sat}$ voltage required at the 100 μA bias condition. This is a result of the transistor sizing, and the high V_{THN} required. It is desirable to reduce the $V_{DS,sat}$ voltage so that more voltage is available for the RRAM cell in Forming, SET, and RESET. In the 100 μA case, it was decided to accept the 500 mV drop, knowing that for lower bias currents, the $V_{DS,sat}$ will be lower, and less headroom is required.

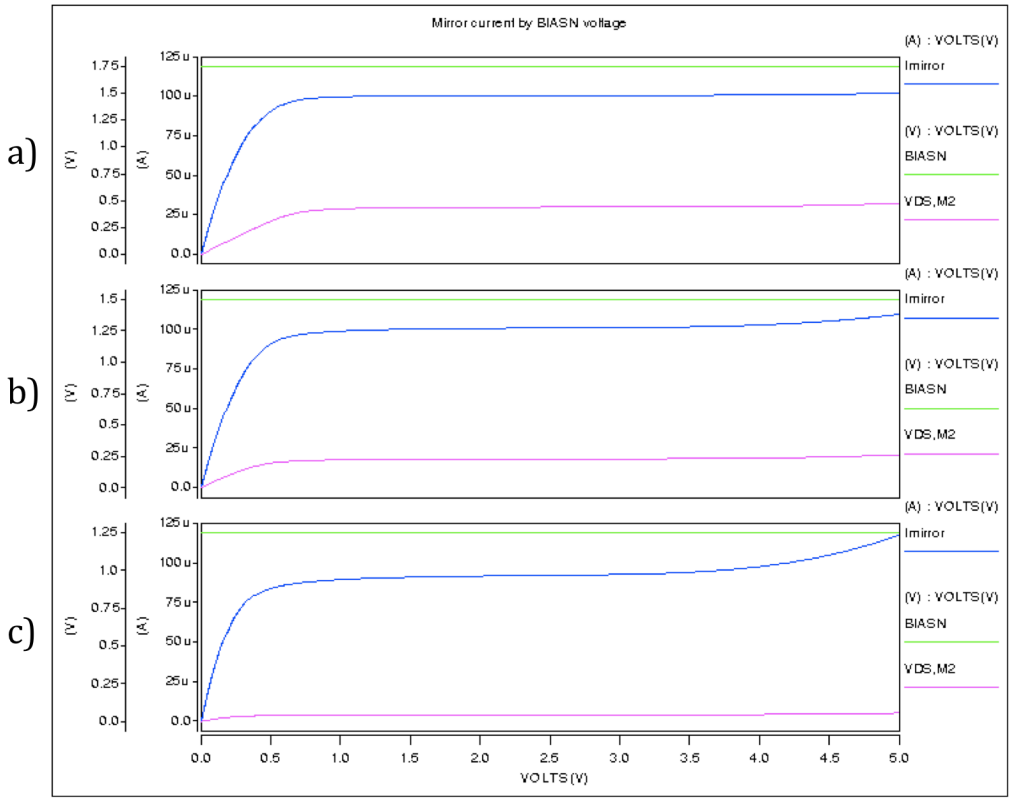


Figure 37 Mirror Current by BIASN voltage

The transient response of the compliance mirror is critical in controlling the SET current through the RRAM cell. Figure 38 shows the transient simulation of a voltage pulse applied to the output of the current mirror, and the current through the voltage

source. The pulse is a 20 *ns* pulse width with a 1 *ns* rise and 1 *ns* fall time. A 60 μA compliance current is used in the mirror. At the beginning of the pulse, an overshoot up to 100 μA is seen, with 185 *ps* above 80 μA. Although any overshoot could affect the placement of SET bits, there are two reasons that it is unlikely to have a significant impact. First, the energy in this pulse is on the order of the energy contained in the cell itself, and second, the full voltage across the cell has not yet developed.

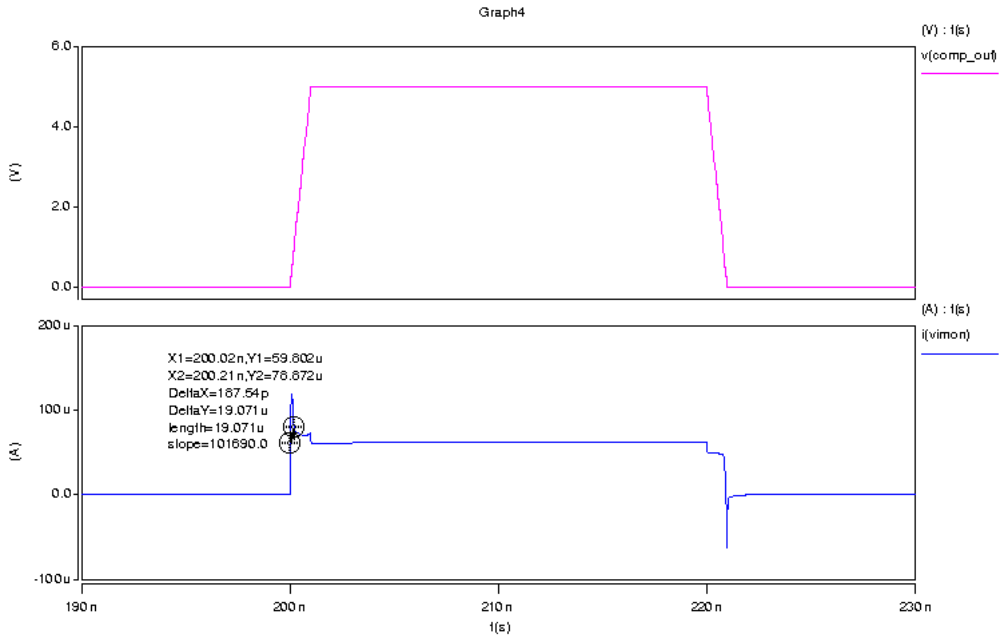


Figure 38 AC Response of Compliance Mirror

3.3 FWD/REV Mux

The mux that controls the RRAM cell direction is shown in Figure 39. This is a tri-state mux that is comprised of two CMOS transmission gates. The control logic uses two lines to enable one or the other of the transmission gates. The complement signals for the PMOS devices are generated locally. When one control signal is high, one input passes to the output. Since the transmission gate is CMOS, it can pass full V_{DD} and full ground signal. If neither control signal is high, then the output is in the Hi-Z state. It is

also possible to enable both control signals to short both inputs to the output. This is useful in the full circuit implementation to short the top and bottom of the cell to V_TOP and to the compliance circuit. This enables the compliance mirror to be characterized without affecting the RRAM cell.

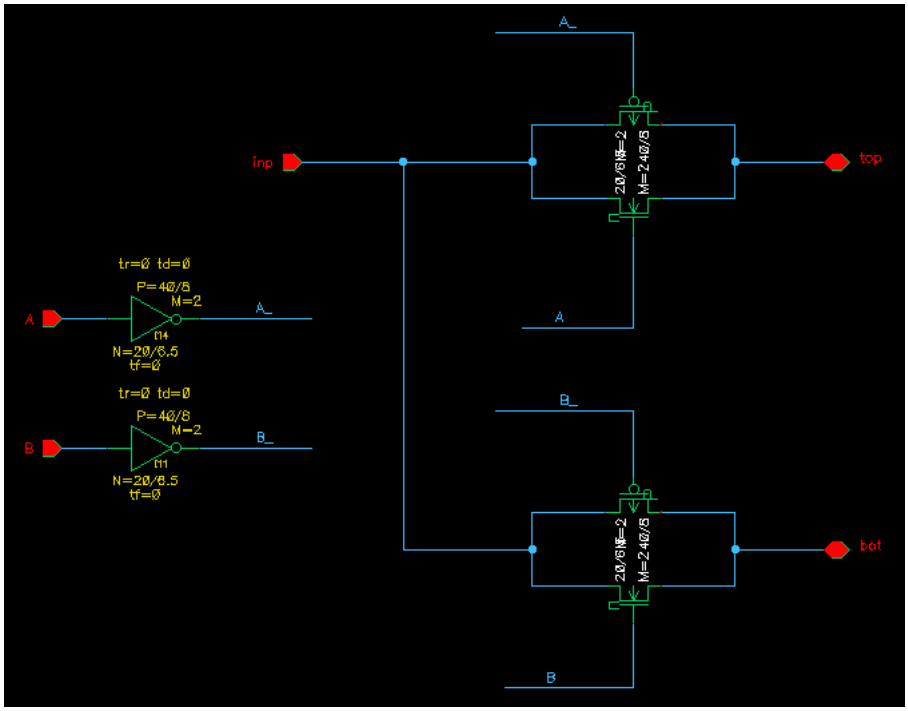


Figure 39 FWD/REV Mux Schematic

3.4 Transient Analysis

The transient analysis of the full circuit is shown in Figure 40. A SET pulse is given in this case, with a 1 ns rise and fall, a 20 *ns* pulse width, and an amplitude of 3.0 *V*. A compliance of 60 μA is applied to the compliance mirror, and the FWD signal is switched before V_TOP is pulsed to the VSET voltage. The control signal for the cell model is switched 5 *ns* into the SET pulse, changing the resistance of the memory cell from 500 $k\Omega$ to 10 $k\Omega$ in 1 *ns*.

As V_{SET} (3.0 V) is applied to V_TOP, the top of the memory cell goes to V_{SET}. With the bottom of the cell held at 0 V through the compliance mirror, a small current flows as a result of the 500 $k\Omega$ memory cell (6 μA). Once the memory cell switches to 10 $k\Omega$, a much larger current would flow (300 μA) if it were not for the compliance mirror. As the resistance of the memory cell reduces, the current through the cell rises, until the compliance current limit is hit. At that point, the dut_bot node rises to reduce the voltage across the memory cell to maintain 60 μA through the cell. In this case, at 10 $k\Omega$, the voltage across the cell (VCELL) is 0.6 V after the cell transition is complete.

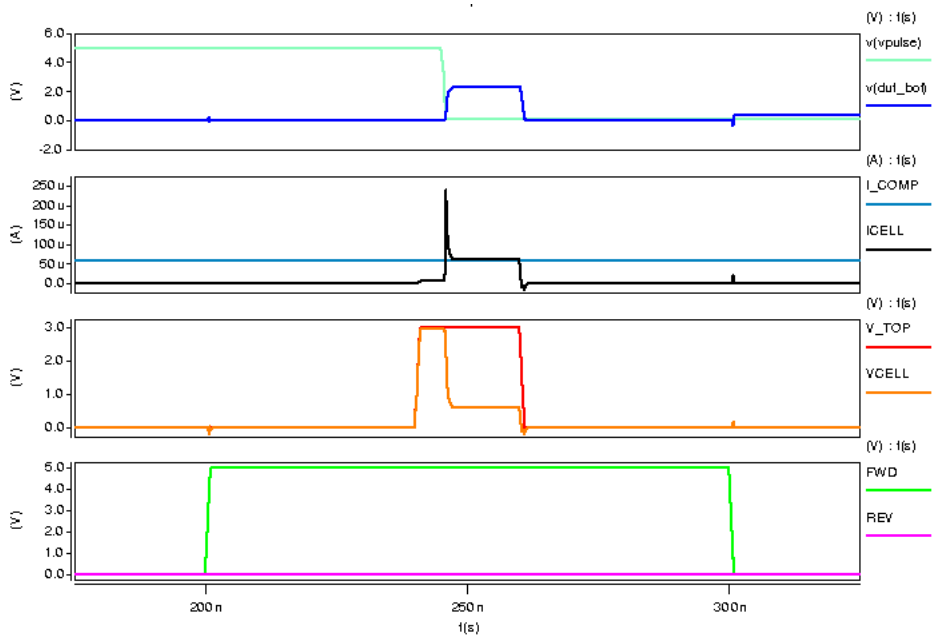


Figure 40 Transient Response of IRCV

It can be seen that there is a large transient current spike through the memory cell (ICELL) as the cell transitions from the HRS to the LRS. The magnitude of this spike can be seen in Figure 41 as 250 μA, with the total width above 100 μA as 450 ps. As previously discussed, this is due to the parasitic capacitance on the V_BOT node, which takes some time to charge as the voltage rises to limit the current through the memory

cell. Since the current to charge up the capacitance on the V_BOT node is flowing through the memory cell, the RC time constant can be calculated to see how accurate the previous estimation of parasitic capacitance is. It was previously shown that C_{PARA} = 11.25 fF and the LRS of the memory cell is 10 $k\Omega$, so the rise time is 2.2 * R * C = 248 ps, which is close to what is observed in the simulation.

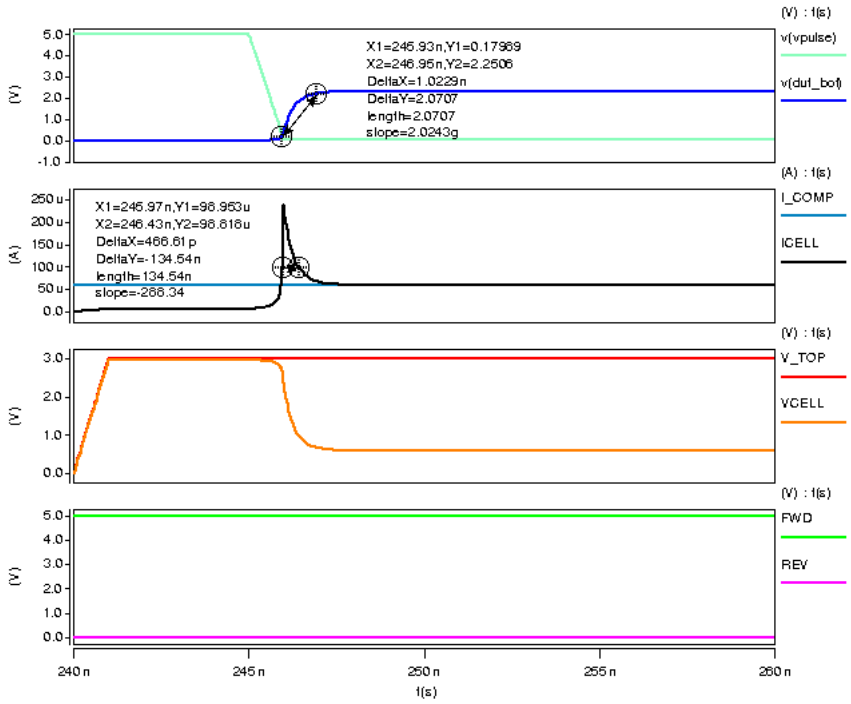


Figure 41 Transient Current Spike

To see how much energy is contained in the spike, we can look at the difference in energy stored in the parasitic capacitance before and after the switching event. The difference in energy must be discharged through the RRAM cell, since no other path exists. The simulations show the true C_{PARA} is ~20 fF based on the time constant of the discharge. Since the initial voltage across the capacitor is 0 V (dut_bot is at 0 V), the initial energy is 0. The delta energy can be shown to be:

$$\Delta E = \tfrac{1}{2} \cdot 20\,fF \cdot 2.3V^2 = 53\,fJ$$

Since the capacitance of the RRAM cell itself was previously calculated, we can compare the energy of this spike with the energy contained in the RRAM cell itself:

$$E_{CELL} = \frac{1}{2} \cdot 350aF \cdot 3V^2 = 1.58fJ$$

The current spike through the RRAM memory cell contains approximately 30 times the energy contained in the RRAM cell itself. Although it is desirable to minimize the energy by reducing the sizing of the components, this must be balanced with the desire to have a low impedance path for the SET and RESET operations. Reducing the size of the transistor components will make a more resistive path, and the resistance could become the current limiter instead of the compliance mirror. This is undesirable since the shape of the current compliance with a resistor is far from ideal, as previously discussed.

CHAPTER FOUR – ELECTRICAL RESULTS

The IRCV was fabricated on 300 *mm* wafers and tested in wafer form using a Suss semi-automatic probe station, and a Micromate 2 electrical tester, shown in Figure 42. The layout of the IRCV is shown in Figure 43, and the corresponding micrograph of the fabricated IRCV is shown in Figure 44. Custom software for the Micromate was written to enable basic functions, and the Perl scripting language was used to string sequences of operations together. 10-pin custom designed needle card was used to connect the wafer to the Micromate tester.

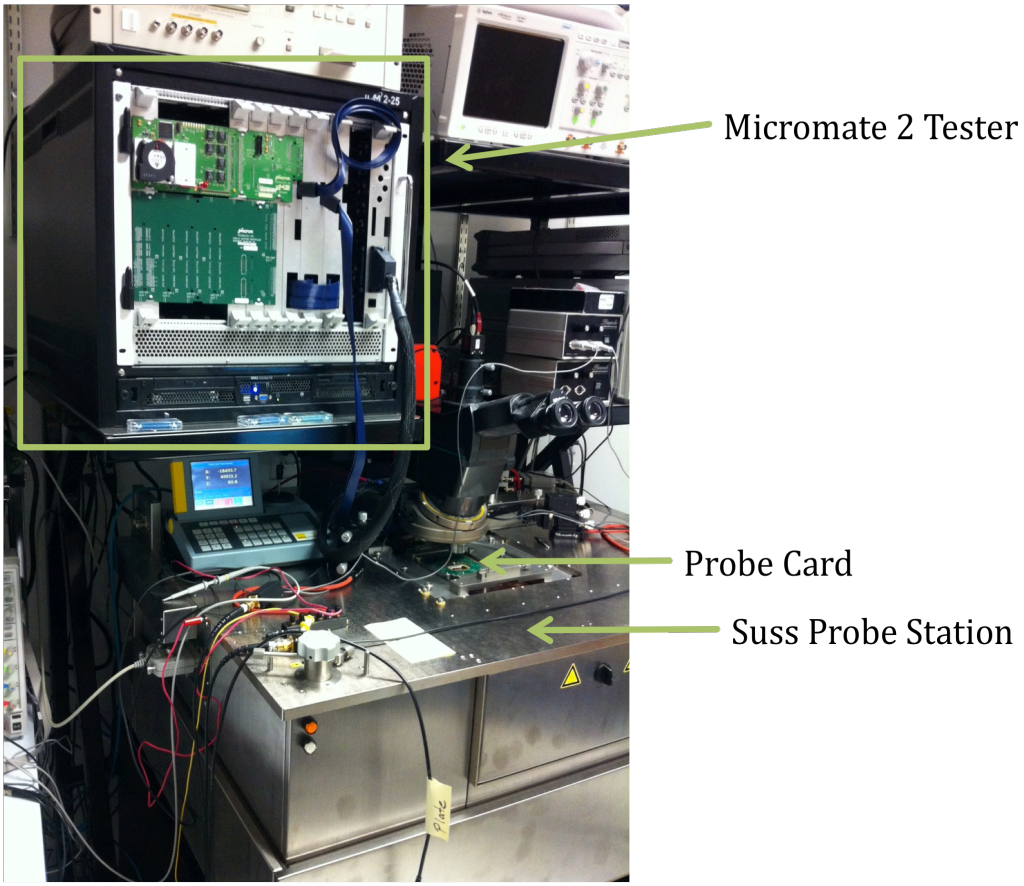


Figure 42 Micromate 2 Tester and Suss Probe Station

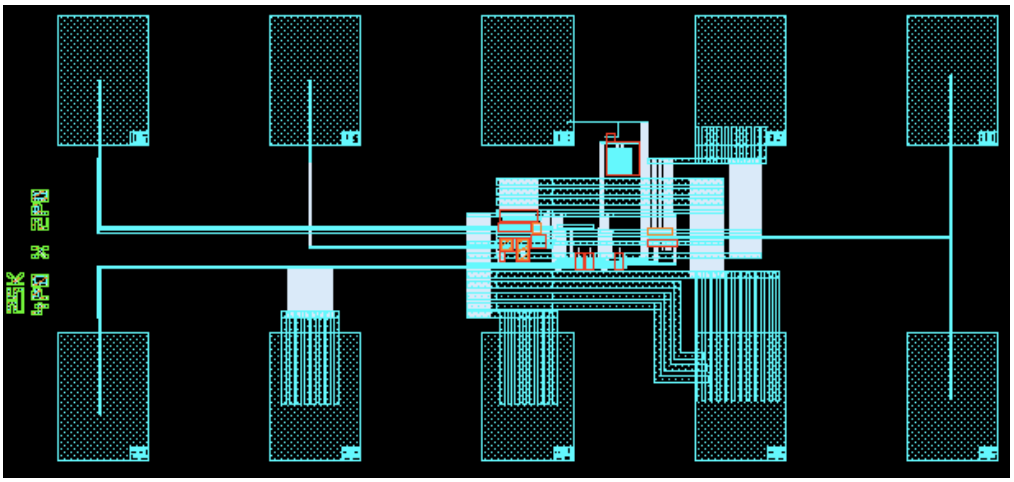


Figure 43 IRCV Layout

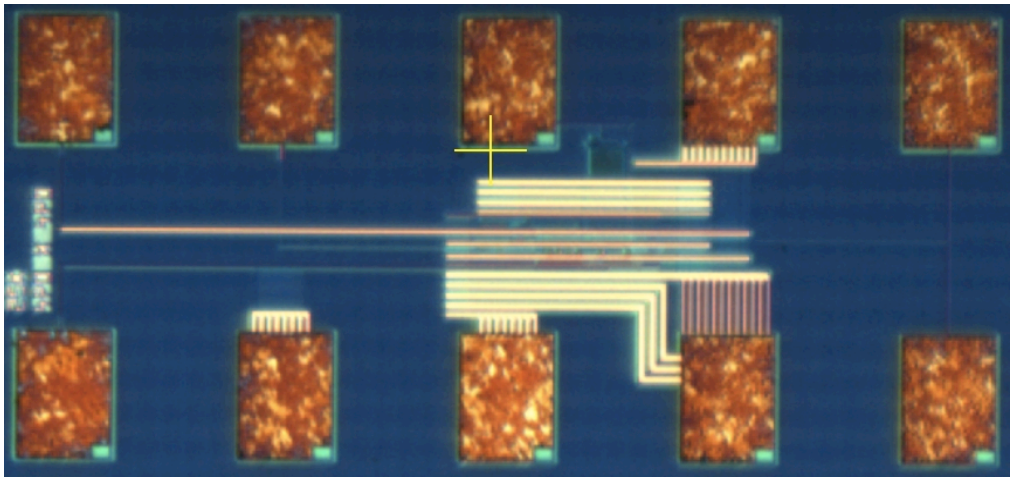


Figure 44 Micrograph of the IRCV

Basic functionality of the FWD/REV mux was confirmed using micro-probes to drop needles on test points at the top and bottom nodes of the RRAM memory cell. To keep parasitic capacitances low, 2 μm x 2 μm metal pads (mini-pads) were used for the micro-probing, using Model 28 probes from Picoprobe. These probes have an input capacitance of 40 fF [23], so were used to verify functionality, but might add too much parasitic capacitance to verify switching behavior.

Read measurements were done using the built-in current measurement unit available in each power supply on the Micromate. Pin drivers were used to drive the FWD/REV inputs, and power supplies were used for the BIASN and I_COMP inputs. A dedicated circuit on the probe card was used to pulse the V_TOP input. This circuit is shown in Figure 45. This circuit is a solid-state relay, controlled by another pin driver that provides the PULSE input. A power supply provides the normally open (NO) V_{SET} voltage and ground is connected to the normally closed (NC) input. The fastest clean pulse that can be given with this circuitry is ~ 50 *ns*. For this work, 100 *ns* pulses were used to ensure that good quality pulses were generated. V_{DD} was connected to a power supply driving 5 *V* to the IRCV.

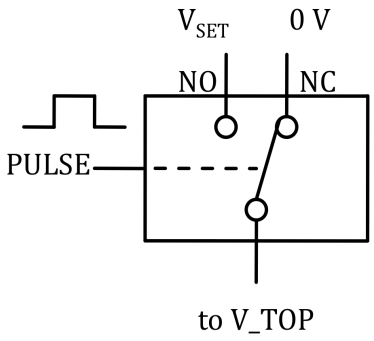


Figure 45 Voltage Pulse Circuit on Card

The DC I-V sweep of the compliance mirror is shown in Figure 46 and Figure 47. To set up this sweep, the FWD and REV inputs are both held high, shorting the input to the current mirror, and shorting out the RRAM cell. Note that even very small currents can be accurately mirrored. For the higher voltages and currents, the current mirror starts to show some non-idealities. At currents > 70 μA, the mirrored current starts to show a slope > 0, which is normally attributed to short-channel effect. It is not known why this inconsistency exists, but could be due to incorrect bias on BIASN, or could be due to a

difference between the models and the silicon. At voltages > 4 *V*, the current increases non-linearly, as was seen in simulation. This is attributed to insufficient BIASN voltage due to an error in the connection of the circuit. The max voltage that can be applied is 1.5 *V* on BIASN, where the simulation still shows the non-linearity above 4 *V*.

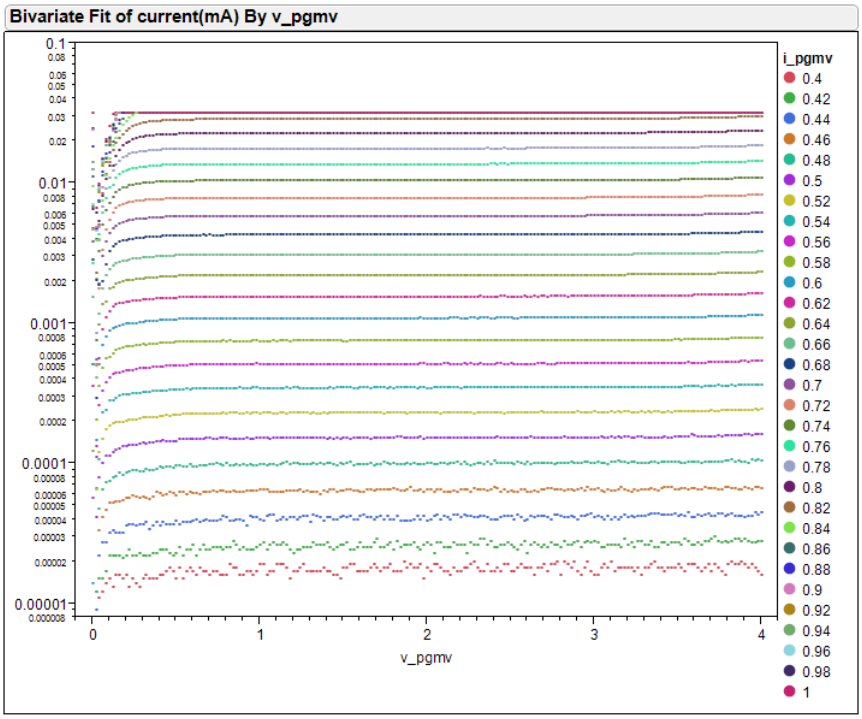


Figure 46 Compliance Mirror I-V

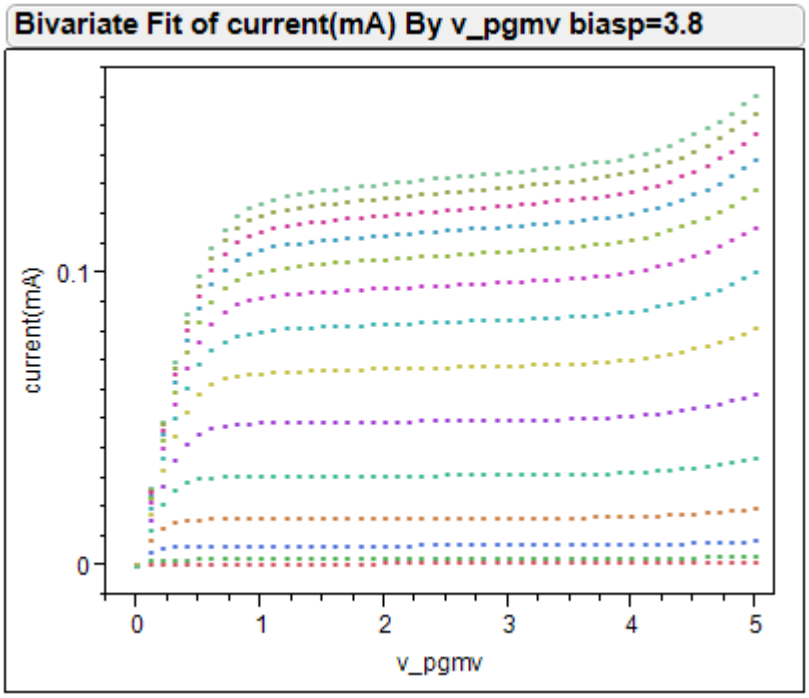


Figure 47 Compliance Mirror I-V, High Range

The Forming, and SET operations are shown in Figure 48. The top and bottom of the memory cell can be seen in yellow and green respectively. The red trace is the voltage pulse applied to the V_TOP input, and the blue trace is the FWD signal. The compliance current was 100 μA in these sequences for both Forming, SET and RESET. As can be seen in the figure, this is a pulsed VSET operation, since the FWD pulse is applied first, then the pulse is defined by the V_TOP input (which is VSET in this case). The dut_top (green) node goes high, and the dut_bot (yellow) node stays low at the beginning of the pulse. In the middle of the pulse, a dip is seen on dut_top, and the dut_bot node rises up as the current in the RRAM cell exceeds the current compliance value. This dip indicates some series resistance exists between the applied pulse (red) and the top of the RRAM cell. Knowing the compliance current value, the voltage between dut_top and dut_bot should give us an indication of what the cell resistance is.

We see ~0.8 *V* delta between dut_top and dut_bot, for an R_{CELL} of ~8 $k\Omega$ for a 100 μA current.

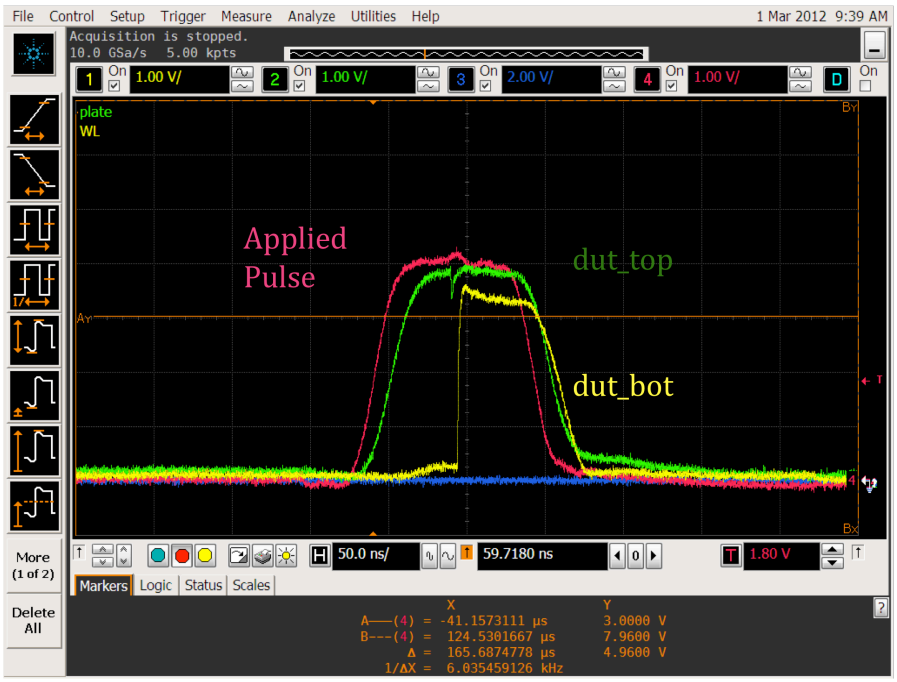


Figure 48 Forming/SET of RRAM Cell

One interesting item to note is that the dut_top and dut_bot nodes do not stay at ground, but float up to an intermediate value. At the beginning of the waveform, both nodes are seen to be ~2.5 *V* before the FWD signal turns on. An issue was discovered related to the ~2.5 *V* that had to be resolved to see successful switching. In the HRS state, when one of the FWD or REV inputs is switched high, only one side of the memory cell is grounded, leaving ~2.5 *V* on the other side of the cell. This causes a partial SET to occur because of the parasitic capacitance. Although it's not pictured, the solution was to pulse both the FWD and REV inputs for a short time at the beginning of the operation to discharge both dut_top and dut_bot to ground.

The RESET operation of the RRAM cell can be seen in Figure 49. In this case, the REV signal is shown as the blue trace. This is again a pulsed VRESET operation

since the FWD/REV inputs are driven before the V_TOP input. Some insight about the RRAM cell can be gained by looking at the waveforms. As the dut_top node rises (yellow), the dut_bot node stays at 0 V until a certain point. At that point, the dut_bot node (green) starts to rise as the current compliance level is reached. The dut_bot node then decreases, indicating an increase in resistance of the RRAM cell. This happens several times as the V_TOP input is ramped up, indicating multiple events during the RESET operation. Also curious is the small spike in the dut_bot node in the middle of the pulse. This is likely to be caused by the noise visible on the V_TOP node increase the voltage across the cell at that moment, and driving another event.

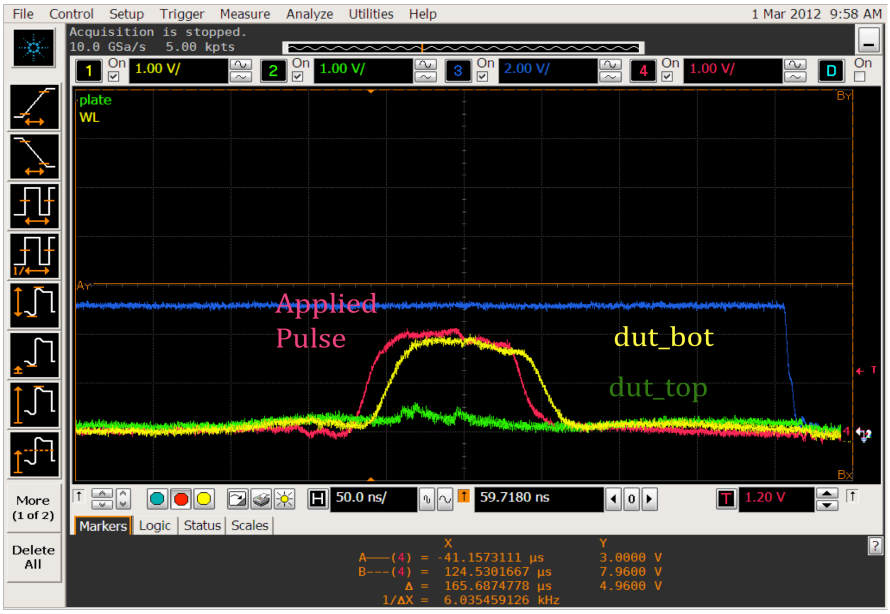


Figure 49 RESET of RRAM cell

The final test of the IRCV is to see if we can continue the trend of lower compliance current to higher resistance. In experimenting with various RRAM cells, it has been observed that they are very non-repeatable in nature. This is likely due to the filament formation and dissolution process. The filament likely does not look the same from one SET operation to the next, and therefore shows different electrical

characteristics. Figure 50 shows the relationship between the compliance current during SET operation and the resistance of the RRAM cell on the subsequent read. To establish the trend, multiple operations were performed at each compliance level on a single bit. The resistance was measured after each SET operation, and the average of the operations for that compliance current is reported in the figure. It can be seen that the resistance of the cell does increase with decreasing compliance current, as one might expect. It is also interesting to note that at very low compliance currents, switching stopped altogether, and the RRAM cell simply remained in the RESET state. This indicates that the parasitic capacitance of the IRCV is low enough that it will not set a cell by itself. It remains to be seen if the parasitic capacitance still has some other impact on the switching behavior.

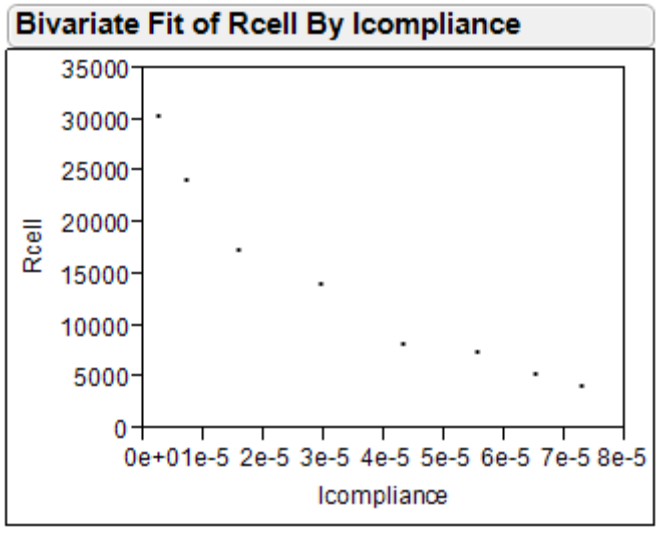


Figure 50 RRAM Cell Resistance as a Function of Current Compliance

CHAPTER FIVE – CONCLUSIONS

The IRCV was successfully designed, simulated and tested. It was shown to operate as expected in the range of currents simulated, and was able to form, set, and reset cells. Some complications had to be overcome in order to see functionality, including pulsing both FWD and REV at the same time to discharge leakage on the cell nodes. This underscores the need for flexibility when designing a test circuit, which was critical in enabling unforeseen issues to be overcome.

RRAM cells are inherently random, and data collection methodology must account for this to establish trends. Larger numbers of data points would help to this end, so future work should employ automated data collection to simplify the process and make it less error prone.

Although this work has posited that there is such a thing as an "ideal" characterization vehicle, it is obvious that no such ideal exists. Tradeoffs between voltage drop, linear region of the compliance mirror, and parasitic capacitance will always need to be made, and so must be chosen according to the specific device characterized.

As a future step, multiple placements of the IRCV with different sizing of current mirrors would be helpful. This would allow a varying current capacity as well as a varying amount of parasitic capacitance. In addition, although the mux gives additional flexibility, it also adds parasitic capacitance. Two placements of the IRCV without the

mux, one with the compliance mirror connected to dut_top and one with the mirror connected to dut_bot could give similar functionality with a lower capacitance.

Another avenue to investigate would be to intentionally add capacitance on the V_BOT node. This could be done with a mux connecting various sizes of MOS capacitors to the V_BOT node. The ability to characterize the same RRAM memory cell with multiple capacitances on the V_BOT node would help determine how much capacitance really affects the SET state of the cell, and might allow trends to be made showing the effect of capacitance down to levels that practically are impossible to implement on silicon.

The IRCV is a good first step in creating a flexible characterization vehicle for RRAM technologies. It gives flexibility to process the memory cell in either orientation, and can apply current compliance in both the SET and RESET direction. Data collection is automated through scripting, and auto-probing could be enabled for even greater statistical data collection.

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