MOSFET MODULATED DUAL CONVERSION GAIN CMOS IMAGE SENSORS

By

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I have read this dissertation and have found it to be of satisfactory quality for a doctoral degree. In addition, I have found that its format, citations, and bibliographic style are consistent and acceptable, and its illustrative materials including figures, tables, and charts are in place.

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ABSTRACT

MOSFET Modulated Dual Conversion Gain CMOS Image Sensors

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In recent years, vision systems based on CMOS image sensors have acquired significant ground over those based on charge-coupled devices (CCD). The main advantages of CMOS image sensors are their high level of integration, random accessibility, and low-voltage, low-power operation. Previously proposed high dynamic range enhancement schemes focused mainly on extending the sensor dynamic range at the high illumination end. Sensor dynamic range extension at the low illumination end has not been addressed. Since most applications require low-noise, high-sensitivity, characteristics for imaging of the dark region as well as dynamic range expansion to the bright region, the availability of a low-noise, high-sensitivity pixel device is particularly important.

In this dissertation, a dual-conversion-gain (DCG) pixel architecture was proposed; this architecture increases the signal to noise ratio (SNR) and the dynamic range of CMOS image sensors at both the low and high illumination ends. The dual conversion gain pixel improves the dynamic range by changing the conversion gain based on the illumination level without increasing artifacts or increasing the imaging readout noise floor. A MOSFET is used to modulate the capacitance of the charge sensing node. Under high light illumination conditions, a low conversion gain is used to achieve higher full well capacity and wider dynamic range. Under low light conditions, a high conversion gain is enabled to lower the readout noise and achieve excellent low light performance.

A sensor prototype using the new pixel architecture with 5.6µm pixel pitch was designed and fabricated using Micron Technology's 130nm 3-metal and 2-poly silicon process. The periphery circuitries were designed to readout the pixel and support the pixel characterization needs. The pixel design, readout timing, and operation voltage were optimized. A detail sensor characterization was performed; a 127*μV/e* was achieved for the high conversion gain mode and 30.8*μV/e* for the low conversion gain mode. Characterization results confirm that a 42*ke* linear full well was achieved for the low conversion gain mode and 10.5*ke* for the high conversion gain mode. An average 2.1*e* readout noise was measured for the high conversion gain mode and 8.6*e* for the low conversion gain mode. The total sensor dynamic range was extended to 86*dB* by combining the two modes of operation with a 46.2*dB* maximum SNR. Several images were taken by the prototype sensor under different illumination levels. The simple processed color images show the clear advantage of the high conversion gain mode for the low light imaging.

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CHAPTER 1 INTRODUCTION

1.1 CMOS Image Sensors vs. CCD Image Sensors

The market for the solid-state image sensors has been experiencing explosive growth in recent years due to the increasing demands of mobile imaging, digital still and video cameras, internet-based video conferencing, automotive imaging, surveillance, and biometrics [1]. A block diagram of a digital imaging system is shown in figure 1.1 [1].

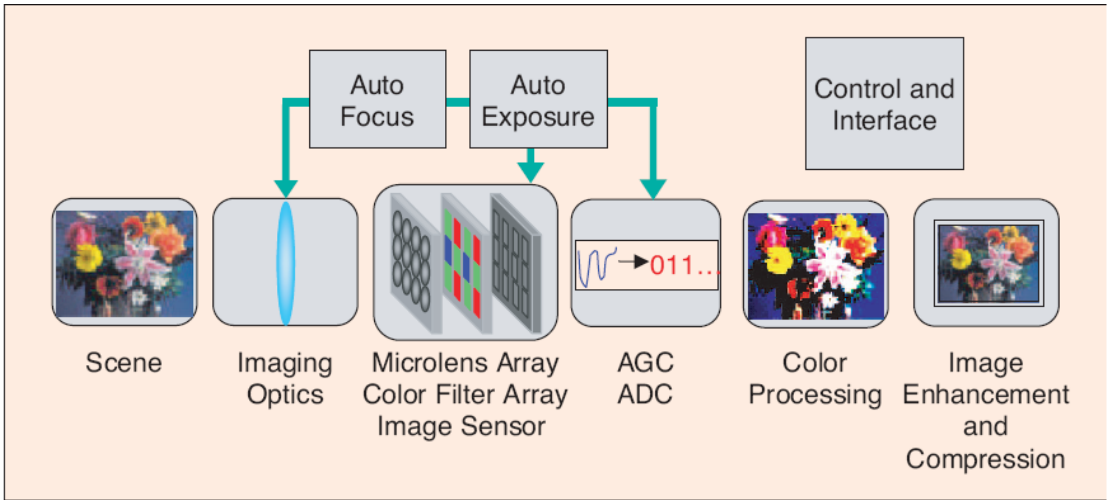


Figure 1.1: A block diagram of digital imaging system [1]

First the scene is focused on the image sensor using the image optics. An image sensor comprising a two-dimensional array of pixels converts the light incident at its surface into an array of electrical signals. These electrical signals are read out of the image sensor and digitized by an analog-to-digital converter (ADC). A significant amount of digital signal processing is employed for color processing, image enhancement, and image compression. Other processing and control operations are also included for performing auto-focus, auto-exposure, and general camera control. Even though each component shown in the figure plays a role in determining its overall performance, the image sensor is the key component, which sets the ultimate performance limit [1].

There are two types of image sensors: CCD (Charge-Couple Devices) image sensors and CMOS (Complementary Metal Oxide Semiconductor) image sensors [1] [2]. The idea of the CMOS imager was first proposed in late 60's [3] [4], about the same time as CCDs [5]. Because the CMOS imagers required the incorporation of transistors into each pixel, which was not feasible at that time due to the large transistor size, the CCD has become the dominant digital technology ever since. In recent years, with the device scaling trend, vision systems based on CMOS image sensors have acquired significant ground over those based on CCD image sensors.

In general, the CCD and CMOS image sensors have no difference in their photo sensing principle. Both devices utilize silicon as the sensing material. The collected photo charges by the image sensors represent the intensity of the incident light. What differentiates these two types of image sensors is where and how the photocharges are converted into an electrical signal and in which form the signal is transferred out of the array. In the CCDs, the electric charges collected by the photodetector array during exposure time are transported sequentially through a series of coupled-gates until the final floating diffusion node performs charge-to-voltage conversion [6]. In order to assure the amount of photo charges is intact during transportation, special device structures, such as coupled poly gates, are developed. The CCD process has evolved into a specialized process among silicon technologies to accommodate these device structures. With more than 30 years of research and development, the CCDs are able to achieve high-quality image sensing in terms of large fill factor, lower dark current level, and lower fixed pattern noise (FPN) compared to the other existing imaging technologies [6]. However, the CCDs have a slow readout speed and high power consumption. The CCDs are fabricated using a specialized process with optimized photodetectors; photodetectors have very low noise and good uniformity. However, this specialized process is not suitable for building efficient transistors and circuits and is incompatible with the standard CMOS process, so the CCD sensors cannot be integrated on the same CMOS chip with the rest of the circuitry [7]. Therefore, a CCD image sensor usually requires another supporting chip to provide control signals and perform signal processing, which could potentially increase the manufacturing cost.

Unlike the CCD imagers, the CMOS image sensors convert photo-generated charges into a voltage signal in the pixel. Because of the early charge-to-voltage conversion, the electrical signal can possibly be processed with analog or digital circuits, which are available from the standard CMOS technology. It is easy to integrate a CMOS image sensor process into an existing commercially available CMOS process with some minor extra steps for color imaging and micro-lens. It can thus significantly reduce the manufacturing cost and increase the yield.

Low power consumption is an important criterion for modern mobile electronics [8]. In this area, the CMOS image sensors offer better performance than the CCDs. That is because the CCDs require high voltage to create a potential well to prevent the overflow of the photo generated charges. Also the control of CCDs needs several different voltage levels and high frequency clock signals to ensure the proper operation and perfect charge transfer efficiency. As a result, the CCD device is a very power hungry device, typically on the order of 1W. In contrast, the CMOS image sensors utilize the same supply voltage of standard CMOS technology, which is continuously scaling down for the optimization of general logic circuits [9].

The CMOS image sensors have another advantage that is difficult to achieve by the CCDs – on-chip signal processing innovation. Because of the small transistor size available from the modern CMOS process, more complicated processing circuitries can be included on chip to extend the functionalities and performance of imaging systems, such as noise reduction, dynamic range expansion, multi-resolution, or motion detection. The incorporation of circuits on CMOS image sensor has expanded the dimension of the system-on-chip (SOC) applications [10].

Other advantages of the CMOS image sensors include random accessibility [1] [2] [11] [12] [13], high frame rate [14], more functionality and ability to extend to very large resolution, which are all limitations of the CCDs.

1.2 Motivations

The signal-to-noise-ratio (SNR) and dynamic range (DR) are very important figures of merit for image sensors [7]. The dynamic range quantifies the sensor’s ability to adequately image both high light and low light scenes. The CMOS image sensors generally suffer from high read noise and non-uniformity, resulting in lower SNR and lower dynamic range than the CCDs [7]. However, more recently, some CMOS image sensors have achieved high quality imaging performance compared to that of the CCDs [15].

Several techniques and architectures have been reported for extending image sensor dynamic range. Previously proposed high dynamic range enhancement schemes focused mainly on extending the sensor dynamic range at the high illumination end; the sensor dynamic range extension at the low illumination has not been addressed. For some schemes, the increase in dynamic range comes at the expense of a decrease in SNR, and for others, the SNR is the same since the sensor readout noise is not reduced [7].

Since most applications require low-noise, high-sensitivity, and characteristics in imaging of the dark region as well as dynamic range expansion to the bright region, the availability of a low-noise high-sensitivity pixel device is particularly important [16] [17] [18] [19]. Thus, there is an urgent need to design a CMOS image sensor which enhances the SNR and dynamic range of CMOS image sensors at both low and high illumination ends.

In this dissertation, a new pixel architecture called MOSFET modulated dual conversion gain pixel is developed. The dual conversion gain pixel is proposed to improve the sensor dynamic range by changing the conversion gain based on illumination levels without increasing artifacts or increasing the imaging readout noise floor. A MOSFET is used to modulate the floating diffusion node total capacitance and thus the conversion gain. The gate of the dual conversion gain transistor is connected to the floating diffusion node; both the drain and source terminals are driven by a DCG control signal. The floating diffusion node total capacitance and the conversion gain are modulated by the voltage applied to the drain and source terminals. Under the high light illumination, a low conversion gain is used to achieve a higher full well capacity and wider dynamic range. Under low light conditions, a high conversion gain is enabled to lower the readout noise and achieve excellent low light performance.

The pixel design, readout timing, and operating voltage are optimized to increase the sensor SNR and extend the sensor dynamic range. A sensor prototype using the new pixel architecture was designed and manufactured using Micron Technology's 130nm process. A detailed sensor characterization was obtained.

1.3 Dissertation Organization

This dissertation is organized into six chapters. Chapter 2 will give some background information about the CMOS imager sensor design, which will start with the optical absorption and photo conversion; then several CMOS image sensor architectures will be presented, followed by the noise analysis of the CMOS image sensors, literature review of the SNR improvement techniques, and dynamic range enhancement schemes. Finally, the state-of-the-art sensor performance will be represented.

Chapter 3 will present the MOSFET modulated pixel design, pixel operation principle, and some SPICE simulation results. The pixel layout design, operating voltage levels, and readout timing will be optimized to reduce the readout noise, and to increase the sensor SNR and dynamic range.

Chapter 4 will present the sensor prototype periphery design, which will include the row decoder and driver design, column decoder and column sample and hold circuitry design, column bias current design, and switch capacitor low noise amplifier design. The existing characterization hardware employs a very good 12-bit ADC on the board, so ADC design will not be included in this work.

Chapter 5 will provide the sensor characterization results, which will include light signal characterization, pixel responsivity measurement, conversion gain measurement, full well capacity measurement, readout noise measurement and the photon transfer curve for both the low and high conversion modes. The spectral quantum efficiency, crosstalk, dark current, and hot pixel performance will be characterized as well.

Chapter 6 will give a summary of the results, provide conclusions, and give suggestions for future work.

CHAPTER 2 OVERVIEW OF CMOS IMAGE SENSORS

2.1 Optical Absorption and Photodiode Operation

When photons with energy $E = hc_0/\lambda$ (where h is the Plank's constant, c_0 the velocity of the light in vacuum, and λ is the wavelength of the light) greater than the band-gap energy are incident on a semiconductor, some of the photons are absorbed and others are reflected. The absorbed photons excite the electrons from the valence band to the conduction band, and thus the electron-hole (e-h) pairs are generated. For an indirect band-gap material, such as silicon, such movement requires a change in energy as well as the change in momentum. While the incident photon provides the necessary energy for the electron excitation from the valence band to the conduction band to take place, the change in momentum, however, must be assisted by lattice vibration, resulting in the reduction of the transition probability. The degree of the optical absorption is indicated by the absorption coefficient α, which varies with semiconductor materials. In the visible spectrum, the α is a decreasing function of wavelength. The intensity of light at the depth x traveled into the semiconductor can be expressed by [20].

$$I(x) = I_0 \exp(-\alpha x) \tag{2.1}$$

where I_0 is the light intensity at the surface.

A photodetector is used to convert the photo generated e-h pairs into photocurrent. A common photodetector used in CMOS image sensors is the photodiode, where the built-in p-n junction provides the electric field for the collection of generated charges. Figure 2.1 shows the band diagram of the p-n diode and the movement of generated e-h pairs under the reverse biased p-n junction [20].

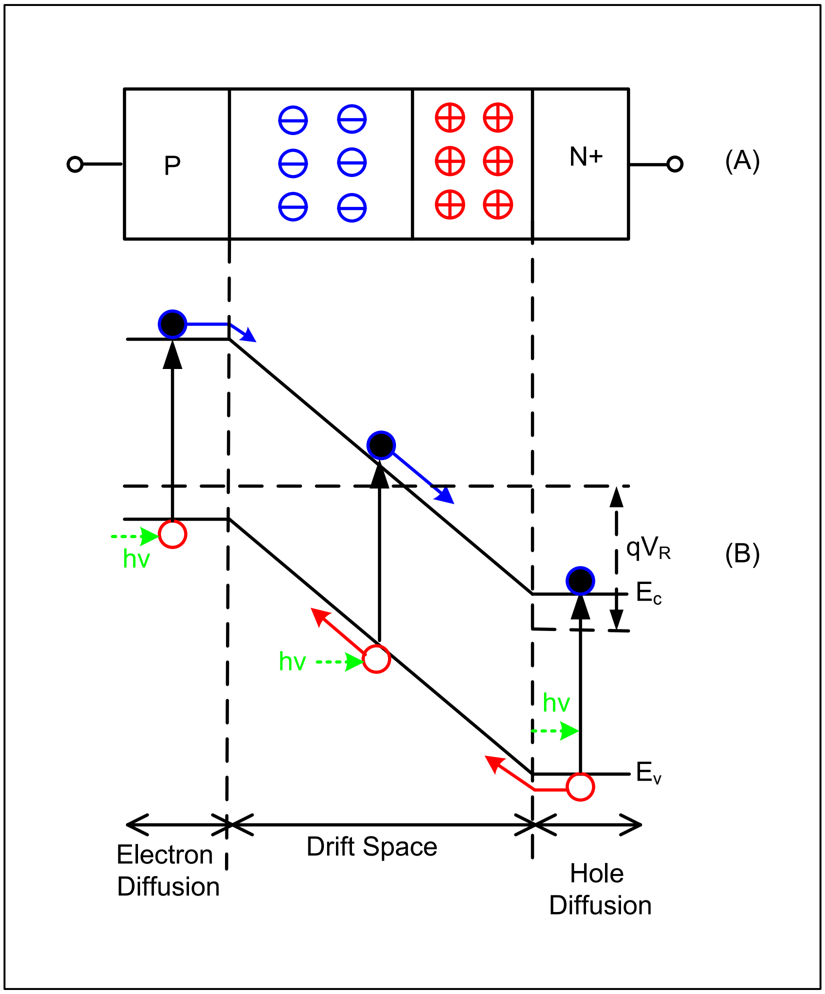


Figure 2.1: Operation of photodiode. (A) Cross-sectional view of PN diode. (B) Energy band diagram under reverse bias [20]

The total photocurrent generated in the photodiode comes from two regions: the depletion region and the quasi-neutral region. While the carriers in the depletion region are collected completely under electric field, the carriers in the quasi-neutral regions often recombine randomly and only those successfully diffused to the depletion regions are collected. The charge collection in the neutral-quasi region depends on the depth of diffusion length, which is the function of the doping concentration, and the depth where the generation occurs (a function of wavelength). The actual number of e-h pairs generated by the incident photons is measured by quantum efficiency (QE) defined as the ratio of the photocurrent generated by the photodetector to the photon flux incident on the device [1]. The rapid decrease in the quantum efficiency with longer wavelengths is determined by the band-gap energy of the material. The gradual decrease at shorter wavelengths is because the optical absorption tends to happen close to the surface and the carriers are increasingly lost due to the interface recombination [21]. The optical generation rate is given by $G(x) = QE \cdot \alpha \cdot I(x)$, with its value falling exponentially from the surface.

The detail derivation of steady-state current density of an N+/P-substrate photodiode is described in [20]. Assuming the absorption in the top doped region and thermal current effect are negligible, the total current density of the photodiode is given by:

$$J_{total} = J_{drift} + J_{diffusion} = qI_0\left[1 - \frac{\exp(-\alpha W)}{1 + \alpha L_n}\right] + qN_{p0}\frac{D_n}{L_n} \tag{2.2}$$

where $L_n = \sqrt{D_n \tau_n}$ the diffusion length, D_n is the diffusion coefficient for electrons, τ_n is the minority carrier lifetime, W is the depletion width, and N_{p0} is the electron density at equilibrium.

Under normal operating conditions, the second term involving N_{p0} is much smaller so that the total current is proportional to the light intensity at the surface I_0. The maximum quantum efficiency can be obtained:

$$QE = \frac{J_{total}}{qI_0} = 1 - \frac{\exp(-\alpha W)}{1 + \alpha L_n} \tag{2.3}$$

Since the typical photocurrent in the range of a few *fA* to a few *nA* is hard to detect [22], a typical photodiode commonly operates under the integration mode, which can be modeled as shown in Figure 2.2, where the capacitance *C* represents the junction capacitance of the photodiode. In this mode, the photodiode is first reset to a reverse bias voltage of V_{pix}. During the integration, the photocurrent discharges the photodiode capacitance causing its voltage to drop at a rate that is ideally proportional to the photocurrent. After the integration, the final voltage is sampled, representing the average light intensity during the integration time. The pixel is then reset again, and the process is repeated for the next frame.

Ignoring dark current, the voltage at node V_{out} is given by [22]:

$$V(t) = \left(V_{pix}^{1/2} - \frac{i_{photon} t}{A(2q\varepsilon_{si} N_A)^{1/2}} \right)^2 \tag{2.4}$$

where N_A is the acceptor concentration in the substrate, ε_{si} is the dielectric constant of silicon, A is the diode area, and $i_{photon} = J_{total} A$ is the photocurrent. From Equation 2.4, it is found that the $V(t)$ is linearly related to the light intensity for a short time period. Light intensity to voltage conversion is thus obtained.

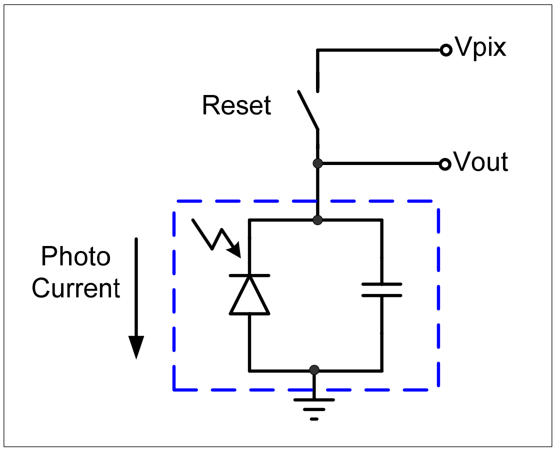


Figure 2.2: Integration operation in a photodiode

2.2 Overall Architecture of CMOS Image Sensors

An overall architecture of a CMOS imager sensor is shown in Figure 2.3. The image sensor consists of an array of pixels. The pixels in the array are addressed through the horizontal line, and the charge or voltage signal is read out from each pixel through the vertical column line. The readout is done by transferring one row at a time to the column storage capacitors, then by reading out the row using the column decoder and multiplexer. This readout method is similar to a memory structure. The column amplifier can achieve functions such as sample and hold, correlated double sampling, providing bias current for the pixel array, and variable gain control. The output amplifier can provide extra output buffer to prevent signal feed through and to increase the driving capacity to the following large load, such as ADC or bonding pad.

Most of the state-of-the-art CMOS image sensor chips may also contain on-chip ADCs to achieve the digital-camera-on-a-chip approach. They can be placed either in column-parallel or shared by all the column signal processing blocks. The digital output of the ADCs (or analog output without on-chip ADC) is selected for readout by a column decoder. A timing and control digital block is also integrated on the chip to control the system operation and coordinate all parts of the circuits. This digital block is usually defined at a high level using tools such as VHDL or VERILOG HDL and implemented on-chip using automated synthesis and auto-routing tools.

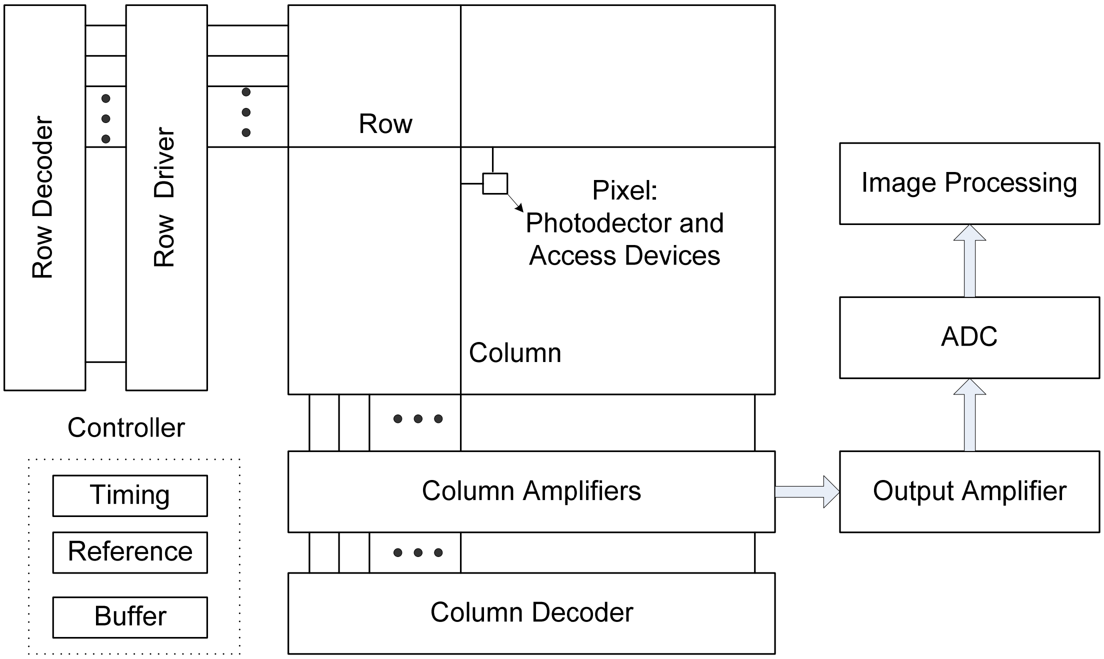


Figure 2.3: Block diagram of a CMOS image sensor

The existence of the row and column select mechanism helps to permit several modes of the image readout, which could be preset by the users in the digital control block. Normally there are two readout modes the CMOS image sensor can support. One is called Electronic Rolling Shutter (ERS) mode, and the other is called Global Reset Release (GRR) mode (or snap shot mode). The ERS mode, shown in Figure 2.4, employs two operations: *RESET* and *READ* to define the length of the pixel exposure time during image capture. The *RESET* operation affects all of the pixels in a row and essentially puts the pixels in a state to convert light into an electrical signal. The image sensor circuits cause the signal to be sequentially applied to each row in the image sensor in order to capture a full frame of image. At some fixed interval after the reset operation, a *READ* signal is applied to all pixels in a row causing the electrical signals from each pixel in a row to be transferred to column sample and hold circuitry. The *READ* signal is sequentially at the same speed of the reset signal, producing an effective window of exposure that rolls over the image sensor. It is easy to see that the effective exposure time of an image capture with this method is determined by the separation (in time) of the *RESET* and *READ* signals. [23]

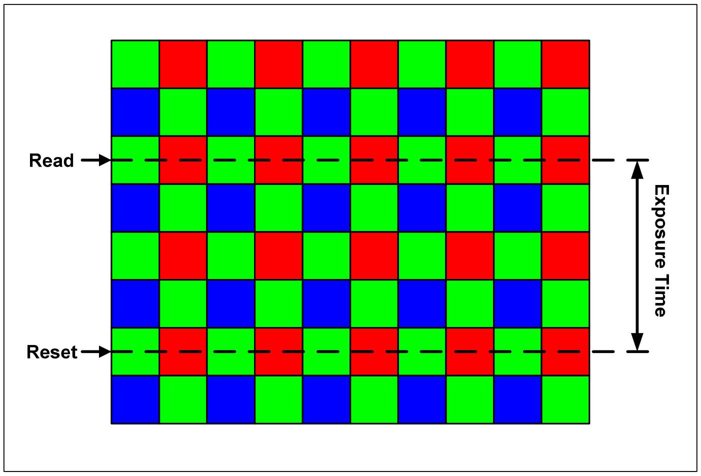


Figure 2.4: Electronic Rolling Shutter (ERS) mode image capture

In order to use a mechanical shutter, simultaneous reset for all pixels, called global reset or a fast reset scanning, is necessary. The Global Reset Release (GRR) mode, shown in Figure 2.5, is quite different from the ERS mode. First, all the pixels are reset simultaneously, or a reset scan is completed while the mechanical shutter is closed. Pixels on each row start integration after the reset. Then the mechanical shutter opens for a predetermined period of time, which corresponds to the light exposure time. Pixel readouts start after the mechanical shutter is closed. Similar to the ERS mode, the pixels are read out row by row.

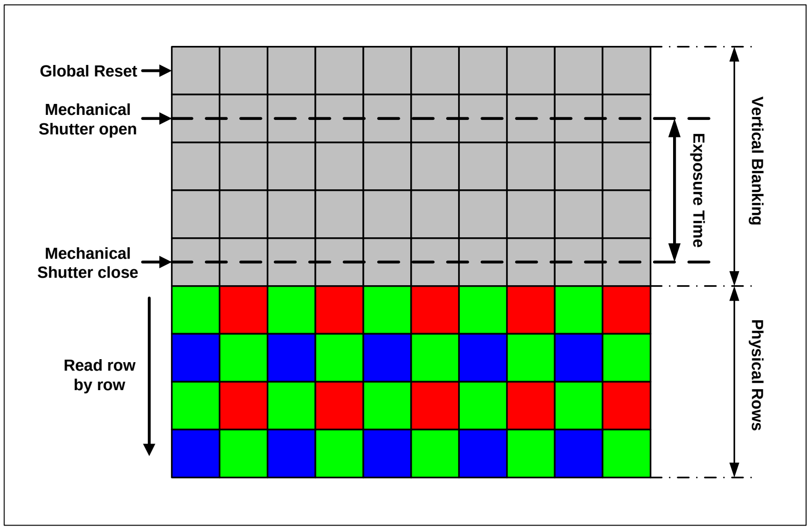


Figure 2.5: Global Shutter Release (GRR) mode image capture

Beside the normal progressive scan readout mode, a window readout mode can be implemented where only a smaller region of pixels is selected for readout. A skip readout mode is also possible where every second (or third, etc.) pixel is read out. The mode allows for sub-sampling of the image to trade off between the readout speed and resolution [9].

2.3 Pixel Architecture

The CMOS image sensors can be divided mainly into two groups: Passive Pixel Sensors (PPS) and Active Pixel Sensors (APS) [11]. The active pixel sensor is so named because it contains an active amplifier, which doesn’t exist in the passive pixel. The active pixel sensor is the most popular architecture for today [1].

2.3.1 Passive Pixel Sensor (PPS)

The photodiode passive pixel approach was first suggested by Welker in 1967 [22] [24]. The passive pixel concept is shown in Figure 2.6. It only consists of one photodiode and a passive transistor, which is controlled by the transfer gate. When the access transistor is activated, the photodiode is connected to a vertical column bus.

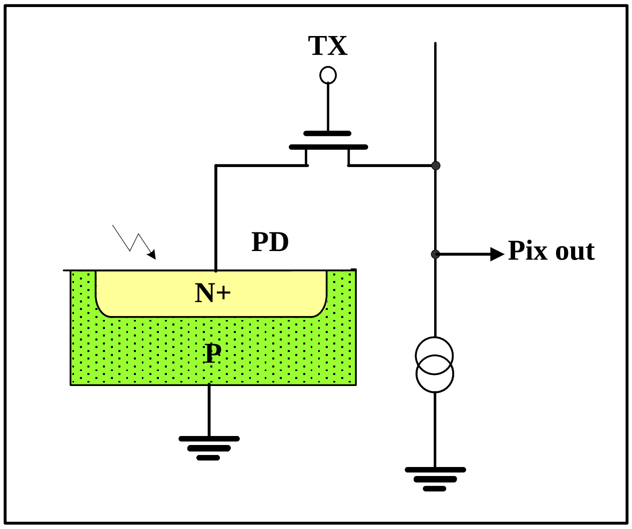


Figure 2.6: Schematic diagram of a passive pixel sensor (PPS)

Normally a charge integration amplifier (CIA) readout circuit at the bottom of the column bus keeps the voltage on the column bus constant [4]. When working, a reset phase is firstly performed after turning on the pass transistor, and then the photo generated charge, which is proportional to the incident light intensity, is integrated and converted to a voltage by the CIA. The fill factor, which is the ratio of the photosensitive area to the pixel size, of the passive pixel can be very large due to the existence of only one pass transistor with a given pixel size and particular CMOS process [9].

The major problems of the passive pixel are also very obvious. Because the signal path is directly connected to the column bus without a buffer, the readout noise is normally one order of magnitude higher than other pixel architectures. As the number of columns increases, the readout speed slows down due to the driving of the large column load capacitance. So the passive pixel does not scale well to large array size or for fast pixel readout speed.

2.3.2 Photodiode Active Pixel Sensor (APS)

A sensor with an active amplifier within each pixel is referred to an active pixel sensor or APS. In contrast with the passive pixel, the active pixel incorporates a buffer (or amplifier) into the pixel to significantly improve the performance of the pixel at the expense of lowering the fill factor. However, the loss in optical signal is more than compensated by the reduction in readout noise for a net increase in Signal-to-Noise-Ratio (SNR) and dynamic range. Also a microlens technology is commonly employed to recover some of the loss of optical signal and effectively increase the fill factor.

Figure 2.7 shows the schematic of the photodiode active pixel sensor. There are three transistors (3T) for each pixel: the reset (RST) transistor, source follower (SF) transistor, and row select (RS) transistor. The photodiode is normally a p-n junction biased in the reverse region. After applying an incident light, the photo generated carriers within the depletion region are separated by the junction electric field; the electrons are collected in the n^+ region and the holes in the p region. Almost all charges that are generated inside the depletion region are collected. However, photocharges generated too close to the surface in the n-diffusion region do not diffuse to the space charge region (or depletion region) but recombine at surface states. Since the blue light is absorbed close to the surface, the surface recombination leads a loss of blue light sensitivity. The large junction capacitance at the photodiode node results in a smaller conversion gain, and thus a lower sensitivity.

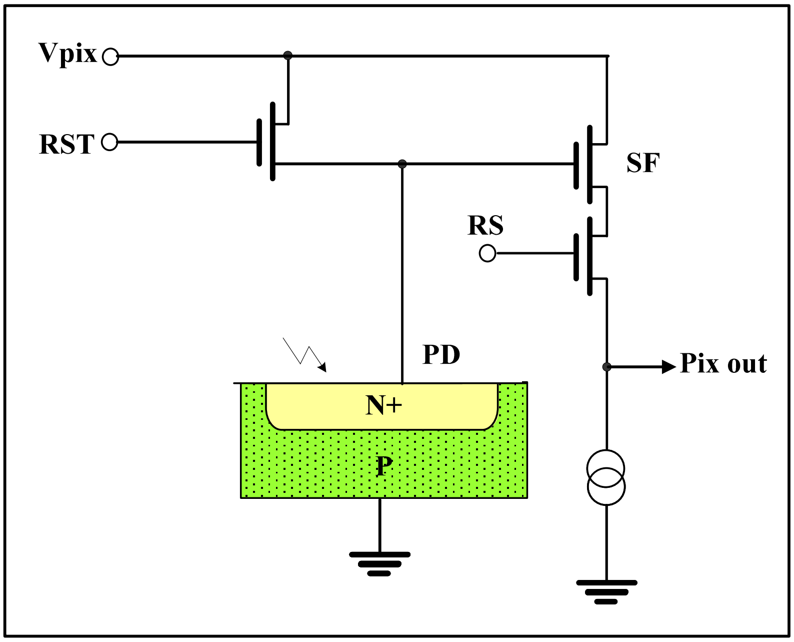


Figure 2.7: Schematic diagram of a photodiode active pixel sensor (APS).

Figure 2.8 shows the readout timing signals of the photodiode active pixel sensor. The photodiode voltage is read out through a source follower buffer and a row select transistor. After integration, a Sample-Hold-Signal (SHS) is turned on to sense the pixel output signal V_{SIG} and the signal is stored in memory. Then the RST transistor is turned on to reset the photodiode again. After reset, a Sample-Hold-Reset (SHR) signal is turned on to sense the pixel output signal V_{RST} again, and the signal is stored in another memory. The difference of these two signals $\left(V_{RST} - V_{SIG}\right)$ represents the integrated signal during this integration period.

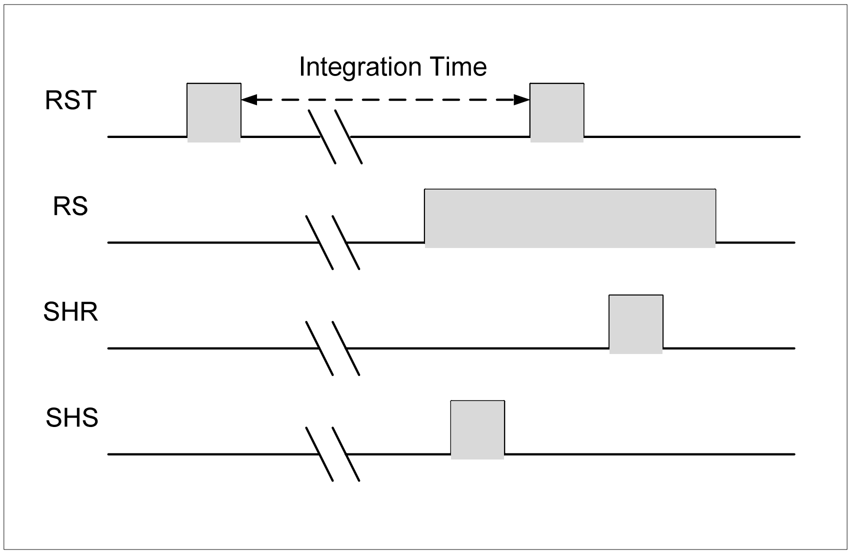


Figure 2.8: Photodiode active pixel sensor (APS) readout timing diagram

The signal integrated on a pixel is measured relative to its reset level. Since there is a reset operation between the two sample phases, the thermal noise uncertainty associated with this reset level is referred to as the reset or kTC noise. This noise comes from the thermal noise of the MOS switch. The photodiode APS (3T) readout timing is not true Correlated Double Sampling (CDS), so the reset noise is a significant problem for photodiode APS architecture [25].

2.3.3 Pinned Photodiode Active pixel Sensor (APS)

The Pinned photodiode active pixel sensor is the most popular sensor today. The idea actually comes from the buried channel CCD in the CCD technology to increase the sensitivity and reduce the dark current. It has proved to be equally beneficial for the CMOS image sensors. The schematic and cross-section of the pinned photodiode active pixel are shown in Figure 2.9.

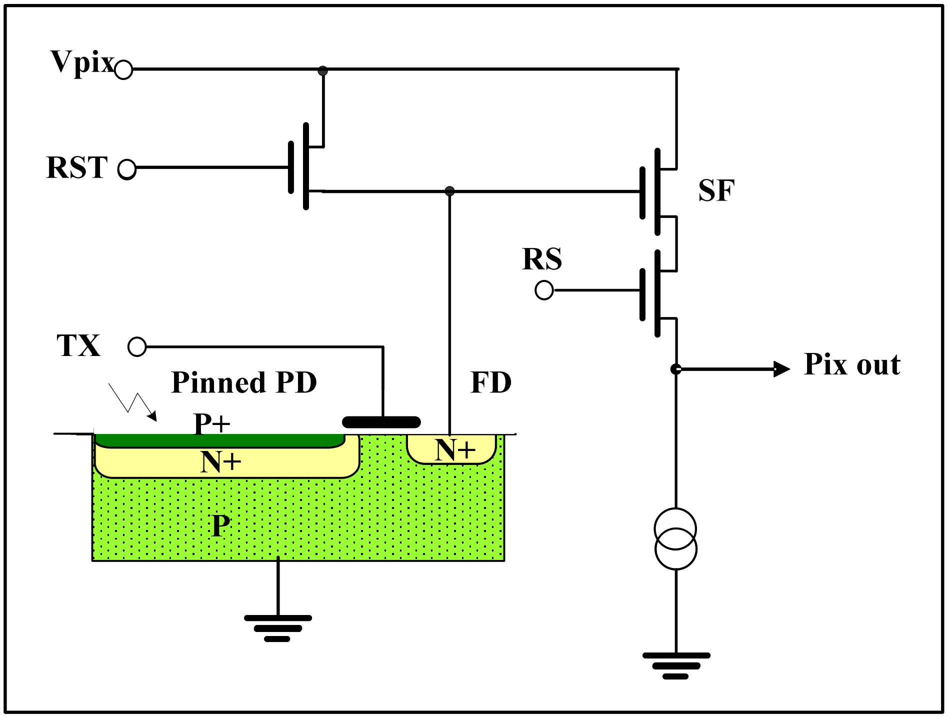


Figure 2.9: Schematic of a pinned photodiode active pixel sensor (4T APS)

The pinned photodiode pixel consists of a pinned diode (p^+-n^+-p), where the n^+ region is pulled away from the silicon surface in order to reduce the surface defect noise (such as due to dark current) [26]. As the voltage applied to the n^+ layer is increased, the depletion regions of both p-n junctions grow toward each other. At a certain voltage, the pinned voltage V_{pin}, the depletion regions meet. Besides the pinned photodiode, the pixel consists of four transistors (4T) that include a transfer gate (TX), reset transistor (RST), source follower (SF), and row-select (RS) transistor. The transfer gate separates the floating diffusion (FD) node from the photodiode node, which makes the correlated double sampling (CDS) readout possible, and thus lower noise.

The readout timing diagram of the pinned photodiode APS is shown in Figure 2.10. Prior to the integration, both the TX gate and the RST gate are turned on at the same time, and a high voltage (V_{pix}) is applied to the floating diffusion node and the pinned photodiode to fully deplete the photodiode. During the integration, the photo-generated electrons are stored in the n^+ region of the device thus lowering the potential there. During the pixel to column readout, the floating diffusion node is first reset to V_{pix}. The reset voltage may now be readout V_{RST} for true correlated double sampling. Next the transfer gate is turned on, and the complete photo-generated charges are transferred to the floating diffusion node, which ensures lag-free operation [26]. Then the voltage is sampled again for the true correlated double sampling, and therefore, lower noise [25]. The Pinned photodiode APS has the advantages of reduced dark current and reduced surface recombination [26], which increases sensitivity to the blue light.

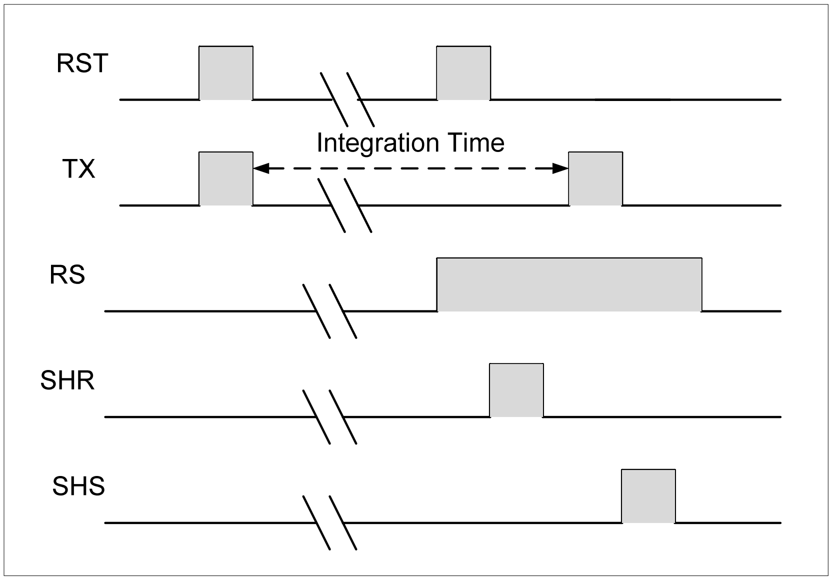


Figure 2.10: Readout timing diagram of a pinned photodiode active pixel sensor

Unlike the photodiode APS 3T structure, the pinned photodiode architecture has the floating diffusion node separated from the photodiode by the transfer gate, so the capacitance of the floating diffusion node can be optimized. The capacitance of the floating diffusion node needs to be large enough to hold all charges transferred from the photodiode; meanwhile the capacitance needs be minimized to increase the conversion gain in order to lower the readout noise floor.

An example of transfer characteristics of a conventional APS sensor is shown in Figure 2.11. The signal increases linearly before it reaches saturation. The dynamic range of the sensor is determined by the full well capacity and the readout noise floor. The full well capacity is limited by the voltage swing and the charge storage capacitor.

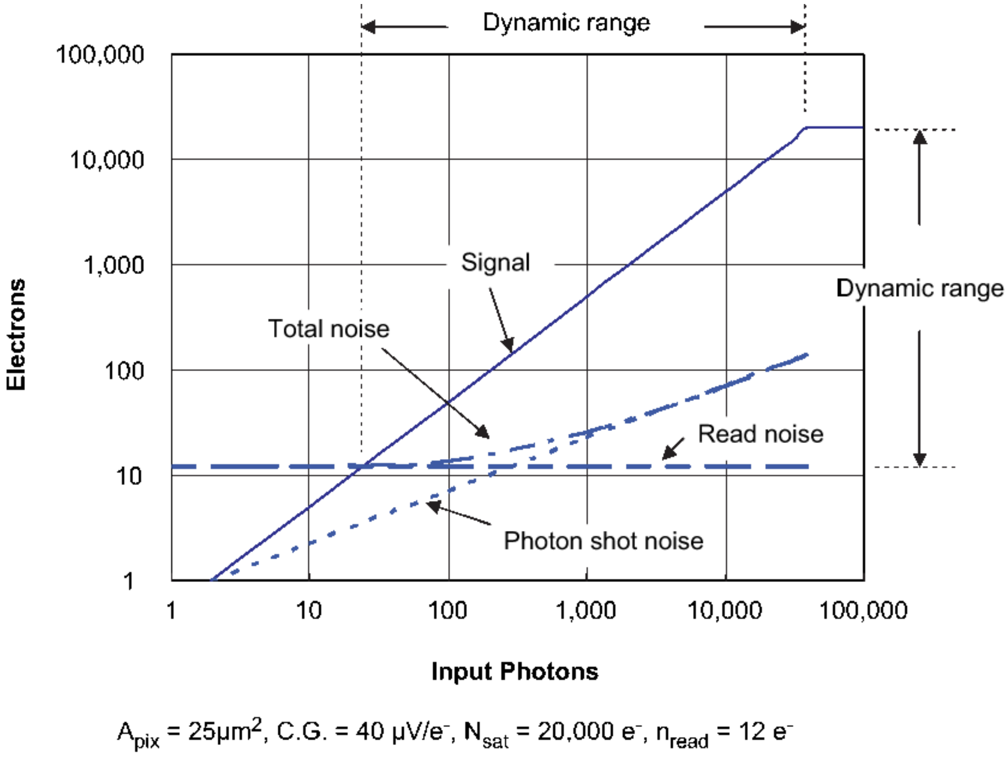


Figure 2.11: Photon transfer curve of a conventional APS [8]

2.4 Noise Analysis of CMOS Active Pixel Sensors

Based on whether the noise is stationary or not, the noise is divided into two categories: temporal noise (or random noise) and fixed pattern noise (FPN). Temporal noise refers to the time-dependent fluctuations in the signal level. Noise appearing in a reproduced image, which is “fixed” at certain spatial positions, is referred to as fixed pattern noise [8].

Temporal noise in the pixel includes photon shot noise, dark current shot noise, reset noise (kTC noise), thermal noise, and flicker noise ($1/f$ noise). Each noise component is originated from a specific mechanism. Therefore, these components can be considered independent of each other, and the variance of total random noise voltage can be written as:

$$\overline{v_{pixel}^2} = \overline{v_{shot-photon}^2} + \overline{v_{shot-dark}^2} + \overline{v_{reset}^2} + \overline{v_{thermal-SF,RS,bias}^2} + \overline{v_{1/f}^2} \tag{2.5}$$

The noise can be either written in numbers of electrons n_{noise} or voltages v_{noise} referenced to the floating diffusion node. The conversion between the two units is:

$$\overline{v_{noise}^2} = CG^2 \times \overline{n_{noise}^2} \tag{2.6}$$

where CG is the conversion gain of the floating diffusion node.

2.4.1 Shot Noise

Both the photocurrent and the dark current shot noise have the same mechanism. The shot noise is generated when a current flows across a potential barrier [8]. The power spectral density (PSD) of the shot noise is constant over all frequency and given by:

$$S_{shot-photon} = CG^2 \times N_{photo} = CG^2 \times \frac{I_{photo} \cdot t_{\mathrm{int}}}{q} \tag{2.7}$$

$$S_{shot-dark} = CG^2 \times N_{dark} = CG^2 \times \frac{I_{dark} \cdot t_{\mathrm{int}}}{q} \tag{2.8}$$

where I_{photo} represents the average photocurrent and I_{dark} is the average dark current. The term t_{int} is the integration time, normally several ms. As shown from the above equations, the photon shot noise has a square root relation with the photocurrent, and thus the illumination. Consequently, as the incident light intensity increasing, the photon shot noise will be the dominate noise source of the pixel. Conversely, under low light levels, the importance of the photon shot noise decreases.

2.4.2 Reset Noise

The signal integrated on a pixel is measured relative to its reset level. The thermal noise uncertainty associated with this reset level is referred to as the reset or kTC noise. This noise comes from the thermal noise of the MOS switch. The noise voltage is given by [8] [25]:

$$\overline{v_{n,KTC}^2} = \int_0^\infty 4kT \frac{R_{on}}{1+\left(2\pi R_{on}Cf\right)^2} df = \frac{kT}{C} \tag{2.9}$$

The noise charge is given by:

$$\overline{n_{n,KTC}^2} = C^2 \cdot \overline{v_{n,KTC}^2} = kTC \tag{2.10}$$

where k is the Boltzmann's constant, T is the temperature, R_{on} is the channel resistance of the reset transistor, and C is the charge sensing node capacitance (photodiode capacitance for the photodiode APS and floating diffusion node capacitance for the pinned photodiode APS). It can be concluded that the noise is a function only of the temperature and the capacitance value, also called "kTC noise".

The low frequency thermal noise can be removed by the correlated double sampling technique, while the high frequency component is removed by the filtering effects of the large column line capacitance, normally several *pF*. Since the photodiode APS readout is not true correlated double sampling, the reset noise is a significant problem. Let's assume the photodiode capacitance is 8fF for a typical photodiode APS, which corresponds to a conversion gain value of $20\mu V/e$. The kTC noise will be $720\mu V$ or 36 electrons, which limits the sensor dynamic range in the low end.

2.4.3 Thermal Noise

Thermal Noise (Johnson noise) is primarily the result of random motion of electrons due to thermal effects [27]. The noise signal can be represented by a series voltage source with a power spectral density:

$$S_{thermal} = 4kTR \tag{2.11}$$

The thermal noise has a white spectral density and a Gaussian amplitude distribution. However, its mean-square value does not depend on the current itself but depends on the absolute temperature and the resistance of the conductor.

In order to find the thermal noise of the CMOS imager, we first draw an equivalent thermal noise model as shown in Figure 2.12 . In this figure, i_{SF}, v_{RS}, and i_{bias} are the thermal noise sources associated with source follower, row-select, and column bias transistor, respectively. $g_{m,SF}$ and $g_{m,bias}$ are the transconductance of the source follower and the column bias transistor, $g_{d,RS}$ is the channel conductance of the row-select transistor, and C_{col} is the total column capacitance.

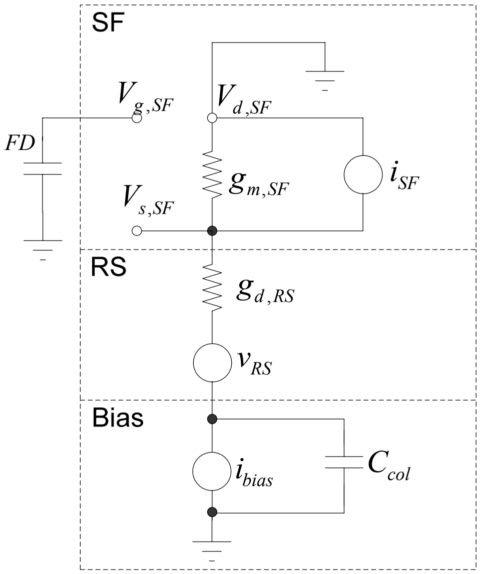


Figure 2.12: Small signal model for the noise analysis

Both the source follower and the column bias transistor are working in the saturation region, and the row select transistor is working in the linear region, so the thermal noise power spectral density of the source follower, the row select transistor, and the current bias transistor can be written as:

$$S_{thermal-SF} = 4kT\frac{2}{3}\frac{1}{g_{m,SF}} \tag{2.12}$$

$$S_{thermal-RS} = 4kT\frac{1}{g_{d,RS}} \tag{2.13}$$

$$S_{thermal-bias} = 4kT\frac{1}{g_{m,bias}} \tag{2.14}$$

Assuming steady state and neglecting the transistor body effect, the input referenced power spectral density of the thermal noise can be given by [25]:

$$S_{thermal-SF} = \frac{2}{3}\frac{kT}{C_{col}}\frac{1}{1+\frac{g_{m,SF}}{g_{d,RS}}}\frac{1}{Av} \tag{2.15}$$

$$S_{thermal-RS} = \frac{kT}{C_{col}}\frac{1}{g_{d,RS}\left(\frac{1}{g_{d,RS}}+\frac{1}{g_{m,SF}}\right)}\frac{1}{Av} \tag{2.16}$$

$$S_{thermal-bias} = \frac{kT}{C_{col}} g_{m,bias}\left(\frac{1}{g_{d,RS}}+\frac{1}{g_{m,SF}}\right)\frac{1}{Av} \tag{2.17}$$

where Av is voltage gain of the source follower. These equations show that the different noise sources are associated with the different noise bandwidth, and thus have different effects on the noise. The total thermal noise voltage is the mean square sum of the above three integrated from the available frequency bandwidth. However, comparing the three noises, it was found that the thermal noise from the row select transistor is very small and can be neglected [25].

2.4.4 Flicker Noise (1/f Noise) and Random Telegraph Signal (RTS) Noise

Flicker Noise or 1/f noise is due to traps or imperfections in the semiconductor, which capture and release carriers randomly. This noise source only occurs when DC current is flowing. The power spectral density of flicker noise is given by [8]:

$$S_{Flicker} = \frac{K_f}{C_{ox}^{'}WL}\cdot\frac{1}{f} = \frac{K_f^{'}}{f} \tag{2.18}$$

where K_f is a process-dependent constant, $C_{ox}^{'}$, W, and L denote the gate capacitance per unit area, gate width, and gate length, respectively. Unlike the thermal noise or shot noise, the frequency distribution of the flicker noise is not white, and the amplitude variation is generally a non-Gaussian distribution. At low frequency, the 1/f noise can be the dominant component, but at high frequency the 1/f noise drops below thermal noise.

To estimate the contribution from the source follower flicker noise, a transfer function of the correlated double sampling operation should be introduced since the flicker noise has a time-domain correlation. Assuming each sampling operation is expressed by the δ-function, the transfer function of the correlated double sampling can be expressed by [8]

$$H(j2\pi f) = 1 - e^{-j2\pi f\Delta t} \tag{2.19}$$

where Δt is the interval between the two samples of correlated double sampling.

The resulting output referred flicker noise component is estimated by

$$\overline{v_{Flicker}{}^{2}} = \int_{0}^{\infty} \left|H_{CDS}(j2\pi f)\right|^{2} \cdot \left|H_{SF}(j2\pi f)\right|^{2} \cdot \frac{K_f^{'}}{f} \cdot df \tag{2.20}$$

where $H_{SF}(j2\pi f)$ is the transfer function of the source follower. Assuming $H_{SF}(j2\pi f)$ is represented by a single-pole, low-pass filter characteristic with the low-frequency cut-off frequency of f_c, the above equation can be rewritten as:

$$\overline{v_{flicker}{}^{2}} = 2K_f^{'} \cdot \int_{0}^{\infty} \frac{A_V^2}{1 + \left(f/f_c\right)^2} \cdot \frac{\left(1 - \cos(2\pi f \cdot \Delta t)\right)}{f} \cdot df \tag{2.21}$$

Therefore, the flicker noise coefficient K_f' and the interval between two samples Δt should be examined carefully when designing the readout circuit.

Recent research proved that the 1/f noise induced by traps located at the Si/SiO_2

interface in the source follower gate region becomes dominant on the pixel read noise floor in CMOS imagers[28] [29]. As pixels and transistor sizes shrink the random telegraph signal (RTS) noise becomes an important factor limiting the performance of the sensor [30] [31]. It has been recognized that the 1/f noise is a result of RTS noise [29] [30].

RTS noise is defined as the random switching of a signal between discrete values. In sub-micron MOSFETs the RTS noise is observed as a switching of the drain current. It is widely agreed that the discrete switching is the result of a modulation of the channel resistance [32]. The modulation in channel resistance is caused by capture and emission of individual electrons at defect sites at the Si/SiO_2 interface and just inside the gate oxide [33]

The effect of the RTS noise on the pixel's output depends on if the correlated double sampling circuit samples the pixel's output when RTS fluctuations are occurring. If we assume a two-level RTS, the channel of the source follower transistor will have two states: a relatively low resistance and a high resistance. So as carriers are captured along the channel of the source follower and as the resistance of the channel changes, the pixel output voltage will fluctuate. If both SHR and SHS sample the signal when the source follower is in either low or high resistance state, the RTS will not be noticed by the readout circuits, and the pixel will output its average value. If SHR catches the high resistance state of the source follower, and SHS catches the low resistance state, the pixel's output signal will be lower than average. Otherwise, if SHR catches the low resistance state, and SHS catches the high resistance state, the pixel's output will be higher than average. The pixel will usually output a central value and randomly switch between a high and low value. In the final image it appears that the pixel is blinking from frame to frame. If a histogram of the pixel's output is plotted over a large number of frames (~1000 frames), it will display a characteristic tri-modal peak, shown in Figure 2.13. The distance between the outer peaks defines the amplitude of the RTS noise, and the height of the outer peaks defines a relative frequency at which the pixel blinks.

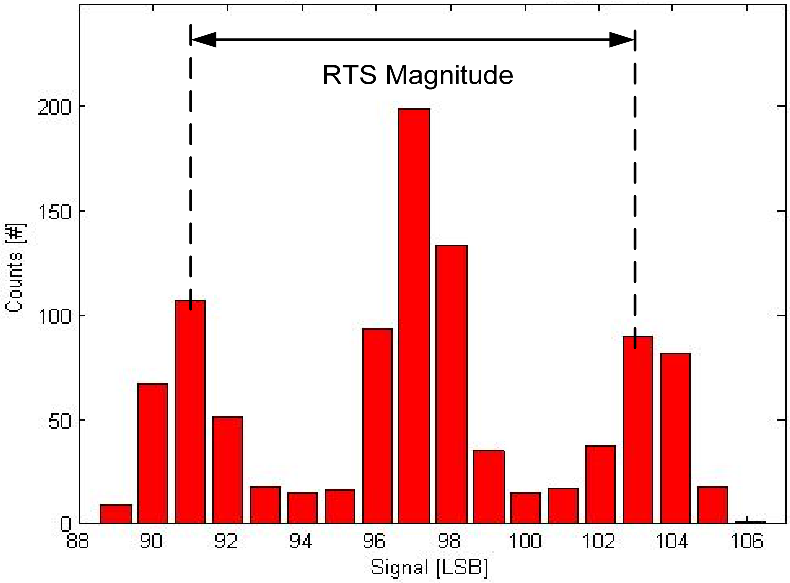


Figure 2.13: Histogram of the output of a pixel displaying the typical tri-modal peak which is characteristic to RTS pixels

It has been shown that the number of RTS pixels and the magnitude of RTS noise are proportional to $1/L^2$ of the source follower transistor [34]. Although it is desirable to shrink the pixel as much as technology allows, the source follower sizing must be carefully considered. Obviously, it is necessary to produce the highest quality interfaces and oxides possible to dramatically reduce the effect of RTS noise.

2.4.5 Noise Floor (Readout Noise)

The noise floor (or readout noise) refers to the residual noise of the image sensor if photon shot noise is excluded. The noise floor limits the image quality in the dark regions of an image and increases with exposure time due to the pixel dark current shot noise. The input referred read noise in electrons can be expressed by [35]:

$$n_{n,read}{}^{2} = n_{n,pix}{}^{2} + \frac{v_{n,sig\_chain}{}^{2}}{(A_V \cdot C.G.)^2} \tag{2.22}$$

where $n_{n,pix}$ and v_{n,sig_chain} are noise generated at a pixel and noise voltage generated in a signal chain, respectively. From the above equation, a higher conversion factor ($A_V \cdot CG$) provides lower input referred noise. The higher conversion factor effectively provides higher signal gain before the signal enters noise-producing readout circuits.

2.4.6 Fixed Pattern Noise (FPN)

Fixed pattern noise (FPN) refers to a non-temporal spatial noise and is due to device mismatches in the pixels and color filters, variations in column amplifiers, and mismatches between multiple programmable gain amplifier and analog to digital converters (ADCs) [35]. FPN can be either coherent or non-coherent.

Dark current FPN due to the mismatches in pixel photodiode leakage currents tends to dominate the non-coherent component of FPN, especially with long exposure times. The low leakage photodiodes are preferable to reduce this FPN component. Dark frame subtraction is an option, but this approach tends to increase the readout time.

The most problematic FPN in image sensors is associated with easily detectable (or coherent) row-wise and column-wise artifacts due to mismatches in multiple signal paths, and un-correlated, row-wise operations in the image sensor. Coherent FPN offset components can generally be eliminated by reference frame subtraction. Gain mismatches are more difficult to remove since this approach requires time or hardware intensive gain correction.

2.4.7 Noise Reduction

Correlated double sampling technique suppresses the low frequency component of the kTC noise, while large column capacitance filters out the high frequency noise component. The photodiode APS (3T) readout timing is not true correlated double sampling; the reset noise is a significant problem and limits the low light performance. The pinned photodiode enables the true correlated double sampling readout, and thus lower noise and better low light performance.

The photon shot noise limits the signal-to-noise-ratio (SNR) when detected signals are large. This noise represents a fundamental limit and can only be improved by increasing the full well capacity of the sensor. When the subject is not illuminated, the dark current is an undesirable current that is integrated as dark charges at a charge storage node inside a pixel. The dark charge reduces the imager's useable dynamic range because the full well capacity is limited. The dark current shot noise is directly related to the fabrication process, so it can be reduced by controlling the fabrication process and operating the sensor at low temperature. Also a careful pixel layout and a proper transistor size and bias setting are required to reduce the dark current even further.

Lowering the sensor operating temperature will reduce the thermal noise related to pixel readout circuitry. Both thermal noise and flicker noise can be reduced by limiting the bandwidth of the amplifier in the pixel. Increasing the size of the source follower transistor will also lower the 1/f noise. The amplifier in a CMOS image sensor pixel suffers from 1/f noise at low frequencies. However, 1/f noise is mostly suppressed by the correlated double sampling as long as the CDS operation is performed in such a way that the interval between the two samples is short enough that the 1/f noise is considered as an offset [8].

2.5 SNR Improvement Techniques Review

Both sensitivity and readout noise floor define the sensor low light performance. The signal-to-noise-ratio (SNR) is considered a measure for true “sensitivity” of the image sensor when the entire illumination range from dark to light is considered [8].

Under very low light conditions, the readout noise limits the sensor SNR, and the SNR increases 20*dB* per decade. Under normal light conditions, SNR is limited by the photon shot noise and increases 10*dB* per decade. The full well defines the maximum achievable SNR.

The Quantum Efficiency (QE) is one of the most important parameters to define the sensor performance. Several techniques have been reported to increase the sensor quantum efficiency. The Fill factor is defined as the light sensitive area over the whole pixel area ratio and is a very important parameter especially for sensors without microlens. The traditional CMOS APS has 3 or 4 transistors per pixel. Novel pixel architectures that reduce the effective number of transistors per pixel by sharing some of the transistors among a group of neighboring pixels have been recently proposed to increase the fill factor [36] [37] [38] [39] [40] [41].

The microlens focuses light onto the photodiode and effectively increases the fill factor. To increase the light-collection efficiency even further, the gap between each microlens has been reduced [42] [43]. Also, a double-layer microlens structure, which has an additional “inner” microlens beneath the conventional microlens, has been developed [44]. The inner microlens improves the angular response, especially when smaller lens F numbers are used, as well as smaller pixel sizes [45].

Incident light is reflected at the interface of two materials when the refractive indices are different. Thus, with the refractive indices of 1.45 for SiO_2 and 3~5 for Si, more than 20% to 30% of the incident light is reflected at the silicon surface in the visible light range ($400nm$–$700nm$). To reduce the reflection at the SiO_2/Si interface, antireflective films formed above the photodiode have been introduced. A 30% increase in photosensitivity was obtained with an antireflective film consisting of optimized $SiO_2/Si_3N_4/SiO_2$ layers [46].

In order to increase SNR at the low end, all efforts should be taken in order to reduce readout noise. A higher conversion factor ($A_V \cdot CG$) provides a lower input referred noise. This effectively provides higher signal gain before the signal enters the noise-producing readout circuits. However, this technique may conflict with the camera’s dynamic range requirement, especially in CMOS image sensors, as the higher conversion factor effectively reduces the full well capacity when a limited power supply voltage is available [8].

2.6 Dynamic Range Enhancement Schemes Review

Several techniques and architectures have been proposed for extending image sensor dynamic range. Below is a review of some representative schemes.

2.6.1 Nonlinear Sensor Response Approach

One of the well known techniques for enhancing dynamic range is the use of the nonlinear response of the pixel device or circuits. The use of logarithmic response [47] [48] [49] [50] and the combination of logarithmic and linear response [51] [52] [53] are reported. The logarithmic pixel is based on a 3T photodiode APS where the reset signal is connected to V_{pix} as shown in Figure 2.14.

The photodiode voltage self-adjusts to a level such that the load transistor current is equal to the photocurrent generated by the photodiode. The sensor achieves high dynamic range via logarithmic compression during the conversion to voltage via the exponential I-V characteristics of the MOS transistor in sub-threshold region.

There are several issues associated with this scheme. First of all, the transistor mismatches are significant due to the poorly defined sub-threshold MOSFET characteristics as well as varying threshold voltage. Second, succeeding circuitry must be extremely precise to make use of the dynamic range afforded by the compressed output voltage. Finally, these approaches have disadvantages in signal-to-noise-ratio and large fixed pattern noise [54].

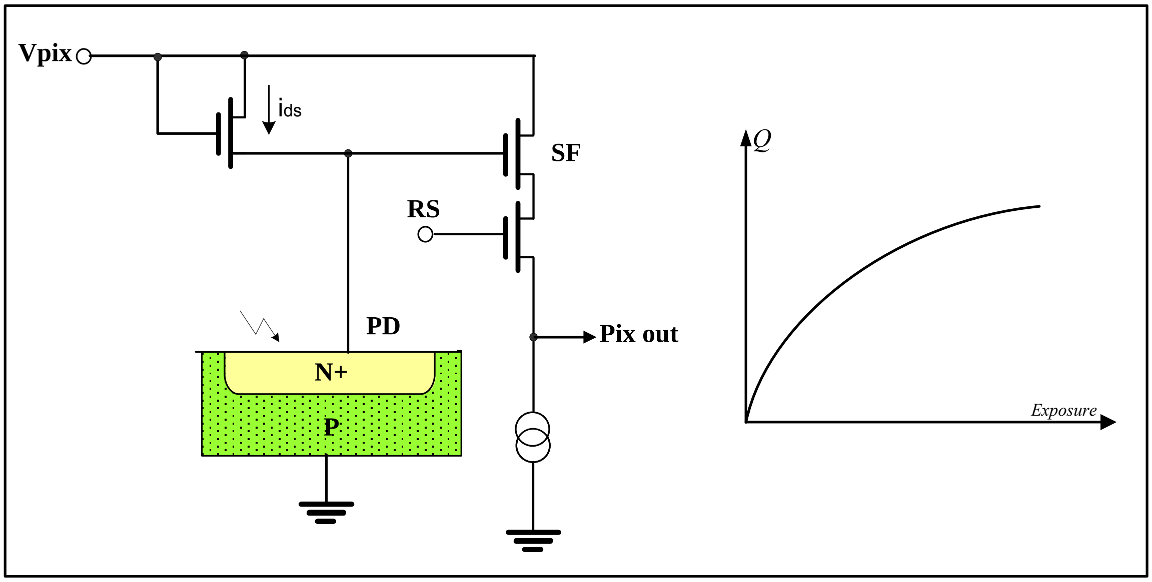


Figure 2.14: Logarithmic pixel scheme and transfer characteristic

2.6.2 Well Capacity Adjusting Approach

A well capacity adjusting scheme was proposed to enhance the sensor dynamic range [55]. In this scheme, the well capacity is increased one or more times during the integration. For APS, this is done by adjusting the reset signal one or more times during integration [56] [57].

Figure 2.15 shows one example of the transfer characteristics of the well capacity adjusting approach. During the integration, the RST gate voltage stays at highest potential; the RST gate voltage is monotonically decreased, which makes the charge capacity (well capacity) of the sensor monotonically increase. Whenever photo-generated charges exceed the charge capacity, the output signal will be clipped until the charge capacity is increased [58]. By controlling the RST gate voltage, any compressed transfer characteristic can be achieved.

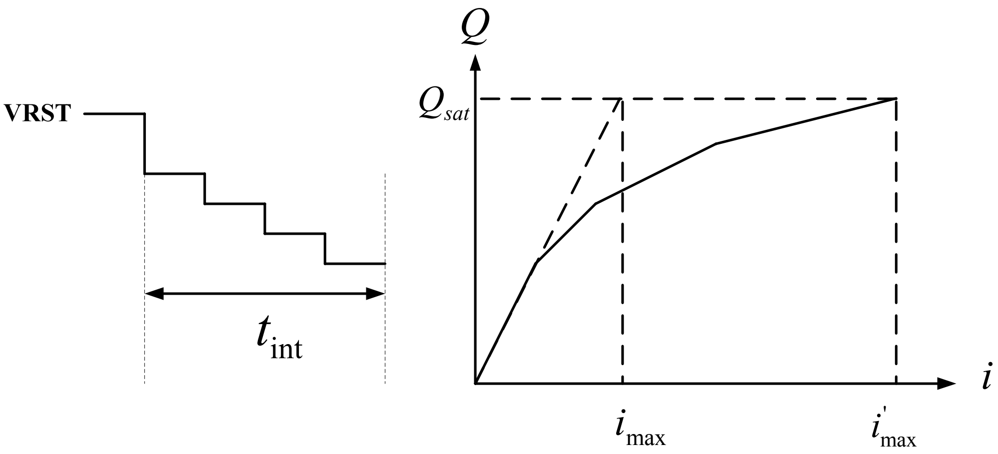


Figure 2.15: Well capacity adjusting APS transfer characteristic

The increase in dynamic range, however, comes at the expense of a decrease in SNR [59]. Also this technique requires complex timing and voltage control. It also suffers from nonlinear transfer curve, as logarithmic APS does [58]. Moreover, the smallest detectable signal does not change in this scheme, so the dynamic range is only enhanced at the high illumination end [7].

2.6.3 Multiple Capture Approach

The other technique uses two or more exposure time signals to expand the dynamic range [59] [60] [61] [62] [63] [64] [65] [66] [67]. The idea is to capture several images at different times within the normal exposure time – shorter exposure time images capture the bright areas of the scene while longer exposure time images capture the darker area of the scene as shown in Figure 2.16 . A high dynamic range image is then synthesized from the multiple captures by appropriately scaling each pixel's last sample before saturation.

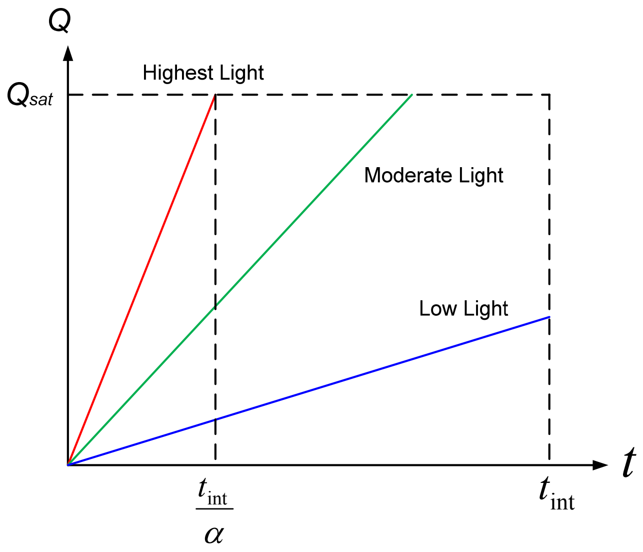


Figure 2.16: Multiple capture APS example

This scheme achieves higher SNR than the well capacity adjusting scheme [64]. However, this scheme does not take full advantage of the captured images. Since readout noise is not reduced, the dynamic range is only extended at the high illumination end. The multiple exposure technique also requires a large amount of space on the chip for the digital frame memory [60] [61] [62] [63].

2.7 State-of-the-Art CMOS Image Sensor Performance

Table 2.1 summaries the sensor performance from the major CMOS image sensor companies, such as the Micron, Omnivision, Sony, Cannon, Samsung, ST Microelectronics, Toshiba, Mashisuta, SilconFile, Kodak, Cypess, Magnachip, etc. The comparison table is based on the recent published papers from major conferences and journals. Table 2.2 summaries the pros and the cons for the different architectures.

The photodiode APS (3T) readout timing is not true correlated double sampling, the reset noise is a significant problem and limits the sensor dynamic range. A 60*dB* dynamic range was reported for the photodiode APS pixel [57] [68]. Pinned photodiode APS (4T) enables the true CDS readout, and thus lower noise and wider dynamic range. More than 70*dB* dynamic range was reported for the pinned photodiode APS with true CDS readout [69][70][71][72] [73].

The dynamic range expansion methods with nonlinear response of the pixel are based on photodiode APS (3T) structure and not compatible with the pinned photodiode structure. Even though more than 120*dB* dynamic range was achieved for the combination of the linear and logarithm pixel response [52] and more than 100*dB* dynamic range was achieved by full well capacity adjusting approach [57], the smallest detectable signal does not change in these schemes, so the dynamic range is only enhanced in the high illumination end. Moreover, the nonlinear response of the pixel is difficult for color processing. The color feature is quite important for many applications. A 96*dB* dynamic range was achieved for the double exposure approach [67], and the dynamic range can be extended to 140*dB* by combining 4 exposure images into one image [66]. The readout noise is not reduced for the multiple exposure approach; therefore the dynamic range is only extended at the high illumination end.

Table 2.1: Performance summary of state-of-the-art CMOS image sensors

Company	Year	Tech.	Pixel (μm^2)	Readout Noise (*e*)	Full Well (*ke*)	Max. SNR (*dB*)	Linear DR(*dB*)	Extended DR (*dB*)
Micron	2008[73]	0.13µm	2.2 x 2.2	2.1	9	39.5	72.6	no
	2005[71]	0.13µm	5.6 x 5.6	8	30	44.8	71.5	no
	2005 [57]	0.18µm	6.0 x 6.0	22	30	44.8	60	100
Sony	2007 [65]	0.18µm+ 90nm Cu	2.9 x 2.9	6.5	9	39.5	62.8	121
	2006[74]	0.18µm	2.5 x 2.5	7	12	40.8	64.7	no
	2006[76]	0.18µm	3.63x3.63	4.8	15	41.8	68	no
Canon	2007[72]	0.18µm	3.2 x 3.2	5.5	24	43.8	72.8	no
Samsung	2006[75]	0.13µm	2.25x2.25	8	14	41.4	64.8	70.8
STmicro	2006[52]	0.18µm	5.6 x 5.6	n/a	n/a	n/a	58	120
Cypress	2005[70]	0.15µm	6.4 x 6.4	25	80	49	70	no
	2006[68]	0.18µm	2.54x2.54	13	13	41.1	60	no
Mashisuta	2008[66]	0.25µm	8.0 x 8.0	n/a	n/a	n/a	n/a	140
	2005[77]	0.18µm	2.8 x 2.8	6	6	37.8	60	no
Magnachip	2007[78]	0.13µm	2.2 x 2.2	6	14.6	41.6	67.7	no
SiliconFile	2007[79]	0.13µm	2.25x2.25	4	4	36	60.2	no
Kodak	2008[80]	0.18µm	4.3 x 4.3	n/a	60	47.8	n/a	no
Toshiba	2006[67]	0.13µm	2.2 x 2.2	n/a	n/a	n/a	60	96

Table 2.2: Comparison of state-of-the-art CMOS image sensors

Company	**Year**	**Architecture**	**Pros.**	**Cons.**
Micron	2008[73]	2 way shared pixel with internal reset structure	2.5T/pixel, higher CG, lower readout noise	Slightly lower full well capacity
	2005[71]	Standard 4T	4T/pixel	
	2005 [57]	5T buried PD to support linear and high DR mode (well capacity adjusting)	True CDS readout for linear mode readout, lower readout noise	Not true CDS for high dynamic range mode, higher readout noise
Sony	2007 [65]	Midpoint driving Multi-Exposures	Wide DR, lower FPN	Potential motion blur
	2006[74]	Zigzag 4 way shared pixel	1.75T/pixel, higher QE, less G1/G2 mismatch	Slightly lower CG, need column shuffling
	2006[76]	Standard 4T	4T/pixel	
Canon	2007[72]	Standard 4T	4T/pixel	
Samsung	2006[75]	Vertical 4-way shared	1.5T/pixel, FD summing	Slightly lower CG
STmicro-electronics	2006 [52]	Combined linear-log Response	Wide DR, good for monochrome sensors	Based on 3T, no CDS, higher noise
Cypress	2005[70]	Standard 4T	4T/pixel, higher full well	Lower CG, higher noise
	2006[68]	3T pixel	3T/pixel	No CDS, high kTC noise
Mashisuta	2008[66]	In pixel multi-exposure	No frame memory needed, wide DR	Extra 3 T and 2 caps. in pixel, complicated timing
	2005[77]	FD driving Pinned PD	3T/pixel with CDS readout	
Magnachip	2007[78]	2 way shared with stratifield PD	Higher full well capacity, slightly higher DR	Charge transfer might be an issue
SiliconFile	2007[79]	Standard 4T	Borderless contact to increase QE	
Kodak	2008[80]	2 way shared with hole based detector	Lower dark current and lower crosstalk	Special fabrication process
Toshiba	2006[67]	Double Exposure	Wide DR, lower FPN	2 line memory required

CHAPTER 3 MOSFET MODULATED DUAL CONVERSION GAIN PIXEL

3.1 Introduction

Previously proposed high dynamic range enhancement schemes mainly focused on extending the sensor dynamic range at the high illumination end; sensor dynamic range extension at the low illumination has not been addressed. Since most applications require low-noise, high-sensitivity characteristics for imaging of the dark region as well as dynamic range expansion for the bright region, the availability of a low-noise, high-sensitivity pixel device with a pinned photodiode structure is particularly important [16] [17] [18] [19].

One typical way to increase the sensor dynamic range is to increase the full well capacity of the pixel. Since the output swing of the image sensor is usually fixed and relatively small due to power supply scaling, obtaining a high dynamic range generally requires a small conversion gain so that the full well capacity is increased. On the other hand, the small conversion gain results in the increase of readout noise in electrons. Thus, an image sensor designed with a small conversion gain provides a large signal handling capacity but poor noise, while that with a larger conversion gain provides better low light imaging capability but with a reduced dynamic range.

A good way of improving dynamic range without increasing artifacts or increasing the imaging readout noise floor is to change the conversion gain based on the illumination levels. At high illumination levels, a low conversion gain is used to achieve higher full well capacity and wider dynamic range. At low light levels, a high conversion gain is enabled to lower the readout noise and achieve excellent low light performance.

3.2 Pixel Architecture

A new conversion gain pixel architecture is proposed here to extend the sensor dynamic range at both the low end and the high end as shown in Figure 3.1.

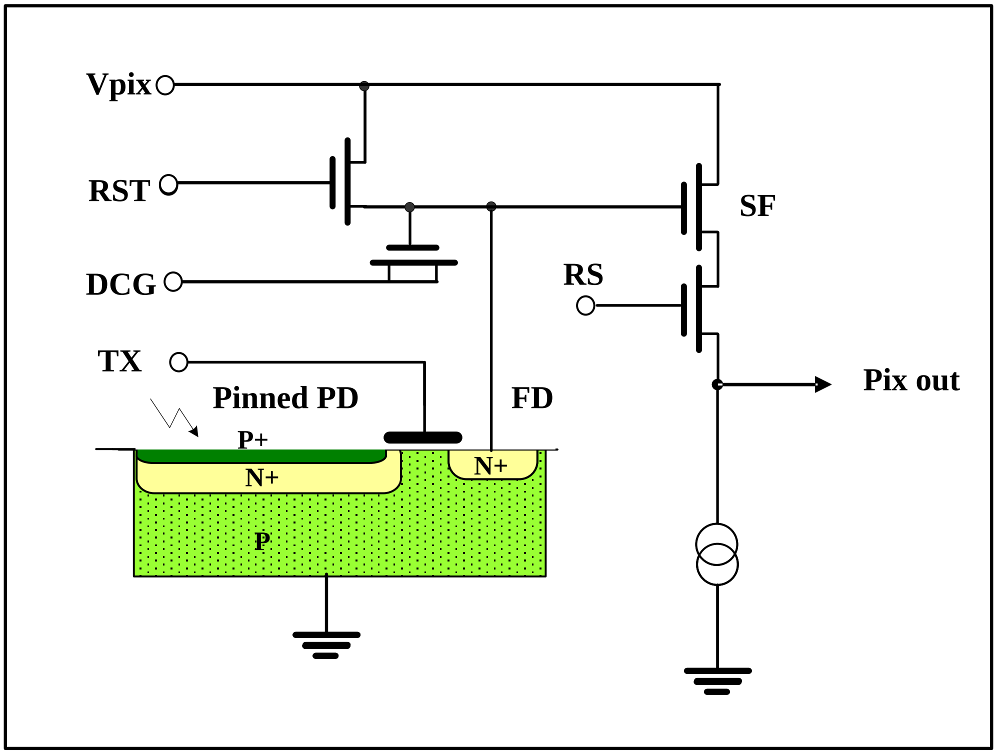


Figure 3.1: Schematic diagram of MOSFET modulated dual conversion gain pixel

The pixel cell includes a pinned photodiode, a floating diffusion node (FD), a transfer transistor (TX), a reset transistor (RST), a source follower transistor (SF), and a row select transistor (RS). In addition, the pixel cell also includes a dual conversion gain transistor (DG), which has its gate connected to the floating diffusion node and has both source and drain terminals driven by a control signal, called DCG control signal.

Similar to the 4T pinned photodiode pixel architecture, during the floating diffusion node reset period, the floating diffusion node will be reset to V_{pix} if the RST gate voltage is boosted one threshold above V_{pix}. Both the source follower and the column bias transistor are working in the saturation region, and the row select transistor is working in the linear region such that the pixel output voltage can follow the potential changes of the floating diffusion node linearly. The pixel output voltage normally is higher than $500mV$ in order to let bias transistor working in the saturation mode. The floating diffusion node potential is at least one threshold voltage higher than the minimum column line voltage. Thus for V_{pix} at $2.8V$, the normal floating diffusion node voltage range is normally between $1.2V$ and $2.8V$. Since the gate of the dual conversion transistor is connected to the floating diffusion node, the gate to source voltage of the dual conversion gain transistor is greater than the threshold voltage if the DCG signal is at low potential. The transistor is working in the strong inversion mode; electrons pile at the interface between the gate oxide and the substrate where they create an inversion layer. The inversion layer and the gate form a very good capacitor as shown in Figure 3.2.

The MOSFET inversion capacitor is given by [27]:

$$C_{inv} = C_{ox} = C_{ox}^{'} \cdot W \cdot L \tag{3.1}$$

where $C_{ox}^{'}$, W, and L denote the gate capacitance per unit area, gate width, and gate length, respectively. This dual conversion gain gate inversion capacitor adds to the floating diffusion node inherent charge storage capacitor, which increases the charge storage capacity of the floating diffusion node.

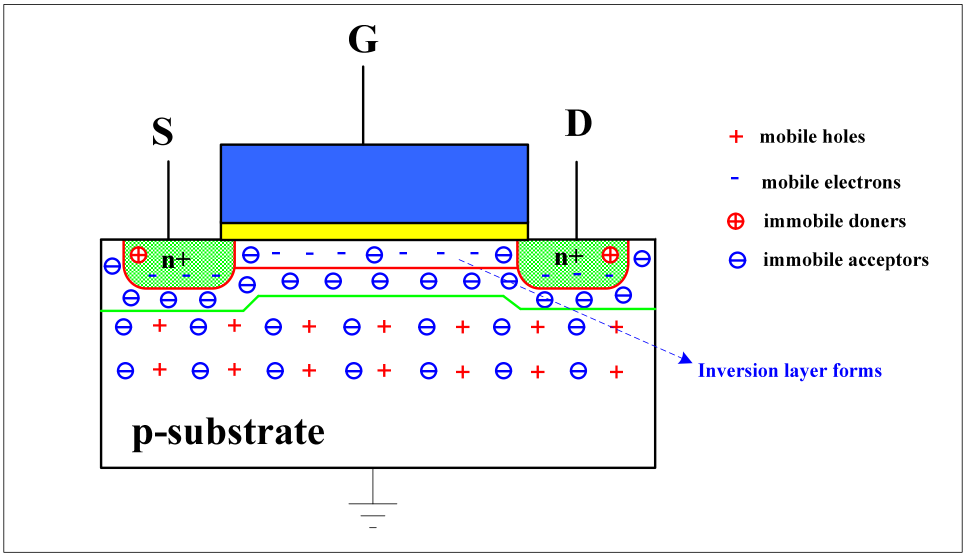


Figure 3.2: NMOS device in strong inversion mode

When the DCG control signal is generated and applied to the source and drain of the dual conversion gain transistor, the transistor is working in the depletion mode as shown in Figure 3.3 , where the channel is depleted. The capacitance between the gate and the source/drain terminal is simply the overlap capacitance, while the capacitance between the gate and the substrate is the oxide capacitance in series with the depletion capacitance [20], which is given by:

$$C_{dep} = \frac{1}{\frac{1}{C_{ox}} + \frac{x_d}{\varepsilon_s}} \tag{3.2}$$

where x_d is the depletion depth, which is calculated from:

$$x_d = \sqrt{\frac{2\varepsilon_s \phi_s}{qN_d}} \tag{3.3}$$

where ϕ_s is the surface potential and N_d is the donor concentration.

The overlap capacitance from the gate to the source (or drain) depends on the lateral diffusion and is given by [27]:

$$C_{gs} = C_{gd} = C'_{ox} \cdot L_{diff} \cdot W \tag{3.4}$$

where L_{diff} is the diffusion length.

The depletion capacitance and the overlap capacitance, which are much smaller compared to the inversion capacitance, will also add to the floating diffusion node. The small floating diffusion node capacitor corresponds to a high conversion gain which is beneficial for low light conditions.

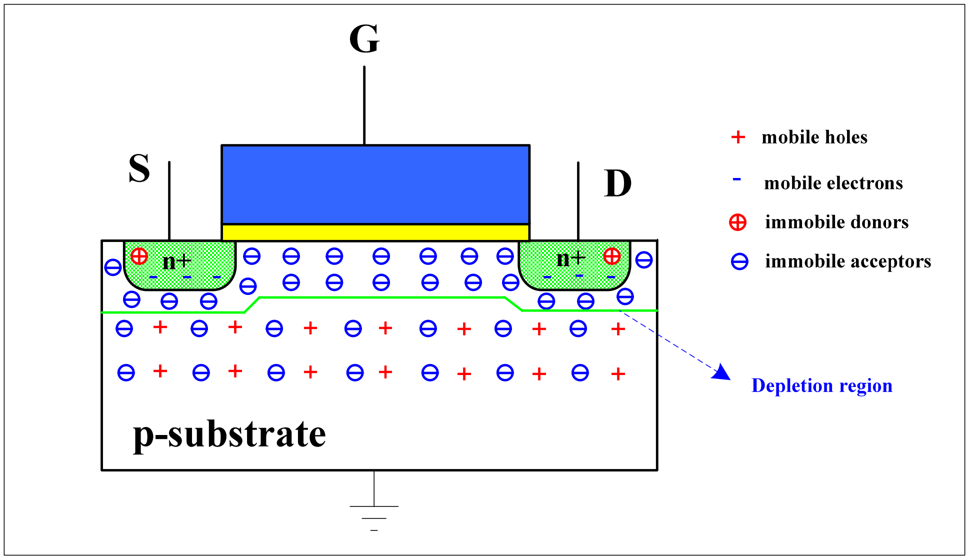


Figure 3.3: NMOS device in depletion mode

3.3 Pixel Operation Principles

3.3.1 Readout Timing and Potential Diagram

The readout timing for the proposed dual conversion gain pixel is similar to that of the regular pinned photodiode with additional control of the DCG signal. Under low light illumination conditions, the high conversion gain mode will be enabled by turning on the DCG signal during the photodiode reset period and the pixel to column readout period as shown in Figure 3.4. For the rest of the time, the DCG control signal stays at a low potential to reserve power consumption. The high potential applied to the drain and source terminals will push the transistor working in the depletion region, which corresponds to a lower capacitance of the floating diffusion node and a higher conversion gain.

Before the photodiode integration, both the photodiode and the floating diffusion node are reset. To accomplish this, high potentials are applied to the RST gate, transfer gate, and the dual conversion gain transistor source and drain terminals, as shown Figure 3.4. This results in the V_{pix} voltage being applied to the floating diffusion node and the photodiode. The V_{pix} applied to the photodiode will fully deplete the photodiode.

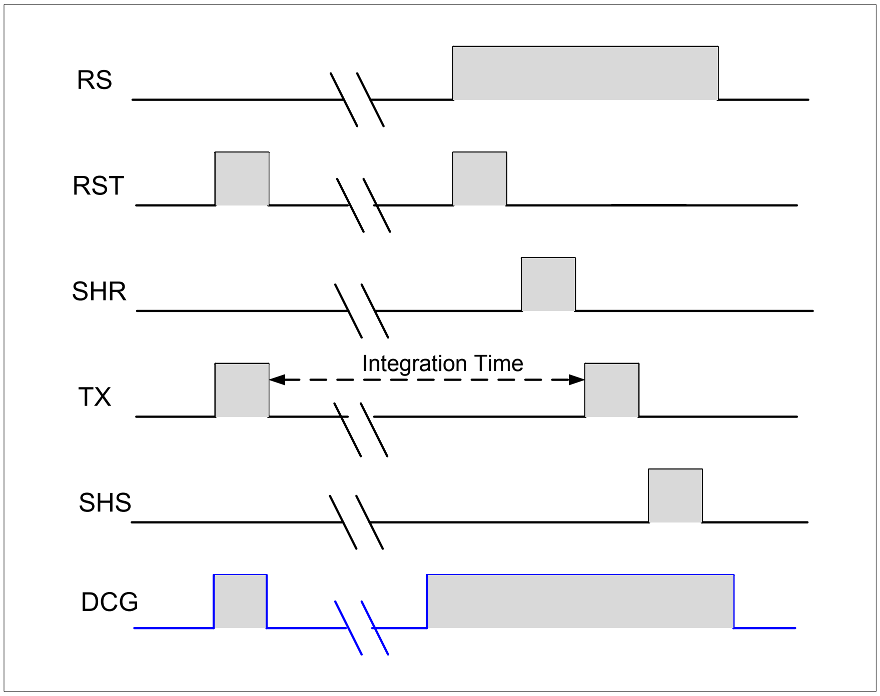


Figure 3.4: Readout timing diagram for the high conversion gain mode

Figure 3.5 shows the potential diagram of the dual conversion gain pixel working in the high conversion gain mode. When the photodiode is fully depleted, the photodiode returns to its respective pinned potential as shown in Figure 3.5A. After reset, the charges start to integrate at the photodiode. Figure 3.5B illustrates the potential diagram of the stored charges caused by a low light exposure. For a low light exposure, the photodiode charge capacity well is only slightly filled with the photo generated electrons.

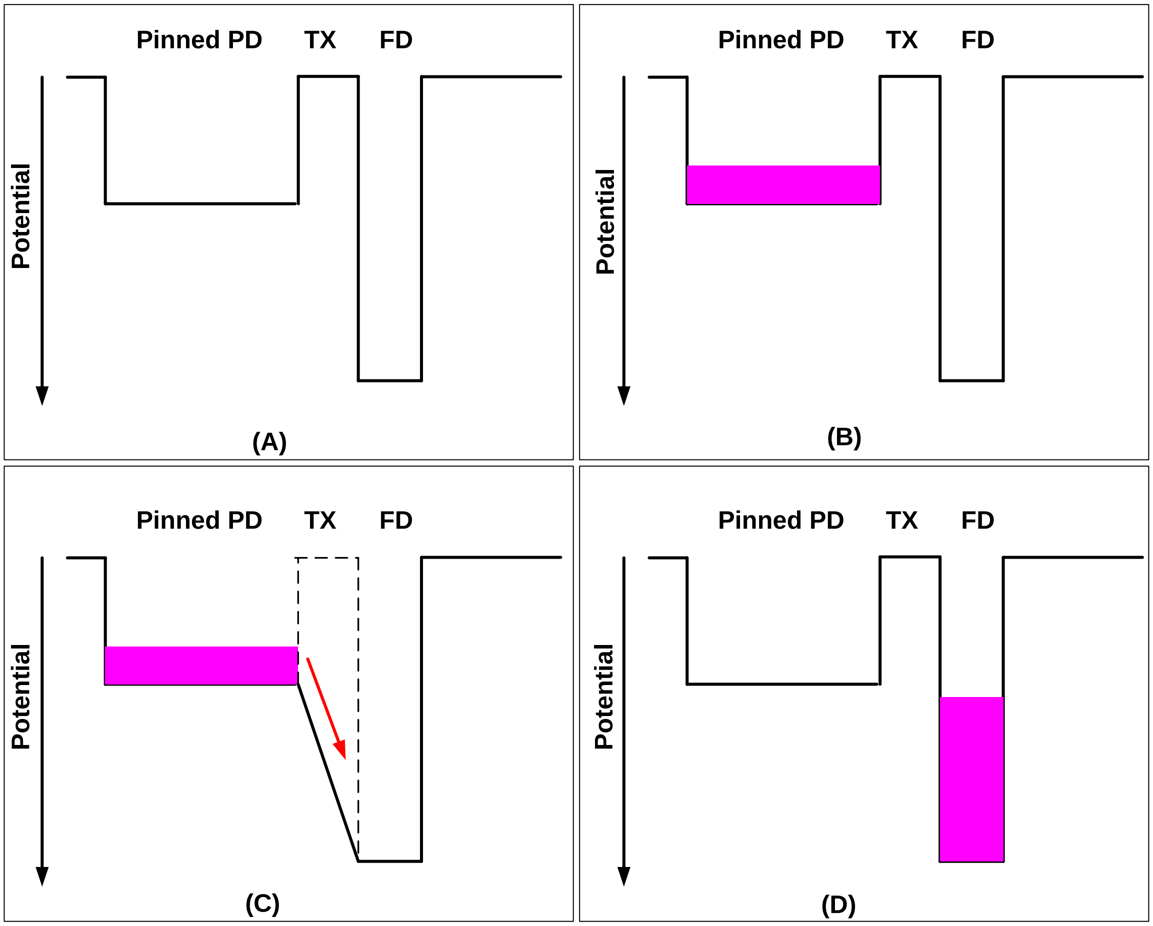


Figure 3.5: Potential diagram for the high conversion gain mode. (A): before charge integration, (B): after charge integration, (C): during charge transfer, (D): after charge transfer

During the pixel to column readout period, the respective row is selected by applying a signal RS to the row select line, thereby turning on the row select transistor. Meanwhile, a high DCG signal is applied to the dual conversion gain transistor drain and source terminals to lower the capacitance of the floating diffusion node and increase the conversion gain. Next, the reset signal RST is applied to the reset transistor, applying V_{pix} to the floating diffusion region, thereby resetting the respective floating diffusion region. Then a sample and hold signal SHR is generated such that sample and hold circuitry connected to a column line of the imager would input, sample, and hold the signal output of the source follower.

Thereafter, a transfer gate control signal TX turns on the transfer transistor, which lets the charges stored in the photodiode transfer into the floating diffusion node as shown in Figure 3.5C. Figure 3.5D illustrates the potential diagram after the charge transfer phase. Another sample and hold signal SHS is generated such that the sample and hold circuitry connected to the column line of the imager would input, sample, and hold the column line of the signal associated with the transferred charge. Correlated the double sampling may then be used to subtract the SHS from the SHR to determine the pixel signal output value change as a result of the light exposure.

During the whole pixel to column sampling period, the floating diffusion node has a low capacitance and a high conversion gain because the dual conversion gain transistor remains in the depletion mode. The low capacitance and high conversion gain of the floating diffusion node result in higher sensitivity and lower readout noise, which are beneficial for the low light performance. During the shutter reset period, the DCG signal stays high to match the transistor operation mode during the pixel to column sampling.

Under the bright or intense light exposures conditions, the dual conversion gain inversion capacitance is switched into the floating diffusion node by turning off the DCG control signal to lower the conversion gain and increase the charge storage capacity of the floating diffusion node. The readout timing diagram for the lower conversion mode is shown in Figure 3.6.

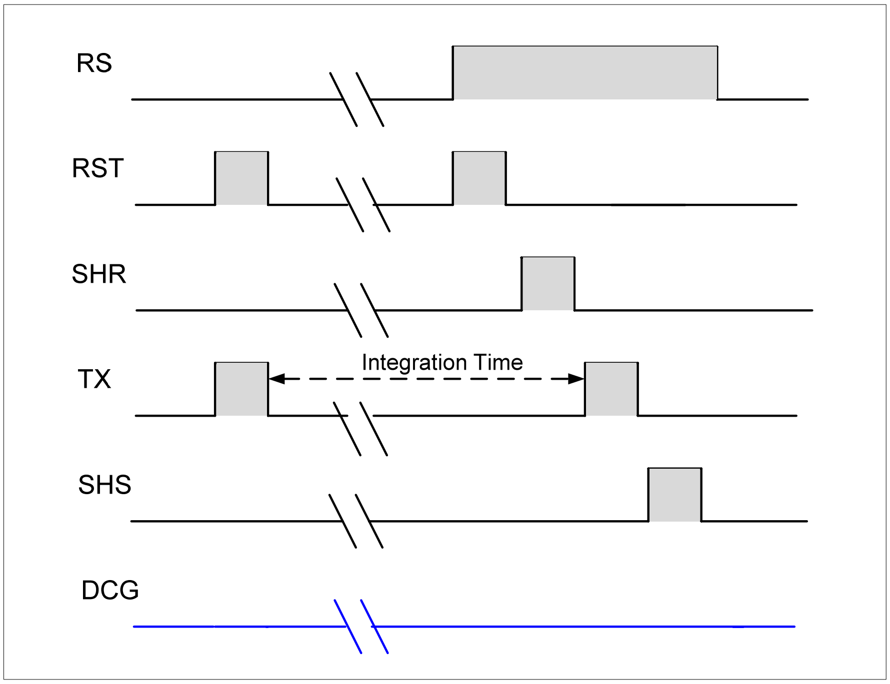


Figure 3.6: Readout timing diagram for the low conversion gain mode

Compared to the higher conversion gain mode operation as shown in Figure 3.4, the only difference is that the DCG signal applied to the source and drain terminals remains at the low potential all the time. The low DCG control signal applied to the source and drain terminals of the transistor will push the dual conversion gain transistor work in the strong inversion mode; thus the inversion capacitance adds to the floating diffusion node to increase the total floating diffusion node charge storage capacity. The potential diagram under the bright light or intense light conditions is shown in Figure 3.7.

Before the integration, both the photodiode and the floating diffusion node are reset by turning on TX transistor and RST transistor at the same time with the DCG signal staying at a low potential. Thereby, the V_{pix} voltage is applied to the floating diffusion node and photodiode to fully deplete the photodiode as shown in Figure 3.7A.

After reset, the charges start to integrate at photodiode. For a high light exposure, the photodiode charge capacity well is filled with a lot of photo generated electrons as shown in Figure 3.7B.

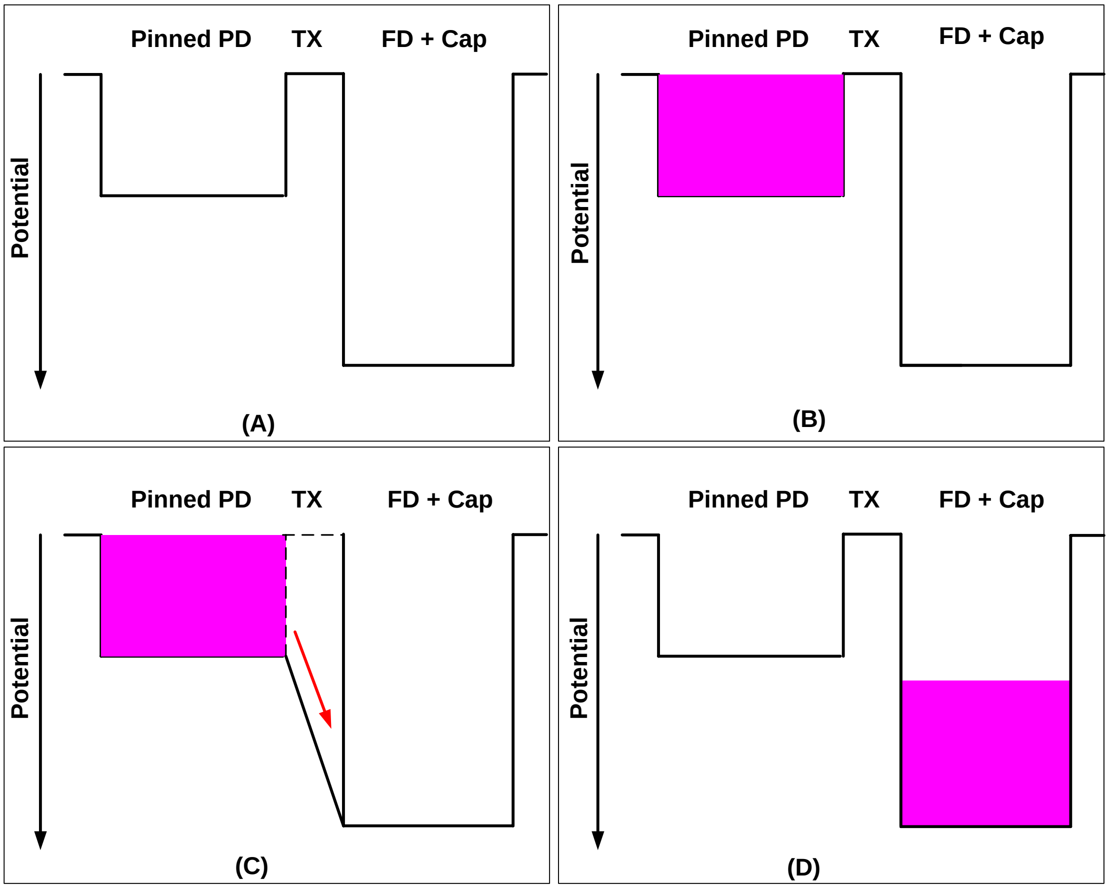


Figure 3.7: Potential diagram for the low conversion gain mode. (A): before charge integration, (B): after charge integration, (C): during charge transfer, (D): after charge transfer

The pixel to column readout starts with floating diffusion node reset by turning on the RST transistor followed by the SHR. Next, the transfer gate is turned on to transfer the charge from the photodiode to the floating diffusion node as shown in Figure 3.7C. The dual conversion gain transistor inversion capacitor is switched into the floating diffusion node in order to increase the charge handling capacity as shown in Figure 3.7D.

After the charge transfer, a SHS signal is enable to sample the signal voltage on the column for correlated double sampling.

By controlling the DCG signal applied to the dual conversion gain transistor source and drain terminals, the operation mode of the transistor is changed, which in turn changes the floating diffusion node total capacitance and the conversion gain. The conversion gain mode is switched depends on the light illumination condition. At normal or high intensity exposure, low conversion gain mode is enabled to increase the charge storage capacity, increase the sensor SNR, and extend the sensor dynamic range at the high end. Under low light conditions, the high conversion mode will be used to increase pixel sensitivity, lower the readout noise, and extend sensor dynamic range in the low end, which are all beneficial for the low light imaging performance.

3.3.2 Noise Analysis

The proposed MOSFET modulated dual conversion gain pixel is based on the Pinned photodiode architecture. During the pixel to column sampling, the DCG control signal stays either at high potential for the high conversion gain mode or low for the low conversion gain mode. There is no switching operation between SHR and SHS; hence the noise related to the DCG transistor will be suppressed by the correlated double sampling. The noise analysis for the 4T pinned photodiode is still valid, and no extra noise is expected for the proposed dual conversion gain pixel architecture. The high conversion gain reduces the pixel noise floor in unit of electrons.

3.3.3 SPICE Simulation Results

SPICE simulation was performed to verify the function of the pixel operation. Figure 3.8 shows the simulation result of the MOSFET capacitance changing with the DCG control signal at different floating diffusion node potentials. There are two steady states for the MOSFET capacitance: the high capacitance state with the DCG control signal at a low potential and low capacitance state with the DCG control signal at a high potential. Based on the simulation results, for 2.8V of V_{pix} operation, 2.8V and 0V of the DCG voltages work pretty well for a wide floating diffusion node operation range.

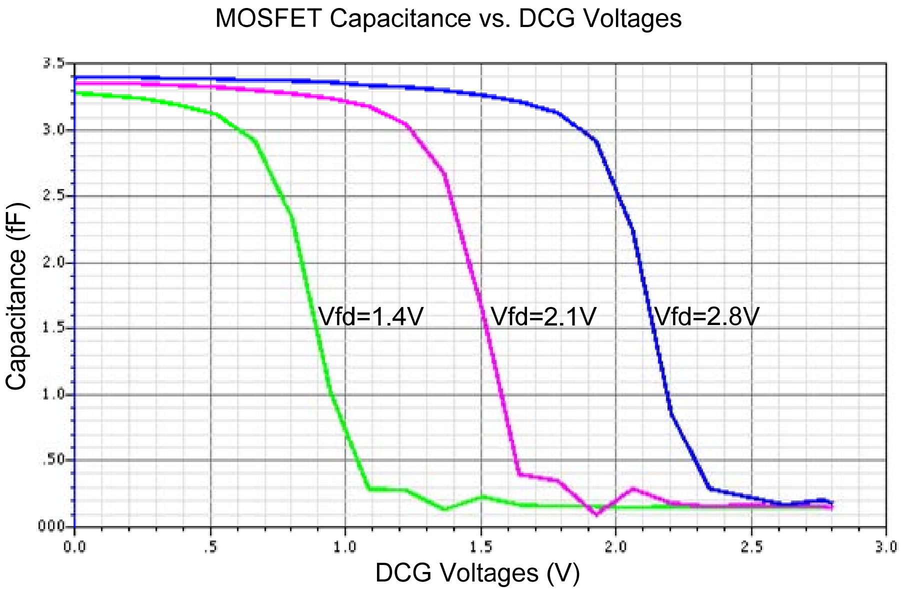


Figure 3.8: SPICE simulation of the MOSFET capacitance versus the DCG voltages at different floating diffusion node potentials

Figure 3.9 shows simulation result of the total capacitance of the floating diffusion node, which includes the parasitic capacitance (such as junction capacitance, coupling capacitance, and source follower gate capacitance) and the extra capacitance added by the dual conversion gain transistor gate. With the DCG control signal stays at a low potential, the total floating diffusion node capacitance is about 4fF. The capacitance of the floating diffusion node changes to $1.14fF$ when the DCG control signal stays at the same potential as V_{pix}. Different floating capacitances are achieved by varying the DCG control signal applied to the source and drain terminals of the dual conversion gain transistor, which corresponds to 3.5 times difference of the conversion gain. Also from Figure 3.9, it can be seen that the capacitance of the floating diffusion node is very stable across a wide floating diffusion node operating range for both the low conversion gain mode and high conversion gain mode, which is very important to achieve a linear response of the pixel.

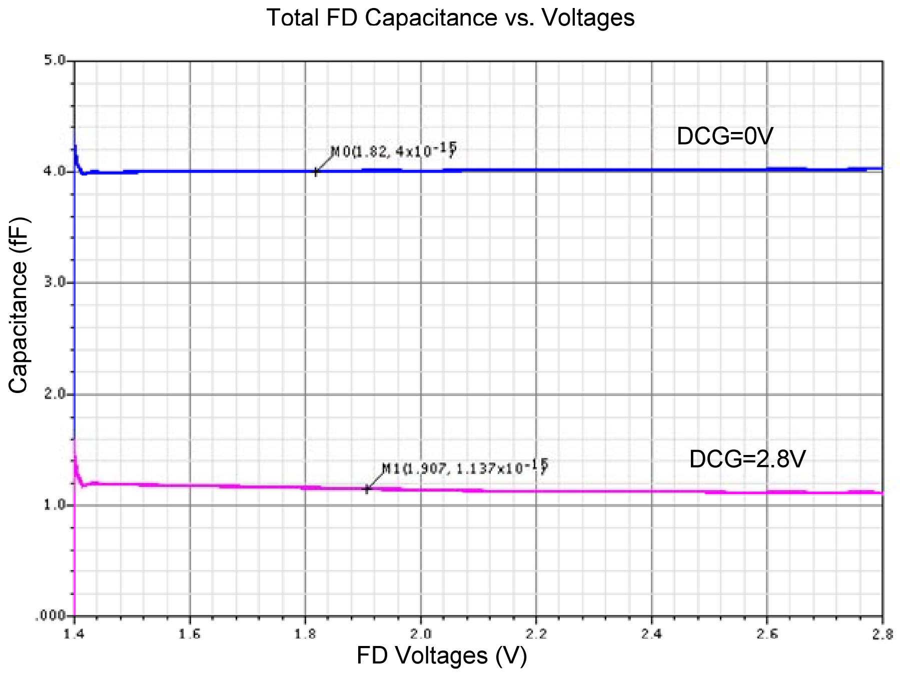


Figure 3.9: SPICE simulation of the total capacitance of the floating diffusion node versus floating diffusion node potentials with DCG control signal at 0V and 2.8V

Figure 3.10 shows the simulation result of the floating diffusion node potential diagram for both the low and high conversion gain modes. From $0.5\mu s$ to $1\mu s$, the RST signal is turned on at least one threshold voltage above V_{pix} to hard reset the floating diffusion node to V_{pix} (2.8V for this simulation). When the RST gate is on, the channel is inverted and an abundance of electrons are injected into the channel. When the RST gate is turned off, some charges under the RST gate will go to the V_{pix} node, and others will go to the floating diffusion node. The charges injected into the floating diffusion node will lower the potential of the floating diffusion node. The charge injection can be reduced by properly sizing the RST transistor size and by using a slightly positive RST low voltage instead of 0V [81]. After the RST gate goes to low, the column voltage can be sampled and stored in memory for CDS. Then the transfer gate is turned on to transfer charges from the photodiode to the floating diffusion node, which lowers the floating diffusion node potential even more.

The floating diffusion node voltage changes are inversely proportional to its capacitance. In this example as shown in Figure 3.10, $10ke$ are transferred from the photodiode to the floating diffusion node, which results in about $250mV$ voltage drop for the low conversion gain mode and $890mV$ for the high conversion gain mode, which corresponds to the conversion gain difference.

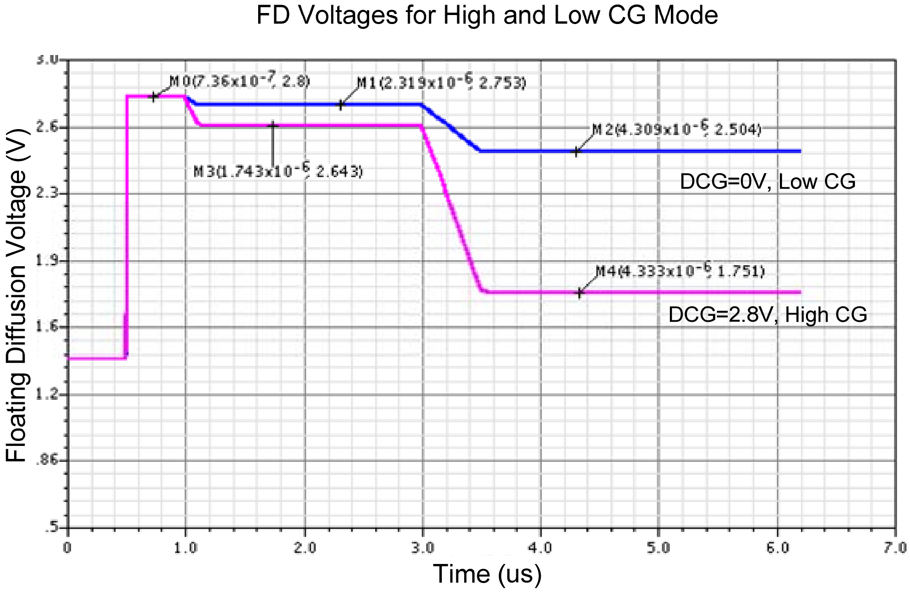


Figure 3.10: SPICE Simulation results of the floating diffusion node potential diagrams for both high and low conversion gain modes

3.3.4 Pixel Transfer Characteristics

Figure 3.11 shows the transfer characteristics for both the low and high conversion gain modes in a linear scale. The x-axis is the exposure in units of $Lux \cdot s$. The responsivity for the high conversion gain mode in units of $V/(Lux \cdot s)$, which is the slope of the signal, is much higher than that of the low conversion gain mode.

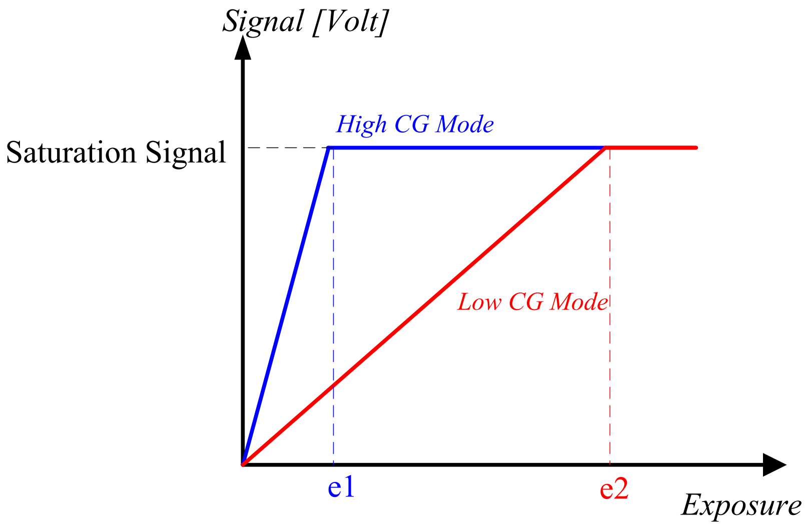


Figure 3.11: Dual conversion gain pixel transfer characteristics in a linear scale

Figure 3.12 shows the pixel transfer characteristic in a log-log scale, with the signal in units of electrons. From Figure 3.12, it can be seen that the noise floor for the high conversion gain is much lower compared to that of the high conversion gain mode, which is beneficial for the low light performance, and the dynamic range extends under the low light conditions. A higher full well is achieved with the low conversion gain mode, so the dynamic range extends in the high light range, and the maximum SNR increases. Thus, the sensor dynamic range extends both in the low light and high light conditions by combining of the two-mode operations.

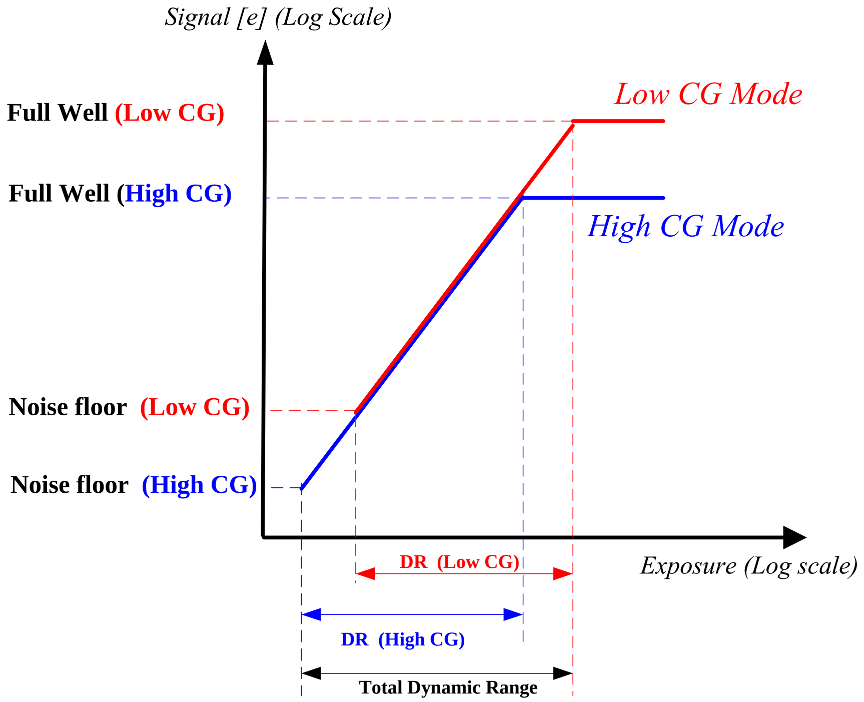


Figure 3.12: Dual conversion gain pixel transfer characteristics in a Log-Log scale

3.4 Pixel Layout Design

Figure 3.13 shows an example of pixel layout with Micron Technology's 130*nm* 3-metal 2-poly process, and the schematic of the pixel is shown in Figure 3.14. The pixel size is 5.6μm x 5.6μm with a Pinned photodiode inside the pixel. The TX line, the RST line, the RS line, and the DCG line route horizontally using metal-2 with a 0.2μm line width. The pixel output line runs vertically using metal-1with a 0.13μm line width. The V_{pix} power line is routed using metal-3 line in both horizontal direction and vertical direction to reduce the voltage droop across the whole array.

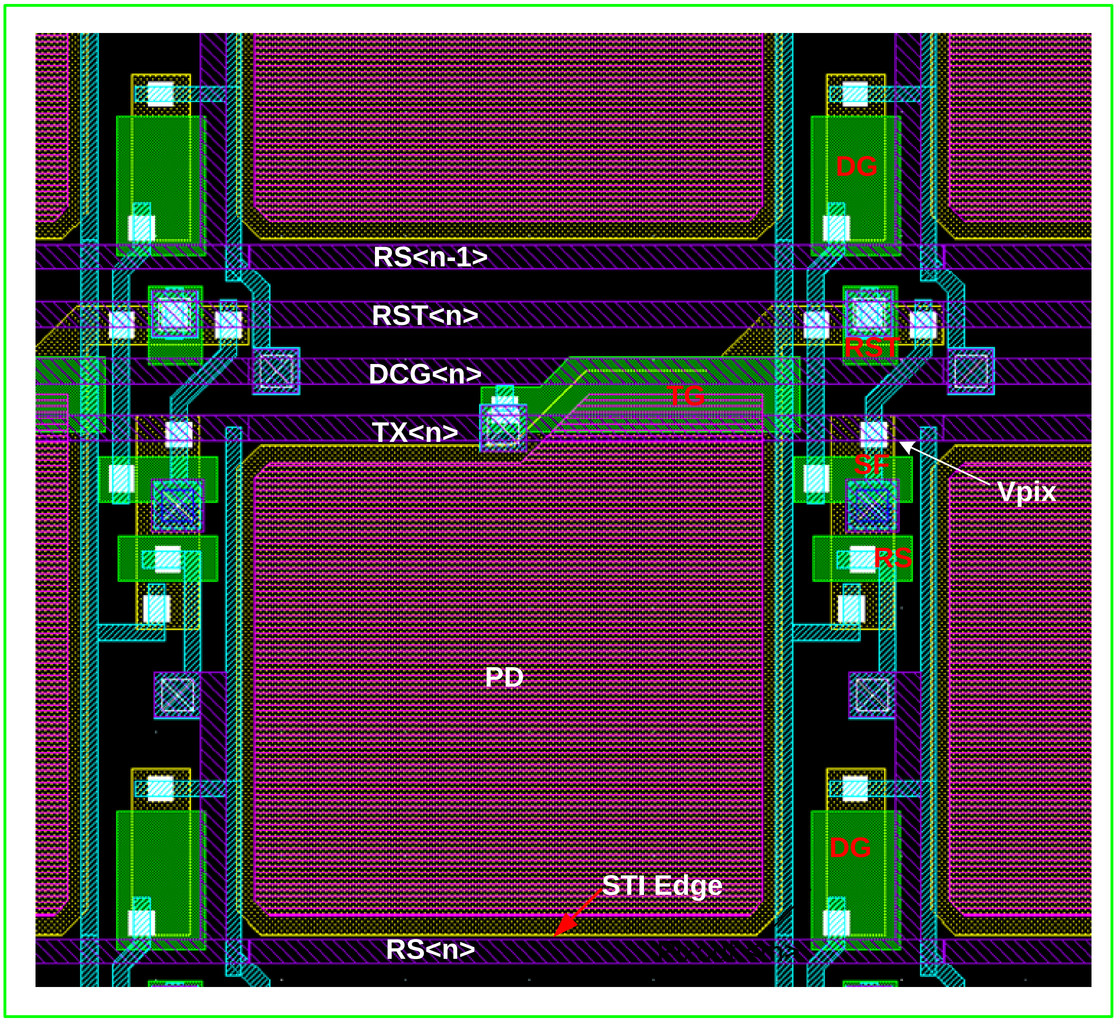


Figure 3.13: Layout of 5.6µm MOSFET modulated dual conversion gain pixel

Both the source follower and row select transistors have 0.5μm channel widths and 0.32μm channel lengths. The bigger W/L ratio of the source follower increases the amplifier transconductance, and thus the drive capability and lets the column line settle faster.

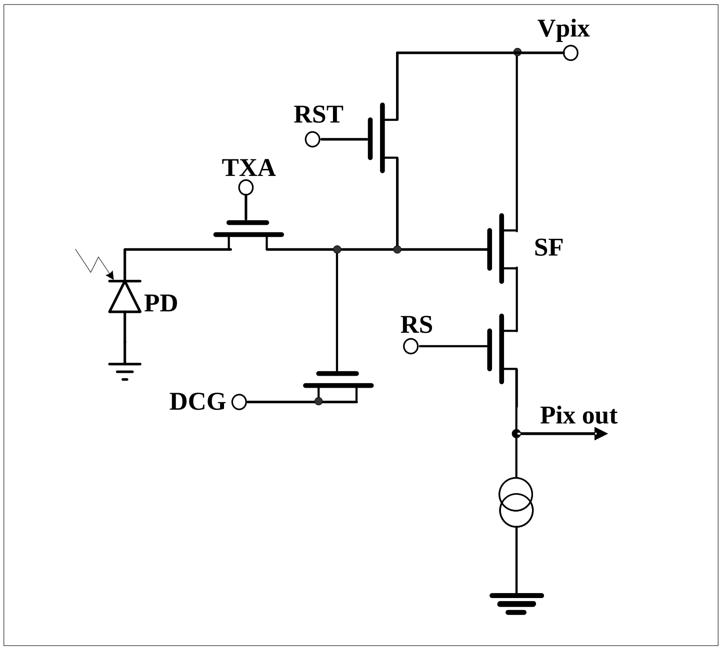


Figure 3.14: Schematics of the dual conversion gain pixel

The reset transistor is slightly smaller and has a 0.32μm channel width and a 0.43μm channel length. The smaller RST gate will lower the charges under the channel when the RST gate is on, which in turn reduces the RST gate channel charge injection when the RST is turned off. The reduction of the charge injection increases the voltage swing, which is especially important for the high conversion gain mode.

In order to reduce the area consumption of the dual conversion gain transistor and reduce the overlap capacitance, the drain and source of the transistor are merged together with a 1μm channel length and a 0.4μm channel width. The reduction of the overlap capacitance will increase the conversion gain when the transistor is working in the depletion mode.

The transfer gate is an asymmetric device, which couples between the photodiode and the floating diffusion node. The transfer gate has a 1.7μm channel width and a 0.6μm channel length. The wider transfer gate width helps the charge transfer from the photodiode to the floating diffusion region.

There are a lot of design considerations to improve the pixel performance, which will be discussed in detail in the next several sections.

3.5 Quantum Efficiency (QE) Improvement

Quantum efficiency is the most important parameter to define the sensor performance. In order to increase the quantum efficiency, a gapless microlens process was implemented, which focuses more light onto the photodiode and effectively increases the fill factor. Also the curvature of the microlens was optimized to focus the light onto the pixel photodiode.

To reduce the reflection at the SiO_2/Si interface, an antireflective film above the photodiode was implemented. Si_3N_4 has a refractive index of 2.0, which is between Si and SiO_2 and is a good choice of antireflective film [46]. A 50*nm*-60*nm* Si_3N_4 above the photodiode was implemented to reduce the reflection and increase the quantum efficiency.

Compared to the standard pinned photodiode pixel, the dual conversion gain transistor is added for each pixel, so the fill factor was lowered slightly. However, the microlens focuses light onto the photodiode and effectively increases the fill factor. For the pixel with a 5.6μm pitch, the extra dual conversion gain transistor has less than 5% impact to the quantum efficiency.

This dual conversion gain approach can be implemented in combination with other shared-transistor architectures to reduce equivalent transistors per pixel. Figure 3.15 shows the schematic of a 2-way shared MOSFET modulated dual conversion gain pixel, in which six transistors are shared between 2 photodiodes from 2 different rows, achieving an effective 3 transistors per pixel. Two pixels from two different rows share the same floating diffusion node, reset gate, source follower, row select transistor, and dual conversion gain transistor. The gate of the dual conversion gain transistor is connected to the shared floating diffusion region and the source and drain is controlled by the DCG control signal. The pixel on each row still has its own transfer gate. The readout timing diagram is similar to the non-shared architecture except that there is separate control of the TXA and the TXB for even and odd row readouts.

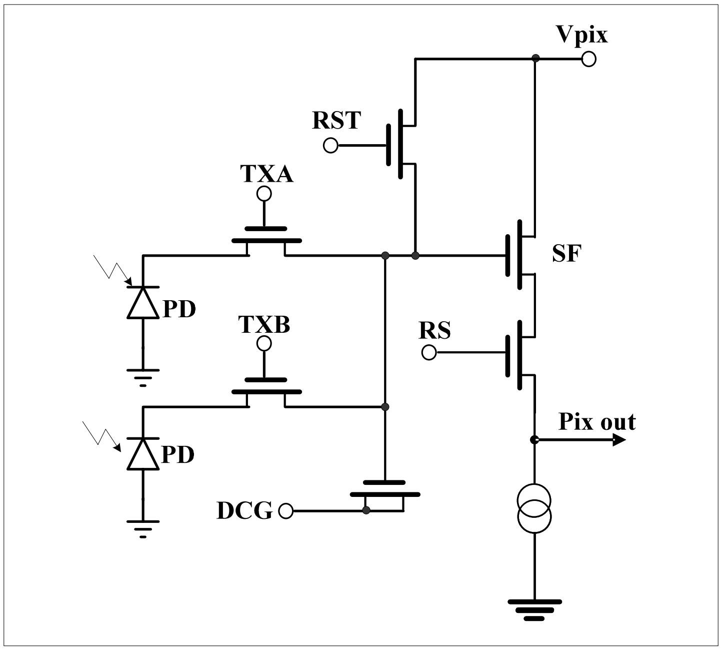


Figure 3.15: Schematic of a 2-way shared dual conversion gain pixel

3.6 Dark Current and Hot Pixels Reduction

The dark current is the leakage current at the photodiode node. This current discharges the pixel capacitance even though there is no light over the pixel [82]. The dark current is detrimental to the imaging performance under low illumination as it introduces shot noise that cannot be corrected due to its large variation over the sensor array [1].

3.6.1 Dark Current Components

The first dark current component is ''ideal'' dark current, depending on doping concentrations, band gap, and temperature of the reversed biased diode. In an ideal p-n junction diode, there are two dominant current sources, i.e., injection-diffusion and generation-recombination current. The injection-diffusion current is due to the injection of thermal electrons and holes, whose energies are higher than the built-in potential energy, to the other side of the junction. This injection results in minority carrier diffusion current. The generation-recombination current is due to electron-hole generation or recombination within the p-n junction depletion in the bulk or at the surface [82].

3.6.2 Temperature Dependence of Dark Current

The generation-recombination current is proportional to n_i, the intrinsic carrier density, while the diffusion current is proportional to n_i^2. Because

$$n_i^{\,2} \propto T^3 \cdot \exp\left(-\frac{E_g}{kT}\right) \tag{3.5}$$

the temperature dependence of dark current is expressed as [8]:

$$I_d = A_{d,gen} \cdot T^{3/2} \cdot \exp\left(-\frac{E_g}{2kT}\right) + B_{d,diff} \cdot T^3 \cdot \exp\left(-\frac{E_g}{kT}\right) \tag{3.6}$$

where $A_{d,gen}$ and $B_{d,diff}$ are the generation-recombination coefficient and diffusion coefficient, respectively. At room temperature or below, the generation current is dominant, because the temperature dependence is proportional to $\exp(-E_g/2kT)$. The diffusion current is a dominant component at high temperatures due to the temperature dependence of $\exp(-E_g/kT)$. In real devices, the temperature dependence is expressed as $\exp(-E_g/nkT)$, where n is between 1 and 2 and E_g/n corresponds to the activation energy of the dark current [8].

3.6.3 Hot Pixels (White Spot Defects)

As design and process technologies have progressed, dark currents have decreased to very low levels. Therefore, pixels that have extremely high dark currents with an extra generation center become visible as a hot pixel (or white spot defect). These white spot defects determine the quality of the image sensor at low light. The causes of the white spot defects include contamination by heavy metals, such as gold, nickel, cobalt, etc., and crystal defects induced by stress during fabrication [83]. A careful pixel layout and a proper transistor length and bias setting are required to suppress this dark current component [8].

3.6.4 Dark Current and Hot Pixels Reduction

The pinned photodiode structure reduces the dark current by introducing an extra P^+ layer at the photodiode surface. The holes accumulated in the surface suppress the current generated thermally through the surface states distributed near the mid-band in the forbidden gap.

From the pixel layout shown in Figure 3.13, a shallow trench isolation (STI) is used to isolate pixels and their components from each other. The STI boundaries may have higher defect densities than the substrate, creating a higher density of “trap sites”, which may result from defects along the SiO_2/Si interface between the STI boundaries and the silicon. In order to reduce the dark current and hot pixel generated current near the SiO_2/Si interface, the photodiode is pulled away from the interface to make sure that the depletion region will not touch the STI edge in the pixel as shown in Figure 3.13.

Inside the pixel, the V_{pix} supply voltage is used to reset the pixel floating diffusion node and the photodiode. The high supply voltage applied to the V_{pix} node will depleted the active area connected to the supply voltage node and also deplete the photodiode to its pinned potential. When this occurs, an electric field may be generated between the supply voltage node and the photodiode, which may pull the photodiode depletion region close to the STI edge. Then dark current and hot pixels may increase at the photodiode and STI interface. In order to further reduce the dark current generated along photodiode and STI interface, a pulsed supply voltage approach was proposed [84]. This technique is achieved by pulsing the V_{pix} voltage to a lower potential (close to the pinned potential of the photodiode) when the photodiode is not in the reset phase or readout phase. The low potential can reduce or eliminate the electric field between the supply voltage node and the photodiode, which pushes the photodiode depletion region far away from the STI edge and reduces the dark current and hot pixels along the STI edges.

For the pinned photodiode structure, the carriers generated under the transfer gate also contribute a significant amount of dark current, which can be reduced by applying a relative small voltage on the gate of the transfer transistor during the charge acquisition period. If a small positive voltage is applied, the depletion region is created under the transfer gate. This region creates a path for the dark current electrons to be transferred to the pixel floating diffusion region. The dark electrons are subsequently removed by a floating diffusion node reset operation. If a small negative voltage is applied to the transfer gate, electrons that would normally create dark current problems will instead recombine with holes, thereby, substantially reducing dark current [85]. For each pixel, the potential applied to the transfer gate during integration needs to be optimized to reduce dark current and hot pixels and achieve excellent low light performance.

3.7 Full Well Capacity and Conversion Gain

The photodiode operates in the charge integrating mode, therefore, has a limited charge handling capacity. The full well capacity limits the sensor dynamic range and maximum achievable SNR.

For the high conversion gain mode, the capacitance of the floating diffusion node needs to be reduced to achieve higher conversion, lower readout noise, and excellent low light performance. The floating diffusion node voltage swing will limit the pixel full well capacity for the high conversion gain mode. Since most of the capacitance of the floating diffusion node is parasitic capacitance. A careful pixel layout and a proper transistor size are required to reduce floating diffusion node parasitic capacitance and increase the conversion gain.

For the low conversion gain mode, an extra MOSFET inversion capacitance is added to the floating diffusion node to increase the charge storage capacity. In this mode, the photodiode capacity will normally limit the pixel full well capacity. However, in order to increase the full well capacity, the photodiode n^+ implant dose needs to be increased. This increase results in higher dark current and hot pixels, which will hurt the low light performance. Meanwhile, if the conversion gain is too low, the pixel responsivity will be reduced and the pixel noise floor will be increased. Therefore, both photodiode n^+ implant dose and the capacitance of the floating diffusion node need to be optimized to increase the full well capacity with good pixel responsivity.

3.8 Charge Transfer

Incomplete charge transfer from the photodiode to the floating diffusion node causes excess noise, image lag, and a nonlinear response [8]. Therefore, the pinned photodiode and the transfer gate in CMOS image sensors should be optimized to let charge easily transfer from the photodiode to the floating diffusion node.

Taking the floating voltage drop at the charge transfer into account, the acceptable pinned potential of the pinned photodiode is 1.0V~1.5V. Therefore, very accurate n^+ implant control is required in fabrication [8]. High transfer efficiency with a low-voltage transfer pulse requires optimizing the structure of the region between the photodiode edge and the transfer gate [86] as well as optimizing photodiode depth. The photodiode n^+ implant is created by tailoring the angle toward the transfer gate to provide good charge transfer characteristics when the transfer gate is on and to lower the leakage when the transfer gate is off [87].

A higher voltage setting for the initial floating diffusion node voltage helps improve efficiency of the charge transfer from the photodiode to the floating diffusion node and the pixel output swing. Increasing the pulse height of the RST pulse through on-chip power boosting is one suitable solution [88]. Also increasing the pulse height and width of TX pulse can effectively improve the charge transfer efficiency from photodiode to floating diffusion node.

3.9 Reset Gate Charge Injection

During the pixel to column readout period, the reset gate is turned on to reset the floating diffusion region for the correlated double sampling readout. As the reset transistor is not an ideal switch, when it turns off, some portion of the channel charges will be relocated to the floating diffusion region, and will reduce the available voltage swing on the floating diffusion region. This reduced voltage swing will increase the pixel charge transfer lag, and reduce the pixel output swing on the column [81]. This problem is expected to get worse for the high conversion gain mode.

A slightly smaller RST gate is preferred to reduce the amount of charges in the channel which in turn reduces the RST gate channel charge injection when the RST turns off. A positive V_{RST_LO} potential was proposed to further reduce the charge injection [81].The reduction of the charge injection increase the voltage swing which is especially important for the high conversion gain mode because the floating diffusion node swing limits the full well capacity.

3.10 Summary

MOSFET modulated dual conversion gain pixel architecture was proposed. The pixel operation was fully simulated with SPICE. The pixel layout, readout timing, and operation voltage levels were optimized to increase the pixel quantum efficiency, SNR, full well capacity, and dynamic range. The dark current and hot pixels performance, FPN, readout noise, and RTS noise were further improved optimizing the pixel layout and operation.

CHAPTER 4 PROTOTYPE SENSOR DESIGN

4.1 System Architecture

To demonstrate the MOSFET modulated dual conversion gain pixel, a prototype sensor was designed using Micron Technology’s 130*nm* 3 metal 2-poly process. The block diagram of the circuitry is shown in Figure 4.1.The followings are descriptions for each part of the building blocks.

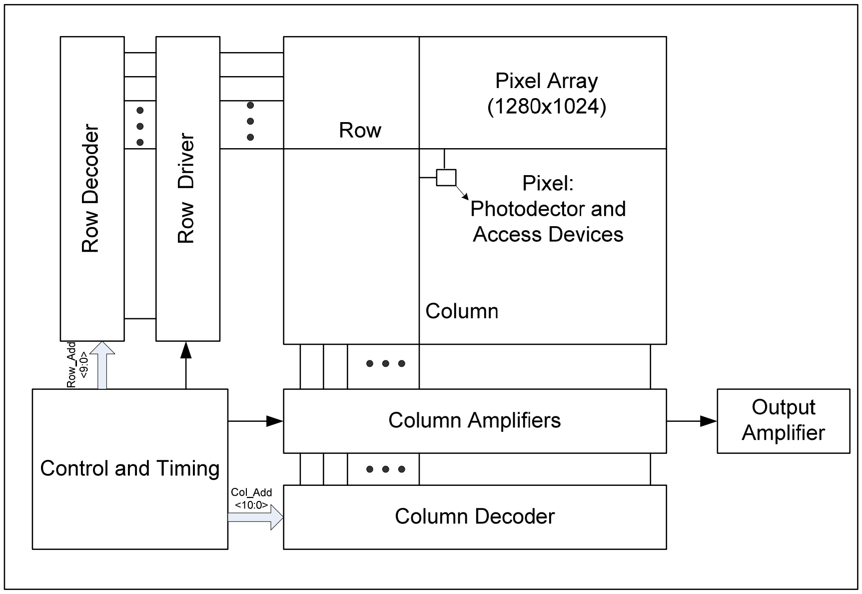


Figure 4.1: Block diagram of the prototype CMOS image sensor

4.2 Pixel Array

A standard SXGA (Super Extended Graphic Array) format [8] was implemented on the prototype sensor, which has 1280 columns and 1024 rows of pixels. The pixel pitch is 5.6*μm* and contains 5 transistors for each pixel. The pixel array is surrounded by an n^+ guard ring and a p^+ guard ring as shown in Figure 4.2. The n^+ guard ring is biased at a high potential, while the p^+ guard ring is grounded. The substrate noise resulting from the periphery circuits can inject current into the pixel array. The p^+ serves as a substrate contact and removes the injected carriers [27].

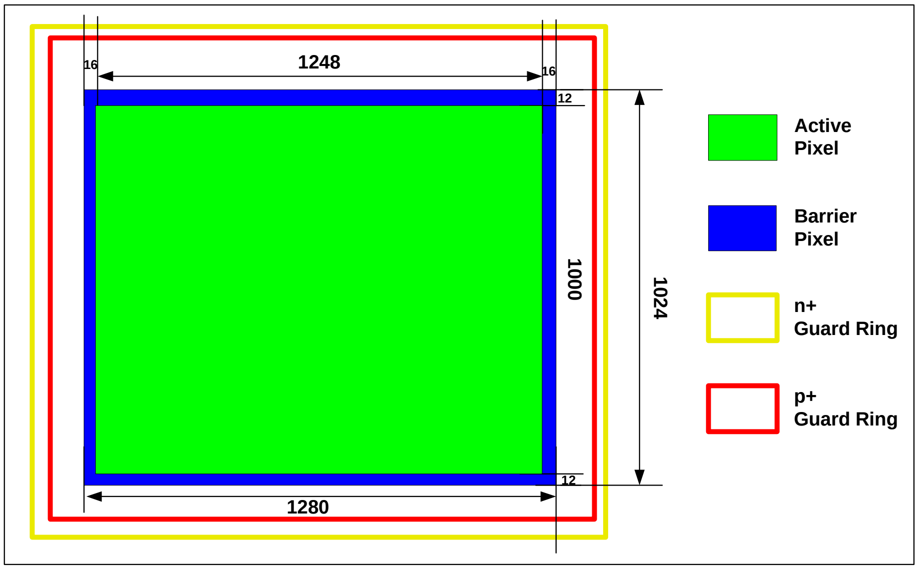


Figure 4.2: Array configuration of the prototype CMOS image sensor

In order to obtain high quality images, it is important that the peripheral circuitry does not interfere with the pixel cells of the array. During the sensor operation, the peripheral circuitry can generate charge carriers, e. g. electrons. If the peripheral circuitry is adjacent to the array, the electrons generated by the periphery circuitry can travel to and interfere with the array pixel cells, especially those pixels on the edges of the array adjacent to the peripheral circuitry. The interfering electrons are misinterpreted as a true pixel signal and image distortion can occur [89]. The n^+ and p^+ guard ring placed around the pixel array will minimize the noise generated from the peripheral circuitry.

A special designed barrier pixel array was placed on the edges of the pixel array to further reduce the interference between the peripheral circuitry and the pixel array [89]. The schematic of the dual conversion gain barrier pixel is shown in Figure 4.3. Compared to the regular dual conversion gain pixel, there is no transfer gate in the barrier pixel. Both photodiode and floating diffusion nodes are connected and shorted to V_{pix}. The high V_{pix} potential will fully deplete the photodiode and the floating diffusion region. Each barrier region collects charge in the charge accumulation region, and the charge is drained from the barrier region to the V_{pix} node. In this manner, the barrier regions serve to isolate the adjacent structures and prevent interference from excess charge. [89]

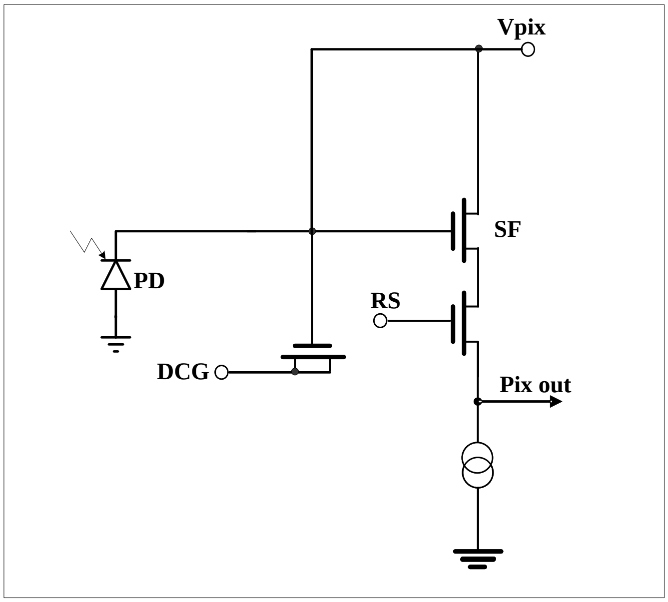


Figure 4.3: Schematic of the dual conversion gain barrier pixel

4.3 Row Decoder and Driver Design

4.3.1 Row Decoder

Several readout modes - electronic rolling shutter (ERS) readout, global reset release (GRR) mode, window readout, and skip readout – can be easily implemented in

CMOS images sensors. Two main structures of the readout control circuit are a shift register and a decoder. Shift registers are relatively easy to implement and use fewer transistors than decoders; however the shift registers cannot be programmed for random access readouts because the shift registers produce only sequential outputs from the first element to the last one. The decoder is preferred for true random access readout controls because the sequence of the outputs can be selected by the input of the decoders. In this design, the decode scheme was implemented.

The block diagram of the row decoder design is shown in Figure 4.4. A binary code is used for the row decoder. The 10-bit row addresses are fed into inverters and buffers to generate the complementary addresses to drive the row decode cell. All decoders were built by a basic cell as shown in Figure 4.5. The row decode cell includes two 5-input NAND gates and one 2-input NOR gate. The output signals of the row decoder were used to select the corresponding row drivers.

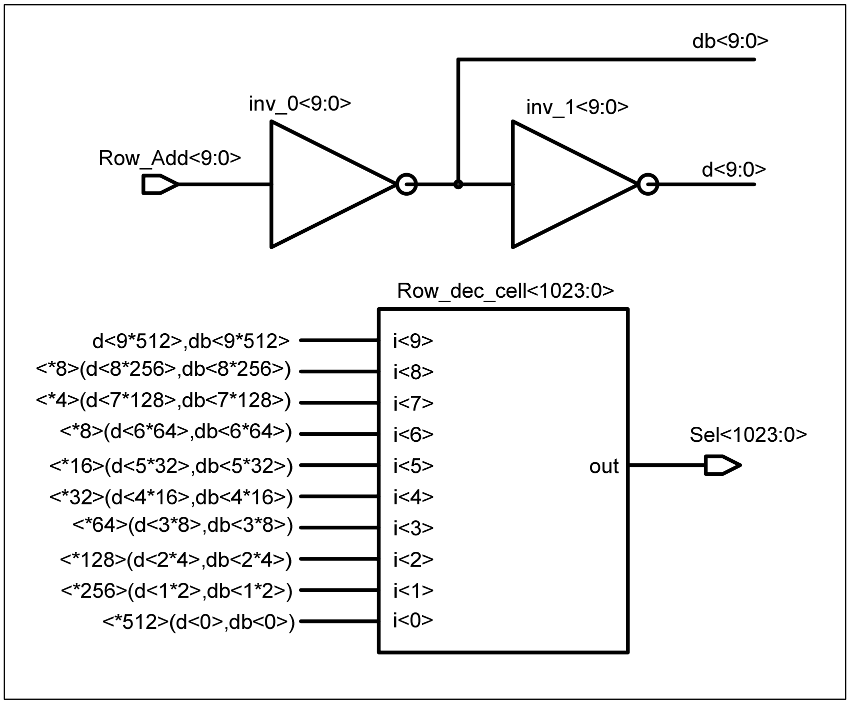


Figure 4.4: Block diagram of the row decoder design

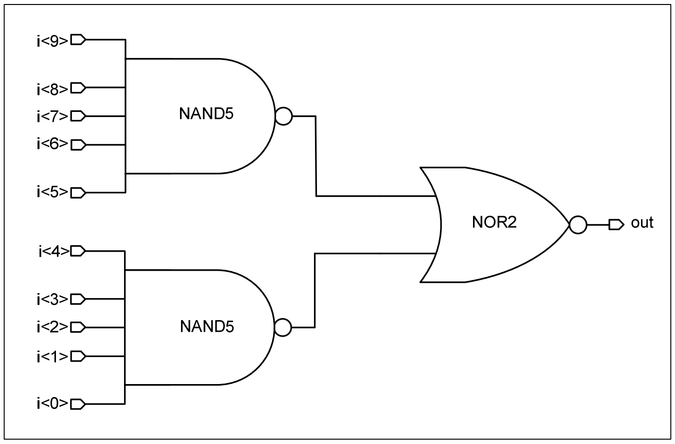


Figure 4.5: Block diagram of the row decoder cell design

4.3.2 Row Driver Design

Four control signals are needed for each row of pixels to enable full operation of the prototype image sensor: the TX signal to control the transfer gate, the RST signal to control the reset transistor, the ROW select signal to control the row select transistor, and the DCG signal to control the source and drain terminals of the dual conversion gain transistor. Figure 4.6 illustrates the block diagram of the row driver design for each row. The row drivers output TX, ROW, RST, and DCG signals that control the corresponding transistors in the pixel array depending on the select signal output from the row decoder. Each signal (TX, ROW, RST and DCG) is driven by the same row driver cell, which takes 6 input signals: *Sel*, *En_**, *Global_**, *Latch_**, **_Hi*, and **_Lo* as shown in Figure 4.7

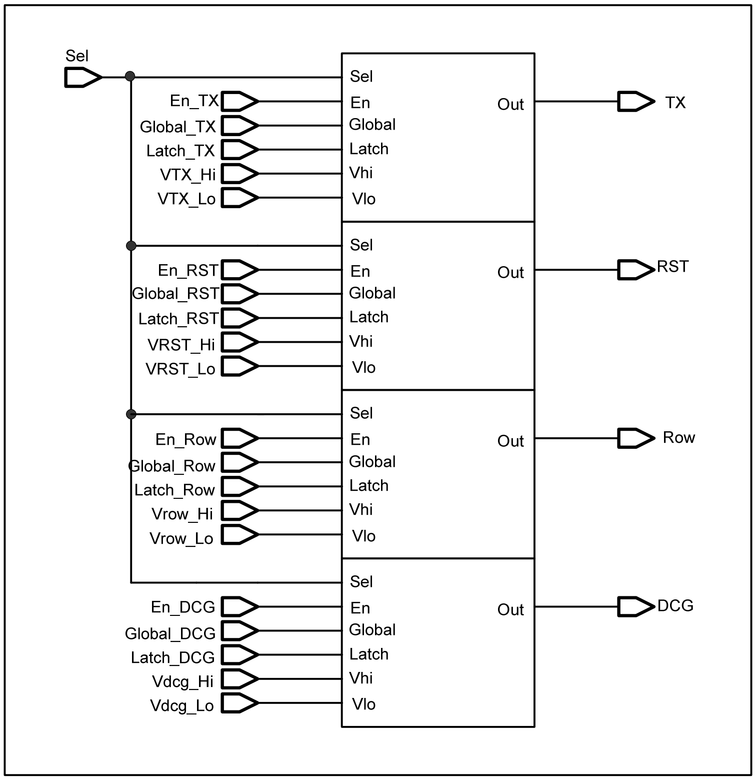


Figure 4.6: Block diagram of the row driver design

Each row driver cells composes of two 2-input NAND gate, one D flip-flop latch, and one level shifter as shown in Figure 4.7. The *Sel* signal is the output of the row decoder to select the addressed row. *Latch_** and *en_** signals are active high. When *Sel* is enabled, the output of the latch is set to the state of *En* when the latch signal is high. The *global_** signal was implemented in the row driver for controlling the signals for the entire row to support global shutter release mode operation. The *global_** is active low; when it is enabled, the output of the latch will be set to *En* for all rows simultaneously.

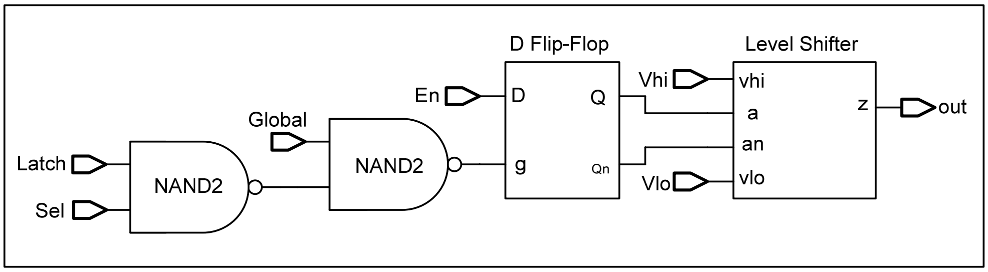


Figure 4.7: Block diagram of row driver cell design

The detail block diagram of the D flip-flop latch is shown in Figure 4.8. The signal (*g*) is the output signal from the second NAND gate. When the signal (*g*) stays at a low potential, the transmission gate TG1 is off while TG2 is on. The next state output will hold the previous state. When the signal (*g*) goes to high, the TG1 stays on and TG2 stays off, such that the output (*Q*) of the latch will be set to the state presented by (*D*).

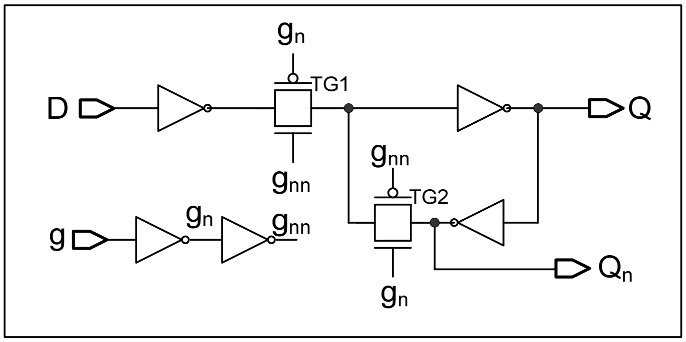


Figure 4.8: Schematics of the D flip-flop latch

The truth table of the D flip-flop latch is shown in Table 4.1. When the node (g) stays at a low potential, the D flip-flop stays at a hold state, and it stays at a set state when the node (*g*) goes to a high potential.

Table 4.1: Truth table of the D flip-flop

D	g	Q	Q' (next state)	
0	0	0	0	hold
0	0	1	1	
1	0	0	0	
1	0	1	1	
0	1	0	0	set
0	1	1	0	
1	1	0	1	
1	1	1	1	

The complementary outputs of the latch, Q and Q_n, are used to control the level shifter as shown in Figure 4.7. The V_{LO} and V_{HI} voltages are brought externally from different pads for each row driver signal to allow the flexible control. The detail schematic of the level shifter is shown in Figure 4.9. The V_{HI} voltage is connected the source of PMOS transistors: MP1, MP3 and Mp5, while the V_{LO} voltage is only connected to the source of MN5.

When the input (*A*) of the level shifter is at a high potential (V_{DD}) and the complementary input signal (*AN*) of the level shifter stays at a low potential (*GND*), the MN1 is turned on, and the (*DN1*) node will be discharged to a low potential, which in turn turns on the NMOS MN2. Therefore, the (*ZN*) node will be discharged to a low potential. The low potential at the (*AN*) node turns the MN3 off and turns the PMOS transistor MP4 on; meanwhile, the low potential at the (*ZN*) node turns the MP3 on. Both MP3 and MP4 will charge the (*ZP*) node to a high potential, which turns off the MP1. The low potential of the (*ZN*) node turns the MP5 on; the output node of the level shifter (*Z*) will be charged to V_{HI}.

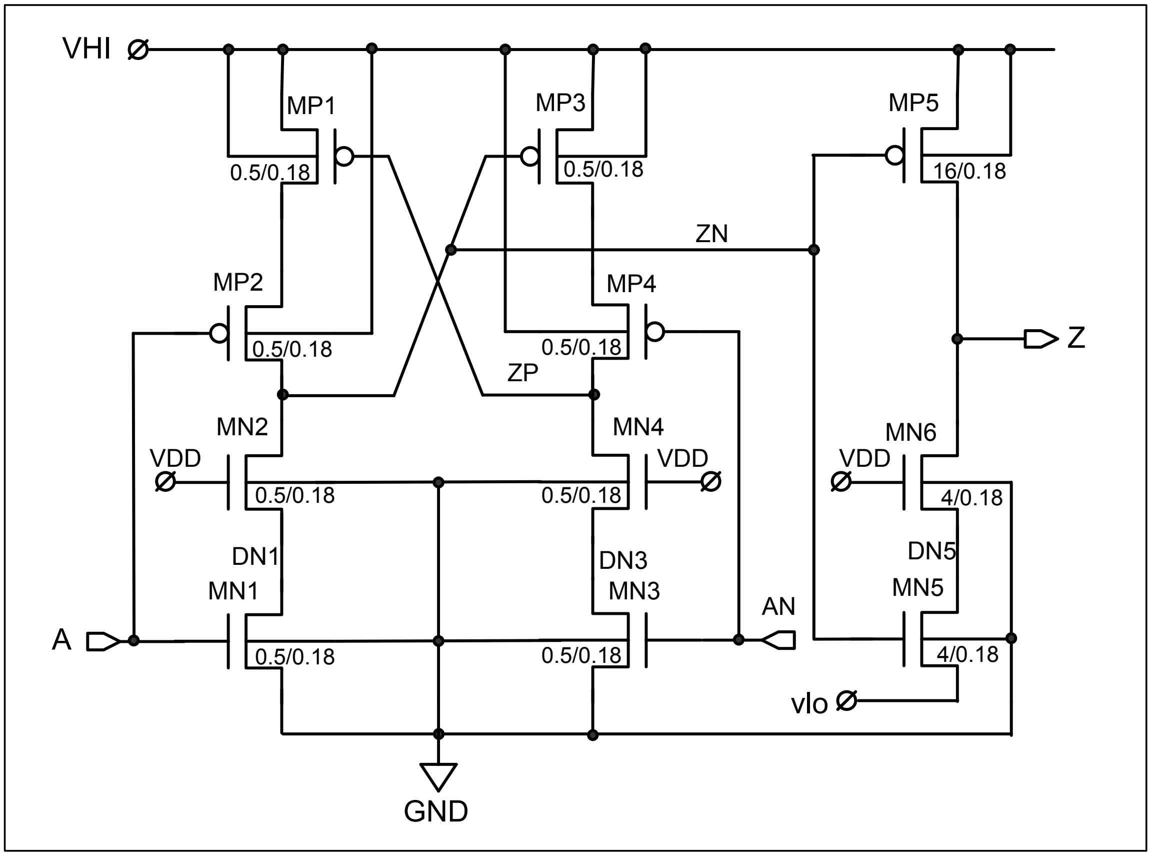


Figure 4.9: Schematic of the level shifter design

When the input (*A*) of the level shifter is at a low potential (*GND*), the complementary input signal (*AN*) stays a high potential (V_{DD}). The high voltage of the node (*AN*) turns the NMOS transistor MN3 and MN4 on, which discharges the (*ZP*) node to a low potential, and then turns the PMOS transistor MP1 on. Both MP1 and MP2 will charge the (ZN) node to a high potential, which turns the MN5 and MN6 on and discharges the output node (Z) to V_{LO} potential.

A transient analysis was performed to simulate the level shifter operation as shown in Figure 4.10. A $2pF$ capacitor was added to the level shifter output node to simulate the row driver load. Simulation results show that it takes about 6ns to charge the output node to V_{HI} (3.8V in the simulation) and takes about 8ns to discharge to V_{LO} (negative $400mV$), which is good enough for the prototype sensor pixel operation.

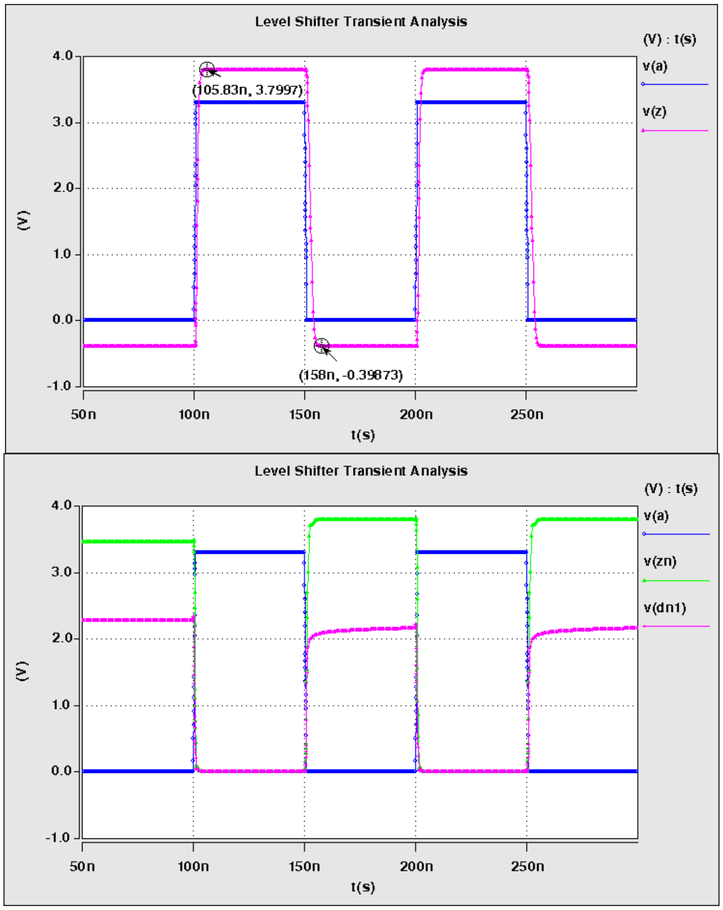


Figure 4.10: Transient analysis of the level shifter with $2pF$ capacitance load

Several NMOS transistors (MN2, MN4, and MN6) were inserted between the NMOS network and PMOS network as shown in Figure 4.9 to reduce voltage stress of the NMOS transistors: MN1, MN3, and MN5 respectively. The gates of MN2, MN4, and MN6 were connected to the power supply voltage V_{DD}. From Figure 4.10, it can be seen that when the input signal is low, the MN1 is off and the drain of the MN1 node is clamped to one threshold voltage lower than V_{DD}. The node (Zn) was charged to V_{HI}. Thus, the high potential of V_{HI} was redistributed between MN1 and MN2, which significantly reduced the NMOS channel hot carrier effect.

4.4 Column Readout Circuitry Design

4.4.1 Column Bias Current Circuitry

VLN column circuitry forms the current sink part of the pixel source follower amplifier [90]. For this prototype sensor, $50\mu A$ current was supplied off the chip, which mirrors to $5\mu A$ for each column as shown in Figure 4.11.

The whole column source follower circuitry is composed of four NMOS transistors as shown in Figure 4.11. The upper half are located inside the pixels while the lower half are shared by a column of pixels that are connected the common column bus. Two of the transistors work as switches. One is the row select transistor which is activated during the pixel to column readout. The other one is located at the bottom of the column bus and is controlled by the VLN_EN pulse. The VLN_EN is turned on during pixel readout time and turned off after that to save power.

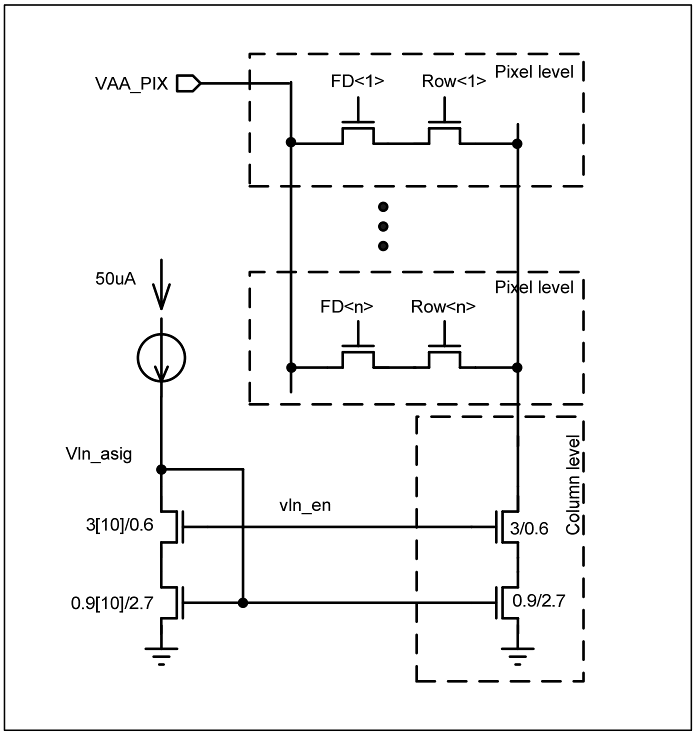


Figure 4.11: Schematic of column bias circuitry

4.4.2 Column Decoder

Column addresses switch much faster than the row addresses for the prototype image sensor. In order to reduce the glitches during the switch operation, the gray code was selected for the column decoder such that the adjacent addresses have only single digit differing by 1.

The block diagram of the column decoder is shown in Figure 4.12. The column decoder is composed of column address inverter and buffer, coarse decoders, and fine decoders. The column address inverter and buffer generate 11-bit complementary addresses to control the logic of the column decoder. The whole column decoder was divided into 40 groups. Each group has a coarse decoder and a fine decoder. The coarse decoder is a 6-input AND gate. Each unique input generates 32 identical outputs. The output of the coarse decoder also acts as enable signals for the fine decoders. The fine decoder is a 5-input AND gate and generates 32 column select signals. Both group select signals and columns select signals are used to control the logic of the column sample and hold circuitry.

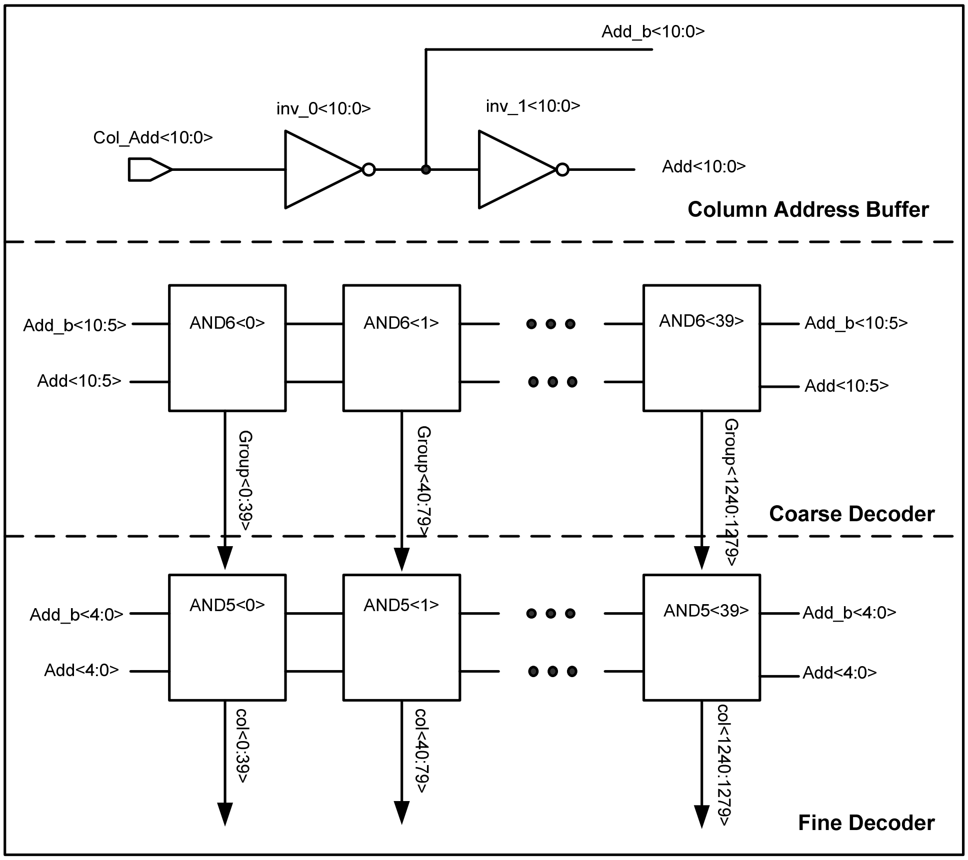


Figure 4.12: Block diagram of the column decoder design

4.4.3 Column Sample and Hold Circuitry

The schematic of the sample and hold circuitry used in the prototype image sensor is shown in Figure 4.13. During the pixel to column readout period, the Clamp switch is on such that the top plate of C_{rst} and C_{sig} are clamped to V_{CL}. The charges on the pixel output line are sampled to the C_{rst} when the SHR switch is on and to the C_{sig} when the

SHS is enabled. During the column to amplifier readout, the Clamp switch will be turned off. The crow-bar (*cb*) switch will be turned off during amplifier reset period and turned on during charge amplifying phase.

The minimum value of the sample and hold capacitor is determined by the kTC noise limitation. A $2pF$ poly-to-poly capacitances was chosen for both C_{rst} and C_{sig}, which gives a noise of $45\mu V$. The bottom plates of the sample and hold poly-to-poly capacitors were connected to pixel output signals to suppress the substrate noise and reduce settling time [27]. The output of the column sample and hold capacitors are fed into the crow-bar charge amplifier controlled by the column select (*Col*) and group select signals as shown in Figure 4.13.

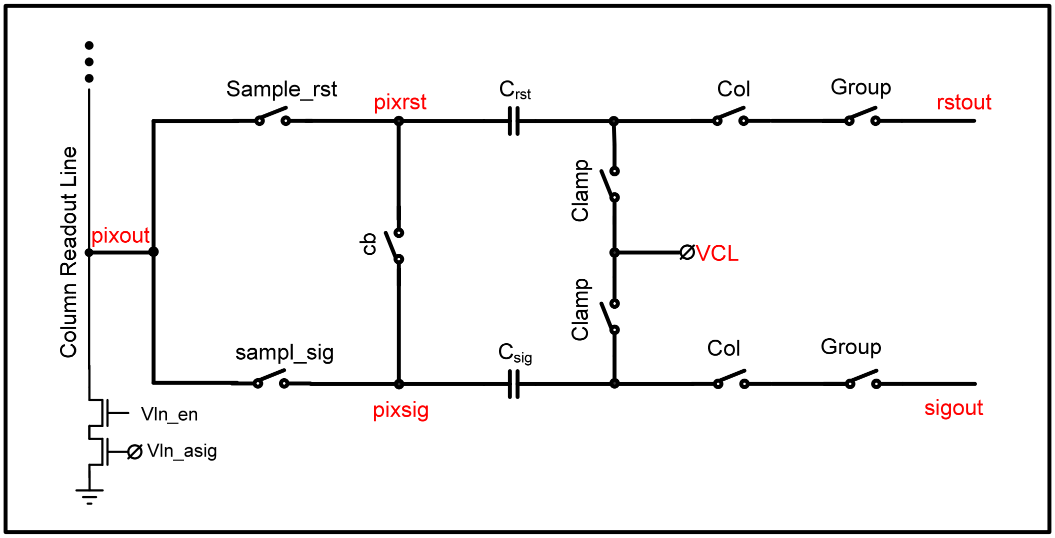


Figure 4.13: Block diagram of the column sample and hold circuitry

4.5 Crow-Bar Charge Amplifier Design

The crow-bar charge amplifier is composed of one nonoverlapping clock generator block, a fully differential cascode amplifier with switched-capacitor common mode feedback (CMFB) circuitry, and several poly-to-poly capacitors for programmable gain control. The crow-bar amplifier was designed for 24MHz operation.

4.5.1 Nonoverlapping Clock Signals

In order to support the switched capacitor CMFB and crow-bar amplifier operation, a pair of nonoverlapping clock signals (*phi1* and *phi2*) were generated on chip as shown in Figure 4.14. Besides the *phi1* and *phi2* clock signals, clock signals *phi1pp* and *phi2pp* were also generated on chip, which have their falling edges slightly earlier than *phi1* and *phi2*, respectively. The *phi1pp* and *phi2pp* were used to reduce potential charge injection and clock feed through effects.

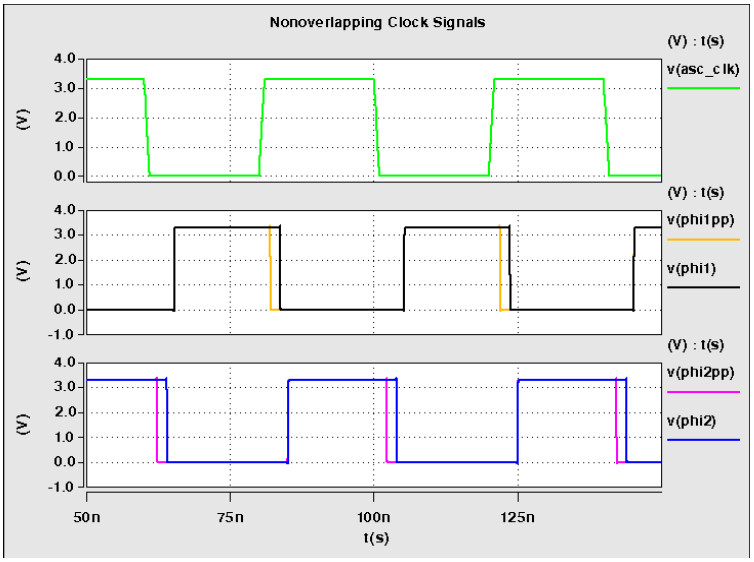


Figure 4.14: Nonoverlapping clock signals for the crow-bar amplifier

4.5.2 Cascode Amplifier Bias Network

The bias network for the cascode amplifier is shown in Figure 4.15. All transistor sizes and the number of fingers are listed in Table 4.2. The current through NMOS transistors MN01 and MN02 is tunable through off chip current sink. The bias transistors have a size ratio of 1:2, which means that if a 12.5μA current is fed through MN01 and MN02, a 25μA current will flow through all other four branches. Five series connected NMOS MN31-MN35 were used to generate V_{biasnc} to bias the cascode NMOS transistor while 7 PMOS MP11-MP17 were used to generate the V_{biaspc} to bias the cascode PMOS transistor in the cascode amplifier. The V_{biasp} and V_{biasn} are used to bias the PMOS and NMOS in the cascode amplifier, respectively.

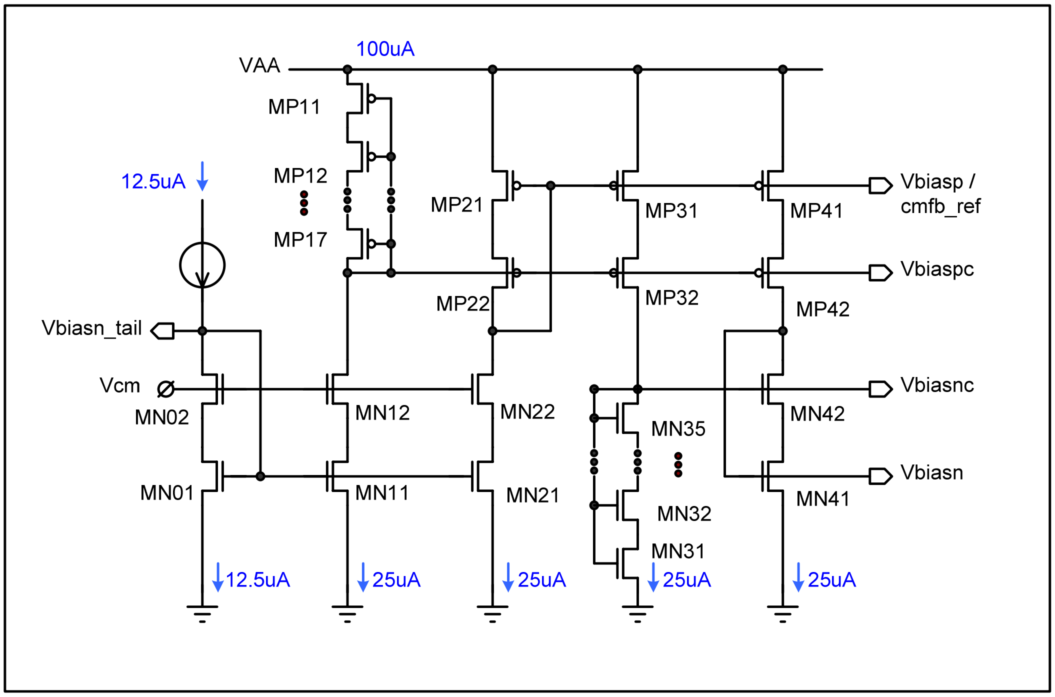


Figure 4.15: Bias network for the cascode amplifier

Five de-coupling capacitors were used for the five primary bias voltages, V_{biasn}, V_{biasnc}, and V_{biasn_tail} are de-coupled to AGND while V_{biasp} and V_{biaspc} are de-coupled to the power supply voltage V_{AA}. The values of the de-coupling capacitors were chosen at $4pF$. During the power down mode, the NMOS bias voltages V_{biasn}, V_{biasnc}, and V_{biasn_tail} are all connected to AGND while PMOS bias voltages V_{biasp} and V_{biaspc} are both connected to V_{AA}.

Table 4.2: Transistor sizes and number of fingers used in the bias network

Transistor Number	Number of Fingers	W/L (μm/μm)	Transistor Number	Number of Fingers	W/L (μm/μm)
MN01	1	5/1	MP11	1	6.6/0.4
MN02	1	6.6/0.3	MP12	1	6.6/0.4
MN11	2	5/1	MP13	1	6.6/0.4
MN12	2	6.6/3	MP14	1	6.6/0.4
MN21	2	5/1	MP15	1	6.6/0.4
MN22	2	6.6/0.3	MP16	1	6.6/0.4
MN31	1	6.6/1.2	MP17	1	6.6/0.4
MN32	1	6.6/1.2	MP21	1	6.6/0.5
MN33	1	6.6/1.2	MP22	1	6.6/0.4
MN34	1	6.6/1.2	MP31	1	6.6/0.5
MN35	1	6.6/1.2	MP32	1	6.6/0.4
MN41	1	6.6/1.2	MP41	1	6.6/0.5
MN42	2	6.6/1.2	MP42	1	6.6/0.4

Figure 4.16 shows the simulation result of the bias network. From Figure 4.16, it can be seen that while the V_{AA} increases from 2.8V to 4.0V, the NMOS bias voltages V_{biasn}, V_{biasnc}, and V_{biasn_tail} are very stable while the PMOS bias voltages V_{biasp} (or V_{cmfb_ref}) and V_{biaspc} increase linearly with V_{AA}, which confirms that the bias network can work well with a wide power supply voltage range.

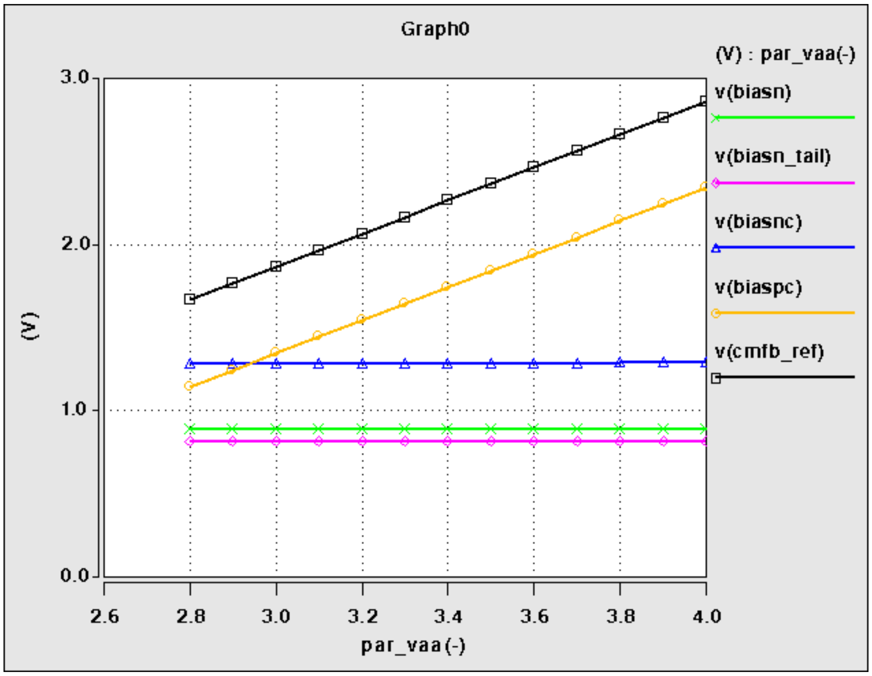


Figure 4.16: Simulation results of the bias network with different power supply voltages

4.5.3 Fully Differential Folded Cascode Amplifier

The differential amplifier has two input nodes and only amplifies the difference between them. The differential structure can provide high common mode rejection and power supply rejection ratio. Also the cascode amplifier structure isolates the input from the output and has a higher gain and better frequency response [91]. The folded cascode architecture increases the output swing with the cost of consuming slightly more power [92]. The schematic of the fully differential folded cascode amplifier used in the crow-bar amplifier was shown in Figure 4.17.All transistor sizes and numbers of fingers are listed in Table 4.3. Large transistors were used to drive large output load. There is about 850µA current flowing through each branch.

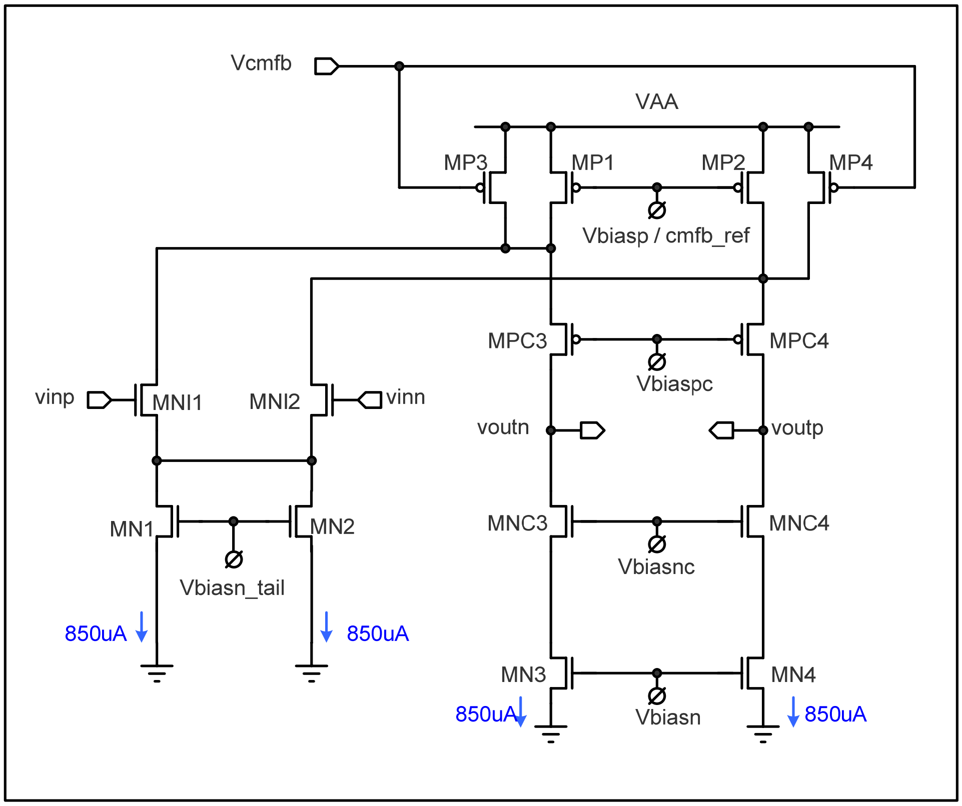


Figure 4.17: Schematic of the fully differential folded cascode amplifier

Table 4.3: Transistor sizes and number of fingers used in the differential amplifier

Transistor Number	Number of Fingers	W/L (μm/μm)	Transistor Number	Number of Fingers	W/L (μm/μm)
MN1	68	5/1	MP1	34	6.6/0.5
MN2	68	5/1	MP2	34	6.6/0.5
MNI1	68	6.6/0.3	MP3	34	6.6/0.5
MNI2	68	6.6/0.3	MP4	34	6.6/0.5
MN3	34	6.6/1.2			
MN4	34	6.6/1.2			
MNC3	68	6.6/1.2			
MNC4	68	6.6/1.2			

The N-type input stage was used in the differential amplifier. The input stage bias transistors MN1 and MN2 are biased by V_{biasn_tail}. The MP1 and MP2 are biased by the V_{biasp} while MP3 and MP4 are biased by the common mode feedback voltage, V_{CMFB}.

Ideally this voltage should be the same as the V_{biasp}. The cascode PMOS transistor MPC3 and MPC4 are biased by the V_{biaspc} while the cascode NMOS transistor MNC3 and MNC4 are biased at V_{biasnc}. NMOS MN3 and MN4 are biased by the V_{biasn}.

Figure 4.18 shows the AC simulation results of the amplifier with 2*pF* capacitor loads on each output node. More than 60*dB* was achieved for the open loop gain with a unity gain bandwidth of 775*MHz*. From Figure 4.18, it can be seen that the phase margin is about 67°, which results in a stable operation.

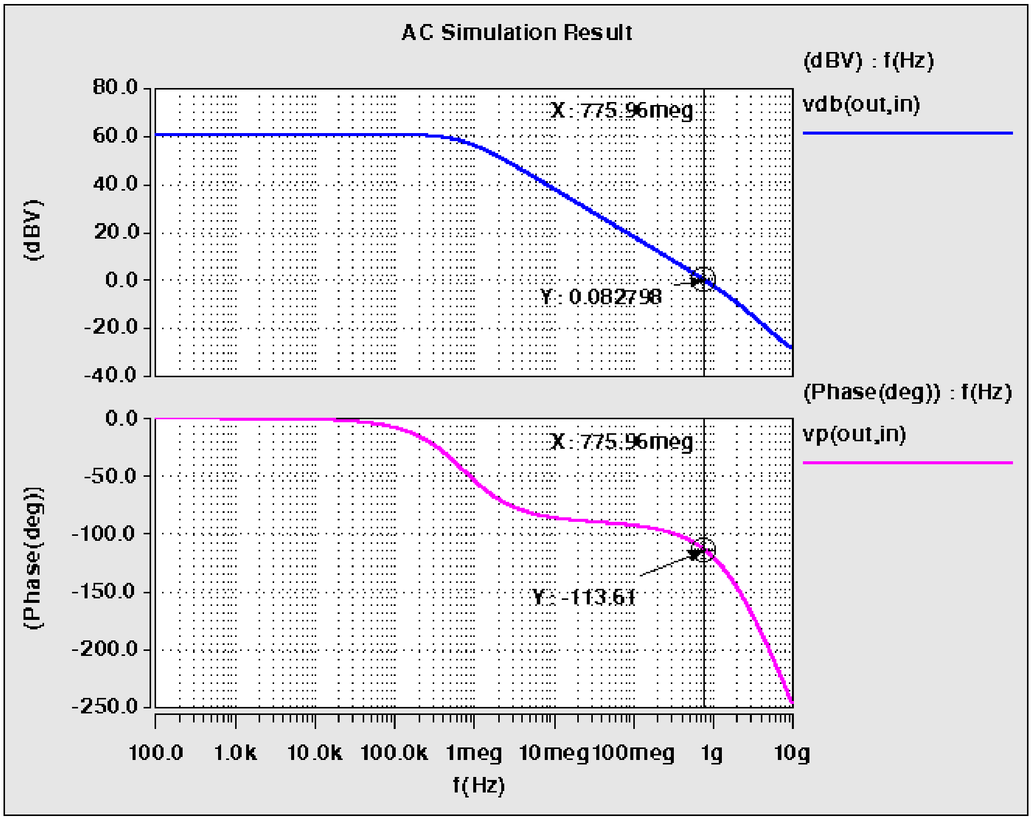


Figure 4.18: AC simulation result of the differential cascode amplifier with 2*pF* output load

4.5.4 Switched-Capacitor Common Mode Feedback

The switched-capacitor common mode feedback (SC CMFB) circuitry was implemented in this prototype sensor design as shown in Figure 4.19. The V_{outp} and V_{outn} are the output of the fully differential amplifier while the V_{cm} is the common-mode voltage. The V_{cmfb_ref} is the one of the output voltages of the bias network to bias the PMOS in the cascode amplifier. V_{cmfb} is the common mode feedback voltage for the differential amplifier.

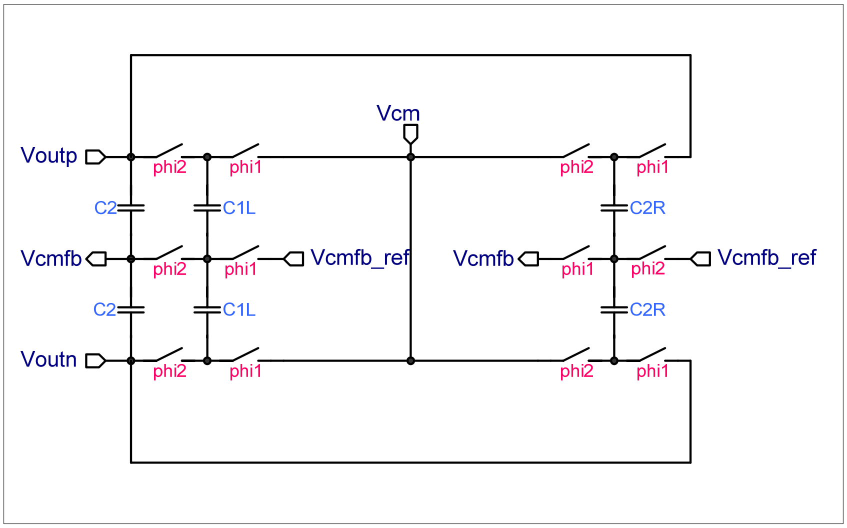


Figure 4.19: Switched-capacitor CMFB circuitry

The C_2 capacitors with a value of 100fF were used for the high-speed averaging. The switched capacitor resistors are formed with left side of capacitors C_{1L}, which perform both the averaging and the differencing needed in the CMFB amplifier. 50fF capacitors were chosen for C_{1L} such that the changes in V_{cmfb} during one clock cycle won't be too large due to the difference between the V_{cmfb_ref} and the actual V_{cmfb} [27]. The right side capacitors C_{1R} with the same value of 50fF were used for resetting the differential output nodes during the reset phase. The *phi2* control switches connected to amplifier outputs, V_{outp} and V_{outn}, are transmission gates such that the circuit can provide balancing from power supply V_{AA} to ground. The output of the switched-capacitor CMFB V_{cmfb} provides negative feedback to the amplifier.

4.5.5 Crow-Bar Charge Amplifier

The overall block diagram of the crow-bar amplifier is shown in Figure 4.20. The operation of the crow-bar amplifier is controlled by the nonoverlapping clock signals, *phi1* and *phi2*. During the reset phase, *phi1*, both inputs and outputs of the amplifiers are reset to common mode voltage V_{cm}; also both sides of the feedback capacitor are connected to the same common-mode voltage. The inputs of the amplifier are controlled by the *phi1pp* switches to ensure that both inputs and outputs of the amplifier are reset to the common mode voltage.

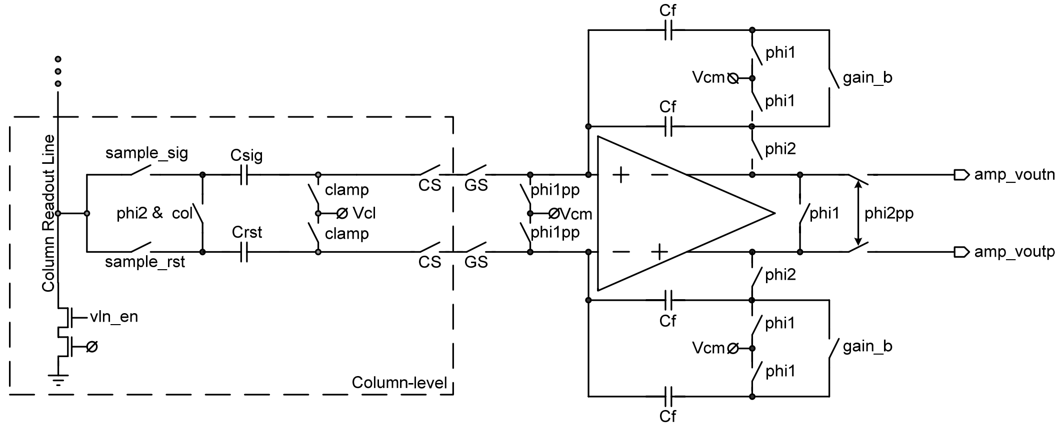


Figure 4.20: Block diagram of the output crow-bar amplifier including the column sample and hold circuitry

During the amplifying phase, *phi2*, the bottom plate of the sample and hold capacitors are shorted for the particular column being readout; the feedback capacitors C_f are connected to the amplifier. The charges on the column sample and hold capacitors are injected into the output buses. Thus, charges are essentially moved from the column sample and hold capacitors to the feedback capacitors. The value of this feedback capacitor sets the stage voltage gain. As was discussed earlier, $2pF$ capacitors were chosen for the column sample and hold capacitors. A capacitor value of $1pF$ was used for the feedback capacitor C_f. When the "gain" is not enabled ("gain" at a low potential and "gain_b" at a high potential), both feedback capacitors are connected to the amplifier. The gain of the amplifier can be given by:

$$A_{amp} = \frac{C_{rst}}{C_f + C_f} = \frac{C_{sig}}{C_f + C_f} = \frac{2p}{1p + 1p} = 1 \tag{4.1}$$

So a unity gain is achieved when the "gain" is not enabled. However, when the "gain" is enabled, only one feedback capacitor is connected to the amplifier such that 2 times voltage gain is achieved:

$$A_{amp} = \frac{C_{rst}}{C_f} = \frac{C_{sig}}{C_f} = \frac{2p}{1p} = 2 \tag{4.2}$$

Figure 4.21 shows the transient simulation result of the crow-bar charge amplifier with 2 times voltage gain. A common mode voltage of $1.4V$ was used for this simulation and $300mV$ differential input signals were fed into the column sample and hold capacitors. The output of the amplifier stays at ground potential at the beginning of the simulation. From Figure 4.21, it can be seen that it takes about 8 clock cycles for the differential output to settle 600mV above and below the common mode voltage, which corresponds to 2 times voltage gain.

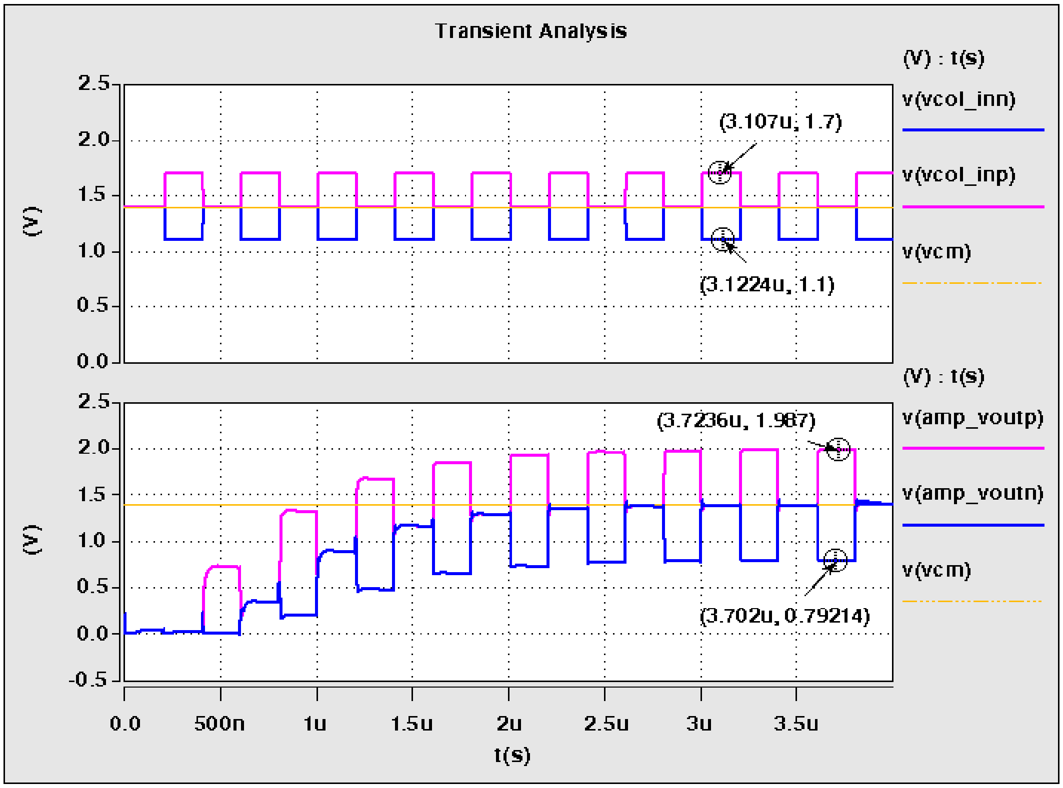


Figure 4.21: Transient analysis of the crow-bar charge amplifier with switched-capacitor CMFB and 2x gain

Figure 4.22 shows the crow-bar charge amplifier characteristics with 2 times gain enabled. As depicted in Figure 4.22, differential amplifier output increases linearly with the increase of the differential input. The output swing can go more than ±1V with 1.4V common mode voltage, which meets the prototype image sensor dual conversion gain pixel operation requirement.

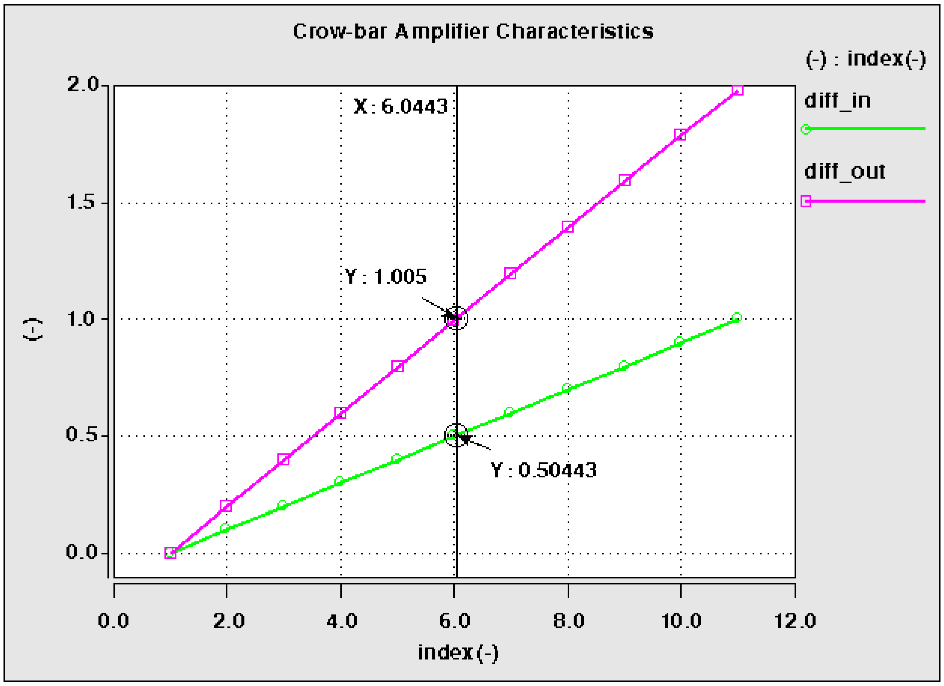


Figure 4.22: Crow-bar amplifier characteristics with 2x gain

4.6 Prototype Image Sensor Timing Control

To control the exposure time, CMOS image sensors require an additional reset scan in which the shutter pulses scan the pixel array prior to a readout scanning [93]. The interval between the reset pulse and the readout pulse determines the exposure time [90].

Reading a row starts with storing a row pixel's information in column sample-and-hold circuits. This period is called the pixel to column sampling or row time. The second period is called the shutter reset period, during which the $<n+m>^{th}$ row was reset and starts integration. Thus, the row selection logic drives 2 separate sets of address. The first address set is used for reading the addressed row, which is called read address pointer. The second address is the reset address pointer used for conditioning a separate row to start integrating. The time lapse between starting the integration row for a particular row and reading that row is called integration time [90]. After the pixel to column sampling period, each column is scanned out by enabling the column select and group select signals. The signals on the sample and hold capacitors for each pixel in the row are transferred to the output crow-bar charge amplifier.

All these readout sequences for both the low conversion gain mode and the high conversion gain mode are depicted in Figure 4.23 and Figure 4.24, respectively. Since latch type row drivers were implemented on the prototype sensor design, the output signals used to control the pixel operation is set to the *En_** state when the latch signal goes to high. As shown in Figure 4.23 and Figure 4.24, in order to reset the floating diffusion node at the beginning of pixel to column readout period, first the *en_RST* signal is turned on, and then the *latch_RST* signal is turned on to latch the RST signal to a high potential V_{RST_HI}. After about 500ns, the *en_RST* is turned off and the RST signal is latch to low at the rising edge of the *latch_RST* signal. The same signal control method was used for TX, RS, and DCG signal.

For the low conversion gain mode, the DCG signal will be latched to a low potential (V_{DCG_LO}) to drive the drain and source terminals of the dual conversion gain transistor such that the transistor is working in the strong inversion mode. The inversion mode capacitor will be added to floating diffusion node to increase the floating diffusion node charge handling capacity, and a low conversion gain is achieved. The DCG signal stays at low for both the pixel to column sampling period and the rolling shutter reset period as shown in Figure 4.23.

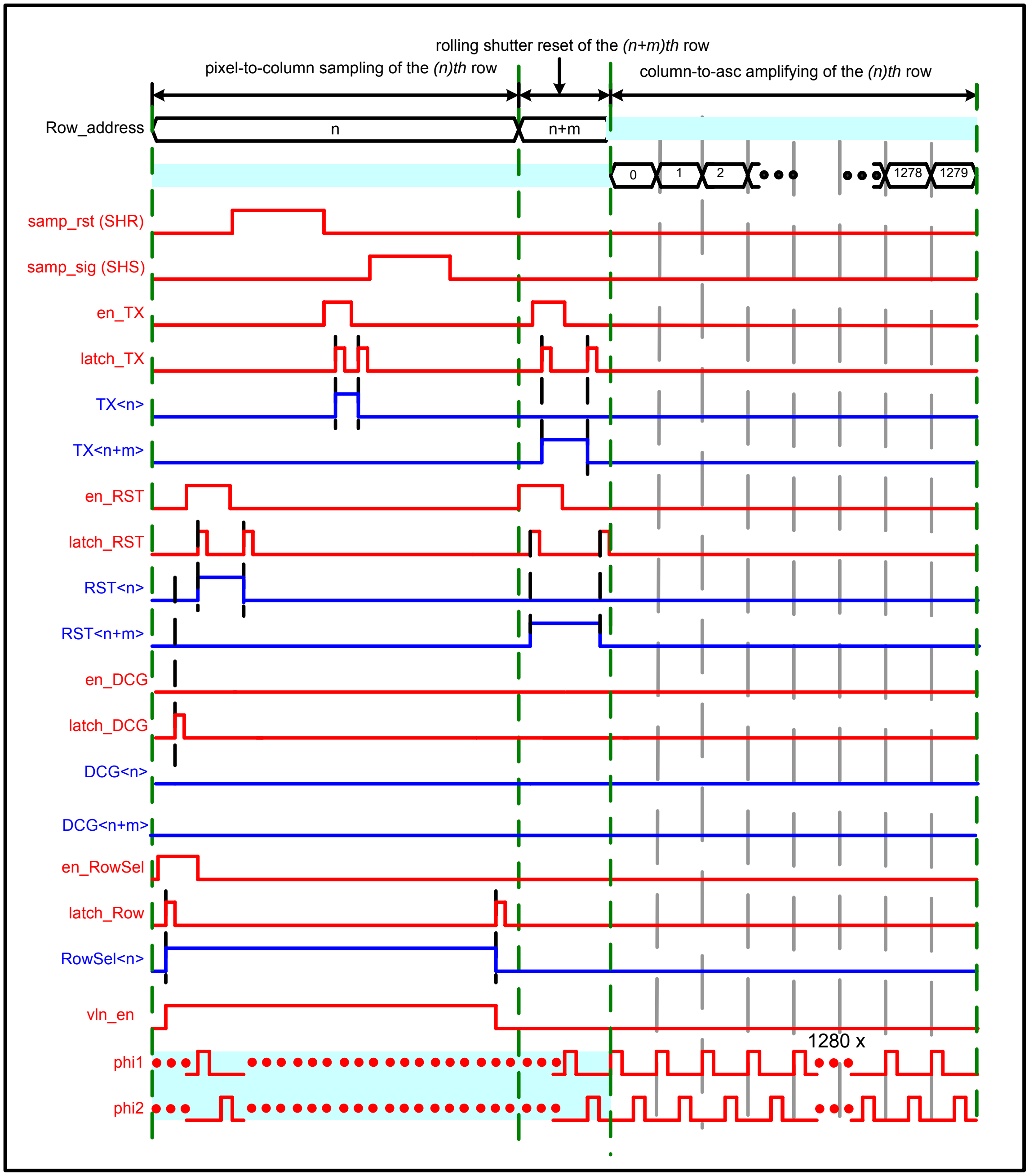


Figure 4.23: Readout timing diagram for the low conversion gain mode operation

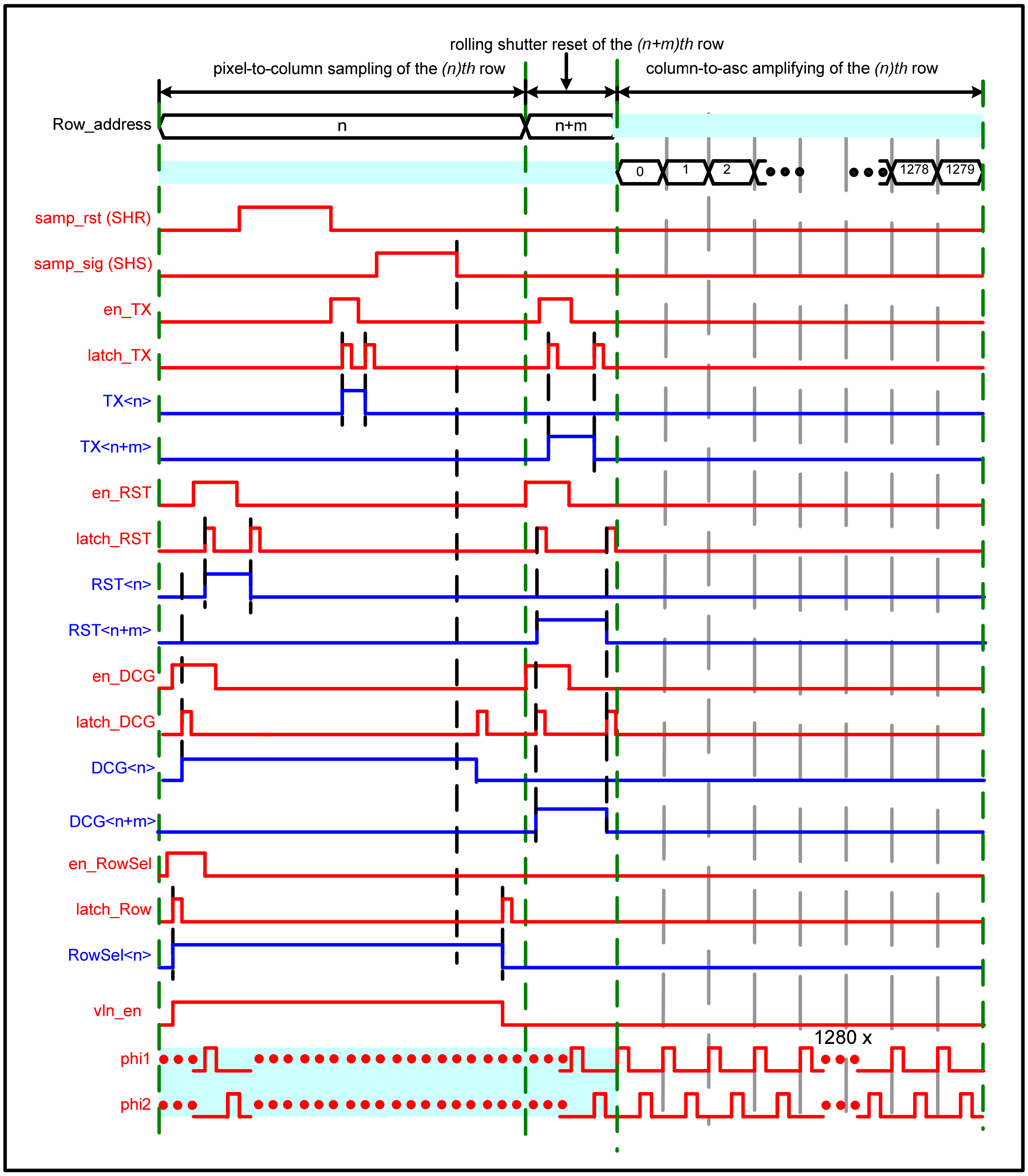


Figure 4.24: Readout timing diagram for the high conversion gain mode operation

For the high conversion gain mode as shown in Figure 4.24, the DCG signal will be latched to a high potential (V_{DCG_HI}) by turning on both *en_DCG* signal and *latch_DCG* signal at the pixel to column sampling period and the rolling shutter readout period. The high DCG signal drives the dual conversion gain transistor in the depletion mode; thus a high conversion gain is achieved.

Right after the pixel to column sampling period and rolling shutter reset period, the column to amplifier readout period (or column readout) starts as depicted in Figure 4.25. During this period, all sample signals on the sample and hold capacitors were shifted out to the global charge amplifier one by one. The detail timing diagram for a single column and the control signals for the global charge amplifier are shown in Figure 4.25.

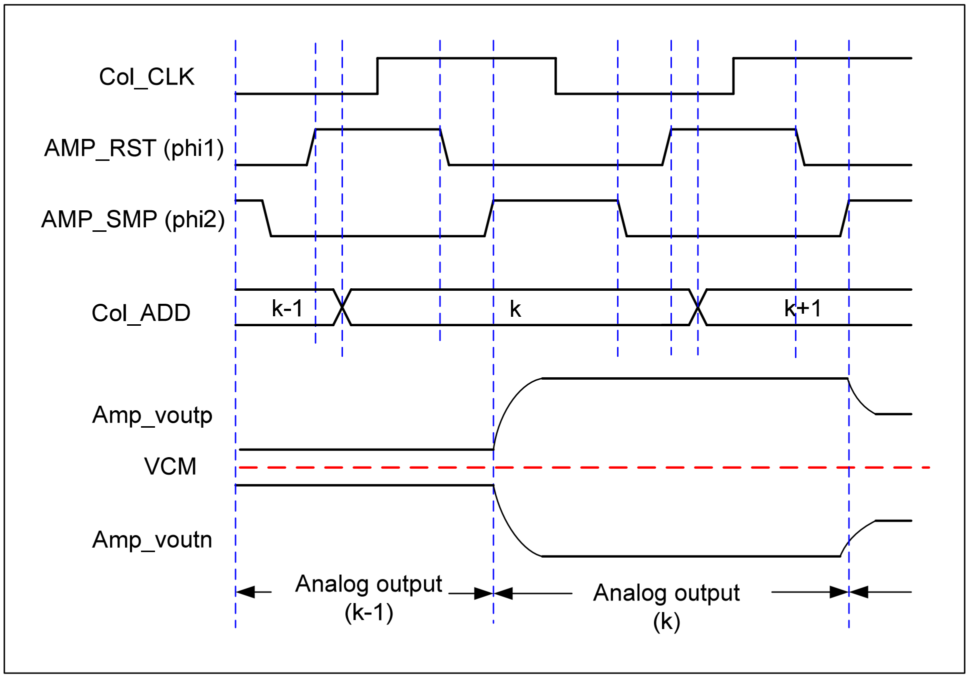


Figure 4.25: Global output amplifier control signals

The nonoverlapping clock control signals *phi1* and *phi2* were generated on chip based on *Col_CLK* signal. During the *phi1* phase, both inputs and outputs of the differential charge amplifier were reset to the common mode voltage V_{CM}. The column address was updated with the new address after the *phi1* goes to high. During the *phi2* phase, the charges on the sample and hold capacitors are amplified, and the output signals (*amp_voutn* and *amp_voutp*) of the amplifier are charged or discharged to the opposite direction centered at the common mode voltage V_{CM}. Then the differential output signals are buffered off chip by a unity gain amplifier.

4.7 Prototype Image Sensor Micrograph

The specifications of the prototype image sensor are given in Table 4.4.

Table 4.4: CMOS APS Prototype image sensor specifications

Process	0.13μm CMOS (2P3M)
Pixel Size	5.6 μm x 5.6μm
Pixel Type	5T Dual Conversion Gain Pixel
Array dimension	1280 (Column) x 1024 (Row)
Output Format	Differential Analog
Power Supply (V_{AA})	4V
Power Supply (V_{PIX})	3.3V
Power Supply (V_{DD})	3.3V
Power Consumption	<50mW
Master Clock	24MHz
Package	84-pin CLCC
Die size	8mm x 8mm
Package Size	29mm x 29mm

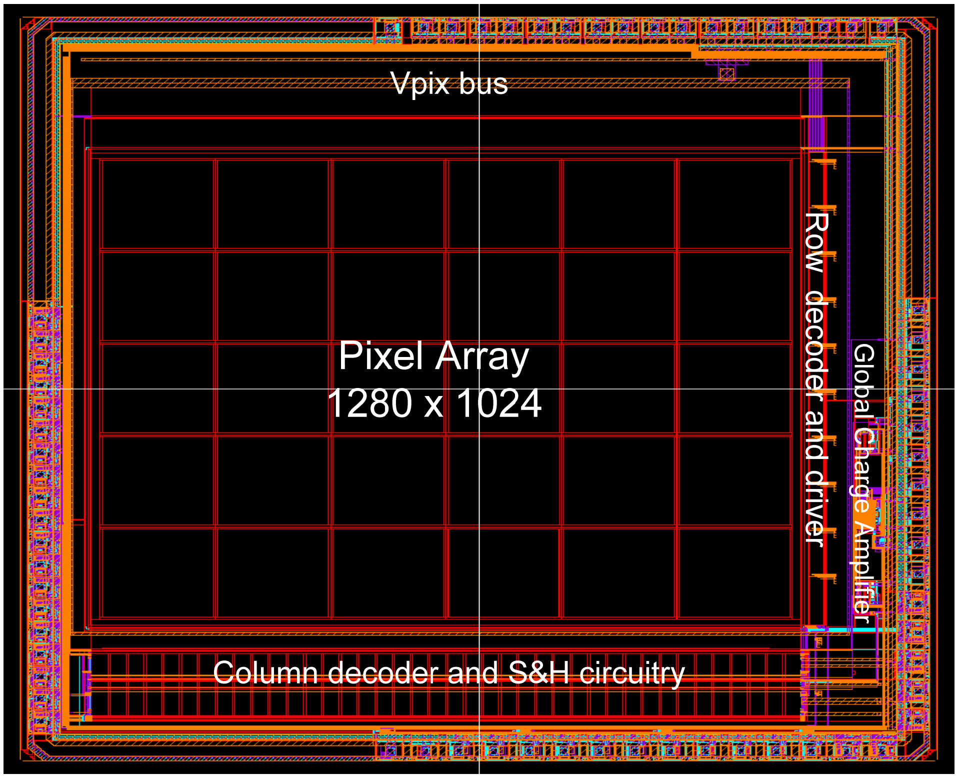


Figure 4.26: Prototype CMOS image sensor layout

As shown in Figure 4.26, the row decoder and driver circuitry are located at the right side of the array; and the column decoder, sample and hold circuitry, and pixel column bias circuitry are at the bottom of the pixel array. The V_{PIX} bus was routed using metal 3 on the top of the pixel array with 50μm wide lines to reduce potential voltage drop. The nonoverlapping clock generator and the global crow-bar charge amplifier with switched-capacitor common mode feedback (SC CMFB) are located on the right side of the chip between the bond pads and the row drivers.

The microphotograph of the prototype chip is shown in Figure 4.27. An 84-pin CLCC (Ceramic Leadless Chip Carrier) package was used with a size of 29*mm* x29*mm*.

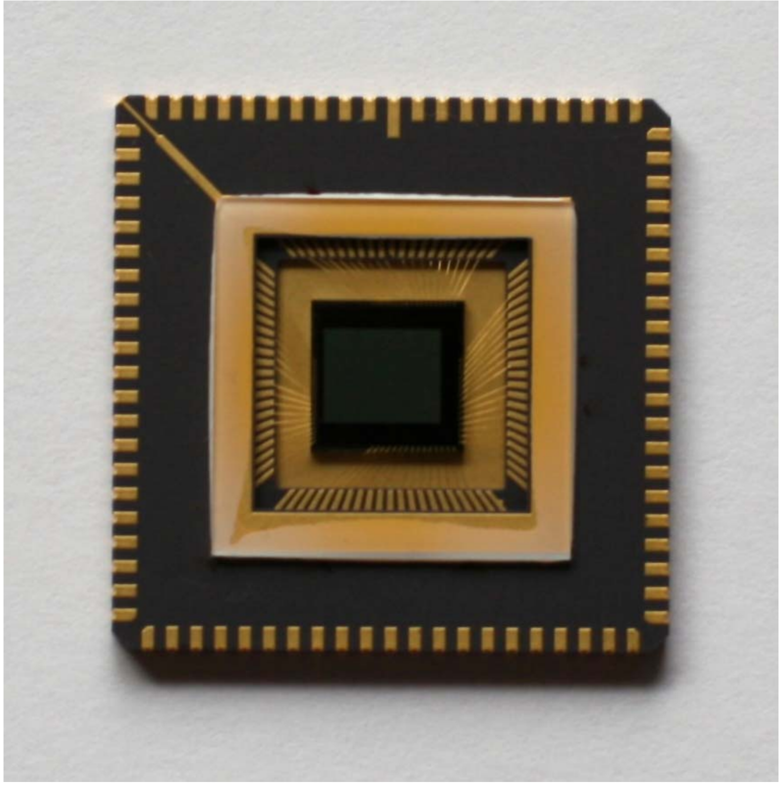


Figure 4.27: Microphotograph of the prototype image sensor

CHAPTER 5 PROTOTYPE SENSOR CHARACTERIZATION

5.1 Characterization Setup

5.1.1 Characterization Hardware

A specially designed test chip setup was used for the chip characterization and image capturing. The setup includes a personality card, a power supply board, a light source driver, a test chip DUT (Device under Test) card, and a set of generic DUT interface cards and cables as shown in Figure 5.1.

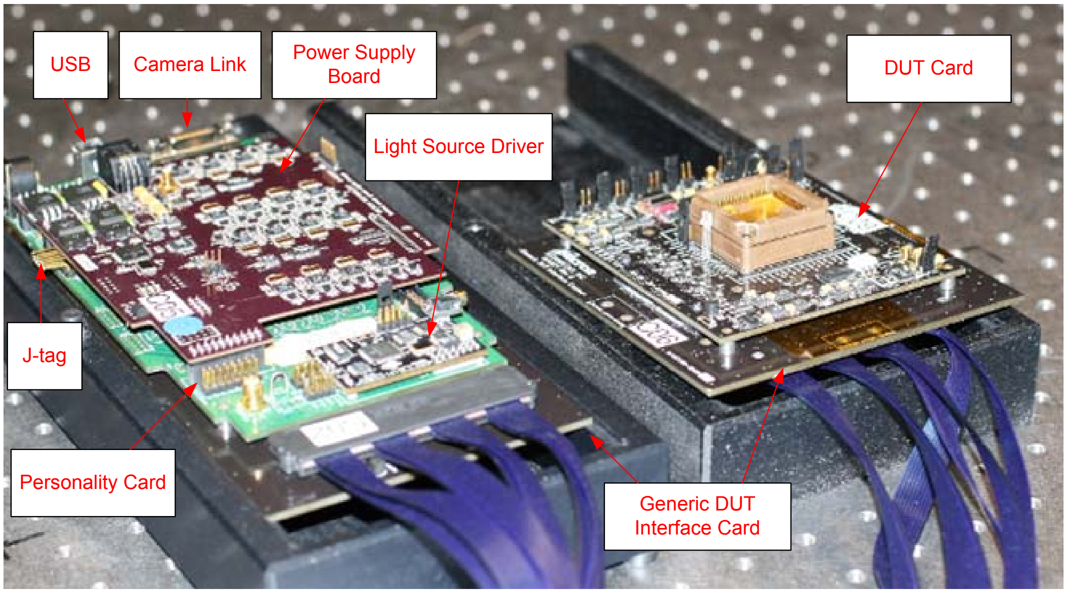


Figure 5.1: Characterization setup

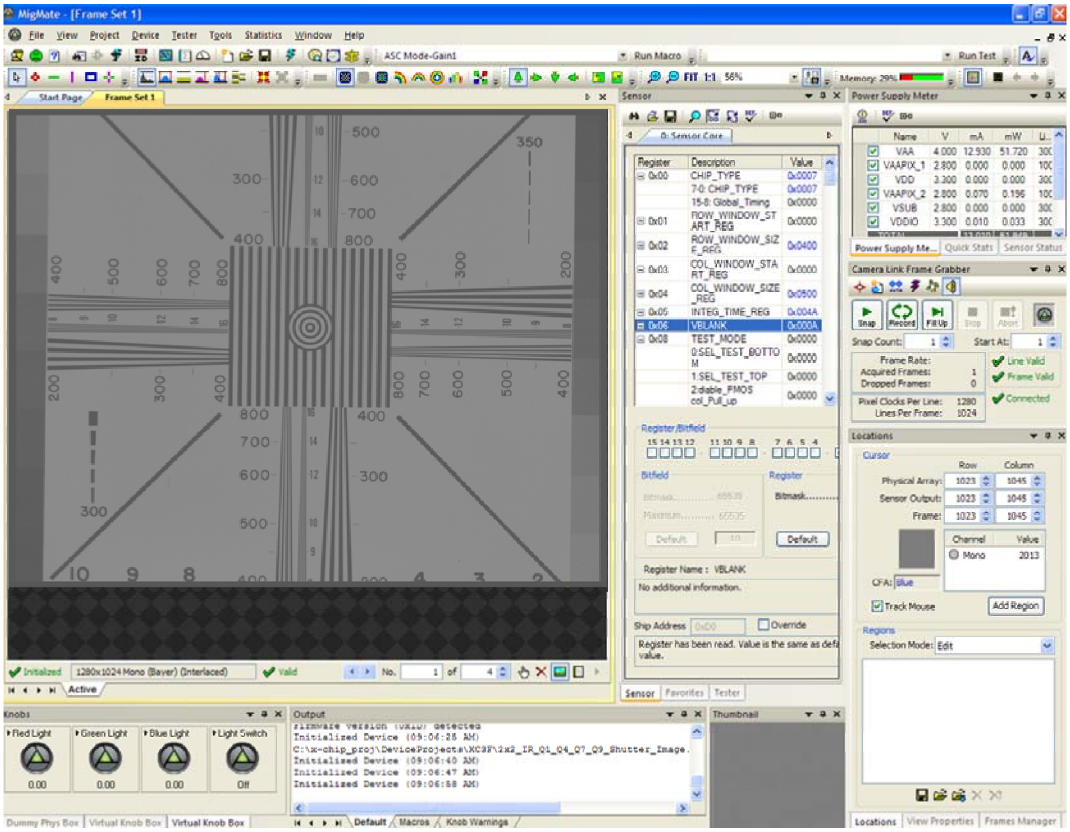
The Personality card consists of a central FGPA device with supporting devices to provide for clock generation, USB interfacing, image buffering, and image data manipulation. The Stratix FPGA device program was written in VERILOG HDL and can be downloaded through a J-tag interface. There are a lot of Inter-Integrated Circuit (I^2C) registers used to control the personality card and the operation of the sensor. The I^2C registers are updated through USB2 interface, and the images are captured through camera link interface. Therefore, a computer equipped with USB2 and camera link interface is required for the sensor control and characterization.

An 8-channel power supply board was designed to interface with the personality card and provide adjustable power supplies with current read back. Each channel of the power supply board can provide 0 to $5V$ output with $80\mu V$ resolution and $15mV$ of accuracy. The light source control board, which is normally soldered on to the personality card, provides control of the external light source. The light source can provide various levels of red, green, and blue light.

The test chip DUT card is equipped with circuitry specifically designed for the test chip. There are 4 banks of digital-to-analog converters (DAC) on the board to allow full control of the voltage levels. A 12-bit ADC was designed on this board to convert the analog signal outputs into digital signals. A set of generic DUT interface (GDI) boards connects the personality card and DUT card.

5.1.2 Characterization Software User Interface

Micron internal software (called MigMate) was used to control the sensor operation, and to collect and analyze image data as shown in Figure 5.2. The captured image is displayed in the main window. The main control window is composed of a lot of frequently used functions such as file operation, zooming, regional image statistics, histogram stretch, color processing, and color plane splitting. The image display window shows the latest captured images.



Register	Description	Value
0x00	CHIP_TYPE	0x0007
	7-0: CHIP_TYPE	0x0007
	15-8: Global_Timing	0x0000
0x01	ROW_WINDOW_START_REG	0x0000
0x02	ROW_WINDOW_SIZE_REG	0x0400
0x03	COL_WINDOW_START_REG	0x0000
0x04	COL_WINDOW_SIZE_REG	0x0500
0x05	INTEG_TIME_REG	0x004A
0x06	VBLANK	0x000A
0x08	TEST_MODE	0x0000
	0:SEL_TEST_BOTTOM	0x0000
	1:SEL_TEST_TOP	0x0000
	2:diable_PMOS col_Pull_up	0x0000

	Name	V	mA	mW
☑	VAA	4.000	12.930	51.720
☑	VAAPIX_1	2.800	0.000	0.000
☑	VDD	3.300	0.000	0.000
☑	VAAPIX_2	2.800	0.070	0.196
☑	VSUB	2.800	0.000	0.000
☑	VDDIO	3.300	0.010	0.033

```
Initialized Device (09:06:25 AM)
C:\x-chip_proj\DeviceProjects\XC3F\2x2_IR_Q1_Q4_Q7_Q9_Shutter_Image.
Initialized Device (09:06:40 AM)
Initialized Device (09:06:47 AM)
Initialized Device (09:06:58 AM)
```

Figure 5.2: Screen shot of characterization user interface

Besides the main control window and the image display window, there are several windows available in the user interface for flexible control. The power supply window is used to set and read the values of the power supplies. The power supply has multiple parameters such as enable state, name, voltage level, current, power consumption, and compliance.

The register reader window is the main interface to the sensor's registers. All registers used to control the prototype sensor operation were divided into three pages. The first page, called the sensor core register page, controls the operation of the prototype image sensor. The second page, called the tester page, controls the operation of the personality card and the DACs on the test chip DUT card. The last page, called the light source control page, is used to control the color and voltage of the LED. The window's data is constantly updated by reading the sensor's registers.

The frame grabber window is used to capture images from the sensor. When the *Snap* image button is hit, the existing image in the current frame set will be replaced by the new captured image. The *Record* images button will begin capturing and displaying images until *Stop* or *Abort* is selected. The locations window displays information about the current pixel under the cursor, regions attached to this frame and averages of the active region. Using the captured images, the software can automatically calculate the statistics based on the region of interest.

5.2 Characterization Methodology

There are two categories of noise source in CMOS image sensor arrays: random temporal noise and fixed pattern noise (FPN). In order to separate the noise into different components, many frames (normally 30 frames) of the image are taken under the same measurement condition. Those data can be expressed by using this notation: $p_n(x, y)$. The x and y are the row and column number of the sensor array. The n is the n^{th} image captured. The relation between x, y, n can be illustrated in Figure 5.3.

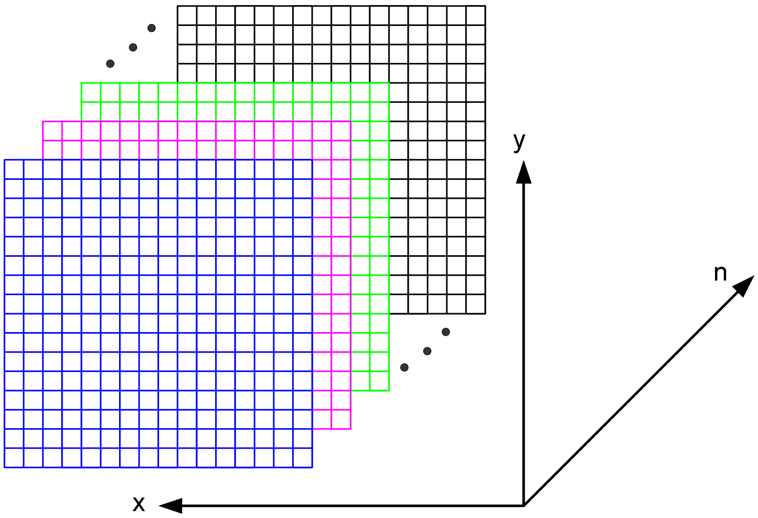


Figure 5.3: Data set to process temporal noise and fixed pattern noise

The mean signal is calculated by:

$$\overline{p} = \frac{1}{XYN} \sum_{n=1}^{N} \sum_{x=0}^{X-1} \sum_{y=0}^{Y-1} p_n(x, y) \tag{5.1}$$

where X, Y and N are the total number of rows, columns, and frames, respectively. The mean signal for each pixel is given by:

$$\overline{p}(x, y) = \frac{1}{N} \sum_{n=1}^{N} p_n(x, y) \tag{5.2}$$

The total noise is calculated by:

$$\sigma_{Total} = \sqrt{\frac{1}{XY(N-1)} \sum_{n=1}^{N} \sum_{x=0}^{X-1} \sum_{y=0}^{Y-1} \left(p_n(x, y) - \overline{p}(x, y)\right)^2} \tag{5.3}$$

while the random temporal noise for each pixel is calculated by:

$$\sigma(x, y) = \sqrt{\frac{1}{(N-1)} \sum_{n=1}^{N} \left(p_n(x, y) - \overline{p}(x, y)\right)^2} \tag{5.4}$$

and the total random temporal noise is given by:

$$\sigma_{Temp} = \frac{1}{XY}\sum_{x=0}^{X-1}\sum_{y=0}^{Y-1}\sigma(x,y) \tag{5.5}$$

The total fixed pattern noise (FPN) is given by:

$$\sigma_{FPN} = \sqrt{\frac{1}{XY}\sum_{x=1}^{X-1}\sum_{y=1}^{Y-1}\left(\overline{p}(x,y)-\overline{p}\right)} \tag{5.6}$$

With the similar methodology, the total temporal noise can be further separated into row temporal noise, column temporal noise, and pixel wise temporal noise. The FPN can be further separated into row wise FPN, column FPN, and pixel wise FPN.

5.3 Pixel Bias Levels

In order to achieve the best pixel performance, the pixel bias levels need to be optimized. All pixel bias levels are summarized in Table 5.1. In order to fully transfer the charge from the photodiode to the floating diffusion node, the V_{TX_HI} was boosted to $4V$. The V_{TX_LO} was set to -0.5V to completely shut down the transfer gate when the transfer gate is off, and thus increase the full well capacity. Under low light conditions, only a small portion of the full well capacity is used, so the V_{TX_LO} needs to be optimized to achieve the best performance of the dark current and hot pixel performance [85].

Table 5.1: Summary table of pixel bias levels

Pixel Bias Levels			
V_{TX_HI}	4V	V_{TX_LO}	-0.5V
V_{RST_HI}	3.8V	V_{RST_LO}	0.5V
V_{ROW_HI}	4V	V_{ROW_LO}	0
V_{DCG_HI}	2.8V	V_{DCG_LO}	0
V_{PIX}	2.8V	Column Bias	5uA

The V_{RST_HI} was boosted to $3.8V$ to reset the floating diffusion node to the same potential as V_{pix}. A $0.5V$ voltage was used for V_{RST_LO} to reduce the reset gate charge injection and increase the pixel output voltage swing [81]. The V_{ROW_HI} was boosted to $4V$ to make the row select transistor working in the linear region, which is very important to reduce the pixel wise FPN. The V_{DCG} signal is used to drive the drain and source terminal of the dual conversion gain transistor. A $2.8V$ bias was used for V_{DCG_HI} to make the dual conversion gain transistor work in the full depletion mode, and $0V$ was used for the low voltage to secure the transistor working in the strong inversion mode.

5.4 Analog Signal Chain Gain Measurement

Analog Signal Chain (ASC) from the floating diffusion node to the output of the external ADC was measured by using a special feature of the test chip DUT card. The gain of the crow-bar amplifier was set to unity. Figure 5.4 shows the readout timing diagram for the analog signal chain measurement.

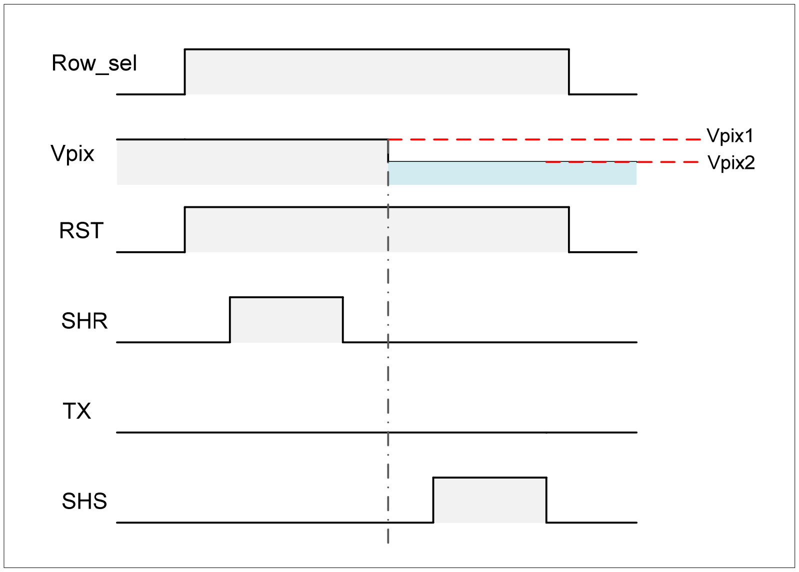


Figure 5.4: Readout timing diagram for the analog signal chain gain measurement [94]

From Figure 5.4, it can be seen that several changes have been made compared to the regular pixel readout timing to measure the gain of the whole analog signal chain. First, the RST gate was kept high (at least one threshold voltage above V_{pix}) during the whole pixel to column readout period; therefore the floating diffusion node will be reset to V_{pix}. The transfer gate pulse (TX) was suppressed in this readout timing, while a V_{pix} switch was introduced between SHR and SHS. During the SHR period, the V_{pix} stays at V_{pix1} and changes to V_{pix2} before the rising edge of the SHS pulse, such that the difference of the V_{pix1} and V_{pix2} was fed into the whole analog signal chain. The measurement result is shown in Figure 5.5. For this measurement, the V_{pix1} was kept at $2.8V$ and V_{pix2} was swept from $2.8V$ to $1.4V$. The gain of the analog signal chain was measured at 0.81 LSB/mV as the slope of the curve shown in Figure 5.5. Also the gain is very linear across a wide voltage range which is very important for the sensor operation. The total analog signal gain includes the gain of the source follower and the gain of crow-bar amplifier.

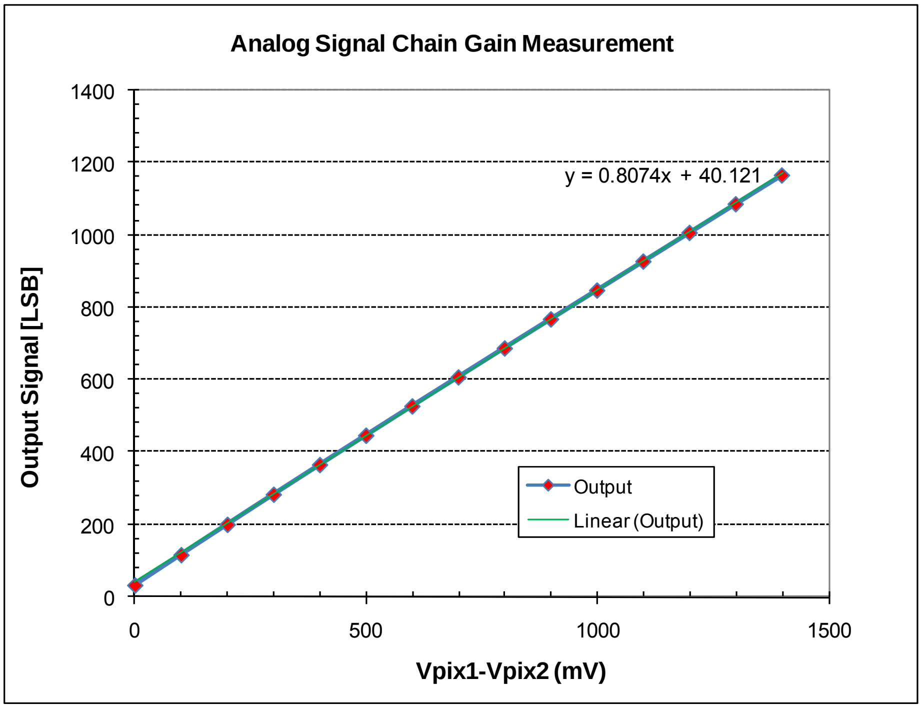


Figure 5.5: Analog signal chain gain measurement result

5.5 Pixel Output Micro-probing Result

A micro-probe of column voltage was performed under different light illumination conditions to secure the pixel operate in the right region. Figure 5.6 and Figure 5.7 show the column micro-probe result under dark condition with low and high conversion gain modes, respectively.

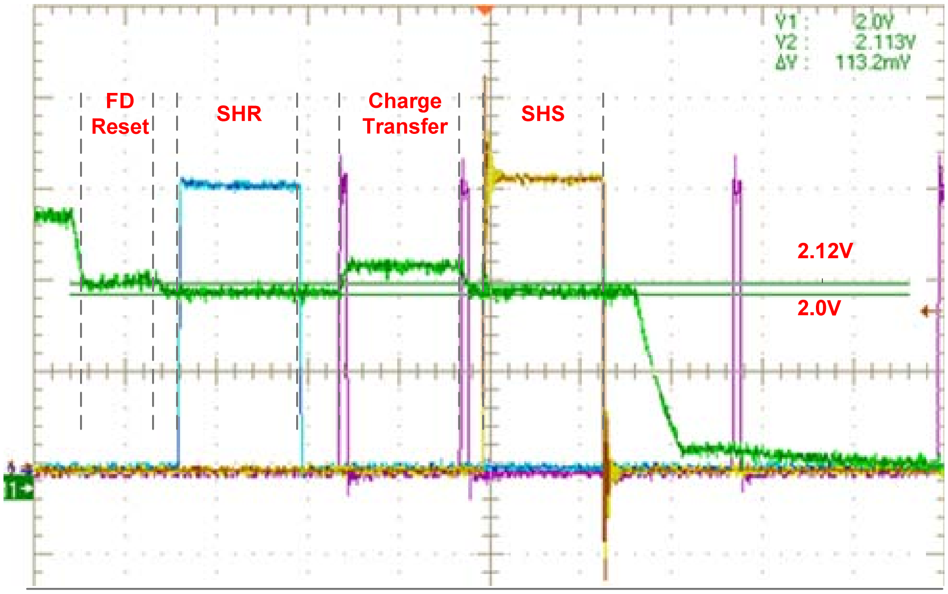


Figure 5.6: Column micro-probe result under dark condition at low conversion gain mode

From Figure 5.6, it can be seen that column is reset to $2.12V$ when the reset gate is on. At the falling edge of the RST signal, a certain portion of the charge under the RST gate is injected into the floating diffusion node, which lowers the potential of the floating diffusion node, and thus the pixel output node. The charge injection was measured at $120mV$ for the low conversion mode. Thereafter, the transfer gate is turned on to transfer the charge from the photodiode to the floating diffusion node. At the rising edge of the TX pulse, some charges are pulled from the floating diffusion node in order to form the channel of the TX gate, which results in a high potential on the floating diffusion node. Then the transfer gate is turned off followed by SHS. Under the dark condition, the pixel output voltage level at end of the SHS period matches very well with voltage level at the end of the SHS period as expected.

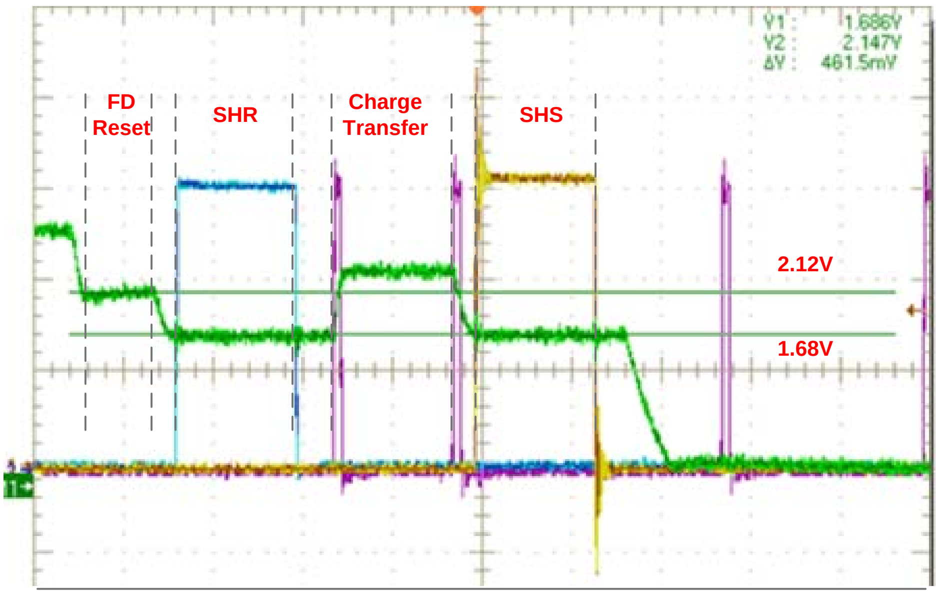


Figure 5.7: Column micro-probe result under dark condition at high conversion gain mode

Since the capacitance of the floating diffusion node is much smaller in the high conversion gain mode compared to the low conversion gain mode, the voltage change is much higher in the high conversion gain mode as shown in Figure 5.7. The charge injection was measured at 440mV at the high conversion gain mode, which leads to 1.68V for the SHR level.

Figure 5.8 and Figure 5.9 show the column micro-probe result under light illumination conditions in the low and high conversion gain mode, respectively. From Figure 5.8, it can be seen that the pixel output stays at the same potential as the dark for the floating diffusion node reset period and the SHS period. After turning on the transfer gate, the charges are transferred from the photodiode to the floating diffusion node, thus lowering the potential of the floating diffusion node and pixel output node. From Figure 5.8, it can also be seen that most of the voltage drop happens after the transfer gate falling edge, which means that a lot of charges are held under the transfer gate when the transfer gate is on. Then the charges flow to the floating diffusion node during the falling edge of the TX pulse.

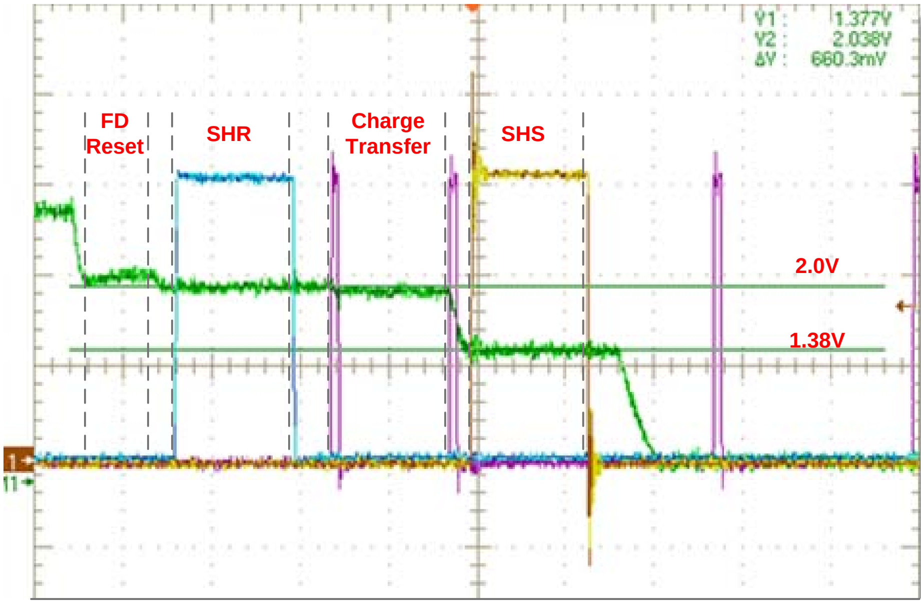


Figure 5.8: Column micro-probe result under light illumination condition at low conversion gain mode

For this light illumination condition, pixel output change during the SHS period is at 600mV for the low conversion gain mode as shown in Figure 5.8. From Figure 5.9, it can be seen that the pixel output during the SHS period goes to 500mV for the high conversion gain mode for this particular light illumination condition.

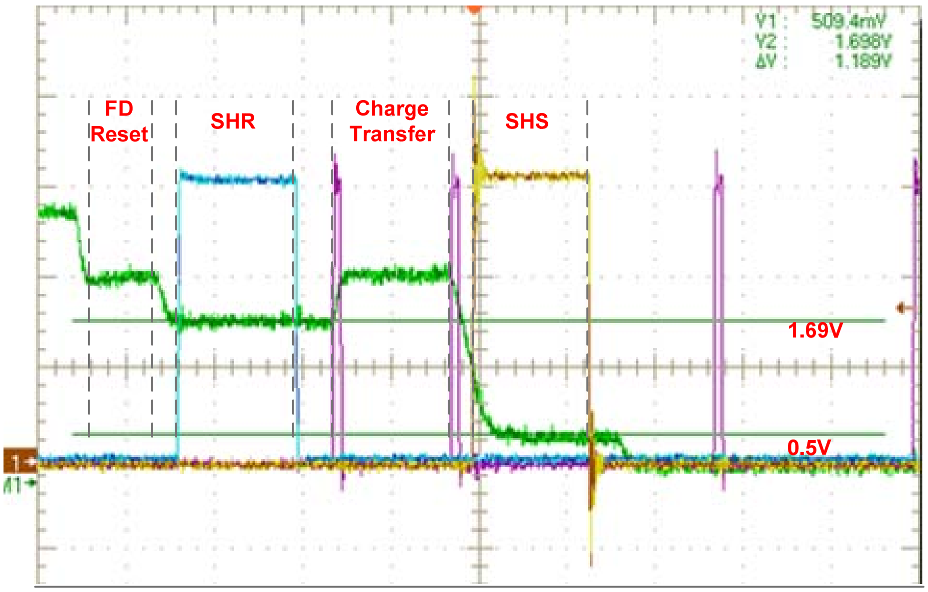


Figure 5.9: Column micro-probe result under light illumination condition at high conversion gain mode

5.6 Light Signal Characterization

Davidson Optronic TVO projector (K-1000) was used for the light signal characterization as shown in Figure 5.10. A green spectral filter with a peak wavelength at ($\lambda_{\max} = 550 \pm 5nm$) and a $40nm$ bandwidth is inserted into the projector. Before doing the experiment, a test pattern slide is inserted into the slot, and the position of projector is adjusted to focus the image on the sensor. When the image of the plate is focused, the light intensity (in “foot-candles”) at the plate location (measured by an intensity detector) is the same as it on the sensor plane. The plate is removed after alignment, and then experiment is performed by varying the exposure.

Exposure is calculated as an illuminance multiplied by an integration time:

$$Exp = I \times C \times t_{\text{int}} \quad [Lux \cdot s] \tag{5.7}$$

where I is the illuminance in foot-candle, C is wavelength dependent illumination conversion factor, (equals to 10.764 for 540nm); and t_{int} is the integration time in second. All light signal measurements were performed by fixing the light intensity and changing the integration time. Signals and noise were calculated in Least Significant Bit (*LSB)* and converted to volts referenced to the floating diffusion node. A neutral density filter was inserted into the projector to achieve low light conditions. At each exposure time, 30 frames were captured to calculate the signal mean and all noise components.

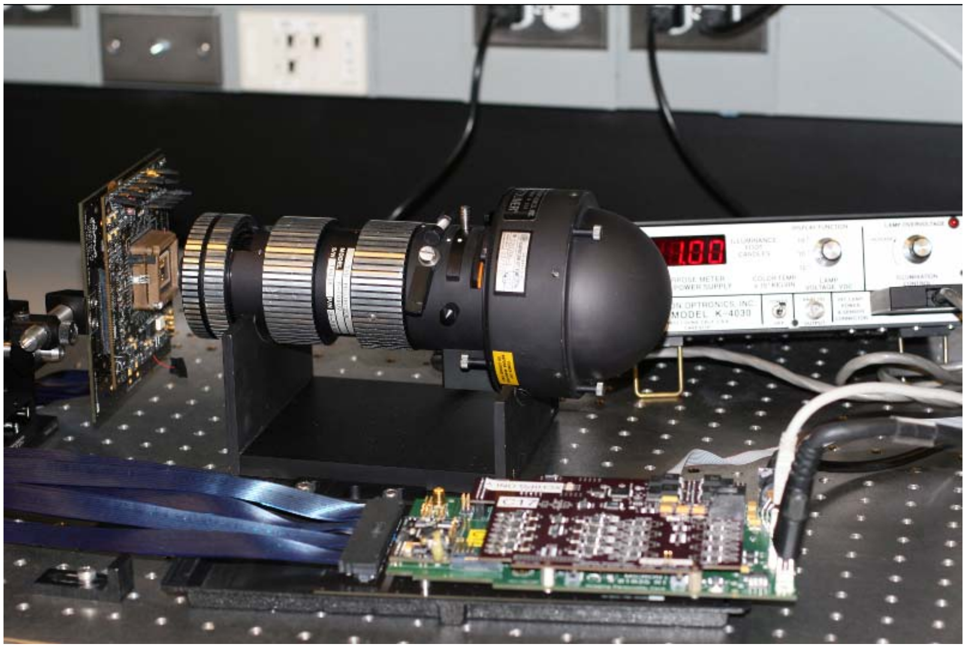


Figure 5.10: Characterization setup for the light signal measurement

5.6.1 Light Signal Characteristics

Figure 5.11 shows the light signal response for both the low and high conversion gain modes. The x-axis is the exposure and the y-axis is the floating diffusion node signal in mV. The voltage swing on the floating diffusion node is about $1600mV$ for the low conversion gain mode, which is limited by the photodiode full well capacity. About

$1800mV$ of the floating diffusion node voltage swing is achieved for the high conversion gain mode, which is limited by the column voltage swing. Normally the pixel only works in the linear region, which means that the signal will be clipped once it exceeds the maximum linear range.

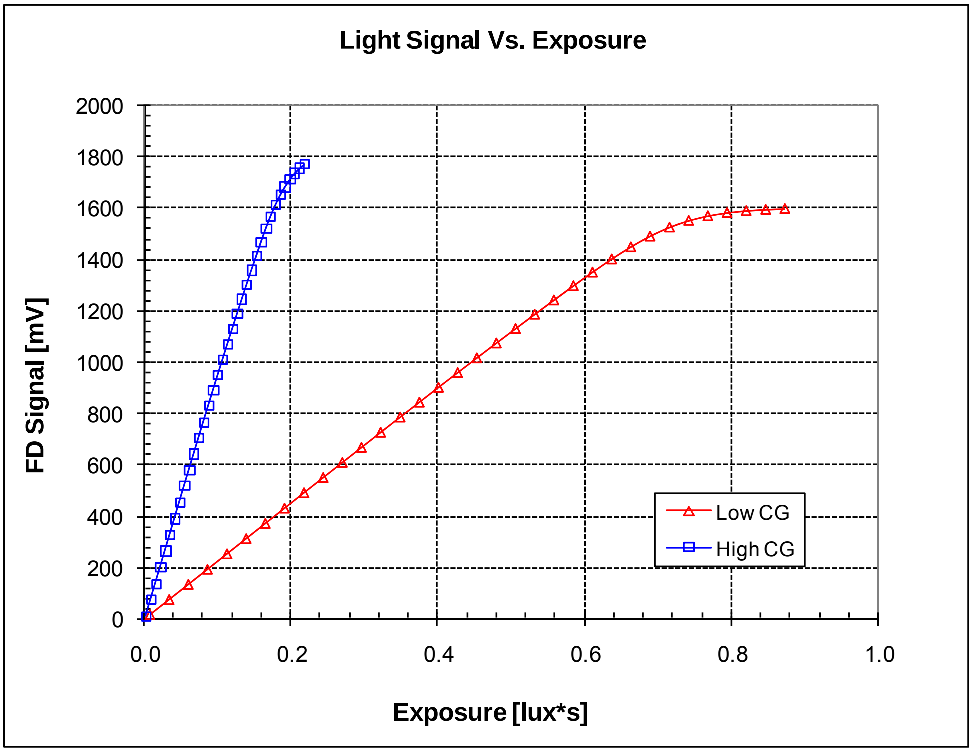


Figure 5.11: Light signal measurement for both low and high conversion gain mode

5.6.2 Pixel Responsivity

The pixel responsivity is defined at the slope of light signal curve and the local responsivity is given by:

$$R_{local} = \frac{\Delta S}{\Delta Exp} \tag{5.8}$$

where S is the mean signal at each exposure level and Exp is the exposure in $[Lux \cdot s]$. The unit of pixel responsivity is "*V(/lux*sec)*". The local responsivity is basically the local derivative of the signal vs. exposure curve as shown in Figure 5.11. At exposure levels less than $Exp_{\max}$ (e.g. within linear pixel capacity), the mean value of local responsivity is defined as pixel responsivity (R_{mean}). The pixel responsivity vs. exposure curve for the low conversion gain mode is shown in Figure 5.12.

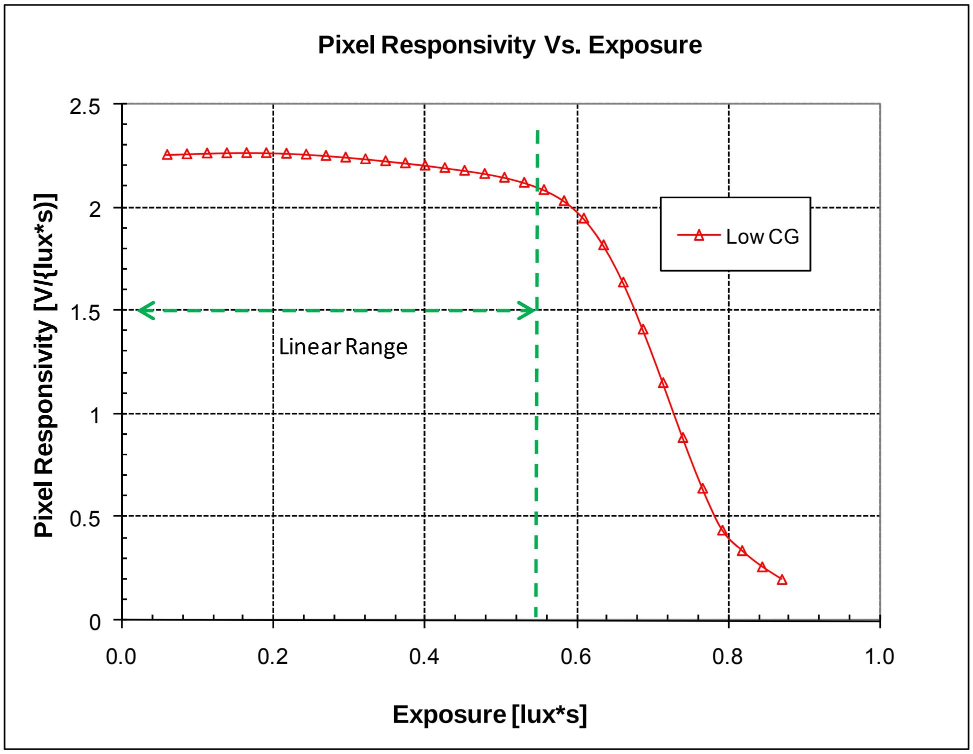


Figure 5.12: Pixel responsivity measurement for the low conversion gain mode

From Figure 5.12, it can be seen that the average pixel responsivity for the low conversion gain mode is about 2.2 *V/(lux*sec)*. The responsivity is linear before the pixel reaches the saturation region and it starts to fall off after that. The pixel output level is normally clipped by the clamp circuitry once the pixel passes the maximum linear range.

The pixel responsivity vs. exposure curve for the high conversion gain mode is plotted in Figure 5.13. The average responsivity increases to 9 *V/(lux*sec)* when the pixel operation is switched to the high conversion gain mode. The linearity of the responsivity at the high conversion gain mode is slightly worse than that of the low conversion gain mode because of the nonlinearity of the junction capacitance of the floating diffusion node, but it is still in an acceptable range.

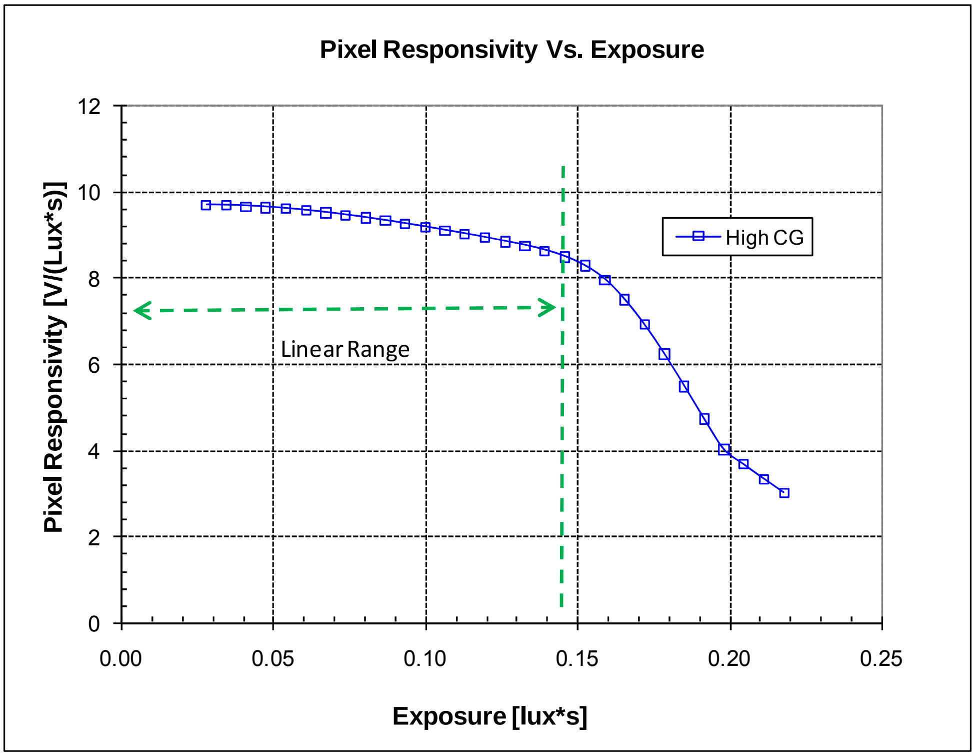


Figure 5.13: Pixel responsivity measurement for the high conversion gain mode

<u>5.6.3 Conversion Gain Measurement</u>

The relationship between the signal charge and the signal voltage at the floating diffusion node is given by:

$$V_{FD} = CG \cdot N \tag{5.9}$$

where *CG* is the conversion gain in the unit of "$\mu V/e$". When the temporal noise is dominated by the photon shot noise, the photon shot noise voltage is given by:

$$\overline{v^2_{shot-photon}} = CG^2 \cdot N \tag{5.10}$$

By using the above two equations, the conversion gain can be calculated as:

$$CG = \frac{\overline{v^2_{shot-photon}}}{V_{FD}} \tag{5.11}$$

The conversion gain measurement results for both the low and high conversion gain modes are shown in Figure 5.14. The x-axis is the signal voltage of the floating diffusion node while the y-axis is the photon shot noise voltage square. The slope of the curve at different exposure levels measures the conversion gain. A 127 $\mu V/e$ was achieved for the high conversion gain mode and 30.8$\mu V/e$ was measured for the low conversion gain mode. The conversion gain ratio is about 4.1, which corresponds to the responsivity ratio.

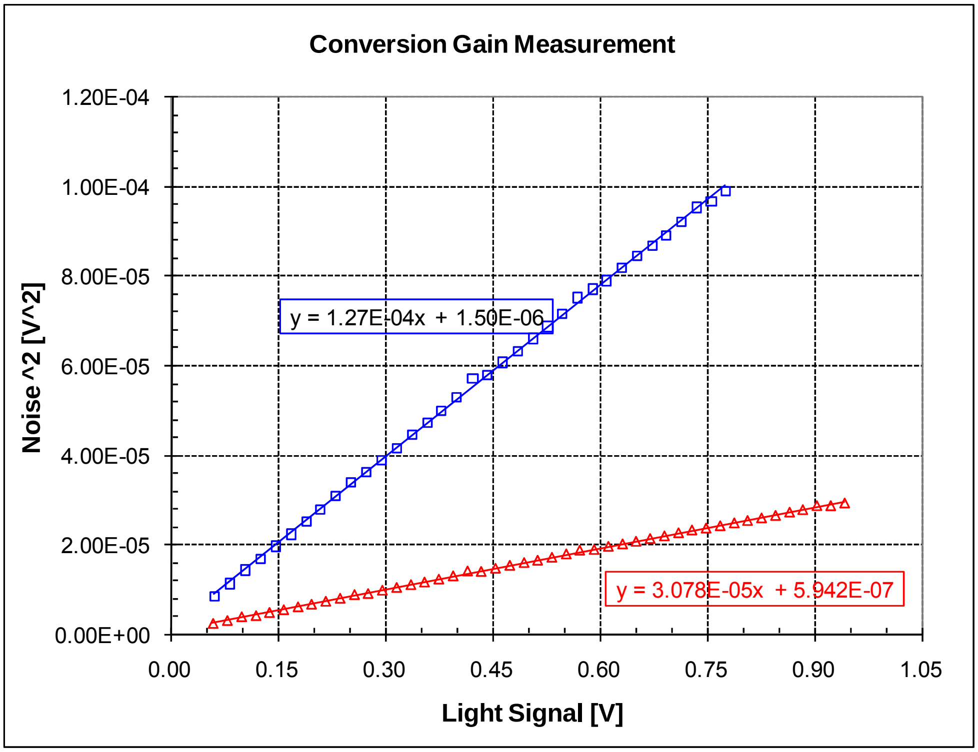


Figure 5.14: Conversion gain measurement for both low and high conversion gain modes

5.6.4 Pixel Full Well Capacity Measurement

The square of signal-to-noise ratio (SNR) for the photon shot noise is calculated as:

$$SNR^2 = \frac{(V_{sig} - V_{offset})^2}{v_{shot-photon}^2} \tag{5.12}$$

where the SNR^2 has the unit of "electrons" . The exposures vs. SNR^2 curves for both the low and higher conversion gain modes are plotted in Figure 5.15 and Figure 5.16, respectively. For the linear region of the curve, a linear fit equation can be derived as:

$$SNR^2 = a \cdot Exp + b \tag{5.13}$$

where a and b are the linear fit coefficients. By plotting the temporal noise vs. exposure curve, the expose level (Exp_{max}) corresponding to the maximum temporal noise can be found. The linear pixel capacity can be calculated as:

$$FW_{linear} = a \cdot Exp_{\max} + b \tag{5.14}$$

The linear pixel full well capacity is in the unit of electrons. From Figure 5.15, it can be seen that a 42*ke* linear full well was achieved for the low conversion gain mode, and a 10.5*ke* linear full well was measured for the high conversion gain mode as shown in Figure 5.16.

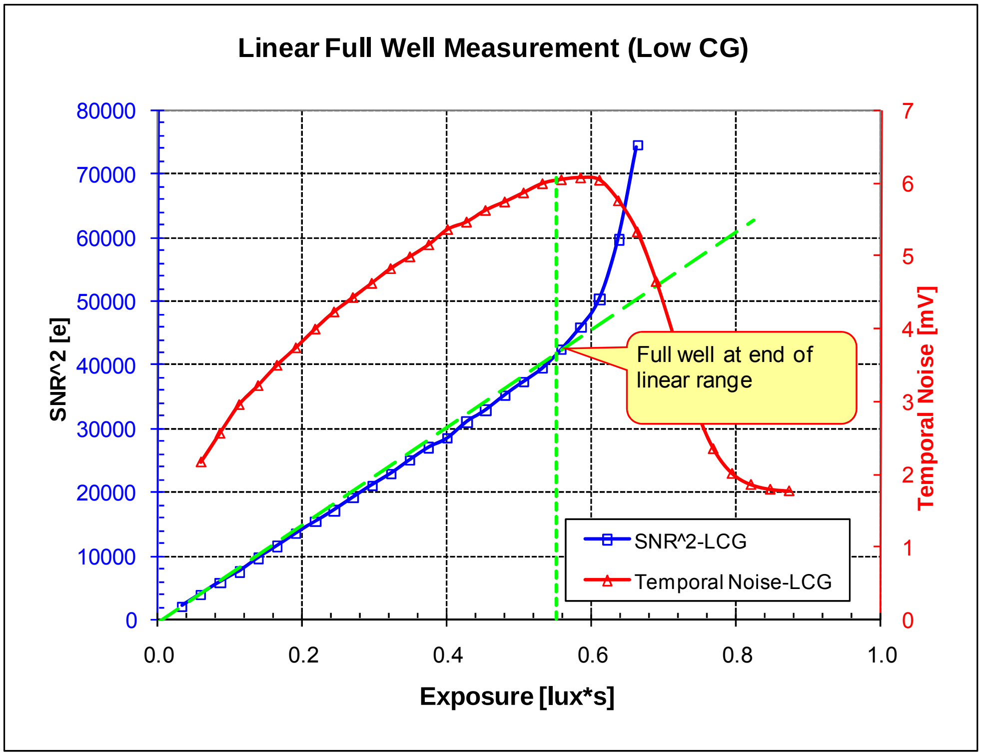


Figure 5.15: Pixel full well measurement at low conversion gain mode

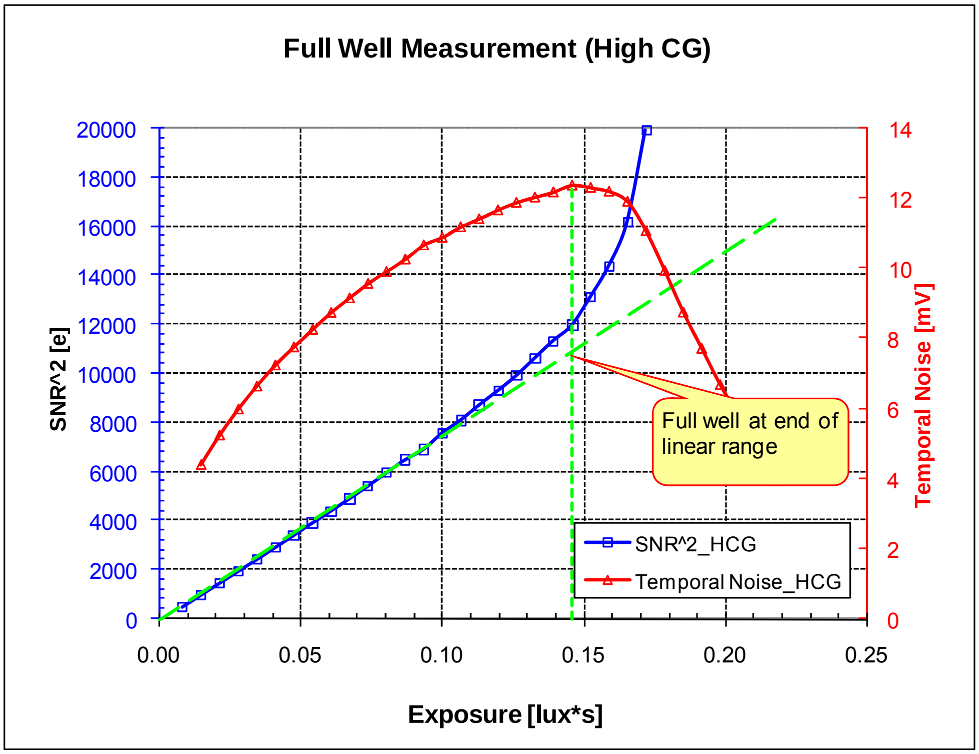


Figure 5.16: Pixel full well measurement at high conversion gain mode

5.6.5 Signal to Noise Ratio (SNR)

The signal to temporal noise ratio for both the low and high conversion modes is plotted in Figure 5.17. It can be seen that a maximum SNR for the low conversion gain mode was measured at 40.2*dB* and the maximum SNR was increased to 46.2*dB* for the low conversion gain mode, which is beneficial for bright light imaging. Under normal light illumination conditions, the photon shot noise dominates, so the SNR increases 10*dB* per decade. The readout noise starts to dominate under very low light illumination conditions; the SNR starts falling off much earlier for the low conversion gain mode, and the high conversion gain starts showing the higher SNR advantage under the low light conditions as shown in Figure 5.17.

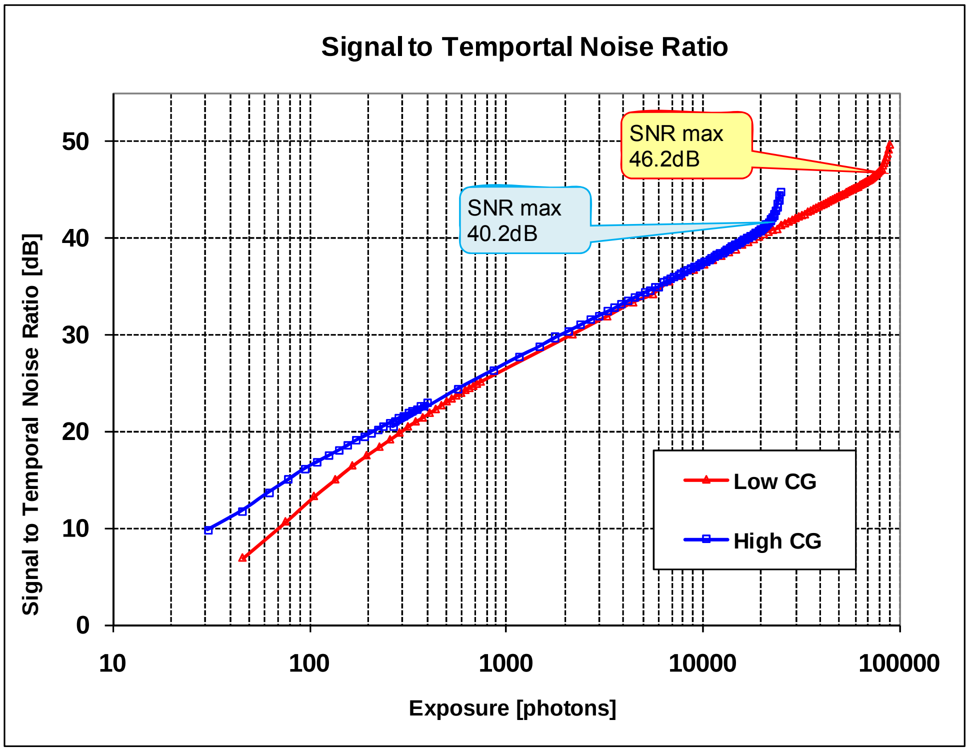


Figure 5.17: Signal to temporal noise ratio measurement result for both low and high conversion gain modes

5.6.6 Photo Response Non-Uniformity

The pixel wise FPN in percentage of the signal for both the low and high conversion gain modes is plotted in Figure 5.18. The photo response non-uniformity (PRNU) is calculated as the pixel wise FPN at the signal equivalent to 50% of the saturation. The PRNU was measured as 0.64% for the low conversion gain mode and 0.73% for the high conversion gain mode. Both values are pretty good. The slightly higher pixel wise FPN of the high conversion mode may caused by large variant of the parasitic capacitance of the floating diffusion node.

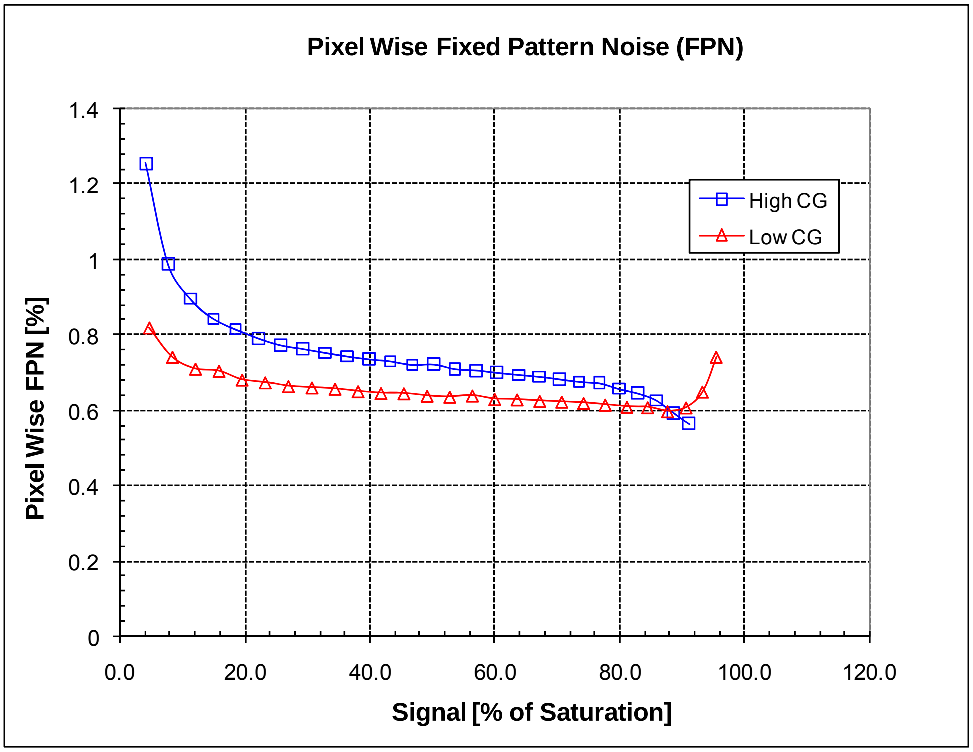


Figure 5.18: Pixel wise fixed pattern noise (FPN) measurement

5.6.7 Readout Noise Measurement

The readout noise is measured as the average temporal noise across the array when the array is isolated from light. The readout noise is measured in *LSB* on the sensor output and is recalculated and reported in equivalent electrons. Maximum analog gain was used for the readout noise measurement. 10 sensors were measured for the readout noise as shown in Figure 5.19. The average readout noise was measured at 8.6 electrons for the low conversion gain mode, and it was reduced to 2.1 electrons for the high conversion gain mode. The lower readout noise of the high conversion mode will benefit the low light imaging for the sensor.

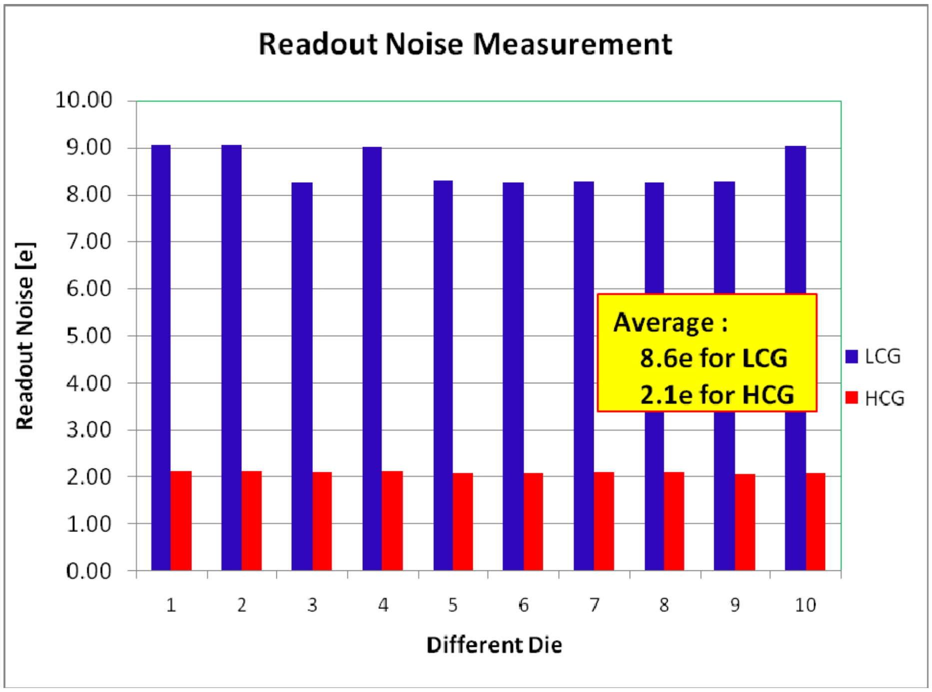


Figure 5.19: Variability chart of the readout noise measurement for both low and high conversion gain modes

5.6.8 Photon Transfer Curves

Figure 5.20 shows the photon transfer curves for the low conversion gain mode. Both temporal noise and FPN components are measured in *LSB* and recalculated for the equivalent electrons. The signal, temporal noise, and FPN in electrons are plotted as a function of exposure photons in the photon transfer curve. Both x-axis and y-axis are in log scale. Since human eyes can easily pick up the FPN when the signal is low, from Figure 5.20, it can be seen that the pixel temporal noise is much higher than the FPN component at low light. The FPN exceeds the pixel temporal noise (or photon shot noise) under middle to high light conditions, but the signal is much higher at the same time and high FPN is not visible. From Figure 5.20, it can also be seen that the pixel temporal noise starts to flatten out at very low exposure, which means that the readout of the pixel starts to dominate.

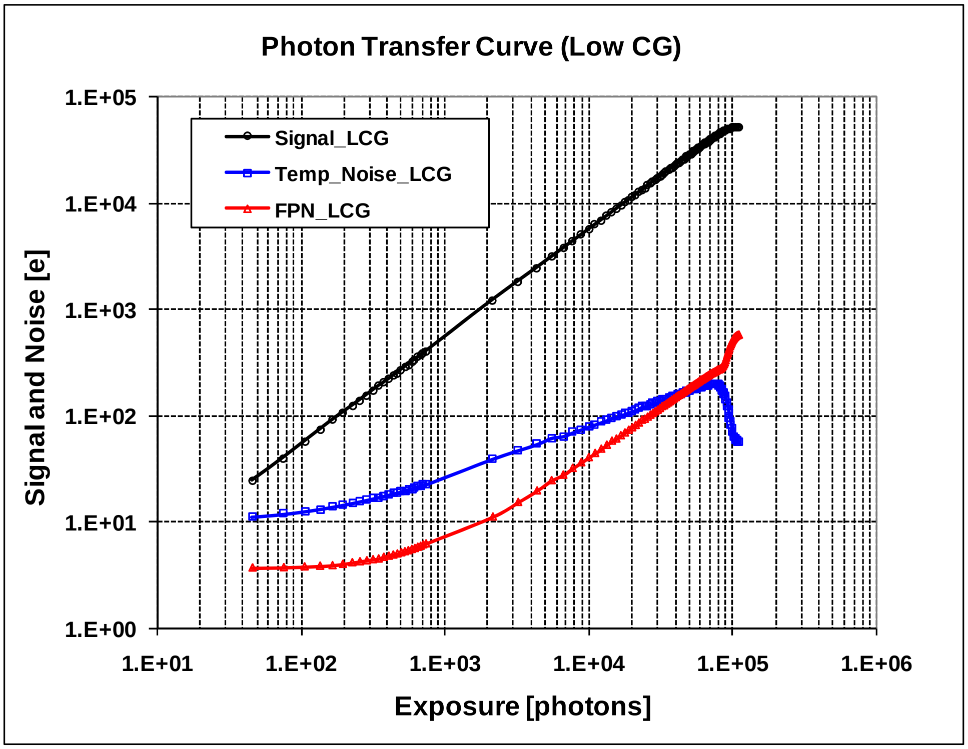


Figure 5.20: Photon transfer curve for the low conversion mode

The photon transfer curves for the high conversion gain mode are shown in Figure 5.21. It can be seen that the FPN is much lower than the pixel temporal across the whole signal range and the FPN will not be visible at all. The photon transfer curve is also a very good measurement of the charge transfer efficiency. If there is some charge transfer issue, the FPN will be much higher and even higher than the pixel temporal noise, and then the FPN will be visible to the human eye.

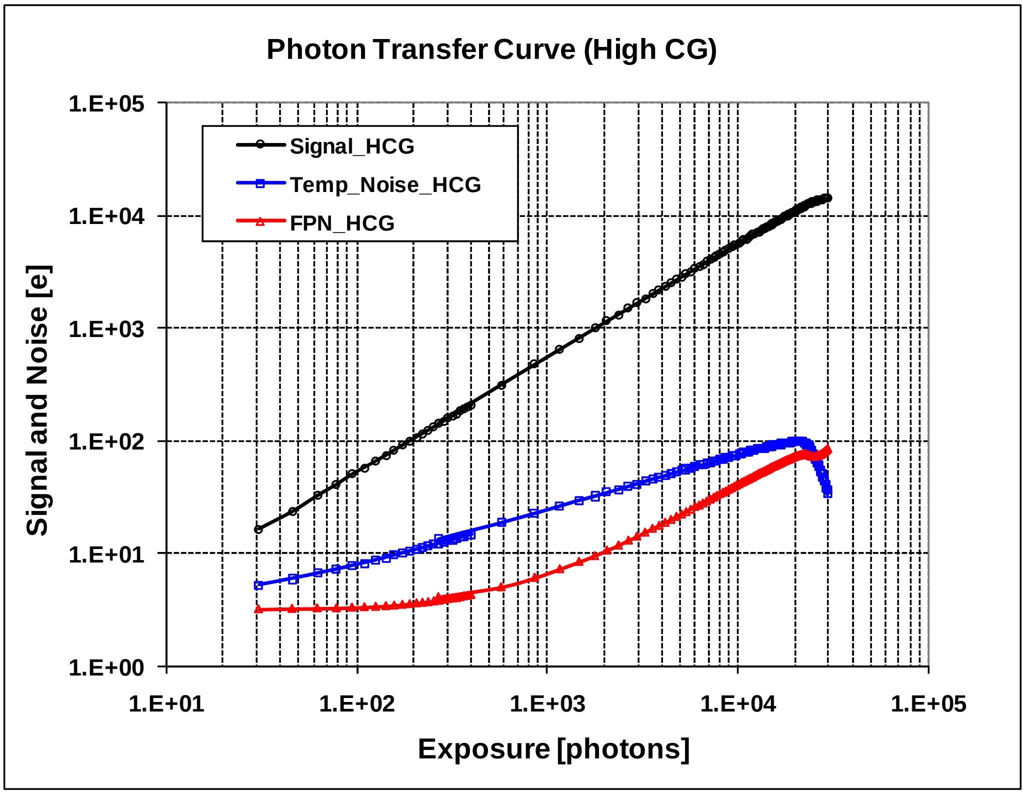


Figure 5.21: Photon transfer curve for the high conversion mode

5.6.9 Sensor Dynamic Range

The dynamic range is the ratio between the full well capacity and the noise floor. For the low conversion gain mode, a 42*ke* of linear full well was achieved and the readout noise floor was 8.6 electrons, which gives a 73.8*dB* dynamic range. For the high conversion gain mode, the full well capacity was measured at 10.5*ke* and 2.1 electrons for the read noise floor, which gives a 73.9*dB* dynamic range. Therefore, an 86*dB* dynamic range was achieved for the whole sensor by combining the two modes of operation. For either mode, the sensor is still working in the linear range, which is essential for the color process.

5.7 Dark Current and Hot Pixel Characterization

The dark current is the leakage current at the photodiode node. The current discharges the pixel capacitance even though there is no light over the pixel [82]. The dark current limits the sensor low light performance especially at high temperature. For the current and hot pixel test, the sensor array is isolated from light. A Temptronic thermal stream TP4100 was used to control the sensor temperature. Dark signal is measured at different integration times and increases linearly with the integration time. The dark current is calculated by finding the slope of the dark signal between the long and short integration times. The dark current has a unit of "*e/s*" per each pixel or "*pA/cm*^{2}". Figure 5.22 shows the dark signal and dark current measurement results at 65°*C*.

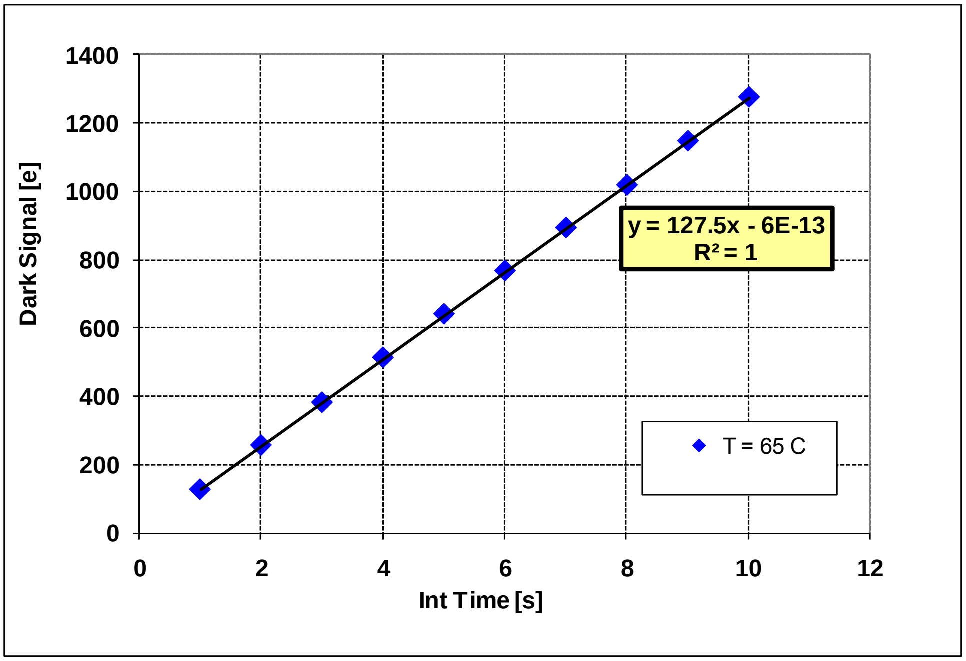


Figure 5.22: Dark current measurement result at 65°C

From Figure 5.22, it can be seen that the average dark current across the whole array was measured at 127.5*e/s* per pixel at 65°C, which corresponds to 65*pA/cm*^{2} for a 5.6µm by 5.6µm pixel area. The dark current histogram and cumulative histogram for each pixel are shown in Figure 5.23. The x-axis is the dark current in the unit of "*e/s*" while the y-axis is the percentage of the occurrence normalized to the peak of the distribution. The dark current histogram is not a Gaussian distribution, and it has a long tale as shown in Figure 5.23. Pixels have extremely high dark current are called hot pixels (or white defects).

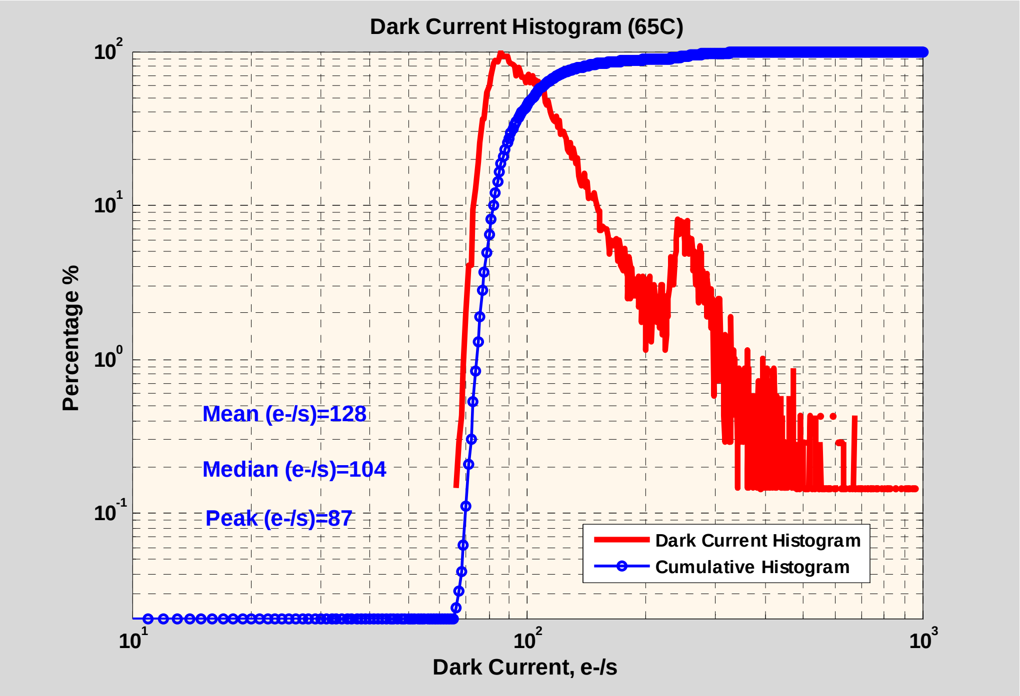


Figure 5.23: Dark current histogram and cumulative histogram at 65°C

The dark current histogram shows a second peak at 250 *e/s*, which may be caused by some contaminations during the fabrication process. It is very important to lower the dark current and hot pixel defects in the image sensor by optimizing the fabrication process.

The dark current measurements were performed at different temperatures. The mean dark current values in the unit of "*e/s*" per pixel and "*pA/cm*^{2}" at different temperatures are summarized in Table 5.2. Even though the dark current doesn't depend on the mode of the conversion gain, all dark current measurements were performed at the high conversion gain mode to take advantage of the lower readout noise benefit.

Table 5.2: Dark current vs. temperature summary table

T [C]	T [K]	1/kT [eV^{-1}]	Mean I_{dark} [e/s]	Mean I_{dark} [pA/cm^2]
55	328.15	35.36	54.35	27.73
65	338.15	34.32	127.50	65.05
75	348.15	33.33	350.61	178.89
85	358.15	32.40	934.11	476.59
95	368.15	31.52	2510.42	1280.83
105	378.15	30.69	6284.78	3206.52

The average dark current measured at different temperatures can be used to calculate the activation energy. The activation energy of the pixel was measured at 1.03*eV* as shown in Figure 5.24. The measured activation energy is very close to the band gap energy of silicon (1.12 *eV*), which means that the diffusion current is the dominant source. The activation energy measurement results give a good sense of the generation of the dark current and hot pixel defect. When the activation energy is measured close to the half band gap of the silicon, it means that the generation current dominates.

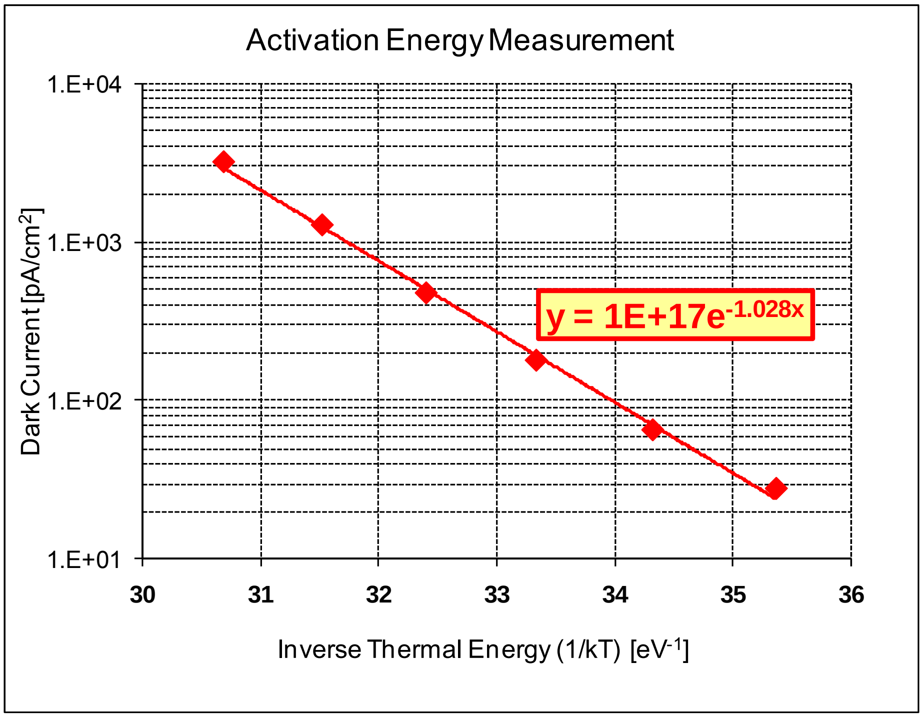


Figure 5.24: Activation energy measurement result

5.8 Spectral Quantum Efficiency and Crosstalk Measurement

An image sensor is basically a monochrome sensor responding to light energies that are within its sensitive wavelength range. Thus, a method for separating colors must be implemented in an image sensor to reproduce an image of a color scene [8]. The most commonly used primary color filter pattern is the “Bayer” pattern, Proposed by B. E. Bayer [95]. The Bayer pattern configuration has twice as many green filters as blue or red filters. This is because the human visual system derives image details primarily from the green portion of the spectrum [8].

For the sensor with a color filter array (CFA), it is very important to measure the quantum efficiency at different wavelengths for color reproduction. The setup used for the spectral measurement is composed of an Oriel 257 monochromator with integrating sphere, an Ocean Optics HR4000 high resolution spectrometer, and an Oriel 71580 calibrated sensor with a Keithley 6517A electrometer as shown in Figure 5.25.

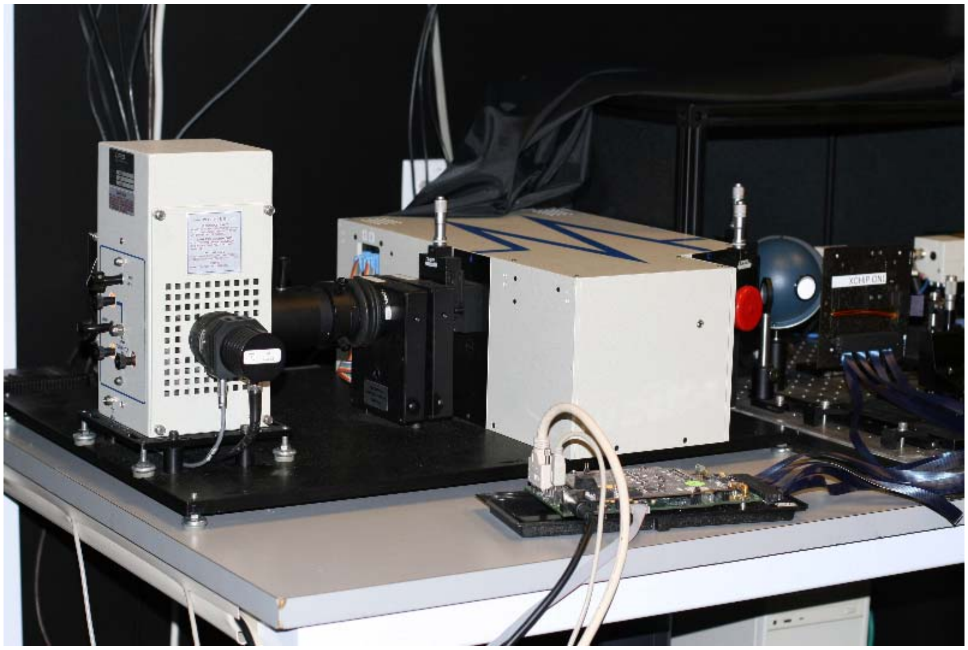


Figure 5.25: Characterization setup for the spectral measurement

The bandwidth of the monochromator was set to 15nm. For each particular wavelength two data points were measured: one with light ON and the other with light OFF for dark reference. All data points were averaged through 30 frames. Before any spectral measurement, an Oriel 71580 calibrated photodiode was placed at a 3" distance from the integrating sphere. The calibrated photodiode was used to measure the irradiance at each wavelength. For monochrome light, the number of incident photons is given by [8]:

$$N_{photon} = \frac{\lambda}{hc} \cdot P \cdot A_{pix} \cdot t_{INT} \tag{5.15}$$

where P is the face-plate irradiance in W/cm^2, A_{pix} the pixel area in cm^2, and t_{INT} the integration time in seconds.

Thereafter, the image sensor was placed at the same position as the calibration diode. With known pixel area and integration time, the number of photons for each pixel at different wavelength was calculated. Then the quantum efficiency was measured as the ratio of number of photo generated electrons to the number of incident photons. The results of the spectral quantum efficiency for different color channels are shown in Figure 5.26.

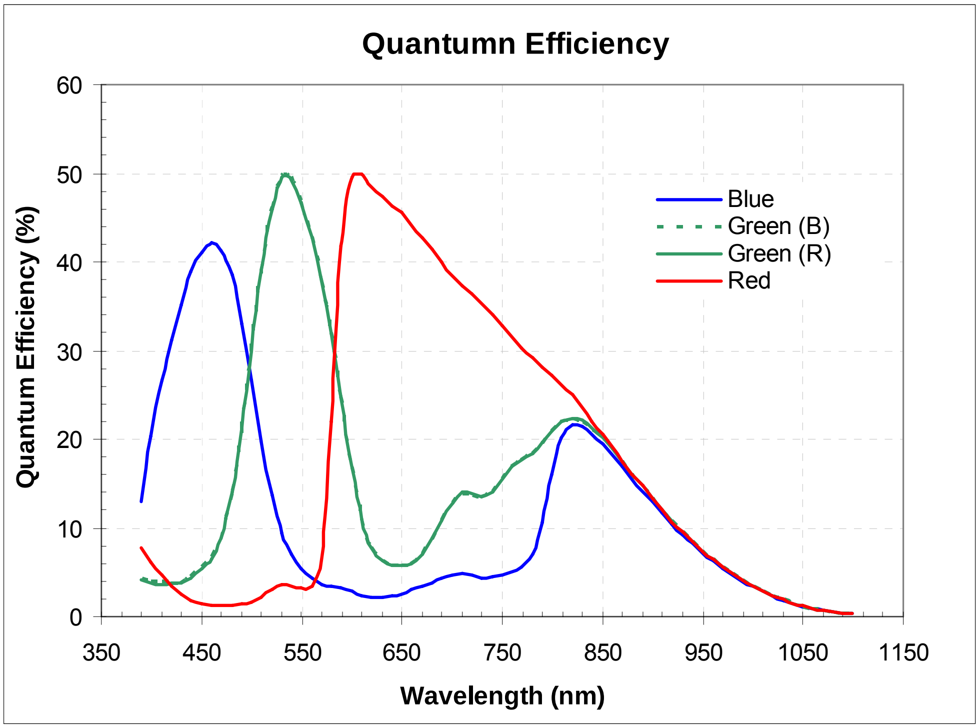


Figure 5.26: Quantum efficiency measurement at different wavelengths

In Figure 5.26, it can be seen that there are two green channels plotted. The green pixel on the same row with blue pixel is called Green (B), and the green pixel on the same row with red pixel is called Green(R). From Figure 5.26, it can be seen that about

48.8% of maximum quantum efficiency was achieved for both green and red pixels at 530nm and 620nm wavelength, respectively. The maximum blue quantum efficiency is about 41.2% at 460nm wavelength. The detail information of the spectral quantum efficiency is summarized in Table 5.3.

Table 5.3: Summary table of the quantum efficiency

	QE @ max %	Max wavelength nm	Relative QE
Blue	41.2	460.0	0.849
Green(B)	48.8	530.0	1.006
Green (R)	48.5	530.0	1.000
Red	48.8	620.0	1.005

Another very important parameter related to spectral response is crosstalk. The crosstalk is directly calculated from the spectral response curve. The integral of the green quantum efficiency from 425nm to 485nm over the blue quantum efficiency under the same wavelength is defined as the blue to green crosstalk. The green band is defined from 515nm to 575nm and 595nm to 655nm for the red band. All crosstalk components for the prototype sensor are summarized in Table 5.4. The average of the green crosstalk is used to calculate the average crosstalk number. About 11.16% of the average crosstalk was achieved as shown in Table 5.4.

The cross-talk degrades the spatial resolution, reduces overall sensitivity, causes color mixing, and leads to image noise after color correction [96] .The crosstalk can be categorized into 3 components: spectral crosstalk, optical spatial crosstalk, and electrical crosstalk [97]. The spectral crosstalk is the component due to imperfect color filters passing through some amount of unwanted light of the other colors. The main reason for the optical component of the crosstalk is that the color filters are located at some distance from the pixel surface due to the metal and insulation layer. The light coming at angles other than the orthogonal can be partially absorbed by the adjacent pixel rather than the one below [97]. The optical crosstalk component can be reduced by optimizing the microlens process [98]. Also a light guide process was reported to reduce the optical cross-talk component significantly [96].

Table 5.4: Summary table of the crosstalk

Color cross-talk (%)	/ Blue 425-485 nm	/ Green 515-575 nm	/ Red 595-655 nm	Average cross-talk (%)
Blue		15.3	4.7	**11.16**
Green (B)	17.4		17.9	
Green (R)	17.1		17.8	
Red	3.8	8.2		

Regarding the electric component, the signal charge generated deep in the photo-conversion area by long wavelength light may diffuse into neighboring pixels. The electrical crosstalk can be reduced by switching to positive biased N-type substrate from P-type substrate and separating different photodiode by deep P-type implant [8].

5.9 Pictures Taken by the Prototype Sensor

Several prototype images were taken to compare the performance of the high and low conversion gain modes at different illumination levels. A Nativa C-mount lens with a 12mm focal distance was mounted onto the DUT card for image capturing. The f-number of the lens was set to 2.8. All images were taken of a Gretagmacbeth color checker chart inside a GTI light box, at a color temperature of 6500K. The light level of the light box was adjusted to about 1000 Lux. Various illumination levels were achieved by inserting different Neutral Density (ND) filters in front of the lens.

Even though, the test chip is running relatively slowly, and 30 frame per second (FPS) cannot be achieved with full resolution. The integration time was adjusted to equal to or less than 33*ms* for the highlight image capturing, which corresponds to 30 FPS frame rate. Under low light conditions, the integration time was increased to 200*ms*, which corresponds to 5FPS frame rate.

After the raw images were captured, the dark image offset was subtracted out from the raw image. Since only a unity gain and 2 times global analog gain are available on the prototype sensor, different digital gains were applied to the different color channels for white balance such that all grey patches have similar red, green and blue signals. Then the images were converted to the RGB color space followed by applying a color correction matrix (CCM) for color reproduction. In order to get the original image performance, there is no row wise or column wise correction applied to the images. Also no noise reduction filter or gamma corrections were applied to the image. All images only run through a very simple color process, so the quality of the image really represents the actual pixel performance. The image quality can be much improved by using more sophisticated color processing pipeline and noise filtering algorithm.

Figure 5.27 shows the image taken by the prototype sensor under 1000lux at the low conversion gain mode. The integration time was adjusted such that the whitest patch (most left bottom patch) was not saturated. The image looks very clean and no visible noise can be seen even on the darkest patch (most right bottom patch).

Figure 5.27 Low conversion gain image taken under 1000 Lux illumination with 30FPS

If the high conversion gain mode was turned on under bright light condition, 4 times less integration time has to be used to avoid the saturation of the bright patch, which may not degrade the image quality too much for the bright region, but the dark region image will be degraded slightly. However, the lower noise of the high conversion gain mode will be beneficial for the low light imaging.

The light illumination was dimmed to 10 Lux Imaby inserting a neutral density filter with a ND number of 2, which reduces the light by 2 orders of magnitude. The integration time was increased to 200*ms* for both the low and high conversion modes. The low conversion gain image is shown in Figure 5.28. The image still looks reasonably good and all colors are correct, but some row wise noise and random noise are visible especially on the dark regions and dark patches.

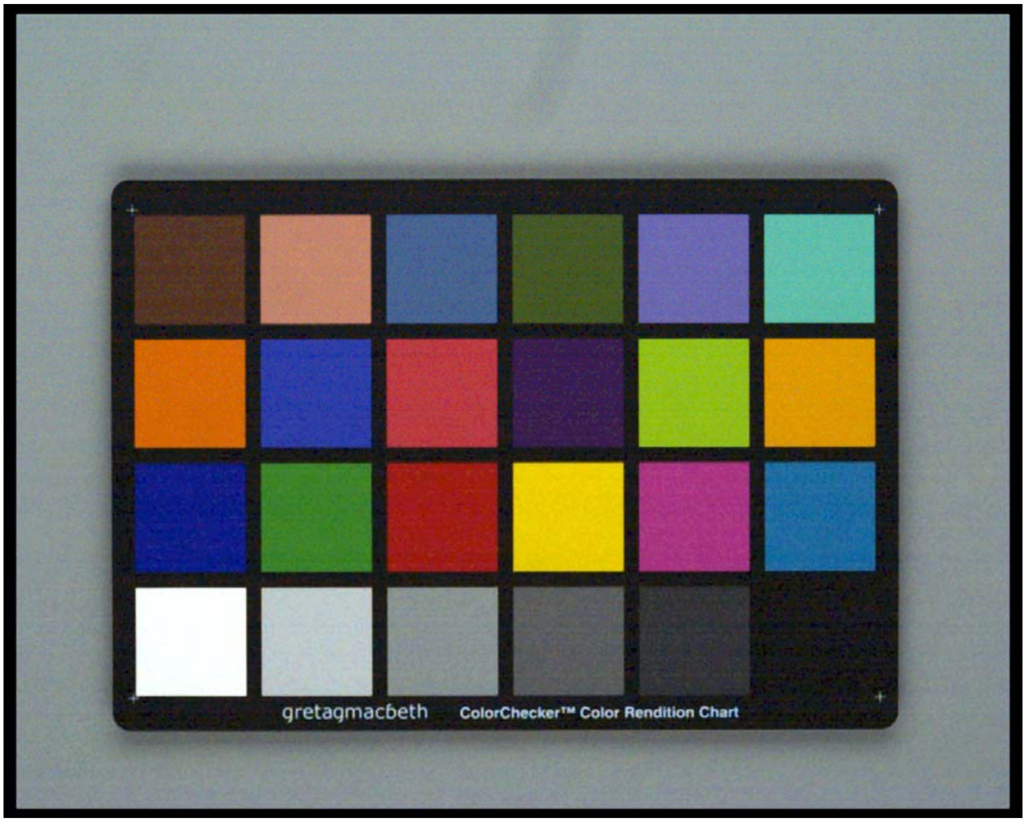


Figure 5.28: Low conversion gain Image taken under 10 Lux illumination with 5FPS

Under the same illumination condition (10 Lux) and with the same integration time (200*ms*), another image was captured with the high conversion gain mode as shown in Figure 5.29. Compared to the low conversion gain image shown in Figure 5.28, the high conversion gain image looks much cleaner. No visible noise can be seen from the image. This result shows the advantage of lower readout noise of the high conversion gain mode. The high conversion gain image outperforms the low conversion gain image under this low light condition.

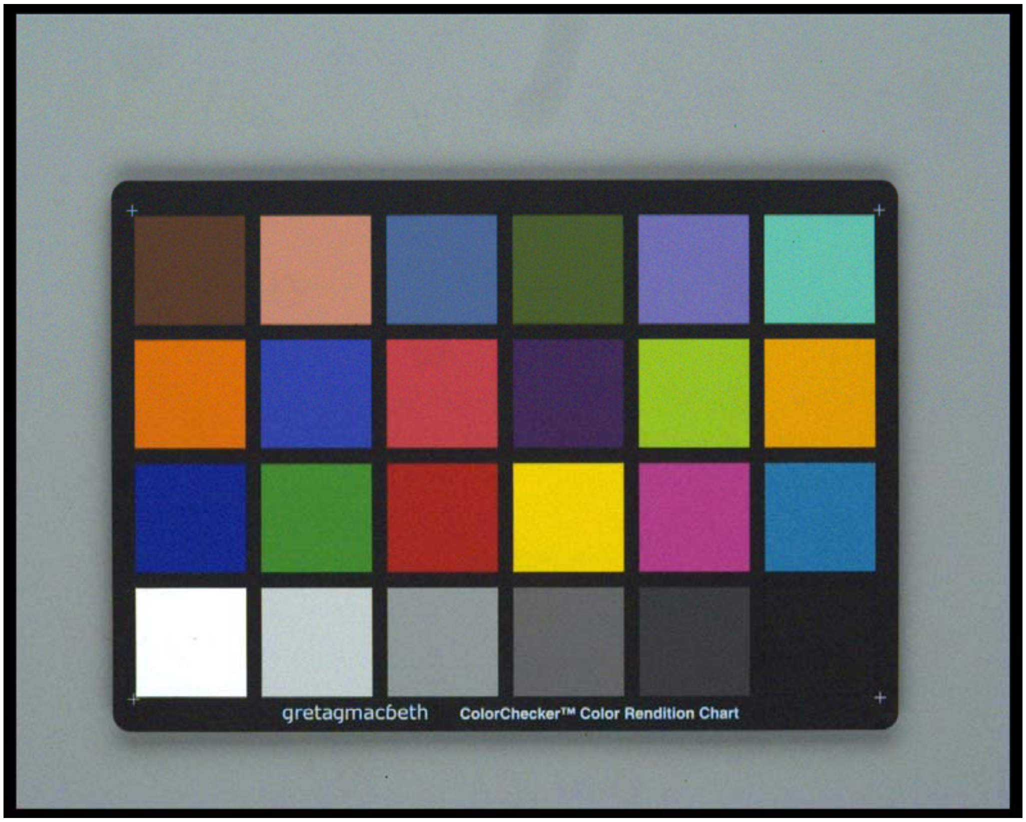


Figure 5.29: High conversion gain image taken under 10 Lux illumination with 5FPS

In order to further examine the advantage of the high conversion mode under low light conditions, the illumination level was further reduced to 1 Lux. The integration time was still kept at 200*ms*, which corresponds to 5FPS frame rate. The low conversion gain image is shown in Figure 5.30. From Figure 5.30, it can be seen that the image quality degrade quite significantly under 1 Lux illumination condition. Different color patches can still be separated; however the row wise noise and pixel wise noise are all visible across the whole array.

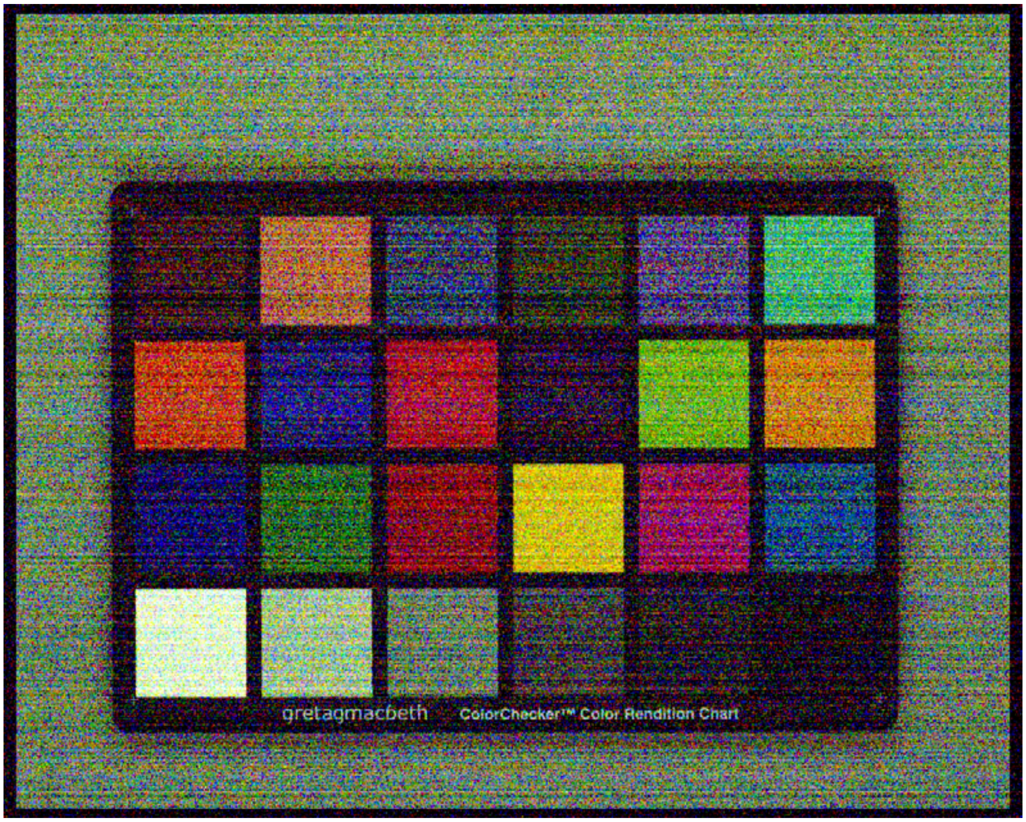


Figure 5.30: Low conversion gain image taken under 1 Lux illumination with 5FPS

Another high conversion gain image was captured under the same extremely low light conditions (1 Lux) with the same image integration time (200*ms*) as shown in Figure 5.31. From Figure 5.31, it can be seen that the high conversion mode shows clear advantage over the low conversion gain mode under 1 Lux illumination condition. The row wise noise is not very visible and the pixel wise noise is much less pronounced than the low conversion gain image. The colors are also more accurate than the low conversion gain image.

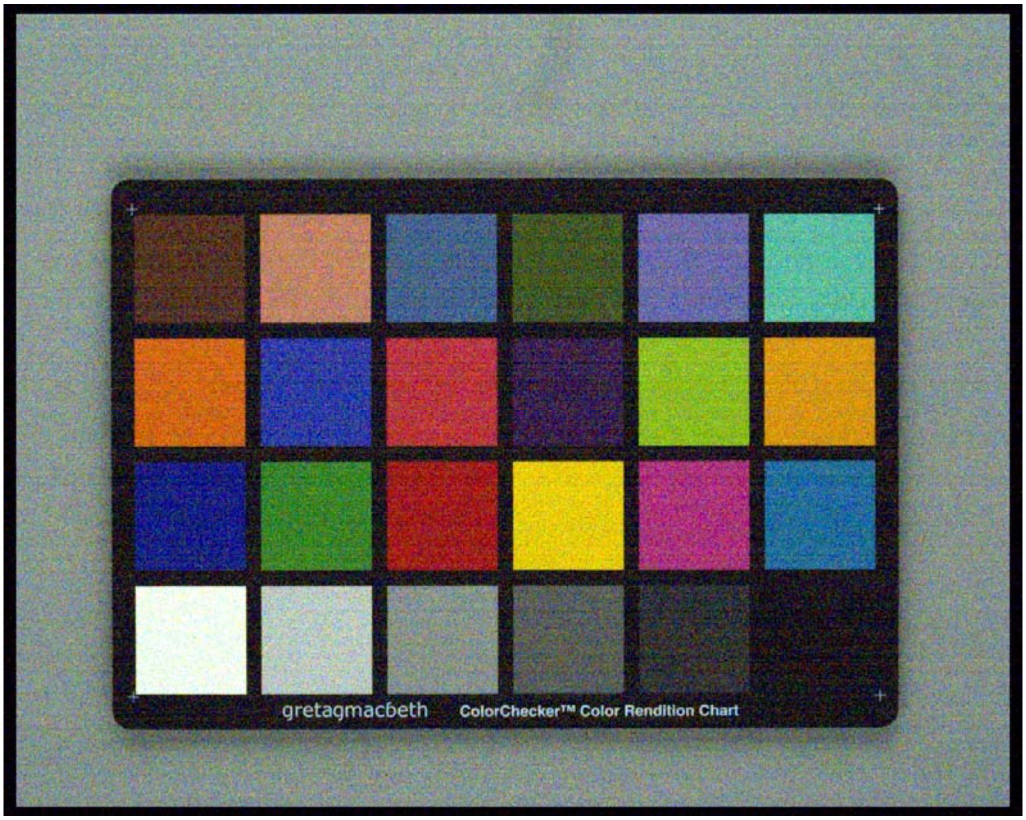


Figure 5.31: Image taken under 1 Lux illumination and 200*ms* integration time at high conversion gain mode with 5FPS

The higher full well capacity of the low conversion gain mode extends the sensor dynamic range under the high light illumination conditions. The lower readout of the high conversion gain mode shows the clear advantage for the low light imaging.

5.10 Summary of Pixel Characteristics

A prototype sensor with MOSFET modulated dual conversion gain pixel was designed and fabricated using the Micron Technology’s 130nm 3 metal and 2-poly process. The detailed pixel performance parameters are summarized in Table 5.5

Table 5.5: Measured pixel parameters summary

Pixel Parameters	Units	Low CG	High CG	Total Sensor
Pixel Size	μm^2	5.6 x 5.6		
Conversion Gain	$\mu V/e$	30.8	127	
Responsivity (Green Pixel @540nm)	*V/(Lux*s)*	2.2	9	
Photo Response Non-Uniformity (PRNU)	*%*	0.64	0.73	
Full Well Capacity	*e*	42000	10500	42000
SNR (max)	*dB*	46.2	40.2	46.2
Readout Noise Floor	*e*	8.6	2.1	2.1
Dynamic Range	*dB*	73.8	73.9	86
Quantum Efficiency (@Max Blue)	*%*	41.2		
Quantum Efficiency (@Max Green)	*%*	48.8		
Quantum Efficiency (@Max Red)	*%*	48.8		
Average Crosstalk	*%*	11.2		
Dark Current (65C)	*e/s*	127.5		
	pA/cm^2	65		
Activation Energy	*eV*	1.03		

CHAPTER 6 CONCLUSIONS AND FUTURE WORKS

6.1 Conclusions

A MOSFET modulated dual conversion gain pixel architecture was proposed and developed in this dissertation; this architecture increases the SNR and the dynamic range of the image sensors at both low and high illumination ends. The dual conversion gain pixel improves the pixel dynamic range by changing the conversion gain based on the illumination level without increasing any artifacts or increasing the imaging readout noise floor. A dual conversion gain MOSFET is used to modulate the capacitance of the floating diffusion node. The dual conversion gain transistor has its gate connected to the floating diffusion node, and has both source and drain terminals driven by the DCG control signal. When a high control signal is applied to the drain and source terminals, the transistor works in the depletion region, which corresponds to a lower capacitance of the floating diffusion node and a higher conversion gain. When a low signal is applied to the source and drain terminals, the transistor works in the strong inversion mode; thus the inversion capacitance adds to the floating diffusion node and increases the total floating diffusion node charge storage capacity and the conversion gain. Under high light illumination conditions, the low conversion gain is used to achieve higher full well capacity and wider dynamic range. Under low light conditions, the high conversion gain mode is enabled to lower the readout noise and achieve excellent low light performance.

A CMOS image sensor prototype with the new pixel architecture with 5.6μm pixel pitch was designed and fabricated using the Micron Technology's 130nm 3-metal and 2-poly silicon process. The pixel layout, readout timing, and operation voltage levels were optimized to increase the pixel quantum efficiency, SNR, full well capacity, and dynamic range. The dark current and hot pixels performance, FPN, readout noise, and RTS noise were further improved optimizing the pixel layout and operation.

The periphery circuitries were well designed to readout the pixel and support the pixel characterization needs. The row decoder and driver, column decoder, column sample and holds circuitry, column bias current, and switch capacitor low noise crow-bar amplifier were designed and fully simulated.

The detail characterization of the sensor was performed. A $127\mu V/e$ was achieved for the high conversion gain mode and $30.8\mu V/e$ for the low conversion gain mode. Characterization results confirm that a $42ke$ linear full well was achieved for the low conversion gain mode and a $10.5\ ke$ linear full well for the high conversion gain mode. An average $2.1e$ readout noise was achieved for the high conversion gain mode and $8.6e$ for the high conversion gain mode. The total sensor dynamic range was extended to $86dB$ with $46.2dB$ maximum SNR. These results represent a substantial performance improvement compared to state-of-the-art CMOS image sensors with a similar pixel size. Several images taken under different illumination levels showed the clear advantage of the high conversion gain mode for excellent low light imaging.

6.2 Future Works

For the MOSFET modulated dual conversion gain pixel, the capacitance of the floating diffusion node strongly depends on the fabrication process for both the high and low conversion gain modes. The dual conversion gain transistor size including both width and length needs to be tuned to achieve targeting conversion gain ratio. Also the channel implant doping profile may also have some impacts to the conversion gain value.

The proposed dual conversion gain pixel can be used in combination with the multiple exposure approach to further increase the sensor dynamic range. The high conversion gain mode can be used for long integration time to capture dark area of the scene, and the low conversion gain mode can be used for the short integration frame to capture the bright area of the scene. Then the final high dynamic range image can be synthesized by combining different images. The conversion gain ratio between the two conversion gain modes needs to be taken into account to get the final wide dynamic range image.

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