HIGH-SPEED RADHARD MEGA-PIXEL CIS CAMERA FOR HIGH-ENERGY PHYSICS

By

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Abstract

This dissertation describes the schematic design, physical layout implementation, system-level hardware with FPGA firmware design, and testing of a camera-on-a-chip with a novel high-speed CMOS image sensor (CIS) architecture developed for a mega-pixel array. The novel features of the design include an innovative quadruple column-parallel readout (QCPRO) scheme with rolling shutter that increases pixel rate, its ability to program the frame rate and to tolerate Total Ionizing Dose effects (TID). Two versions of the architecture, a small (128 × 1,024 pixels) and large (768 × 1,024 pixels) version were designed and fabricated with a custom layout that does not include library parts. The designs achieve a performance of 20 to 4,000 frames per second (fps) and they tolerate up to 125 krad of radiation exposure.

The high-speed CIS architecture proposes and implements a creative quadruple column-parallel readout (QCPRO) scheme to achieve a maximum pixel rate, 10.485 gigapixels/s. The QCPRO scheme consists of four readout blocks per column and to complete four rows of pixels readout process at one line time. Each column-level readout block includes an analog time-interleaving (ATI) sampling circuit, a switched-capacitor programmable gain amplifier (SC-PGA), a 10-bit successive-approximation register (SAR) ADC, two 10-bit memory banks. The column-parallel SAR ADC is area-efficient to be laid out in half of one pixel pitch, 10 µm. The analog ATI sampling circuit has two sample-and-hold circuits. Each sampling circuit can independently complete correlated double sampling (CDS) operation. Furthermore, to deliver over $10^{10}$ pixel data in one second, a high-speed differential Scalable Low-Voltage Signaling (SLVS) transmitter for every 16 columns is designed to have 1 Gbps/ch at 0.4 V. Two memory banks provide a ping-pong operation: one connecting to the ADC for storing digital data and the other to the SLVS for delivering data to the off-chip FPGA. Therefore, the proposed CIS architecture can achieve 10,000 frames per second for a 1,024 × 1,024 pixel array.

The floor plan of the proposed CIS architecture is symmetrical having one-half of pixel rows to read out on top, and the other half read out on the bottom of the pixel array. The rolling shutter feature with multi-lines readout in parallel and oversampling technique relaxes the image artifacts for capturing fast-moving objects. The CIS camera can provide complete digital input control and digital pixel data output. Many other components are designed and integrated into the proposed CMOS imager, including the Serial Peripheral Interface (SPI), bandgap reference, serializers, phase-locked loops (PLLs), and sequencers with configuration.
registers. Also, the proposed CIS can program the frame rate for wider applications by modifying three parameters: input clock frequency, the region of interest, and the counter size in the sequencer.

The radiation hardening feature is achieved by using the combination of enclosed geometry technique and P-type guardrings in the 0.18 $\mu$m CMOS technology. The peripheral circuits use P-type guardrings to cut the TID-induced leakage path between device to device. Each pixel cell is radiation tolerant by using enclosed layout transistors. The pinned photodiode is also used to get low dark current, and correlated double sampling to suppress pixel-level fixed-pattern noise and reset noise. The final pixel cell is laid out in $20 \times 20 \mu m^2$. The total area of the pixel array is $2.56 \times 20.28 \ mm^2$ for low-resolution imager prototype and $15.36 \times 20.28 \ mm^2$ for high-resolution imager prototype.

The entire CIS camera system is developed by the implementation of the hardware and FPGA firmware of the small-format prototype with $128 \times 1,024$ pixels and 754 pads in a $4.24 \times 25.125 \ mm^2$ die area. Different testing methods are also briefly described for different test purposes. Measurement results validate the functionalities of the readout path, sequencer, on-chip PLLs, and the SLVS transmitters. The programmable frame rate feature is also demonstrated by checking the digital control outputs from the sequencer at different frame rates. Furthermore, TID radiation tests proved the pixels can work under 125 krads radiation exposure.
This dissertation is the outcome of my six-year study, research experience at University of Nevada, Las Vegas and Alphacore, Inc.. I would like to take this opportunity to express my gratitude to all the people who have helped me during my Ph.D. study.

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