HIGH-SPEED RADHARD MEGA-PIXEL CIS CAMERA FOR HIGH-ENERGY PHYSICS

By

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Abstract

This dissertation describes the schematic design, physical layout implementation, system-level hardware with FPGA firmware design, and testing of a camera-on-a-chip with a novel high-speed CMOS image sensor (CIS) architecture developed for a mega-pixel array. The novel features of the design include an innovative quadruple column-parallel readout (QCPRO) scheme with rolling shutter that increases pixel rate, its ability to program the frame rate and to tolerate Total Ionizing Dose effects (TID). Two versions of the architecture, a small ($128 \times 1,024$ pixels) and large ($768 \times 1,024$ pixels) version were designed and fabricated with a custom layout that does not include library parts. The designs achieve a performance of 20 to $4,000$ frames per second (fps) and they tolerate up to 125 $krads$ of radiation exposure.

The high-speed CIS architecture proposes and implements a creative quadruple column-parallel readout (QCPRO) scheme to achieve a maximum pixel rate, 10.485 $gigapixels/s$. The QCPRO scheme consists of four readout blocks per column and to complete four rows of pixels readout process at one line time. Each column-level readout block includes an analog time-interleaving (ATI) sampling circuit, a switched-capacitor programmable gain amplifier (SC-PGA), a 10-bit successive-approximation register (SAR) ADC, two 10-bit memory banks. The column-parallel SAR ADC is area-efficient to be laid out in half of one pixel pitch, 10 μm. The analog ATI sampling circuit has two sample-and-hold circuits. Each sampling circuit can independently complete correlated double sampling (CDS) operation. Furthermore, to deliver over 10^{10} pixel data in one second, a high-speed differential Scalable Low-Voltage Signaling (SLVS) transmitter for every 16 columns is designed to have 1 $Gbps/ch$ at 0.4 V. Two memory banks provide a ping-pong operation: one connecting to the ADC for storing digital data and the other to the SLVS for delivering data to the off-chip FPGA. Therefore, the proposed CIS architecture can achieve $10,000$ frames per second for a $1,024 \times 1,024$ pixel array.

The floor plan of the proposed CIS architecture is symmetrical having one-half of pixel rows to read out on top, and the other half read out on the bottom of the pixel array. The rolling shutter feature with multi-lines readout in parallel and oversampling technique relaxes the image artifacts for capturing fast-moving objects. The CIS camera can provide complete digital input control and digital pixel data output. Many other components are designed and integrated into the proposed CMOS imager, including the Serial Peripheral Interface (SPI), bandgap reference, serializers, phase-locked loops (PLLs), and sequencers with configuration

registers. Also, the proposed CIS can program the frame rate for wider applications by modifying three parameters: input clock frequency, the region of interest, and the counter size in the sequencer.

The radiation hardening feature is achieved by using the combination of enclosed geometry technique and P-type guardrings in the 0.18 μm CMOS technology. The peripheral circuits use P-type guardrings to cut the TID-induced leakage path between device to device. Each pixel cell is radiation tolerant by using enclosed layout transistors. The pinned photodiode is also used to get low dark current, and correlated double sampling to suppress pixel-level fixed-pattern noise and reset noise. The final pixel cell is laid out in 20×20 μm^2. The total area of the pixel array is 2.56×20.28 mm^2 for low-resolution imager prototype and 15.36×20.28 mm^2 for high-resolution imager prototype.

The entire CIS camera system is developed by the implementation of the hardware and FPGA firmware of the small-format prototype with $128 \times 1,024$ pixels and 754 pads in a 4.24×25.125 mm^2 die area. Different testing methods are also briefly described for different test purposes. Measurement results validate the functionalities of the readout path, sequencer, on-chip PLLs, and the SLVS transmitters. The programmable frame rate feature is also demonstrated by checking the digital control outputs from the sequencer at different frame rates. Furthermore, TID radiation tests proved the pixels can work under 125 $krads$ radiation exposure.

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Chapter 1

Introduction

1.1 Overview of Imaging Sensors

A solid-state imaging sensor is a semiconductor device designed to detect optical information that can be used to create an image. An image sensor converts light into electric signals which use the photo-electric effect[1]. Image sensors can detect light across the electromagnetic spectrum by using different detector structures or different light-sensitive materials. This dissertation's image sensor design focuses on "visible" light with wavelengths ranging from 390 to 720 nm. A standard CMOS camera prototype is shown in Figure 1.1.

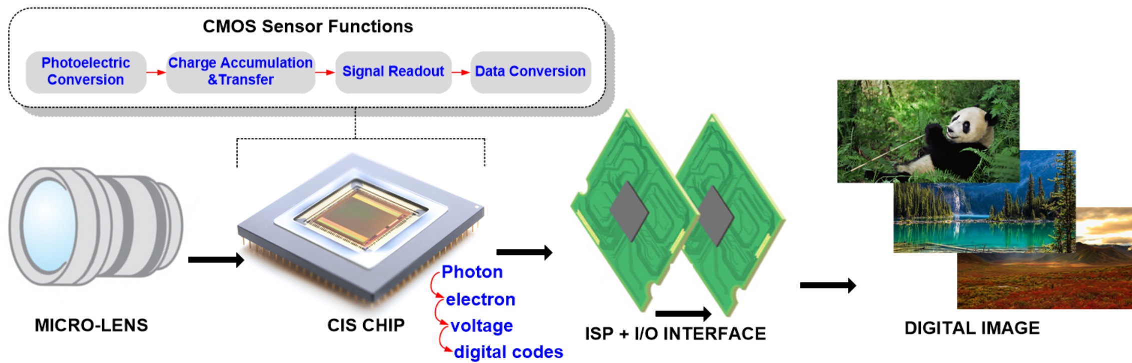


Figure 1.1: Typical CMOS camera prototype

Solid-state image sensors, in general, are classified by their sensor structures. Two prevalent image sensor technologies are the complementary metal-oxide-semiconductor (CMOS) and charge-coupled device (CCD) image sensor. The CCD was first proposed in the early 1970s. The CMOS image sensor chip was first invented at the Jet Propulsion Laboratory (NASA) in the 1990s [2]. Both technologies depend on the photo-electric effect to convert light into electric charge and then into an electric signal. CCDs were the main image sensor technology until about the mid-2000s. A comparison between these two techniques is presented in Table 1.1.

CCDs have historically been more competitive regarding image criteria such as low readout noise, higher quantum efficiency, high fill factor, and high dynamic range. CCDs were the key technology in the imaging sensor field for over 25 years according to the top cited publications of image sensors from 1973 to 1999. By using the Publish or Perish software[3], an image sensor survey based on the database of Microsoft Academic was conducted and the result is shown in Figure 1.2. A special manufacturing process is necessary for CCD cameras to transfer the charge in the pixel array without distortion. However, CMOS sensors are more inexpensive than CCDs since they use the standard CMOS manufacturing processes - the same processes used to make microprocessors. It is difficult to use CCDs in a low light, low temperature, and in a radiation environment. It is also challenging to design CCDs with a large pixel array, high frame rate and high integration with other camera functions on the same chip[4].

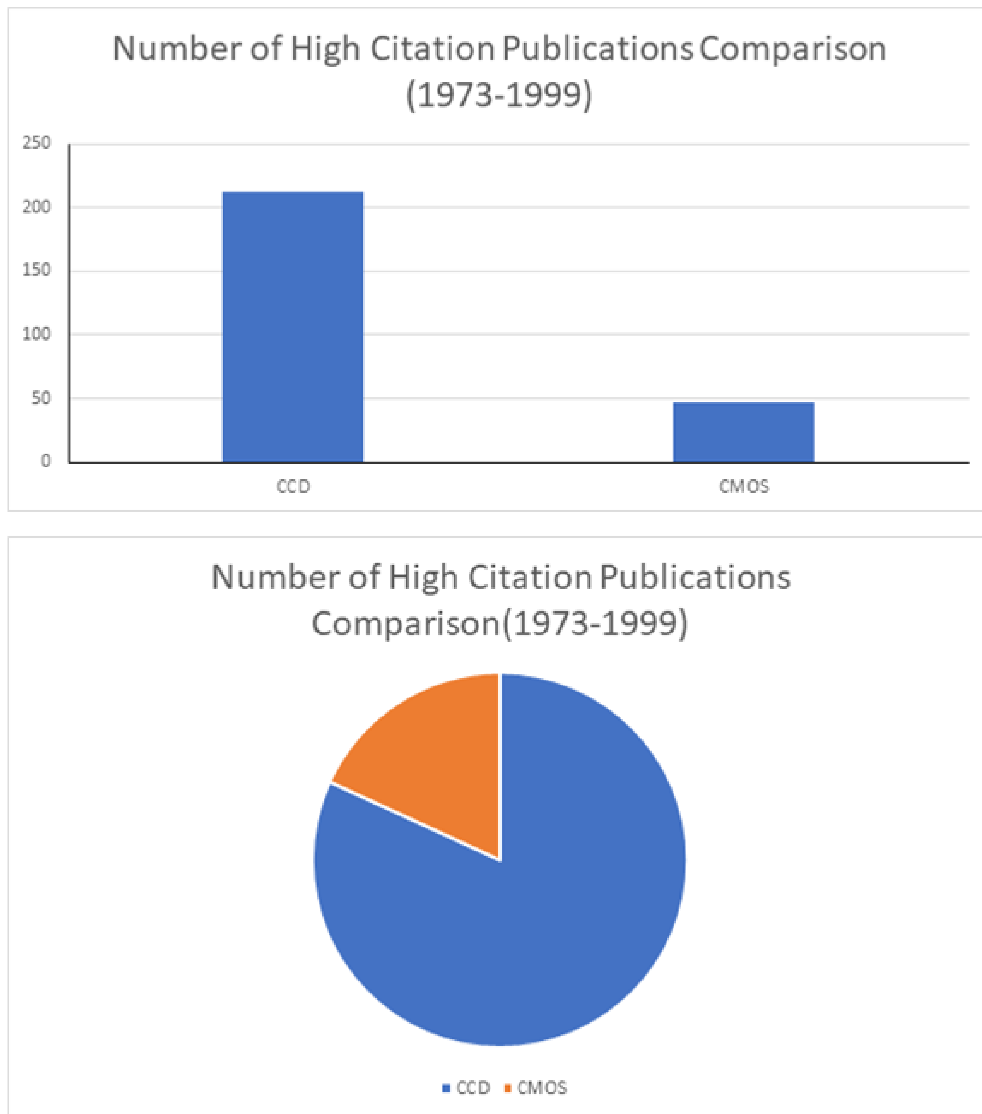


Figure 1.2: CCD vs CMOS sensors' publications with top citation from 1973 to 1999

The CMOS image sensor (CIS) technology has been developed for a couple of years and has become a mainstream technology. Figure 1.3 shows the developing status of CMOS image sensors by sorting top-citation image sensor publications from 1999 to 2017. The fast-growing market of CMOS image sensors benefits from the continuous scaling trend of CMOS technology. Several aspects make CMOS image sensors as a better alternative to CCDs.

First, the CIS sensor allows for the integration of other functions such as logic, memory, analog to digital converters (ADCs) and high-speed I/O interfaces on the same chip. Due to such integration, CIS makes it feasible to realize a camera-on-a-chip [5].

Second, in the CMOS pixel array, each pixel can detect the light and convert the charge to a voltage

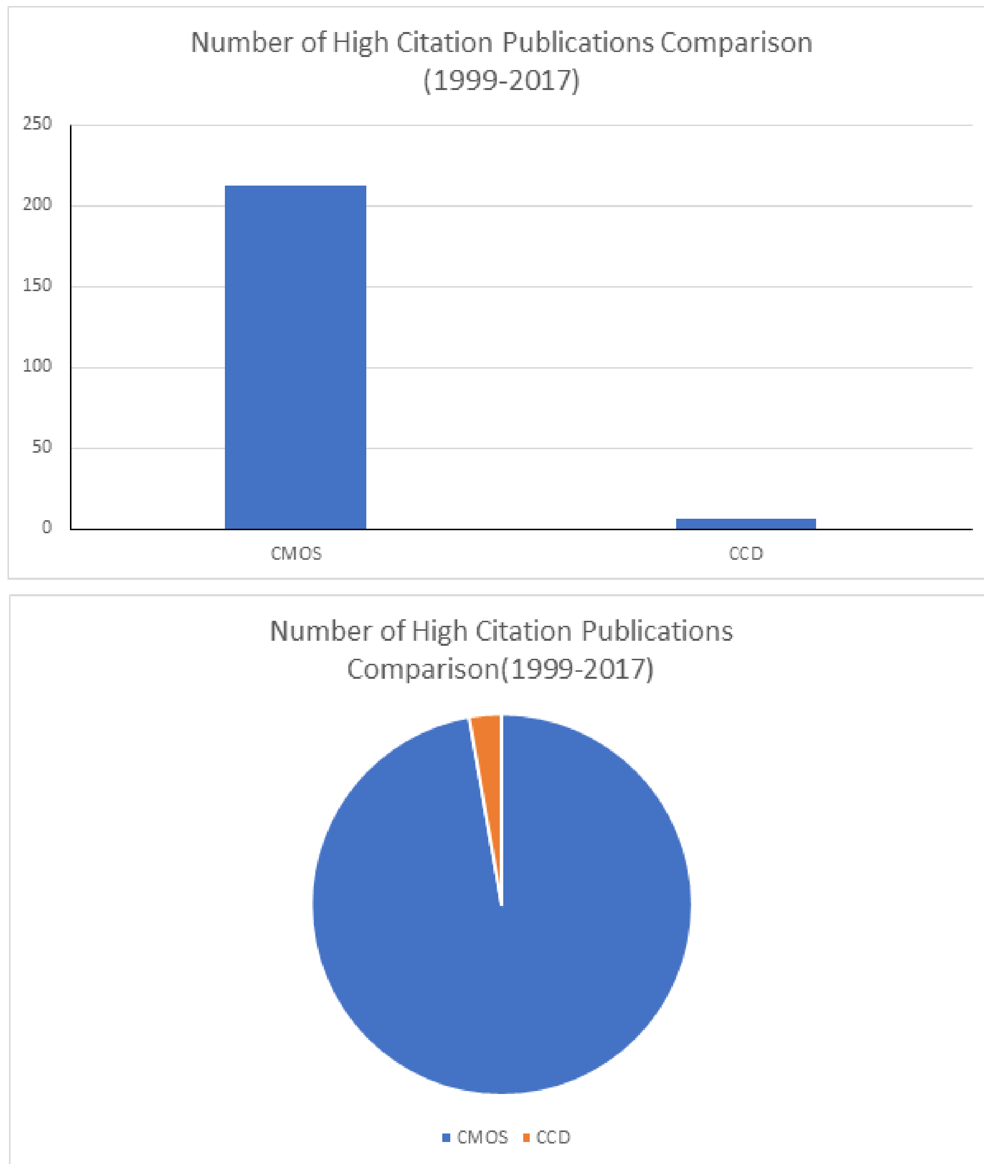


Figure 1.3: CCD vs CMOS sensors' publications with top citation from 1999 to 2017

independently. With the integration of other analog and mixed-signal integrated circuits, the CMOS sensors enable digital outputs. However, each pixel only performs the photon-to-electron conversion in a CCD sensor. The electron-to-voltage conversion is completed by a limited number of output amplifiers. Therefore, CMOS sensors far exceed at the readout process speed. Figure 1.4 depicts the comparison of CCD and CIS architectures.

Third, the CIS architecture has developed into an active pixel sensor (APS) from a passive pixel sensor (PPS). The active pixel sensor brings in better noise performance, higher frame rate, and an enormously increased functionality [6–18]. Moreover, new CMOS technologies provide a smaller pixel size, lower power consumption, and faster digital I/O interface.

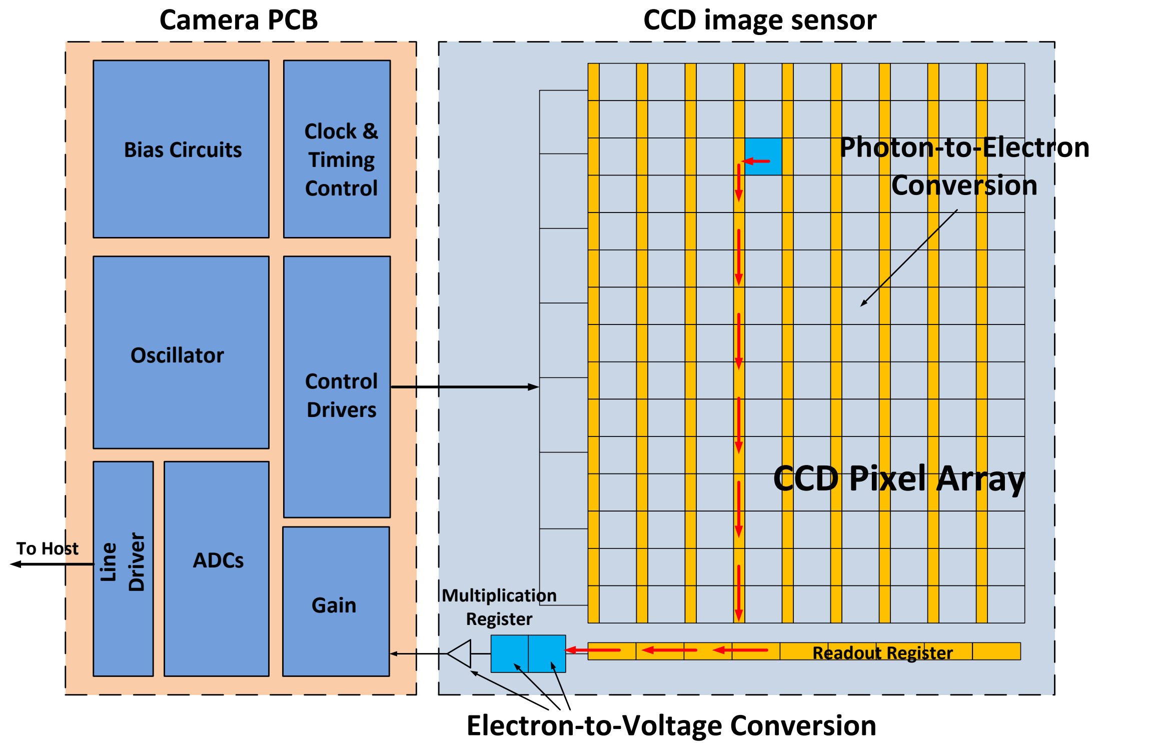
Within the last ten years, CMOS image sensors have stolen large market shares from CCDs in the imaging sensor industry. The 2018 O-S-D report, conducted by IC Insights company, predicts that automotive safety systems, medical and scientific imaging, as well as security and surveillance will be the main growth areas for CMOS image sensors. Worldwide sales are estimated to rise to about $19 billion total in 2020 as shown in Figure 1.5. Hence, the demand for CMOS image sensors will lead to continual performance improvement, and possibly maintain a breakneck growth in the image sensor market.

Table 1.1: Comparisons between CCD and CMOS

	CCD sensor (EMCCD or interline CCD)	**CMOS sensor**
Pixel Output	Electron	Voltage
Chip output	Analog	Digital
Chip Integration	Low	High
Windowing	Limited	Multiple
Speed	less than 10 frames/s	Hundreds and even thousands of frames/s
Power Supply	More than one power supply and various clock pulses with higher than 10V	One power supply lower than 5V
Image Artefact	Smearing, charge transfer inefficiency	FPN, motion
Shutter Mode	Global	Global or Rolling
Dynamic Range	>70dB	>70dB
Read Noise	less than 1 e- (rms)	less than 10 e- (rms)

EMCCD: Electron Multiplying CCD

In the CMOS image sensors, the front-side illuminated (FSI) architecture [20–39] may be used. FSI technology places the pixel array and peripheral circuits on the same side of the chip. Each CIS pixel includes a photo-detector (which could be a reverse-biased PN junction, photo-gate, or pinned photodiode) and several transistors to make a charge-to-voltage (C2V) conversion. The peripheral circuits include a digital control block, biasing block, ADCs, PLLs, high-speed transmitters, and memory banks. For the CIS system, there are three main metrics to evaluate the performance of a CIS: pixel layout, pixel physics, and pixel readout. Pixel layout relates to the number of pixels, pitch size, and fill factor. Pixel physics relates



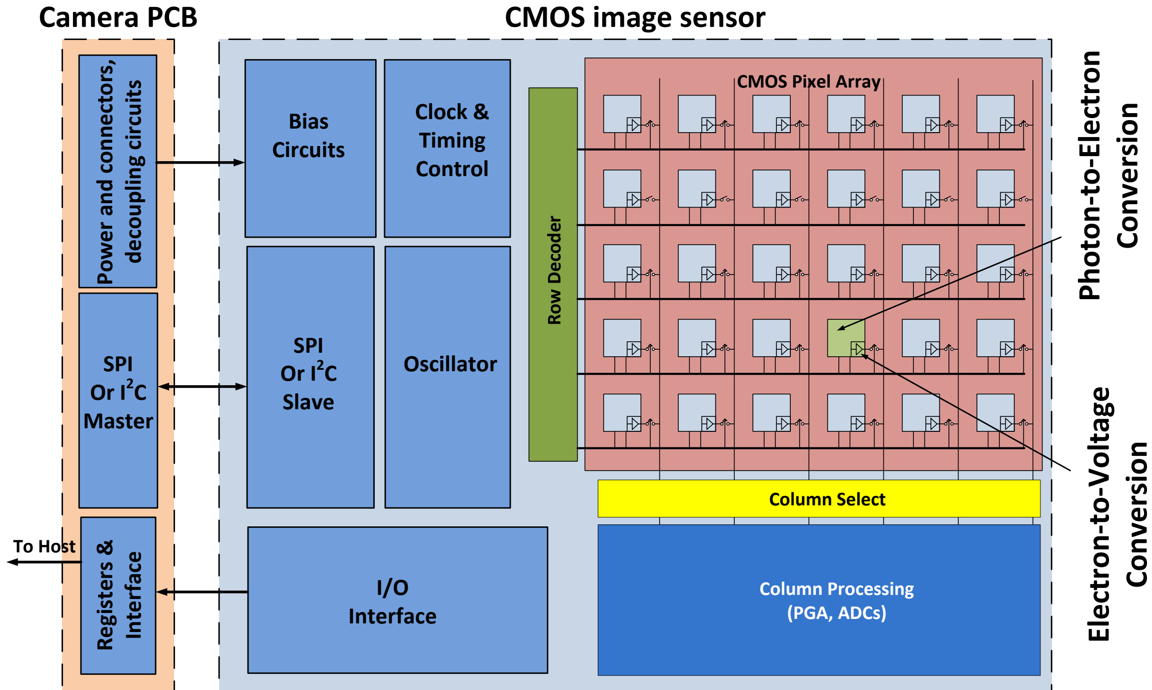


Figure 1.4: CCD vs CIS architecture

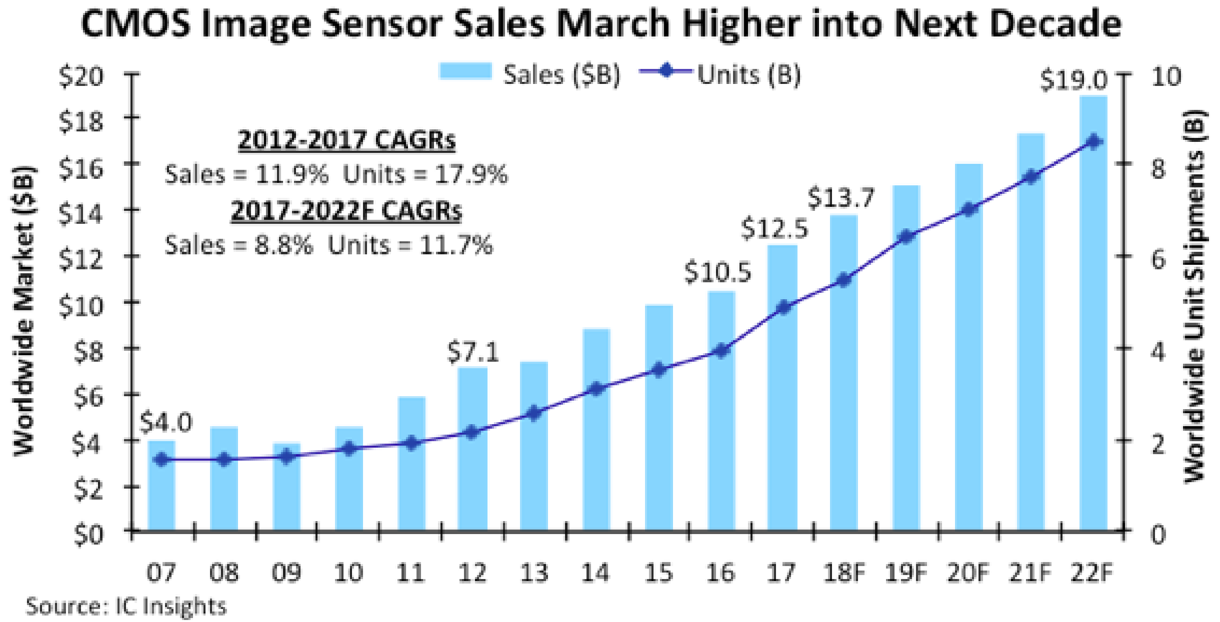


Figure 1.5: CIS camera market sales' trend[19]

to dark current, dynamic range, full-well capacity, quantum efficiency, and conversion gain. Pixel readout relates to frame rate, bit depth, signal-to-noise ratio, power efficiency, and more.

The pixel size of FSI CISs continue to decrease in size due to the scaling trend of CMOS technologies. Typically, smaller pixel size results in a higher image format, lower power and cost, and more functionalities added to the CIS camera. However, a smaller pixel reduces its full-well capacity, fill factor, and signal-to-noise ratio. A smaller pixel size also results in an increase of the system complexity and output data rate. It becomes difficult to meet the sub-circuits' design requirements, especially for high-speed and high-resolution CISs.

CIS manufactures are seeking new architectures for reducing the pixel size for high-resolution purpose, while preserving or augmenting electro-optical performance. One promising technology, back-side illumination (BSI)[7, 8], as shown in Figure 1.6 was developed to collect light through the backside of the chip by turning the pixel upside down for increasing the fill factor close to 100%.

Recently, a 3D stacked technique has been used to further improve CIS performance (pixel characteristics, frame rate, and resolution) [6–9, 40–47]. The stacked structure allows for the splitting of the detector array, memory blocks, and readout block into different chips by using wafer bonding or Cu-Cu connection. Both the sensor performance and camera functionalities are improved. However, all these improvements have inevitably increased the design and manufacturing cost of CIS cameras.

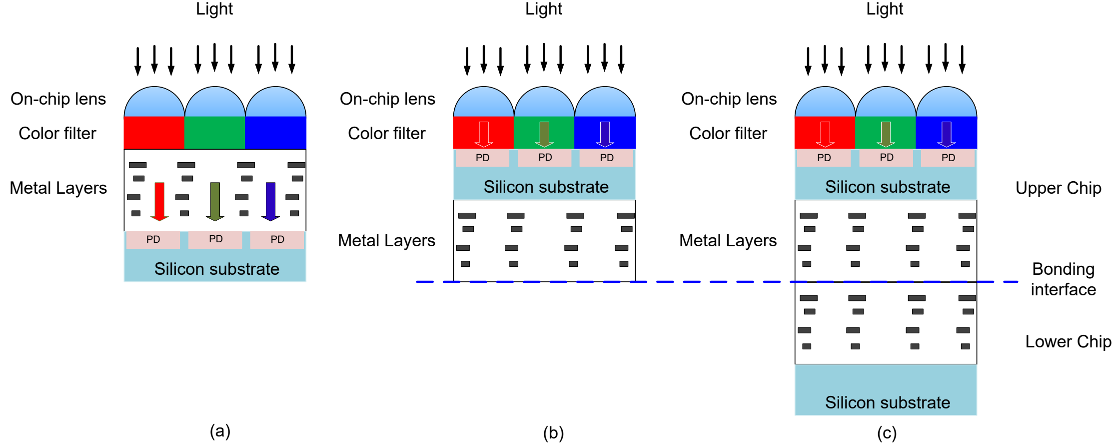


Figure 1.6: (a) FSI sensor, (b) BSI sensor, (c) 3D-stacked BSI sensor

1.2 High-speed High-resolution CMOS Image Sensor

High-speed high-resolution imagers have widely used CMOS technology with active pixels. The major advantages include low cost, low power operation, and the integration of the sensor array and processing circuits on the same chip. High-speed imaging sensors are widely used in the analysis of high-speed machinery, the observation of high-speed phenomena, and broadcasting television stations and sports. The demand for slow-motion video capturing in popular smartphones and other portable cameras has also increased. Fast captured images or videos can achieve a slow-motion feature while playing the images back at a lower speed. Therefore, more efforts [6–9, 11, 13, 20–39, 47–50] have been made to improve the frame-rate enhancement in CMOS image sensors.

High-speed CISs can be classified into two main categories: off-chip ADC scheme [20, 33, 35, 37–39] and on-chip ADC scheme [6–9, 11, 13, 21–27, 29–31, 34, 36, 47–50]. In terms of on-chip ADCs, three major architectures are widely employed in the CIS cameras: the channel ADC, column-parallel ADCs and pixel-level ADCs. The channel ADC approach uses a single or several ADCs on-chip for a whole pixel array. This requires extremely high-speed ADCs for high frame rate achievement in a medium or large pixel array. The column-parallel ADC method applies one ADC per column. Given the same image format and frame rate, each column ADC is responsible for one column of pixels instead of the whole pixel array to accomplish data conversion. This obviously relaxes the requirement of each ADC speed requirement. The pixel-level ADC allows one ADC per pixel which allows each pixel to output digitally. In this case, the pixel-level ADC architecture results in extremely high frame rate at the price of silicon area and power consumption.

CMOS sensors with on-chip ADCs enable data conversion to occur on the chip. They facilitate serial digital data to be transferred to the on-board DSP or microprocessor. This on-chip ADCs architecture permits high-speed data transfer and better resistant to noise, compared to those with off-chip ADCs. Since the mid of 1990s, high-speed CISs have employed either the column-parallel ADC[11, 21–27, 30–32, 36, 50] or the pixel-level ADC method[34, 47, 51]. Prior to 2015, the column-parallel ADC approach was preferred

because of an excellent trade-off between the number of ADCs, chip size, power consumption, and speed of readout processing. While the size of CMOS technology used in CMOS image sensors was scaling from 0.5 μm to 0.13 μm to get a smaller pixel size and the larger pixel array, the architecture would not need to change much. More ADCs are used in each column because of the column-parallel ADCs could be located at either one side of pixel array or both sides. As a result, for a given pixel array, CIS enables to permit more pixels to make data conversion at the same, resulting in a shorter readout time in each frame. The frame rate has been successfully increased from hundreds of frames per second (fps) to thousands of frames per second.

The design of high-speed CMOS imagers poses three main challenges: I/O bottleneck for high pixel rate, correlation between frame rate and pixel array, and short exposure time. The first issue is related to the I/O. High-speed high-resolution CMOS imagers require high pixel rate, which can be implemented either by increasing the number of I/Os or by increasing the speed of each I/O. However, the CIS architecture consumes more power and makes the on-board acquisition system more complicated and challenging to process a massive amount of image data.

The second issue is that the frame rate is tightly correlated to the pixel resolution. Equation 1.1 illustrates that pixel rate (PR) is a product of frame rate and pixel resolution, in a unit of $pixels\ per\ second$ or $pixels/s$ or $pixs/s$. The available pixel rate is constrained by the output I/Os. At a given fixed PR, the frame rate is inversely proportional to the pixel resolution. As shown in Figures 1.7 and 1.8, high-speed (over 1000 frames per second) CIS imagers do not have an image format over 1 $Mpixels$. High-resolution CIS cameras have a lower frame rate of less than 300 fps.

$$\begin{aligned} PR &= Frame\ Rate \times Pixel\ Resolution \\ &= Frame\ Rate \times \#\ of\ pixels\ per\ frame \end{aligned} \tag{1.1}$$

The third problem is the challenge of implementing high-speed imaging for low-light applications. A dim environment requires increased exposure time to ensure that the image is properly exposed. How can such an increased exposure time be realized in high-speed cameras? The field of view can be sacrificed to allow for a greater frame rate. Two digital techniques of binning and windowing grant the CIS sensors to have no restrictions on the location of regions of interest.

Within the last five years, advanced techniques[6–9, 47, 52] such as back-illumination, 3-D wafer/chip stacking, and Cu-Cu connection techniques have become more popular. These methods are used to increase the speed of CMOS image sensors without sacrificing the image resolution and other pixel-related parameters, such as fill factor and full-well capacity. CISs are made to have the capability of employing different CMOS technologies for pixel design and readout circuitry, separately. Furthermore, a much higher integration of logic circuits, and column processing circuits are enabled to improve sensor performance and expand sensor functionality. As a result, the pixel-level ADC architecture has become more prevalent in high-speed imaging.

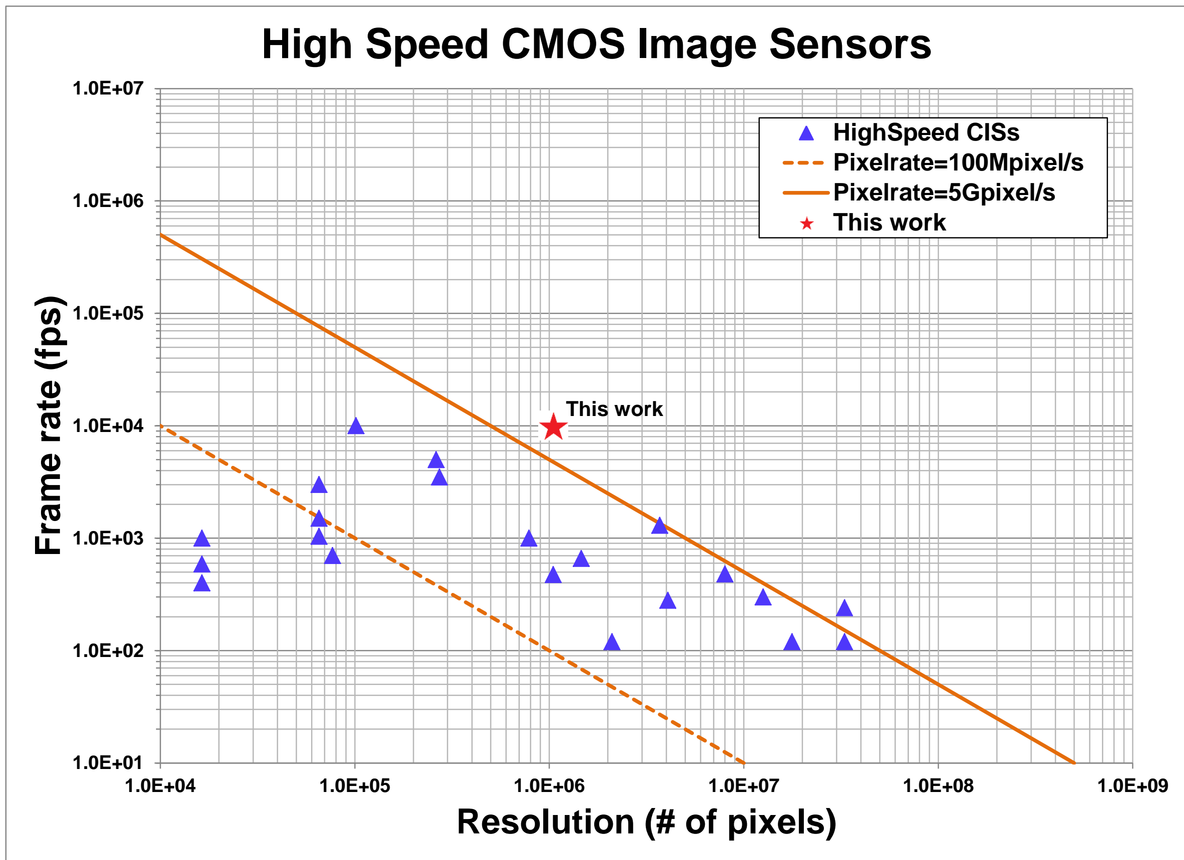


Figure 1.7: High-speed CMOS image sensors

ADCs play a significant role in CIS imagers in the conversion of the image data into digital information, regardless of CIS architecture. Four different types of ADCs are commonly used: successive-approximation register (SAR) ADC, cyclic ADC, Sigma-delta ADC, and single-slope ADC. The most popular architecture is the single-slope ADC as shown in Figures 1.9 and 1.10.

The shutter mode is another significant design point for high-speed CIS cameras. There are typically two modes: rolling shutter and global shutter. Recent high-speed CMOS sensors commonly operate at the global shutter mode, allowing all pixels to expose simultaneously and to process the readout row by row. Rolling shutter CISs expose each line of pixels in sequential order and results in visible aberrations by allowing the target to move from one line to next. The global shutter technique allows the same exposure time for each pixel resulting in no distortion for high-speed imaging capture, while it achieves lower speed than the rolling shutter. However, the distortion introduced by rolling shutter becomes less problematic when the speed of CISs is significantly higher than the moving speed of the target. Also, the rolling shutter provides a higher exposure time than the global shutter at the same speed operation.

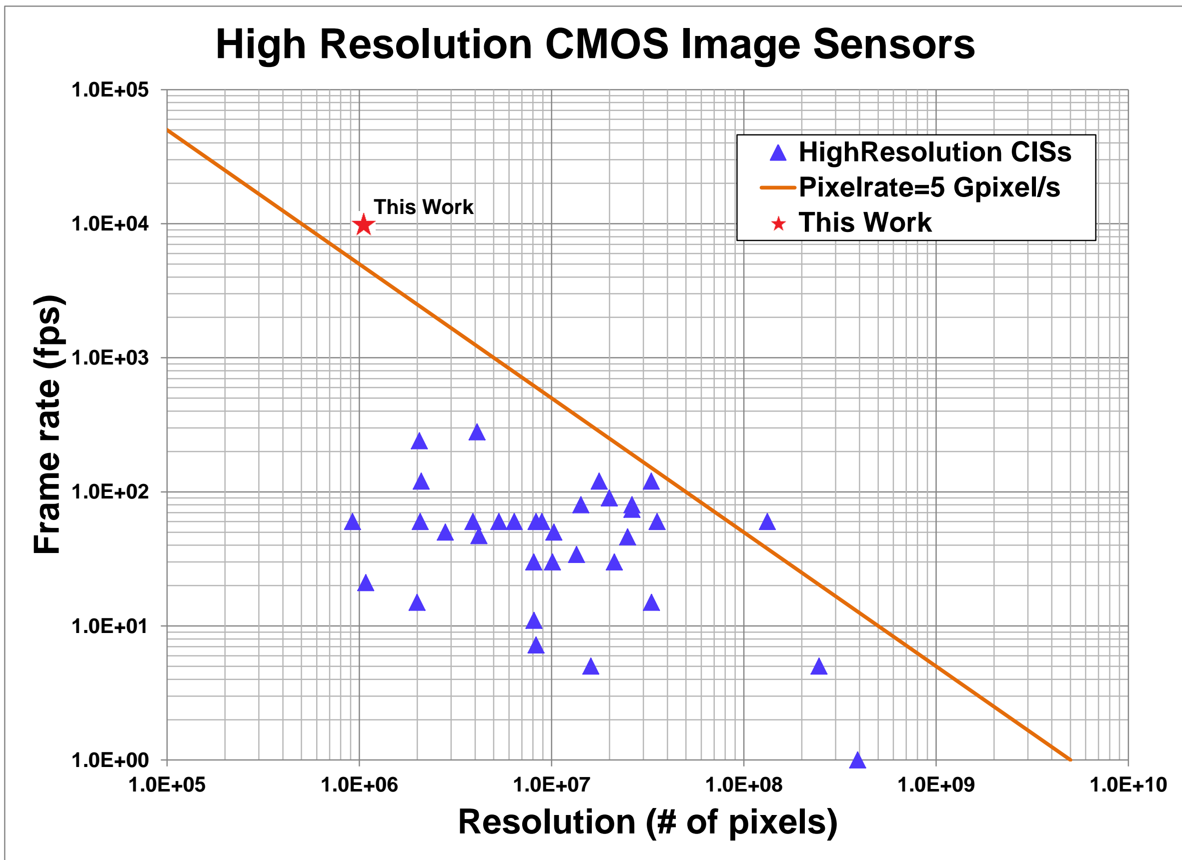


Figure 1.8: High-resolution CMOS image sensors

This Dissertation mainly focuses on the design of a camera-on-a-chip (CoC) with the implementation of a column-parallel ADC architecture to achieve high frame rate with a megapixel array. Instead of using an expensive CMOS process or other advanced techniques, a standard 0.18 μm CIS process is used to take advantage of the largest chip size to get highest pixel rate and massive resolution.

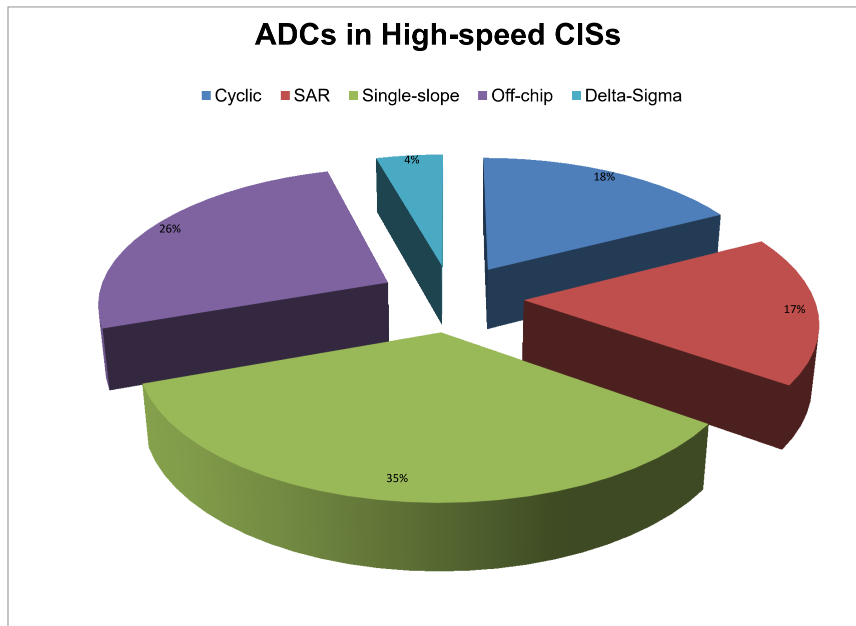


Figure 1.9: ADCs [6–8, 11, 22–27, 30–39, 47, 50] in high-speed CMOS image sensors

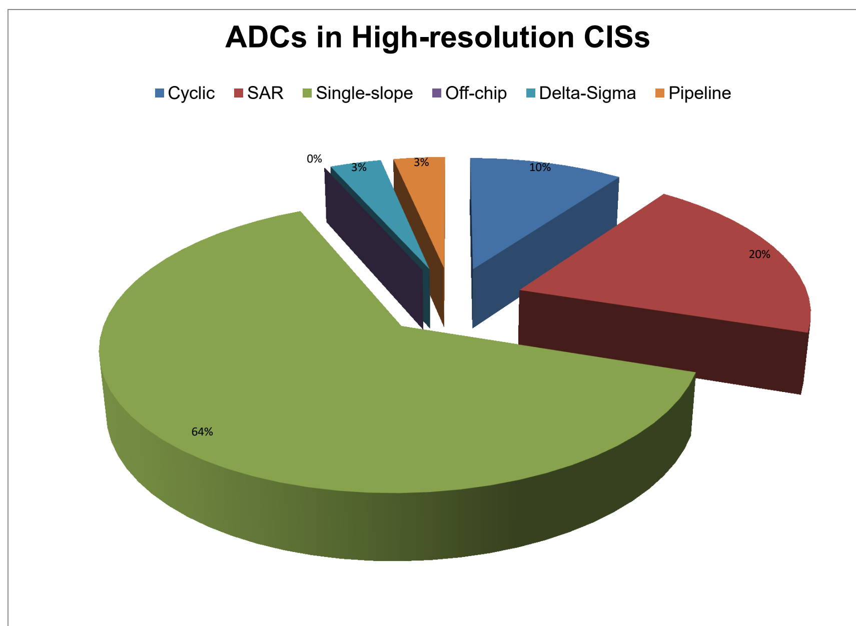


Figure 1.10: ADCs [15–18, 40–43, 46, 53–77] in high-resolution CMOS image sensors

1.3 Radhard CMOS Image Sensor

In recent years, a specific set of applications require CMOS image sensors that are capable of operating in harsh radiation environments. These applications include nuclear applications, space remote sensors, medical imaging, and particle detection. The definition of radiation in physics is a type of energy emitted or transmitted through space or a material medium in the form of waves or particles. The radiation effect has two classifications that depends on the energy of radiated particles: ionizing and non-ionizing effects. These two mechanisms are illustrated in Figure 1.11.

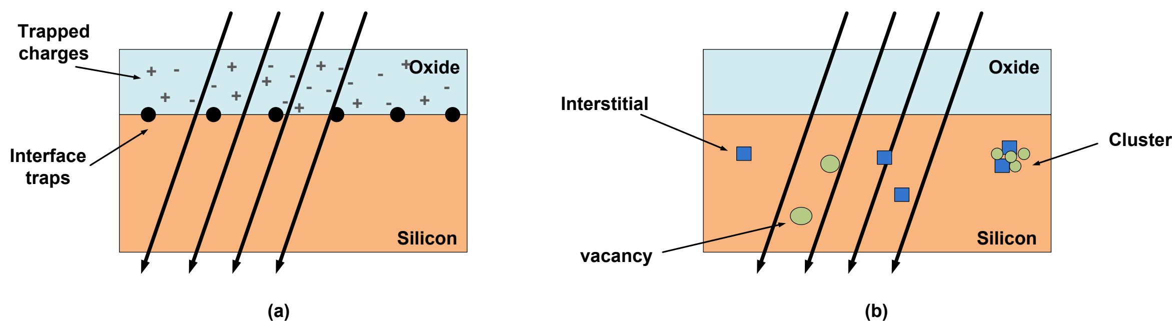


Figure 1.11: Representations of energy transfer through (a) ionizing, (b) non-ionizing mechanisms

Ionizing radiation, also called radioactivity, contains enough energy to overcome the binding energy of electrons in atoms, thus creating ions. Ionizing radiation is induced by radioactive substances that can emit different types of radiation. The radiation can be characterized by the three forms of radiations: α, β, γ. Alpha radiation consists of helium nuclei, beta radiation contains electrons and positrons, and gamma radiation is made up of photons, respectively. The ionizing radiation effect consists of two main effects: the single event effect and total ionizing dose effect. The generation process of the ionizing mechanism can take place not only in silicon but also in silicon oxide. Up to now, the ionizing radiation interaction with SiO_2 has been widely studied for integrated circuits fabricated using CMOS technology. Two units of ionizing radiation damage in semiconductors are rad (radiation absorbed dose) and Gy (Grey). One hundred rad is equal to one Gy, 100 $rad = 1Gy$. Moreover, the rad is typically to specify the material because of its material dependence.

Non-ionizing radiation refers to displacement damage (DD) in general. High-energy particles, such as protons or neutrons, are the source of displacement damage in silicon. DD is a cumulative, long-term damage to CMOS devices. High-energy particles can kick out an atom from its equilibrium position. The atom becomes an interstitial defect and leaves a vacancy in the original position on the silicon lattice. Figure 1.12 illustrates a collision and the subsequent displacement of an atom from the silicon lattice. Displacement effects are measured via the total number of particles crossing a given area, which is defined as the fluence with units of p/cm^2. Although some interstitial defects can be annihilated by the vacancies later, some of them remain.

Moreover, divacancies are formed by some vacancies and interrupt the crystal periodicity. Thus, bulk effects in semiconductor devices and materials are caused by the displacement damage. The measurement of substrate current could be used to analyze the displacement damage.

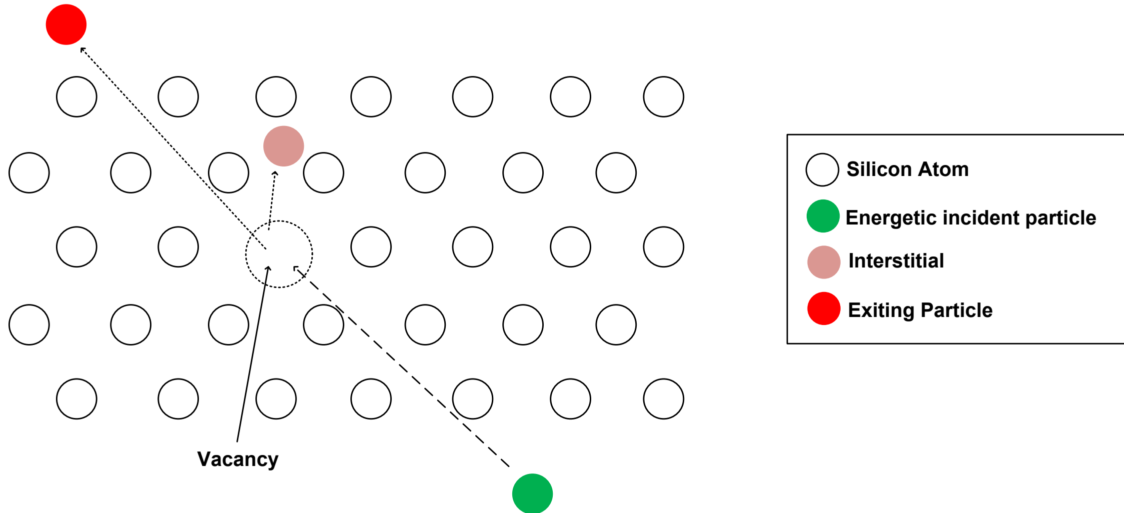


Figure 1.12: Displacement damage causes lattice defect

Two main radiation effects are induced by different sources on CMOS image sensors. They are cumulative effects and single-event effect. The long-term cumulative effects include total ionizing dose (TID) and displacement damage (DD). A classification diagram of radiation effects is shown in Figure 1.13. Cumulative effects are the gradual degradation of semiconductor devices until the damage reaches the maximum value that the device can tolerate. For the TID effect, the ionization dose is deposited by particles passing through the semiconductor materials constituting the electronic devices. It is usually characterized by the maximum drift of the main device parameters.

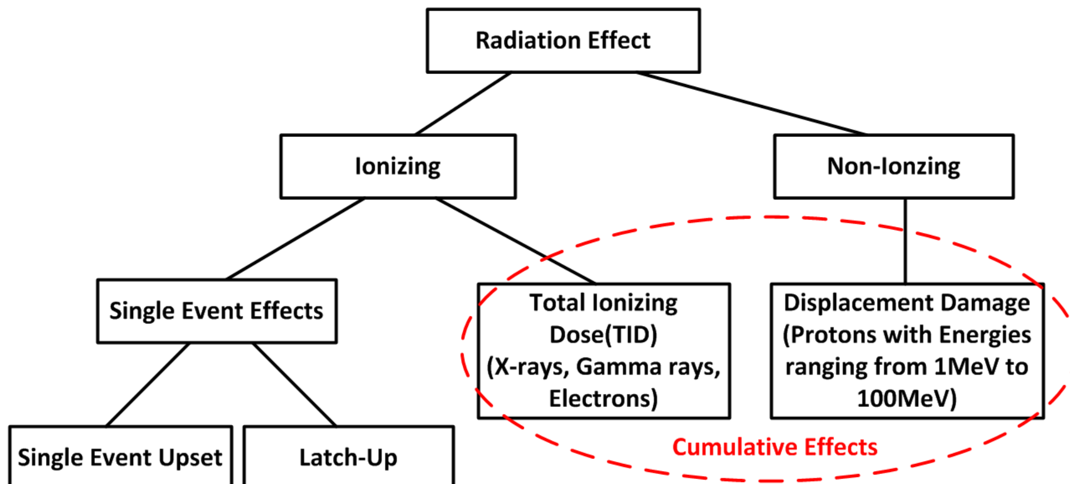


Figure 1.13: Classification of radiation effects

Single event effect (SEE) is caused by the energy deposition from one single particle. SEE is a transient effect and can happen at any moment. SEE is the immediate result of a single radiant charged particle that crosses a sensitive device region, which includes single-event upsets (SEUs), single-event functional interrupts (SEFIs), single-event transient (SETs), and single-event latchups (SELs). Extensive studies have made on the SEE, which mostly affects digital circuits. The high-energy particle can leave an ionized track when traveling through a semiconductor. The stochastic effects may lead to destructive or non-destructive damage to the device. As far as SEE is concerned, the most important figure is the rate of occurrence.

From MOSFETs to bipolar ICs, oxides and insulators are vital components of many electronic devices. Ionizing radiation can cause device degradation and failure by inducing significant charges built up in these oxides and insulators. The work in this Dissertation focuses on the high-energy particle accelerator application which exposes CMOS image sensors to high fluxes of electrons and protons causing a significant reduction of system lifetime due to TID. Therefore, the work aims to focus on TID effect on CMOS active pixel sensors (APSs).

1.4 Motivations

Two prominent Figure of Merits (FoMs) in CMOS image sensors is the frame rate and resolution. Due to the high demand of CMOS imaging technique in high-energy physics, space exploration, medical imaging, or other scientific experiments, radiation tolerance becomes another important FoM.

The high frame rate can provide the feature of capturing images in a short time. High resolution can quantify the sensor's ability to capture images in a vast region of interest. Radiation hardness brings resistance to the effects of ionizing radiation for CMOS image sensors having a longer lifetime.

However, high-speed CISs, in general, suffer from high power consumption and low pixel format. High-resolution CISs need either a large chip area for photodetectors or advanced CMOS technology with smaller fill factor and lower sensitivity. Having a radiation hardness feature makes the CMOS image sensor design more challenging.

The work discussed in this Dissertation can be applied to high-energy physics applications for studying the nature of particles. Specifically, the CIS prototype will be used in a particle accelerator to capture images in a harsh environment. Particle accelerators, as the well-known tool, plays an essential role in national security and scientific experiments for particle and nuclear physics.

Recent research discoveries in radhard CMOS CISs are promising. Yet, none of them push the radhard cameras to be high speed and high resolution.

This dissertation aims to design a radhard CMOS image sensor with a high frame rate and a megapixel array. Two CIS prototypes are fabricated using XFAB CIS 0.18 μm process. They use the same readout architecture, a new radhard 4T pixel, and high-speed SLVS transmitters. The primary purpose of this dissertation is to create a more power, area, cost and speed efficient radhard CMOS imager - while considering results for future optimization.

1.5 Dissertation Organization

This dissertation is organized into six chapters. Chapter 1 gave an overview of the CMOS image sensors. It also provided a survey of CISs with high frame rate and high pixel format. A brief discussion on radiation effects on CMOS technology and CISs was also contained in Chapter 1.

Chapter 2 reviews the characterization of CMOS image sensors. This chapter includes further details regarding the radiation effects on CMOS image sensors.

Chapter 3 introduces a high-speed readout architecture for a 10,000 fps CIS with 1024×1024 pixels. The pixel array is specially designed for radiation tolerance.

Chapter 4 discusses more details on the entire system and its sub-components. These components include a row decoder, column-parallel ADC, programmable amplifier, time-interleaving sample and holds for correlated double sampling, and SPI interface. Technical discussions with simulations have been given for some circuits. Two prototypes with the same architecture and different pixel format have been fabricated. In the end of the chapter, pictures of final layouts, CIS die and chip are posted.

Chapter 5 briefly discusses the hardware design and PCB implementation for testing the small-format CIS chip. The chip measurement of the proposed CIS has also been described. The functionality of the sequencer, master PLLs, and SLVS drivers have been demonstrated. Moreover, the programmable feature of the frame rate and radhard pixels are validated.

Chapter 6 summarizes the results of the Dissertation including the work's specific contributions to advancing the state of the art beyond previous work. It also gives some suggestions for future work.

Chapter 2

Overview of CMOS Image Sensors and Radiation Effects

This chapter provides a discussion of light-to-electric conversion, two types of photodiodes, and radiation effects. The first section discussed the light-to-electric conversion process. Then, the second section describes two types of photodiodes in CMOS technologies: the PIN photodiode and the pinned photodiode. The PIN photodiode is a PN junction with an intrinsic region between the n- and p-doped regions. The pinned photodiode, not be confused with the PIN photodiode, places a shallow doped p+ layer above an N+/P-sub diode. The additional p+ layer pins the potential at the surface to that of the substrate yielding a low dark current and an improvement of the quantum efficiency for the photodiode. Various parameters, such as dark current, quantum efficiency, and full-well capacity, are also discussed for better characterizing the CIS performance. Finally, the ionizing radiation effects on CISs are detailed, with total ionization dose (TID) effect as the primary focus.

2.1 Light-to-Electric Conversion

According to classical electromagnetic theory, light is made up of small particles, called photons. When light shines on photodetectors, some of the incident photons enter the semiconductor device and collide with atoms. When the energy of photons exceeds the semiconductor's band-gap energy, E_g, some electrons in the active area absorb the energy from the photons and break free from the atom, resulting in the generation of electron-hole pairs, which is called the photoelectric effect.

$$E_{photon} = h \times v = \frac{h \times c}{\lambda} \geq E_g \tag{2.1}$$

where v is the speed of light, λ is light wavelength, h is Planck's constant($4.135 \times 10^{-15}\ eV$), and c is light speed ($3 \times 10^{8}\ m/s$).

The equation above is used to compute the energy of a photon that corresponds to different visible light wavelengths as depicted in Figure 2.1. The visible E_{photon} varies from 1.7 eV to 3.8 eV. The silicon (Si) bandgap is 1.14 eV as shown in Table 2.1. Since the silicon's bandgap energy is less than the energy of the photon, silicon is a widely used semiconductor material for visible light detection. When a photon has an energy less than 1.1 eV, or its wavelength is longer than 1100 nm, silicon is transparent. Thus, silicon material can be used for photodetection in CMOS image sensors. which accommodate image capture, readout, and processing on a single chip.

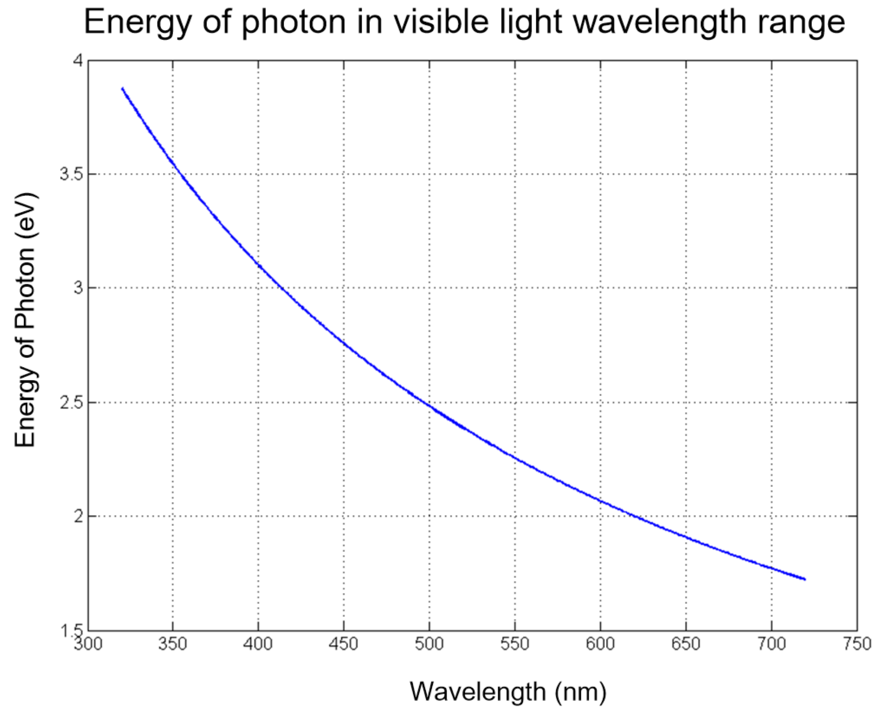


Figure 2.1: Energy of a photon vs visible light wavelength

Table 2.1: List of bandgap in different materials[78]

Group	**Material**	**Symbol**	**Bandgap (eV) @ 302K**
IV	Germanium	Ge	0.67
IV	Silicon	Si	1.14
III-V	Gallium arsenide	GaAs	1.43
III-V	Gallium phosphide	GaP	2.26
III-V	Gallium nitride	GaN	3.4
IV-V	Silicon nitride	Si_3N_4	5
IV	Diamond	C	5.5
III-V	Aluminium nitride	AlN	6
IV-VI	Silicon dioxide	SiO_2	9

2.2 Photodetectors

Each pixel in an image sensor is a photodetector (PD). A photodetector acts like a "charge bucket" that accumulates charge in the active area of the photodetector during the exposure time. The charges at a photodetector are converted into an equivalent current or voltage that corresponds to a certain light intensity. Various types of PDs exist, including photodiodes, photogates, phototransistors, and avalanche photodiodes. These diodes can detect photons and generate electron-hole pairs (EHP). They also have different strengths which can be applied to different applications. This section focuses on two main structures: the PIN photodiode and the pinned photodiode.

2.2.1 Photodiode

Many types of photodiodes exist in CMOS imaging sensors. The most basic photodiode is a PN junction. The photodetection occurs within the depletion area of the diode. Figure 2.2 illustrates the cross-sectional view of a standard PN photodiode. When a photodiode is illuminated by light with energy greater than the band-gap energy, electrons in the valence band are excited to the conduction band by absorbing the photon energy. Vacancies are left in the valence band resulting in hole generation. The generation of electron-hole pairs happens throughout the depletion layer, that is, in both the p- and n-layers of the diode's depletion region. A photocurrent is then generated by the electric field in the depletion layer attracting electrons to the cathode as well as pushing holes to the anode. The current caused by the generation of electron-hole pairs is proportional to the amount of the incident light.

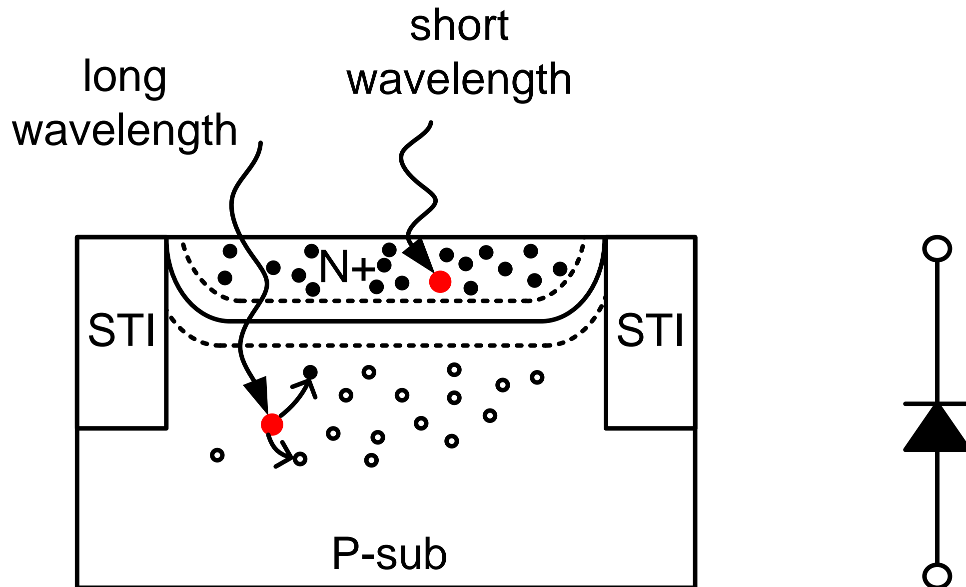


Figure 2.2: Cross-sectional layout view of a standard PN diode

Another popular form of photodiodes is the PIN photodiode. It is constructed by inserting an intrinsic

region in between the P and N layers in order to stretch out the electric field and thus increase the volume of the diode that can absorb photons. This results in more photogenerated current from a fixed amount of light. Figure 2.3 shows a reverse-biased PIN photodiode.

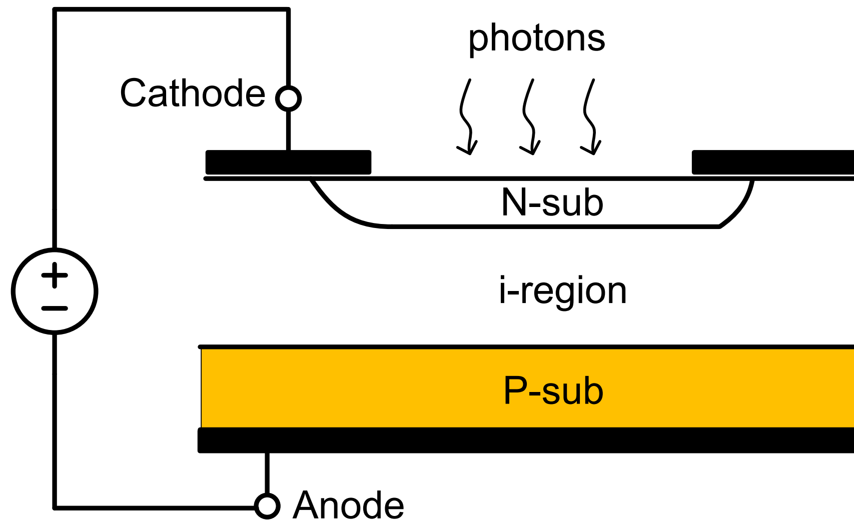


Figure 2.3: Cross-sectional view of a PIN photodiode

There are three operating modes in a photodiode, that is, the photovoltaic mode, photoconductive mode, and avalanche mode. Under a zero-biased condition, the photodiode operates in a photovoltaic mode having a small dynamic range and nonlinear photon-to-voltage generation. Under a reverse-biased condition, the photodiode operates in the photoconductive mode. The reverse voltage increases the width of depletion region (or absorption region) to capture photons and also creates a electric field to sweep the electron-hole pairs in the depletion region. Under a high reverse-biased condition, the photodiode operates in the avalanche mode. The electric field is increased by the high reverse voltage. The velocity of free carriers generated through absorption of a photon is increased in the depletion region. The primary fast-moving electron or hole collides with the silicon lattice and kicks out some electrons creating secondary electron-hole pairs. This collision ionization will keep on repeating in the new generated electron-hole pairs resulting in an avalanche. Consequently, the avalanche photodiode obtains an internal multiplication.

In the early generation of CMOS image sensors, these two types of photodiodes, PN and PIN, were commonly used in 3T pixels, as shown in Figure 2.4. The standard 3T pixel consists of three transistors: a reset transistor, a source follower, and a row select switch. The 3T pixel employing either a PN or PIN diode possessed a larger full-well capacitance, which is desirable, but higher dark current and noise, which are both undesirable. The surface generation of carriers near the top of the chip introduced imperfections in the crystal structure resulting in larger thermal generation of carriers and thus larger dark current.

Two main operating phases of the 3T pixel are described as follows [79, 80]:

- The reset phase. The PN/PIN photodiode is reset by turning on the reset transistor to connect the

cathode node to the V_{DD}. The reset phase charges the photodiode capacitor to reach a voltage of $V_{DD} - V_{TH}$ and is considered as the dark condition. In Figure 2.4, this corresponds to the case when the red trace is flat. The reset transistor can be thought of as a resistor while the photodiode can be thought of as a capacitor. During this reset phase, there will be an associated kT/C noise sampled on the diode. Larger diode area reduces this noise by increasing the diodes's capacitance. The cost for this reduction in noise is less sensitivity to lower light levels.

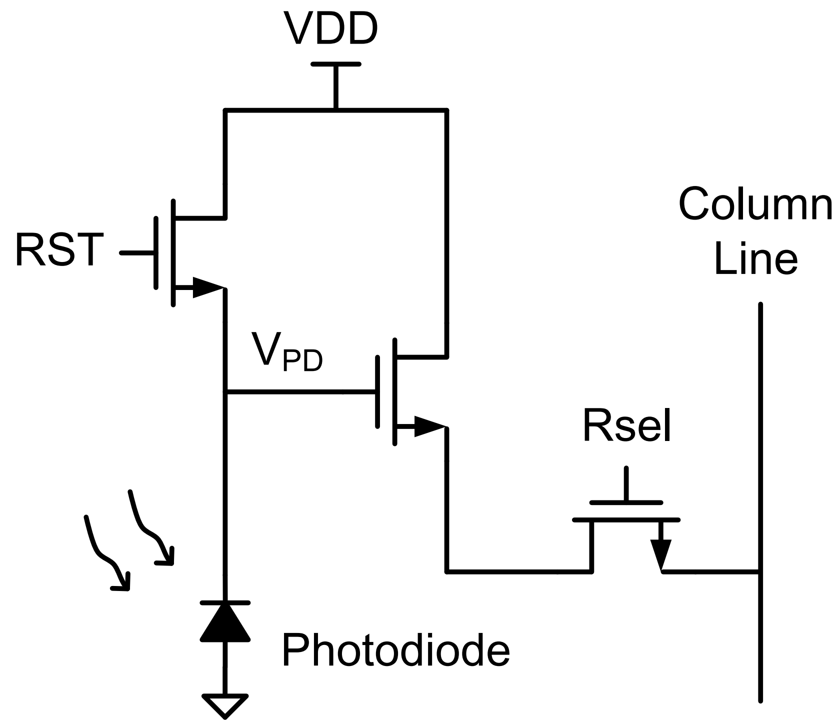
- The charge accumulation phase. The reset transistor is shut off leaving the diode's capacitance charged. The incident photons striking the photodiode causes the photocurrent generation to discharge the photodiode capacitor. In Figure 2.4, this is indicated by the red line indicating the voltage across the diode is dropping linearly. After the exposure time (also called integration time), the row select transistor is switched on and the voltage across the diode is buffered on the column line. One key point is that a darker image results in a higher voltage on the column line while a brighter image results in a lower voltage on the column line.

2.2.2 Pinned Photodiode

At the time of this writing, imaging sensors used for consumer products, such as smartphones or document cameras, don't use either a PN or PIN junction. Rather these devices use a "pinned" photodiode which is discussed here.

A standard 4T pixel with a pinned PD (PPD) is shown in Figure 2.5. The PPD is constructed by adding a thin and heavily doped p+ layer on the top of the n-type diffusion layer. The vertical p+np structure has two PN junctions sharing the middle n-type layer: the p^+/n junction and $n/psub$ junction. The fermi level of the n-type layer is pinned because it's surrounded by p-type. By applying a sufficient voltage to the middle n-type layer, these two depletion regions can be merged resulting in a fully depleted n layer of the PPD. The specific voltage is called the pinning voltage.

The technique of using the pinning layer was initially created in CCD technology for increasing the quantum efficiency and reducing dark current [81, 82]. Implementing the method to CMOS active pixels helped PPDs achieve an extremely low dark current compared to PN junctions. The shallow pinning layer buries the PN junction away from the photodiode surface and moves its depletion region down in the semiconductor substrate. The heavily p-type doping provides high hole concentrations at the surface to maintain the $SiO_2 - Si$ surface in thermal equilibrium through suppressing the thermal generated electrons. As a result, free electrons are absent at the $SiO_2 - Si$ surface resulting in a low dark current [82, 83].



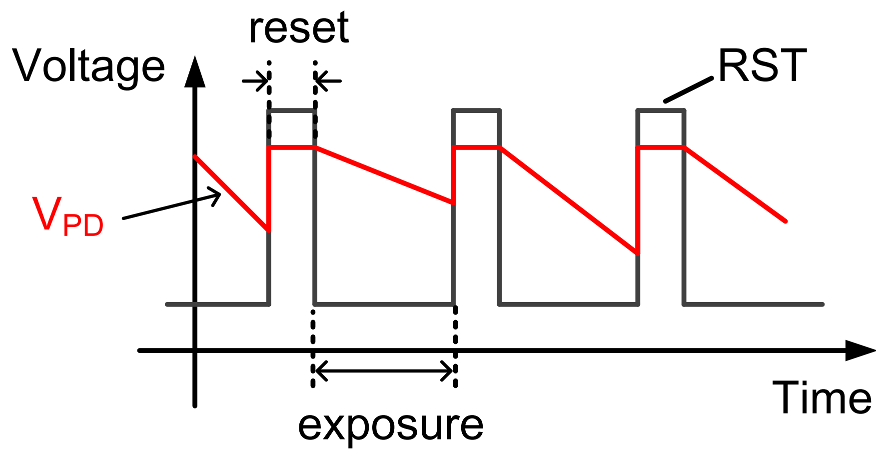


Figure 2.4: A traditional 3T pixel with a timing of reset pulses and pixel signal

2.3 4T Active Pixel Architecture

A standard CMOS 4T pixel is shown in Figure 2.5. It consists of a pinned photodiode (PPD), a source follower (SF), a transfer gate transistor (TX), a reset transistor (RST), and a row select transistor (RSel). Unlike 3T pixels, the additional transistor (transfer gate transistor) is added to separate the photodiode and the source follower. The floating diffusion is connected to the gate of the source follower and the parasitic capacitance is used to achieve a charge-to-voltage conversion. Thus, the transfer gate succeeds to isolate the photo-detection and charge-conversion processes. Both transfer gate and reset transistors are used to reset the photodiode. The reset transistor is also responsible for resetting the floating diffusion (FD) before starting to transfer charges from PPD to the FD node.

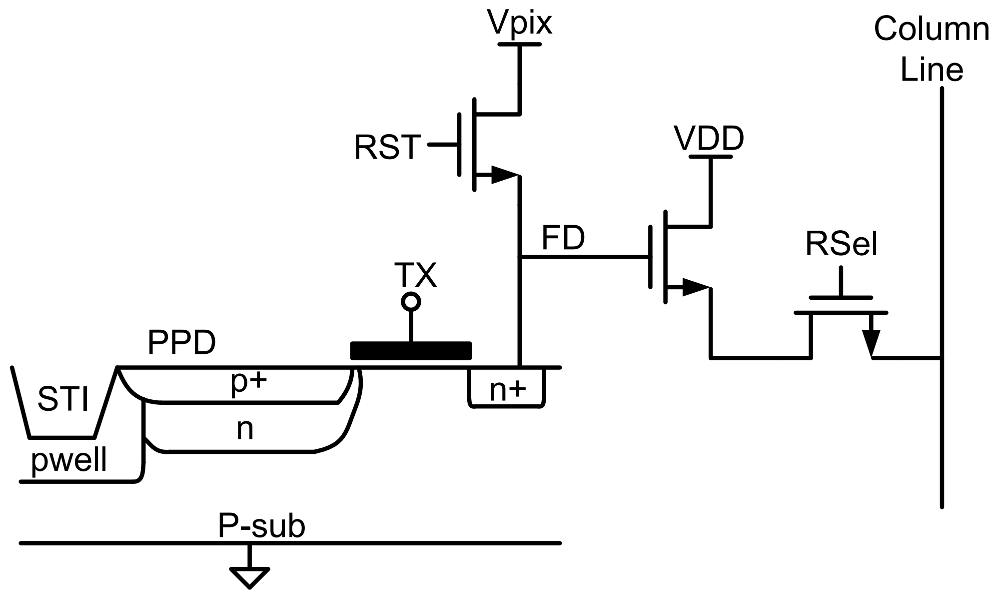


Figure 2.5: A standard 4T pixel

A common operating procedure for a standard 4T pixel is described as follows:

- Photodiode reset step. Unlike the 3T pixel structure, the photodiode's cathode in a 4T pixel needs to turn on two transistors (reset transistor and transfer gate) to be connected to a reset voltage, V_{pix}, for making the photodiode fully depleted.
- Charge accumulation step. Switch off the transfer gate and reset transistor simultaneously to start the charge accumulation. The photocurrent generated by photon absorption is integrated at the photodiode. The maximum number of charges represents the full well capacity (FWC) of the photodiode. Larger photosensitive area means bigger photodiode capacitance, which could give larger FWC. The integration process is kept on until the next time the transfer gate is switched on. The off-state trans-

fer gate plays a significant role in the photodiode dark current. If the transfer gate is not completely turned off, the depletion region under the gate could create a path for dark electrons to discharge the storage capacitor at the floating diffusion. The efficient method is to use a negative voltage to turn off the transfer gate completely [83].

- FD reset step. Turn on the row select switch to prepare for the correlated double sampling[79]. The floating diffusion capacitor is reset by turning on the reset transistor again.
- Reset sampling step. Turn off the reset transistor. The current voltage at the floating diffusion is the sum of the reset signal and noise signal. The first sampling process samples the voltage, $V_{FD1} = V_{rst} + V_{noise}$, into the column analog front-end circuit. The parasitic resistance and capacitance on the column line limits the sampling speed.
- Charge transfer step. Turn on the transfer gate to transfer the charges from photodiode to floating diffusion node. Incomplete transfer can leave some charges in the photodiode, which is defined as image lag [84].
- Pixel sampling step. Turn off the transfer gate. The current voltage at the floating diffusion is the pixel signal plus noise signal $V_{FD2} = V_{pd} + V_{noise}$. The second sampling process samples and subtracts the current signal from the first one. The voltage difference represents the pixel signal without noise, $V_{rst} - V_{pd}$. The "black" pixel has a small difference value and the "white" pixel a large difference value.

2.4 Characterization of CMOS Image Sensors

Most common parameters for measuring pixel performance are described, including fill factor, quantum efficiency (QE), full well capacity (FWC), conversion gain (CG), image lag, and dark current. Some other parameters are used to evaluate the sensor, such as frame rate, resolution, bit depth, modulation transfer function, and different types of noise.

2.4.1 Fill Factor

Fill factor determines the area in which a single pixel can capture light. It is the ratio of pixel detection area to the entire pixel area. For CCD sensors, fill factor is not an issue because of CCD pixels having nearly 100% fill factor [85]. However, the CMOS pixel integrates transistors, resulting in a smaller fill factor. Fortunately, using micro-lens and back-side illumination techniques improve the effective fill factor of modern CMOS pixels to nearly 100%. The fill factor can be expressed by

$$FF = \frac{A_{pd}}{A_{pixel}} * 100\% \quad (2.2)$$

where A_{pd} and A_{pixel} represents the photosensitive area in a pixel and the entire pixel area, respectively.

2.4.2 Quantum Efficiency

Quantum efficiency (QE) is also known as the spectral response. It is a vital pixel parameter to evaluate the quality of photodiodes. It is defined by the ratio of incident photons and charges converted by the photodiode. The spectral response is used to reflect the capability of photocurrent generation in terms of different wavelengths of light. Both doping concentration and geometric arrangement of the photodiode can affect the quantum efficiency.

Overall quantum efficiency in a photodiode is given by

$$QE(\lambda) = N_{sig}(\lambda)/N_{ph}(\lambda) \tag{2.3}$$

where N_{sig} is the charge signal generated in the pixel, and N_{ph} is the total number of incident photons per pixel. Ideally, QE is 100%, meaning that in the pixel area, every photon can generate one electron-hole pair. However, the number of photons absorbed by the photodiode is limited by the effective FF. The surface might be reflecting some incident photons or some photons might be absorbed by metal layers above the photodiode, which makes the photo-generated charges less than expected. The photodiode structure also determines the charge collection efficiency. Thus, QE can be written by

$$QE(\lambda) = T(\lambda) * FF * \eta(\lambda) \tag{2.4}$$

where $T(\lambda)$ is the transmittance of light above a detector, FF is the pixel fill factor, and $\eta(\lambda)$ is the charge collection efficiency of the photodiode.

Therefore, a distinction can be made between the external and the internal QE. The external QE considers only a portion of the total number of incident photons that hit the photosensitive area, which is quantized by the FF. It also considers defects causing a loss of photons, e.g., reflection and absorption by metal lines above the pixel. The internal QE is used to measure how well photons are absorbed and how efficiently the generated electrons are collected [86, 87].

2.4.3 Full Well Capacity

Full well capacity (FWC) defines the maximum amount of charge that can be accumulated in the active area of each photodiode. FWC is expressed by the number of electrons and can be computed by the maximum amount of charges:

$$FWC = \frac{Q_{max}}{q} \tag{2.5}$$

where Q_{max} is the maximum amount of charges held in the photosensitive area, and q is a single electron charge.

The maximum number of accumulated charges in the PPD is given by [88, 89]:

$$Q_{max} = C_{ppd} * (V_{pinning} - V_{blooming}) \tag{2.6}$$

where C_{ppd} is the photodiode capacitance, $V_{pinning}$ is the pinning voltage at the PPD's fully depleted state, and $V_{blooming}$ is the minimum voltage when charges exceed the FWC. In CMOS imaging sensors, two factors can limit the swing of maximum output voltage: the saturation of the readout circuit and the pixel FWC. Therefore, the FWC becomes one of the primary factors to affect the dynamic range of the imaging sensor [90].

2.4.4 Image Lag and Transfer Efficiency

Image lag is caused by an insufficient charge transfer from PPD to FD in a 4T pixel. Ideally, all accumulated charges in the photosensitive area can be transferred to floating diffusion and converted to an electric signal before sampling to the column readout circuit. However, the charge transfer process is not perfect. For example, in a 4T pixel, some electrons are left in the photodiode after turning on the transfer gate. The incomplete transfer leaves some charge for the next frame, which deteriorates the quality of the next image [91].

To avoid the effects of different light sources and PPD geometry, charge transfer efficiency is used for better characterization of image lag. It is defined as the ratio of successfully transferred charges compared to the total amount needed to be transferred in one cycle [90].

Several factors can cause image lag. These factors are transfer time, electric field, trapping effect, and turn-on voltage of the transfer gate [84, 92].

2.4.5 Conversion Gain

Conversion gain (CG) presents the voltage difference converted by a single charge. The conversion gain defines the efficiency of electron-to-voltage conversion in a pixel. In a 4T pixel, the charge-to-voltage conversion happens at the floating diffusion node and the CG depends on the node capacitance at the floating diffusion. It can be computed by

$$CG = \frac{q}{C_{FD}}[uV/e^{-}] \tag{2.7}$$

where C_{FD} is the effective FD capacitance and q is a single electron charge. The equation shows that the conversion gain in a 4T pixel is independent of the photodiode capacitance. Furthermore, a larger CG requires a smaller FD capacitance.

One method to measure CG is to get the photon-transfer-curve [83, 93, 94]. When the temporal noise is dominated by photon shot noise, the noise characteristic is plotted on a log-log graph. It is portrayed as a function of the number of photons, as shown in Figure 2.6. The square root of the average amount of incident photons in a given pixel is equal to the RMS value of short noise [95].

$$log\overline{V_{shot,rms}} = \frac{1}{2} \times log\overline{N} \tag{2.8}$$

where $\overline{N}$ is the average number of photons collected in a given pixel.

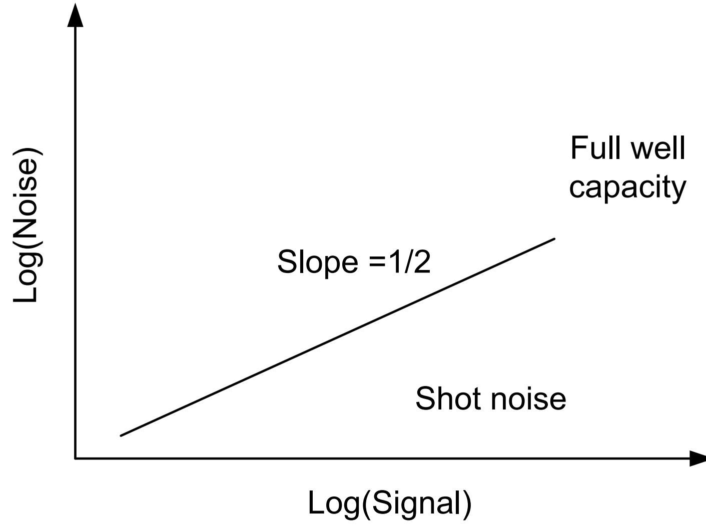


Figure 2.6: RMS shot noise vs input photons on a log-log curve[95]

Assume the voltage at the floating diffusion node is V_{FD}. It can be computed by multiplying the conversion gain and the average number of input photons.

$$V_{FD} = CG \cdot \overline{N} \tag{2.9}$$

Based on Equations 2.8 and 2.9, the CG equation can be rewritten as

$$CG = \frac{\overline{V_{shot,rms}^2}}{V_{FD}} \tag{2.10}$$

2.4.6 Dark Current

When no external light is applied, a photodiode should not generate any current. However, in the depletion region of a PN junction, electron-hole pairs can be thermally generated to cause a small current, which is called dark current [90, 90, 96]. Dark current is dependent on the photodiode structure and temperature. This undesired current is added to the photocurrent generated by photons' absorption. A photodiode with larger dark current gives a lower dynamic range, since the photodiode capacitor accumulates dark electrons. As previous discussed, the pinned photodiode obtains a lower dark current compared to PN/PIN junctions. Dark current is integrated as an undesirable dark charge at the in-pixel storage cell. It is usually measured at room temperature. Furthermore, a non-uniformity issue is caused by the substantial variation of dark current across the pixel array, which is called dark signal non-uniformity.

2.4.7 Responsivity

Photodiode responsivity is defined as the ratio of the photo-current generated by the incident photons to the incoming light power. It is in a unit of A/W and can be expressed by

$$R = \frac{I_{ph}}{P} = QE \cdot \frac{q\lambda}{hc} \tag{2.11}$$

where QE is quantum efficiency, λ is the light wavelength, h is the Plank constant, and c is the light speed in a vacuum.

2.4.8 Dynamic Range

Dynamic range (DR) indicates how well an imaging sensor can capture images that have both bright spots and dark shadows. It is defined as the ratio of saturation level divided by the noise level and measured in decibels, as shown in Figure 2.7. The full-well capacity and the resolution of the readout circuit determine the maximum detectable light. Noise resources such as dark current and shot noise limits the noise floor. The DR can be calculated by

$$DR = 20log(\frac{Q_{FWC}}{Q_{noise\ floor}}) \tag{2.12}$$

where Q_{FWC} is the largest detectable signal at the saturation level (or full-well capacity) of the photodiode and $Q_{noise\ floor}$ is the smallest detectable signal. Both variables are expressed in electrons.

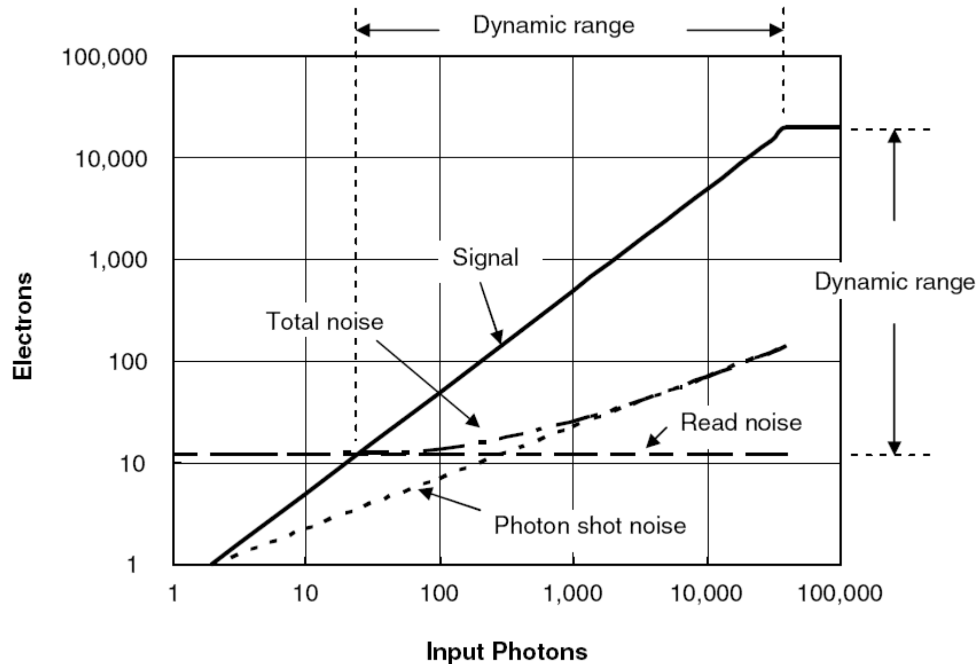


Figure 2.7: The dynamic range waveform [1]

2.4.9 Signal-to-Noise Ratio

Signal-to-noise ratio (SNR) is the ratio between the input signal and the corresponding noise. Unlike the dynamic range, SNR considers total noise sources, including read noise, photon shot noise, and 1/f noise. If the read noise is dominant that includes the noise generated in the column-level readout process, the SNR can be expressed by

$$SNR = 20log(\frac{N_{sig}}{n_{read}})\ [dB] \quad (2.13)$$

Due to the photon collection process in the photodiode follows the Poisson distribution, the photon shot noise can be modeled by the Poisson process and the electron RMS value of photon shot noise is the square root of input signal [1]. Thus, if the photon shot noise is dominant, the SNR equation is expressed by

$$SNR = 20log\frac{N_{sig}}{n_{shot}} = 20log\frac{N_{sig}}{\sqrt{N_{sig}}} = 10logN_{sig}\ [dB] \quad (2.14)$$

When the image sensor only considers shot noise, the SNR is increased with the number of photons collected by the photodiode at 10 dB per decade. Its maximum value is limited by the pixel FWC.

However, when the imaging sensor operates at a low light environment, the dark current shot noise, read noise, and dark signal non-uniformity become dominant, and the increase rate of SNR becomes 20 dB per decade.

2.4.10 Shutter Mechanism

Two shutter mechanisms exist for CIS cameras: rolling shutter and global shutter. The rolling shutter (RS) uses a block readout method, that is, it reads out one line or a group of lines of pixels, while it keeps other lines on the exposure of light. Due to the sequential scanning method, CMOS image sensors with rolling shutter do not need an in-pixel storage capacitor. Each line of pixels must be read out before the image sensor steps into the next exposure period. Thus, different rows of pixels can be exposed for the same amount of time, but they can not be exposed at the same time. Another primary drawback of applying rolling shutter in CMOS image sensors is the image artifacts that remain when fast-moving objects are being photographed [1].

In contrast, the global shutter (GS) takes a snapshot of the target object, so all pixels capture the light at the same time. An extra storage element added in pixel is the key to hold the image signal before the readout process begins. After reading out all pixels, the CMOS image sensor starts the next exposure. Therefore, the global shutter mode enables CMOS image sensors to have continuous images in time, with no image artifacts [1].

2.5 Noise Analysis in CMOS Image Sensors

Two categories of noise sources can be divided into CMOS image sensors: spatial noise and temporal noise. Spatial noise includes dark signal non-uniformity, photo response non-uniformity, and fixed pattern noise.

Temporal noise consists of photon shot noise, thermal noise, and electrical noise from readout circuitry.

2.5.1 Temporal Noise

Temporal noise is also called random noise. It does not depend on the pixel location. Under the same environmental conditions, the temporal noise can result in variations in pixel output from frame to frame.

2.5.1.1 Reset Noise

Reset noise occurs when resetting the floating diffusion or a photodiode through a transistor. It is assumed that the storage capacitance in the floating diffusion node or a photodiode is fixed. We can use an equivalent model of a capacitor with one MOSFET switch to calculate the reset noise. Thus, the capacitor can be charged through the switching-on resistance. Due to the resistor's thermal noise is $4kTR_{on}$ and the noise bandwidth is $\frac{1}{4R_{on}C}$, so the voltage RMS noise, which is called "kT/C" noise, can be expressed by

$$\overline{V_{noise,rms}} = \sqrt{\frac{kT}{C}} \tag{2.15}$$

In image sensors, measuring noise in electrons is useful. The electron RMS noise, which is also called "kTC" noise, can be calculated by

$$\overline{n_{e,rms}} = \frac{C \cdot \overline{V_{noise,rms}}}{q} = \frac{C}{q} \cdot \sqrt{\frac{kT}{C}} = \frac{\sqrt{kTC}}{q} \tag{2.16}$$

Table 2.2 lists kT/C noise and kTC noise of different capacitance at room temperature $T = 300\ K$. A larger capacitor has less reset voltage noise but has more reset electron noise. Thus, in different applications, either the second column or the fourth column can be used as a good reference to help choose the sampling capacitance in the circuit design.

Table 2.2: Reset noise of different capacitance at room temperature $T = 300K$

Capacitance (fF)	**rms noise voltage (kT/C) in uV**	**peak-to-peak noise 6.6*$V_{noise,rms}$**	**rms noise electrons (kTC) in e^-**
1	2034.70	13429.01	12.72
10	643.43	4246.63	40.21
20	454.97	3002.82	56.87
40	321.71	2123.31	80.43
50	287.75	1899.15	89.92
60	262.68	1733.68	98.50
100	203.47	1342.90	127.17
120	185.74	1225.90	139.31
150	166.13	1096.47	155.75
240	131.34	866.84	197.01
1000	64.34	424.66	402.14

2.5.1.2 Read Noise

The noise that arrives from the readout circuitry is defined as readout noise or read noise. It excludes the noise generated from the photodiode. The following items [1] account for the most contributions:

1- Source follower noise: It includes 1/f noise and thermal noise of the in-pixel source follower. Because of tiny pixels and a low noise readout chain, the electrical noise of the readout chain is typically dominated by the source follower noise. To reduce 1/f noise, the ideal choice is to use a maximum gate dimension for the source follower. The smaller size the source follower, the more significant its noise contribution.

2- kT/C noise in the sample and hold circuits (S/Hs): S/Hs are located on the front end of a readout chain. As discussed in the section on reset noise, this noise can be reduced by using a larger sampling capacitor. However, a larger capacitor means more layout area.

3- Amplifier noise: Column amplifiers are widely used to buffer the signal before feeding into the data converter and also amplify the signal when it is needed in low light conditions. Amplifier noise includes flicker noise and thermal noise.

4- ADC's quantization noise: The column-level A/D converters aim to complete the digitization process. The finite signal-to-noise ratio of ADCs introduces quantization noise.

2.5.1.3 Shot Noise

Shot noise comes from fluctuations in current caused by the discrete nature of charges, electrons or holes. The random arrival of photons causes a photo current, which produces photon shot noise. The random generation of electrons and holes within the depletion region of the photodiode causes dark current shot noise.

Typically, the statistical distribution of shot noise can be described by a Poisson distribution, which contains a standard deviation equal to the square root of the mean value ($\sigma = \sqrt{\mu}$) [80, 90].

In a typical photodiode with a dark current density (J_{dark}) and a photo-sensitive area (A), the variance of dark current shot noise in electrons can be calculated over an integration time, t_{int}.

$$\overline{n_{dark}^2} = \frac{J_{dark} A t_{int}}{q} \tag{2.17}$$

The variance of the photon shot noise in electrons can be calculated by

$$\overline{n_{ps}^2} = QE \cdot P_0 A t_{int} \tag{2.18}$$

where QE is the quantum efficiency, P_0 is the photon flux ($photons/cm^2 \cdot s$).

Thus, the total RMS shot noise in electrons for the photodiode is expressed by

$$\overline{n_{shot}} = \sqrt{\overline{n_{dark}^2} + \overline{n_{ps}^2}} = \sqrt{\frac{J_{dark} A t_{int}}{q} + QE \cdot P_0 A t_{int}} \tag{2.19}$$

2.5.2 Spatial Noise

2.5.2.1 Fixed Pattern Noise

Fixed pattern noise (FPN), the first type of spatial noise, is a time-invariant noise. Under the uniform illumination, device mismatches result in the variation of the pixel output, referred to as FPN. Two different sources in CMOS image sensors can generate FPN.

The first source of FPN involves the variations between individual pixels. Ideally, each pixel is identical in the pixel array. The threshold variation and source follower's offset in each pixel result in pixel FPN. It can be removed by column-level correlated double sampling technique [1].

The second source of FPN is the variation of column readout circuitry, including column amplifiers and column ADCs. Column FPN is more noticeable and causes tripes in the produced image. To eliminate column FPN, an average dark image or a different dark image can be used to calibrate column FPN by subtracting a dark image from all captured images [1].

2.5.2.2 Photo Response Non-Uniformity

Photo response non-uniformity (PRNU) is a spatial noise that comes from a light source. PRNU might be caused by a mismatch in optical properties between pixels or a mismatch in the charge-to-voltage conversion capacitance.

A mismatch in optical properties is typically found on a larger spatial scale in the sensor and is often determined by the combination of lens and sensor. For example, the angle of incidence of the light is different in the center of the array and at the side of the array, which may cause less light to reach the pixels nearer to the side. Less light reaching the pixel causes a gradient in the sensor response from the center to the edges of the sensor.

Mismatches in the conversion capacitance are different, depending on the pixel structures. For a 3T pixel, the mismatch occurs in the photodiodes. For a 4T pixel, the mismatch happens in floating diffusions. These mismatches are wholly determined by the processing and are typically in the order of $1 - 2\%$ RMS of the capacitance, which results in a spatial noise contribution that is zero in darkness and scales with the signal [1].

2.5.2.3 Dark Signal Non-Uniformity

Dark signal non-uniformity (DSNU) is produced by the image sensors in darkness. Typically, the dark signal is dominated by the signal caused by photodiode dark current. The dark current differs from pixel to pixel and depends on temperature and integration time [1, 81].

2.6 Radiation Effects on CMOS Technology

This section describes the most common outcomes caused by radiation on devices and circuits in standard CMOS technologies. It begins with a brief discussion of the effects of radiation from high-energy particles, namely displacement damage (DD) and single events. There is also a description of the total ionizing dose (TID) effect, which includes the formation of oxide-trapped charges and leakage paths in field oxides.

2.6.1 Single-Event Effects

High-energy particles penetrating semiconductor devices can cause single-event effects (SEEs), as shown in Figure 2.8. Radiation resources such as solar wind, galactic cosmic rays, and radiation belts can introduce SEEs. Digital circuits such as memories, processors, and FPGAs are most sensitive to SEEs. Advanced CMOS technologies with smaller channel lengths have become even more sensitive because of the smaller node capacitances and lower power supplies [97].

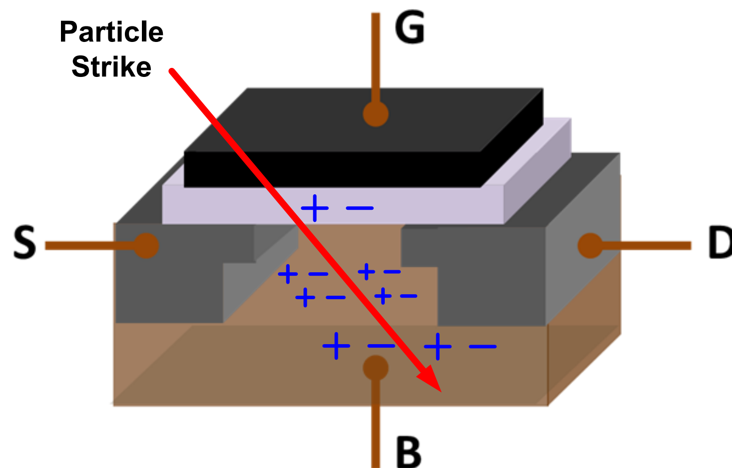


Figure 2.8: A penetration of a high-energy particle through a MOSFET

As mentioned in Reference [98], the SEE mechanism is comprised of three fundamental processes:

1- Charge generation occurs when a high-energy particle passes through the semiconductor. EHPs are created along with the particle moving path to produce free carriers.

2- Charge transport occurs when, by diffusion or by drift, the electric field moves charges from SEE-induced EHPs, to adjacent devices such as PN junctions, while those EHPs can also recombine.

3- Transient disturbance or circuit response occurs when a strong electric field in the sensitive region collects charges. These additional charges on the sensitive node can change the node voltage resulting in voltage propagation through the circuit.

SEEs can be classified into two categories [97]: destructive and non-destructive. Potentially destructive SEEs include single event latch-up (SEL), single event snap-back (SESB), single event burnout (SEB), single event gate rupture (SEGR), and single event dielectric rupture (SEDR). They can permanently affect CMOS devices and circuits. Non-destructive SEEs include single event upset (SEU), multiple bit upset (MBU), single event functional interrupt (SEFI), and single event transient (SET).

2.6.2 Displacement Damage

High-energy particles such as heavy ions, protons, as well as neutrons, can displace atoms from their positions in a semiconductor's lattice. The collisions generate vacancy-interstitial pair (VIP) defects, which are known as displacement damage (DD), as shown in Figure 2.9.

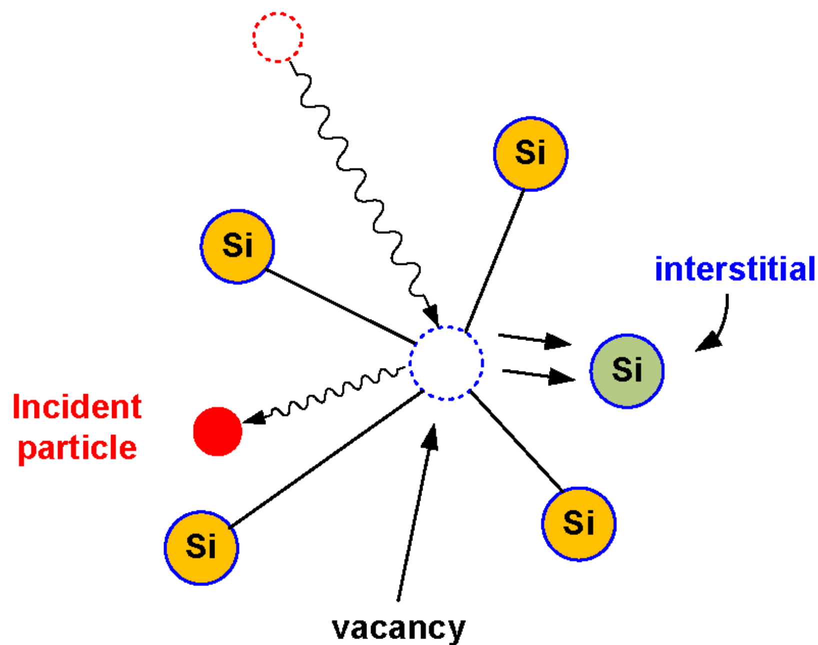


Figure 2.9: The collision between a silicon atom and high-energy particle creates displacement damage

DD-induced VIP defects in a crystal lattice could be either simple or complex[99]. A simple defect occurs when only a few atoms in the lattice are displaced. Complex defects result from longer chains of disordered atoms.

Figure 2.10 illustrates five different processes of DD-induced vacancies:

1- Electron-hole pairs (EHP) are generated in deep-level traps. Electrons in the valence band are promoted to trap levels and then to the conduction band.

2- The recombination of EHPs also come from deep traps. The recombination process happens when an EHP is spatially close to the site of defects.

3- Some carriers can be trapped temporarily in some shallow-level traps. For CCD sensors, this process could decrease the efficiency of transferring charges in the CCD pixel array.

4- The compensation process may be caused by deep- or shallow-level traps. The trap centers compensate for acceptors or impurities in the semiconductor lattice. The equilibrium concentration of majority carriers can be reduced by the compensation processes.

5- A tunneling process can also be the result of radiation-induced defects or traps. The reverse current of junction diodes can be increased by carriers' tunneling.

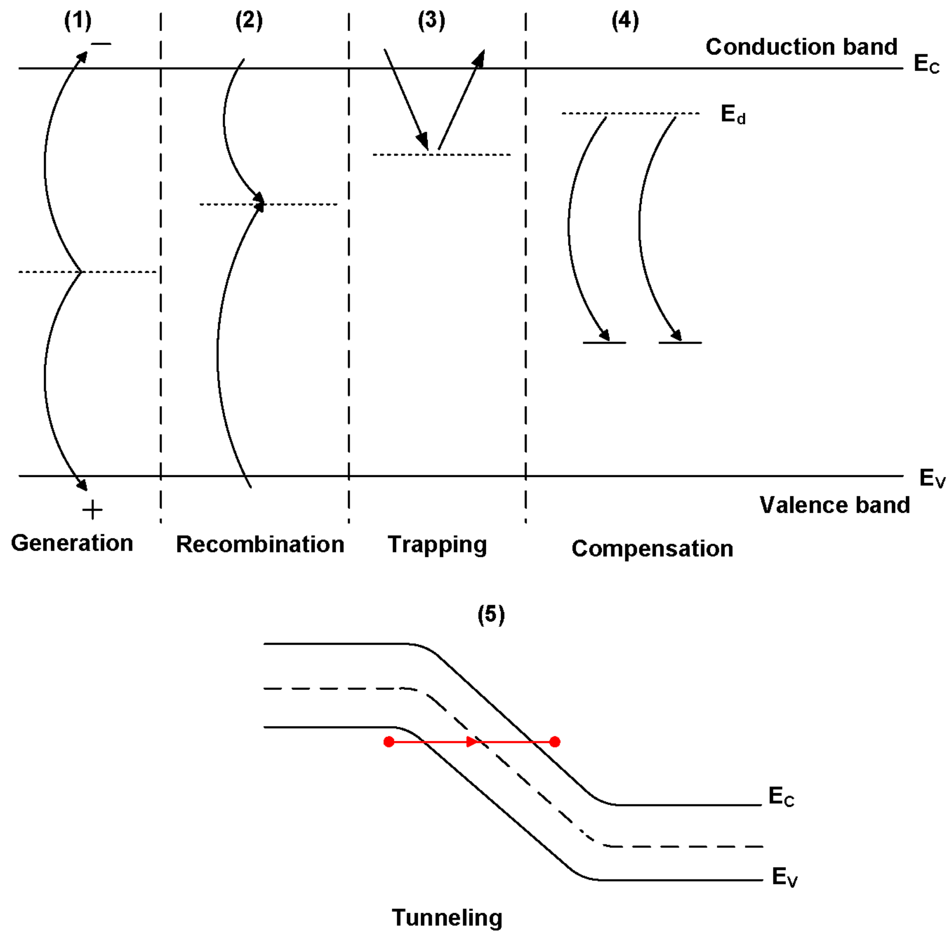


Figure 2.10: Five processes of DD-induced vacancies in the CMOS process [100]

2.6.3 Total Ionizing Dose Effects

This Section discusses the topic of total ionizing dose (TID) effects on CMOS devices, which is the main concern in this dissertation. Sub-section 2.6.3.1 addresses radiation interaction with solids, and EHP generation in the MOSFET oxides. Recombination processes that occur immediately after EHP generation are discussed in 2.6.3.2. Subsection 2.6.3.3 introduces electron tunneling through the oxide and 2.6.3.4 treats

the transport process of TID-induced charges in SiO_2. The formation of oxide trapped charges and interface traps is addressed in 2.6.3.5 and 2.6.3.6, respectively. Figure 2.11 illustrates a summary of the TID formation on the silicon dioxide interface. The final subsection 2.6.3.7 discusses the formation of leakage paths in field oxides induced by TID effects.

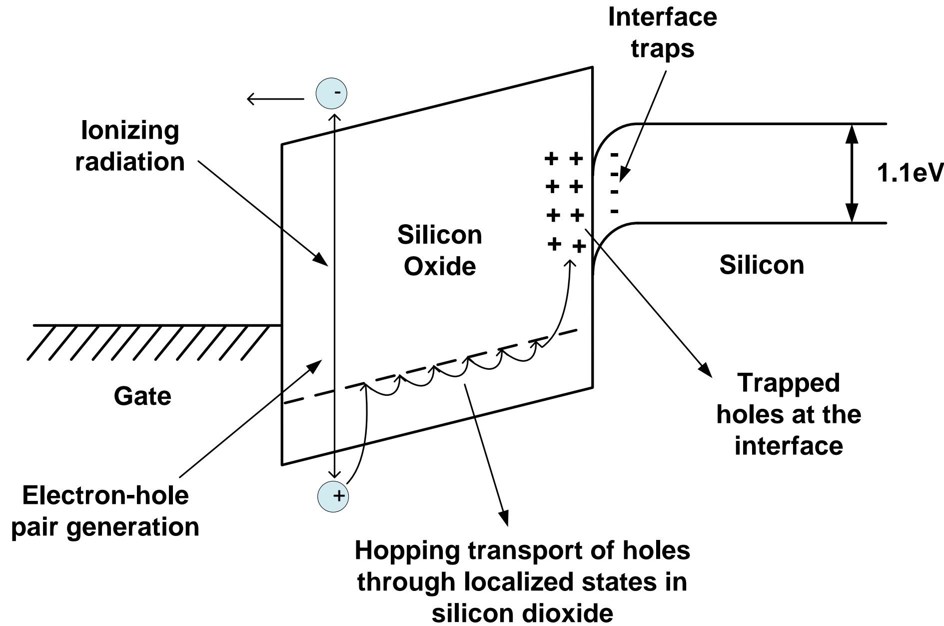


Figure 2.11: Five different formations of TID on the silicon dioxide interface [101, 102]

2.6.3.1 Generation of Electron-Hole Pairs

Electron-hole pairs are produced by the interaction of ionizing radiation and semiconductor solids. EHPs are produced in proportion to how much energy the material received [103]. The primary process is called Coulomb scattering. In this process, an electron at the outer shell is ejected from the atom causing a loss of energy in incident particles [104]. As the particle passes through the material, EHPs are continuously created.

EHPs can also be generated when photons interact with semiconductor solids, typically by Compton scattering. Compton scattering occurs and produces energetic electrons and ionized atoms from the collision between photons and atoms in the semiconductor solid. As previously discussed, the Coulomb scattering process occurs by the interaction of energetic electrons and the solid. Thus, a typical TID testing approach is to use a Co^{60} gamma ray to create EHPs [105].

Linear energy transfer (LET) describes the generation efficiency of electron-hole pairs. Particle energy, particle mass and the material density can influence LET. The unit of LET can be $MeV - cm^2/g$ or $MeV - cm^2/mg$.

The total ionizing dose (TID) rate is the energy induced by incident particles causing the production of EHPs in the semiconductor material. The units for TID is radiation absorbed dose (rad) or gray (Gy). One gray is equivalent to one hundred rads [105]. Additionally, the TID rate is also determined by the target material.

2.6.3.2 Recombination

Some TID-induced EHPs can recombine immediately after generation. The initial recombination time is less than a few picoseconds. The mobility of electrons is relatively high, comparing to holes. For example, the electron mobility in silicon oxide is between 20 to 40 $cm^2/V \cdot s$. The potential of the transistor gate (electric filed in oxide) and device temperature can influence the mobility of electrons. A positive gate voltage can quickly sweep electrons from the oxide under the channel. However, a saturation velocity exists for electrons at a higher electric field, $10^7 cm/s$ [102].

Some holes are left without recombination [106–108]. The number of unrecombined holes is influenced by particle energy and gate voltage. Figure 2.12 shows different radiation sources versus the fraction of unrecombined holes.

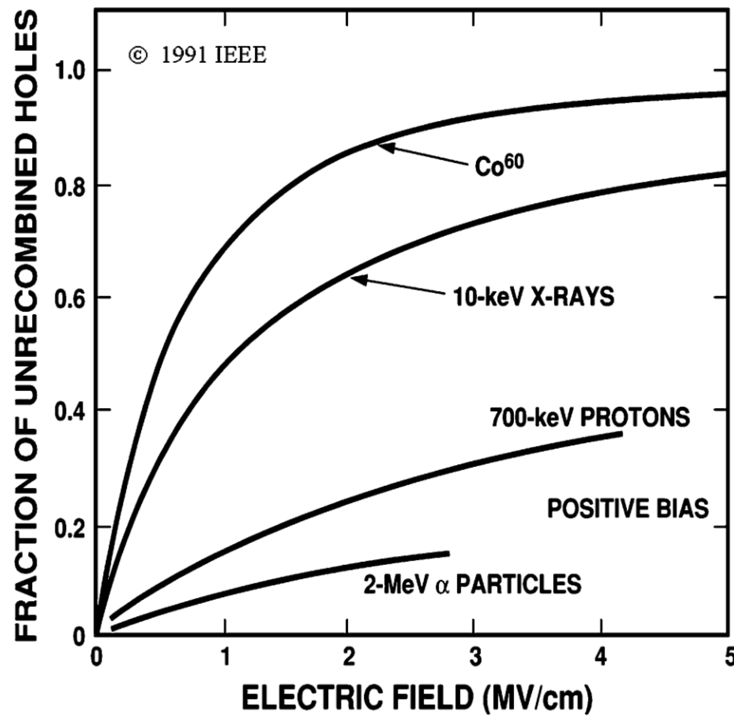


Figure 2.12: Fractional unrecombined holes versus electric field in terms of different radiation resources radiation [108]

2.6.3.3 Tunneling

Tunneling is the movement of electrons from the silicon to $SiO_2 - Si$ interface [109–112]. The tunneling electrons can neutralize the oxide-trapped carriers. The spatial distribution of trapped holes must be necessary to be close to the $SiO_2 - Si$ interface to activate the tunneling process. The maximum distance is approximately 5 nm [105].

2.6.3.4 Hole Transport to Silicon Oxide Interface

Holes that do not recombine can transport through the oxide toward the $SiO_2 - Si$ interface or the gate oxide interface in MOS technologies depending on the electric field [113]. Two mechanisms can introduce this transport process: Polaron hopping and multiple trapping [102, 106, 114]. The Polaron hopping mechanism moves holes by hopping between localized shallow trap states in the oxide. Hole hopping can cause a lattice and local electric field distortions. The multiple trapping mechanism moves holes through the conduction band between trap levels. These two mechanisms for hole transport are illustrated in Figure 2.13.

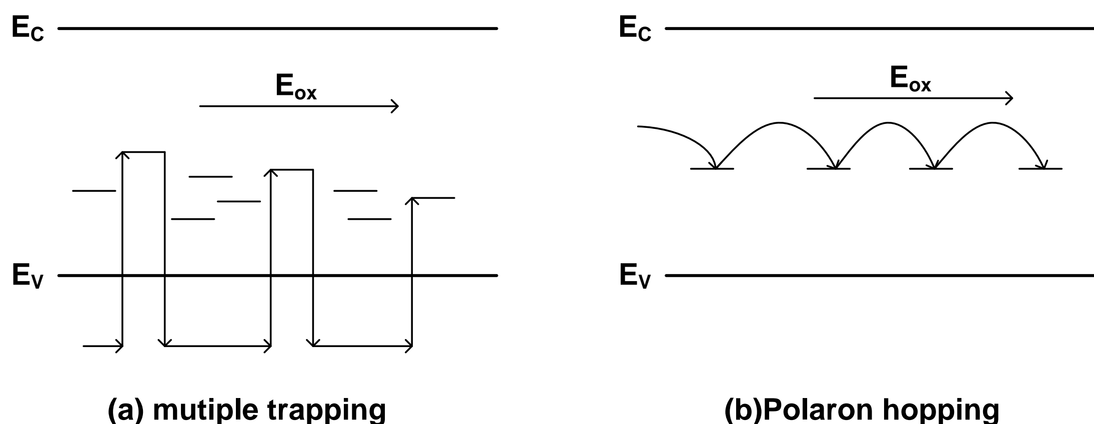


Figure 2.13: Two mechanisms of hole transport in silicon dioxide [106]

2.6.3.5 Oxide-Trapped Charge

After the hopping transport process, holes can be trapped in long-term trapping sites close to the silicon dioxide interface, resulting in an oxide defect in SiO_2, which is called an oxygen vacancy. This has been verified by Electron Spin Resonance. The capture efficiency depends on the electric field, temperature, and CMOS technology [102].

Oxygen vacancy defects in silicon dioxide, which induces hole trapping, are called an E' centers. Figure 2.14 shows the formation. The weak $Si - Si$ bond is broken by the trapped hole resulting in the creation of an E' center. The most common type of E' centers is the E'_1 center [115], which has been considered responsible for the oxide-trapped charge in silicon dioxide. The positive structure is the E'_1 center with a positive charge.

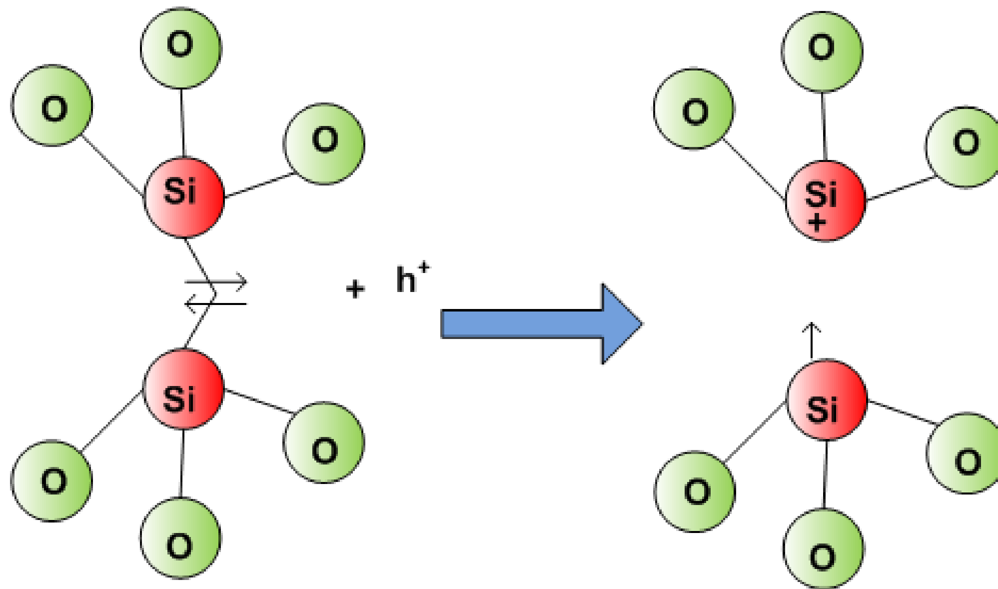


Figure 2.14: Mechanism of E' center formation [106]

E' centers that are close to the silicon oxide interface are called border traps. If the E' center is close enough (less than 3 nm), charges can be exchanged between border traps and silicon through electron tunneling.

Threshold voltage of MOSFETs is shifted by oxide trapped carriers and the variation is proportional to the square of the thickness of the silicon dioxide [116]. Since advanced CMOS technologies continue to shrink the the thickness of the gate dioxide, the charges trapped in gate oxide are dramatically reduced. However, the isolation field oxides are still thick in the range of $300 - 450$ nm. Thus, the significant issues caused by TID in sub-micron CMOS technologies are the trapped charges and leakage currents in field oxides.

The TID annealing process includes two mechanisms: electron tunneling and hole neutralization. The annealing process depends on three factors: time, temperature, and electric field [117].

Electron tunneling is the process by which electrons in the substrate tunnel into oxide and neutralize holes. This mechanism is a long-term annealing process, which is highly dependent on electric field condition and oxidation process.

Hole neutralization is the process in which oxide-trapped positive charges are neutralized by thermal emission of electrons from the valence band of the silicon dioxide. This neutralization mechanism is temperature and electric-dependent.

2.6.3.6 Interface Trapped Charge

Interface trapped charges are also known as interface traps or interface states. The generation of interface states is another process that occurs at the silicon dioxide interface.

Interface traps result from a silicon structural imperfection in the silicon. In theory, each Si is bonded to four Si atoms in a silicon lattice structure. At the surface, most Si atoms are bonded to oxygen, some bond to hydrogen, and some are unbonded. Interface traps are trivalent Si atoms with an unpaired electron in the fourth dangling orbital. Reference [118] developed a model to explain the formation of P_b center defects, which have been considered responsible for generating the interface traps.

Depending on the trap location and external bias situation, interface traps at the oxide interface can be acceptor-like, donor-like, or neutral. Thus, the interface traps can increase the leakage current, degrade carrier mobility, and shift the threshold voltage [102, 117].

Figure 2.15 shows the influence of interface trapped charges in the IV curves of NMOS and PMOS transistors.

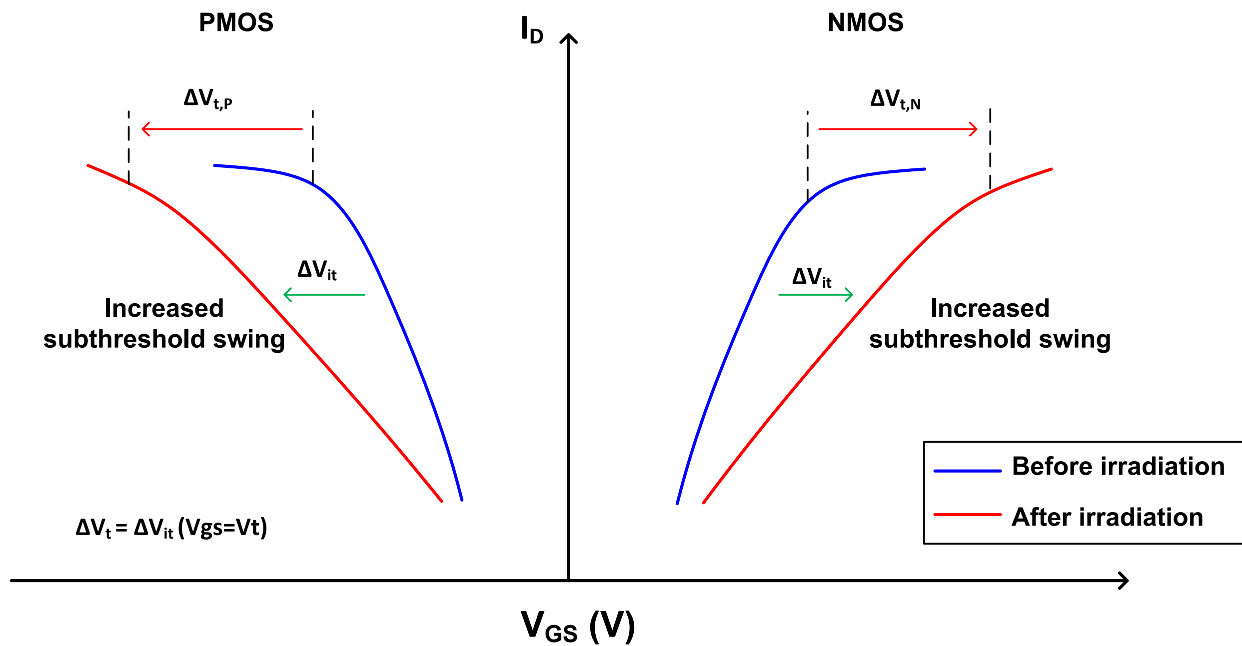


Figure 2.15: Interface trapped charges affect the subthreshold swing of NMOS and PMOS [107]

2.6.3.7 Field Oxide Effects

An increase of TID-induced off-state current in the field oxides (FOX) becomes a primary issue when the threshold voltage shift is diminished by using advanced CMOS technologies with ranges of less than a flew nanometers for gate oxide thickness. Generally, the thickness of isolation field oxides is $100 - 500$ times as high as that of the gate oxide. Reference [119] reported that CMOS technologies with a channel length less than 130 nm have fewer problems with FOX leakage. However, the TID still causes an increase of off-state current in the larger I/O transistors [120].

CMOS technologies have two common types of isolation oxides: local oxidation of silicon (LOCOS) and shallow trench isolation (STI). Figure 2.16 shows the two leakage paths in STI oxides. The off-state leakage from drain to source in an N-type transistor is the path marked "1". The trapped charges at the silicon-oxide interface form the path along the sidewalls of the STI. Figure 2.17 shows the effects of TID on IV curves of an NMOS transistor in a 250 nm width and length. The subthreshold current becomes severe in a higher TID dose making the transistor suffering a turn-off issue [121]. Fortunately, this intra-device leakage path does not exist in PMOS devices since it located in an N-well region.

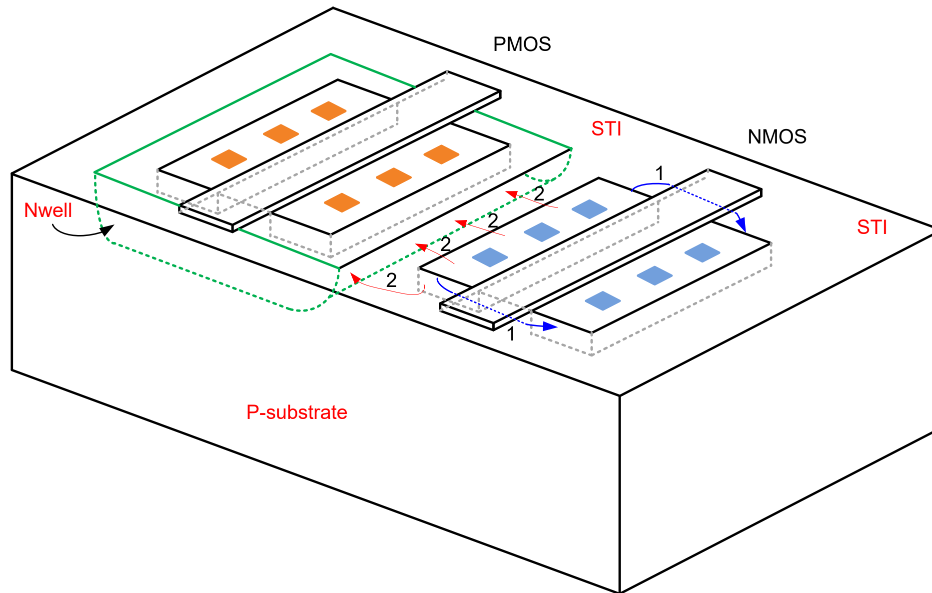


Figure 2.16: TID induces two leakage paths in MOSFETs

The other leakage paths caused by trapped charges at the bottom of STIs are NMOS-to-NMOS (or device-to-device) and NMOS-to-PMOS (or device-to-N-well) paths. The leakage path from NMOS active region to the PMOS N-well is marked "2" in Figures 2.16. Figure 2.18b illustrates the cross-sectional view of this leakage path. The N-well of a PMOS is tied to the high voltage level. The source or drain of an NMOS has a low voltage level. The trapped charges at the $Si - SiO_2$ interface can result in a leakage path between active regions of the NMOS to an adjacent N-well. The leakage path between the device to device is shown in Figure 2.18a. The trapped charges form a leakage path between active regions of two adjacent NMOSs.

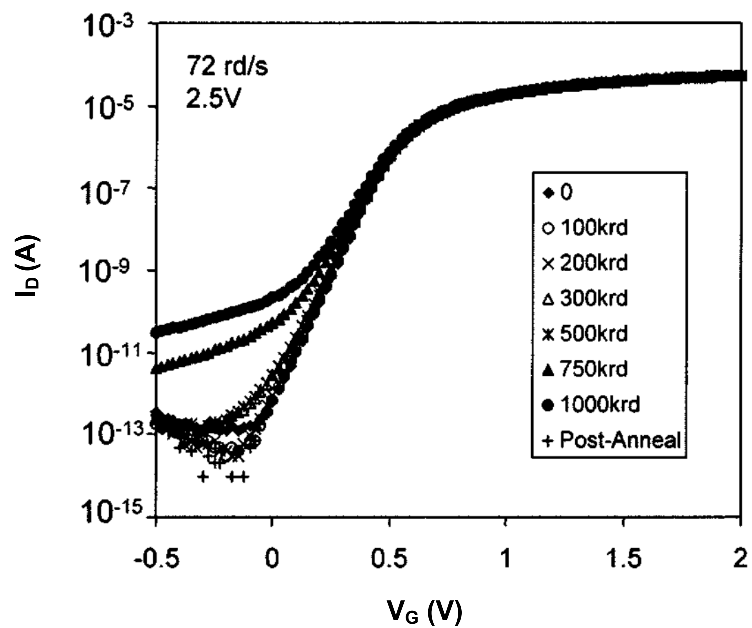


Figure 2.17: Drain current curves for an N-channel transistor with a $250\ nm$ **width and length [121]**

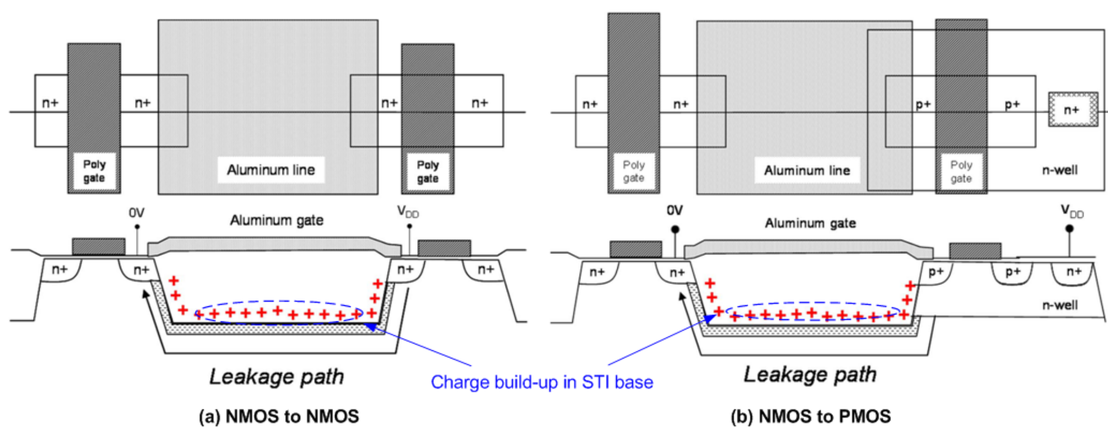


Figure 2.18: Two leakages path between devices caused by TID [107]

2.6.4 Radiation Effect on CMOS Sensors

The previous discussion focused mainly on the radiation effects on MOSFET devices and circuits. Three primary TID effects on standard CMOS technologies are the shift of threshold voltage, leakage currents in NMOSs, and N-channel inter-transistor [122]. Those radiation-induced issues also occur in peripheral circuits in CMOS image sensors. Furthermore, as a highly integrated system, the CMOS image sensors operating in a harsh environment must give the pixel array radiation hardness.

Generally, CISs have a higher radiation tolerance with respect to CCDs because CCDs have a radiation-induced loss of charge transfer efficiency and sensitive pixel structure [123–125]. CMOS image sensors have become preferable in radiation-tolerance imaging systems. Many studies have been conducted on the radiation characterization of CISs [126–141] for specific applications in radiation harsh environments.

After reviewing these publications, it can be concluded that the primary degradation in photodiodes caused by TID is the increase of dark current. Table 2.3 shows several on the analyses of the dark current induced by TID in CMOS image sensors.

Table 2.3: Publications on the analysis of TID induced dark current

Reference	Pixel Pitch	Process	Maximum Total Dose	Dark Current at Maximum Total Dose	Pixel Type
[126]	25 μm	0.7 μm	21 $krad$	45 nA/cm^2	PD
[138]	50 μm	1.2 μm	10 $krad$	1.5 nA/cm^2	PD
[139]	26.4 μm	1.2 μm	10 $krad$	6 nA/cm^2	PD
[140]	25 μm	0.5 μm	22.5 $Mrad$	0.8 V/s	PD
[141]	20 μm	0.5 μm	5.5 $Mrad$	60 nA/cm^2	PD
[128]	16.2 μm	0.35 μm	30 $Mrad$	~20 nA/cm^2	PD at a 3T pixel
[129]	25 μm	0.5 μm	10 $Mrad(Si)$	1.4 nA/cm^2	PD at a 3T pixel
[131]	10 μm	0.18 μm	100 $krad$	750 e^-/s	PPD at a 4T pixel

The following discussion focuses on dark current in a pinned photodiode (PPD) without ionizing radiation. Three main elements constitute the PPD dark current: a surface leakage current, bulk leakage current, and depletion region leakage current. The transfer gate MOSFET can also affect the PPD dark current through the turn-off gate voltage, $V_{off,TG}$. When $V_{off,TG}$ is not small enough to turn off the transfer gate, the TG operates in a weak inversion or the subthreshold region. The TX depletion region can merge with the PPD depletion region, resulting in a large contribution to the PPD dark current. Thus, to reduce the TG contribution to PPD dark current, $V_{off,TG}$ is better to give a negative value to completely turn off transfer gate and put it in the accumulated region [137, 142].

Furthermore, the layout design of the pixel, electric field, temperature, and potential distribution within the pixel also contribute to the PPD dark current [143, 144].

Several factors cause an increase of the PPD dark current along with increasing the total ionizing dose level reported in [145–150]. The first factor is the thick SiO_2 layer above the pinning layer, also called pre-metal dielectric (PMD). More trapped holes induced by ionizing radiation can extend the depletion region of

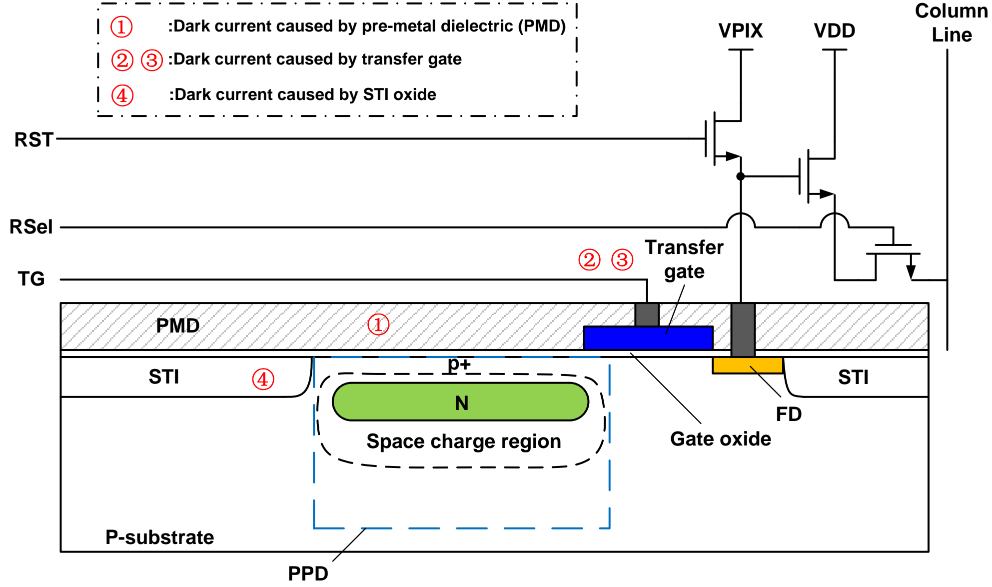


Figure 2.19: Cross-sectional view of a 4T pixel showing the factors of TID-induced dark current

the PPD to the top of the silicon dioxide interface by affecting the doping concentration of the pinning layer. A large diffusion current on the top $Si - SiO_2$ interface is also introduced by an increase in interface state density, which becomes more massive than the diffusion current generated by neutral bulk by increasing the total radiation dose level. As a result, the dark current becomes dependent on the area of the pinned photodiode.

Meanwhile, both the size of transfer gate and its gate voltage at the “off” condition have a significant influence on the TID-induced dark current in the photodiode. This is because the biasing region of the TG has a chance to merge with the PPD depletion region, resulting in a leakage current[132].

The TID can also cause a formation of a lateral leakage path to raise the dark current[146]. A parasitic transistor is introduced by the trapped charges in the sidewall STI oxide of the TG.

The STI oxide surrounding the PPD is another significant factor in the increase of TID-induced dark current. More trapped charges or holes can expand the depletion region of the PPD, which contains more generation centers used to increase the PPD dark current.

A cross-sectional view of TID-induced dark current in the 4T pixel is shown in Figure 2.19.

Concerning the mitigation of dark current induced by the TID, two main aspects could be used to make the 4T pixel radiation hardness. The first aspect is to mitigate the effects from the transfer gate. An enclosed TG layout can remove the lateral leakage path. A negative voltage can be used to turn off the transfer gate and to make it an accumulation region. A post-irradiation soft reset of the PPD can suppress the dark signal by using the reset transistor [147].

The second method to reduce the TID-induced dark current is to surround the STIs with a P-well structure and to increase the space between the N-implant to the STI [151], as shown in Figure 2.20.

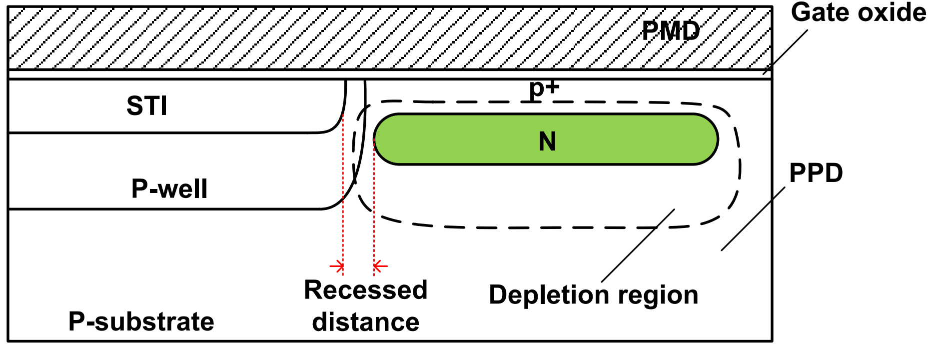


Figure 2.20: Recessed distance between sidewall STIs and buried n-layer in the PPD

Moreover, different types of oxides can be used to surround the pinned photodiode with a slow buildup of interface states. These methods can result in a higher immunity to the TID effects.

2.6.5 Radiation Hardening by Design against TID Effects

Radiation hardening techniques can be mainly divided into two categories. Radiation-hardening-by-process (RHBP) uses a specialized process to fabricate integrated circuits, which is both expensive and an older technology node. When prioritizing low fabrication cost, higher speed, and higher integration density, radiation-hardening-by-design (RHBD) is a better solution to mitigate the TID effects on CMOS image sensors.

Two primary defects caused by TID are the threshold voltage shift and leakage current. The trapped or created holes in the gate oxide are the primary factor that influences the magnitude of the TID-induced threshold voltage shift. The gate oxide thickness determines the number of holes caused by the TID. It has been demonstrated that thinner gate oxide causes a smaller V_{TH} shift for MOSFETs. This is because these holes trapped in a less than 12 nm gate oxide have a higher probability of tunneling through the oxide before converting to interface states.

For eliminating the TID-induced leakage current, the RHBD method is used to avoid the current path between NMOS's source and drain diffusion region. Several possible ringed NMOS layouts are shown in Figure 2.21. Radiation-tolerant thin gate oxide surrounds either the source and drain, or both, and also covers the active region under the gate without $n+$ doping. The enclosed layout transistor (ELT), also called edge-less transistor, has proved to be a very effective method where one of the diffusion, source or drain, is surrounded by the other. Furthermore, using a p+ guardring with minimum-width p+ diffusion is an effective technique to remove the TID-induced leakage current paths between transistor to transistor or between n-well to a transistor.

Hence, this dissertation combines the ELT NMOSs and guardrings in the 0.18 μm CIS process to overcome the TID dose up to 300 krads.

For the radhard consideration in 4T pixels, placing a field plate above the overlapping area of the P-well

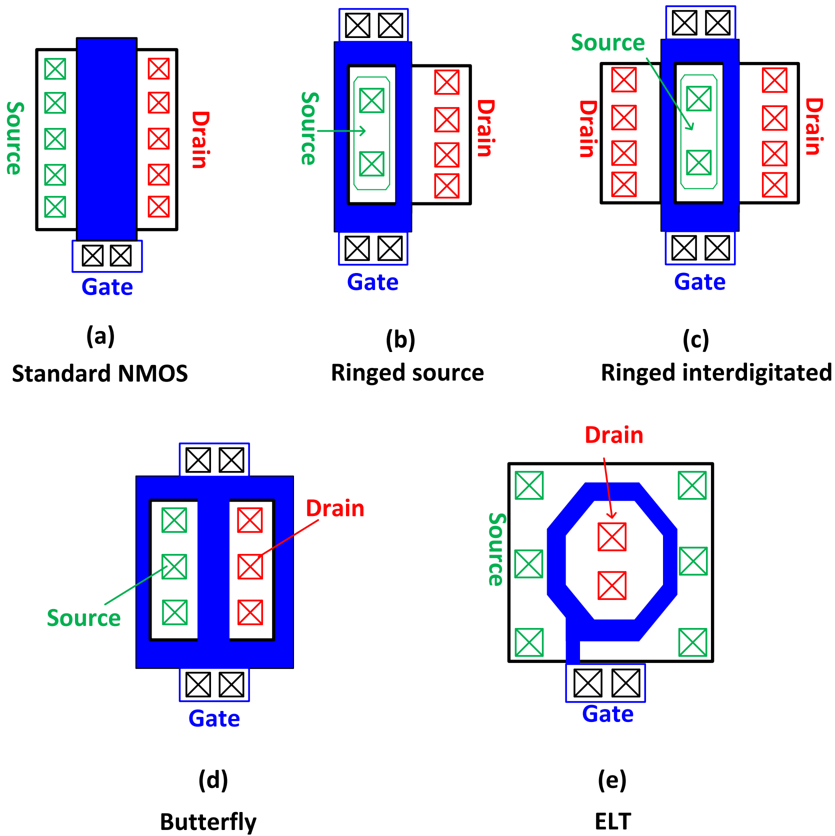


Figure 2.21: Standard NMOS layout and four different enclosed NMOS layouts

and PPD depletion region, as shown in Figure 2.22, could be an effective approach. The field plate is the polysilicon layer. When the voltage of the field plate is set to make the surface of the channel accumulated, the interface becomes inactivated. Then, the TID-induced dark current at the peripheral area is strongly suppressed, as mentioned in [141, 152]. Furthermore, increasing the distance between the STI and the edge of the pinning layer is an effective RHBD method, as proved in [130].

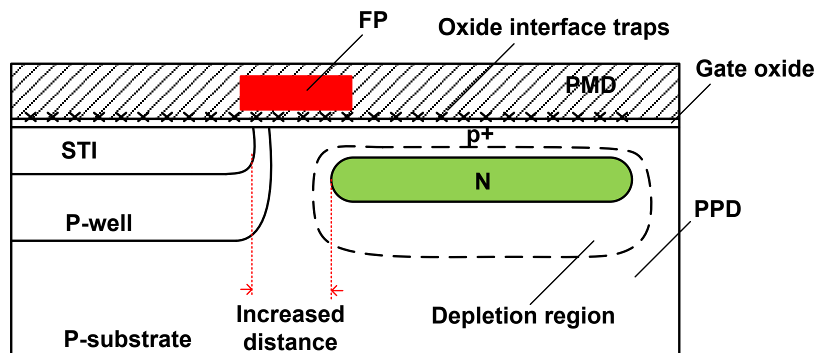


Figure 2.22: Cross-sectional view of an PPD with increased recessed distance and field plate

One of the major penalties of these RHBD techniques mentioned above is the increase in size of the layout of all circuit components. The pixel pitch cannot be less than 10 μm in the 0.18 μm process. For the high image format requirement, the area of the pixel array accounts for most of the sensor chip area. On the other hand, the layout area is limited for peripheral circuits, which makes their design more challenging.

This dissertation has offered three recommendations for the proposed CIS architecture to raise its radiation tolerance to a total dose level of 300 $krads$.

1- Employ the physical design techniques of enclosed N-channel transistors (3.3 V and 6.5 nm gate oxide thickness) and P-type guardrings in pixels and column-level S/Hs.

2- Use P-type guardrings to surround 1.8 V N- and P-type transistors (4 nm gate oxide thickness) in readout and clock circuitry.

3- Use 1.8 V combinational logic circuits in memory banks, row decoders, and other logic circuits.

Chapter 3

High Frame Rate CIS with Radhard Megapixels

This chapter discusses a high frame rate scheme for radhard megapixel CMOS imaging sensors. It focuses on a 1024×1024 pixel CIS architecture with quadruple column-parallel pipelined readout blocks per column. The proposed readout circuit includes four successive-approximation ADCs, eight 10-bit memory banks, and high-speed I/Os with a double data rate (DDR) up to 1 $Gbits/s$ for every 16 columns. The CIS makes use of the new readout architecture operating at rolling shutter to achieve $10,000$ $frames/s$ or 10.48 $Gpixels/s$. This chapter also presents noise analysis of significant components in the readout chain. Moreover, the radiation hardness consideration of the high-speed CIS is discussed for high energy physics applications, particularly total ionizing dose (TID) tolerance.

3.1 A 10,000 frames/s CIS with Megapixels

This section focuses on the architecture of a $10,000$ $frames/s$ CIS with an image resolution of 1024×1024 pixels. The pixel is 20 $\mu m \times 20$ μm in size and consists of four N-type MOFETs with enclosure layout.

The floor plan of the proposed image sensor core is illustrated in Figure 3.1. The image sensor core has a symmetrical architecture. The sensor consists of the pixel array, column readout circuits on both the top and bottom sides of the pixel array, a row decoder, two sequencers, memory banks (not shown), serializers, and SLVS transmitters.

To be specific, the CMOS sensor has over one million pixels, 4096 column readout circuits, 128 serializers, 2 sequencers (top and bottom), and 128 SLVS transmitters. The image sensor provides complete digital input control and series digital output. All pixel control signals are provided by the row decoder, which is fully controlled by the bottom sequencer.

The architecture enables 2D windowing by programmable addressing in the Y-direction in steps of 4 pixels per step and in the X-direction in steps of 16 columns per step. The windowing feature is achieved by

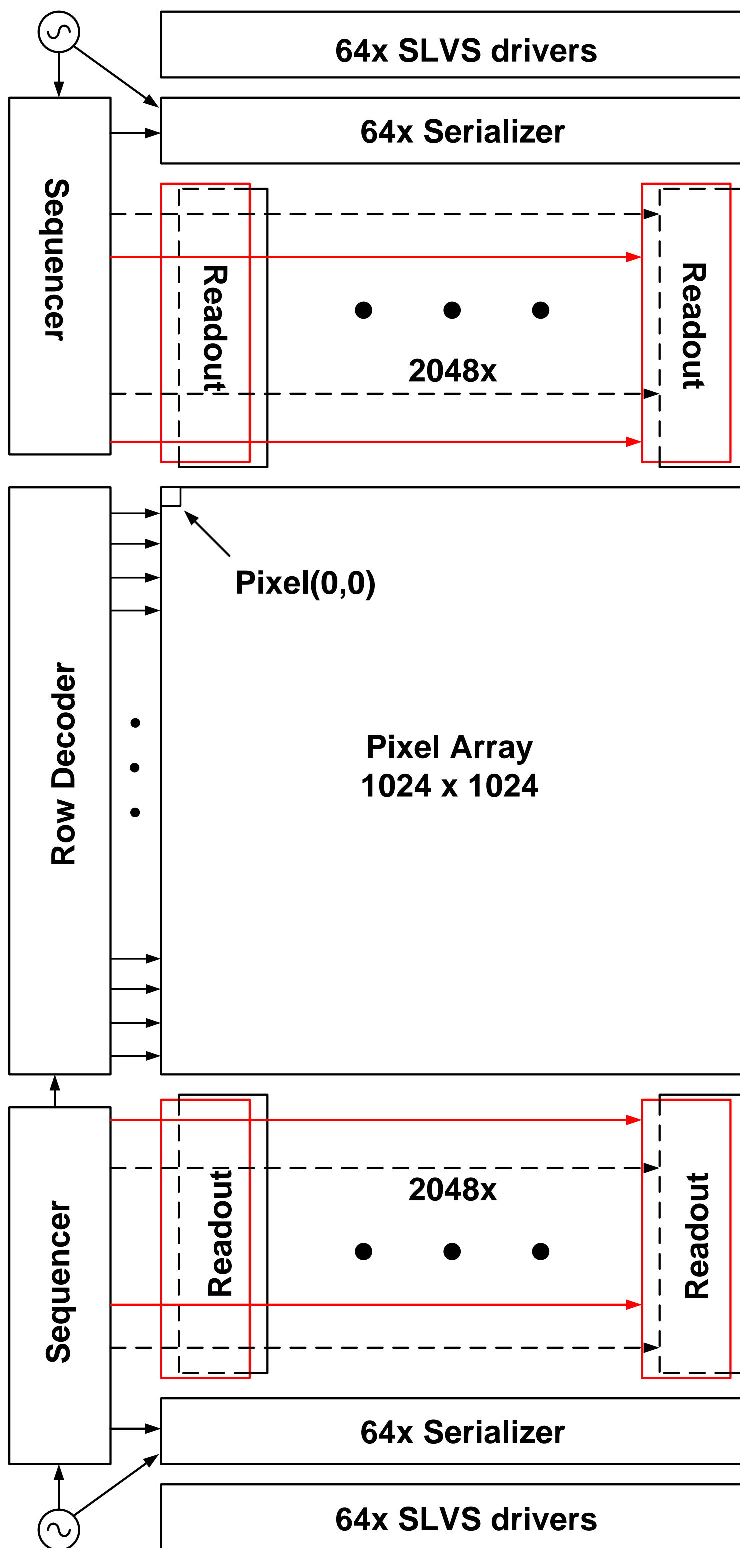


Figure 3.1: Imager floor plan

SPI interface to set the starting and stopping points of the Y address. The window size in the X-direction is achieved by selecting specific I/Os to the acquisition system. Furthermore, all required control, bias, and clock signals are generated on-chip. The incoming clock signal is fed into the master PLLs on top and bottom sides to generate a main clock signal for sequencers. The on-chip bandgap reference provides voltage references. The on-chip sequencer is used to generate all control signals for the pixel array, ADCs, and memory banks.

3.2 Quadruple Column-Parallel Readout Scheme

This section discusses the principle of the quadruple column-parallel readout (QCPRO) scheme. The proposed readout scheme enables the sensor to read out one million pixels at a fast frame rate, as shown in Figure 3.2. The scheme has four identical column readout blocks operating in parallel for each column. Two are located at the top readout block and two at the bottom. Each readout block includes one analog front-end (AFE) circuit, one ADC, and two memory banks based on D flip-flops. Two sequencers provide reference voltages and control signals for $2 \times N$ of readout blocks for the top and bottom peripheral readout circuits, respectively (N represents the total number of columns). More details on each sub-circuit in the readout block are discussed in Chapter 4.

Rolling shutter mode is chosen for this CMOS image sensor to achieve a high frame rate. The image is captured by scanning the rows vertically instead of by taking a snapshot of the entire pixel array. Although it suffers from skew issue for capturing fast-moving objects, the negative effects could become negligible if the criterion is met in the relationship between the speed of the sensor and the moving target. This is discussed in Chapter 4.

The principle of the proposed QCPRO is described to explain how to achieve a $10,000\ frames/s$ rate in a 1024×1024 active pixel array. The number of rows and columns are the same, 1024. The QCPRO is capable of reading out four rows at one time, and the column-parallel architecture enables to process all columns simultaneously. Therefore, the sensor can convert analog signals of 4096 pixels into digital codes and deliver $4096 \times N_{ADC}$ digital bits to the FPGA (N_{ADC} is the resolution of the ADC). The entire pixel array with 1024×1024 pixels only need 256 readout cycles to complete one full frame, which is 4 times faster than that of single readout block per column.

The time of one frame, called frame time (t_{FT}), is computed by

$$t_{FT} = \frac{1}{Frame\ Rate} = \frac{1}{10\ kfps} = 100\ \mu s \tag{3.1}$$

The time to read 4 rows at one time is called line time (t_{LT}). So one frame time is equal to 256 line times. The line time is computed by

$$t_{LT} = \frac{t_{FT}}{1024} \times 4 = \frac{100\ \mu s}{256} \approx 390\ ns \tag{3.2}$$

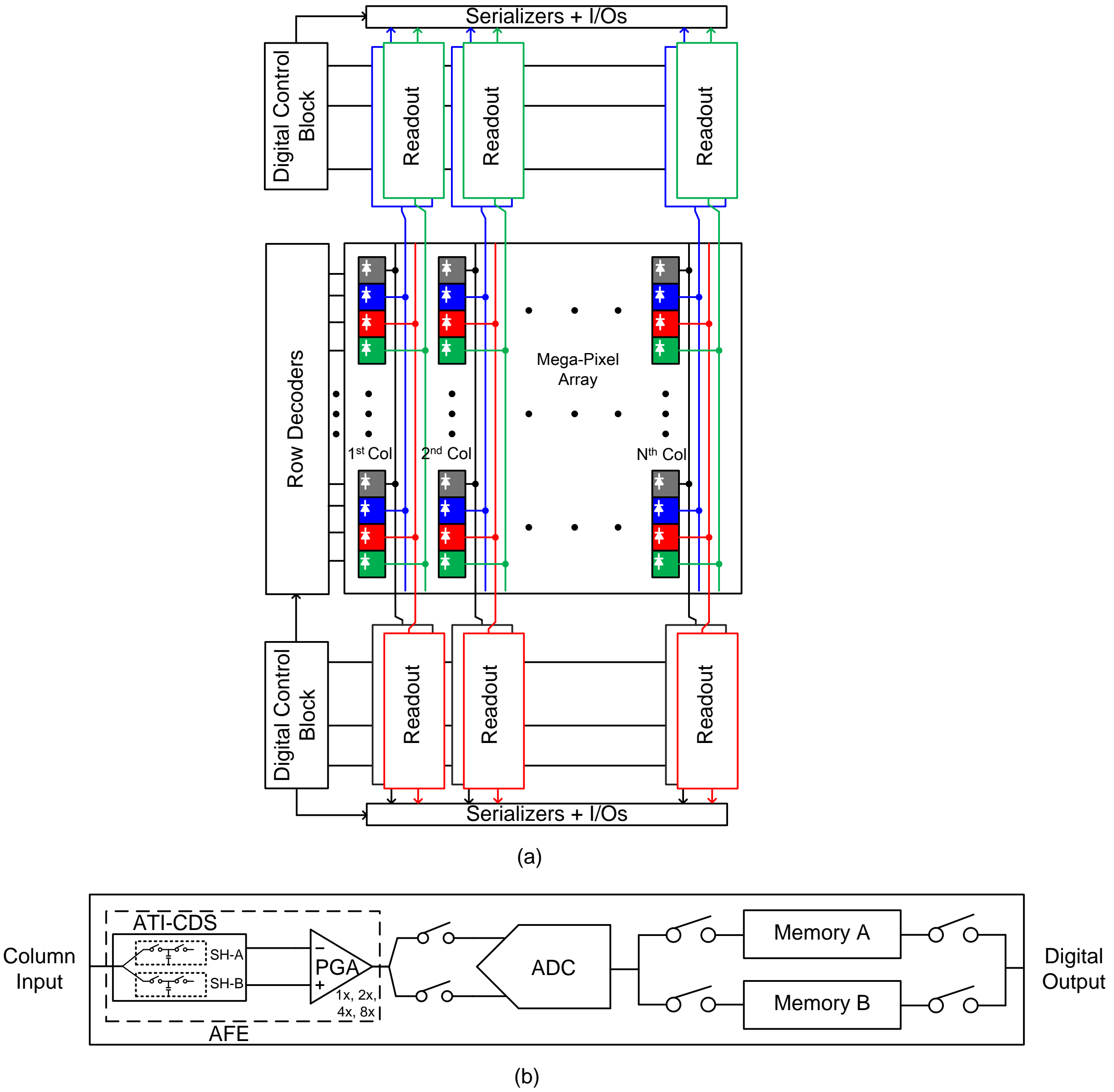


Figure 3.2: (a) Proposed quadruple readout architecture, (b) single readout block diagram

Two ADCs with different resolutions, 10 bits and 12 bits, are used to analyze the proposed QCPRO architecture. For 1024 columns, the total number of ADCs is 4096. Having multiple ADCs per column allows the reduction of sampling rate (or conversion rate) required for each ADC, when compared to using a single ADC per column or using a single ADC per sensor. Furthermore, a lower sampling rate generally improves power efficiency and reduces the overall CIS power consumption.

To achieve a rate of $10,000\ frames/s$, one ADC conversion is assumed to complete in one line time. Thus, the highest clock frequency in one cycle of the 10-bit or 12-bit SAR ADC is given by

$$\begin{aligned} 10\ bit \Rightarrow f_{clk} &= \frac{10}{t_{LT}} = \frac{10}{390\ ns} \approx 25.64\ MHz \\ 12\ bit \Rightarrow f_{clk} &= \frac{12}{t_{LT}} = \frac{12}{390\ ns} \approx 30.77\ MHz \end{aligned} \tag{3.3}$$

Each line time has two essential phases: sampling and converting. The above calculations use the whole line time for data conversion, with no time left to deliver the pixel signal from in-pixel source-follower to the ADC input. As a result, either slowing down the sensor speed or increasing the ADC speed is a possible solution to provide some time for sampling.

The proposed readout circuit in Figure 3.2(b) provides a more efficient solution by using a time-interleaving sampling circuit and two memory banks with a ping-pong operation. The normal operation of each readout block is illustrated in Figure 3.3. Two sampling blocks (SH-A and SH-B) and two readout blocks (ReadoutA and ReadoutB) are implemented in one readout circuit. One time slot means one line time with 390 ns. The operation starts out with a latency of two time slots before it is ready to send out the digital data. The ADC is constantly converting pixel data in each time slot. These two sample and hold circuits can have independently correlated double sampling operations. When SH-A is connected to the column line for sampling, SH-B is connected to the column ADC for digitizing the previously sampled data, and vice versa. Therefore, this method succeeds to accomplish three operations, sampling, conversion, and readout in one line time.

For high-speed CISs, another significant aspect is to consider how to deal with the fast data rate, particularly in a large image format. The proposed CIS architecture with 1024×1024 pixels and $10,000\ frames/s$ results in an aggregate pixel rate of 10.48 $Gigapix/s$. It is less efficient to send the digital data out after finishing the conversion of all pixels and storing all digital data.

Nonetheless, it could be much more efficient to deliver partial pixels or even a single row of pixels at a time. For example, the aggregate data rate of the proposed CIS in each line time is 40.96 *kbits* for using 10-bit ADCs and 49.152 *kbits* for using 12-bit ADCs. Thus, the ping-pong memory-bank (PPMB) method provided by the readout block is to use reasonable but sufficient amount of memories to store the 4 rows of digital data.

Two memory banks, MB-A and MB-B, are in one PPMB block. When MB-A is storing the data for the ADC, MB-B will be connected to a high-speed I/O to send the data off-chip and vice versa. As a result, the proposed sensor can achieve a faster speed with less on-chip digital memories, because it only needs to store and deliver four rows of digital data for one line time.

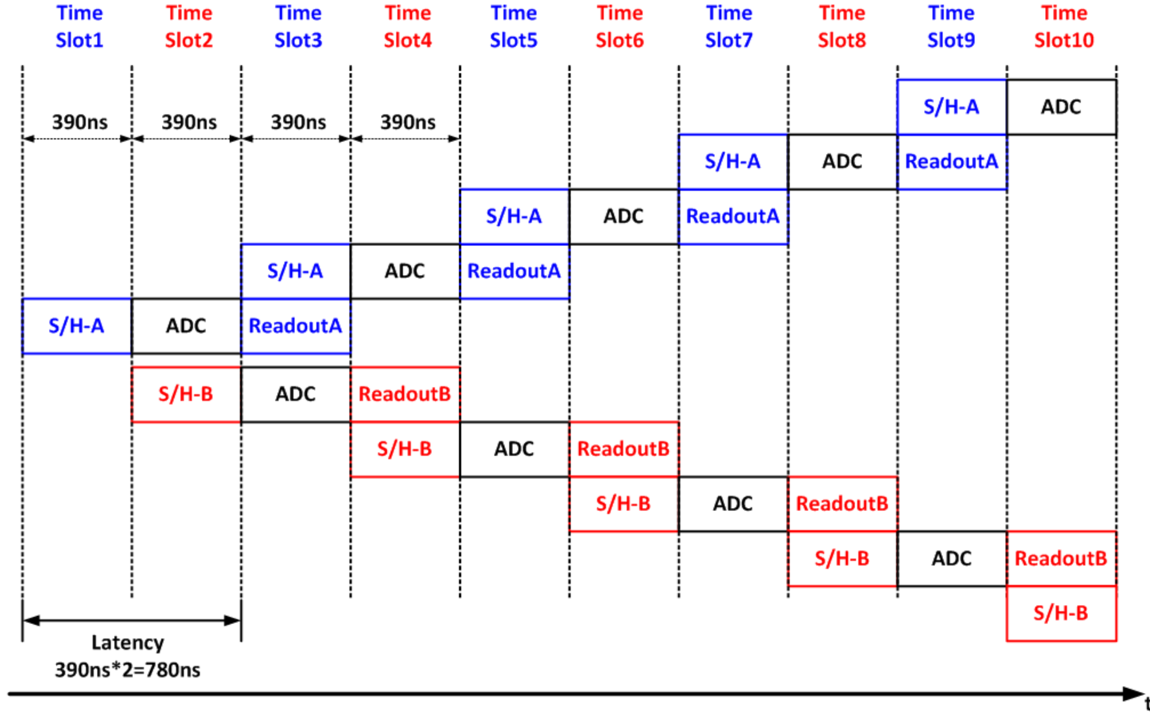


Figure 3.3: Time-interleaving sampling and ping-pong memory banks in proposed QCPRO

The next consideration is the number of I/Os and how fast they need to be when the sensor operates at the maximum frame rate. The maximum data rate is equal to the product of the number of I/Os and operating speed. The maximum date rate is required to be larger than the multiplication of total number of ADCs, the resolution and conversion rate of single ADC.

$$\# \ of \ I/Os \times f_{IO} \geq \# \ of \ ADCs \times N_{ADC} \times conversion \ rate \tag{3.4}$$

where f_{IO} is the speed of the I/O channel and N_{ADC} is the ADC resolution.

The I/O speed must match the receiver speed on the testing acquisition board. As shown in the equation below, the digital dynamic power consumption is directly proportional of the I/O speed, the load capacitance, and the square of the power supply. For a better power efficiency, the low-power SLVS transmitter is chosen to operate at 1 $Gbits/s$ and a 0.4 V power supply.

$$P = C_{load} \times V_{DD}^2 \times f_{IO} \tag{3.5}$$

Then, the maximum number of columns connected to the same I/O is computed by

$$\begin{aligned} 10\ bit &\Rightarrow \frac{1\ Gbits/s}{2 * 10\ bits/390\ ns} \approx 19\ columns \\ 12\ bit &\Rightarrow \frac{1\ Gbits/s}{2 * 12\ bits/390\ ns} \approx 16\ columns \end{aligned} \tag{3.6}$$

The proposed CIS architecture chooses 16 columns connected to one I/O. Since the CIS is symmetrical, thus, total number of I/Os in the CMOS image sensor is $2 \times \frac{1024}{16} = 128$.

The maximum clock frequency of the I/O is

$$\begin{aligned} 10\ bit &\Rightarrow f_{IO,Max} = 0.5 \times \frac{20\ bits}{390\ ns} \times 16 \approx 410.25\ MHz \\ 12\ bit &\Rightarrow f_{IO,Max} = 0.5 \times \frac{24\ bits}{390\ ns} \times 16 \approx 492.3\ MHz \end{aligned} \tag{3.7}$$

Consequently, a 500 MHz on-chip phase-locked loop (PLL) can be used to support the clock frequency requirement.

3.3 Operation of Proposed Readout Scheme

The detailed operation of the QCPRO block is described in this section. As shown in Figure 3.4, the QCPRO processes four rows of pixels in one line time. As mentioned in the previous section, each column has four ADCs (ADC1, ADC2, ADC3, and ADC4), two samples and holds (SH-A and SH-B) per ADC, and two memory banks (MB-A and MB-B) per ADC.

When starting to read the first 4-row pixels, four SH-As sample the reset and pixel signals for corresponding pixels in one line time. Then, the second 4-row pixels are sampled by four SH-Bs. Meanwhile, each SH-A is connected to the corresponding ADC for digitization. The digital bits are stored in MB-As. In the third line time, three operations process simultaneously: the sampling of the third 4-row pixels, the conversion of the pixel data on SH-Bs, and the transfer of the digital data saved in MB-As to the SLVS transmitter. Therefore, after a latency of two line times, the regular readout operation of the sensor begins in the third line time.

Two addressing pointers from the bottom sequencer, $P1$ and $P2$, are used in this sensor to control the exposure time. Point $P1$ is responsible for resetting row by row. Pointer $P2$ is responsible for selecting the row which can start the readout procedure. The number of rows between two points is customized to determine the exposure time. Therefore, the exposure time of the CMOS image sensor can be calculated by

$$T_{exposure\ time} = \frac{n}{256 \times Frame\ Rate} \tag{3.8}$$

where n is the rows between two points divided by 4. The maximum exposure time happens when $P1$ points to the last row and $P2$ points to the first row, which is $\frac{1}{Frame\ Rate} = 100\ \mu s$.

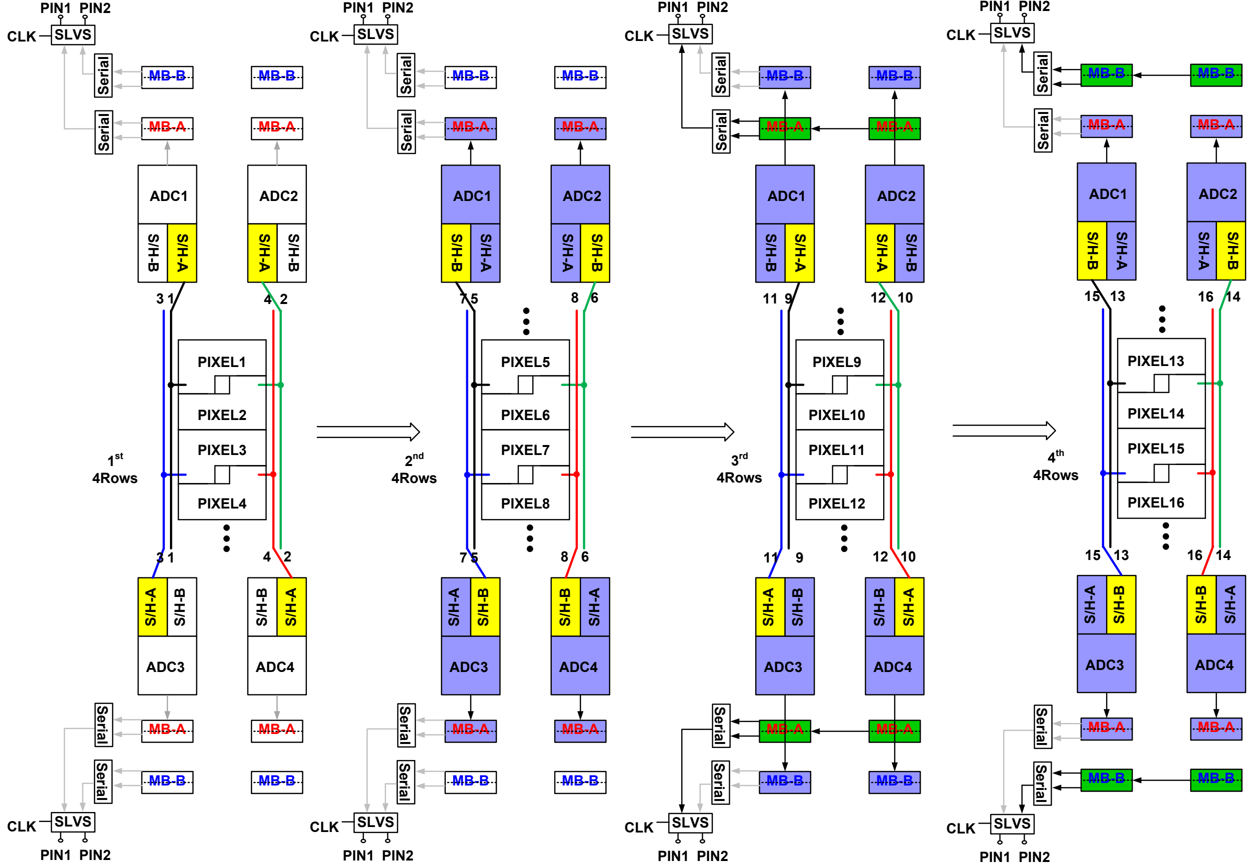


Figure 3.4: Readout operation of one column with 4 ADCs

3.4 Noise Analysis of Proposed Readout Chain

Noise components in the proposed readout chain are depicted in Figure 3.5. Since noise sources like reset noise and pixel-to-pixel FPN can be canceled by column-level correlated double sampling, the remaining noises are the source follower noise, the kT/C noise in the sample-and-hold circuits, the amplification noise, and the ADC noise. The column-to-column FPN, which is caused by the mismatch of column amplifiers and column-level ADCs, can be reduced or removed by subtracting a dark frame from the current frame. The dark frame stores all dark pixels off chip as a reference. A system-level imaging processing technique can be used for column-to-column FPN cancellation.

3.4.1 Noise in Source Follower

The noise of the source follower consists of the thermal noise and flicker noise from the source follower MOSFET and the current sink. Figure 3.6 shows the in-pixel source follower used in the proposed readout chain and its equivalent noise model. The thermal noise power spectral density (PSD) of a MOSFET in the saturation region is expressed as

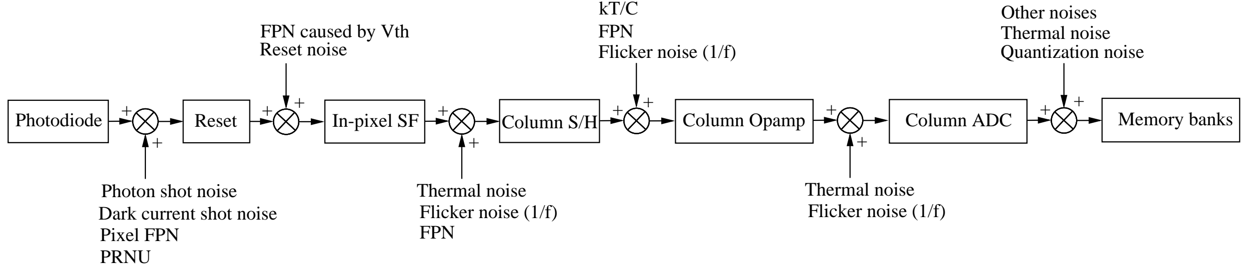


Figure 3.5: Noise components in one column readout chain

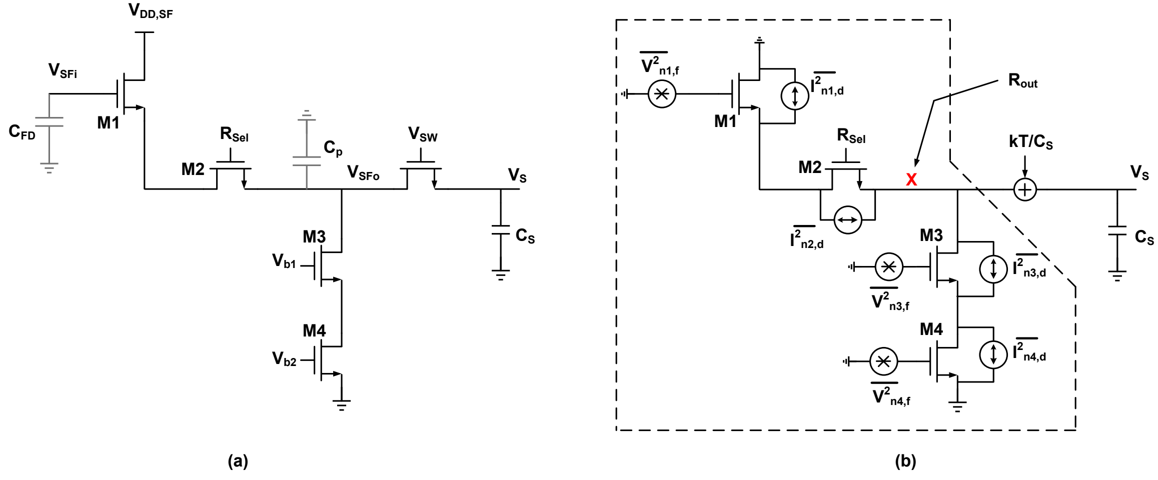


Figure 3.6: Source follower and equivalent noise model

$$\frac{\overline{I_{n,d}^2}}{\Delta f} = 4kT\gamma \cdot g_m, \ [A^2/Hz]$$
$$or \ \frac{\overline{V_{n,d}^2}}{\Delta f} = \frac{4kT\gamma}{g_m}, \ [V^2/Hz]$$
$$\gamma = 2/3 \ for \ long \ channel \ length \ MOSFETs$$
$$\gamma = 2 - 3 \ for \ short \ channel \ length \ MOSFETs \tag{3.9}$$

where k is the Boltzmann constant, g_m is the MOSFET transconductance, T is the temperature in Kelvin, and Δf is the bandwidth.

The flicker noise PSD of a MOSFET is expressed as

$$\frac{\overline{I_{n,f}^2}}{\Delta f} = \frac{K_f \cdot g_m^2}{WLC_{ox}f}$$
$$or \ \frac{\overline{V_{n,f}^2}}{\Delta f} = \frac{K_f}{WLC_{ox}f} \tag{3.10}$$

where K_f is the flicker noise coefficient.

The total noise PSD of a MOSFET is

$$\begin{aligned} \frac{\overline{I_{n,t}^2}}{\Delta f} &= 4kT\gamma \cdot g_m + \frac{K_f \cdot g_m^2}{WLC_{ox}f} \\ or\ \frac{\overline{V_{n,t}^2}}{\Delta f} &= \frac{4kT\gamma}{g_m} + \frac{K_f}{WLC_{ox}f} \end{aligned} \tag{3.11}$$

The following calculations assume that the MOSFETs are long channel and operate at saturation region. When calculating the output noise PSD of the source follower, some noise sources in Figure 3.6 can be neglected. These noise sources are the thermal noise sources of M2 and M3 and the flicker noise of M3. Thus, the output current noise PSD at the X node is expressed as

$$\begin{aligned} \frac{\overline{I_{n,SFo}^2}}{\Delta f} &= \frac{\overline{I_{n,M1}^2}}{\Delta f} + \frac{\overline{I_{n,M4}^2}}{\Delta f} = (\frac{\overline{I_{n1,d}^2}}{\Delta f} + \frac{\overline{I_{n1,f}^2}}{\Delta f}) + (\frac{\overline{I_{n4,d}^2}}{\Delta f} + \frac{\overline{I_{n4,f}^2}}{\Delta f}) \\ &= (\frac{8kT \cdot g_{m1}}{3} + \frac{K_f \cdot g_{m1}^2}{W_1 L_1 C_{ox} f}) + (\frac{8kT \cdot g_{m4}}{3} + \frac{K_f \cdot g_{m4}^2}{W_4 L_4 C_{ox} f}) \\ &= \frac{8kT}{3}(g_{m1} + g_{m4}) + n_f \cdot (\frac{g_{m1}^2}{W_1 L_1} + \frac{g_{m4}^2}{W_4 L_4}) \cdot \frac{1}{f} \end{aligned} \tag{3.12}$$

where $n_f = \frac{K_f}{C_{ox}}$ is the flicker noise parameter.

The output resistance at the X node is

$$R_{out} = (\frac{1}{g_{m1} + g_{mb1}} + R_{col})||g_{m3}r_{o3}r_{o4} \tag{3.13}$$

where R_{col} includes the M2 switching resistance and parasitic resistance on the column line.

Based on the column line resistance and parasitic capacitance, the equation for a simple RC low-pass filter can be used to compute the equivalent noise bandwidth (ENB). The parasitic capacitance at X node is assumed to be C_{col}, including the C_{GS} capacitance of all row select switches and parasitic coupling capacitance. Thus, the ENB is $\frac{1}{4 \times R_{out} C_{col}}$ for the first order low-pass filter model. Table 3.1 depicts the relationship between the ENB value and the order of low-pass filters.

Table 3.1: ENB vs the order of low-pass filters

Filter Order	ENB
1	$1.57 \times f_{3dB}$
2	$1.11 \times f_{3dB}$
3	$1.05 \times f_{3dB}$
4	$1.025 \times f_{3dB}$

Assuming the low frequency and high frequency are f_L and f_H, respectively, the total output noise power of the source follower is calculated by

$$\begin{aligned}\overline{V_{n,SFo}^2} &= \frac{\overline{V_{n,d}^2}}{\Delta f} \times ENB + \int_{f_L}^{f_H} \frac{\overline{V_{n,f}^2}}{\Delta f} df \\ &= \frac{\overline{I_{n,SFo}^2}}{\Delta f} \times R_{out}^2 \times ENB + \int_{f_L}^{f_H} \frac{K_f}{C_{ox} f} (\frac{g_{m1}^2}{W_1 L_1} + \frac{g_{m4}^2}{W_4 L_4}) \times R_{out}^2 df \\ &= \frac{2kTR_{out}}{3C_{col}} (g_{m1} + g_{m4}) + n_f \cdot R_{out}^2 (\frac{g_{m1}^2}{W_1 L_1} + \frac{g_{m4}^2}{W_4 L_4}) \cdot ln \frac{f_H}{f_L}\end{aligned} \tag{3.14}$$

where ENB is equal to $F_H - F_L$. Typically, the F_L is $10Hz$.

Therefore, the output RMS noise voltage,$\overline{V_{rms,SFo}}$, is

$$\overline{V_{rms,SFo}} == \sqrt{\frac{2kTR_{out}}{3C_{col}} (g_{m1} + g_{m4}) + n_f \cdot R_{out}^2 (\frac{g_{m1}^2}{W_1 L_1} + \frac{g_{m4}^2}{W_4 L_4}) \cdot ln \frac{f_H}{f_L}} \tag{3.15}$$

As long as the gain of the source follower, $A_{V,SF}$, is known, the input-referred noise power, $\overline{V_{n,SFi}^2}$, and RMS noise voltage,$\overline{V_{rms,SFi}}$, can be determined by

$$\begin{aligned}\overline{V_{n,SFi}^2} &= \overline{V_{n,SFo}^2} \times \frac{1}{A_{V,SF}^2} \\ &= \{\frac{2kTR_{out}}{3C_{col}} (g_{m1} + g_{m4}) + n_f \cdot R_{out}^2 (\frac{g_{m1}^2}{W_1 L_1} + \frac{g_{m4}^2}{W_4 L_4}) \cdot ln \frac{f_H}{f_L}\} \times \frac{1}{A_{V,SF}^2} \\ \overline{V_{rms,SFi}} &= \frac{1}{A_{V,SF}} \cdot \sqrt{\frac{2kTR_{out}}{3C_{col}} (g_{m1} + g_{m4}) + n_f \cdot R_{out}^2 (\frac{g_{m1}^2}{W_1 L_1} + \frac{g_{m4}^2}{W_4 L_4}) \cdot ln \frac{f_H}{f_L}}\end{aligned} \tag{3.16}$$

3.4.2 Noise in Column S/H

The purpose of column S/H is to sample pixel output prior to data conversion. However, sampling noise is introduced by the sampling operation. The sampling noise comes from the thermal noise of MOSFET switches during the switch-on period or sampling period. Although the sampling capacitors are noiseless, the output noise power is inversely proportional to the size of the sampling capacitor. This is generally referred to as "kT/C" noise given by

$$\overline{V_{n,SH}^2} = \frac{kT}{C_S} \tag{3.17}$$

Both Table 2.2 and the above equation depict that an increase of sampling capacitance decreases the kT/C noise. Since the S/H circuit is a low-pass filter with gain equal to one, the input referred voltage noise PSD is equal to the output voltage noise PSD.

Based on the reference [153, 154], 1/f noise power for CDS is given by

$$\overline{V_{nf,SH}^2} = \int_0^{\infty} S_n(x)_{1/f} \frac{4sin^2 x}{1 + (\frac{x}{\omega_c T_0/2})^2} dx \cong 2N_f\{\gamma + ln(\omega_c T_0)\} \tag{3.18}$$

where $S_n(x)_{1/f} = N_f/f$ is the power spectral density of the input 1/f noise source, N_f is the coefficients of 1/f noise, ω_c is the cutoff angular frequency of the first-order low pass filter, T_0 is the sampling period, and γ is Euler–Mascheroni constant (= 0.577215...).

The total noise power of the S/H block referred to floating diffusion node is

$$\overline{V_{n,SHi}^2} = \frac{\overline{V_{n,S/H}^2} + \overline{V_{nf,SH}^2}}{A_{V,SF}^2} = \frac{\frac{kT}{C_S} + 2N_f\{\gamma + ln(\omega_c T_0)\}}{(g_{m1} R_{out})^2} \tag{3.19}$$

The sampling noise in column S/H is similar to the reset noise in pixels discussed in the previous section. Before sending the pixel data to ADCs, these two noise sources exist in the sampling capacitors. Fortunately, the 4T PPD pixel architecture allows a truly correlated double sampling (CDS) technique to eliminate both reset and sampling noise before data conversion.

3.4.3 Noise in the SC Amplifier

The analog front-end (AFE) in the QCPRO block includes three circuits: two S/H circuits and programmable gain amplifier (PGA). As the essential circuit, the PGA is used as a buffer or sampler located between the S/H circuit and the following ADC. A switched-capacitor PGA is used in the proposed QCPRO block. It operates in two phases. Phase-I resets the buffer's output by a fixed reference voltage, V_{RefAmp}, and cuts off the connection to the S/H for completing the CDS process. Phase-II delivers the pixel differential value to the ADC for data conversion.

Figure 3.7 illustrates the noise model of the SC amplifier with one S/H circuit at two phases. Assume the input-referred noise PSD of the operational amplifier is $\overline{V_{n,op}^2}$. For the simplicity of the noise calculation, the voltage gain of SC-PGA is set to be one, $A_v = 1$. Thus, the output noise PSD of the SC amplifier at Phase-I is expressed by

$$\frac{\overline{V_{n,\phi 1}^2}}{\Delta f} = (\frac{\overline{V_{n,op}^2}}{\Delta f} + \frac{\overline{V_{n,s3}^2}}{\Delta f}) \times |A_v|^2 + \frac{\overline{V_{n,s4}^2}}{\Delta f} = \frac{\overline{V_{n,op}^2}}{\Delta f} + 4kTR_{on3} + 4kTR_{on4} \tag{3.20}$$

The output noise PSD of the SC amplifier at Phase-II is expressed by

$$\frac{\overline{V_{n,\phi 2}^2}}{\Delta f} = (\frac{\overline{V_{n,op}^2}}{\Delta f} + \frac{\overline{V_{n,s2}^2}}{\Delta f}) \times |A_v|^2 + \frac{\overline{V_{n,s4}^2}}{\Delta f} = \frac{\overline{V_{n,op}^2}}{\Delta f} + 4kTR_{on2} + 4kTR_{on4} \tag{3.21}$$

The total output noise PSD is given by

$$\begin{aligned} \frac{\overline{V_{n,OPo}^2}}{\Delta f} &= \frac{\overline{V_{n,\phi 1}^2}}{\Delta f} + \frac{\overline{V_{n,\phi 2}^2}}{\Delta f} \\ &= 2 \times \frac{\overline{V_{n,op}^2}}{\Delta f} + 4kTR_{on3} + 4kTR_{on2} + 4kTR_{on4} \times 2 \end{aligned} \tag{3.22}$$

The equivalent noise bandwidth is limited by the output node resistance and capacitance. The total output noise power is given by

$$\begin{aligned} \overline{V_{n,OPo}^2} &= \frac{\overline{V_{n,opo}^2}}{\Delta f} \times \Delta f_{BW} \\ &= \{(2 \times \frac{\overline{V_{n,op}^2}}{\Delta f} + 4kTR_{on3} + 4kTR_{on2}) \times |A_v|^2 + 4kTR_{on4} \times 2\} \times \frac{1}{4R_{tot}C_{ADC}} \end{aligned} \tag{3.23}$$

where R_{tot} is the total resistance at the output node of the SC buffer and C_{ADC} is the total sampling capacitance of the following ADC.

Considering noise contributions of the SC buffer, the total input-referred noise power at floating diffusion node is

$$\begin{aligned}\overline{V_{n,OPi}^2} &= \frac{\overline{V_{n,opo}^2}}{A_{V,SF}^2 \cdot A_{V,SH}^2 \cdot A_{V,OP}^2} \\ &\approx \frac{1}{A_{V,SF}^2 \cdot R_{tot}C_{ADC}} \cdot \{0.5 \times \frac{\overline{V_{n,op}^2}}{\Delta f} + kT(R_{on3} + R_{on2}) + \frac{2kTR_{on4}}{A_{V,OP}^2}\}\end{aligned} \tag{3.24}$$

The Equation 3.24 illustrates that a larger voltage gain of the SC-PGA could degrade the input referred noise contributed by PGA and ADC.

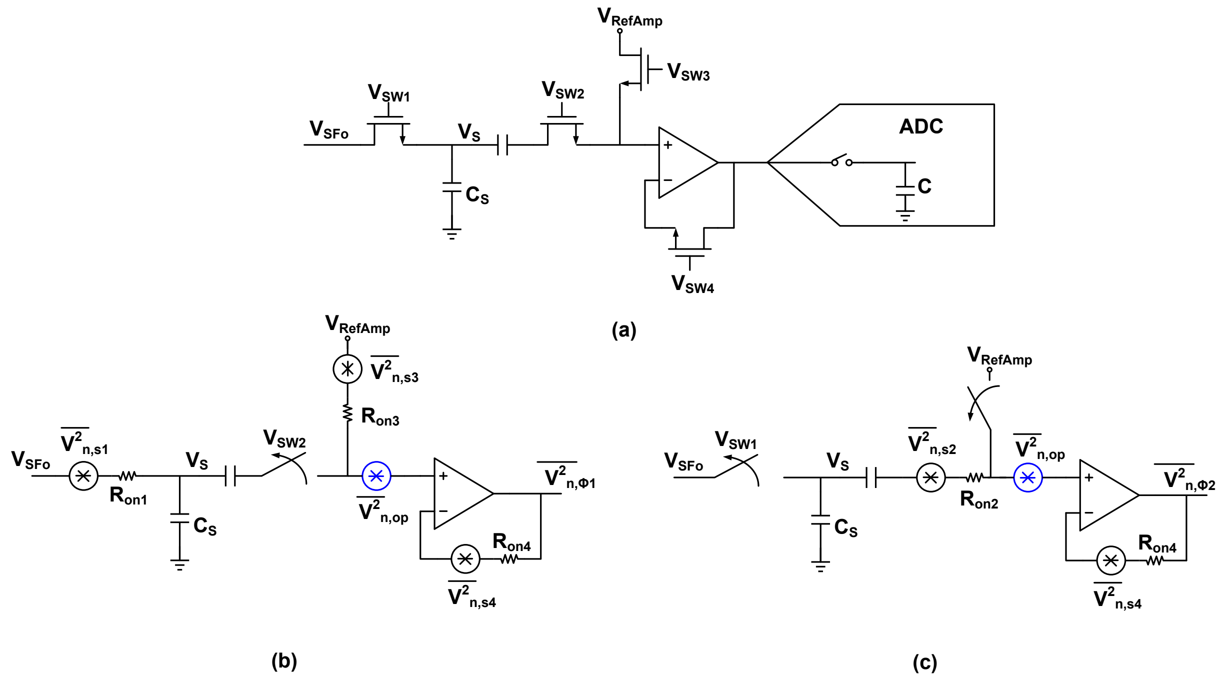


Figure 3.7: Simplified SC buffer (a) block diagram, (b) Phase-I and (c) Phase-II noise model

3.4.4 Column ADC Noise

Column ADC noise comes from many sources, including inherent ADC noise, internal amplifier or comparator noise, internal or external voltage reference noise, non-ideal power supplies, internal or external clock jitter, and poor layout design. Each ADC contributes both thermal noise and quantization noise. Noise from other parts or adjacent circuits could be coupled into the sensitive subcircuits in the ADC. Poor layout could couple noise from other parts or adjacent circuits into the sensitive analog sub-circuits the ADC. The clock signal contributes jitter or phase noise that translates into non-uniform sampling and poor timing control, which is more critical for high-speed ADCs. Other sources can add thermal noise or 1/f noise that will appear in the ADC's output code.

Inherent ADC noise has two primary sources, quantization noise and thermal noise. The two sources are uncorrelated. The total root-mean-square value of ADC noise can be expressed as

$$\overline{V_{n,total}} = \sqrt{\overline{V^2_{n,quantization}} + \overline{V^2_{n,thermal}}} \tag{3.25}$$

ADC quantization noise comes from mapping an infinite number of analog voltages to a finite number of digital codes, so that each digital output corresponds to several analog input voltages. Thus, the maximum error that arises in an ideal ADC when converting an analog signal is $\pm\frac{1}{2}LSB$, as shown in Figure 3.8. The peak-to-peak value of an uncorrelated sawtooth waveform is one LSB and can represent the quantization error for any analog input signal. Therefore, the quantization noise power is obtained by computing the variance of a uniform distribution, which is given by

$$\overline{V^2_{n,quantization}} = \sigma^2_{quantization} = \frac{\Delta^2}{12} \tag{3.26}$$

where Δ is one LSB of the ADC.

The rms value of quantization noise is expressed by

$$\overline{V_{n,quantization}} = \frac{\Delta}{\sqrt{12}} = \frac{\frac{V_{FS}}{2^N}}{\sqrt{12}} \tag{3.27}$$

where V_{FS} is the full scale of input signal and N is the resolution of the ADC.

The maximum signal-to-noise ratio (SNR) for an N-bit ADC can be expressed as

$$\begin{aligned} SNR_{max} &= 20 \cdot log_{10} \frac{V_{FS,rms}}{\overline{V_{n,quantization}}} = 20 \cdot log_{10} \frac{\frac{V_{FS}}{2\sqrt{2}}}{\frac{\frac{V_{FS}}{2^N}}{\sqrt{12}}} \\ &= 20 \cdot log_{10}(2^{N-1} \cdot \sqrt{6}) = 6.02 \times N + 1.76dB \end{aligned} \tag{3.28}$$

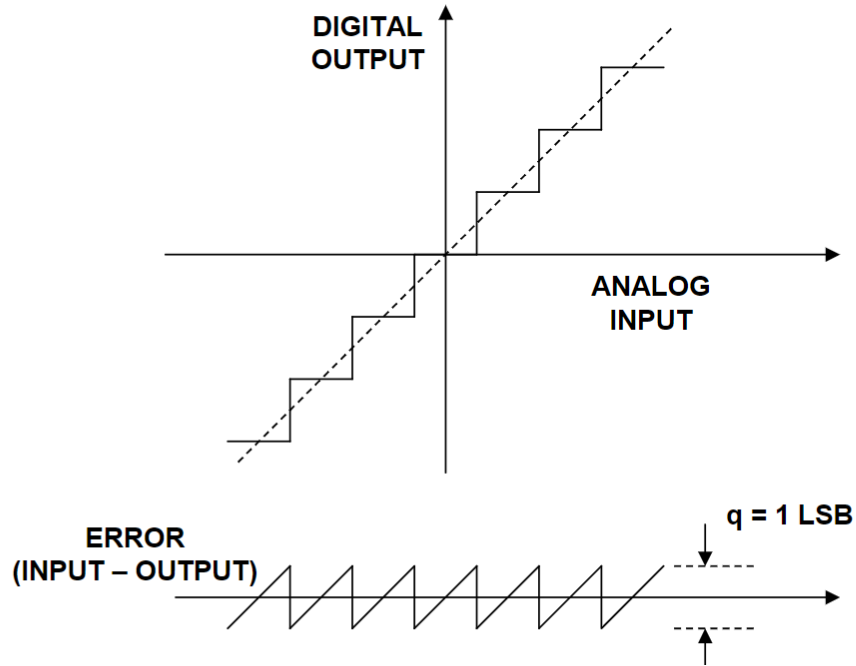


Figure 3.8: Ideal N-bit ADC quantization noise

In this equation, the RMS quantization noise is measured over the full Nyquist bandwidth from DC to $f_s/2$. The total ADC noise for a low-resolution ADC with less than 16-bit level typically depends more on quantization noise, because the contribution from the quantization noise is more substantial than the contribution from thermal noise.

When measuring an ADC noise performance, a Fast Fourier Transform (FFT) spectrum graph is commonly used to obtain total harmonic distortion (THD), noise floor, spurious-free dynamic range (SFDR), signal-to-noise ratio and distortion (SINAD), and the effective number of bits (ENOB). Consequently, the final ENOB is the figure of merit used to consider the effects of all noise sources on the ADC. The total noise power and RMS value can be expressed by

$$\begin{aligned} \overline{V^2_{n,total}} &= \frac{\frac{V_{FS}}{2^{ENOB}}}{12} \\ \overline{V_{n,total}} &= \frac{(\frac{V_{FS}}{2^{ENOB}})^{0.5}}{\sqrt{12}} \end{aligned} \tag{3.29}$$

The noise calculations for the proposed QCPRO block help determine the total noise power referred to floating diffusion, which is expressed by

$$\begin{aligned}
&\overline{V_{n,tot}^2} = \overline{V_{n,SFi}^2} + \overline{V_{n,SHi}^2} + \overline{V_{n,OPi}^2} + \overline{V_{n,ADCi}^2} \\
&= \{\frac{2kT}{3g_{m1}R_{out}C_{col}}(1+\frac{g_{m4}}{g_{m1}}) + \frac{K_f}{R_{out}C_{col}C_{ox}f}(\frac{1}{W_1L_1}+\frac{1}{W_4L_4}\cdot\frac{g_{m4}^2}{g_{m1}^2})\} + \frac{\frac{kT}{C_S}+2N_f\{\gamma+ln(\omega_c T_0)\}}{A_{V,SF}^2} \\
&+ \frac{1}{A_{V,SF}^2\cdot R_{tot}C_{ADC}}\cdot\{0.5\times\frac{\overline{V_{n,op}^2}}{\Delta f} + kT(R_{on3}+R_{on2}) + \frac{2kTR_{on4}}{A_{V,OP}^2}\} + \frac{V_{FS}}{12\cdot 2^{ENOB}}\cdot\frac{1}{A_{V,SF}^2A_{V,OP}^2}
\end{aligned} \tag{3.30}$$

The RMS noise voltage is the square root of the total noise power. Therefore, the lowest number of detectable electrons is computed by

$$Q_{e^-} = \frac{\sqrt{\overline{V_{n,tot}^2}}}{CG} = \sqrt{\overline{V_{n,SFi}^2} + \overline{V_{n,SHi}^2} + \overline{V_{n,OPi}^2} + \overline{V_{n,ADCi}^2}} \times \frac{C_{FD}}{q} \tag{3.31}$$

where C_{FD} includes all capacitance at the floating diffusion node and q is the single electron charge.

3.5 Radhard 4T Pixel

This dissertation mainly focuses on the mitigation of total ionizing dose (TID) effects on the pixel array. As discussed in the previous chapter, one of significant TID effects is oxide-trapped carriers. Two primary issues in active pixels are the TID-induced degradation of the in-pixel MOSFETs and photodiodes.

For the improvement of radiation tolerance of 4T pixels, the enclosure layout technique (ELT) is applied to the reset transistor, in-pixel amplifier, and row select transistor. The ELT technique helps mitigate threshold voltage shifts, radiation-induced narrow channel effects, sidewall leakages, and junction leakages. The integration of P+ guard-rings is also used to reduce the inter-device leakage current. Thus, in-pixel MOSFETs could be tolerant of TID beyond the 10 kGy (equal to 1 $Mrads$) range [155].

This dissertation is mainly concerned with the dark current of the PPD induced by TID effects. For low and moderate TID levels (below $50 - 500$ $krads$ (Si)), the dominant contribution to the dark current comes from the gate oxide and TG channel STI sidewalls[142]. In addition, the TID-induced dark current and TG subthreshold leakage result in the drop of PPD full-well capacity. Therefore, applying the enclosed layout TG could help mitigate those effects.

The CMOS technology used for the results discussed in the dissertation has two types of transistors: thick-oxide transistor in 3.3 V and thin-oxide one in 1.8 V. The thick-oxide NMOS used in pixels is chosen to have a wide voltage swing. The thin-oxide MOSFETs are used in row decoder, sequencers, column readout blocks, PLLs and SLVS I/Os for better trade-offs between integration, power consumption, and speed. Level shifters are added between the row decoder and the pixel array.

Figure 3.9 illustrates a radhard pixel cell with four annular transistors. To simplify the drawing, this cross-sectional view assumes all components are aligned. The final schematic and layout of the proposed radhard pixel is discussed in detail in Chapter 4.

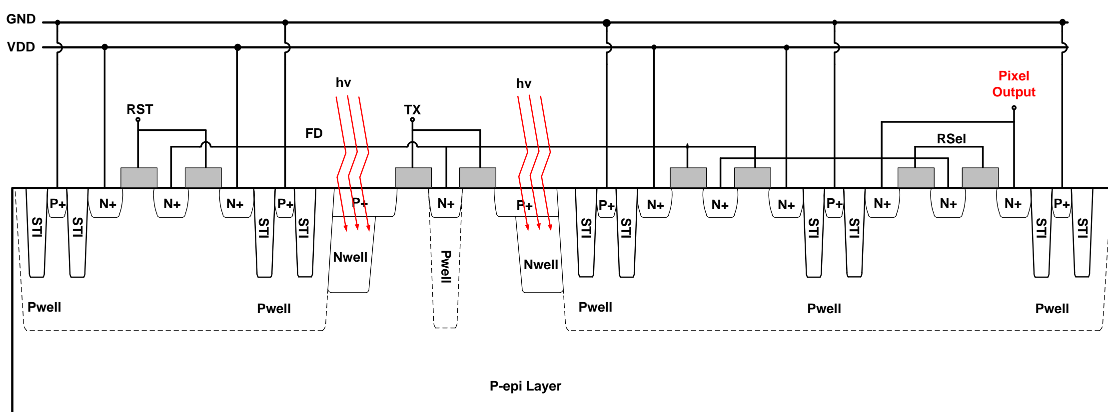


Figure 3.9: Cross-section view of the radhard pixel cell

Chapter 4

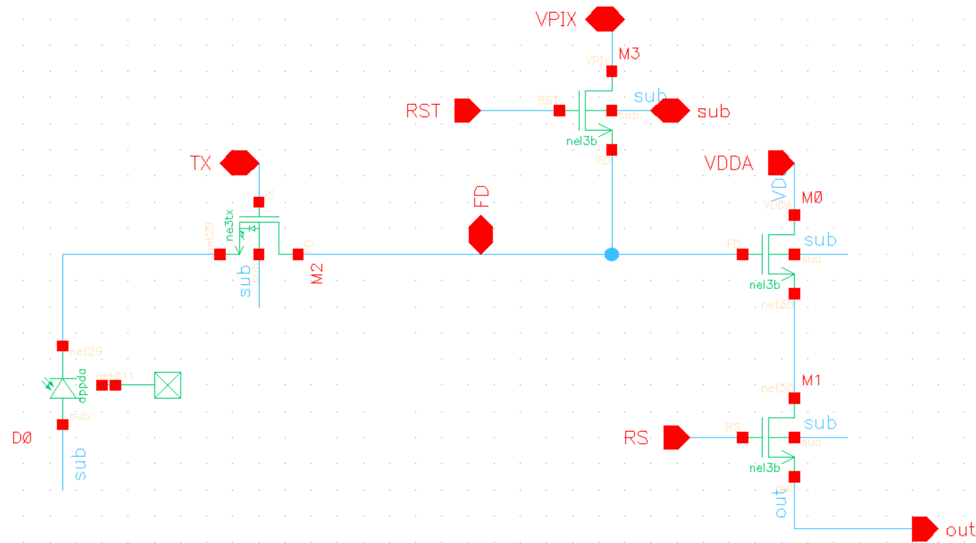
CIS Prototype

This chapter discusses the prototype implementation of the proposed high-speed megapixel CMOS image sensor in a 0.18 μm CIS process with 6-metal layers and 1-poly layer. The 4T radhard pixel is introduced in the first section. The sequencer block with the Serial Peripheral Interface (SPI) slave module is discussed in Section 4.2. The row control block is discussed in Section 4.3. The quadruple parallel readout architecture is described in Section 4.4, including analog front-end (AFE), ADC, and memory banks. The AFE block is discussed in two separate parts: analog time-interleaving correlated-double sampling (ATI-CDS) in subsection 4.4.1 and switched-capacitor programmable gain amplifier (SC-PGA) in subsection 4.4.2. Section 4.5 describes the phase-locked loop (PLL) and the scalable low-voltage signaling (SLVS) transmitter. The final section illustrates the chip layout and photograph and summarizes the sensor specifications.

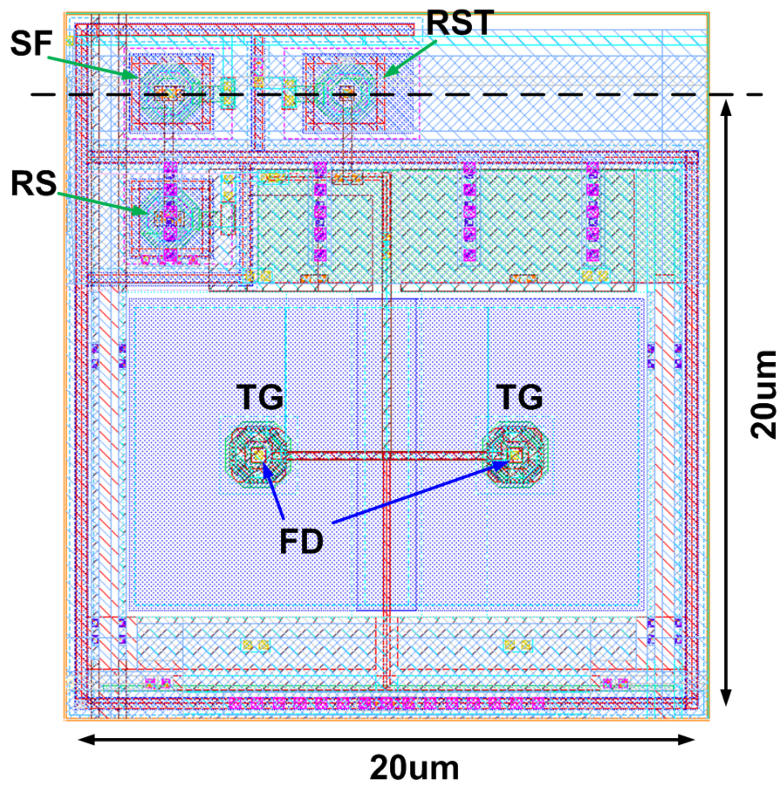
4.1 Pixel Design

The proposed CIS architecture is implemented in two image formats: one has 128 $\times$ 1024 pixels and the other 768 $\times$ 1024 pixels. The same pixel architecture is applied in both pixel arrays. The schematic and layout of a single pixel cell are shown in Figure 4.1a and 4.1b. Each pixel size is 20 $\mu m \times 20$ μm. The total area for the small and large image format is 2.56×20.28 mm^2 and 15.36×20.28 mm^2, respectively. All four in-pixel transistors are N-channel and radiation hardened by enclosure layout technique (ELT) as discussed in previous two chapters. Furthermore, each NMOS is surrounded by the P+ guardring for eliminating the inter-device leakage path. Consequently, the radiation tolerance of the active pixel is improved by sacrificing the photodetective area.

As shown in Figure 4.1b, the pixel locates three transistors, including the source follower, the reset transistor, and the row select switch, on the top area of the pixel layout. The two pixels' layouts are placed back-to-back to maximize the photodetective area. As the image sensor operates in rolling shutter mode and the proposed readout architecture enables to read out four rows of pixels in parallel, one select signal is used by every four rows of pixels. The RST and TG signals are buffered to connect each row of pixels



(a)



(b)

Figure 4.1: Schematic and layout view of the proposed radhard 4T pixel

instead of four rows, to reduce the parasitic effect caused by the increasing number of pixel columns. Those control signals are routed horizontally, and the four column lines are routed vertically.

A four-pixel cell in the same column is designed as an unit to build up the pixel array, as shown in Figure 4.2. The top two metal layers are used for power routing above the enclosed MOSFETs. Also, the floating diffusion connection is protected by the third metal layer from light incidents to generate a dark current.

In a large 4T pixel, ranging between 10 μm to 200 μm, the image lag and transfer efficiency become the key challenges. The charge transfer speed from PPD to FD is also one of the potential causes of image lag. Moreover, the short exposure time causes the image lag more severe in high-speed CISs. To eliminate the image lag issue, a 4T pixel with double TGs is proposed, as depicted in Figures 4.1b and 4.2. The TG transistors and FDs are connected to form a single unit.

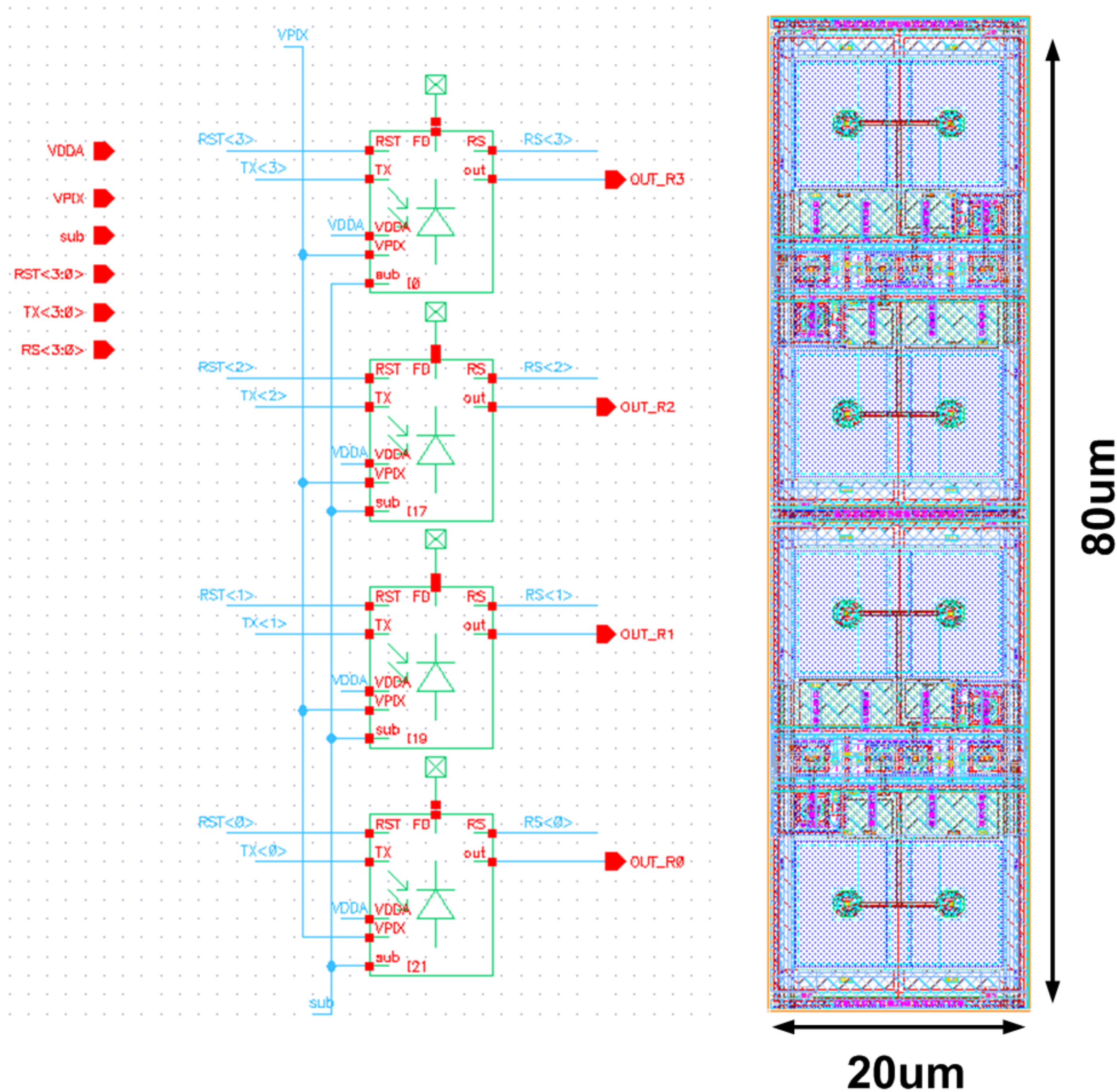


Figure 4.2: Schematic and layout view of four proposed pixels in the same column

Furthermore, the proposed sensor is required to work under low light conditions. A high conversion gain is an important parameter to improve the dynamic range by lowering the readout noise to achieve excellent low light performance. Because of conversion gain, discussed in Chapter 2, it is crucial to take into account the parasitic capacitance at the floating diffusion. Minimizing the parasitic capacitance at the floating diffusion is an effective way to increase conversion gain. Therefore, the active area of reset and TG transistor connecting to FD are placed in the middle of each ELT, which has a smaller area compared to the outside.

Figure 4.3 illustrates all of the parasitic capacitance connected to the floating diffusion node. These include the gate overlapping capacitance of the reset transistor (C_{rov}) and TG transistor (C_{tov}), the FD junction capacitance, C_J, and the coupling capacitance related to the metal wires, C_M. So the total capacitance at the floating diffusion [156] is defined as

$$C_{FD} = C_{rov} + C_{tov} + C_J + C_M \tag{4.1}$$

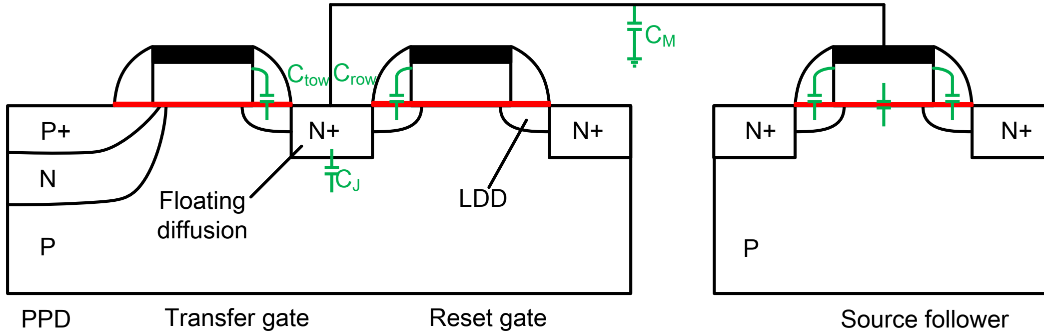


Figure 4.3: Total parasitic capacitance at FD

When the charges transfer to floating diffusion, the input capacitance of the SF should also be included, which is

$$C_{SFin} = C_{GD} + (1 - A_{SF}) \cdot C_{GS} = C_{GO} * W + (1 - A_{SF}) \cdot 2/3 \cdot WL * C_{ox} \tag{4.2}$$

The SF gain can be obtained from the simulation in Figure 4.4, $A_{SF} \approx 0.92$. Therefore, based on previous discussions, the calculation of pixel conversion gain is shown in Table 4.1.

A programmable DAC block with on-chip reference is used to control the current source in each column line, ranging from 5 μA to 80 μA. The DC sweep analysis of the SF is shown in Figure 4.5.

The noise analysis summaries for 15 μA and 80 μA are shown in Figure 4.6 and 4.7. The RMS noise referred to floating diffusion is 313.279 μV and 542.712 μV, respectively.

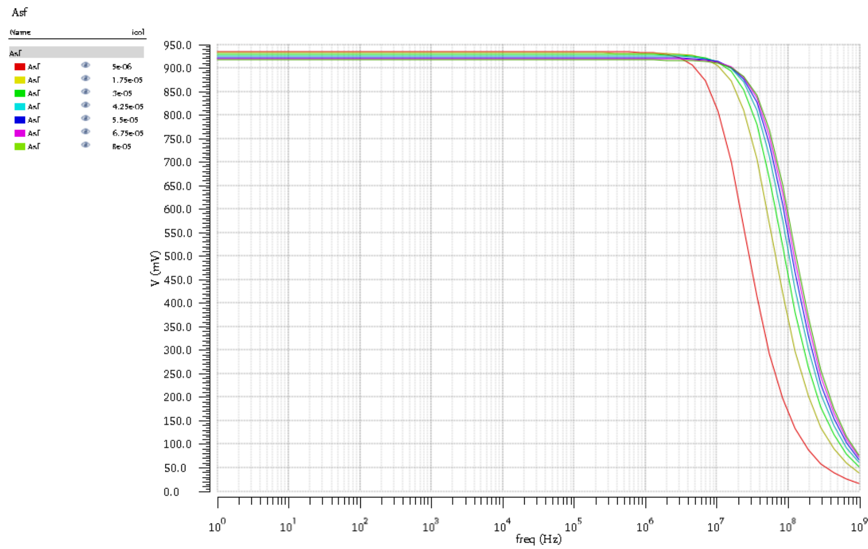


Figure 4.4: AC analysis of the SF with different current source

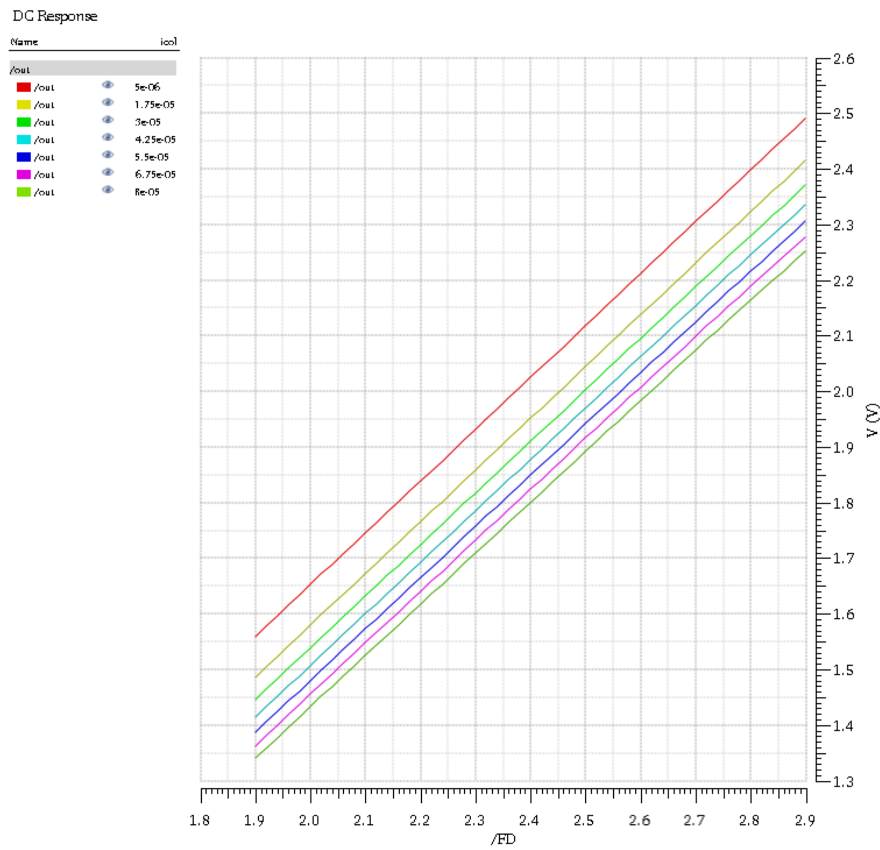


Figure 4.5: DC analysis of the SF with different current source

Device	Param	Noise Contribution	% Of Total
M3.m1	fn	0.000210276	51.88
M8.m1	fn	0.000197224	45.64
M5.m1	fn	2.81836e-05	0.93
M5.m1	id	2.45015e-05	0.70
M8.m1	id	1.81581e-05	0.39

Integrated Noise Summary (in V) Sorted By Noise Contributors

Total Summarized Noise = 0.000291932

Total Input Referred Noise = 0.000313279

Figure 4.6: Noise summary analysis of the SF at $15\ \mu A$ **current source**

Device	Param	Noise Contribution	% Of Total
M3.m1	fn	0.000358816	52.07
M8.m1	fn	0.000341632	47.20
M5.m1	fn	3.24906e-05	0.43
M5.m1	id	1.60957e-05	0.10
M8.m1	id	1.36574e-05	0.08

Integrated Noise Summary (in V) Sorted By Noise Contributors

Total Summarized Noise = 0.000497251

Total Input Referred Noise = 0.000542712

Figure 4.7: Noise summary analysis of the SF at $80\ \mu A$ **current source**

Table 4.1: Floating diffusion parasitic capacitance for the proposed radhard 4T pixel

Descriptions	PARAMETERS	Value
lateral diffusion	L_{diff} (μm)	0.25
Area junction capacitance	CJA ($fF/\mu m^2$)	0.78
gate overlap capacitance (W/L>>1)	CGO ($fF/\mu m$)	0.23
middle active area of two ELT TGs	area of TG middle (μm^2)	0.5508
middle acitve perimeter of two ELT TGs	perimeter of TG middle (μm)	3.896
middle active area of ELT RST	area of RST middle (μm^2)	0.6258
middle active perimeter of RST ELT	perimeter of RST middle (μm)	2.88
parasitic capacitance related to metal wires	CM (fF)	1.7237
FD junction cap	CJ (fF)	0.9177
overlapping cap Cov at RST	Ctov (fF)	0.6624
overlapping cap Cov at TG	Crov (fF)	0.8961
Gate-oxide capacitance	C_{ox} ($fF/\mu m^2$)	5
SF input capacitance ($W/L : 4.97\mu m/0.535\mu m$)	C_{SF} (fF)	1.8522
Total FD parasitic capacitance	C_{FD} (fF)	6.0521
Conversion gain	CG ($\mu V/e^-$)	26.4

4.2 SPI ASIC Module

Serial Peripheral Interface (SPI) is used to communicate between onboard FPGAs and CMOS image sensor chip. The block diagram of the digital module is shown in Figure 4.8. The module is made up of a serial peripheral interface (SPI) slave block and the register bank module. The SPI bus consists of 5 signals, Master Out Slave In (*mosi*), Master In Slave Out (*miso*), the SPI clock (*sck*), Slave Select (*ss*), and reset signal (rst_n).

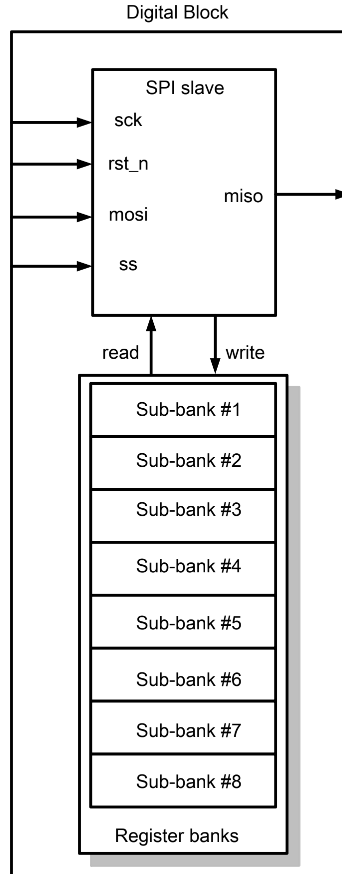


Figure 4.8: Top block diagram of digital module

The onboard FPGAs or micro-controllers perform write and read operations on the register bank modules through SPI interface. The SPI slave module on the CIS chip can receive clock and reset signals from the external (*sck*) and (rst_n) pins respectively. The SPI slave module receives data from the onboard SPI master module on the *mosi* pin. The SPI slave module also sends to the SPI master on the *miso* pin. When the master of the SPI bus wants to initiate a transfer, the *ss* signal is pulled low. Once the *ss* signal is low, the SPI slave module will "listen" on the bus. The master is then free to start sending the data.

The register bank module is made up of eight sub-banks. Each sub-bank is made up of 32 registers and each register has 12 bits. There is a total number of 384 bits in each sub-bank. Each read or write operation must be performed on an entire sub-bank. Therefore, in every read or write transaction from the SPI master

Table 4.2: **List of all pins communicating between SPI master and slave modules**

PIN Name	Function
sck	clock signal provided by the SPI master to SPI slave
rst_n	reset signal from SPI master and active low
ss	select signal for the SPI slave and active low
mosi	data from SPI master to SPI slave
miso	data from SPI slave to SPI master

to the on-chip slave module, an integral multiple of 384 bits of data must be transferred.

$$The\ size\ of\ a\ single\ subbank = 32\ registers \times 12\ bits/register = 384\ bits \tag{4.3}$$

The register configuration files are stored in the host computer. The Universal Asynchronous Receiver/Transmitter (UART) communication is used between the host computer and the on-board FPGA. The transmitted data is organized into a packet. Each packet with 16 bits contains an 8-bit data frame. The SPI slave receives or sends 8 bits of data for every 16 *sck* clock cycles on *mosi* or *miso* pins respectively. Therefore, 48 packets worth of 8-bit data or one byte data is exchanged during a reading or writing operation.

$$The\ number\ of\ packages = \frac{384\ bits}{8\ bits/package} = 48\ packages \tag{4.4}$$

Figure 4.9 shows the six states in the SPI slave state machine: $Reset$, $Init$, *Rcmd*, $Wcmd$, $Wadd$, and *Radd*. *Rcmd* and *Radd* states are associated with a read operation. $Wcmd$ and $Wadd$ states are related to a writing operation. The $Reset$ state is active when any phase of reading or write operation is complete. The $Init$ state is the initial state for the SPI slave module. There is no condition moving from $Reset$ state to $Init$ state.

In the beginning, a reset operation is to initialize the SPI slave, as shown in Figure 4.10. The *rst_n* signal goes low to reset the SPI slave module. Then, select signal, *ss*, is active to enable sending the command to SPI slave. After a specific delay time, a clock signal, *sck*, synchronizes the communication between SPI master and slave. In every 16 clock cycles, SPI master sends one-byte data to SPI slave, aligned at negative edges of first eight cycles. Without any condition, the $Reset$ state will automatically transfer to $Init$ state, and there is no useful data in a reset state, the 16-bit code can be varied from $2'h00$ to $2'hFF$.

4.2.1 Write Mode

The write mode has two phases: one sends the control information (command phase), and the other sends the data to the sub-banks (data phase). Figure 4.11 shows the control information in the command phase with one byte (8 bits). Two MSBs are used to illustrate the status of the state machine in the SPI slave module. The fourth bit is the enable bit for the write operation. The last three LSBs are the sub-bank address bits.

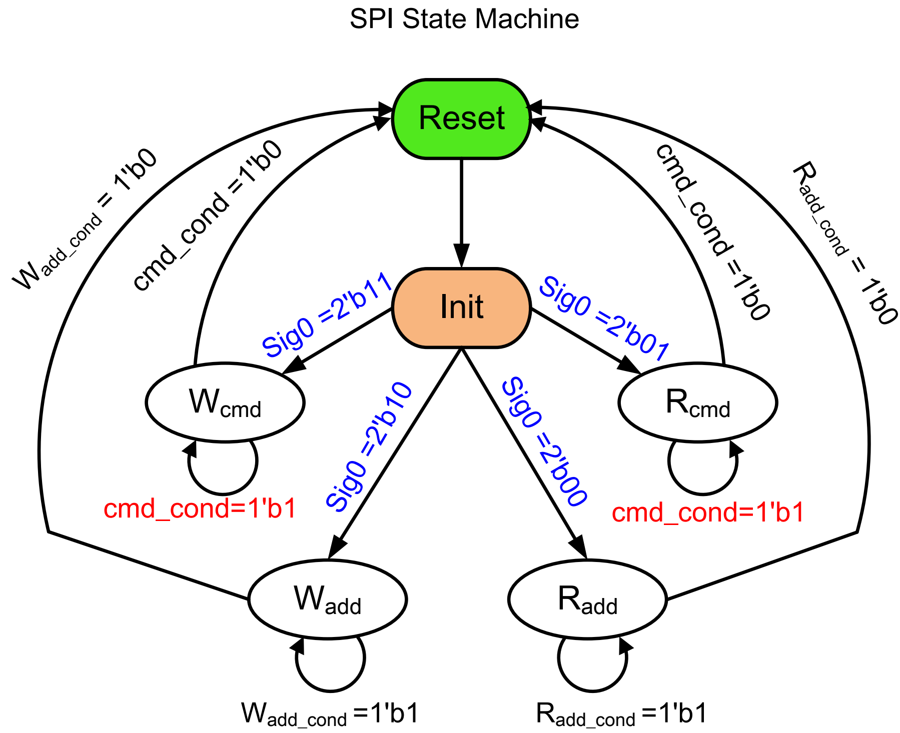


Figure 4.9: SPI slave module state machine

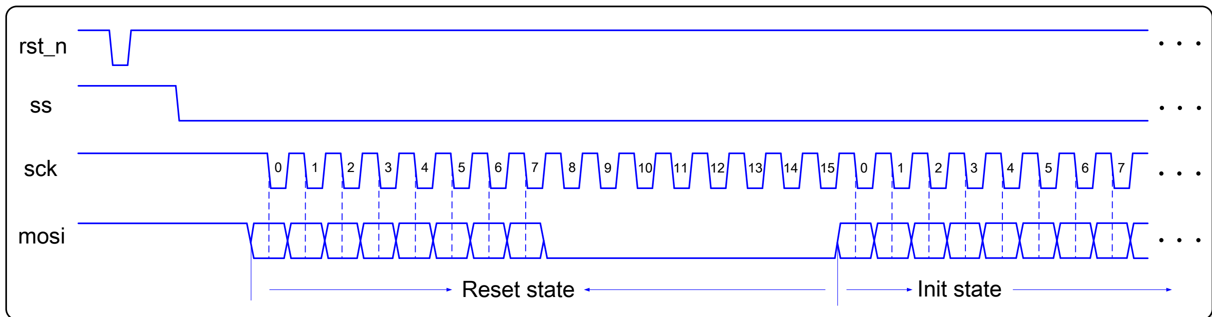


Figure 4.10: Initialization of the SPI bus

4.2.2 Read Mode

The read mode also has two phases: one sends the control information (command phase), and the other sends the data from the onchip sub-banks to SPI master (data phase). Figure 4.12 shows the control information in the command phase with one byte (8 bits). It is similar to the write mode, except that there is no enable bit. The first two MSBs are still used to illustrate the status of the state machine in the SPI slave module, and the last three LSBs are the sub-bank address bits.

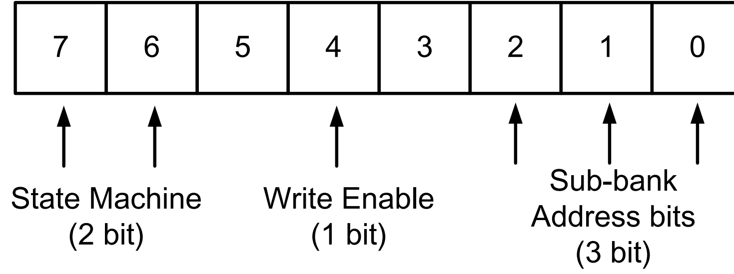


Figure 4.11: One byte command codes for SPI writing operation

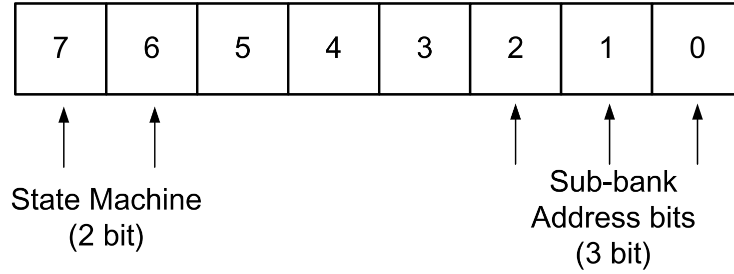


Figure 4.12: One byte command codes for SPI reading operation

4.3 Row Control Block

The row control block, which consists of 256 row decoder blocks and 1024 level shift blocks, is designed for the rolling shutter operation and windowing. Two pointers for windowing select the starting and stopping row address. With the help of the sequencer, different configurations can be efficiently applied to the sensor to operate at different frame rates and change the region of interest.

4.3.1 Row Decoder and Driver

The function of the row control block is to access the pixel array row by row, and then complete three processes: resetting the floating diffusion and photodiode, turning on the transfer gate, and selecting the entire row of pixels. The top block diagram of the row control block is shown in Figure 4.13. Two 10-bit binary codes are used as row addresses of two pointers of the row decoder. Because the dissertation proposed a quadruple readout scheme, four rows at a time can be read out so that only 8-bit binary code is needed. The highest 2 bits enable the row decoder cell to adapt to a higher resolution, so a resolution of 4096 rows by 1024 columns is very possible in the future.

Two pointers, $DinP1$ and $DinP2$, select rows and have these control signals: reset, select, and transfer-gate control. $TXP1$, $RSTP1$, and $SelP1$ are used for $DinP1$. $TXP2$, $RSTP2$, and $SelP2$ are used for $DinP2$. Two global signals, $Global_RST$, and $Global_TX$, are prepared at the initial state to reset all floating diffusion and photodiodes in the pixel array. Instead of using two standard overlapping clock signals, two control signals, $ClkMaster$ and $ClkSlave$, are clock signals used in shift registers. All these signals are fed into a buffer cell before driving row decoder cells.

Single row decoder is shown in Figure 4.14. For two pointers implementation, each cell has two-row addresses, $A < 9 : 0 >$ for start pointer and $B < 9 : 0 >$ for stop pointer. The 10-bit decoder consists of three NAND gates and one NOR gates. The output of the start decoder or stop decoder is fed into the start shift register or stop shift register, respectively. Consequently, the vertical readout window can be sized by setting the start pointer and stop pointer, which independently roll down row by row.

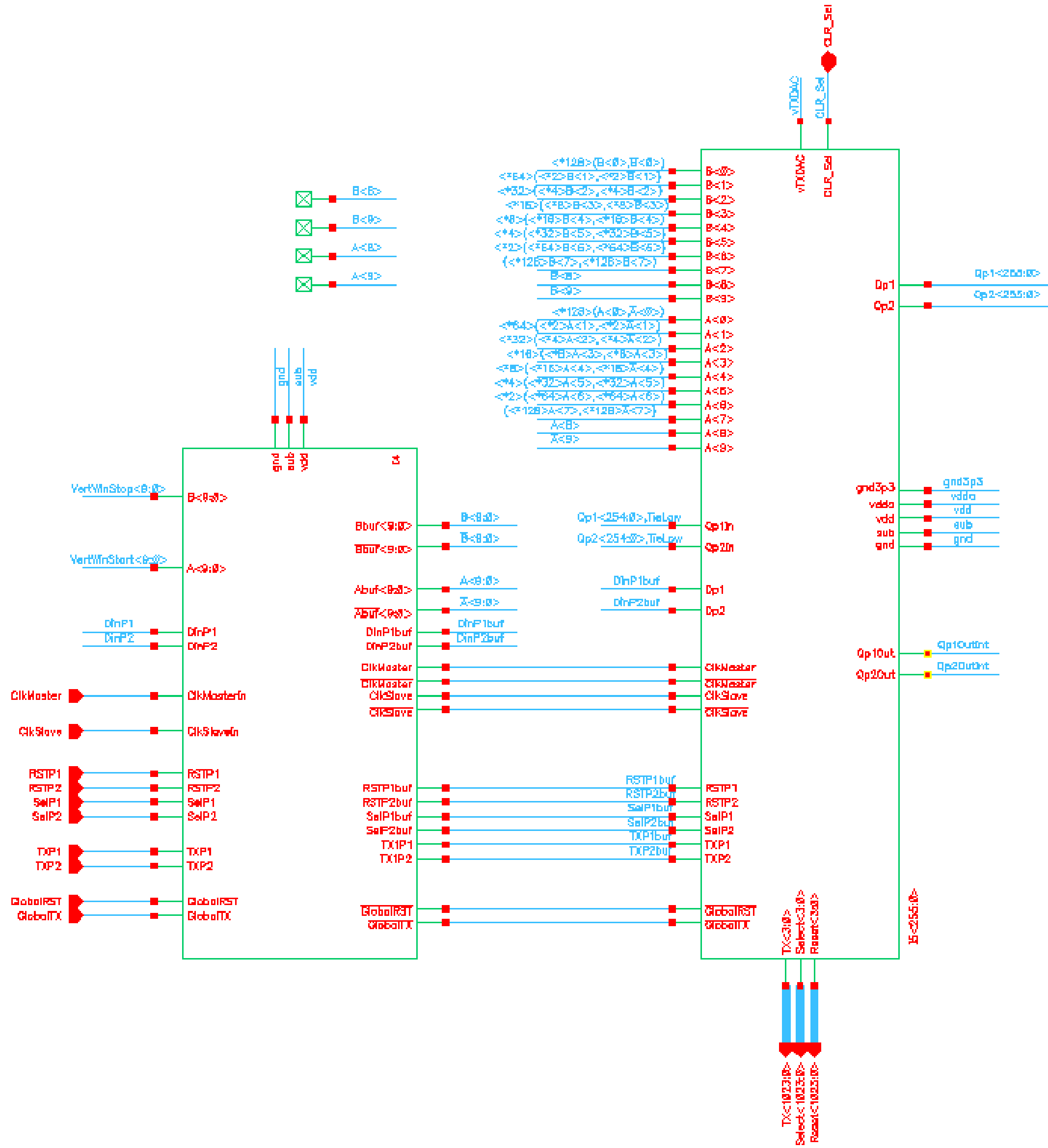


Figure 4.13: Top block diagram of row control block

Three control signals are needed for each row of pixels, and every four rows operate at the same line time, so their control signals are connected. Figure 4.15 illustrates the block diagram of the row driver cell. Each cell has three drivers for controls signals used in each pixel: *Reset* to control the reset transistor, *Select* signal to control the row select transistor, TX signal to turn the transfer gate on or off.

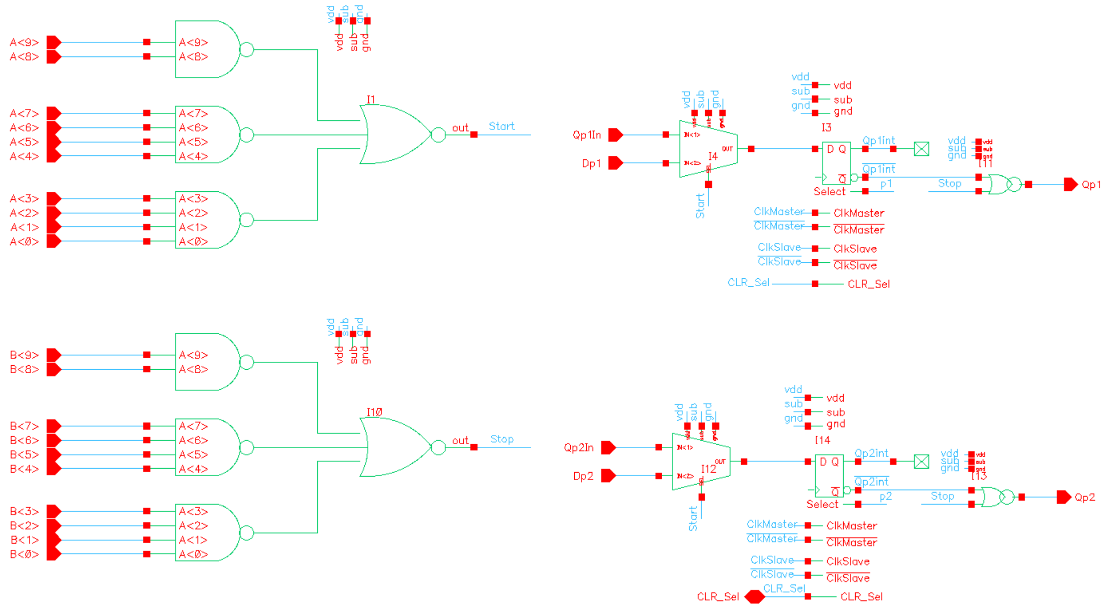


Figure 4.14: Block diagram of one row decoder

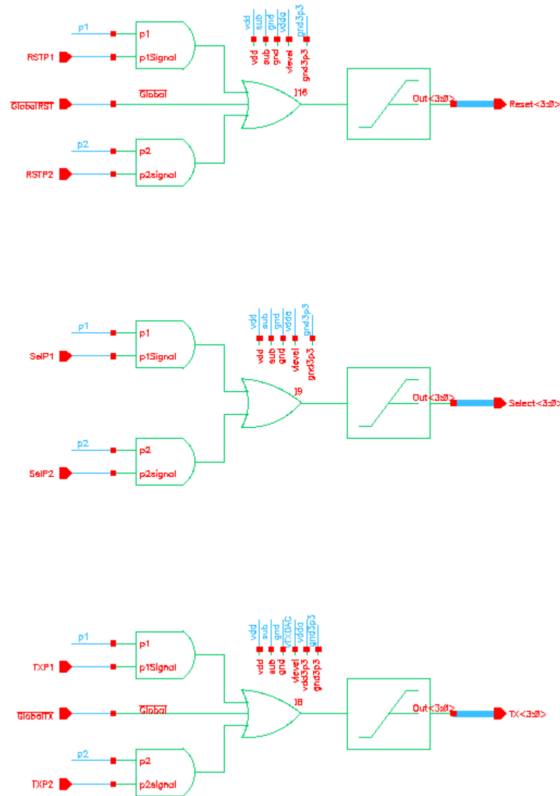


Figure 4.15: Block diagram of row driver cell

The row drivers of TX and reset signals comprise two 2-input NAND gates, one 3-input AND gate, one level shifter, and four output buffers. The row driver of select signal comprise two 2-input NAND gate, one 2-input AND gate, one level shifter, and four output buffers. These three row drivers have two pointer signals and two sets of control signals from the row decoder. However, the only difference is that the select driver does not have the $Global_*$ signals, $GlobalRST$ and $GlobalTX$. The $Global_*$ is active low; when $GlobalRST$ or $GlobalTX$ is enabled, the output of $RST < 3 : 0 >$ or $TX < 3 : 0 >$ will be active for all pixels simultaneously. Since row drivers are located between the row decoder and the pixel array, two power domains, 1.8V and 3.3V, are employed. Hence, thin-oxide transistors can be used in logic gates, and level shifters are designed by thick-oxide transistors to shift the voltage signal up to $3.3V$.

Figure 4.16 is a schematic of the level shifter used in the row driver. It consists of two thick-oxide PMOSs and two thick-oxide NMOSs. When the input (in) of the level shifter is at a high logic level, 1.8V, and the complementary input signal ($\overline{in}$) stays at a low logic level, the output node (out) is charged to a high potential, $vlevel$, which is adjustable from $2.5V$ to $4.5V$. When the input (in) is at the low logic level, and the complementary input signal will be at the high logic level, the output node (out) is discharged to a low potential.

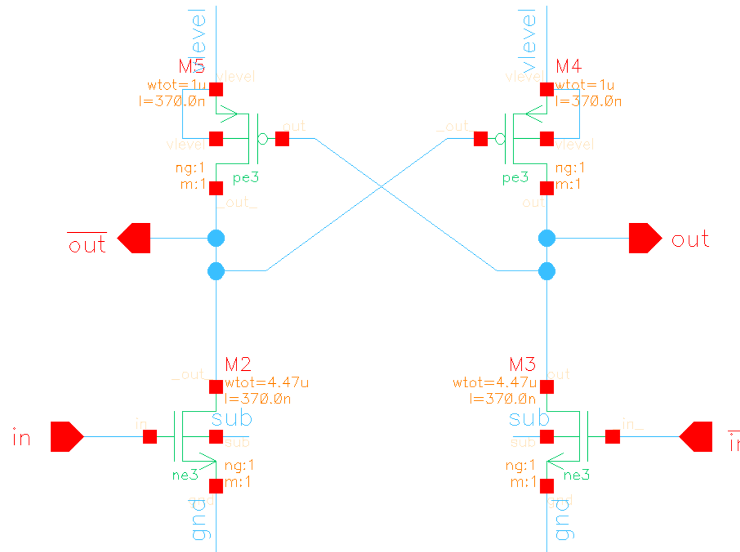


Figure 4.16: Schematic of the level shifter design

Transient analysis of the level shifter was performed with 2 pF load capacitor as shown in Figure 4.17. The simulation result shows that the propagation delay is 0.84 ns. The rising and falling time is 2.7 ns and 580 ps, respectively. Hence, the level shift is good enough for the prototype sensor pixel operation.

The layout of the level shifter is illustrated in Figure 4.18. The enclosure-layout technique and P-type guardring are used to protect the transistors from TID effects.

4.3.2 Rolling Shutter

The rolling shutter (RS) mode in this dissertation is designed to scan every four rows of pixels from top to bottom. The entire sensor array is converted four rows at a time since each column has four ADCs working in parallel. So, every four rows will start and end their exposure offset slightly in time from the preceding four rows. If the CMOS image sensor works at the maximum frame rate of $10,000\ fps$, the readout time of a single line in a 1024×1024 pixel array, and consequently the offset between adjacent four rows exposure time is

$$\begin{aligned} Frame\ Time &= t_{FT} = \frac{1}{Frame\ Rate} = 100\ \mu s \\ Line\ Time &= t_{LT} = adjacent\ time\ offset = \frac{t_{FT}}{1024\ rows} \times 4 = 390.625\ ns \end{aligned} \tag{4.5}$$

The mechanism of rolling shutter mode is illustrated in Figure 4.19. Four rows of pixels are integrated at the same exposure time and simultaneously selected to be read out and converted to digital codes with the help of four column-parallel A/D converters. Hence, in each pixel of every four rows, control signals of those three transistors (reset, transfer and row select) have the same timing.

Figure 4.20 illustrates the control timing in each pixel. As discussed in the previous section, two pointers exist in row decoder block to choose the starting and stopping rows. For each pixel, the first pointer activates RST and TX signals together to turn on reset and transfer gate transistors for resetting the photodiode. When the second pointer arrives, the RST signal goes high, but TX stays low in order to reset floating

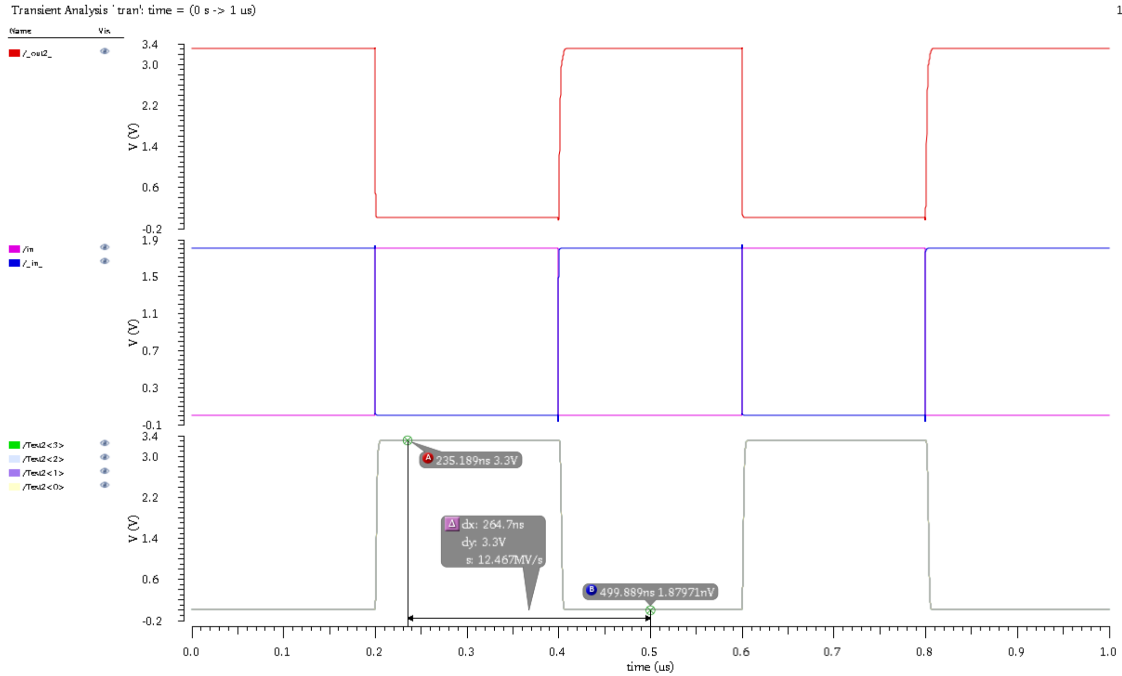


Figure 4.17: Transient analysis of the level shifter with a 2 pF load capacitor

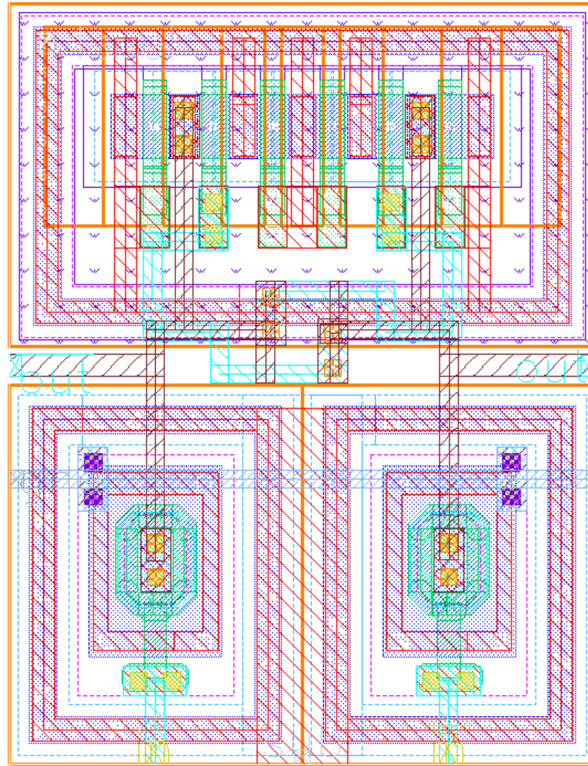


Figure 4.18: Level shifter layout with radhard NMOSs

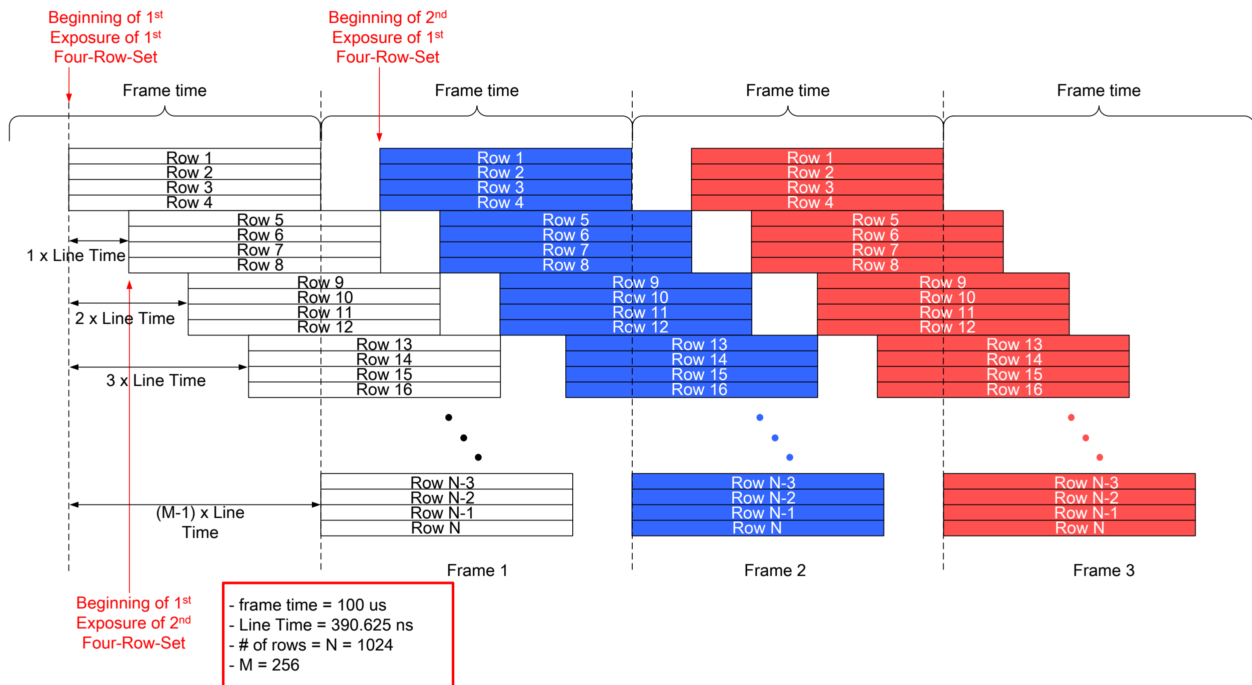


Figure 4.19: Rolling shutter mechanism

diffusion. Then, by turning on row select transistor, the in-pixel source follower will transfer the reset voltage from floating diffusion to one column line. $PixSample$ in the readout circuit is turned on twice to achieve correlated double sampling. Between these two sampling phases, TX is active to turn on the transfer gate transistor for transferring the charge from the photodiode to the floating diffusion node.

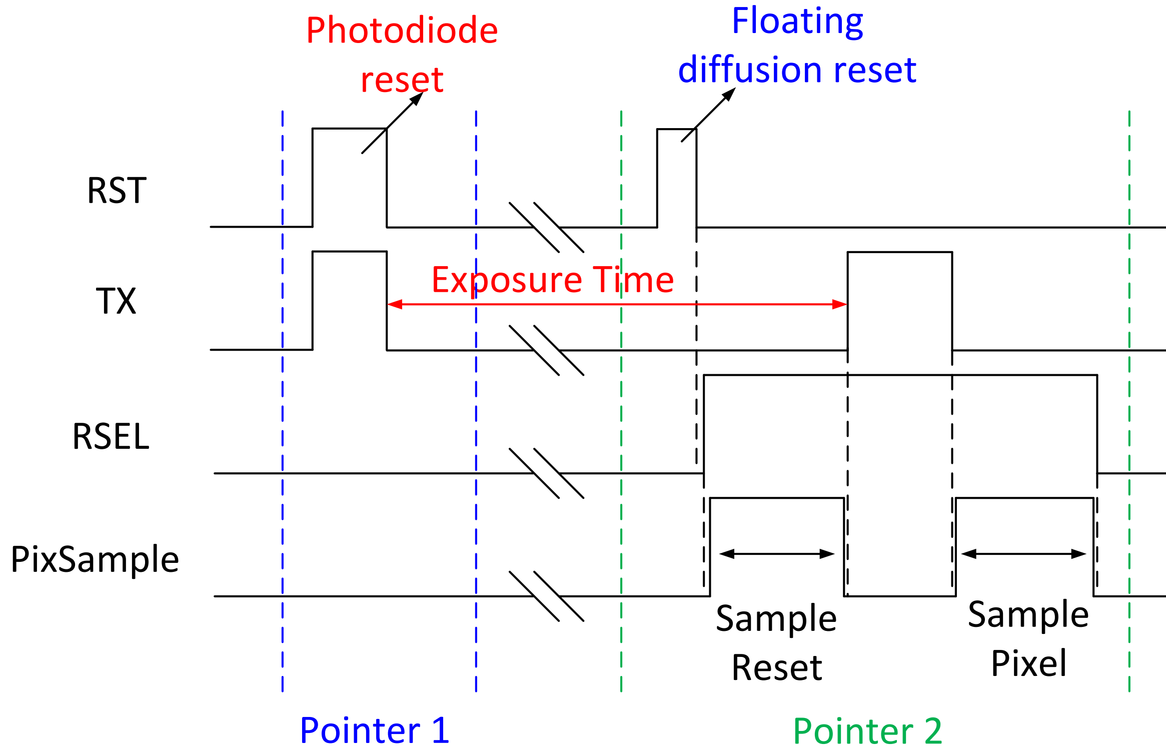


Figure 4.20: Timing of control signals in each pixel of every four rows

For the whole pixel array, the control timing in terms of two pointers is illustrated in Figure 4.21. The rolling shutter process starts as the first pointer, $P1$, becomes active at the start row, which is the first 4-row in the example. Two signals, RST, and TX, reset the photodiode to prepare a light capture. The shift register in the row decoder makes the $P1$ roll down one row at a time. When the second pointer, $P2$, becomes active at the same start row, the selected four rows will have a floating diffusion reset, a charge transfer process, and a readout operation. The time interval between the actions of $P1$ and $P2$ is equal to the exposure time for every 4 rows of pixels. The row decoder rolls down the $P2$ one row at a time to make sure every 4 rows have the identical exposure time. When the first pointer or the second pointer reaches the stop row, it re-starts from the start row to begin another rolling process.

The simulation using the Cadence schematic model in 0.18 μm process demonstrated the functionality of the rolling shutter mode, as shown in Figures 4.22 and 4.23.

The main drawback of a rolling-shutter CMOS imager is that the start and stop of the exposure time are slightly shifted row by row. The mechanism causes the deformation of fast-moving objects, which is called spatial distortion. This distortion can be more apparent in cases where larger objects are moving at a rate

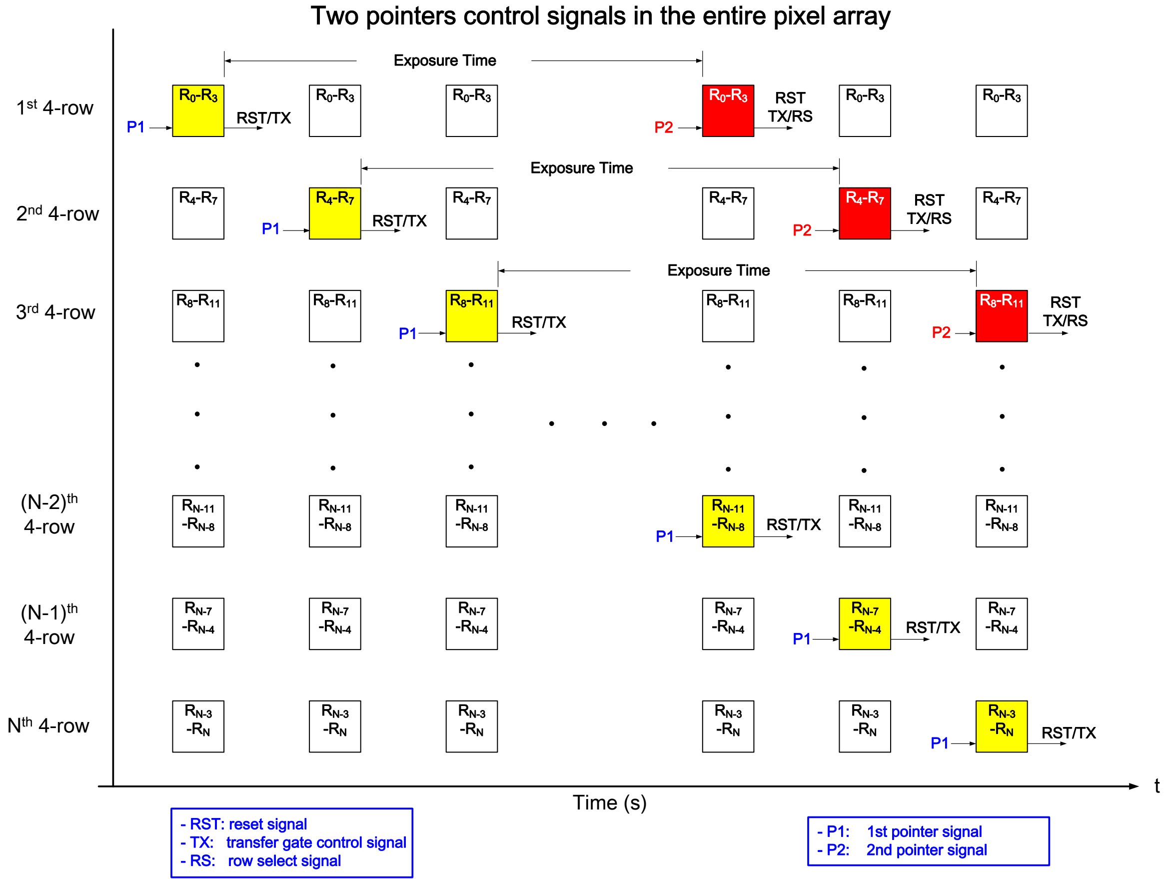


Figure 4.21: Timing of two pointers' control signals in the entire pixel array

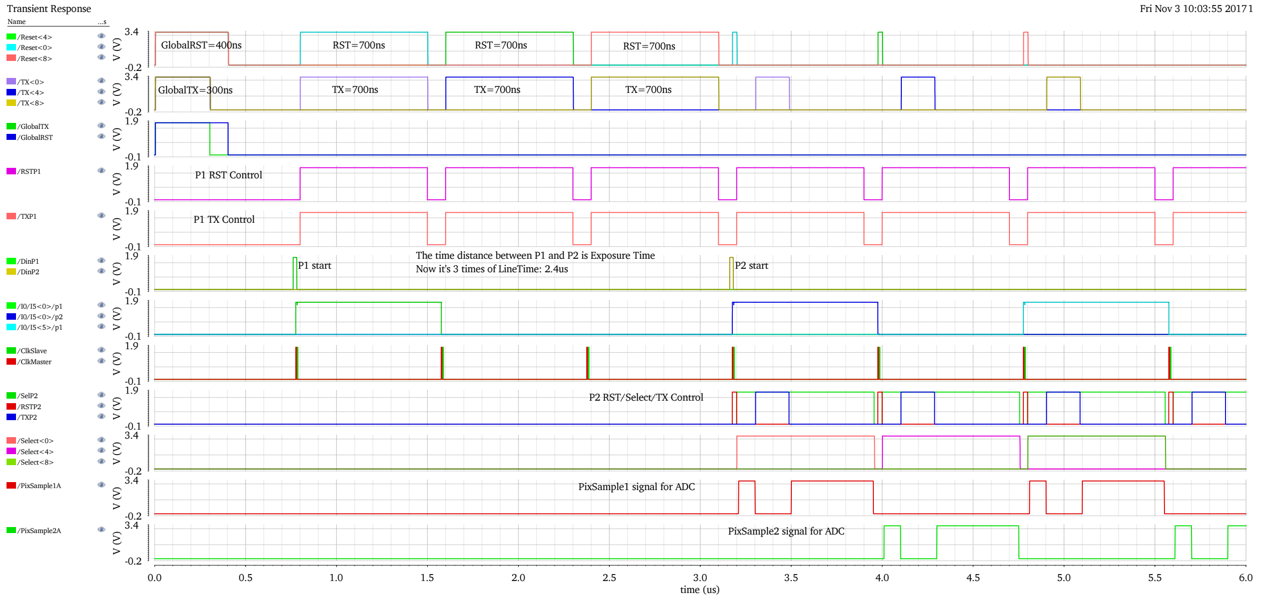


Figure 4.22: Simulation of control signals from row decoder at 800 ns line time

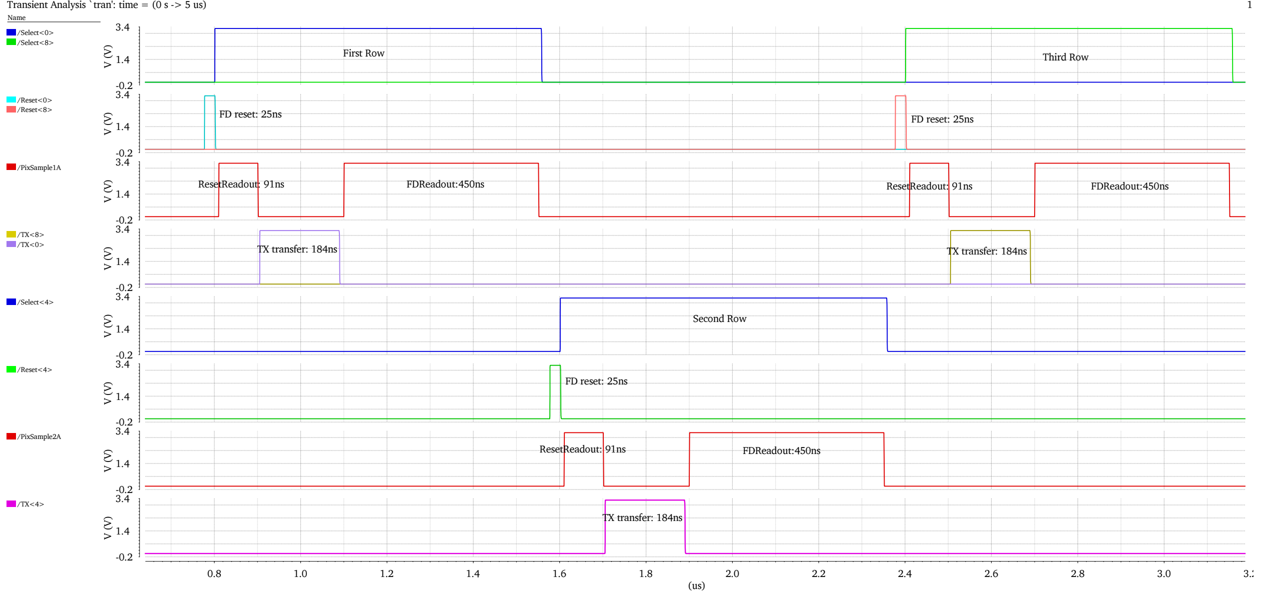


Figure 4.23: Simulation of control signals for pixels at 800 ns line time

that the image readout cannot match. However, if the object is relatively small and moves at a rate that can be over-sampled by a fast frame rate, the spatial distortion can be negligible.

Imaging moving objects requires consideration for the object's size and velocity in order to sample and avoid blur properly. If a blur of no more than 10% is acceptable, the required exposure time for imaging sensors can be calculated as

$$T \leq \frac{\Delta L}{10 \times v} \tag{4.6}$$

where T is the required exposure time to avoid blur, ΔL is the object's length, and v is the object's velocity.

A straightforward way to determine if the object will cause rolling shutter spatial distortion is to use the logic: if exposure time is smaller than object height (or # of rows) * line time, then the imager with rolling shutter will expect spatial distortion.

To illustrate this rule, consider the example of using the proposed image sensor with $10,000$ fps and operating at rolling shutter in a slide scanner. The sensor size of the proposed CIS is 768×1024, and the line time is 400 ns. Assume a tissue with 8 mm height and at 150 mm/s scanning velocity. The required exposure time to avoid a 10% blur must be smaller than 5.3 ms. The frame time of the sensor is 256×400 $ns = 102.4$ μs. Due to 102.4 μs is much smaller than 5.3 ms, therefore, the rolling shutter spatial distortions are not expected.

4.3.3 2D Windowing

Windowing is a technique that enables CMOS imagers to directly read out a selected group of pixels. It is used to restrict the image acquisition to a region of interest rather than the full image. It can increase the readout speed by selecting pixels of interest and shorten the readout time in one smaller frame. Therefore, the proposed CMOS image sensor could achieve a higher frame rate by choosing a smaller window of interest, instead of using the full resolution.

As shown in Figure 4.24, a fully configurable window can be selected for readout by using X and Y scanner to change X and Y dimension. The parameters to configure this window are:

1. Y_start: The starting line of the readout window.

2. Y_end: The end line of the readout window.

3. X_start/X_end: It is the start or end position of the X readout.

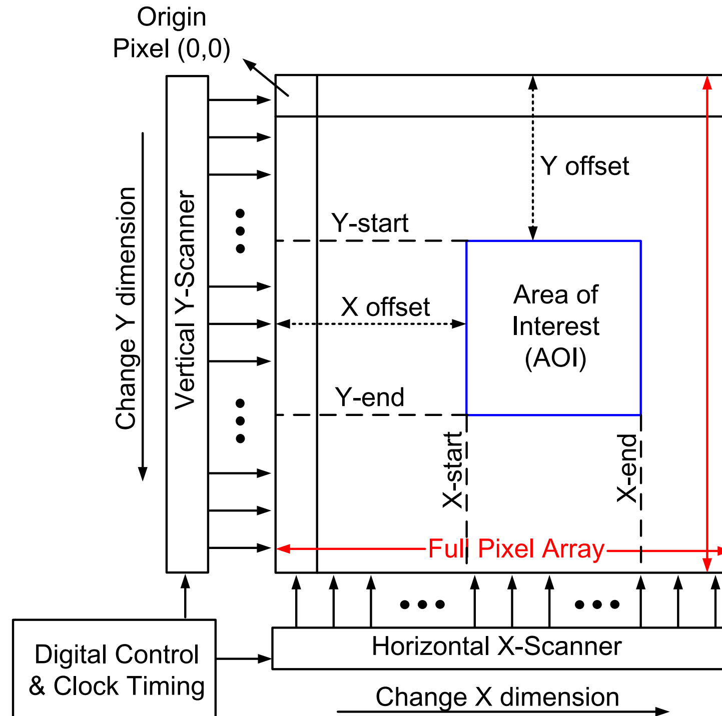


Figure 4.24: Selected window of interest for readout

The proposed CMOS image sensor employs a novel two-dimension(2D) windowing feature to digitally zoom in on a rectangular region of the sensor array without a horizontal X-scanner. For the vertical dimension, the proposed readout circuitry discussed in Section 4.4, enabling the sensor to read four rows of pixels out at one time, makes the difference between the start and stop address as an integral multiple of four. $VertWinStart < 9:0 >$ and $VertWinStop < 9:0 >$ in the row decoder define the Y_start and Y_stop, respectively.

Without a horizontal X-scanner, on-chip X windowing is impossible. The off-chip method is the only way to change the X dimension. Two methods could be applied in the sensor. In the first, software method can select how many columns of data constitute an image. The second method is to select how many I/Os connect to the onboard microcontroller or FPGAs. The first method does not improve speed. The second, however, by deciding how many fast data FPGAs need to transfer to the PC, could enables a faster speed. Also, because each I/O on the top and bottom of imager provides series data from 16 columns, the difference between the starting and stopping address is an integral multiple of 16.

4.4 Column Readout Design

4.4.1 Analog Time-Interleaving Correlated-Double Sampling

Correlated double sampling (CDS) is a noise reduction technique used in CMOS image sensors. In CMOS active pixel sensors, reset noise (kT/C noise), flicker noise, and fixed pattern noise from the pixel level can be reduced by the CDS technique through subtracting the reset and pixel signals for each pixel cell.

Typically, each column in every image sensor has CDS circuitry that consists of several sampling switches, two capacitors, C_S and C_R, and a fully differential amplifier as shown in Figure 4.25. Two sample and hold circuits sample reset and pixel signals sequentially. Then, at ϕ_Y phase, the amplifier input becomes $V_{PIX} - V_{RST}$. Until the subtraction signal is transferred to the subsequent data converter, the next phase of sampling has to wait.

There are two phases, sampling and transferring, existing before the column-ADC can start the data conversion. During the sampling phase, pixel and reset voltage signals are sampled separately onto column-sampling capacitors. During the transferring phase, the voltage difference is fed into column-ADCs to complete the digitization.

The timing consideration of these two phases is different. The sampling phase needs to consider two sampling operations including the setting time in column lines, charge transfer time in the pixel and reset time for the floating diffusion node, as shown in Figure 4.25. The transferring phase is limited by the bandwidth of the operational amplifier. To increase the frame rate, the better efficient method is to start the sampling phase of next readout row when the transferring phase of the current readout row is running. Otherwise, the sampling phase of the next readout row has to wait for completing the transferring phase of the current readout row. Therefore, a robust analog time-interleaving CDS (ATI-CDS) is proposed in this dissertation.

The proposed time-interleaving CDS block, illustrated in Figure 4.26, consists of four sampling capacitors, five switches, one unity gain buffer, and one reference voltage, V_{RefAmp}. Instead of using two S/Hs to store pixel and reset voltages separately, the proposed CDS technique is achieved by taking advantage of one S/H and a floating-node capacitor.

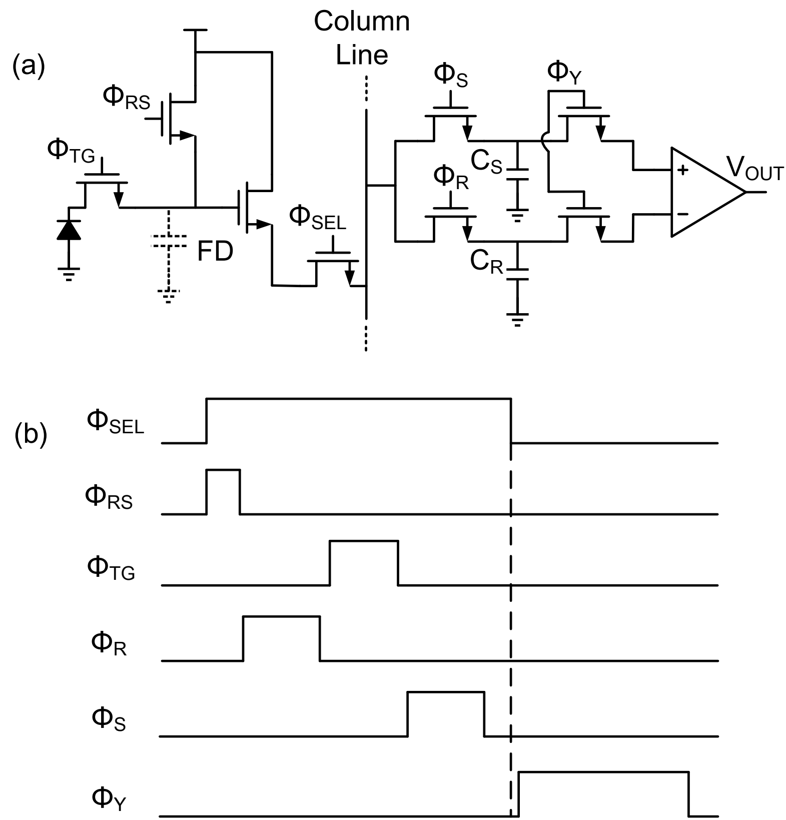


Figure 4.25: (a)Traditional CDS with 4T APS and (b)timing diagram

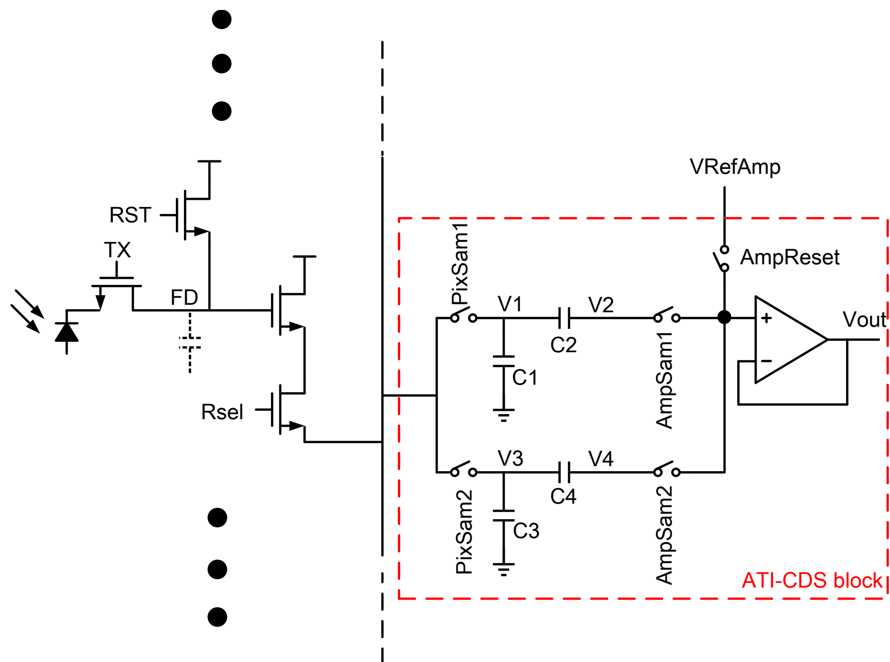


Figure 4.26: Proposed analog time-interleaving CDS circuit

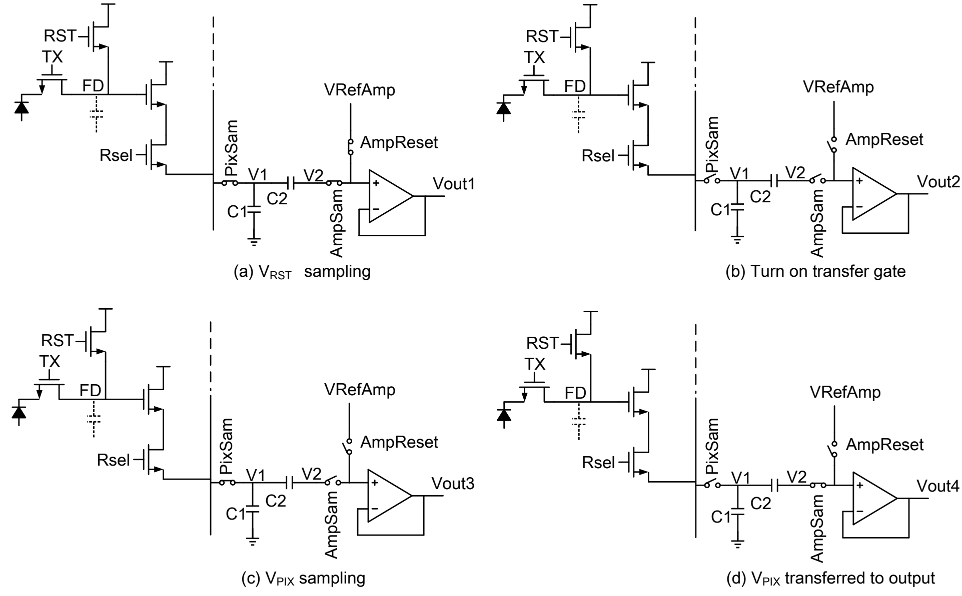


Figure 4.27: Operation of proposed CDS technique

Before discussing ATI-CDS, it is important to focus on the proposed CDS idea. Four steps are involved, as shown in Figure 4.27. Assume a rolling-shutter mode controls the pixel array. The first step is to sample V_{RST}. After resetting the floating diffusion of a specific row of 4T pixels and turning on that row of Rsel switches, PixSam and AmpSam switches are turned on at the same time. Meanwhile, the switch AmpReset is turned on to connect reference voltage, V_{RefAmp}, on the input node of the unity gain buffer. So, the output voltage, V_{out1}, is equal to V_{RefAmp}. Those two sampling capacitors, $C1$, and $C2$, have different bottom-plate connections. After a while, the top plate of $C1$ and $C2$ settles to V_{RST}. The second step is to turn on the transfer gate to move the charges in the photodiode to the floating diffusion. Before starting the charge transfer, all other switches must be turned off to keep the sampled signals on the capacitors unchanged. Then, the V_{pixel} sampling starts by turning on PixSam switch and keeps AmpSam and AmpReset off. The top plate voltage, $V1$, becomes equal to V_{pixel}. Because the bottom plate of $C2$ is floating, the voltage, $V2$, changes to $V_{RefAmp} - V_{RST} + V_{pixel}$. As a result, the difference value between reset and pixel voltages is achieved. The last step is to transfer the voltage difference to the buffer's output. After turning the PixSam switch off, turn on the AmpSam switch to make $V_{out4} = V_{RefAmp} - V_{RST} + V_{pixel}$.

An ideal LTspice model of proposed CDS was built to verify the functionality as shown in Figure 4.28. A pulse voltage source represents the signal on the column line. The reset voltage is set to be $3V$, and the pixel value is $2.5V$. The reference voltage is $1.4V$, so that the output voltage of the amplifier is supposed to be $1.4V + 2.5V - 3V = 0.9V$. The simulation results in Figure 4.29 show that V_{out} is $1.3999984V$ turning on the AmpSam switch for the first time. The second time that V_{AmpSam} rises, the output voltage becomes $900mV$. The voltage difference is the same as the subtraction between reset and pixel voltages. Therefore, the proposed CDS technique can be achieved.

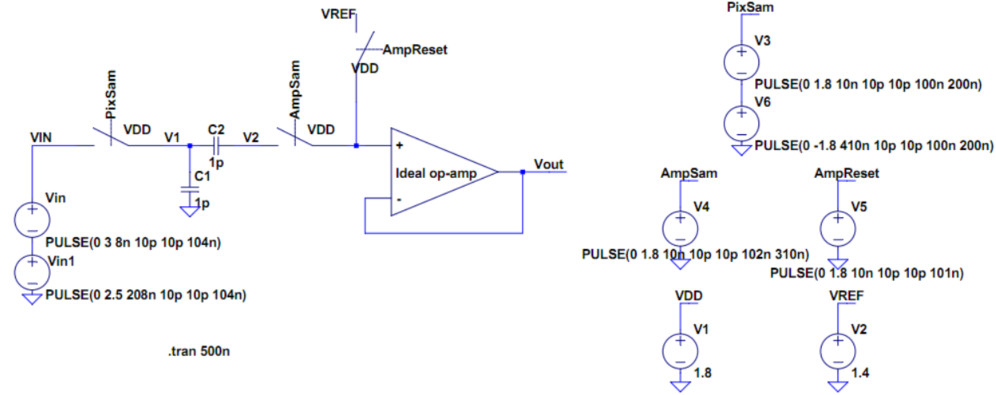


Figure 4.28: LTspice model of proposed CDS technique

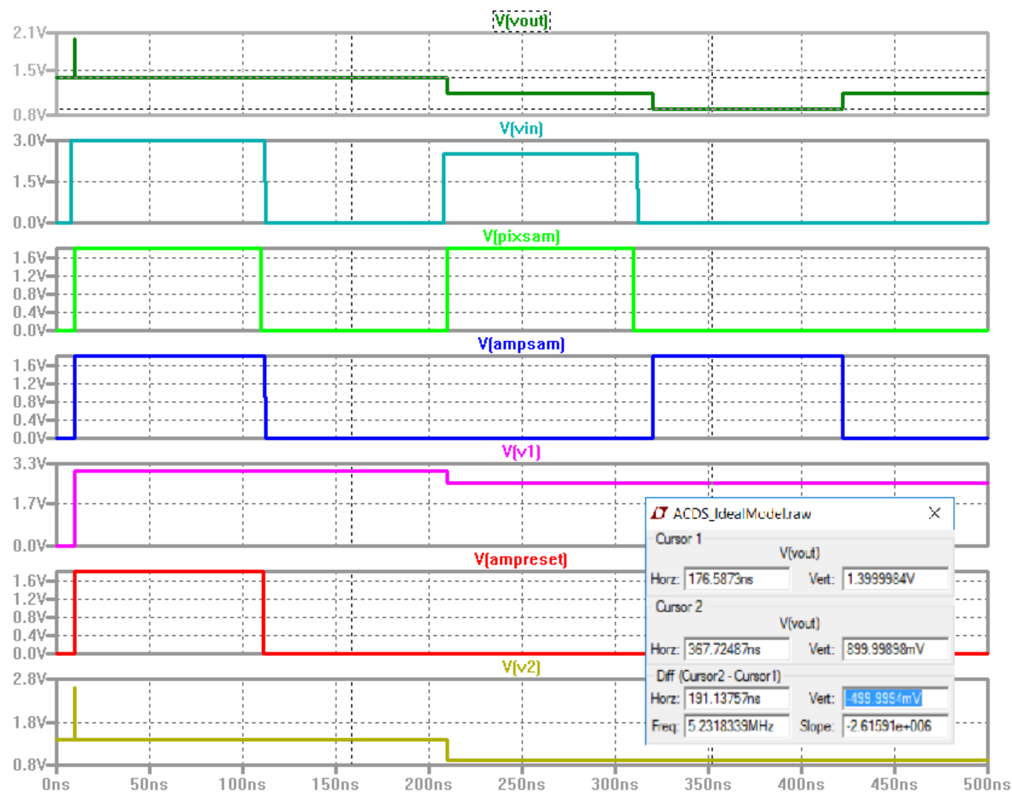


Figure 4.29: Simulation result of the CDS LTspice model

Figure 4.30 illustrates six phases of the proposed ATI-CDS. Assume each column readout block has a single ATI-CDS circuit. In its architecture an ATI-CDS circuit has two identical S/Hs, each one consisting of two capacitors and two switches. The two S/Hs share the input node connected to the column line and output node connected to the input of the unity gain buffer.

More details of each phase are listed below:

1. $phase(a)$: Sample N-th V_{RST} on the top plates of $C1$ and $C2$ by turning on PixSam1 and AmpSam1. Meanwhile, turn off PixSam2 and AmpSam2.

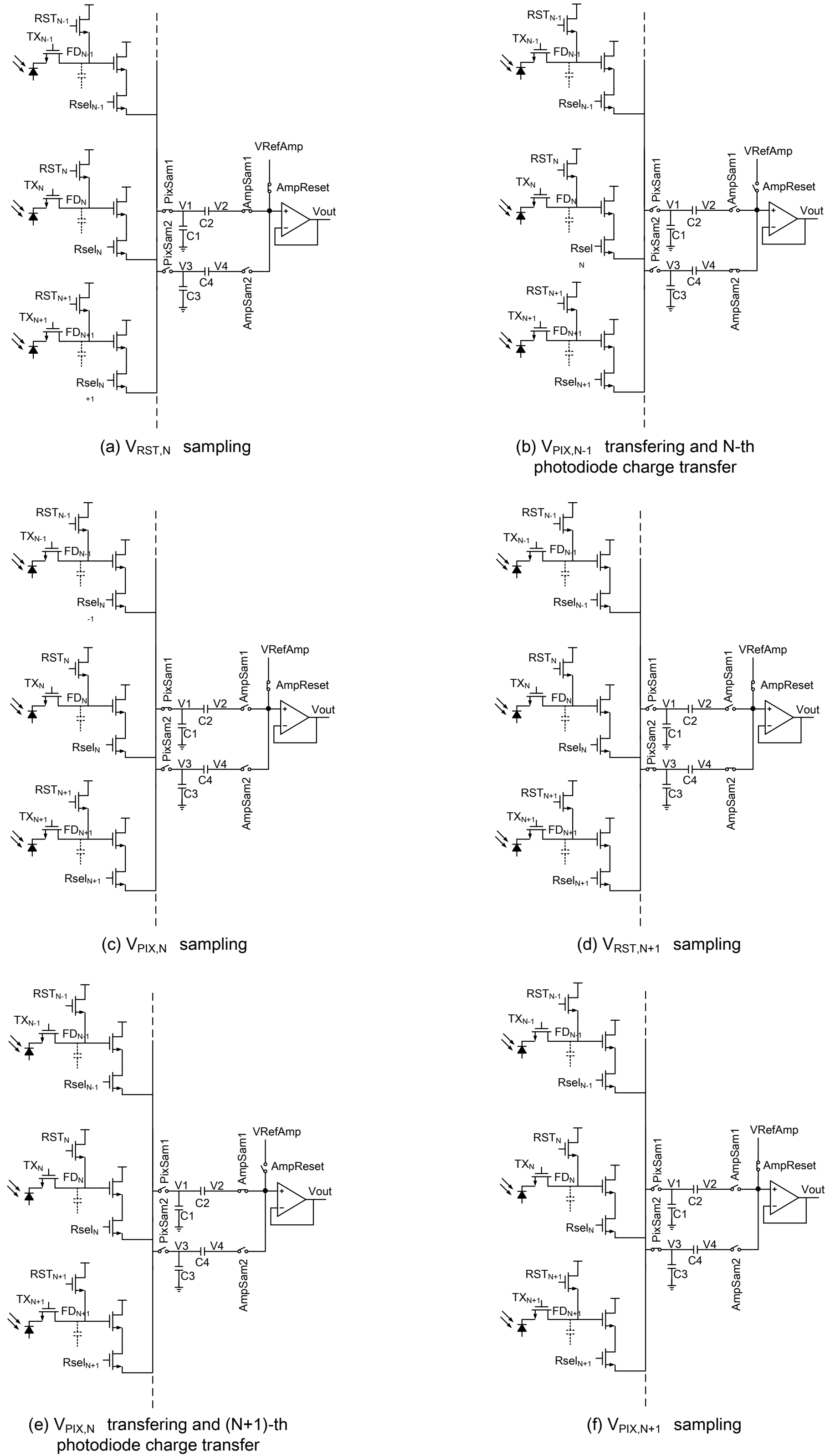


Figure 4.30: Operations of proposed ATI-CDS technique

2. $phase(b)$: Transfer (N-1)-th V_{PIX} on the bottom plate of $C4$ to the output of the buffer by turning on AmpSam2 and turning off the other switches. At the same time, turn on TX on the N-th row to transfer the photodiode charges to the floating diffusion.

3. $phase(c)$: Sample N-th V_{PIX} on top plate of $C1$ capacitor by turning PixSam1. AmpReset is turned on, ready for the next phase.

4. $phase(d)$: Sample (N+1)-th V_{RST} on top plates of $C3$ and $C4$ by turning on PixSam2 and AmpSam2. Meanwhile, PixSam2 and AmpSam2 are off.

5. $phasse(e)$: Transfer N-th V_{PIX} on the bottom plate of $C2$ to the output of the buffer by turning on AmpSam1 and turning off the other switches. At the same time, turn on TX on the (N+1)-TH row to transfer the photodiode charges to the floating diffusion.

6. $phase(f)$: Sample (N+1)-th V_{PIX} on top plate of $C3$ by turning PixSam2. The AmpReset switch is on, ready for the next phase.

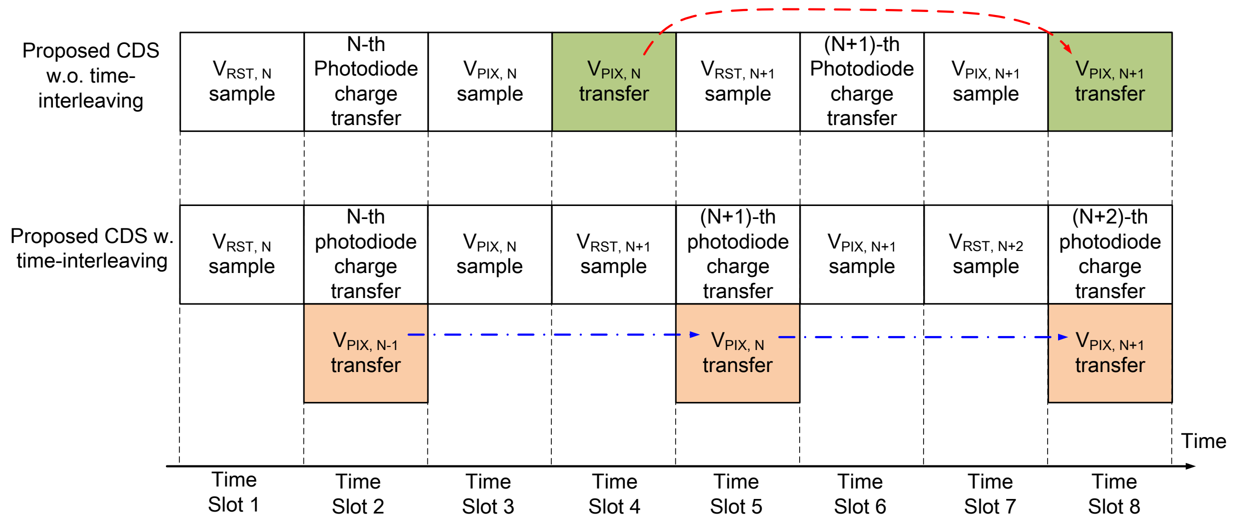


Figure 4.31: A comparison of the proposed CDS technique with- and without time-interleaving

To better understanding why the ATI-CDS has superior speed, the ATI-CDS technique was compared to proposed CDS without time interleaving, as shown in Figure 4.31. Among the eight time slots, ATI-CDS could transfer 3-pixel values to the output of the buffer, which provides one more sample and only takes two-thirds of the time compared to proposed CDS without time interleaving.

In addition, ATI-CDS allows the difference between the reset voltage and the pixel voltage to be sampled in column readout circuitry in parallel, which removes kT/C noise on the floating diffusion node, and suppresses the source follower 1/f noise.

4.4.2 Switched-Capacitor Programmable Gain Amplifier

In the analog front-end block, the programmable gain amplifier aims to maximize sensor array signal levels to the subsequent ADC's dynamic range. This dissertation proposed a switched-capacitor programmable gain amplifier (SC-PGA) with four gain settings available through three registers in the sequencer block. This amplifier allows four different gains (1×, 2×, 4×, or 8×).

A conceptual view of switched-capacitor amplifiers is shown in Figure 4.32(a). Two phases commonly take place in switched-capacitor amplifiers: sampling and amplification. A clock signal is required in the circuit to activate each phase.

Figure 4.32(b) illustrates the implementation of the proposed SC-PGA. The sampling block uses the ATI-CDS technique discussed in Section 4.4.1. The amplification block is a non-inverting switched-capacitor amplifier with different gain settings.

In the discussion of the sampling phase in the previous section, the amplification phase was implemented by a unity-gain buffer. This section analyzes the amplification phase using the proposed SC-PGA. To simplify the analysis, the proposed analog CDS technique is applied in the sampling phase, rather than ATI-CDS, as shown in Figure 4.33.

Analyzing the feedback amplifier in Figure 4.33, which is a series-shunt feedback, with open-loop gain, A_{OL}, and a feedback network (β network), which includes four capacitors ($C_F, C_{G0}, C_{G1}, C_{G2}$) and five switches. The closed-loop gain of the amplifier is

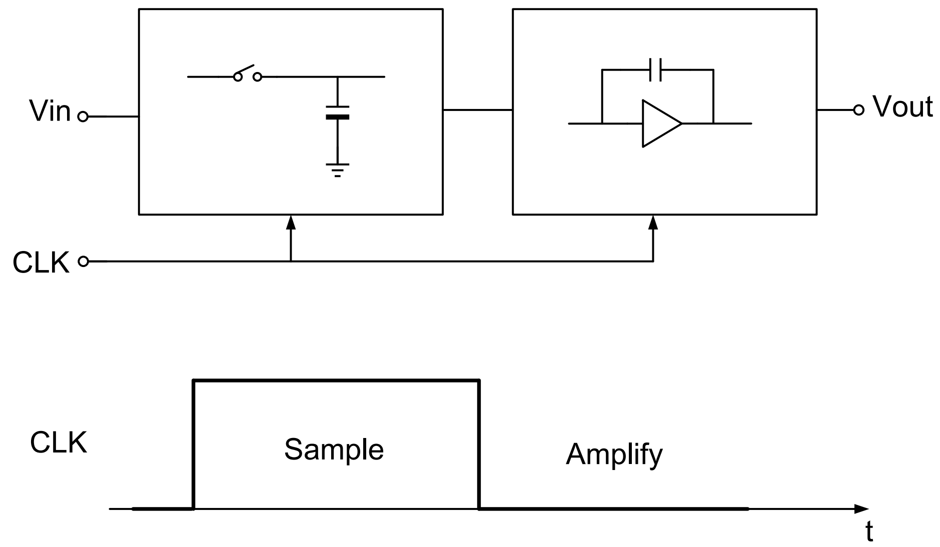
$$\begin{aligned} A_{CL} &= \frac{V_{out}}{V_x} = \frac{A_{OL}}{1 + A_{OL} \cdot \beta} \\ \beta &= \frac{V_f}{V_{out}} = \frac{G2 \cdot Z_{C_{G2}} + G1 \cdot Z_{C_{G1}} + G0 \cdot Z_{C_{G0}} + \overline{G0} \cdot Z_{C_F}}{G2 \cdot Z_{C_{G2}} + G1 \cdot Z_{C_{G1}} + G0 \cdot Z_{C_{G0}} + Z_{C_F}} \end{aligned} \tag{4.7}$$

Notice that as open-loop gain, A_{OL}, approaches infinity, the closed-loop gain approximates to

$$A_{CL} \approx \frac{1}{\beta} = \frac{G2 \cdot Z_{C_{G2}} + G1 \cdot Z_{C_{G1}} + G0 \cdot Z_{C_{G0}} + Z_{C_F}}{G2 \cdot Z_{C_{G2}} + G1 \cdot Z_{C_{G1}} + G0 \cdot Z_{C_{G0}} + \overline{G0} \cdot Z_{C_F}} \tag{4.8}$$

The impedance of those different capacitors in β network are given as

$$\begin{aligned} Z_{C_{G0}} &= Z_{C_F} \\ Z_{C_{G2}} &= 4 \cdot Z_{C_{G0}} \\ Z_{C_{G1}} &= 2 \cdot Z_{C_{G0}} \end{aligned} \tag{4.9}$$



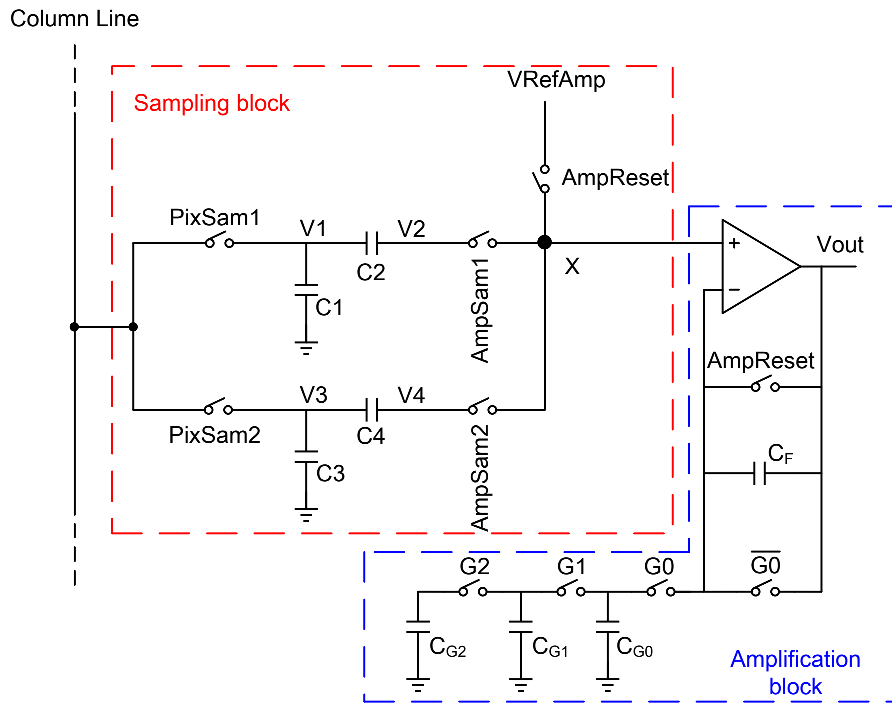
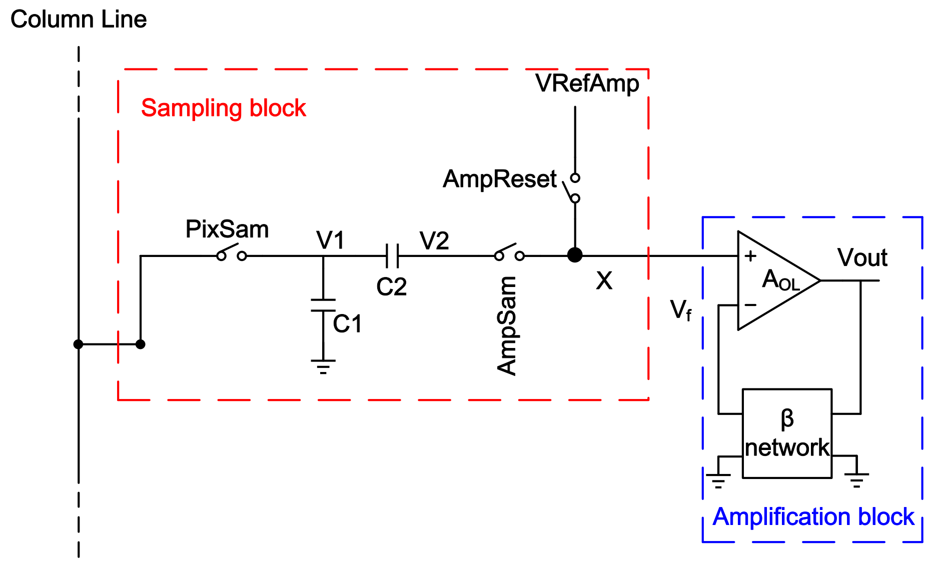
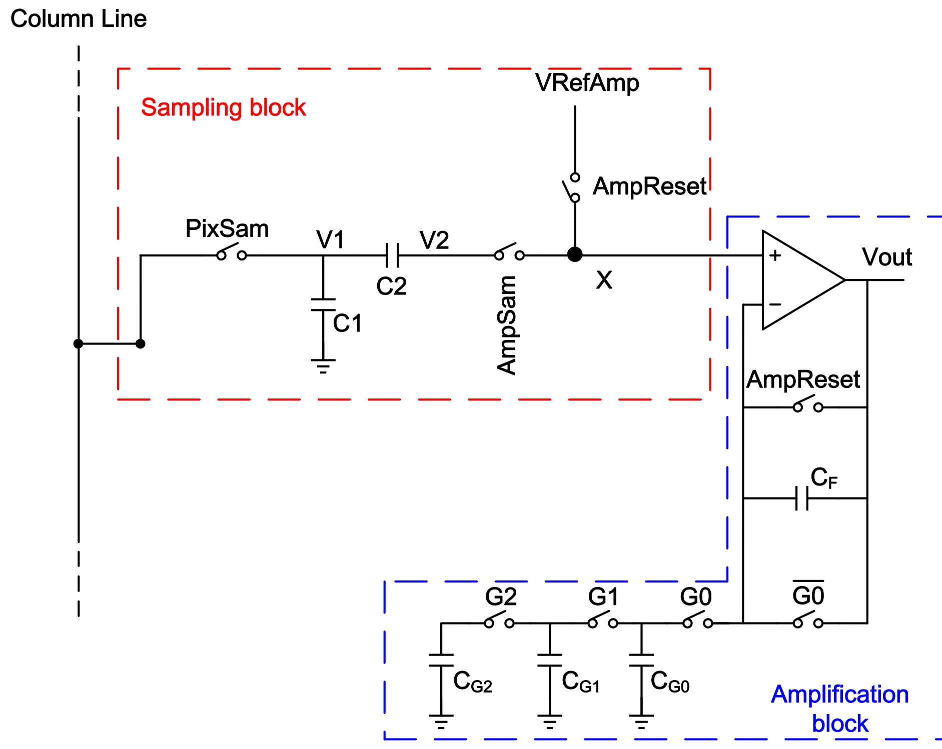


Figure 4.32: (a) General view of switched-capacitor amplifier; (b) SC implementation of PGA with ATI-CDS



(a)



(b)

Figure 4.33: Proposed SC-PGA block with analog CDS technique: (a) ideal closed-loop amplifier, (b) switched-capacitor implementation

Figure 4.34 depicts four gain settings controlled by four switches. When $G2G1G0 = 000$, the closed-loop gain becomes one, leading the voltage on the X node, V_X, buffered to the amplifier's output. When $G2G1G0 = 001$, the closed-loop gain becomes two and leads two times of the voltage on the X node, $2 \times V_X$, buffered to the amplifier's output. When $G2G1G0 = 011$, the closed-loop gain becomes four and leads four times of the voltage on the X node, $4 \times V_X$, buffered to the amplifier's output. When $G2G1G0 = 111$, the closed-loop gain becomes eight and leads eight times of the voltage on the X node, $8 \times V_X$, buffered to the amplifier's output. The gain configuration is summarized in the Table 4.3.

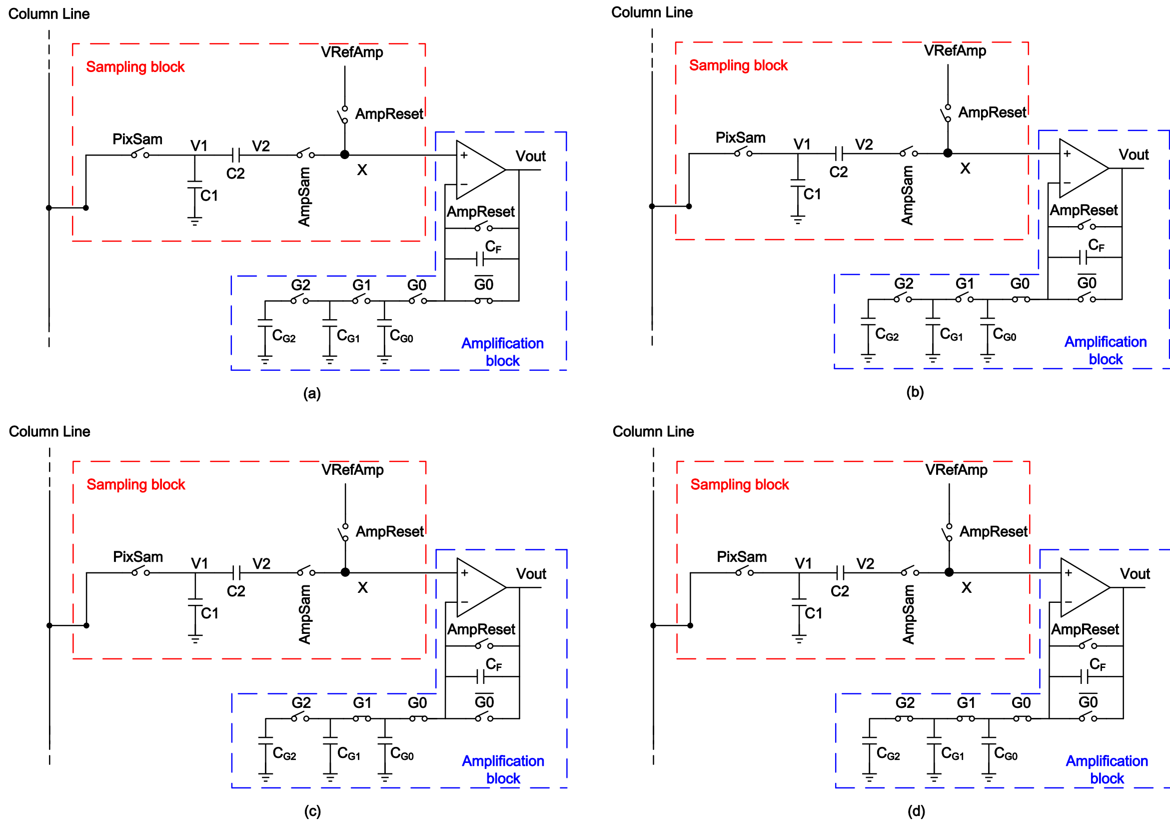


Figure 4.34: Proposed PGA operating at (a) Gain =1, (b) Gain =2, (c) Gain =4, (d) Gain =8

Table 4.3: Gain Settings for proposed SC-PGA

Settings	Gain	Amplifier's output
$G2G1G0 = 000$	1x	$V_{out} = V_X$
$G2G1G0 = 001$	2x	$V_{out} = 2 * V_X$
$G2G1G0 = 011$	4x	$V_{out} = 4 * V_X$
$G2G1G0 = 111$	8x	$V_{out} = 8 * V_X$

Several factors determine the operational amplifier in the proposed SC-PGA to have a wide input and output voltage range: (1) the opamp is used as a buffer to provide different voltage gains; (2) the maximum voltage difference of pixel and reset signal is 1 V; (3) the reference voltage V_{RefAmp} was set to 1.4 V; (4) the output voltage fed into the subsequent ADC needs to match the ADC's input range from 0.4 V to 1.4 V. Therefore, the input common-mode range (ICMR) and the output range of the operational amplifier were designed to be variable from 0.4 V to 1.4 V.

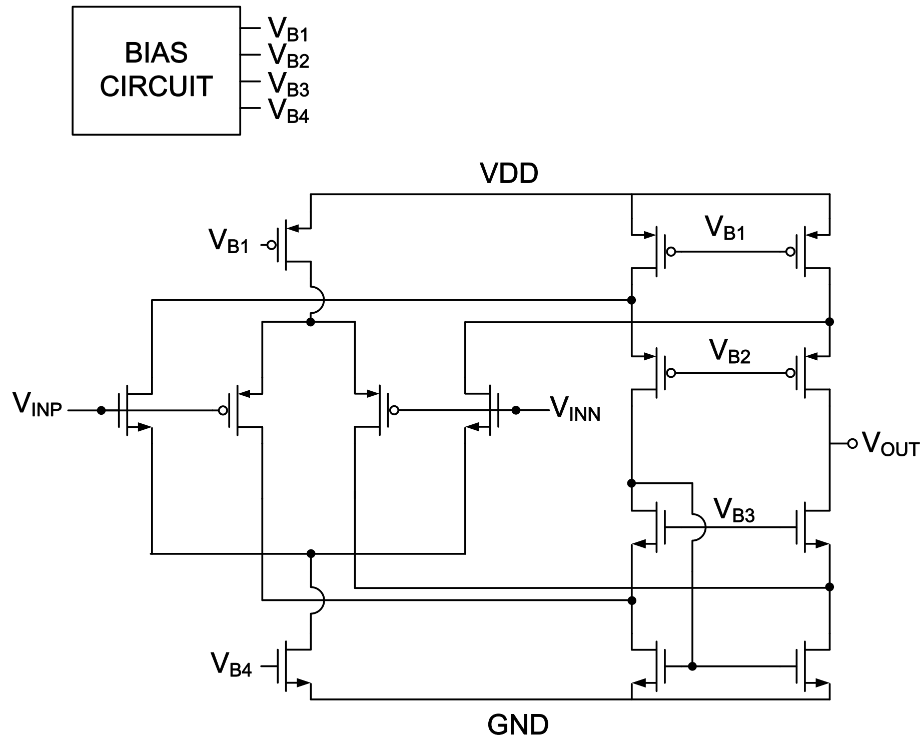


Figure 4.35: Block diagram of the operational amplifier used by the proposed SC-PGA

The operational amplifier input topology shown in Figure 4.35 has two differential input stages (NMOS- and PMOS- input pairs in parallel) in single power supply (1.8 V), taking advantages of both to achieve a wide input range. When input common-mode voltage (V_{CM}) is close to the negative rail, the PMOS-input pair is entirely on, and the NMOS-input pair is entirely off. Otherwise, when V_{CM} is close to the positive rail, the NMOS pair is in use, and the PMOS pair is off.

The performance of the single-supply operation amplifier with a 4 pF loading capacitor will be discussed next including noise, stability, input common-mode range, common-mode rejection ratio, power supply rejection ratio and slew rate requirement. Figure 4.36 shows the stability analysis with an unity-gain buffer configuration. The loop gain of the topology is equal to the opamp's open-loop gain. When the frequency is lower than $f_{3dB} = 4.06$ kHz, it has 71.76 $4dB$ voltage gain. The gain-bandwidth product is approximate 15.13 MHz. Because it is a single stage amplifier, the opamp is stable, and it has an 87.46-degree phase margin.

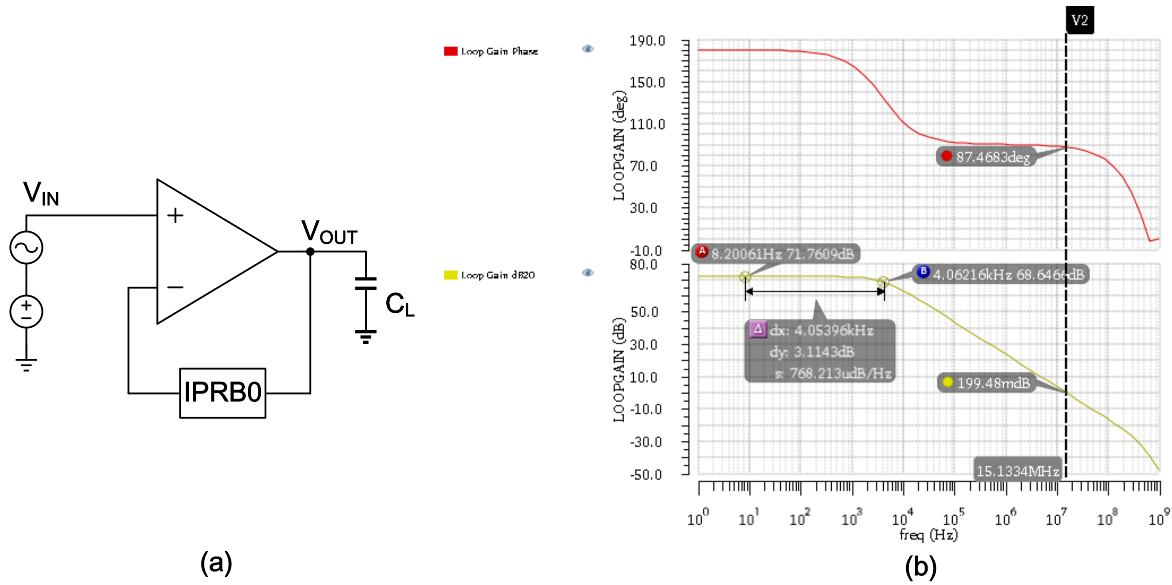


Figure 4.36: (a) Opamp stability testbench (b) simulation result

The input common-mode range was shown in Figure 4.37. To test ICMR, a unity feedback configuration is used, and positive input was swept from 0 V to 1.8 V. By observing the range in which gain is one, the input common-mode voltage can be varied from 326 mV to 1.589 V. Because the opamp was used as a buffer, the output swing is equal to the input swing. While the closed-loop gain was set to be higher than one, the input swing will be divided by the gain factor.

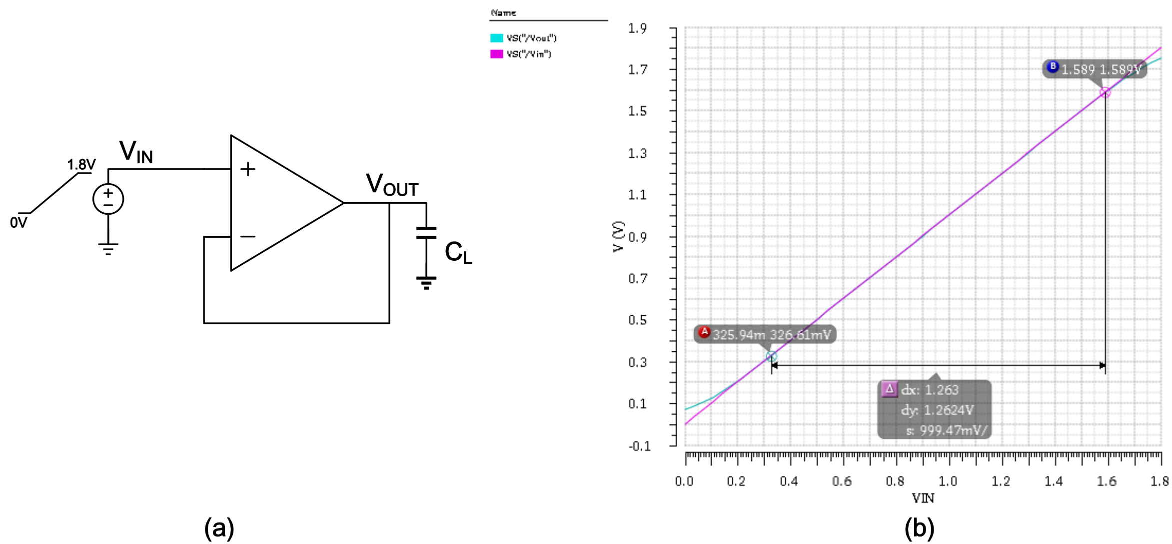


Figure 4.37: (a) Opamp ICMR testbench (b) simulation result

The common-mode rejection ratio (CMRR) of the opamp was also obtained through the circuit configuration, as shown in Figure 4.38. Two circuits were used to get open-loop gain and common-mode gain, respectively. The simulated CMRR is about 71.1 dB.

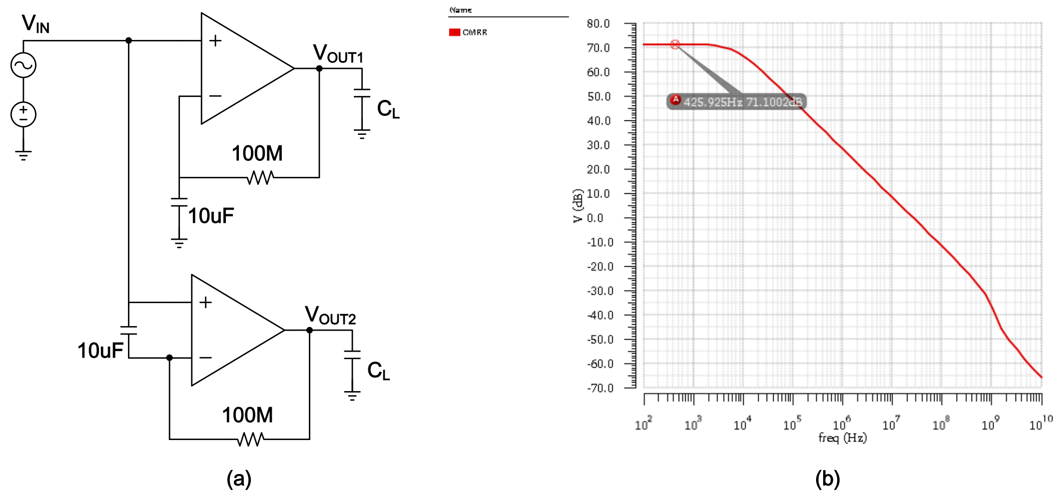


Figure 4.38: (a) Opamp CMRR testbench (b) simulation result

The power supply rejection ratio (PSRR) describes how well the amplifier can tolerate the noise coming from power supply and ground. Higher PSRR means better noise rejection. Both positive and negative PSRR in the proposed opamp are higher than 58.5 dB.

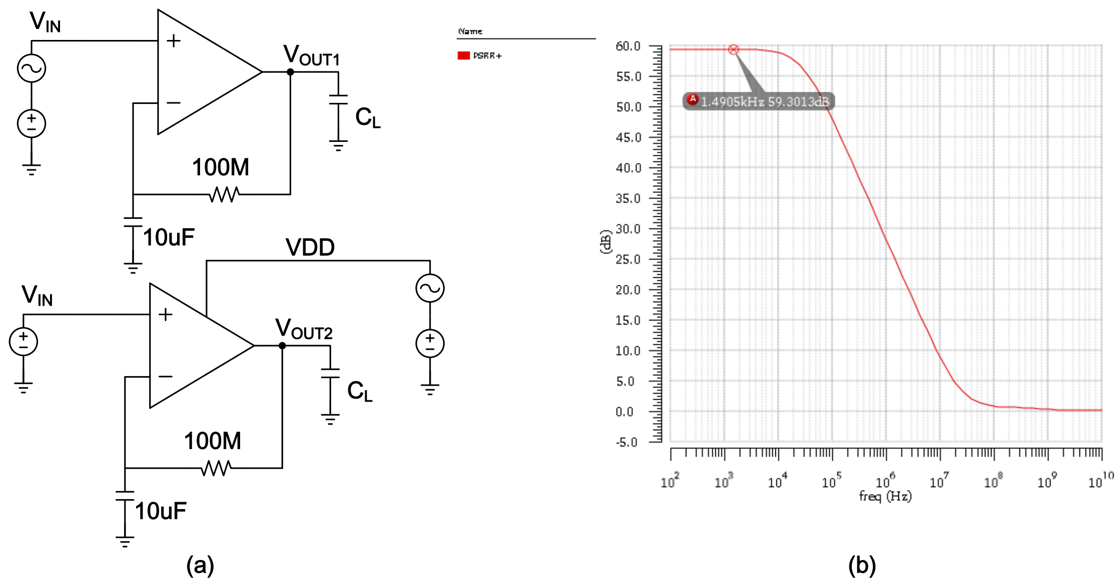


Figure 4.39: (a) Opamp positive PSRR testbench (b) simulation result

Figure 4.41 shows the opamp's step response with changing bias current ($20\mu\ A, 40\mu\ A, 60\mu\ A$). High bias current makes the opamp rise and fall more quickly, but it uses more power. The input pulse in the testbench was toggled from 0.4 V to 1.4 V with a 600 ns period.

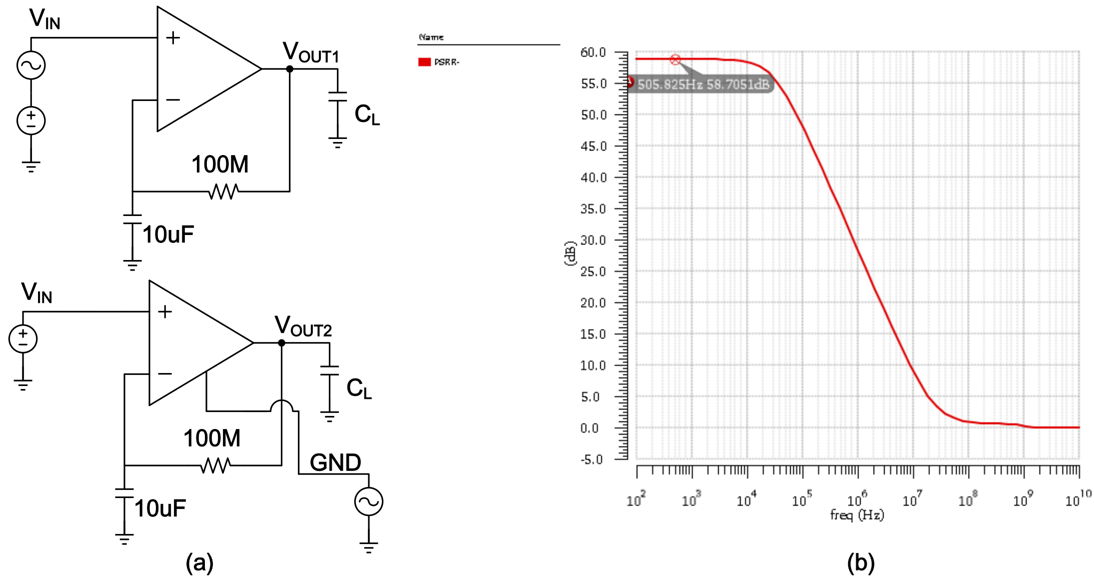


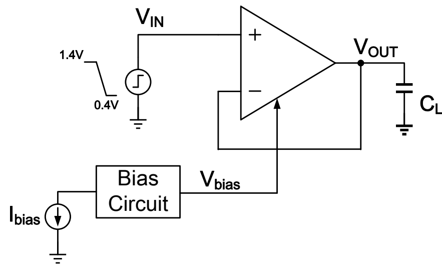
Figure 4.40: (a) Opamp negative PSRR testbench (b) simulation result

For a sinusoidal signal, the slew rate (SR) capability must satisfy the condition:

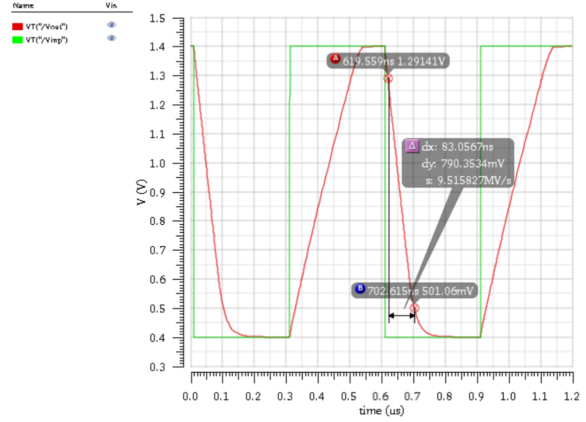
$$SR \geq 2\pi \cdot f \cdot V_{peak} \tag{4.10}$$

Consider the system timing requirement, only $200ns$ is left for the amplification time by using the opamp. Hence, the maximum SR required to buffer 1 V pulse is approximate 7.82 $V/\mu s$. For all three biasing currents, the SR satisfies the requirement.

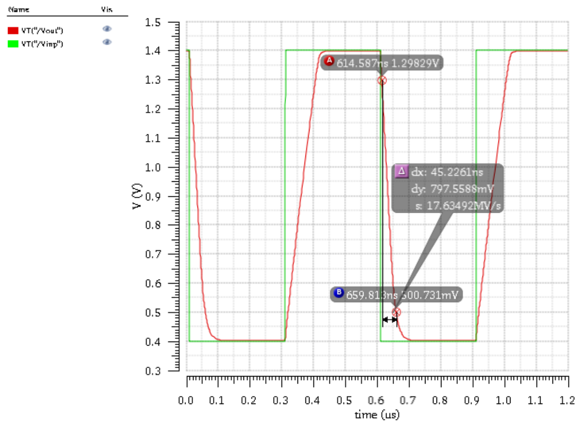
The noise performance of the opamp is shown in Figure 4.42. The RMS value of the total input referred noise is 37.57 uV.



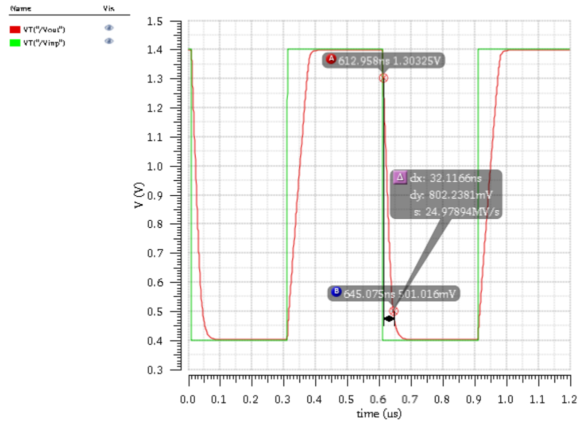
(a)



(b)

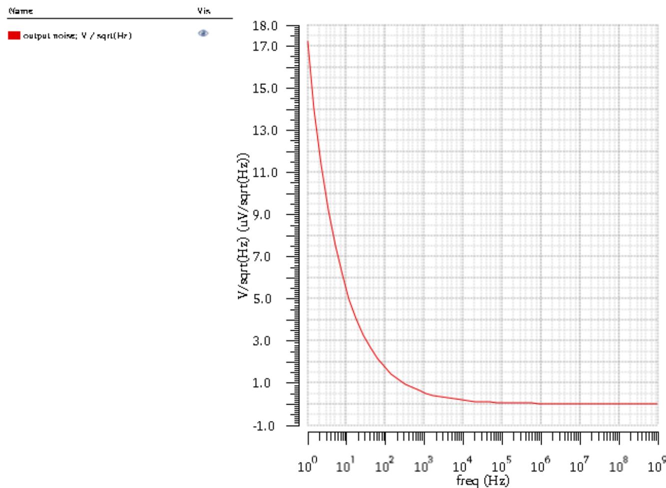


(c)



(d)

Figure 4.41: (a) Opamp slew rate testbench and (b)(c)(d) simulation results with different bias current



(a)

Results Display Window

Window Expressions Info Help cādence

Device	Param	Noise Contribution	% Of Total
I8.M23.m1	fn	1.96516e-05	27.36
I8.M22.m1	fn	1.96372e-05	27.32
I8.M36.m1	fn	1.65871e-05	19.49
I8.M35.m1	fn	1.6584e-05	19.49
I8.M18.m1	fn	5.41745e-06	2.08

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 3.75677e-05
Total Input Referred Noise = 3.75763e-05
The above noise summary info is for noise data

841 HelpAction

(b)

Figure 4.42: (a) Opamp noise plot and (b) noise report summary

4.4.3 Quadruple Column-Parallel Readout Architecture

To increase the speed of the readout flow, the dissertation proposes a quadruple column-parallel readout architecture, as shown in Figure 4.43. It leads four column lines reading out four rows of pixel data in parallel. Two readout blocks are on the top side of the image sensing area and two more on the bottom. This increases the readout speed to four times the rate of using one readout line per column.

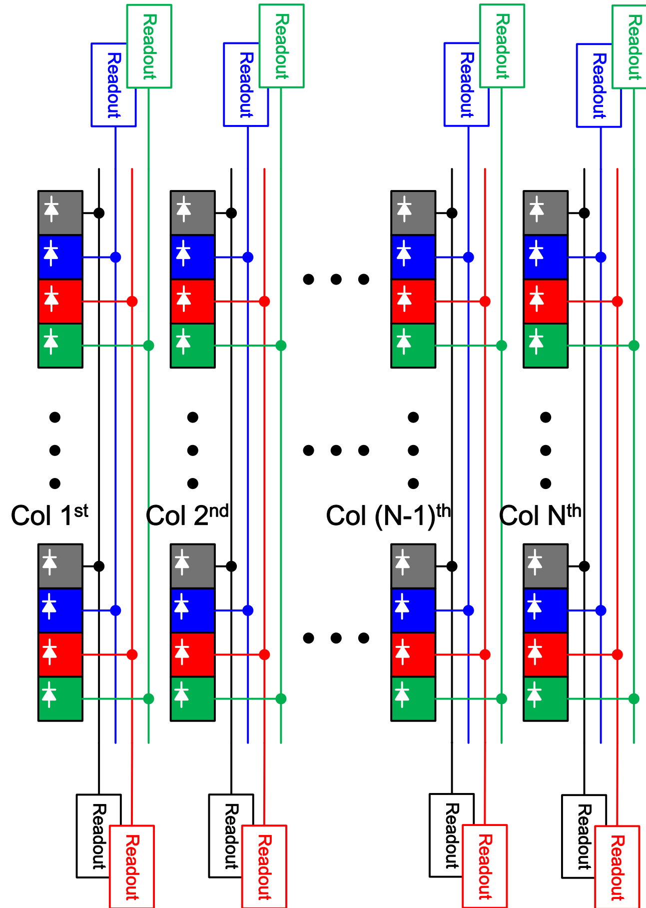


Figure 4.43: Quadruple column-parallel readout architecture

The number of rows with the pixel pitch in the pixel array determines the length of column lines. For a big pixel array, more rows demand a longer column line, resulting in a longer readout line. Meanwhile, more rows require an increasing number of select and sample switches to connect to each column line, enlarging parasitic capacitance. The parasitic consideration in column line is similar to a bit line of random access memory (RAM)[157]. Instead of having a memory cell intersecting row and column lines, each node has an active pixel cell. Therefore, high resolution leads to more parasitic capacitance and resistance in a column line.

The parasitic capacitance of each column line has two components. One is the parasitic of the capacitance of the column line to the substrate. It can be calculated using

$$C_{Col2Sub} = Area \times C_{\square} \tag{4.11}$$

where $Area$ is equal to $length \times width$ and $C_{\square}$ is the parasitic capacitance per um^2.

The second component is the junction capacitance on the column line from each switch source or drain implant that can be obtained by

$$\begin{aligned} C_{SW} = &(number\ of\ rows) \times (number\ of\ switches\ in\ a\ row) \\ &\times (capacitance\ of\ single\ MOS\ switch's\ source/drain) \end{aligned} \tag{4.12}$$

where parasitic capacitance brought by each MOS switch is assumed to be equal to half of gate oxide capacitance, C_{OX}.

The parasitic resistance of the column line to the substrate can be calculated using

$$R_{Col} = \frac{Length}{Width} \times R_{\square} \tag{4.13}$$

where $R_{\square}$ is the sheet resistance of the column line in $\Omega/square$.

A simple RC circuit can be used to estimate the time delay through column line to sampling capacitors, which in the worst case is

$$t_{d,worst} = 0.7 \cdot R_{Col} \cdot C_{Col} = 0.7 \cdot R_{Col} \cdot (C_{Col2Sub} + C_{SW}) \tag{4.14}$$

And the rising time of the output signal is

$$t_{r,worst} = 2.2 \cdot R_{Col} \cdot C_{Col} = 2.2 \cdot R_{Col} \cdot (C_{Col2Sub} + C_{SW}) \tag{4.15}$$

The previous discussions indicate that three aspects must be considered in parasitic calculations to improve the rising and delay time in each readout line: column line length, width, and switch size. Under the same area condition, shorter length and larger width of a column line could have less parasitic resistance. However, the length is determined by the number of rows in the pixel array. For a fixed pixel array, the length of each column line is fixed as well. A larger width could limit the active pixel area because it needs to cross from top to bottom of the whole pixel array. Besides, the larger width brings more parasitic capacitance to the column line. Furthermore, the junction capacitance is usually much larger. Therefore, it is more efficient to find a solution to reduce the parasitic capacitance introduced by the transistor switches connected to column lines.

By introducing four readout lines in each column, the proposed readout architecture is able to divide junction capacitance in each column by four.

Several calculations help estimate the settling time for each column. At first, which metal for routing the column line must obtain the sheet resistance. The dissertation used a 0.18 μm CMOS imaging sensor

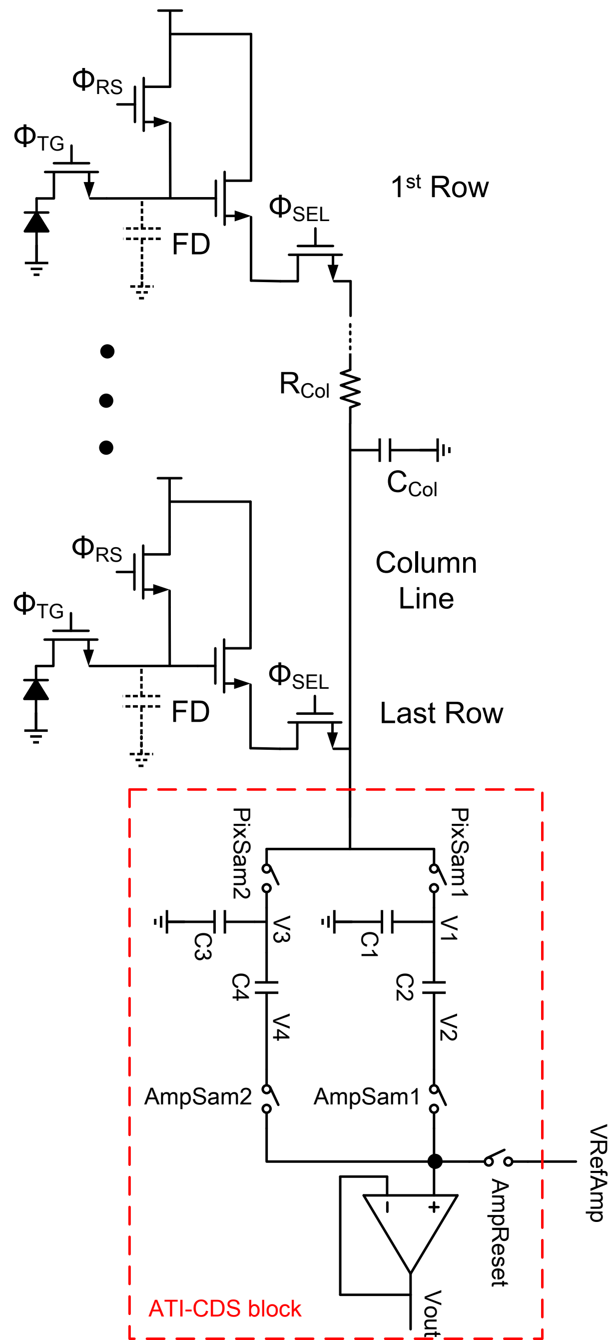


Figure 4.44: One column line with time delay consideration

(CIS) process, which has 1 poly layer and 6 metal layers. Table 4.4 and 4.5 list the sheet resistance and parasitic capacitance. Metal 2-5 layers have the same design rule and sheet resistance, roughly equal coupling capacitance. Either one metal layer or a stack of metal layers can be used to route the column line. Stacked layers could give less parasitic resistance. However, this is determined by the physical layout design. This dissertation used even-numbered metal layers for horizontal routing and odd-numbered metal layers for

vertical routing. The poly and the first metal layer are usually used for connections inside transistors. Hence, metal layer 3 and 5 could be used for column lines connected to row select and sampling switches.

For simplification, assume metal layer 3 is used for column lines. The width is set to be two times of minimum width, 0.56 μm, keeping both sheet resistance and parasitic capacitance small. Assume both above and under the column line have no other parallel metal layers so that the coupling and perimeter capacitance can be neglected. Table 4.6 can be used to calculate the periodic capacitance on the column line from each MOSFET's source or drain implant. Thick-oxide MOSFETs are considered in the design because it could provide larger swing and smaller gate oxide capacitance. However, thick-oxide MOSFETs need bigger layout area.

Take a megapixel array with 1,000 rows as an example. Each pixel has an area of 20 $\mu m \times 20 \mu m$, and each column has one readout line. The parasitic resistance of one readout line routed by Metal 3 from top to bottom can be calculated by

$$R_{Col} = \frac{Length}{Width} \times R_{\square} = \frac{1000 \cdot 20\ \mu m}{0.56\ \mu m} \times 74\ m\Omega/\square \approx 2.643\ k\Omega \tag{4.16}$$

With $W = 1\ \mu m, L = 350\ nm$ of thick-oxide NMOS as row select and sampling switch, the parasitic capacitance of the column line can be calculated by

$$\begin{aligned} C_{Col} &= C_{Col2Sub} + C_{SW} \approx C_{SW} = 1000 \cdot C_{OX}^{'} \cdot W \times L \\ &= 1000 \cdot 5.31\ fF/\mu m^2 \cdot 1\ \mu m \cdot 0.35\ \mu m = 1.8585\ pF \end{aligned} \tag{4.17}$$

The estimated delay time and rising time in the worst case of a column line is calculated by

$$t_d = 0.7 \cdot R_{Col} \cdot C_{Col} = 0.7 \times 2.643\ k * 1.8585\ pF = 3.438\ ns \tag{4.18}$$

$$t_r = 2.2 \cdot R_{Col} \cdot C_{Col} = 2.2/0.7 \times t_d = 10.8\ ns \tag{4.19}$$

Table 4.4: Different metal layer sheet resistance and width design rule

Name	Sheet Resistance ($m\Omega/\square$)	Minimum width (μm)	Minimum space (μm)
Metal1	$77(95@W = 0.23um)$	0.23	0.23
Metal2	$74(85@W = 0.28um)$	0.28	0.28
Metal3	$74(85@W = 0.28um)$	0.28	0.28
Metal4	$74(85@W = 0.28um)$	0.28	0.28
Metal5	$74(85@W = 0.28um)$	0.28	0.28

Table 4.5: **Different metal layer coupling, area and perimeter capacitance**

Name	Coupling capacitance ($aF/\mu m$)	Area capacitance ($aF/\mu m^2$)	Perimeter capacitance ($aF/\mu m$)
Metal1	113	M1-Poly: 45.7 M1-Active: 35.2	M1-Poly: 9.5 M1-Active: 8.6
Metal2	101	M2-M1: 39.2	M2-M1: 9.6
Metal3	102	M3-M2: 39.2	M3-M2: 9.6
Metal4	102	M4-M3: 39.2	M4-M3: 9.6
Metal5	103	M5-M4: 39.2	M5-M3: 9.6

Table 4.6: **Oxide thickness and oxide capacitance for thin- and thick-oxide CMOSs in the used CIS process**

Name	Value
T_{OX}(1.8V NMOS)	4.1 nm
T_{OX}(1.8V PMOS)	3.9 nm
C'_{OX}(1.8V NMOS)	8.4 $fF/\mu m^2$
C'_{OX}(1.8V PMOS)	8.85 $fF/\mu m^2$
T_{OX}(3.3V NMOS)	6.5 nm
T_{OX}(3.3V PMOS)	6.3 nm
C'_{OX}(3.3V NMOS)	5.31 $fF/\mu m^2$
C'_{OX}(3.3V PMOS)	5.47 $fF/\mu m^2$

In sum, the architecture with one readout line per column needs $t_d + t_r = 14.238\ ns$ for settling each signal pulse. Using the proposed architecture, the settling time could be reduced to $\frac{1}{4} \times (t_d + t_r) = 3.582\ ns$. Therefore, each column line with ATI-CDS needs only two-thirds of settling time requirement compared to single CDS. The quadruple parallel architecture speeds up the total readout time by 4. Combining the two techniques could increase the readout speed by 600%.

A voltage drop is another essential concern caused by a parasitic resistance in a column line. A stack-metal solution is used to reduce the voltage drop in the layout design of the pixel array. To keep the $20\mu m$ pixel pitch unchanged, the column lines need to be above photodiodes. Wide metal layers reduce the active area of photodiodes, so that a minimum width is set to all metals used for column lines in this CMOS image sensor. However, the column resistance could be a problem. For example, if only metal 3 is used with $0.28\mu m$, the total resistance in a column with 1024 rows is

$$R_{Col} = \frac{L}{W} \times R_{\square} = \frac{1024 \times 20\mu m}{0.28\mu m} * 85m\Omega \approx 6.217\ k\Omega \tag{4.20}$$

So, for a given column bias current, 20uA, the voltage drop in the column line is $124.34mV$.

The proposed stack-metal layout approach is depicted in Figure 4.45. The column line uses 256 stack-metal blocks, and each block has $40\mu m$-long Metal 3, $35\mu m$-long Metal 2, $12\mu m$-long Metal 4 and Metal 5. They are connected in each block and have the same width, $0.28\mu m$. A simple schematic model is shown in Figure 4.46.

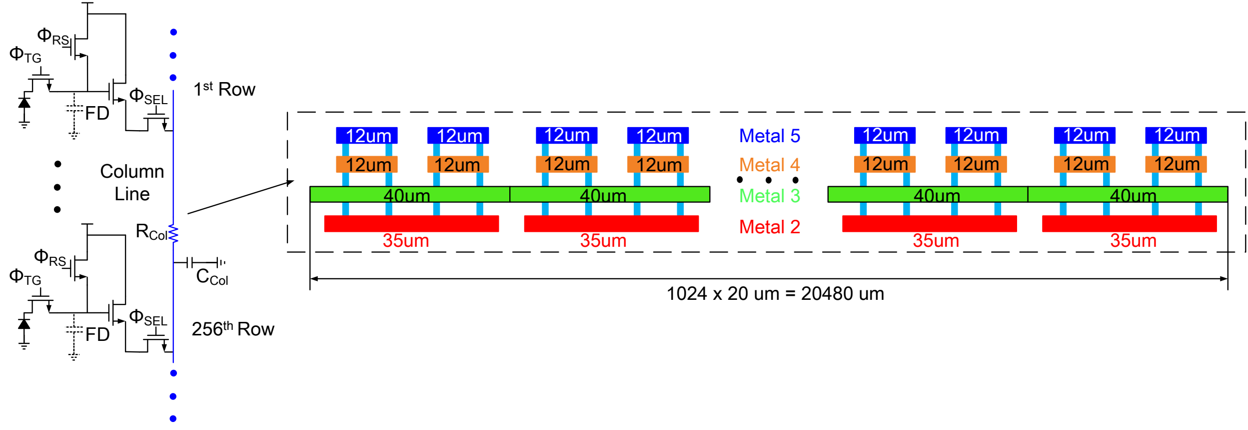


Figure 4.45: A stack-metal method applied to each column line with 256 rows

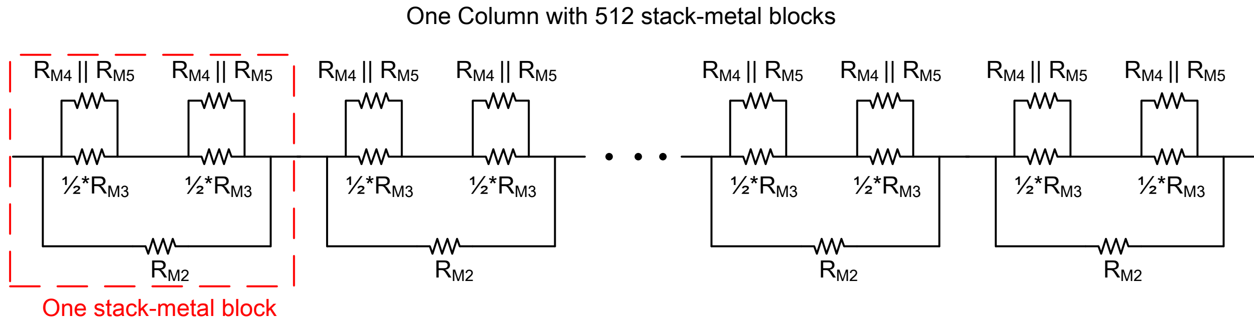


Figure 4.46: Equivalent resistor model in one column using proposed stack-metal method

The equivalent resistance of one stack-metal block is

$$\begin{aligned} R_{OneMetalBlock} &= R_{M2} \; || \; \{2 \times [(\tfrac{1}{2}R_{M3}) \; || \; (R_{M4} \; || \; R_{M5})]\} \\ &= (\tfrac{35\mu m}{0.28\mu m} \times 85m\Omega) \; || \; \{2 \times [(\tfrac{1}{2} \times \tfrac{40\mu m}{0.28\mu m} \times 85m\Omega) \; || \; (\tfrac{1}{2} \times \tfrac{12\mu m}{0.28\mu m} \times 85m\Omega)]\} \\ &= 10.625\Omega \; || \; [2 \times (6.071\Omega \; || \; 1.821\Omega)] \\ &\approx 2.216\Omega \end{aligned} \tag{4.21}$$

The total resistance in one column line is

$$R_{Col} = R_{OneMetalBlock} \times 512 = 1.134k\Omega \tag{4.22}$$

Hence, for a given column bias current, 20uA, the voltage drop is reduced to 22.68mV, less than one-fifth of the column line routed by only metal 3.

4.4.4 Analog-to-Digital Converter

The A/D converter in CMOS image sensors plays a vital role in digitizing the captured image. Its resolution affects the image quality; its sampling rate affects the frame rate; its power consumption and area affect the imager's power and layout, respectively. Most CMOS image sensors have ADC resolutions of 10 to 12 bits. In addition, the proposed CMOS imager has four ADCs per column, and the total number of ADCs could be over 4,000 for a megapixel resolution. The total power consumption of these ADCs is a significant concern, as it can have a large effect on the battery life, and also influence the die temperature. This could degrade image quality due to the higher leakage and noise. Hence, the successive-approximation register (SAR) ADC was selected to provide medium-to-high resolution and consume as little power as several tens of $fJ/conv - level$.

Two pseudo-differential unipolar SAR ADCs have been designed with the same topology in this dissertation but have different resolution: one has 10-bit, and the other has 12-bit. The differential analog input voltage ($VIN^+ - VIN^-$) is over a span of 0.4 V to 1.4 V. In this range, a single-ended unipolar input signal, driven on the IN^+ pin (or IN^- pin), is measured concerning high reference level, driven on the IN^- pin (or IN^+ pin). Either input pin is allowed to swing from 0.4 V to 1.4 V. When one input pin swings, however, the other one is restricted to the high reference voltage 1.4 V. Pseudo-differential inputs, as shown in Figure 4.47, are ideal for applications that require DC common-mode voltage rejection, for single-ended input signals and for applications that do not want the complexity of differential drivers. Pseudo-differential inputs simplify the ADC driver requirement, reduce complexity, and lower power dissipation in the signal chain.

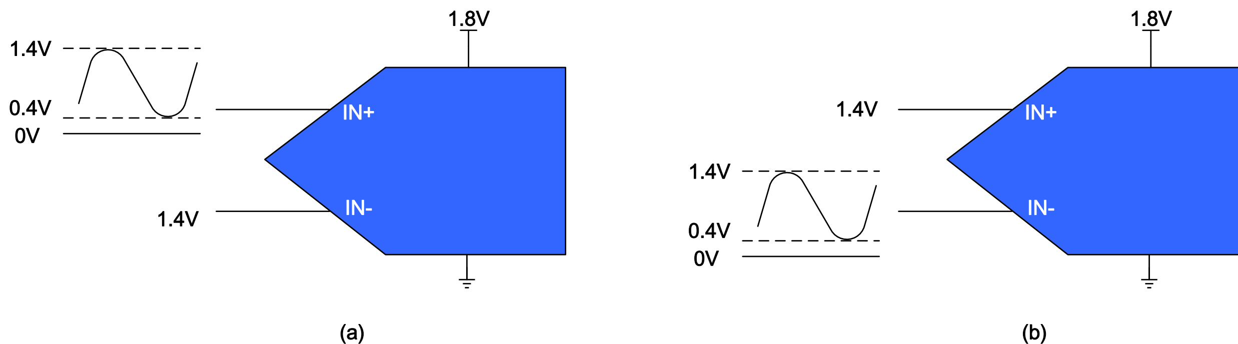


Figure 4.47: Pseudo-differential unipolar ADC

Since each column has two identical ADCs on both top- and bottom-side of the pixel array and each pixel has 20 μm, the layout pitch of ADCs must be less than 10 μm. The chip fabrication constraint limits the maximum length of the ADC layout. Figure 4.48 depicts the layout of proposed 10-bit ADC, which includes bootstrapped switch circuits, capacitive DAC, dynamic comparator, and two 10-bit memory banks. Figure 4.49 shows the proposed 12-bit ADC having the same topology.

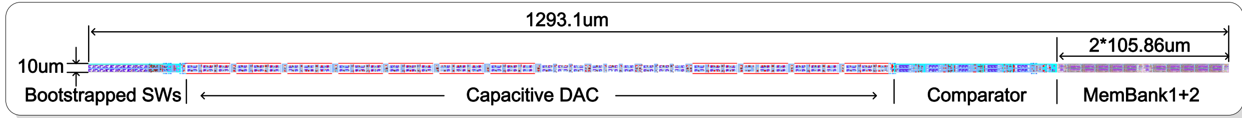


Figure 4.48: Layout view of proposed 10-bit pseudo-differential unipolar ADC

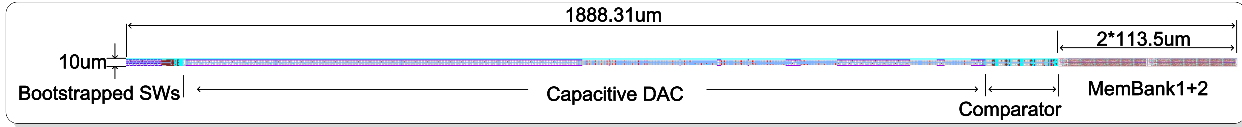


Figure 4.49: Layout view of proposed 12-bit pseudo-differential unipolar ADC

The proposed SAR ADC architecture is shown in Figure 4.50. It consists of a capacitive DAC array with bootstrapped switches and three off-chip references to complete sampling operation, a dynamic comparator, SAR logic block and two memory banks using shift registers. Each conversion cycle has two phases: a sampling phase and a conversion phase. During the sampling phase, the capacitive DAC is worked as a sample-and-hold circuit by using the bootstrapped switches and the entire capacitor array in which all bottom plates are connected to ground. During the conversion phase, all column-level ADCs are operating in parallel and controlled by the same SAR logic in the sequencer. One of memory banks are used to store the digital bits and the other memory bank is connected to the serializer in each line time.

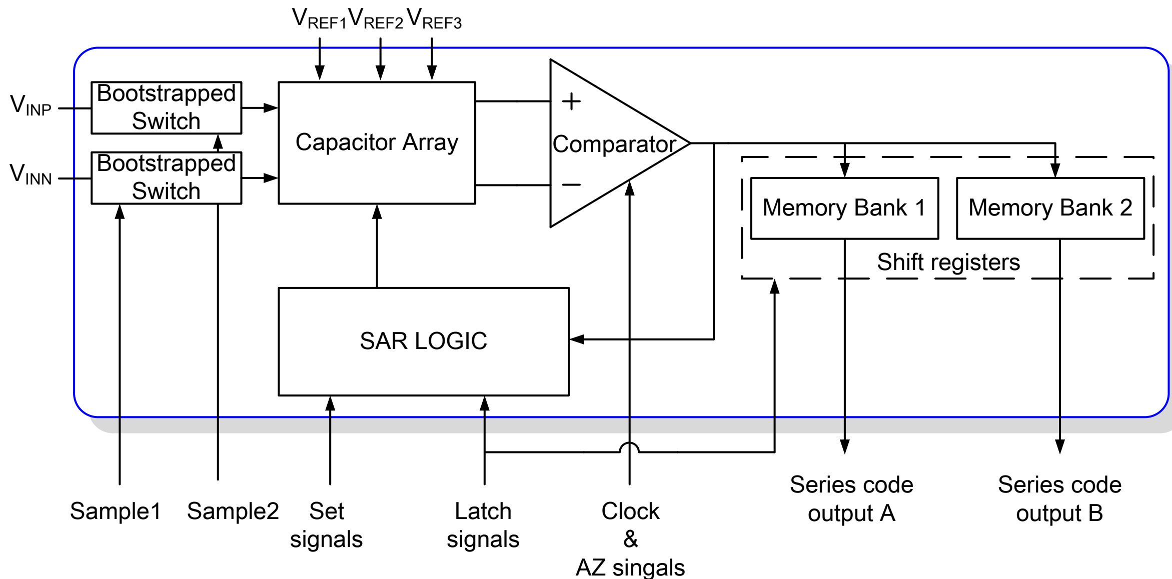


Figure 4.50: Block diagram of proposed SAR ADC

4.4.4.1 Capacitive DAC

The minimum total capacitance of each side array is limited by the kT/C noise associated with the array charging and discharging. Since the quantization noise power is $\frac{LSB^2}{12}$ and the RMS thermal noise value is required to be small than half of LSB, the total capacitance requires

$$C_{total} > \frac{12 \times kT}{(LSB/2)^2} \tag{4.23}$$

where k is Boltzmann's constant, 1.38×10^{-23} J/K; T is the temperature; LSB is the ADC's least significant bit, $LSB = \frac{V_{REF}}{2^N}$. In this project, the proposed SAR ADC has 1 V reference voltage. Hence, the total capacitance at room temperature (300 K) needs to be larger than 833 fF for 10 bits resolution or 3.33 pF for 12 bits resolution.

Mismatch in the capacitor array is the next consideration. Each capacitor in a switched-capacitor DAC can be expressed as below considering capacitor mismatch and parasitic.

$$C_i = 2^{i-1}C_u + C_{par,i} + \Sigma_1^{2^{i-1}}\delta_j \quad (i = 1, ..., N) \tag{4.24}$$

where $C_{par,i}$ is the parasitic capacitance related to the i-th capacitor and δ_j the mismatch equivalent capacitance affecting the unit capacitor. The capacitor mismatch can be modeled as a Gaussian distribution with a mean value equal to the unit capacitor, so the standard deviation is

$$\sigma_C = \frac{C_u k_c}{\sqrt{2A_{cap}}} \tag{4.25}$$

where C_u, k_c and A_{cap} is the unit capacitance, the Pelgrom mismatch coefficient, and the area of the unit capacitor, respectively. Hence, a larger size capacitor could have less mismatch. The parasitic capacitances depend on layout inaccuracies, capacitor geometry, and wiring.

However, for the 10 μm layout pitch, each ADC could have less than 5 μm width for each capacitor since each switch-capacitive DAC array (SC-DAC) has two identical capacitor array. Also, the length of a unit capacitor is one of the significant factors to determine the DAC layout length. As one of the significant components in a SAR ADC, the unit capacitor accounts mostly for the ADC layout. Consequently, to satisfy the layout pitch, a capacitor with 22.096 fF and 3×3 um^2 in 0.18 μm CIS process was chosen as a unit capacitor.

The size of the unit capacitor is not the only factor affecting the final layout size of the capacitive DAC. The total number of capacitors becomes the other factor. Many studies have been made in past 10 years have tried different capacitor topologies and different switching approaches reducing the layout size of the capacitive DAC array. For a n-bit traditional switched-capacitor DAC [158] with binary-weighted capacitor array and conventional switching procedure, the number of unit capacitors in a capacitor array is 2^n. The monotonic switching method [159] and merged-capacitor switching method [160] reduce the number needed by half by using top-plate sampling to complete the first comparison without any capacitor

switching. Tri-level switching scheme [161] or monotonic multi-switching scheme [162] further reduce the number of capacitors in the array by 75%.

The principal scheme to reduce the layout size of the capacitive DAC is to build a split-capacitor topology with one or several attenuation capacitors. An attenuation capacitor, in series with the LSB-capacitor array, is required to equal to one-unit capacitor. For example, a N-bit single-ended charge-redistribution SAR ADC has one attenuation capacitor splitting the MSB-capacitor and LSB-capacitor array. Assume the attenuation capacitor is in the middle, so in the LSB-capacitor array and the MSB-capacitor array is 2^M and $2^M - 1$, respectively. So the attention capacitance is expressed as

$$C_{attenuation} = \frac{C_{total,LSB}}{C_{total,LSB} - 1} \tag{4.26}$$

Hence, the total number of unit capacitors in the entire array is

$$\begin{aligned} C_{total} &= C_{attenuation} + C_{total,LSB} + C_{total,MSB} \\ &= 2^M + 2^M - 1 + \frac{2^M}{2^M - 1} = 2^{M+1} + \frac{1}{2^M - 1} \end{aligned} \tag{4.27}$$

So, a 10-bit single-ended SAR ADC needs 63 unit capacitors and an attenuation capacitor with $\frac{32}{31}$ unit capacitance, which is about 6.25% of total capacitances in a conventional one.

However, it is difficult to develop an attenuation capacitor with a fractional value and match perfectly to the entire capacitor array. This results in a capacitor mismatch issue. Although [163] proposed a method to achieve an integer attenuation capacitor, the split-capacitor topology is more sensitive to mismatch compared to traditional one without the attenuation capacitor. The parasitic capacitance connected to the top-plate node of the MSB-capacitor array and the LSB-capacitor array, in particular, parallel with the attenuation capacitor, could cause linearity degradation and gain error. Furthermore, in practice, the split-capacitor DAC architecture would need to increase the unit capacitance to meet the noise requirements. Therefore, the split-capacitor scheme is not very beneficial.

A robust topology was used with three reference voltages ($V_{ref}, V_{ref}/4, V_{ref}/16$) to divide the entire capacitor array into three segments, and their top plates are connected. This scheme avoids the linearity issue caused by the top-plate parasitic capacitance, and it also reduces the total capacitance, which still meets the noise requirement.

Because the SAR ADC has a pseudo-differential input structure, a single-ended switching scheme is applied in the proposed capacitive DAC. It not only saves switching power but also reduces the number of transistors and area in each SAR logic block. Top-plate sampling is used but needs switching operations to make comparisons. The single-ended switching procedure does not need the downward transition, so it speeds up the DAC settling process. All these control signals are shared with the entire one-side ADC array. Hence, ADCs will simultaneously start to sample, make conversions, and store digital bits.

An offset compensation scheme for dark pixels was added in the proposed SAR ADC. An extra $SetOffset$ control signal is used to achieve an offset shifting function. In the sampling mode, $SetOffset$ stays low to be inactive. Before starting the conversion process, $SetOffset$ goes high to shift the pixel signal sampled to the DAC by the amount of $V_{offset} \times \frac{C_{offset}}{C_{total}+C_{offset}}$.

When the offset capacitor, $C_{offset} = 34 \cdot C_u$, the total capacitance of the proposed DAC array is $295 \cdot C_u$. Sweep V_{offset} from 0 V to 1 V and obtain the maximum digital output can be 550 ($12'b$0010 0010 0110). The waveform of digital codes is shown in Figure 4.51.

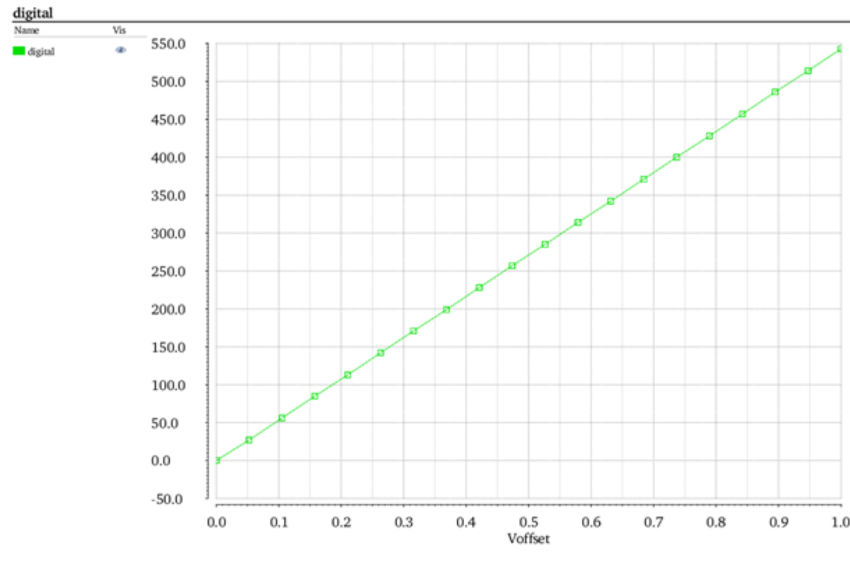


Figure 4.51: Waveform of digital codes by sweeping offset from 0V to 1V and having 295 unit capacitors

When the offset capacitor, $C_{offset} = 17 \cdot C_u$, the total capacitance of the proposed DAC array is $278 \cdot C_u$. Sweep V_{offset} from 0 V to 1.8 V and the maximum digital output can be 500 ($12'b$0001 1111 0100). The waveform of digital codes is shown in Figure 4.52.

Another concern is to consider the amount of time needed to settle the input structure of the proposed SAR ADC during the acquisition phase. If the acquisition time is not long enough, the signal value will be lower than expected, and the signal-to-noise ratio in the phase will be smaller. Furthermore, the conversion rate of a SAR ADC is also affected by the acquisition time. The conversion rate is equal to the reciprocal of the addition of acquisition time and conversion time.

In the sampling phase, the analog input signal charges the entire capacitor array (C_{total}) through the switch resistance (R_{SW}) to a level proportional to the analog input. The combination of the switch resistance, the source resistance (or the previous stage output resistance), and the sampling capacitor determine the rate of charge on the sampling capacitor. A rising time characteristic in a single pole response can be illustrated in the sampling process.

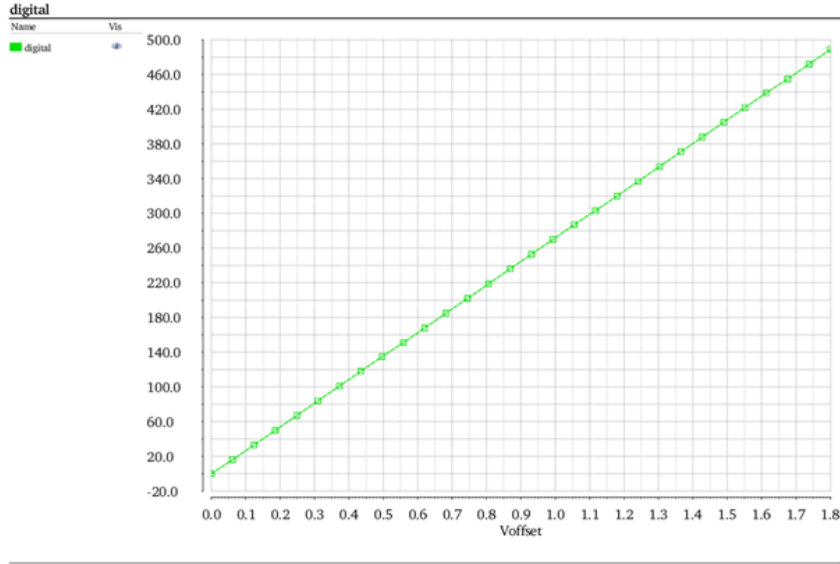


Figure 4.52: Waveform of digital codes by sweeping offset from 0V to 1.8V and having 278 **unit capacitors**

Table 4.7 shows a different time constant multiplier is needed to settle to within one-half LSB to a given resolution. For a 12-bit example, the time constant multiplier is required to be 9 or $k = 9$. The on-resistance of the sampling NMOS is, $R_{on} = \dfrac{L}{W} \times R_{\square} = 1.1\ k\Omega$. The total capacitance of one side is $C_{total} = 6.1\ pF$. So the time constant of the ADC is $\tau_{ADC} = R_{on} \cdot C_{total} = 6.71\ ns$. The minimum time constant to meet the half-LSB settling requirement is $k \times \tau_{ADC} = 60.39\ ns$.

Table 4.7: Required settling time for a ADC with different resolutions

number of bits	**0.5LSB**	**Time Constant (k) multiplier for 1/2 LSB settling accuracy**	**Time Constant (k) multiplier for 1/4 LSB settling accuracy**
8	0.1953125%	6.2	6.9
9	0.0976563%	6.9	7.6
10	0.0488281%	7.6	8.3
11	0.0244141%	8.3	9.0
12	0.0122070%	9.0	9.7
14	0.0030518%	10.4	11.1
16	0.0007629%	11.8	12.5

In one column time or line time, t_{LT}, the ADC completes one conversion. So the throughput rate is equal to $\frac{1}{t_{LT}}$. In other words, the addition of acquisition time and conversion time is equal to one column time, which is $\sim 390.625\ ns$ for the proposed CMOS image sensor operating at full speed, $10,000\ fps$. Since the acquisition time was decided, the conversion time for 12 cycles or 10 cycles depends on the speed of the comparator.

4.4.4.2 Comparator

This section focuses on the comparator design. To begin the comparator requirements will be discussed. As shown in Figure 4.50, DAC's outputs feed into the comparator. The comparator's output will be latched to memory banks. Hence, the input difference of the comparator swings from 0.4 V to 1.4 V, and the output swings from 0 V to 1.8 V.

For the 12-bit SAR ADC, ideally, the LSB input value can be detected by the comparator, which is equal to $\frac{1\ V}{2^{12}} = 244\ \mu V$. Therefore, to obtain the half-LSB precision, the minimum voltage gain of the comparator can be expressed

$$A_{V,min} = \frac{1.8V}{0.5 \cdot 244\mu V} = 14,754 \quad V/V \tag{4.28}$$

For the proposed SAR ADC, the acquisition process has to reset the total capacitors by the $V_{Ref,Amp}$ and sample the differential value in the DAC array so the minimum acquisition time is doubling the settling time constant, $2 \times 60.39\ ns$. The maximum conversion time for the CMOS imager operating in full speed is equal to $t_{LT} - t_{acq,min}$, which has 12 conversion steps for the 12-bit ADC or 10 conversion steps for the 10-bit ADC. Assume f_{3dB} is the comparator bandwidth. The settling time constant is equal to $\frac{1}{2\pi f_{3dB}}$. Allowing five times of τ for comparator output to settle in each comparison, therefore, the comparator bandwidth can be calculated by

$$f_{3dB} = \frac{N \times 5}{2\pi(t_{LT} - t_{acq,min})} \tag{4.29}$$

where N is the column ADC resolution, t_{LT} and $t_{acq,min}$ represent the line time and minimum acquisition time, respectively. Since the line time is 390.625 ns at the 10,000 fps frame rate and the acquisition time is $2 * 60.39\ ns$ for 12-b resolution, the comparator bandwidth is expressed as

$$\begin{aligned} f_{3dB} &= \frac{60}{390.625\ ns - 2 * 60.39\ ns} \approx 35.4\ MHz\ for\ 12\ bits \\ f_{3dB} &= \frac{50}{390.625\ ns - 2 * 60.39\ ns} \approx 29.5\ MHz\ for\ 10\ bits \end{aligned} \tag{4.30}$$

Assume the acquisition time of the 10-bit ADC is the same as the 12-bit ADC.

Due to the ADC layout limitation, the size transistors in one stage is constrained with a small transconductance. Furthermore, the power consumption is also limited, since 4096 comparators operate at the same time in a megapixel CMOS imager. Hence, it is challenging to use a single-stage comparator to reach the gain and bandwidth requirements for the 10-bit or 12-bit ADC.

The dissertation uses a cascade comparator topology including four pre-amplifier stages plus one high-sensitivity latch stage as shown in Figure 4.53. For an N-stage cascade comparator, its frequency response is expressed by

$$A_T(j\omega) = [A_v(j\omega)]^N = \frac{[A_v(0)]^N}{[1 + j\frac{\omega}{\omega_o}]^N} \tag{4.31}$$

where $A_v(0)$, $A_T(j\omega)$, ω_o represents the open-loop DC gain of one stage, the gain of the cascade comparator, and the 3dB frequency of one stage, respectively. Define ω_{oN} is the $3dB$ frequency of the N-stage cascade comparator, and ω_u is the unity gain bandwidth in one stage.

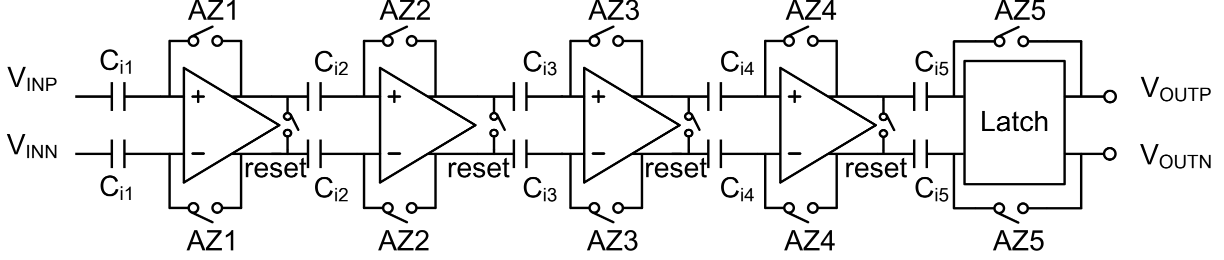


Figure 4.53: Block diagram of proposed 5-stage dynamic comparator with autozeroing

So, the gain magnitude of the N-stage cascade comparator at the ω_{oN} frequency is

$$|A_T(j\omega_{oN})| = \frac{[A_v(0)]^N}{\sqrt{2}} \tag{4.32}$$

And for a specified $|A_T(0)|$, the ω_{oN} frequency is

$$\omega_{oN} = \omega_o\sqrt{2^{1/N}-1} = \frac{\omega_u}{|A_v(0)|}\sqrt{2^{1/N}-1} = \frac{\omega_u}{|A_T(0)|^{1/N}}\sqrt{2^{1/N}-1} \tag{4.33}$$

Thus, the bandwidth amplification can be calculated by

$$\frac{\omega_{oN}}{\omega_{o1}} = |A_T(0)|^{(N-1)/N}\sqrt{2^{1/N}-1} \tag{4.34}$$

where ω_{o1} is defined as one stage bandwidth. Table 4.8 summarizes the bandwidth amplification and single-stage gain reduction features for cascade comparators.

Table 4.8: Bandwidth amplification and one-stage gain for cascade comparators in different stages

# of stages N	**BW amplification** ω_{oN}/ω_o	**gain for one stage** $\|A_v(0)\|$ **in (V/V)**	**gain for one stage** $\|A_v(0)\|$ **in (dB)**
1	1	14800	83.41
2	78.30	121.66	41.70
3	307.32	24.55	27.80
4	583.67	11.03	20.85
5	836.30	6.82	16.68
6	1045.25	4.95	13.90

A conversion sample using this 5-stage comparator is depicted in Figure 4.54. Because the maximum dimension of the chip limited by the CMOS PDK is 27 mm, using the 12-b ADC in each QCPRO must reduce the row number of the pixel array. Thus, the 10-b ADC is selected for the high-speed readout architecture and keeping the pixel array with 1024 rows. As shown in Figure 4.55, the ADC has 9.51 b ENOB at a 1.25 MHz sampling frequency.

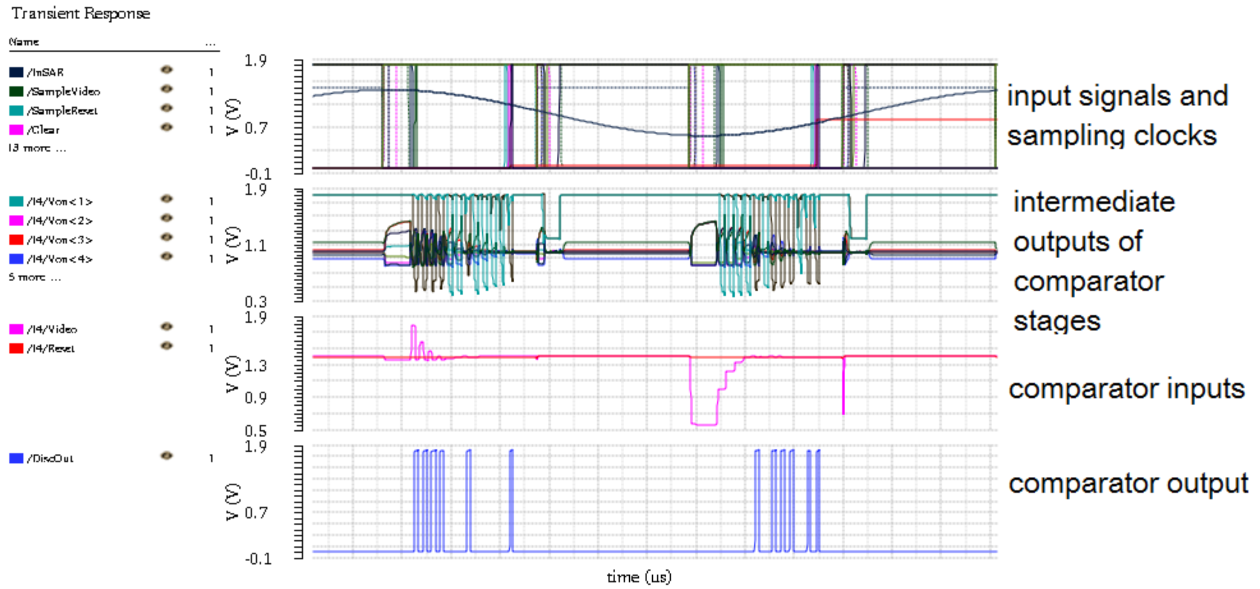


Figure 4.54: ADC transient simulation result for one sample conversion

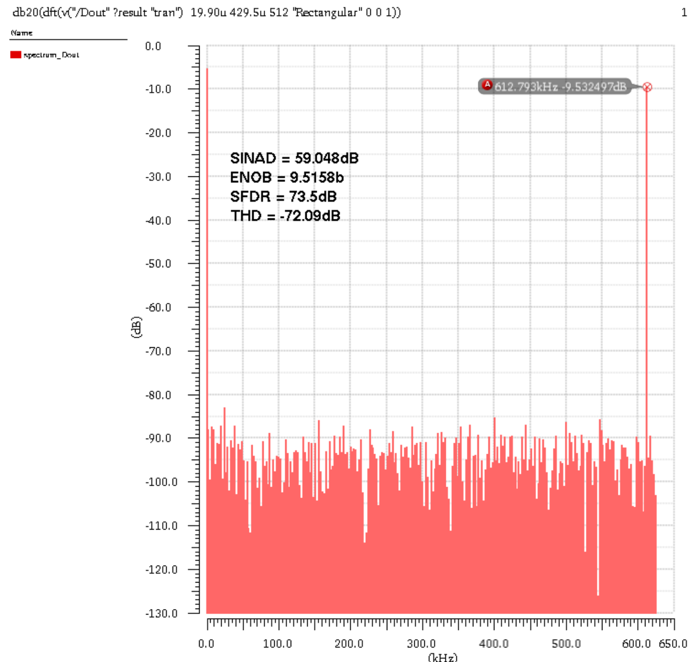


Figure 4.55: The 10b ADC FFT simulation to get SINAD/ENOB/SFDR/THD

4.5 PLL and SLVS drivers

On-chip phase-locked loops provide a stable clock signal for sequencer, memory banks, serializers, and other timing control circuits. The PLL block, used as a frequency multiplier, consists of five different sub-circuits: phase frequency detector, loop filter, voltage-controlled oscillator, feedback factor, and an output shaper. The PLL provides a 4× faster clock by multiplying the input reference clock from the on-board crystal oscillator. It was also designed with a digital reset and power down control signals. Step response of the PLL is shown in Figure 4.56. The primary performance is summarized in Table 4.9. The layout view of the PLL is depicted in Figure 4.57.

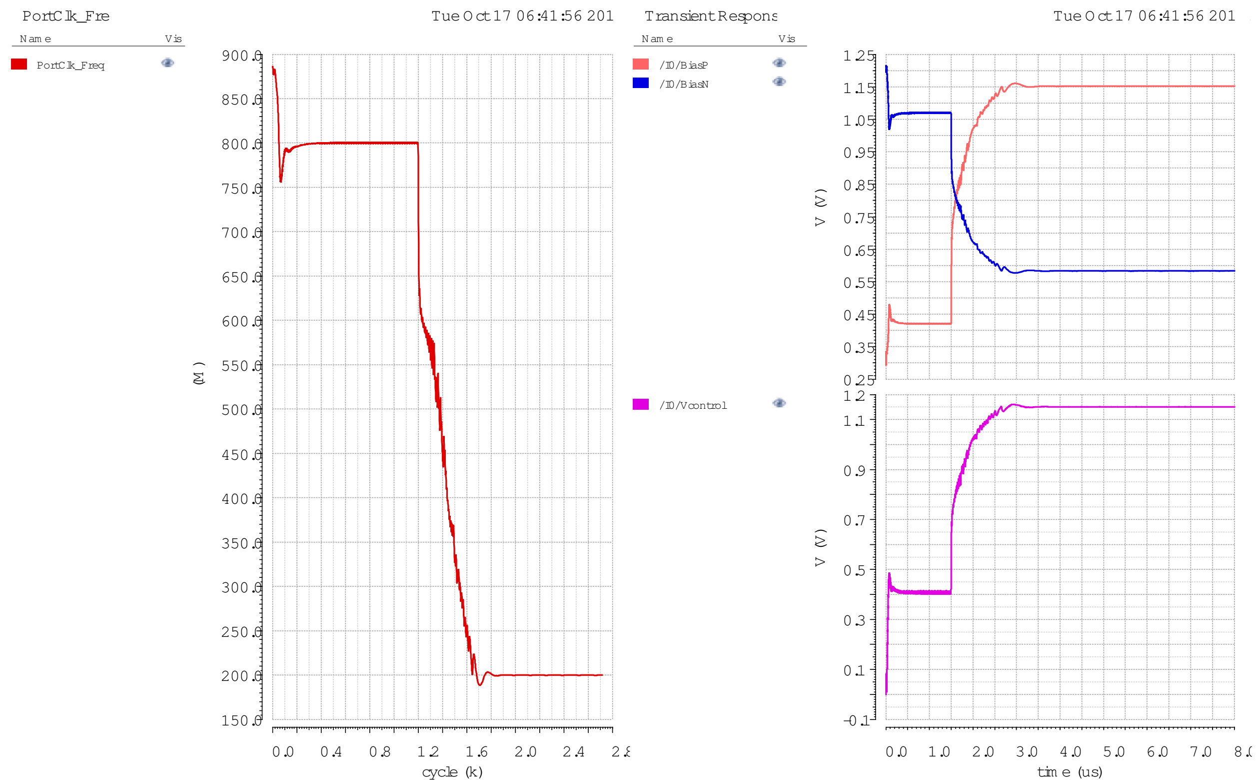


Figure 4.56: PLL step response from 800 MHz **to** 200 MHz

The SLVS block with a serilizer circuit converts the digital data from memory banks into standard serial SLVS data running at maximum 1 *Gbps*. The sensor with 128×1024 pixels and 768×1024 pixels has 18 and 98 SLVS differential pairs (2 pins for each SLVS channel), respectively. Two clock channels are added for data synchronization purpose. That means a total of 36 pins in the small sensor and 196 pins in the large sensor are used for the SLVS outputs.

Each SLVS channel is responsible for transferring 10-bit data words from sensor to receiver in the FPGA. The SLVS transmitters is allowed to connect to LVDS recievers for data transmission. In one line time, each SLVS channel transmits $2 * 10 * 16 = 320$ *bits*. In one frame time, each SLVS channel transmits $320 * 256 = 81.92$ *kbits* of digital data in total.

Table 4.9: **A performance summary of the PLL**

Input Freq. (MHz)	Output Freq. (MHz)	Lock time	Phase noise	RMS jitter (ps)	Peak-to-peak Jitter(ps)
50	200	2.3us	-144.16dBc/Hz @10MHz	0.339	2.09502
75	300	1.5us	-141.688dBc/Hz @10MHz	0.304	1.87872
100	400	1.2us	-144.4679dBc/Hz @10MHz	0.178	1.10004
125	500	980ns	-145.7717dBc/Hz @10MHz	0.134	0.82812
150	600	880ns	-145.8564dBc/Hz @10MHz	0.119	0.73542
200	800	420ns	-144.3804dBc/Hz @10MHz	0.113	0.69834
Assume the Bit error ratio is 10^{-3}					

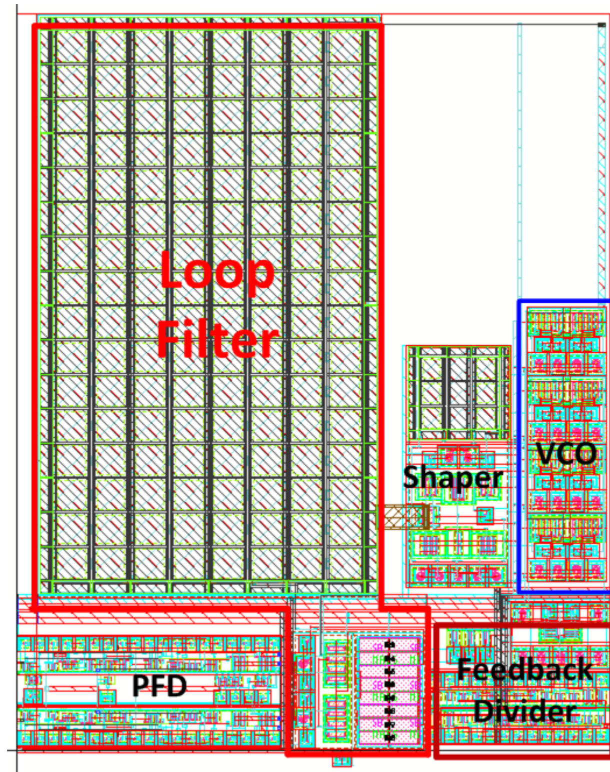


Figure 4.57: Layout view of the PLL used in the proposed CIS

The output clock channel transports a dual data rate (DDR) clock, synchronous to the digital data on the other SLVS channels. The clock is a DDR clock, which means the frequency is half of the output data rate. When the maximum data rate is set 1 $Gbps$, the SLVS output clock is 500 MHz. Since the sensor is a symmetric architecture, half of SLVS channels are located on the top- and bottom-side of the sensor. One clock at either side is used by the reciever on the FPGA to deserialize the data.

The SLVS block could provide a voltage swing of 200 mV on a 100 Ω load and a common-mode voltage of 200 mV. So, the differential voltage is, therefore, 400 mV as depicted in Figure 4.58. The output current is 2 mA with power consumption at the load of 0.4 mW. The layout of a 12-bit header, a serializer block, I/O pads, and SLVS drivers is shown in Figure 4.59.

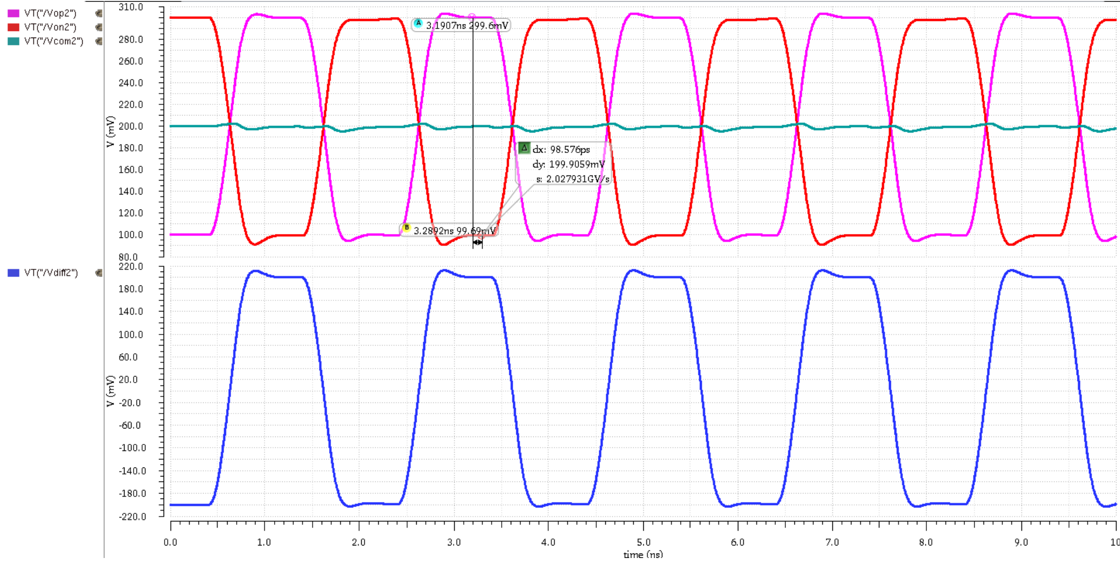


Figure 4.58: Single-end, differential, common-mode outputs of one SLVS block

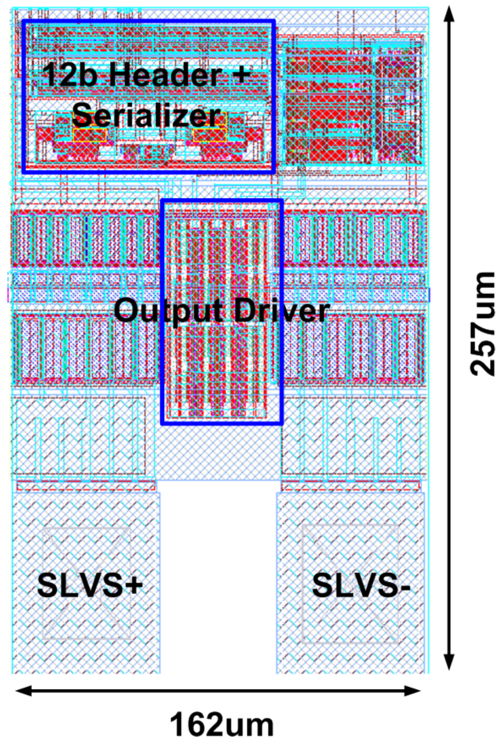


Figure 4.59: Single SLVS PAD includes a fixed header, serializer and SLVS driver

4.6 Final Layout and Chip Photograph

Two prototypes of the proposed CIS architecture have been fabricated in CIS 0.18 μm process. Their specifications are summarized in in Table 4.10. By comparison with On Semiconductor LUPA3000 product [10], the proposed CIS provides a higher pixel rate and frame rate as shown in Table 4.11.

Table 4.10: Proposed CIS architecture specifications

Process	0.18μm CIS (1P6M)
Pixel Size	$20\mu m \times 20\mu m$
Pixel Type	4T radhard Pixel with low image lag
Array dimension	$768(H) \times 1024(V)$ $128(H) \times 1024(V)$
Output format	Differential serial digital
Power Supply	3.3V: Pixel array 1.8V: Periphery circuit
Power Consumption	-
Master Clock	250 MHz
Package	Chip-on-Board
Die size	$17.04\ mm \times 25.125\ mm$ $4.24\ mm \times 25.125\ mm$
Camera Board size	$5\ inch \times 2.5\ inch$
Main FPGA Board size	$5\ inch \times 6\ inch$

Table 4.11: Specification comparisons of different CISs

CIS Parameters	Unit	OnSemi LUPA3000	768 x 1024 CIS	128 x 1024 CIS
Pixel array	pixels	2.90E+06	786432	131072
Frame rate	fps	485	1.00E+04	1.00E+04
# of LVDS/SLVS	-	32	96	16
each LVDS/SLVS speed	bits/s	4.12E+08	1.00E+09	1.00E+09
# of ADCs	-	64	3072	512
ADC speed	samples/s	2.58E+07	3.13E+06	3.13E+06
ADC resolution	bit	8	10	10
Data Rate	bits/s	1.32E+10	9.60E+10	1.60E+10
Pixel rate	pix/s	1.41E+09	7.86E+09	1.31E+09

The top layout views were shown in Figure 4.60 and 4.61. The large format CIS has 12 slices, and the small format CIS has only two slices, left- and right side-slice of the latter one. The pixel array is located in the middle. The row decoder and driver are located at the left side of the pixel array, and each slice has the same readout circuitry located on the top and bottom of the pixel array. Each column has four readout lines, two on the left and two on the right. The proposed readout block is located on both top and bottom side. The small format CIS has 754 PADs, and the large format CIS has 1114 PADs. The micro-photograph of these two chips on the same wafer are shown in Figure 4.62.

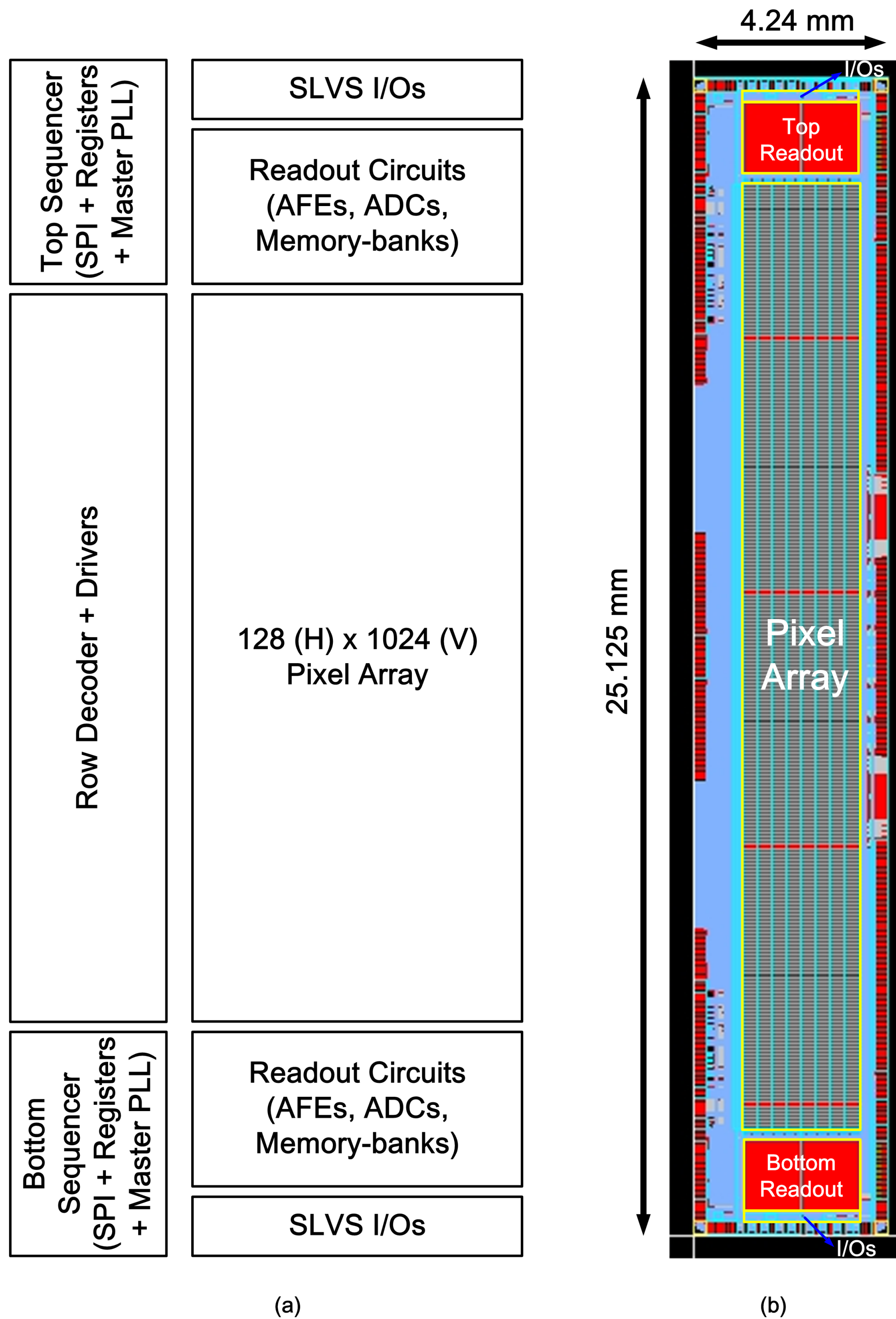


Figure 4.60: (a) Block diagram and (b) top layout view of the 128×1024 imaging chip

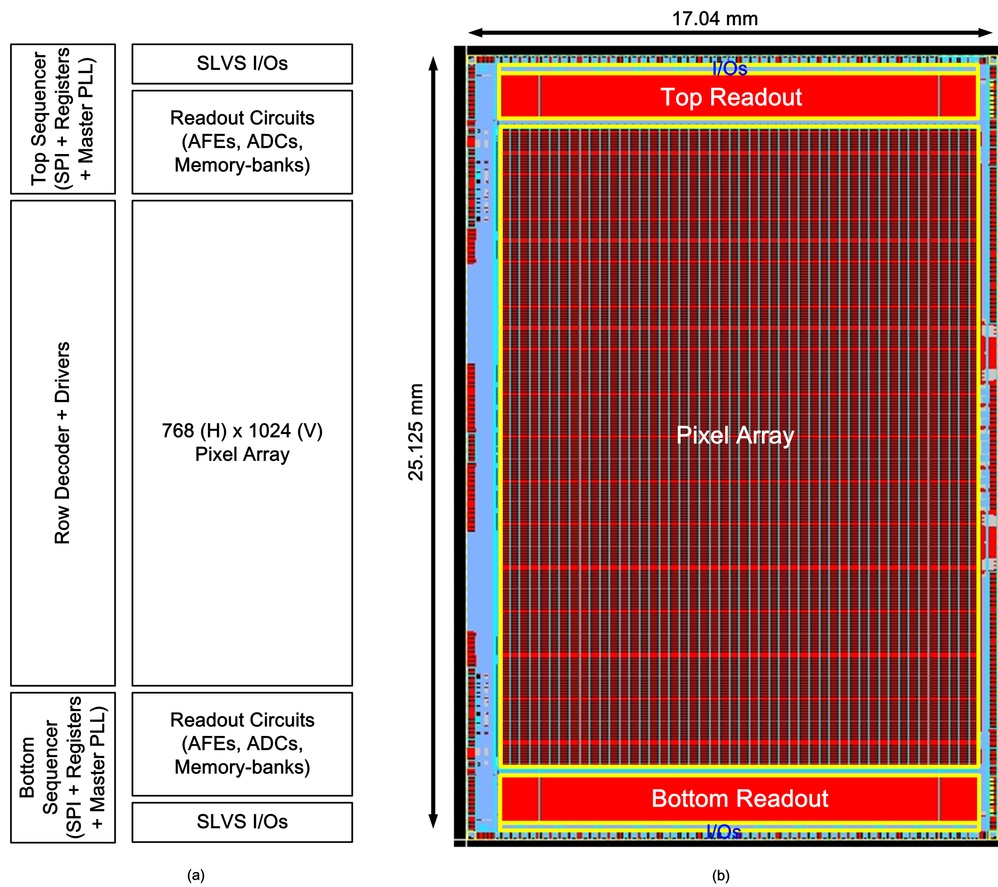


Figure 4.61: (a) Block diagram and (b) top layout view of the 768×1024 imaging chip

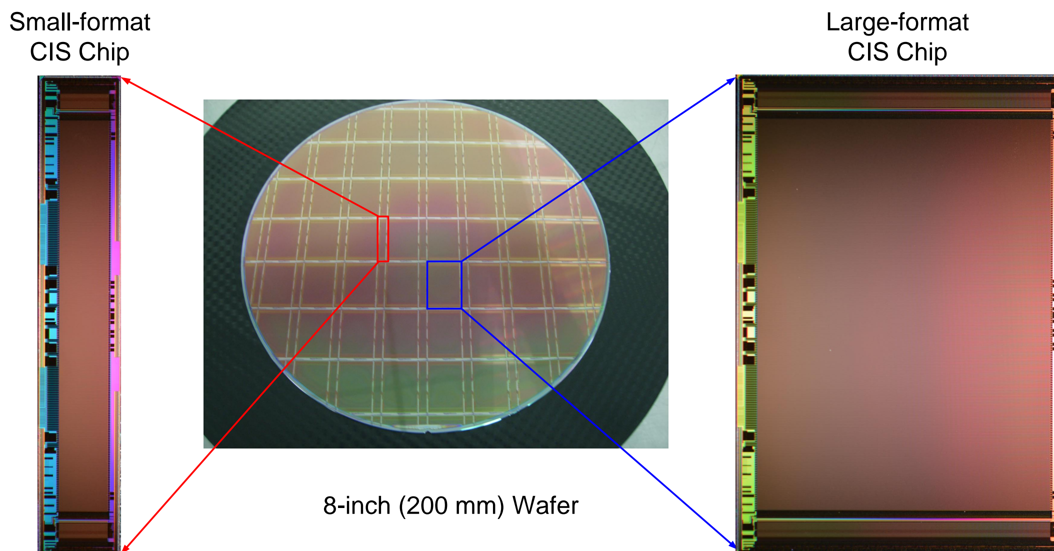


Figure 4.62: Die photos for two camera prototypes on a 8-inch wafer

Chapter 5

CIS Chip Measurement

This chapter focuses on the chip measurement of the small-format CIS. The first section 5.1 of this chapter briefly describes the hardware design and PCB implementation of the small-format CIS prototype. Next, Section 5.2 discusses the chip test, including the on-chip master PLL testing in Sub-section 5.2.1, the sequencer test in Sub-section 5.2.2, the fixed-pattern data test in Sub-section 5.2.3, the programmable frame rate test in Sub-section 5.2.4, and the TID radiation test in the final sub-section.

5.1 Hardware Design and PCB Implementation

In order to test the small-format CIS chip with 128×1024 pixels, a total of seven boards — one main FPGA board and six daughterboards — have been designed and fabricated. The main FPGA board and five of the daughterboards are used to place the FPGA chip and the other peripheral ICs in order to provide clock and power supplies for the FPGA. In addition, the peripheral ICs that provide the power supplies, reference signals, and clock signals for the sensor chip are placed around the mezzanine connectors in order to keep the signal traces as short as possible. The final daughterboard is used to place the sensor chip. Figure 5.1 depicts the main FPGA board which houses the FPGA chip, the camera link connectors to connect the frame grabber, the mezzanine connectors to connect the sensor board, six sockets to connect the other daughterboards to the housing of the DDR3 memory chip, camera link transmitters, power management ICs and oscillator ICs. The daughterboards are shown in Figure 5.2.

The sensor daughterboard is shown in Figure 5.3. Four SMA connectors are used by the on-chip PLLs for testing the output clock. Four testing headers, containing 20 pins each, are connected to digital control signals coming out of the top and bottom sequencers. Due to the fact that the sensor board has 754 pads, there is no standard package to fit in the sensor chip. The chip-on-board (COB) packaging technology is used to wire-bond the sensor chip to the daughterboard and most of the bypass capacitors are placed on the underside of the board. The mezzanine connectors (board-to-board connectors) are used to connect the sensor daughterboard to the main FPGA board. Two mezzanine connector plugs with 120 pins are placed

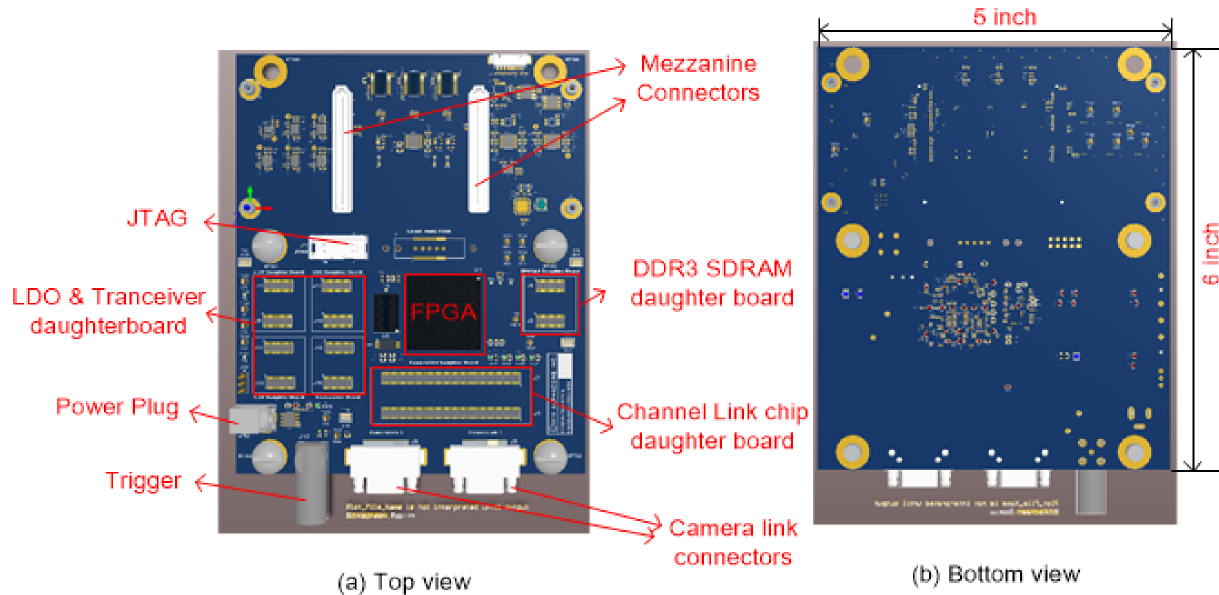


Figure 5.1: The 3D view of the main testing board with FPGA

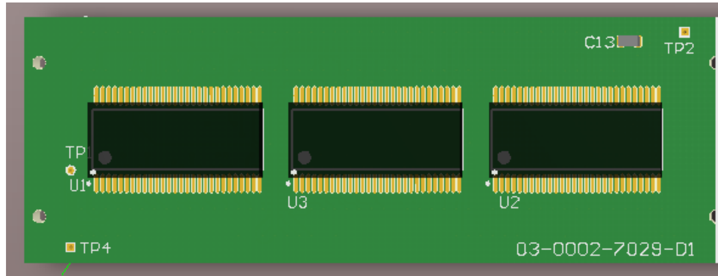
on the sensor daughterboard, while two mezzanine connector receptacles with 120 pins are placed on the main FPGA board. Figure 5.4 illustrates the pin assignment of the mezzanine connector plugs.

Table 5.1 lists the major ICs in the PCB boards that test the CIS chip. The peripheral ICs used by the CIS chip are placed around the mezzanine connectors on the main FPGA board. Both the main FPGA board and the sensor daughterboard were designed in ten layers, with several power and ground planes, while the other daughterboards were designed in four layers. The 16 channels of differential SLVS signals were routed carefully in order to keep their impedance match and placed between the power and ground planes. Several power domains, including 3.3 V, 1.8 V digital, 1.8 V analog, 1.8 V for the PLL, and 0.4 V for SLVS I/Os, make designing the PCB more difficult.

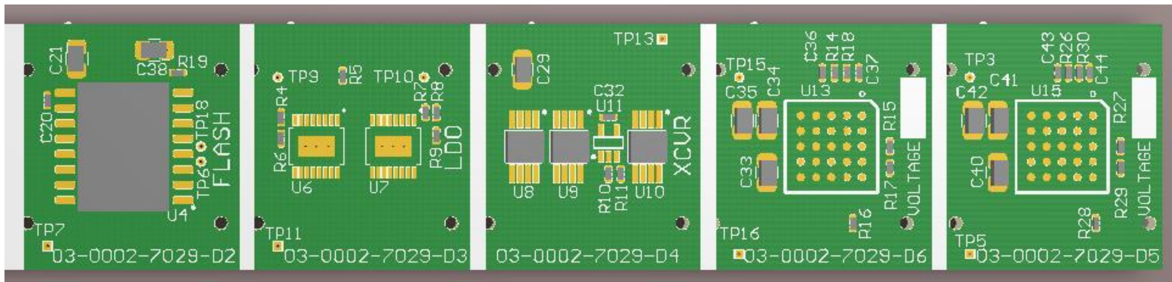
5.2 CIS Chip Test

The sensor testing system is illustrated in Figure 5.5. An external frame grabber (iPORT CL-Ten designed by Pleora Technologies Inc.) is used to transmit raw image data simultaneously from two camera link connectors on the main FPGA board to the PC through a high-performance GigE Vision 2.0 over a 10-Gigabit Ethernet (10 GigE) link. As the imaging data is converted to Ethernet packets, the frame grabber enables the aggregation of the system cable and analysis equipment outside of harsh radiation environments.

The camera system's firmware can be programmed into the FPGA through the USB-Blaster II cable by the PC. Two LVDS pairs in the camera link interface are used for Universal Asynchronous Receiver/Transmitter (UART) communication to and from the FPGA and the frame grabber. Pleora Technologies Inc. has developed a software application programming interface (API) that can send and receive series data from the FPGA.



(a) Camera link transmitter board

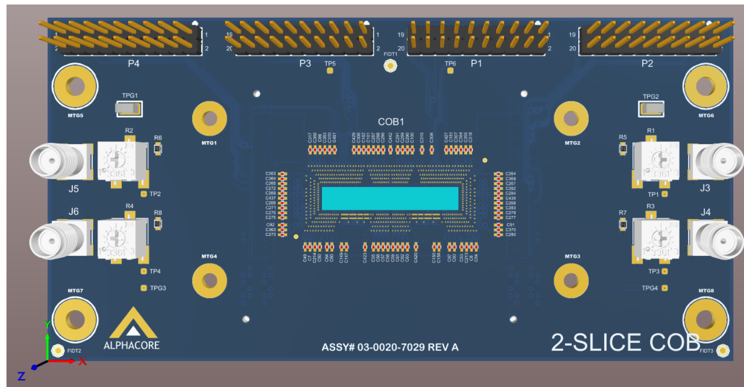


(b) Boards with power manager ICs and oscillator ICs

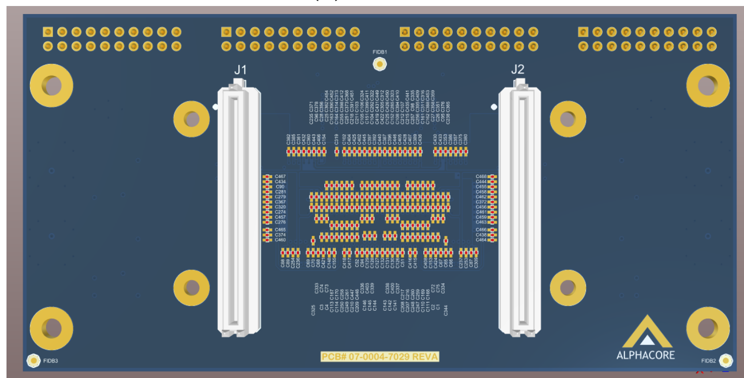
Figure 5.2: The 3D view of daughterboards with power manager and oscillator ICs for the FPGA

The chip testbench setup is shown in Figure 5.6. A block diagram of the proposed camera testing system is illustrated in Figure 5.7. The Serial Peripheral Interface (SPI) protocol is used by the PLL (Si5326), DACs (Max5318 and AD5624), and the CIS chip. Three different SPI masters are designed in the FPGA firmware, with each one having an independent first-input first-output (FIFO) block that can store the configuration files. All of the configuration files are transmitted through the UART from the PC host.

In order to run the camera system, we must follow a three-step process. The first step is to enable the LDOs to provide the primary power supplies for all the ICs on the boards and to reset every register in the camera system. The second step is to configure all SPI masters in the FPGA's firmware to prepare the clock signal, the reference signals, and settings of the sensor chip. Finally, the third step is to enable the clock selection block on the sensor chip to run the finite state machine in the on-chip SPI slave for the normal operation of the CIS chip. In every line time, each SLVS channel then transmits 332 digital bits — 320 bits of serial data with a 12-bit digital header — to the FPGA, with the data frequency being equal to four times that of the clock input provided by the Si5326 IC. One frame consists of 256 line-times, and the sensor chip constantly transmits serial data to the FPGA until the state machine clock is stopped, or the reset signal is



(a) Top-view



(b) Bottom-view

Figure 5.3: The 3D view of the small-format CIS COB

activated. Although the camera link interface has three different configurations(base, medium, and full) and the maximum possible throughput is 680 MB/s, this is still insufficient for transmitting 16 SLVS channels, each with a full speed of 1 $Gbps$. Therefore, the serial image data has to be converted to parallel data, which is stored in a DDR3 memory chip. A data recovery block is necessary to detect the 12-bit digital header in each line time and to store the subsequent effective 320b image data. The image data can then be read out from the DDR3 memory and can be encoded and transmitted by the DS90CR287MTD ICs based on camera link protocol. Finally, the complete image can be plotted by the eBUS player in the PC.

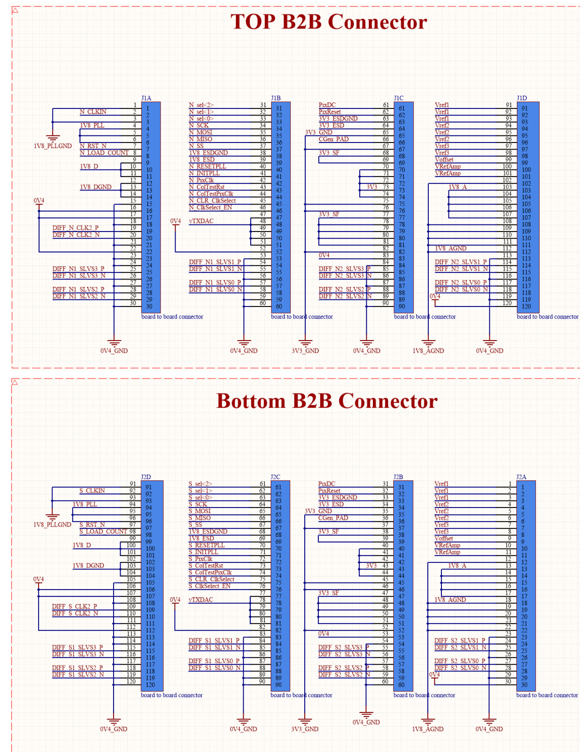


Figure 5.4: The schematic of the mezzanine connector plugs

Table 5.1: Major ICs used in the 2Slice Camera System

Item	Quantity	Integrated Circuit	Function Description
1	3	MAX5318	DACs to provide analog reference voltages used by column-parallel ADCs
2	1	FPGA 5CEFA9	Intel Cyclone V FPGA
3	6	LT3045	LDOs to provide low-noise power supplies
4	1	IS43TR16128B	DDR3 Memory with 2Gbs128M x 16
5	1	LM27761	Negative charge pump to provide -1.5V
6	2	AD5624	12B DAC external reference
7	1	ADR4530ARZ	low drift voltage reference
8	1	Si5326	Clock generator to provide clock input for the sensor
9	3	LTC2052	Opamp quad zero drift as buffers
10	1	LTC2368-24	24B ADC for calibrating DAC reference voltage
11	3	DS90CR287MTD	LVDS 28-Bit Channel Link Transmitter for Camera Link Interface
12	1	EPCQ128	quad-serial configuration (EPCQ) devices. EPCQ is an in-system programmable NOR flash memory
13	1	ASDMB-12MHz	Standard Clock Oscillators 12.000MHZ 50ppm
14	1	SG-210SGB	Crystal Oscillator to provide 19.2MHz
15	2	LT3022	LDO to provide 1.1V and 2.5V for the FPGA
16	2	LTM4623	Step-Down DC/DC μModule Regulator

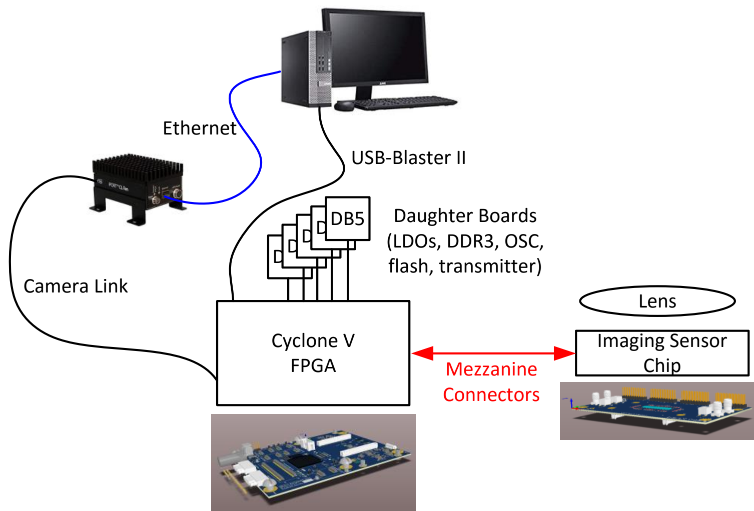


Figure 5.5: Block diagram of camera testing system

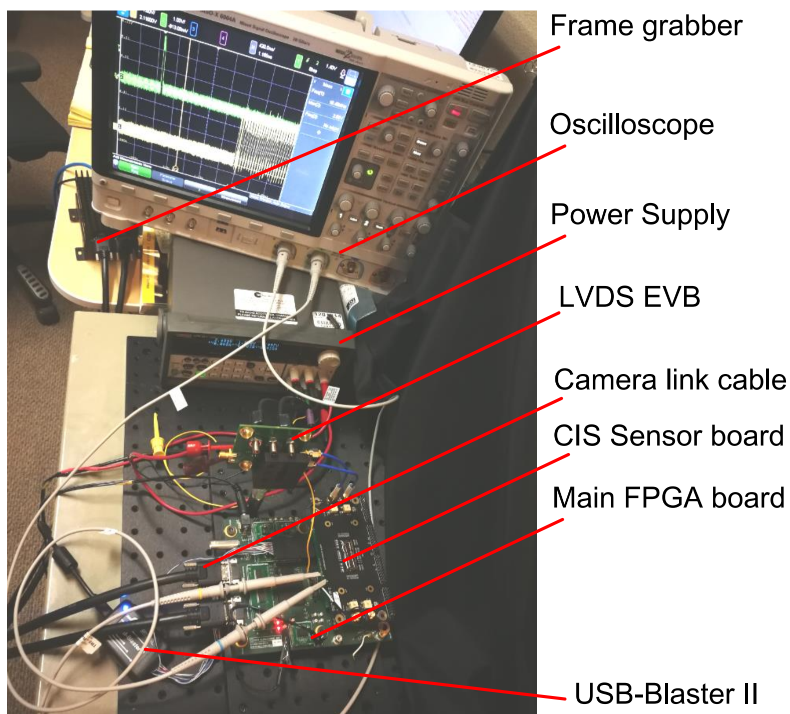
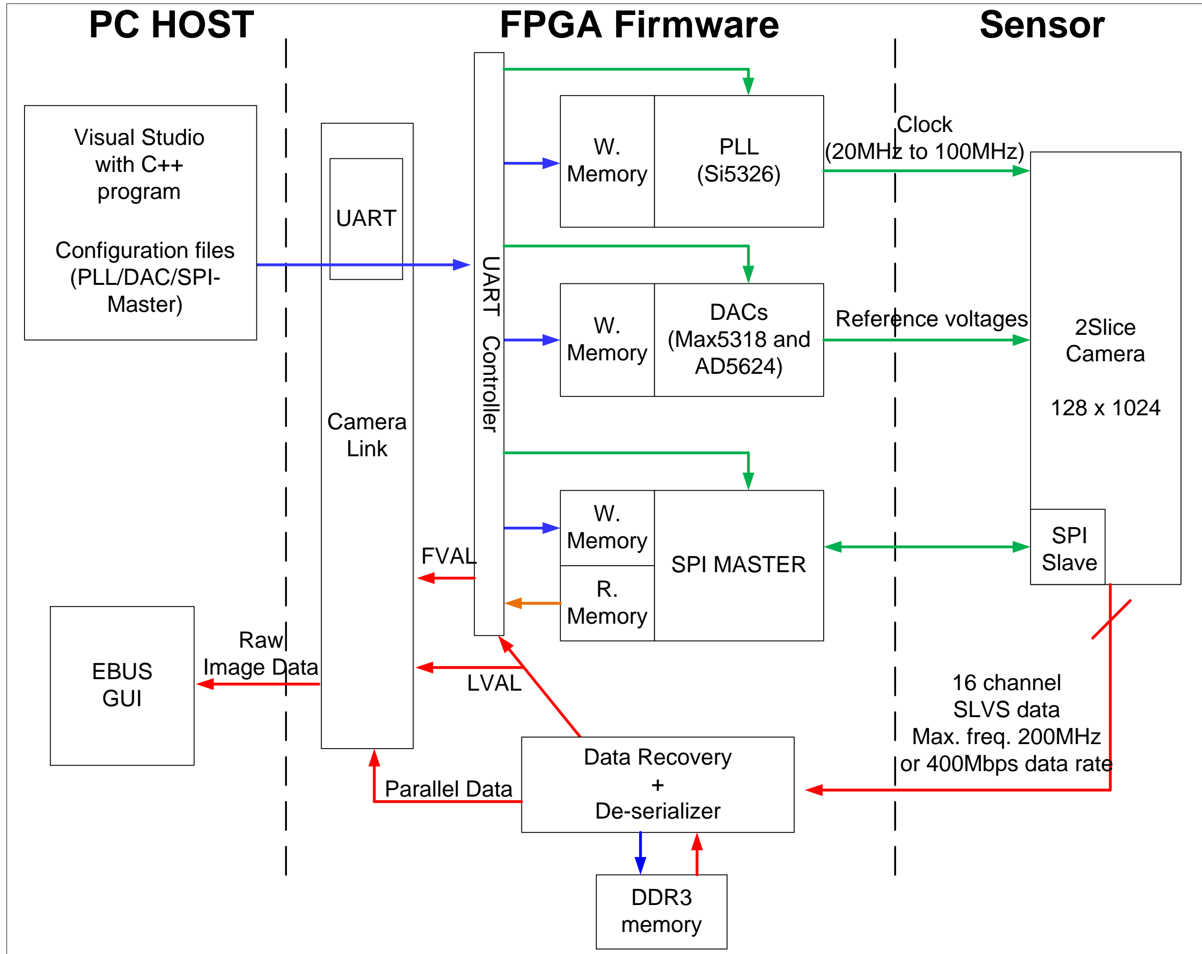


Figure 5.6: CIS testbench setup



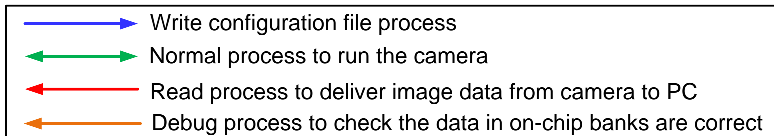


Figure 5.7: Block diagram of camera testing system

5.2.1 PLL Test

Two master PLLs, working as a frequency multiplier, have independently differential SLVS outputs. Two pairs of SMA connectors are used by clock outputs on the board as shown in Figure 5.3. The timing of the entire sensor is clocked by master PLLs. The top master PLL (on the right side of the figure) provides the clock signal for the top sequencer block and readout chain, while the bottom master PLL (on the left side of the figure) provides the clock signal for the bottom sequencer, the row decoders and the bottom readout chain. Both of these PLLs have differential outputs for testing their functionality.

For sensor testing, the primary step is to validate the functionality of the master PLLs. Figure 5.8 illustrates the testing structure. The ADN4651/ADN4652 evaluation board with dual LVDS channels is used to connect the PLL outputs to an oscilloscope.

The input reference clock is provided by the Si5326 IC from Silicon Lab, Inc. on the main FPGA board. Varying the input clock from 20 MHz to 125 MHz, the master PLL can provide a four-times faster clock output. The testing results that were captured by an oscilloscope have demonstrated its functionality, as shown in Figures 5.9-5.12. Furthermore, the SLVS transmitter is also validated in a frequency range from 80 MHz to 500 MHz by the PLL testing results.

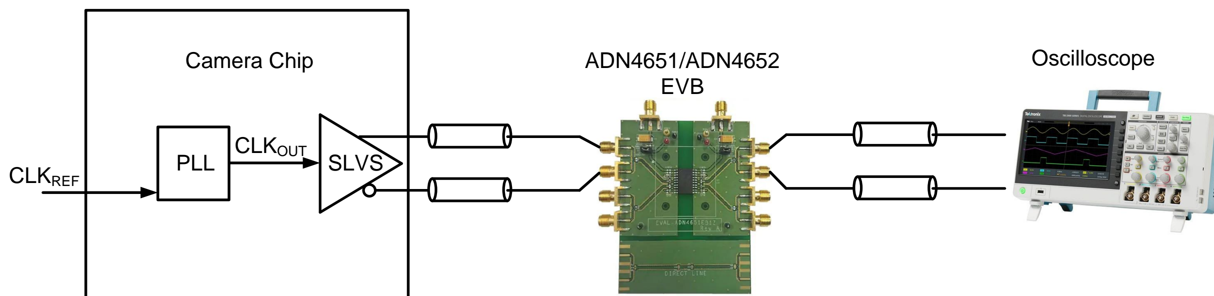


Figure 5.8: PLL test connection

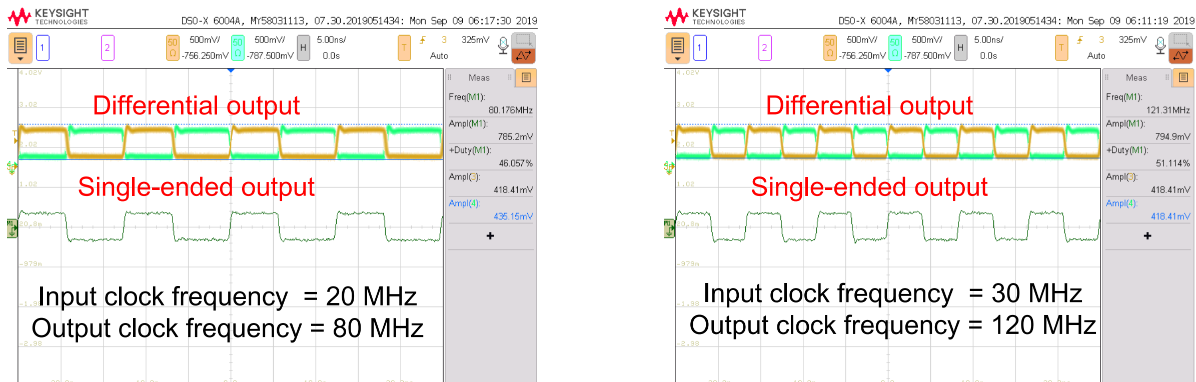
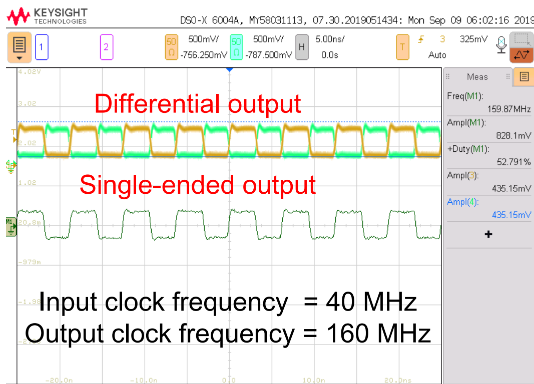


Figure 5.9: PLL output frequency 80 MHz **and** 120 MHz



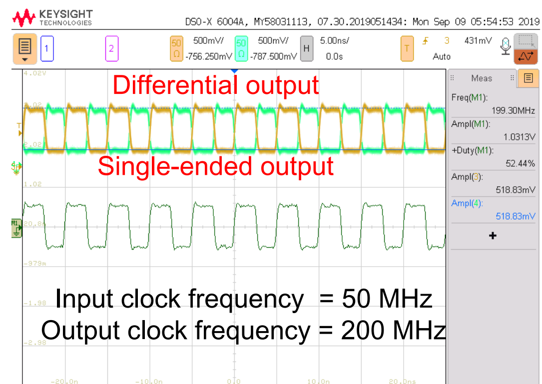
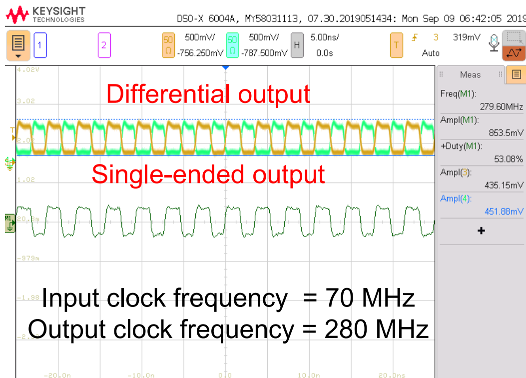


Figure 5.10: PLL output frequency $160\ MHz$ **and** $200\ MHz$



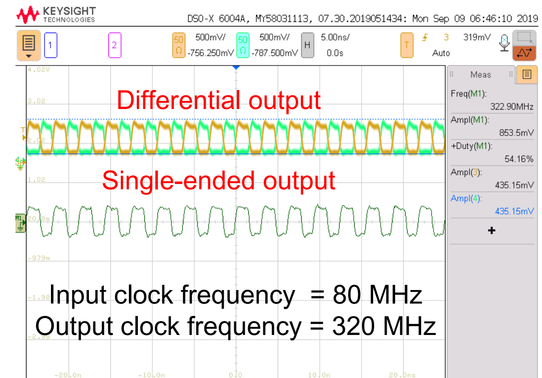
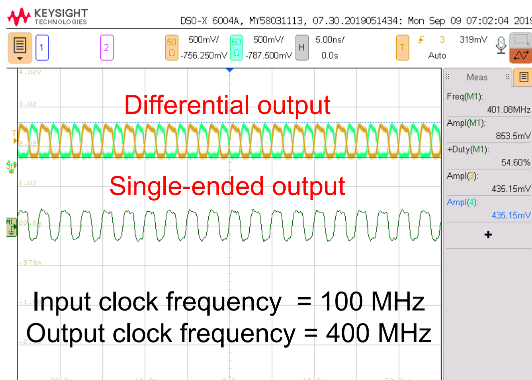


Figure 5.11: PLL output frequency $280\ MHz$ **and** $320\ MHz$



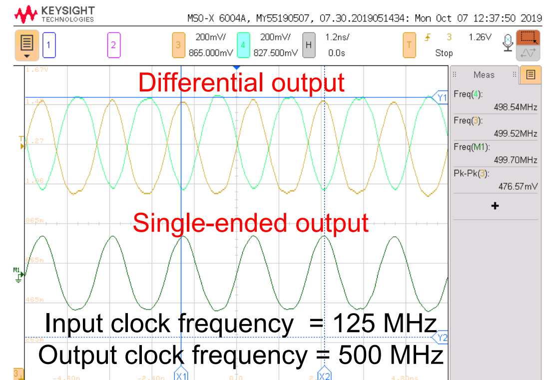


Figure 5.12: PLL output frequency $400\ MHz$ **and** $500\ MHz$

5.2.2 Sequencer Test

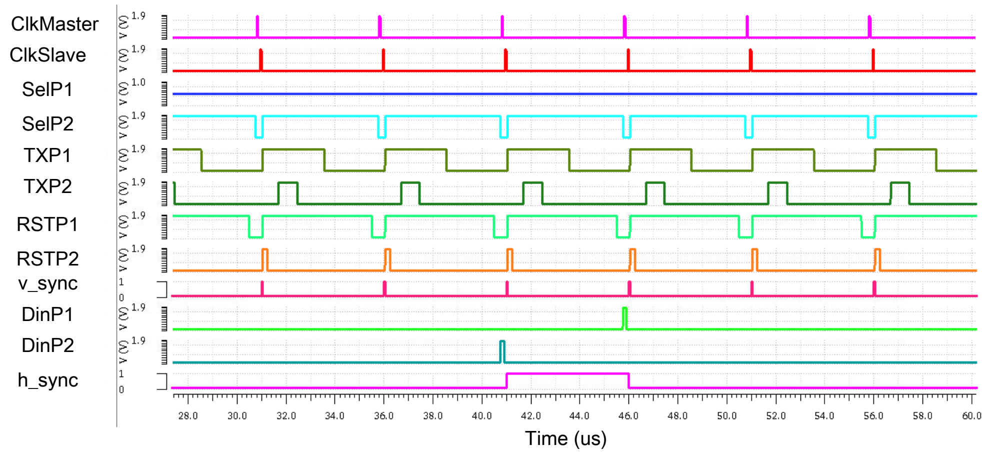
The sequencer is an essential component for the CIS prototype. It can configure the frame time, line time, and the starting and stopping row to be read out. It also defines the rising and falling edges of control signals used by column-parallel ADCs, PLLs, row decoders and SLVS transmitters. This means that validation of the sequencer is the next step after obtaining the correct clock signal.

An 8-to-1 debug multiplexer with 12-bit inputs is added on the CIS chip to test the functionality of the sequencer, which means each selection can output 12 different control signals that are used inside the CIS chip. Table 5.2 lists eight selections of control signals that can check sequencer functionality. When the selection signal is equal to $3'b100$, control signals of the row decoders - such as pixel reset, transfer gate, the beginning of the frame, etc. - can be detected at the outputs. For checking the start and stop row of the pixel windowing, the selection signal can be set to $3'b110$ and $3'b111$. The registers used to configure the programmable DACs in order to provide different bias current for comparators, PGAs, or current sources in column lines can be detected by setting the selection signal to $3'b011$. Other selections show the control signals of column readout circuitry.

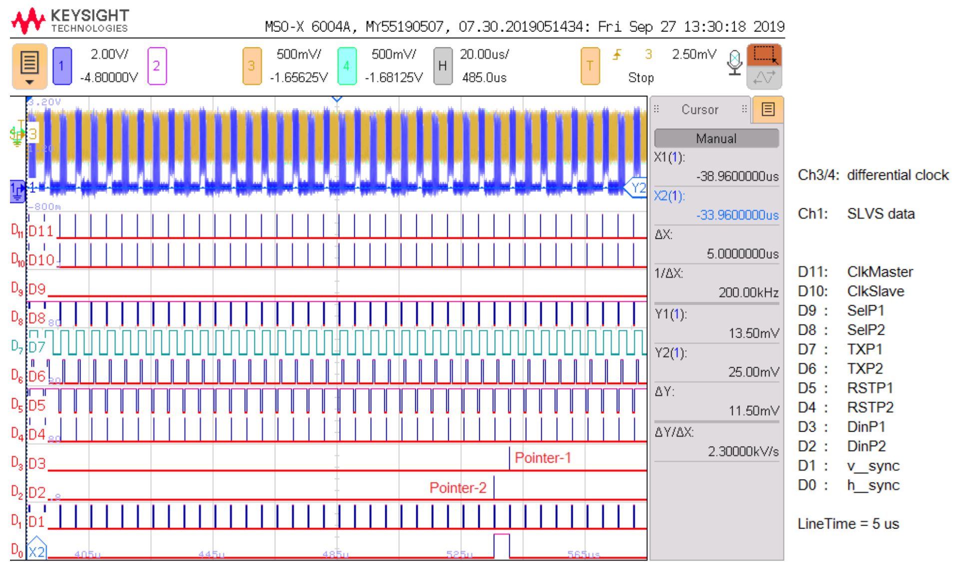
Figures 5.13 and 5.14 shows the simulation results versus the testing results.

Table 5.2: Eight different outputs by the debug multiplexer

Sel<2:0>	Debug MUX_OUT	Function
3'b000	SetBit<11:0>	ADC control signals
3'b001	LatchBit<11:0>	ADC control signals
3'b010	AmpReset,AmpSample1,AmpSample2, Clear, Latch, SampleReset, SampleVideo, EnReadMemA, EnReadMemB, Restore, Comp, Amp	Column peripheral circuits
3'b011	Sel_IADC,Sel_IColBias, Sel_IPGA	Current sources in the column lines and programmable DAC
3'b100	ClkMaster,ClkSlave, SelP1, SelP2, TXP1, TXP2, RSTP1, RSTP2, DinP1, DinP2, v_sync, h_sync	Row decoders
3'b101	AZ5,AZ4, AZ3, AZ2, AZ1, PixSample2,PixSample1, SetOffset, LatchOffset, GlobalTX, EnablePE1, EnablePE2	Comparator and SLVS
3'b110	VertWinStart	Row start address
3'b111	VertWinStop	Row stop address

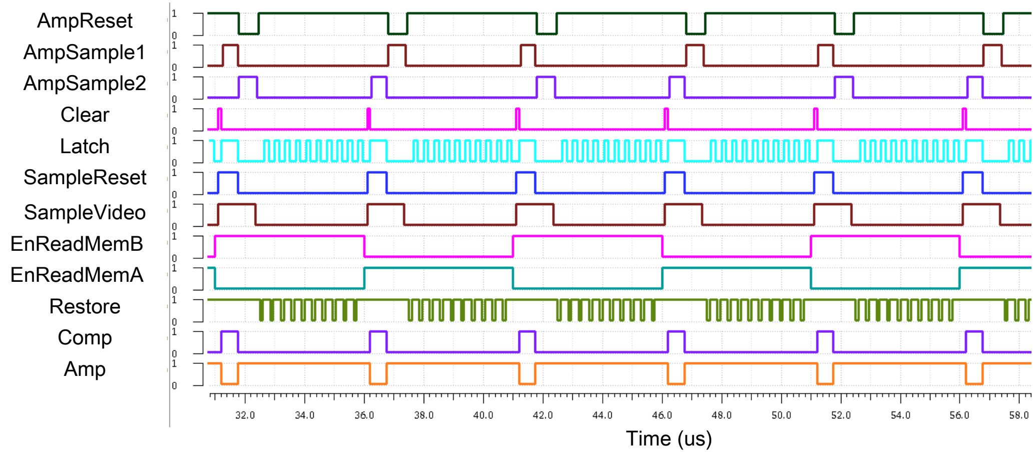


(a) simulation result

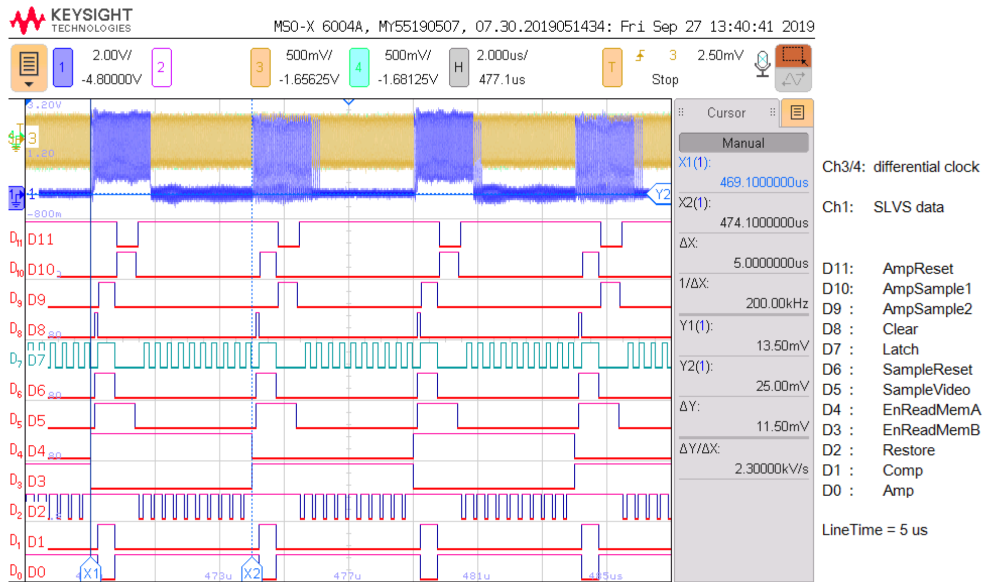


(b) measurement result

Figure 5.13: Measurement results of multiplexer outputs for row decoders matched simulation results



(a) simulation result



(b) measurement result

Figure 5.14: Measurement results of multiplexer outputs for ADCs matched simulation results

5.2.3 Fixed Pattern Test

The CIS prototype is designed to have the capability to be written by fixed-pattern data into memory banks. In every line time, one SLVS I/O transmits a 12b fixed header, $12'h50F$, and a 10b digital data with a total of 32 times. As shown in Figure 5.15, the header has been correctly detected and aligned with the clock output at 20 MHz. A fixed-pattern dataset, $10'h3F0$, was written into the CIS and is shown in Figure 5.16. Another example has two different fixed-pattern dataset, $10'h2AA$ and $10'h10A$. The fixed-pattern dataset, $10'h10A$, is written to all Membank-A, which can be delivered when EnReadMemA signal is low. The fixed-pattern dataset, $10'h2AA$, is written to all Membank-B, which can be delivered when EnReadMemB signal is low. As shown in Figures 5.17 - 5.19, the measurement results were matched to the Cadence simulation results.

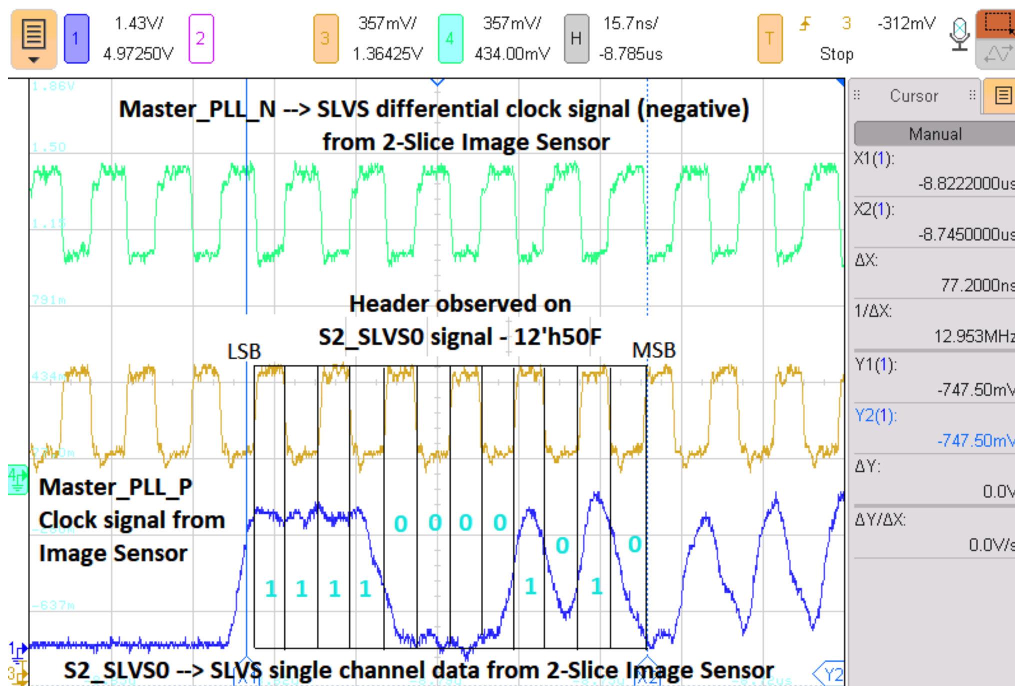


Figure 5.15: The fixed 12b digital header in every SLVS channel

Figure 5.16: One SLVS channel with $12'h50F$ header and $10'h3F0$ fixed pattern data

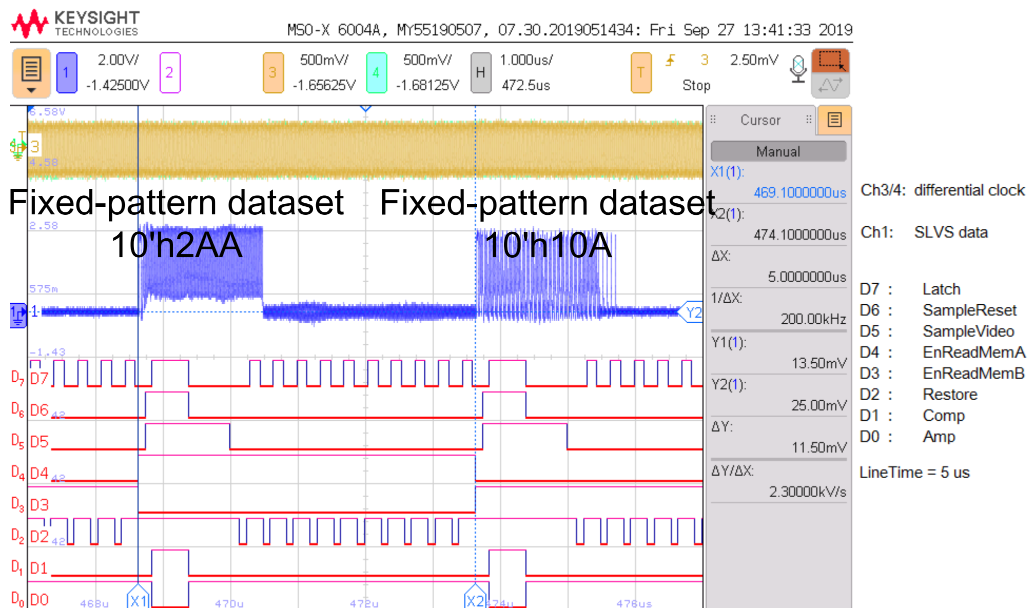
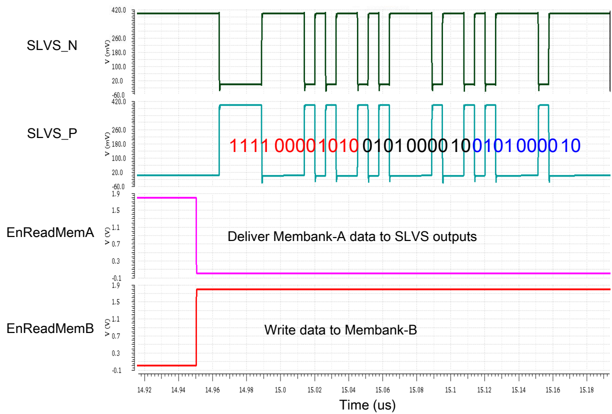
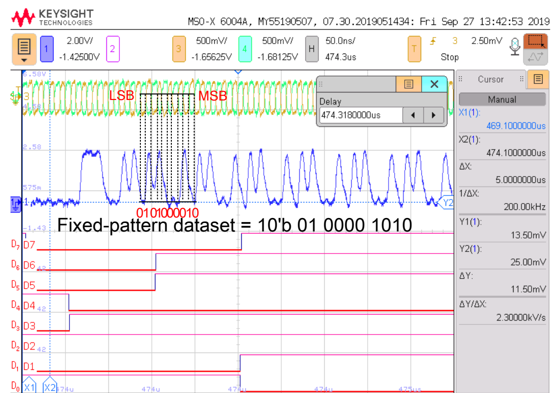


Figure 5.17: One SLVS channel with two different fixed pattern data in two line times

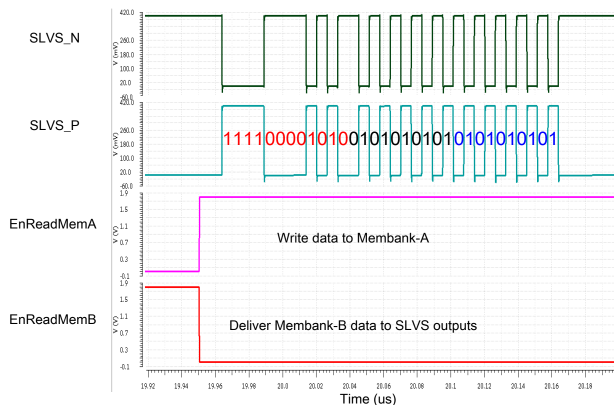


(a) Fixed-pattern dataset A simulation result

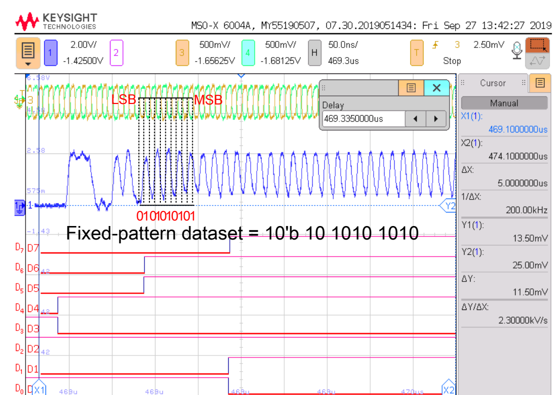


(b) Fixed-pattern dataset A measurement result

Figure 5.18: Fixed pattern data A simulation and measurement



(a) Fixed pattern data B simulation result



(b) Fixed pattern data B measurement result

Figure 5.19: Fixed pattern data B simulation and measurement

5.2.4 Frame Rate Test

The CIS prototype can program the frame rate through three parameters: the frame window size (or region of interest), the input reference clock, and the size of the counter in the sequencer. The frame window, or region of interest, is controlled by setting the start and stop addresses of the pixel array. A smaller frame window has fewer pixels but reduces the frame time for achieving a higher frame rate. The input reference clock can control the frequency of the counter which is used in the sequencer. The sequencer counter is used to determine when the rising and falling edges of control signals are used in the row decoders and readout circuitry. A higher frequency of the input clock can speed up the control timing.

When the input clock is fixed at a certain frequency, the size of the counter can then be used to program the frame rate. The counter is located in each sequencer and the size of the counter decides the line time. A single line time is equal to the maximum number of the counter multiplied by the input clock period. The sequencer has register banks, which can be programmed and written through SPI interface. Every 12b register stores the actual rising or falling edges of controls signals, and whenever the counter counts are equal to the register number, the corresponding control signal will go up or down. In other words, a look-up-table is used to save the rising and falling information of the control signals.

Figure 5.20 depicts the control signals and SLVS data when the CIS operates at 800 fps. The input clock frequency is 20 MHz and the counter size is 100. Therefore, a single line time can be calculated by

$$T_{LT} = \frac{1}{20MHz} \cdot 100 = 5\ \mu s \tag{5.1}$$

where T_{LT} is the line time.

The window size is 128×1024, which means that the start row address is $12'h000$ and the stop row address is $12'h0FF$. Considering the proposed CIS enables to read four rows of pixels at one line time, one frame time and frame rate can be calculated by

$$\begin{aligned} T_{FT} = T_{LT} \times \frac{1024}{4} &= 1.28\ ms \\ frame\ rate\ = \frac{1}{T_{FT}} &= 781\ fps \approx 800\ fps \end{aligned} \tag{5.2}$$

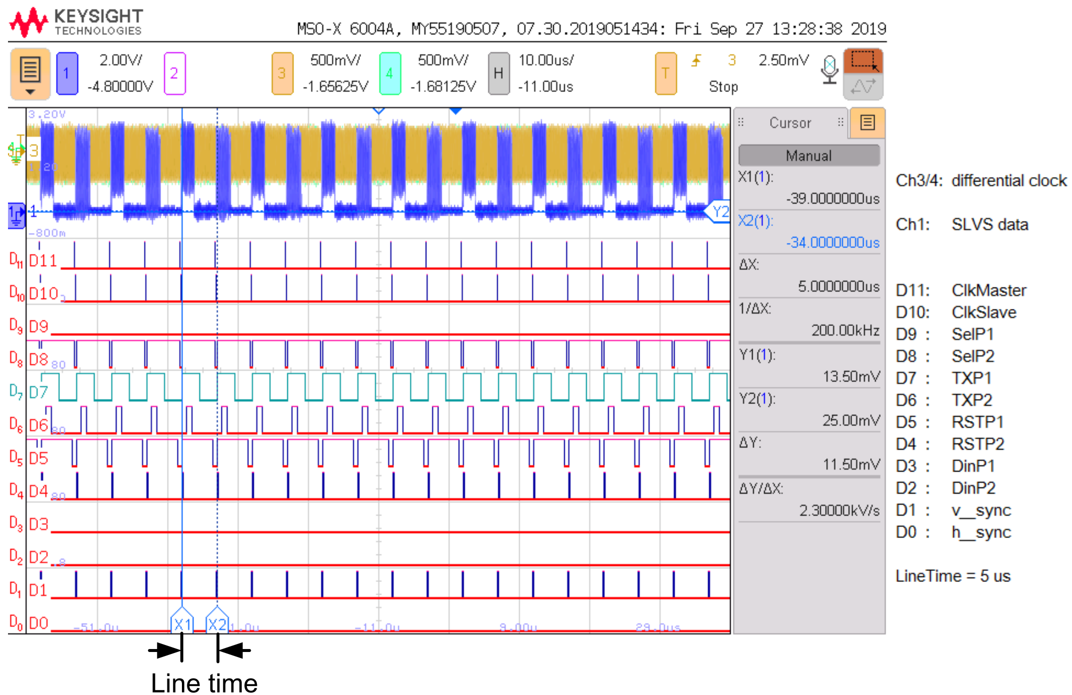
where T_{FT} is the frame time. Figure 5.21 shows one frame when CIS operates at 800 fps.

In order to increase the frame rate, rewriting the on-chip SPI slave configuration file to change the stop row address is convenient as there is no need to modify the clock frequency and the size of the counter. For example, Figure 5.22 illustrates the control signals and SLVS data when the CIS operates at 1600 fps by setting the stop row address to $12'h03F$.

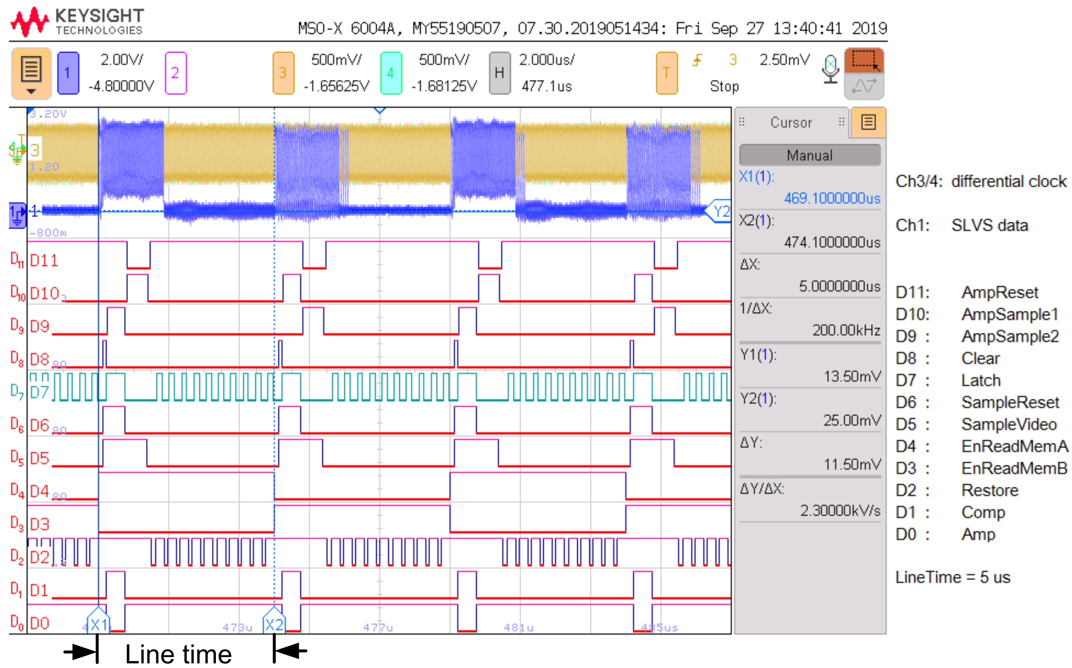
The input clock frequency can also be increased in order to increase the frame rate. Figures 5.23 and 5.24 depict the control signals and SLVS data when the CIS operates at $1,000$ fps by increasing the input clock frequency to 25 MHz. The line time is changed to 4 μs and the frame time becomes 1.024 ms with a 100 counter size and a full resolution, 128×1024.

The highest frame rate has been tested in full resolution is $4,000\ fps$ which can be achieved by increasing the input clock frequency to $100\ MHz$, as shown in Figure 5.25.

The proposed CIS not only leads to a faster frame rate, it can also be configured to obtain a low frame rate. By using the lowest input clock and maximum counter size, the CIS prototype can operate at $20\ fps$. Figure 5.26 shows the control signals and SLVS data when the CIS operates at $20\ fps$ with a counter size of $4,095$.



(a) Control signals provided by sequencer block for row decoders and one SLVS data @ LineTime = 5us



(b) Other control signals provided by sequencer block for ADCs and one SLVS data @ LineTime = 5us

Figure 5.20: Control signals when CIS operates at 800 fps

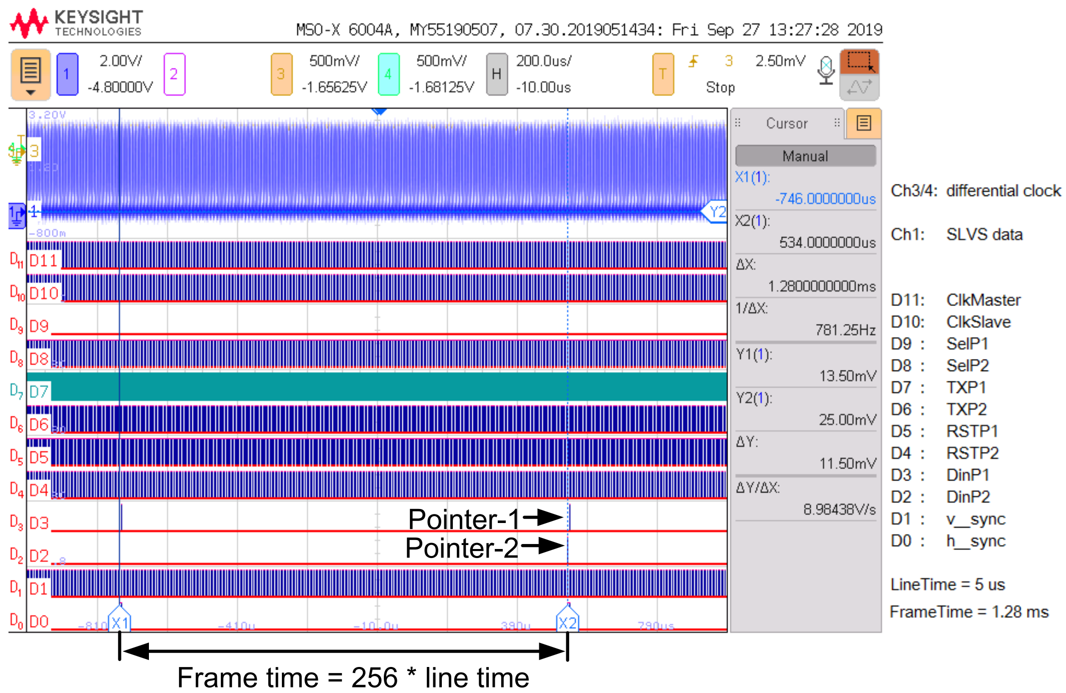
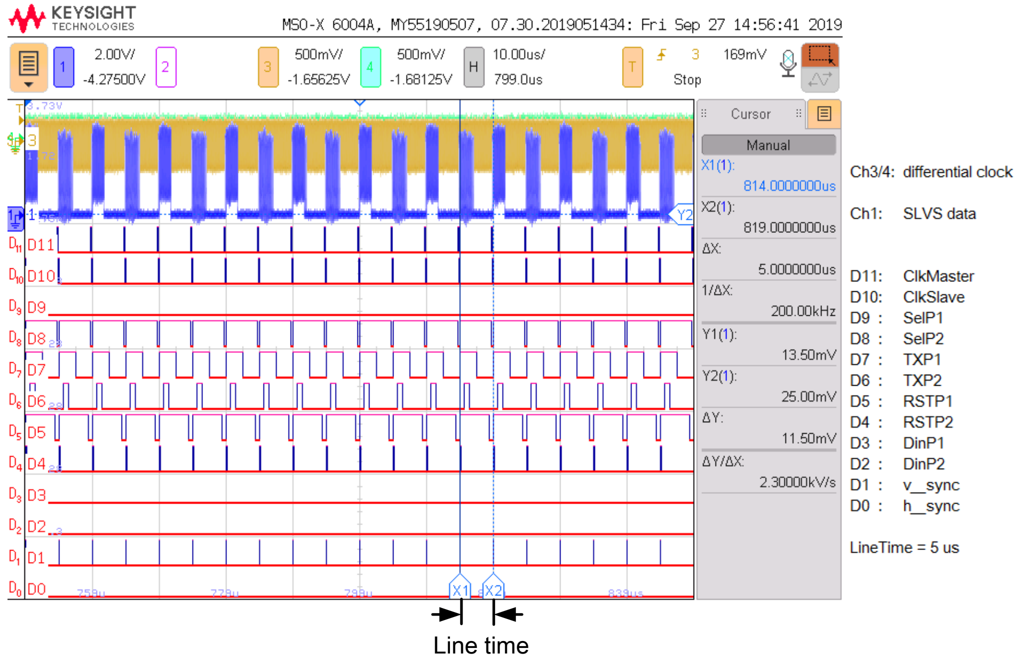
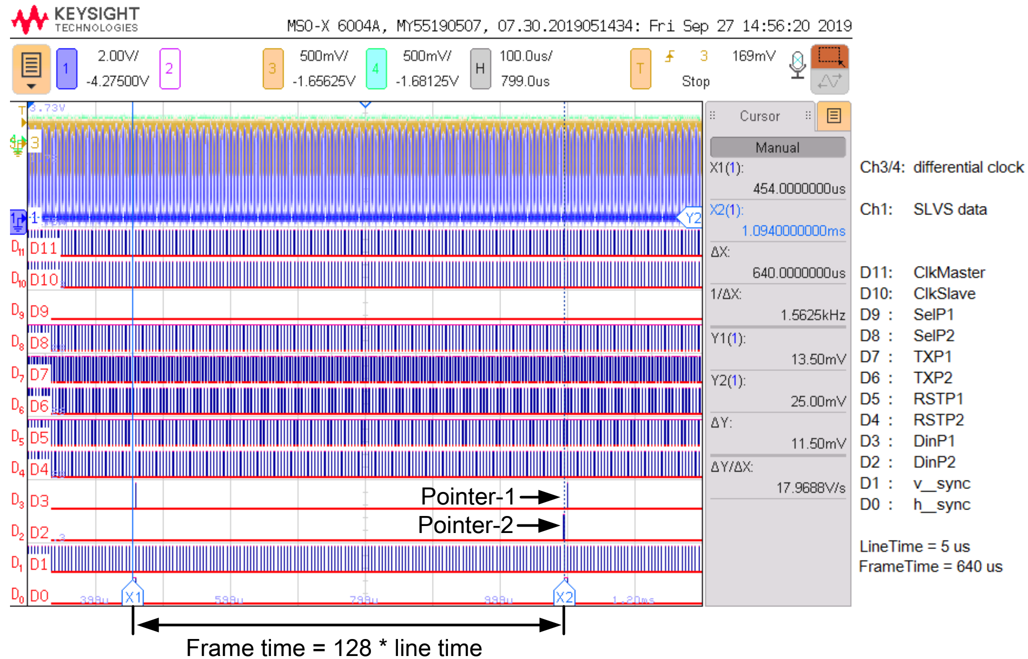


Figure 5.21: CIS operates at $800\ fps$

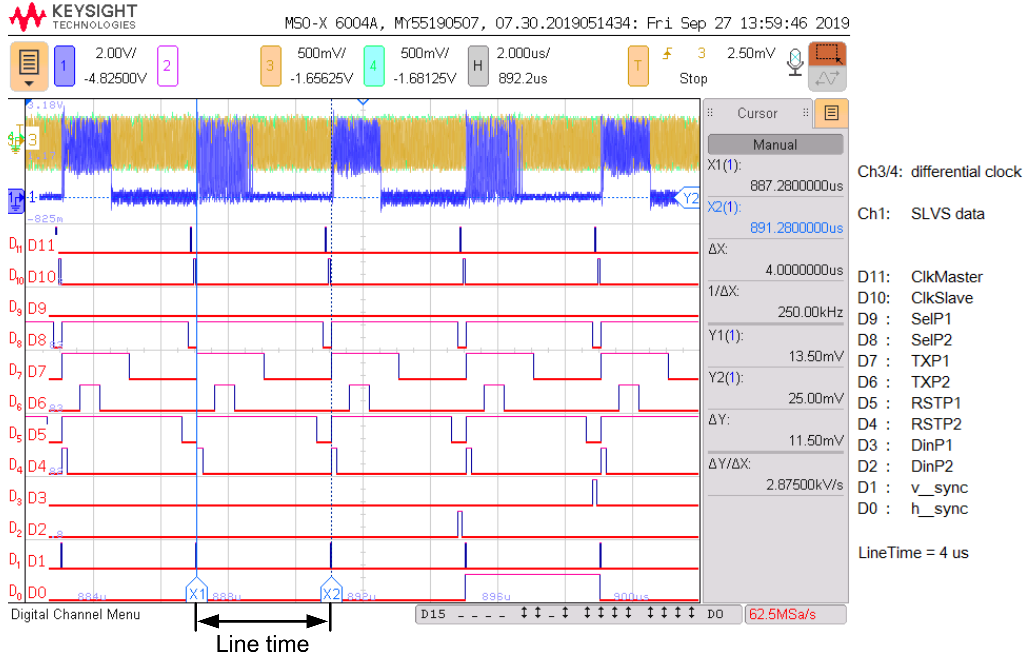


(a) Control signals provided by sequencer block for row decoders and one SLVS data @ LineTime = 5us

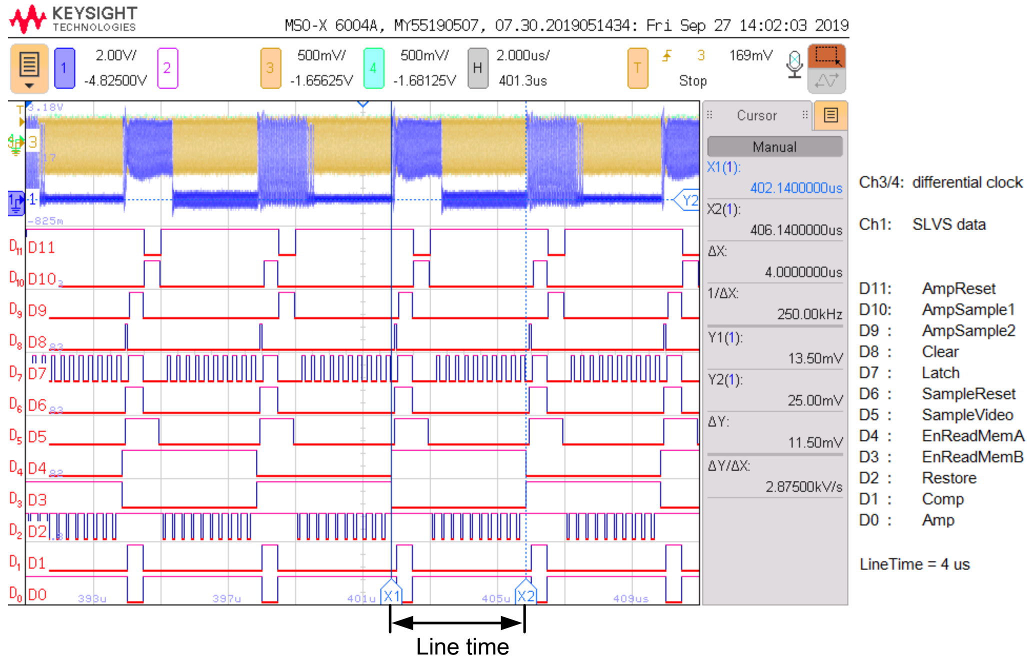


(b) Control signals and one SLVS data in one frame time of 640 us (frame rate = 1600 fps)

Figure 5.22: CIS operates at 1600 fps



(a) Other control signals provided by sequencer block for ADCs and one SLVS data @ LineTime = 4us



(b) Other control signals provided by sequencer block for ADCs and one SLVS data @ LineTime = 4us

Figure 5.23: Control signals when CIS operates at 1000 fps

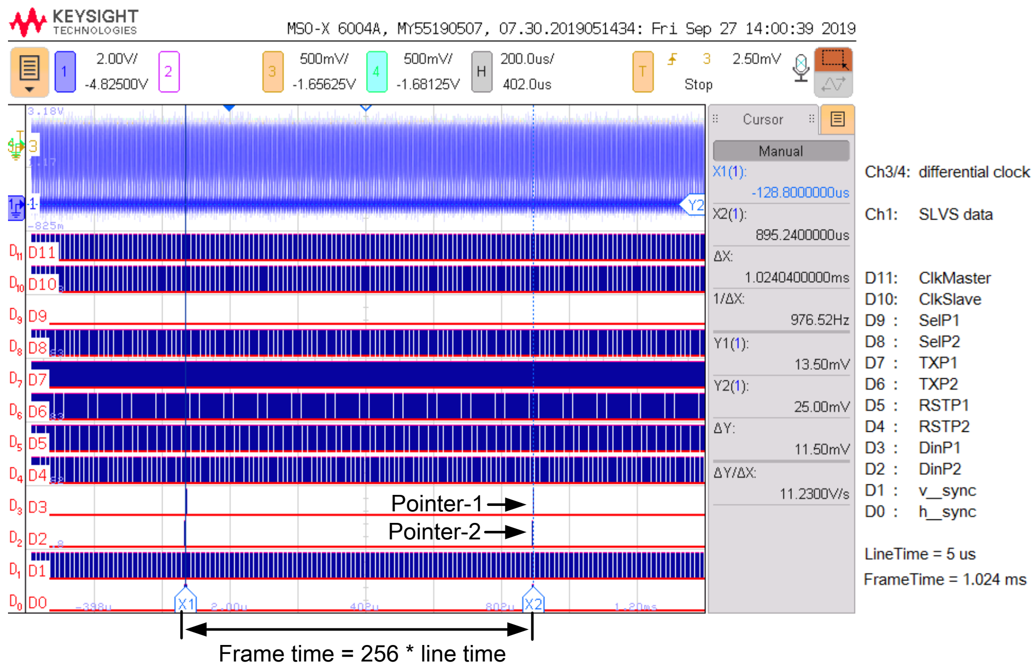
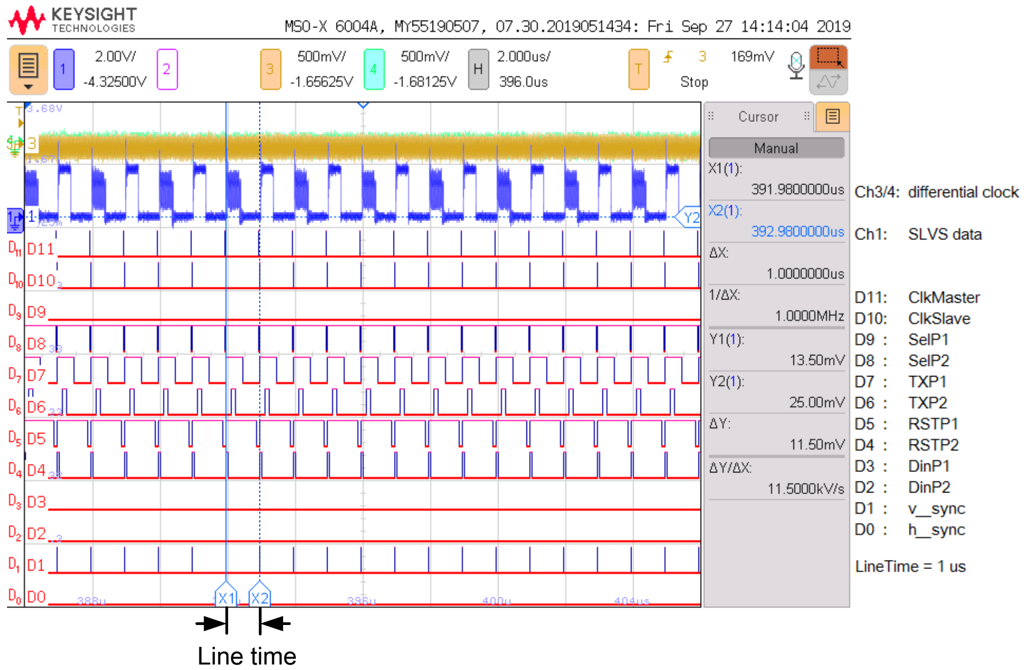
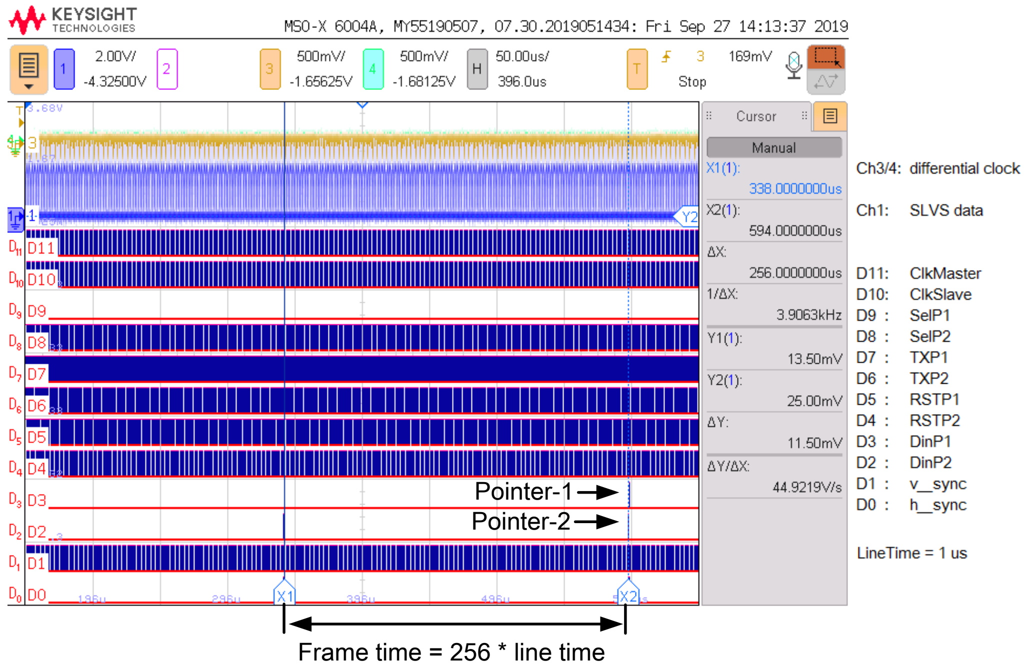


Figure 5.24: CIS operates at 1000 fps

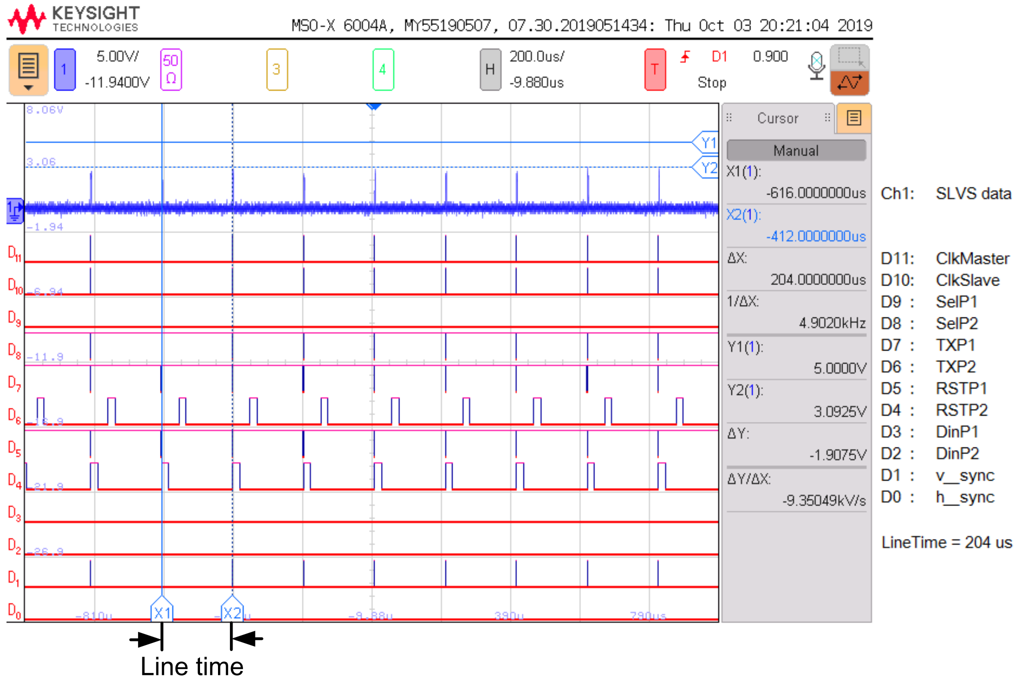


(a) Control signals provided by sequencer block for row decoders and one SLVS data @ LineTime = 1us

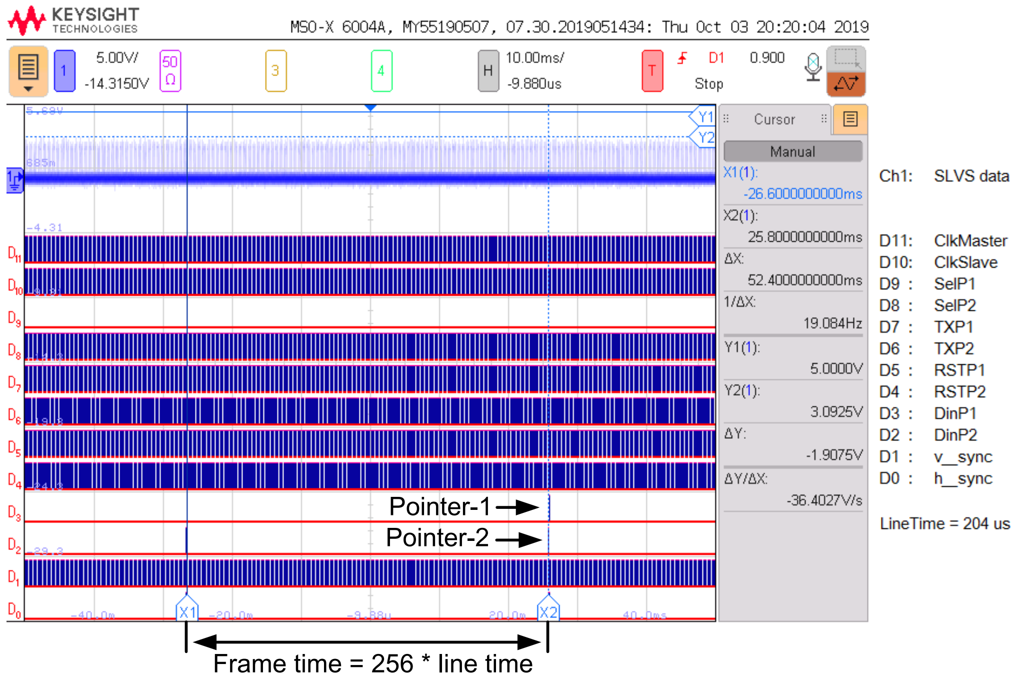


(b) Control signals and one SLVS data in one frame time of 256 us (frame rate = 4000 fps)

Figure 5.25: CIS operates at $4000\ fps$



(a) Control signals provided by sequencer block for row decoders and one SLVS data @ LineTime = 204us



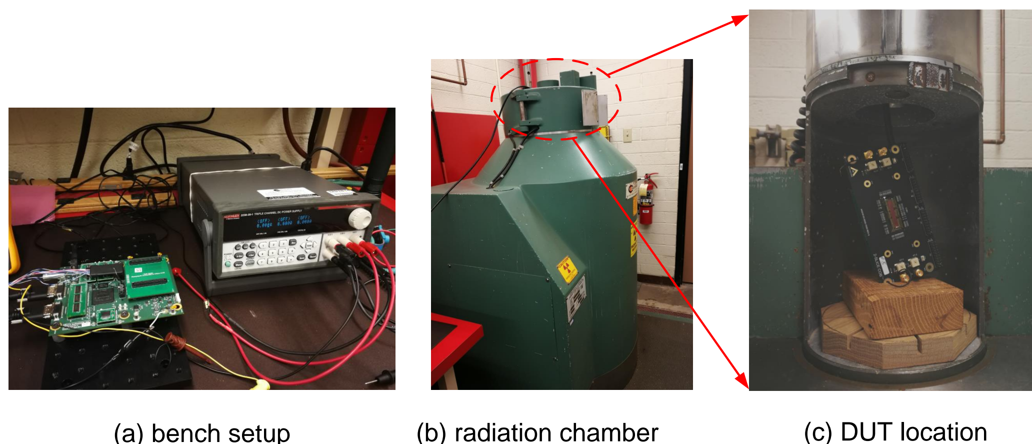
(b) Control signals and one SLVS data in one frame time of 52.4 ms (frame rate ≈ 20 fps)

Figure 5.26: CIS operates at 20 fps

5.2.5 TID Test

The CIS sensor was designed to be more tolerant of TID-induced damages. Each 4T pixel has enclosed-layout transistors and P-type guardrings for radiation tolerance. The sequencer block and register banks were placed in an isolated N-well. The readout circuitry uses thin-oxide transistors. The TID test is used to check the radiation tolerance of the pixel array.

Two TID radiation tests are illustrated in this section, which have been conducted by using Co60 gamma ray as the source. The dose rate is 259 $rad(SiO_2)$ per minute. The radiation test setup is shown in Figure 5.27. The small-format CIS chip (Device Under Test) was irradiated to a maximum total ionizing dose level of 125 $krad(SiO2)$ with incremental readings at 1 $krad(SiO_2)$, 2 $krad(SiO_2)$, 4 $krad(SiO_2)$, 6 $krad(SiO_2)$, 8 $krad(SiO_2)$, 10 $krad(SiO_2)$, 15 $krad(SiO_2)$, 20 $krad(SiO_2)$, 30 $krad(SiO_2)$, 50 $krad(SiO_2)$, 75 $krad(SiO_2)$, 100 $krad(SiO_2)$ and 125 $krad(SiO_2)$. Electrical testing occurred within five to ten minutes following the end of each irradiation segment. The pixel array of the DUT was biased by 3.3 V power supply when putting DUT into the radiation chamber.



(a) bench setup (b) radiation chamber (c) DUT location

Figure 5.27: TID test setup

The first test checks whether the TID induces a leakage current around the reset transistor. The reset transistor aims to reset the in-pixel storage node (floating diffusion). The TID-induced leakage current can pull the floating diffusion node up in order to reset the voltage, so that the pixel becomes dark even when shooting light on pixels. The method is tested by turning on all transfer gates and shooting light on the pixel array in order to discharge the parasitic capacitors in all diffusion nodes. During a long integration time or exposure time, the floating diffusion can have the lowest voltage level. After irradiation, if there is a TID-induced leakage current in each reset transistor, the total number of 128×1024 reset transistors in the whole pixel array could draw a large current from the power supply which can be detected in the power supply instrument. In addition, the current source in each column line is programmed to be zero to avoid the TID effects from row select transistors.

The second test checks whether the TID effect make the row select switch hard to turn off. In the rolling shutter mode, the proposed CIS prototype selects four rows of pixels at a time to start the pixel readout operation. If the row select switches are affected by the TID, they are either turned on at the wrong time, or worse, remain on constantly. The testing method involves turning on the reset transistors permanently and turning off the transfer gates and row select switches. Under conditions of no light, the pixel array should consume a constant power supply. After irradiation, if there is a TID-induced leakage current in each row select transistor, the total number of $128 \times 4 = 512$ column lines in the whole pixel array could show a current flowing. Also, the current source in each column line is programmed to be 20 μA.

The test results are shown in Figure 5.28. The current drawn from the 3.3 V power supply in both tests has almost remained unchanged in the TID dose, varying from 1 $krad(SiO_2)$ to 125 $krad(SiO_2)$. During every electrical testing, the globalTX signal - which turns on all transfer gates in the pixel array - could be detected in the debug multiplexer output, which means the sequencer was working properly under the radiation environment. Furthermore, after finishing the radiation test, the DUT can operate normally to detect the correct fixed-pattern test in the lab during the 24-hour annealing period.

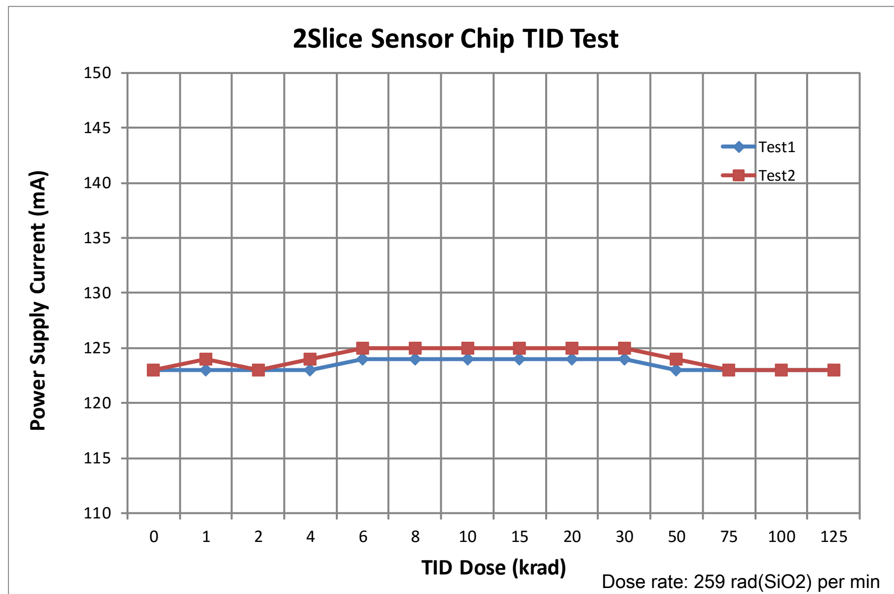


Figure 5.28: TID test results

Chapter 6

Conclusions and Future Work

6.1 Conclusions

This dissertation proposed the design of a novel high-speed CMOS image sensor architecture for a radhard mega-pixel array. Without using the 3D-stack method or other costly techniques, the camera-on-a-chip (COC) architecture developed an innovative quadruple column-parallel readout (QCPRO) scheme to use a standard 0.18 μm CMOS process to achieve over $10,000$ fps frame rate in one million pixel array. For medical and scientific applications, the proposed CIS also developed a radhard pixel cell by using the physical design techniques of enclosed geometry and P-type guardrings. The additional programmable feature of the frame rate further extends the applications of the proposed CIS camera. Furthermore, the dissertation described the development of the entire CMOS camera system and measurement methods to test the system.

Two CIS prototypes with a 20 μm-pitch radhard 4T pixel architecture were designed, laid out, and fabricated using a 180 nm CIS process. They use the same proposed high-speed architecture and enable to provide complete digital input control and digital pixel data. The sensor architecture is symmetrical and is divided into two functionally independent blocks with two identical sets of pins for the top and bottom halves. The power and control signals were duplicated for both top and bottom readout circuitry. Several techniques, such as time interleaving, quadruple parallel reading, and digital ping-pong data storing, were used to maximize the CMOS imager's frame rate. Moreover, the proposed CIS camera used radiation-hardening-by-design (RHBD) techniques to improve its TID tolerance.

Separate power supplies were used for each block inside the chip, and power supplies with three different primary voltage values were used in the sensor. The 3.3 V power supply is used by the thick-oxide MOSFETs in the pixel array and row buffers. The 1.8 V power supply is used by the peripheral circuits including sequencer block, row decoders, readout chain, and PLLs. In contrast, the 0.4 V power supply is only used by the SLVS drivers. All subcircuit blocks including sequencer, row decoders, amplifiers, PLLs, and SLVS I/Os were designed, simulated, laid out, and most importantly validated by the silicon testing results. The column readout circuitry is well designed in a pixel pitch that achieves a fast-parallel readout process. The

scheme was clarified by the noise analysis of the proposed readout chain.

Spatial distortion is a significant concern since the CIS is operated at the rolling shutter. Fortunately, the CIS architecture mitigates distortion by reading out four rows of pixels at each line time. Also, the distortion is less likely when relatively small objects are moving at a rate that is being over-sampled by a high frame rate.

Customized camera hardware system with commercial off-the-shelf (COTS) FPGA, AD/DA converters, power manager and oscillator ICs were designed, while seven different PCB boards were developed and fabricated. The complex firmware design was developed with radhard test consideration. Different communication protocols were involved in the firmware development process, including camera link, SPI, and UART. The small-format CIS prototype was validated by the results of the measurements. The CIS prototype with 128×1024 pixels has been shown to have a programmable frame rate from 20 fps to $4,000$ fps for a broad range of applications including high frame rate and long exposure time. The functionalities of the sequencer and PLLs were validated by operating the clock frequency ranging from 20 MHz to 125 MHz. Furthermore, the TID radiation test with biased condition illustrated the CIS working properly up to 125 $krad(SiO_2)$ total dose level.

6.2 Future Work

High-speed CISs with radiation hardness are becoming necessary in various scientific applications. In order to better characterize the small-format CIS chip, an optimized testing boards will be fabricated and fewer bondwires will be connected to the CIS daughterboard in order to keep the COB service from shorting issues in adjacent pads. The pixel testing structure will be activated to characterize the pixel performance. Meanwhile, an interposer board will be designed to connect the CIS daughter board to the Xilinx Spartan-6 FPGA SP605 evaluation board through an FMC-LPC expansion connector. The data recovery and de-serializer blocks will be developed in Xilinx FPGA and the captured images will be displayed on the screen through a DIV or VGA connector. The standard EMVA 1288 will be used to measure and present the specifications for the proposed camera system.

Furthermore, the proposed CIS architecture has plenty of room for optimization. The innovations can be made in different aspects:

- Initially, the number of pads need to be reduced. These two CIS prototypes have 754 and 1,114 pads, respectively. No standard package would currently meet this requirement. Although the COB technique can bond wires to connect to the bare sensor die on FR4 substrate, a great deal of pad number and small pad pitch make the PCB assembly service costly and challenging. Therefore, the next spin will begin by focusing on choosing a standard package such as PGA with less than 400 pins to limit the padring.

- The ADC number is another important concern. Four ADCs per column required a 10 μm layout pitch to make the ADC suitable for the proposed high-speed CIS architecture. However, this layout pitch also limits the performance of a single ADC. One solution is to add more parallel analog front-end blocks to achieve multiple sampling operations. Another solution is to implement several redundant cycles in the SAR ADCs to increase the SNR without increasing the layout area. The third one is to use a different type of ADC, such as the single-slope or multi-slope ADC architecture, for a better trade-off between the number of ADCs and their conversion speed.

- Finally, the radhard pixel can be optimized for improving radiation tolerance. For example, the peripheral of the PPD can be covered by the field-gate, which was proven to be useful for reducing the TID effect in photodiodes. In addition, the 4T pixel can be replaced by 5T pixel to implement global shutter and rolling shutter operations in the same CIS chip for more applications.

Bibliography

[1] J. Nakamura, *Image sensors and signal processing for digital still cameras.* CRC press, 2016.

[2] M. Technology, "The evolution of digital imaging: From ccd to cmos - a micron white paper," 2006.

[3] A. W. Harzing, "Publish or perish." available from https://harzing.com/resources/publish-or-perish.

[4] E. R. Fossum, "Active pixel sensors - are ccd's dinosaurs," 1993.

[5] E. R. Fossum, "CMOS image sensors: electronic camera-on-a-chip," *IEEE Transactions on Electron Devices*, vol. 44, pp. 1689–1698, Oct. 1997.

[6] Y. Oike, K. Akiyama, L. D. Hung, W. Niitsuma, A. Kato, M. Sato, Y. Kato, W. Nakamura, H. Shiroshita, Y. Sakano, Y. Kitano, T. Nakamura, T. Toyama, H. Iwamoto, and T. Ezaki, "8.3 m-pixel 480-fps global-shutter cmos image sensor with gain-adaptive column adcs and chip-on-chip stacked integration," *IEEE Journal of Solid-State Circuits*, vol. 52, pp. 985–993, April 2017.

[7] T. Takahashi, Y. Kaji, Y. Tsukuda, S. Futami, K. Hanzawa, T. Yamauchi, P. W. Wong, F. Brady, P. Holden, T. Ayers, K. Mizuta, S. Ohki, K. Tatani, T. Nagano, H. Wakabayashi, and Y. Nitta, "A 4.1mpix 280fps stacked CMOS image sensor with array-parallel ADC architecture for region control," in *Proc. Symp. VLSI Circuits*, pp. C244–C245, June 2017.

[8] T. Arai, T. Yasue, K. Kitamura, H. Shimamoto, T. Kosugi, S. Jun, S. Aoyama, M. C. Hsu, Y. Yamashita, H. Sumi, and S. Kawahito, "A 1.1um 33mpixel 240fps 3D-stacked CMOS image sensor with 3-stage cyclic-based analog-to-digital converters," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, pp. 126–128, Jan. 2016.

[9] K. Akiyama, Y. Oike, Y. Kitano, J. Fjimagari, W. Satoru, Y. Sakano, T. Toyama, H. Iwamoto, T. Ezaki, T. Nakamura, T. Imaizumi, and N. Yasuhiro, "A front-illuminated stacked global-shutter cmos image sensor with multiple chip-on-chip integration," in *Proc. IEEE Int. 3D Systems Integration Conf. (3DIC)*, pp. 1–3, Nov. 2016.

[10] OnSemiconductor, "Lupa3000,3megapixel high speed cmos image sensor," tech. rep., OnSemiconductor, 2016.

[11] S. Okura, O. Nishikido, Y. Sadanaga, Y. Kosaka, N. Araki, K. Ueda, and F. Morishita, "A 3.7 m-pixel 1300-fps cmos image sensor with 5.0 g-pixel/s high-speed readout circuit.," *J. Solid-State Circuits*, vol. 50, no. 4, pp. 1016–1024, 2015.

[12] D. Kim, J. Bae, and M. Song, "A high speed cmos image sensor with a novel digital correlated double sampling and a differential difference amplifier," *Sensors*, vol. 15, no. 3, pp. 5081–5095, 2015.

[13] Y. Zhou, Z. Cao, Y. Han, Q. Li, C. Shi, R. Dou, Q. Qin, J. Liu, and N. Wu, "A low power global shutter pixel with extended fd voltage swing range for large format high speed cmos image sensor," *Science China Information Sciences*, vol. 58, no. 4, pp. 1–10, 2015.

[14] S. Machida, S. Shishido, T. Tokuhara, M. Yanagida, T. Yamada, M. Izuchi, Y. Sato, Y. Miyake, M. Nakata, M. Murakami, M. Harada, and Y. Inoue, "A 2.1-mpixel organic film-stacked rgb-IR image sensor with electrically controllable IR sensitivity," *IEEE Journal of Solid-State Circuits*, vol. 53, pp. 229–235, Jan. 2018.

[15] A. Suzuki, N. Shimamura, T. Kainuma, N. Kawazu, C. Okada, T. Oka, K. Koiso, A. Masagaki, Y. Yagasaki, S. Gonoi, T. Ichikawa, M. Mizuno, T. Sugioka, T. Morikawa, Y. Inada, and H. Wakabayashi, "A 1/1.7-inch 20mpixel back-illuminated stacked CMOS image sensor for new imaging applications," in *Proc. IEEE Int. Solid-State Circuits Conf. - (ISSCC) Digest of Technical Papers*, pp. 1–3, Feb. 2015.

[16] R. Funatsu, S. Huang, T. Yamashita, K. Stevulak, J. Rysinski, D. Estrada, S. Yan, T. Soeno, T. Nakamura, T. Hayashida, H. Shimamoto, and B. Mansoorian, "133mpixel 60fps CMOS image sensor with 32-column shared high-speed column-parallel SAR adcs," in *Proc. IEEE Int. Solid-State Circuits Conf. - (ISSCC) Digest of Technical Papers*, pp. 1–3, Feb. 2015.

[17] C. S. Hong, K. Palle, T. Bao, V. Wang, Y. Fong, W. Choi, K.-B. Cho, and R. Panicacci, "High-speed, high sensitivity 25 mega pixel cmos image sensor with column parallel 12 bit hybrid adc architecture," *2015 International Image Sensor Workshop*, 2015.

[18] T. Geurts, T. Cools, C. Esquenet, R. Sankhe, A. Prathipati, M. R. E. Syam, A. B. Dayalu, V. P. R. Gaddam, and O. Semiconductor, "A 25 mpixel, 80 fps, cmos imager with an in-pixel-cds global shutter pixel," in *Int. Image Sensor Workshop (IISW)*, 2015.

[19] I. Insights, "Cmos image sensors sales stay on record-breaking pace," resreport, IC Insights, Inc., 05 2018.

[20] Y. Tochigi, K. Hanzawa, Y. Kato, R. Kuroda, H. Mutoh, R. Hirose, H. Tominaga, K. Takubo, Y. Kondo, and S. Sugawa, "A global-shutter CMOS image sensor with readout speed of 1-Tpixel/s burst and 780-mpixel/s continuous," *IEEE Journal of Solid-State Circuits*, vol. 48, pp. 329–338, Jan. 2013.

[21] B. Cremers, M. Innocent, C. Luypaert, J. Compiet, I. C. Mudegowdar, C. Esquenet, G. Chapinal, W. Vroom, T. Blanchaert, T. Cools, *et al.*, "A 5 megapixel, 1000 fps cmos image sensor with high dynamic range and 14-bit a/d converters," in *2013 Int. Image Sensor Workshop*, 2013.

[22] R. Xu, B. Liu, and J. Yuan, "A 1500 fps highly sensitive 256 ,*times*,256 CMOS imaging sensor with in-pixel calibration," *IEEE Journal of Solid-State Circuits*, vol. 47, pp. 1408–1418, June 2012.

[23] T. Watabe, K. Kitamura, T. Sawamoto, T. Kosugi, T. Akahori, T. Iida, K. Isobe, T. Watanabe, H. Shimamoto, H. Ohtake, *et al.*, "A 33mpixel 120fps cmos image sensor using 12b column-parallel pipelined cyclic adcs," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, pp. 388–390, IEEE, 2012.

[24] J. Bogaerts, "High speed 36 gbps 12 mpixel global pipelined shutter cmos image sensor withcds," in *Proc. 2011 International Image Sensor Workshop*, pp. 335–338, 2011.

[25] Y. Chae, J. Cheon, S. Lim, M. Kwon, K. Yoo, W. Jung, D.-H. Lee, S. Ham, and G. Han, "A 2.1 m pixels, 120 frame/s cmos image sensor with column-parallel delta-sigma adc architecture," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 1, pp. 236–247, 2011.

[26] T. Toyama, K. Mishina, H. Tsuchiya, T. Ichikawa, H. Iwaki, Y. Gendai, H. Murakami, K. Takamiya, H. Shiroshita, Y. Muramatsu, *et al.*, "A 17.7 mpixel 120fps cmos image sensor with 34.8 gb/s readout," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International*, pp. 420–422, IEEE, 2011.

[27] S. Lim, J. Lee, D. Kim, and G. Han, "A high-speed cmos image sensor with column-parallel two-step single-slope adcs," *IEEE Transactions on Electron Devices*, vol. 56, pp. 393–398, Mar. 2009.

[28] G. Meynants, G. Lepage, J. Bogaerts, G. Vanhorebeek, and X. Wang, "Limitations to the frame rate of high speed image sensors," in *Proc. Int. Image Sensor Workshop*, pp. 153–156, 2009.

[29] B. Cremers, M. Agarwal, T. Walschap, R. Singh, and T. Geurts, "A high speed pipelined snapshot cmos image sensor with 6.4 gpixel/s data rate," in *Proc. 2009 International Image Sensor Workshop P*, vol. 9, 2009.

[30] M. Furuta, Y. Nishikawa, T. Inoue, and S. Kawahito, "A high-speed, high-sensitivity digital cmos image sensor with a global shutter and 12-bit column-parallel cyclic a/d converters," *IEEE Journal of Solid-State Circuits*, vol. 42, pp. 766–774, Apr. 2007.

[31] Y. Nishikawa, S. Kawahito, M. Furuta, and T. Tamura, "A high-speed cmos image sensor with on-chip parallel image compression circuits," in *Proc. IEEE Custom Integrated Circuits Conf*, pp. 833–836, Sept. 2007.

[32] A. I. Krymski and N. Tu, "A 9-V/lux-s 5000-frames/s 512 x 512 cmos sensor," *IEEE Transactions on Electron Devices*, vol. 50, pp. 136–143, Jan. 2003.

[33] S. Lauxtermann, G. Israel, P. Seitz, H. Bloss, J. Ernst, H. Firla, and S. Gick, "A mega-pixel high speed cmos imager with sustainable gigapixel/sec readout rate," in *IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, 2001.

[34] S. Kleinfelder, S. Lim, X. Liu, and A. El Gamal, "A 10000 frames/s cmos digital pixel sensor," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 12, pp. 2049–2059, 2001.

[35] N. Stevanovic, M. Hillebrand, B. J. Hosticka, and A. Teuner, "A cmos image sensor for high-speed imaging," in *Proc. IEEE Int. Solid-State Circuits Conf.. Digest of Technical Papers*, pp. 104–105, Feb. 2000.

[36] A. Krymski, D. V. Blerkom, A. Andersson, N. Bock, B. Mansoorian, and E. R. Fossum, "A high speed, 500 frames/s, 1024×1024 CMOS active pixel sensor," in *Proc. Symp. VLSI Circuits. Digest of Papers (IEEE Cat. No.99CH36326)*, pp. 137–138, June 1999.

[37] N. Stevanovic, M. Hillebrand, B. J. Hosticka, U. Iurgel, and A. Teuner, "A high speed camera system based on an image sensor in standard CMOS technology," in *Proc. IEEE Int. Symp. Circuits and Systems ISCAS '99*, vol. 5, pp. 148–151 vol.5, 1999.

[38] G. Yang, O. Yadid-Pecht, C. Wrigley, and B. Pain, "A snap-shot cmos active pixel imager for low-noise, high-speed imaging," in *Electron Devices Meeting, 1998. IEDM'98. Technical Digest., International*, pp. 45–48, IEEE, 1998.

[39] C. H. Aw and B. Wooley, "A 128/spl times/128-pixel standard-cmos image sensor with electronic shutter," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 12, pp. 1922–1930, 1996.

[40] S.-F. Yeh, K.-Y. Chou, H.-Y. Tu, C. Y.-P. Chao, and F.-L. Hsueh, "A 0.66 e rms- temporal-readout-noise 3-d-stacked cmos image sensor with conditional correlated multiple sampling technique," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 2, pp. 527–537, 2018.

[41] T. Takahashi, Y. Kaji, Y. Tsukuda, S. Futami, K. Hanzawa, T. Yamauchi, P. W. Wong, F. T. Brady, P. Holden, T. Ayers, *et al.*, "A stacked cmos image sensor with array-parallel adc architecture," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 4, pp. 1061–1070, 2018.

[42] O. Kumagai, A. Niwa, K. Hanzawa, H. Kato, S. Futami, T. Ohyama, T. Imoto, M. Nakamizo, H. Murakami, T. Nishino, *et al.*, "A 1/4-inch 3.9 mpixel low-power event-driven back-illuminated stacked cmos image sensor," in *Solid-State Circuits Conference-(ISSCC), 2018 IEEE International*, pp. 86–88, IEEE, 2018.

[43] P.-S. Chou, C.-H. Chang, M. M. Mhala, C. C.-M. Liu, C. Y.-P. Chao, C.-Y. Huang, H. Tu, T. Wu, S.-F. Yeh, S. Takahashi, *et al.*, "A 1.1 μm-pitch 13.5 mpixel 3d-stacked cmos image sensor featuring 230fps full-high-definition and 514fps high-definition videos by reading 2 or 3 rows simultaneously using a column-switching matrix," in *Solid-State Circuits Conference-(ISSCC), 2018 IEEE International*, pp. 88–90, IEEE, 2018.

[44] S.-H. Kim, H. Shin, Y. Jeong, J.-H. Lee, J. Choi, and J.-H. Chun, "A 12-gb/s stacked dual-channel interface for cmos image sensor systems," *Sensors*, vol. 18, no. 8, p. 2709, 2018.

[45] Y. Kim, W. Choi, D. Park, H. Jeoung, B. Kim, Y. Oh, S. Oh, B. Park, E. Kim, Y. Lee, *et al.*, "A 1/2.8-inch 24mpixel cmos image sensor with 0.9 μm unit pixels separated by full-depth deep-trench isolation," in *Solid-State Circuits Conference-(ISSCC), 2018 IEEE International*, pp. 84–86, IEEE, 2018.

[46] T. Haruta, T. Nakajima, J. Hashizume, T. Umebayashi, H. Takahashi, K. Taniguchi, M. Kuroda, H. Sumihiro, K. Enoki, T. Yamasaki, *et al.*, "4.6 a 1/2.3 inch 20mpixel 3-layer stacked cmos image sensor with dram," in *Solid-State Circuits Conference (ISSCC), 2017 IEEE International*, pp. 76–77, IEEE, 2017.

[47] M. Sakakibara, K. Ogawa, S. Sakai, Y. Tochigi, K. Honda, H. Kikuchi, T. Wada, Y. Kamikubo, T. Miura, M. Nakamizo, *et al.*, "A 6.9-μm pixel-pitch back-illuminated global shutter cmos image sensor with pixel-parallel 14-bit subthreshold adc," *IEEE Journal of Solid-State Circuits*, no. 99, pp. 1–9, 2018.

[48] T. G. Etoh, V. T. S. Dao, K. Shimonomura, E. Charbon, C. Zhang, Y. Kamakura, and T. Matsuoka, "Toward 1gfps: Evolution of ultra-high-speed image sensors -isis, bsi, multi-collection gates, and 3D-stacking-," in *Proc. IEEE Int. Electron Devices Meeting*, pp. 10.3.1–10.3.4, Dec. 2014.

[49] Y. Zhou, Z. Cao, Q. Qin, Q. Li, C. Shi, and N. Wu, "A high speed 1000 fps cmos image sensor with low noise global shutter pixels," *Science China Information Sciences*, vol. 57, no. 4, pp. 1–8, 2014.

[50] A. I. Krymski, N. E. Bock, N. Tu, D. V. Blerkom, and E. R. Fossum, "A high-speed, 240-frames/s, 4.1-mpixel CMOS sensor," *IEEE Transactions on Electron Devices*, vol. 50, pp. 130–135, Jan. 2003.

[51] A. El Gamal, D. X. Yang, and B. A. Fowler, "Pixel-level processing: why, what, and how?," in *Sensors, Cameras, and Applications for Digital Photography*, vol. 3650, pp. 2–14, International Society for Optics and Photonics, 1999.

[52] Y. Kagawa, N. Fujii, K. Aoyagi, Y. Kobayashi, S. Nishi, N. Todaka, S. Takeshita, J. Taura, H. Takahashi, Y. Nishimura, *et al.*, "Novel stacked cmos image sensor with advanced cu2cu hybrid bonding," in *Electron Devices Meeting (IEDM), 2016 IEEE International*, pp. 8–4, IEEE, 2016.

[53] K. Nishimura, S. Shishido, Y. Miyake, M. Yanagida, Y. Satou, M. Shouho, H. Kanehara, R. Sakaida, Y. Sato, J. Hirase, *et al.*, "An 8k4k-resolution 60fps 450ke–saturation-signal organic-photoconductive-film global-shutter cmos image sensor with in-pixel noise canceller," in *Solid-State Circuits Conference-(ISSCC), 2018 IEEE International*, pp. 82–84, IEEE, 2018.

[54] S.-I. Hwang, J.-H. Chung, H.-J. Kim, I.-H. Jang, M.-J. Seo, S.-H. Cho, H. Kang, M. Kwon, and S.-T. Ryu, "A 2.7-m pixels 64-mw cmos image sensor with multicolumn-parallel noise-shaping sar adcs," *IEEE Transactions on Electron Devices*, vol. 65, no. 3, pp. 1119–1126, 2018.

[55] M. Kobayashi, Y. Onuki, K. Kawabata, H. Sekine, T. Tsuboi, Y. Matsuno, H. Takahashi, T. Koizumi, K. Sakurai, H. Yuzurihara, *et al.*, "4.5 a 1.8 e rms- temporal noise over 110db dynamic range 3.4 μm pixel pitch global shutter cmos image sensor with dual-gain amplifiers, ss-adc and multiple-accumulation shutter," in *Solid-State Circuits Conference (ISSCC), 2017 IEEE International*, pp. 74–75, IEEE, 2017.

[56] K. Yasutomi, M. Seo, M. Kamoto, N. Teranishi, and S. Kawahito, "A 0.61 e-noise global shutter cmos image sensor with two-stage charge transfer pixels," in *VLSI Circuits, 2017 Symposium on*, pp. C248–C249, IEEE, 2017.

[57] C. Ma, Y. Liu, Y. Li, Q. Zhou, X. Wang, and Y. Chang, "A 4-m pixel high dynamic range, low-noise cmos image sensor with low-power counting adc," *IEEE Transactions on Electron Devices*, vol. 64, no. 8, pp. 3199–3205, 2017.

[58] K. Kawabata, M. Kobayashi, Y. Onuki, H. Sekine, T. Tsuboi, Y. Matsuno, H. Takahashi, S. Inoue, and T. Ichikawa, "A 1.8 e- temporal noise over 90db dynamic range 4k2k super 35mm format seamless global shutter cmos image sensor with multiple accumulation shutter technology," in *Electron Devices Meeting (IEDM), 2016 IEEE International*, pp. 8–6, IEEE, 2016.

[59] H. Totsuka, T. Tsuboi, T. Muto, D. Yoshida, Y. Matsuno, M. Ohmura, H. Takahashi, K. Sakurai, T. Ichikawa, H. Yuzurihara, *et al.*, "An aps-h-size 250mpixel cmos image sensor using column single-slope adcs with dual-gain amplifiers," in *Solid-State Circuits Conference (ISSCC), 2016 IEEE International*, pp. 116–117, IEEE, 2016.

[60] T. Kondo, N. Takazawa, Y. Takemoto, M. Tsukimura, H. Saito, H. Kato, J. Aoki, K. Kobayashi, S. Suzuki, Y. Gomi, *et al.*, "3-d-stacked 16-mpixel global shutter cmos image sensor using reliable in-pixel four million microbump interconnections with 7.6-um pitch," *IEEE Transactions on Electron Devices*, vol. 63, no. 1, pp. 128–137, 2016.

[61] J. Bogaerts, R. Lafaille, M. Borremans, J. Guo, B. Ceulemans, G. Meynants, N. Sarhangnejad, G. Arsinte, V. Statescu, and S. van der Groen, "105× 65mm2 391mpixel cmos image sensor with¿ 78db

dynamic range for airborne mapping applications," in *Solid-State Circuits Conference (ISSCC), 2016 IEEE International*, pp. 114–115, IEEE, 2016.

[62] C. C.-M. Liu, M. M. Mhala, C.-H. Chang, H. Tu, P.-S. Chou, C. Chao, and F.-L. Hsueh, "A 1.5 v 33mpixel 3d-stacked cmos image sensor with negative substrate bias," in *Solid-State Circuits Conference (ISSCC), 2016 IEEE International*, pp. 124–125, IEEE, 2016.

[63] S. Shishido, Y. Miyake, Y. Sato, T. Tamaki, N. Shimasaki, Y. Sato, M. Murakami, and Y. Inoue, "210ke- saturation signal 3μm-pixel variable-sensitivity global-shutter organic photoconductive image sensor for motion capture," in *Solid-State Circuits Conference (ISSCC), 2016 IEEE International*, pp. 112–113, IEEE, 2016.

[64] S. Sukegawa, T. Umebayashi, T. Nakajima, H. Kawanobe, K. Koseki, I. Hirota, T. Haruta, M. Kasai, K. Fukumoto, T. Wakano, K. Inoue, H. Takahashi, T. Nagano, Y. Nitta, T. Hirayama, and N. Fukushima, "A 1/4-inch 8mpixel back-illuminated stacked CMOS image sensor," in *Proc. IEEE Int. Solid-State Circuits Conf. Digest of Technical Papers*, pp. 484–485, Feb. 2013.

[65] H. Honda, S. Osawa, M. Shoda, E. Pages, T. Sato, N. Karasawa, B. Leichner, J. Schoper, E. S. Gattuso, D. Pates, J. Brooks, S. Johnson, and I. Takayanagi, "A 1-inch optical format, 14.2m-pixel, 80fps CMOS image sensor with a pipelined pixel reset and readout operation," in *Proc. Symp. VLSI Circuits*, pp. C4–C5, June 2013.

[66] K. Kitamura, T. Watabe, T. Sawamoto, T. Kosugi, T. Akahori, T. Iida, K. Isobe, T. Watanabe, H. Shimamoto, H. Ohtake, S. Aoyama, S. Kawahito, and N. Egami, "A 33-megapixel 120-Frames-per-second 2.5-Watt CMOS image sensor with column-parallel two-stage cyclic analog-to-digital converters," *IEEE Transactions on Electron Devices*, vol. 59, pp. 3426–3433, Dec. 2012.

[67] T. Toyama, K. Mishina, H. Tsuchiya, T. Ichikawa, H. Iwaki, Y. Gendai, H. Murakami, K. Takamiya, H. Shiroshita, Y. Muramatsu, and T. Furusawa, "A 17.7mpixel 120fps CMOS image sensor with 34.8Gb/s readout," in *Proc. IEEE Int. Solid-State Circuits Conf*, pp. 420–422, Feb. 2011.

[68] S. Lim, J. Cheon, Y. Chae, W. Jung, D. H. Lee, M. Kwon, K. Yoo, S. Ham, and G. Han, "A 240-frames/s 2.1-mpixel cmos image sensor with column-shared cyclic adcs," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 2073–2083, Sept. 2011.

[69] C. Esquenet, J. Compiet, T. Blanchaert, T. Geurts, and J. Decupere, "A 26.2 mpixel, 74fps, global shutter cmos imager with 20gb/s interface for multi object monitoring," in *Proc. 2011 International Image Sensor Workshop*, pp. 332–334, 2011.

[70] Y. Chae, J. Cheon, S. Lim, D. Lee, M. Kwon, K. Yoo, W. Jung, D. H. Lee, S. Ham, and G. Han, "A 2.1mpixel 120frame/s CMOS image sensor with column-parallel $\Delta\ \Sigma$ ADC architecture," in *Proc. IEEE Int. Solid-State Circuits Conf. - (ISSCC)*, pp. 394–395, Feb. 2010.

[71] H. Wakabayashi, K. Yamaguchi, M. Okano, S. Kuramochi, O. Kumagai, S. Sakane, M. Ito, M. Hatano, M. Kikuchi, Y. Yamagata, *et al.*, "A 1/2.3-inch 10.3 mpixel 50frame/s back-illuminated cmos image sensor," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*, pp. 410–411, IEEE, 2010.

[72] S. Matsuo, T. J. Bales, M. Shoda, S. Osawa, K. Kawamura, A. Andersson, M. Haque, H. Honda, B. Almond, Y. Mo, J. Gleason, T. Chow, and I. Takayanagi, "8.9-megapixel video image sensor with 14-b column-parallel sa-ADC," *IEEE Transactions on Electron Devices*, vol. 56, pp. 2380–2389, Nov. 2009.

[73] K. B. Cho, C. Lee, S. Eikedal, A. Baum, J. Jiang, C. Xu, X. Fan, and R. Kauffman, "A 1/2.5 inch 8.1mpixel CMOS image sensor for digital cameras," in *Proc. IEEE Int. Solid-State Circuits Conf.. Digest of Technical Papers*, pp. 508–618, Feb. 2007.

[74] S. Yoshihara, Y. Nitta, M. Kikuchi, K. Koseki, Y. Ito, Y. Inada, S. Kuramochi, H. Wakabayashi, M. Okano, H. Kuriyama, J. Inutsuka, A. Tajima, T. Nakajima, Y. Kudoh, F. Koga, Y. Kasagi, S. Watanabe, and T. Nomoto, "A 1/1.8-inch 6.4 mpixel 60 frames/s CMOS image sensor with seamless mode change," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 2998–3006, Dec. 2006.

[75] I. Takayanagi, M. Shirakawa, K. Mitani, M. Sugawara, S. Iversen, J. Moholt, J. Nakamura, and E. R. Fossum, "A 1.25-inch 60-frames/s 8.3-m-pixel digital-output CMOS image sensor," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 2305–2314, Nov. 2005.

[76] M. Mori, M. Katsuno, S. Kasuga, T. Murata, and T. Yamaguchi, "1/4-inch 2-mpixel MOS image sensor with 1.75 transistors/pixel," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 2426–2430, Dec. 2004.

[77] B. Mansoorian, H.-Y. Yee, S. Huang, and E. Fossum, "A 250 mW, 60 frames/s 1280×720 pixel 9 b CMOS digital image sensor," in *Proc. IEEE Int. Solid-State Circuits Conf.. Digest of Technical Papers. ISSCC. First Edition (Cat. No.99CH36278)*, pp. 312–313, Feb. 1999.

[78] Wikipedia contributors, "Band gap — Wikipedia, the free encyclopedia," 2018. [Online; accessed 4-December-2018].

[79] O. Yadid-Pecht and R. Etienne-Cummings, *CMOS imagers: from phototransduction to image processing*. Springer Science & Business Media, 2007.

[80] A. Theuwissen, "CMOS image sensors: State-of-the-art and future perspectives," in *Proc. ESSDERC 2007 - 37th European Solid State Device Research Conf*, pp. 21–27, Sept. 2007.

[81] A. Boukhayma, *Ultra Low Noise CMOS Image Sensors*. PhD thesis, Ecole polytechnique fédérale de Lausanne (EPFL), 2016.

[82] E. R. Fossum, D. B. Hondongwa, *et al.*, "A review of the pinned photodiode for ccd and cmos image sensors," *IEEE J. Electron Devices Soc.*, vol. 2, no. 3, pp. 33–43, 2014.

[83] X. Li, *MOSFET Modulated Dual Conversion Gain CMOS Image Sensors.* PhD thesis, Biose State University, 2008.

[84] E. R. Fossum *et al.*, "Charge transfer noise and lag in cmos active pixel sensors," in *Proc. 2003 IEEE Workshop on CCDs and Advanced Image Sensors, Elmau, Bavaria, Germany*, pp. 11–13, Citeseer, 2003.

[85] N. B. Zurich, "Ccd versus cmos–has ccd imaging come to an end?," 2001.

[86] J. S. Lee, R. I. Hornsey, and D. Renshaw, "Analysis of cmos photodiodes. i. quantum efficiency," *IEEE Transactions on Electron Devices*, vol. 50, no. 5, pp. 1233–1238, 2003.

[87] J. S. Lee, R. I. Hornsey, and D. Renshaw, "Analysis of cmos photodiodes. ii. lateral photoresponse," *IEEE Transactions on electron Devices*, vol. 50, no. 5, pp. 1239–1245, 2003.

[88] A. Pelamatti, V. Goiffon, M. Estribeau, P. Cervantes, and P. Magnan, "Estimation and modeling of the full well capacity in pinned photodiode cmos image sensors," *IEEE Electron Device Letters*, vol. 34, no. 7, pp. 900–902, 2013.

[89] S. Yu, Z. Ping, X. Jiangtao, G. Zhiyuan, and X. Chao, "Full well capacity and quantum efficiency optimization for small size backside illuminated cmos image pixels with a new photodiode structure," *Journal of Semiconductors*, vol. 33, no. 12, p. 124006, 2012.

[90] R. I. Hornsey, "noise in image sensors." course notes, 2010.

[91] H. Liqiang, Y. Suying, X. Jiangtao, X. Chao, and G. Zhiyuan, "Analysis of incomplete charge transfer effects in a cmos image sensor," *Journal of Semiconductors*, vol. 34, no. 5, p. 054009, 2013.

[92] L.-E. Bonjour, N. Blanc, and M. Kayal, "Experimental analysis of lag sources in pinned photodiodes," *IEEE electron device letters*, vol. 33, no. 12, pp. 1735–1737, 2012.

[93] J. R. Janesick, *Photon transfer.* SPIE press San Jose, 2007.

[94] A. Boukhayma, A. Peizerat, and C. Enz, "Temporal readout noise analysis and reduction techniques for low-light cmos image sensors," *IEEE Transactions on Electron Devices*, vol. 63, no. 1, pp. 72–78, 2016.

[95] D. Gardner, "Characterizing digital cameras with the photon transfer curve," *Summit imaging (undated document supplied by Jake Beverage)*, 2012.

[96] D. McGrath, S. Tobin, V. Goiffon, P. Magnan, and A. Le Roch, "Dark current limiting mechanisms in cmos image sensors," *Electronic Imaging*, vol. 2018, no. 11, pp. 354–1, 2018.

[97] L. Mutuel, "Single event effects mitigation techniques report," *Federal Aviation Administration, William J. Hughes Technical Center, Aviation Research Division, Atlantic City International Airport, Final report DOT/FAA/TC-15/62*, 2016.

[98] D. Munteanu and J.-L. Autran, "Modeling and simulation of single-event effects in digital devices and ics," *IEEE Transactions on Nuclear science*, vol. 55, no. 4, pp. 1854–1878, 2008.

[99] E. C. Auden, *Heavy ion-induced single particle displacement damage in silicon.* Vanderbilt University, 2013.

[100] J. R. Srour and J. M. McGarrity, "Radiation effects on microelectronics in space," *Proceedings of the IEEE*, vol. 76, no. 11, pp. 1443–1469, 1988.

[101] F. B. McLean and T. R. Oldham, "Basic mechanisms of radiation effects in electronic materials and devices," tech. rep., HARRY DIAMOND LABS ADELPHI MD, 1987.

[102] T. R. Oldham, "Basic mechanisms of tid and ddd response in mos and bipolar microelectronics," *NSREC Short Course*, 2011.

[103] T. Oldham, "Analysis of damage in mos devices for several radiation environments," *IEEE Transactions on Nuclear Science*, vol. 31, no. 6, pp. 1236–1241, 1984.

[104] J. R. Schwank, M. R. Shaneyfelt, D. M. Fleetwood, J. A. Felix, P. E. Dodd, P. Paillet, and V. Ferlet-Cavrois, "Radiation effects in mos oxides," *IEEE Transactions on Nuclear Science*, vol. 55, no. 4, pp. 1833–1853, 2008.

[105] R. Lacoe *et al.*, "Cmos scaling design principles and hardening-by-design methodologies," in *IEEE NSREC Short Course*, 2003.

[106] T. R. Oldham, *Ionizing radiation effects in MOS oxides.* World Scientific, 1999.

[107] H. Barnaby, "Total-ionizing-dose effects in modern cmos technologies," *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3103–3121, 2006.

[108] M. Shaneyfelt, D. Fleetwood, J. Schwank, and K. Hughes, "Charge yield for cobalt-60 and 10-kev x-ray irradiations of mos devices," *IEEE transactions on nuclear science*, vol. 38, no. 6, pp. 1187–1194, 1991.

[109] S. Manzini and A. Modelli, "Tunneling discharge of trapped holes in silicon dioxide," in *Insulating Films on Semiconductors*, pp. 112–115, Elsevier, 1983.

[110] M. Schmidt and H. Köster Jr, "Hole trap analysis in sio2/si structures by electron tunneling," *physica status solidi (b)*, vol. 174, no. 1, pp. 53–66, 1992.

[111] P. McWhorter, S. Miller, and W. Miller, "Modeling the anneal of radiation-induced trapped holes in a varying thermal environment," *IEEE Transactions on Nuclear Science*, vol. 37, no. 6, pp. 1682–1689, 1990.

[112] T. Oldham, A. Lelis, and F. McLean, "Spatial dependence of trapped holes determined from tunneling analysis and measured annealing," *IEEE Transactions on Nuclear Science*, vol. 33, no. 6, pp. 1203–1209, 1986.

[113] M. Bagatin and S. Gerardin, *Ionizing radiation effects in electronics: from memories to imagers.* CRC press, 2018.

[114] T. R. Oldham, "Switching oxide traps," *International journal of high speed electronics and systems*, vol. 14, no. 02, pp. 581–603, 2004.

[115] F. J. Feigl, W. B. Fowler, and K. L. Yip, "Oxygen vacancy model for the e1 center in sio2," *Solid State Communications*, vol. 14, no. 3, pp. 225–229, 1974.

[116] T.-P. Ma and P. V. Dressendorfer, *Ionizing radiation effects in MOS devices and circuits.* John Wiley & Sons, 1989.

[117] M. Poizat, "Total ionizing dose mechanisms and effects," tech. rep., Technical Report. Space Center EPFL and European Space Agency. http://space . . . , 2009.

[118] F. McLean, "A framework for understanding radiation-induced interface states in sio2 mos structures," *IEEE transactions on Nuclear Science*, vol. 27, no. 6, pp. 1651–1657, 1980.

[119] R. C. Lacoe, "Improving integrated circuit performance through the application of hardness-by-design methodology," *IEEE transactions on Nuclear Science*, vol. 55, no. 4, pp. 1903–1925, 2008.

[120] M. McLain, H. J. Barnaby, K. E. Holbert, R. D. Schrimpf, H. Shah, A. Amort, M. Baze, and J. Wert, "Enhanced tid susceptibility in sub-100 nm bulk cmos i/o transistors and circuits," *IEEE Transactions on Nuclear Science*, vol. 54, no. 6, pp. 2210–2217, 2007.

[121] R. C. Lacoe, J. V. Osborn, R. Koga, S. Brown, and D. C. Mayer, "Application of hardness-by-design methodology to radiation-tolerant asic technologies," *IEEE Transactions on Nuclear Science*, vol. 47, no. 6, pp. 2334–2341, 2000.

[122] E. El-Sayed, "Design of radiation hard CMOS aps image sensors for space applications," in *Proc. Seventeenth National Radio Science Conf. 17th NRSC '2000*, pp. D5/1–D5/9, 2000.

[123] M. Cohen and J. P. David, "Radiation effects on active pixel sensors," in *1999 Fifth European Conference on Radiation and Its Effects on Components and Systems. RADECS 99 (Cat. No.99TH8471)*, pp. 450–456, Sep. 1999.

[124] G. Hopkinson, C. Dale, and P. Marshall, "Proton effects in charge-coupled devices," *IEEE transactions on nuclear science*, vol. 43, no. 2, pp. 614–627, 1996.

[125] G. Hopkinson, "Radiation-induced dark current increases in ccds," in *RADECS 93. Second European Conference on Radiation and its Effects on Components and Systems (Cat. No. 93TH0616-3)*, pp. 401–408, IEEE, 1993.

[126] G. R. Hopkinson, "Radiation effects in a CMOS active pixel sensor," *IEEE Transactions on Nuclear Science*, vol. 47, pp. 2480–2484, Dec. 2000.

[127] W. Dulinski, G. Deptuch, Y. Gornushkin, P. Jalocha, J. L. Riester, and M. Winter, "Radiation hardness study of an aps CMOS particle tracker," in *Proc. IEEE Nuclear Science Symp. Conf. Record (Cat. No.01CH37310)*, vol. 1, pp. 100–103 vol.1, Nov. 2001.

[128] E. S. Eid, T. Y. Chan, E. R. Fossurn, R. H. Tsai, R. Spagnuolo, J. Deily, W. B. Byers, and J. C. Peden, "Design and characterization of ionizing radiation-tolerant CMOS aps image sensors up to 30 mrd (si) total dose," *IEEE Transactions on Nuclear Science*, vol. 48, pp. 1796–1806, Dec. 2001.

[129] J. Bogaerts, B. Dierickx, G. Meynants, and D. Uwaerts, "Total dose and displacement damage effects in a radiation-hardened cmos aps," *IEEE Transactions on electron devices*, vol. 50, no. 1, pp. 84–90, 2003.

[130] V. Goiffon, P. Cervantes, C. Virmontois, F. Corbiere, P. Magnan, and M. Estribeau, "Generic radiation hardened photodiode layouts for deep submicron CMOS image sensor processes," *IEEE Transactions on Nuclear Science*, vol. 58, pp. 3076–3084, Dec. 2011.

[131] M. Innocent, "A radiation tolerant 4t pixel for space applications," *Proc. IISW*, 2009.

[132] V. Goiffon, M. Estribeau, O. Marcelot, P. Cervantes, P. Magnan, M. Gaillardin, C. Virmontois, P. Martin-Gonthier, R. Molina, F. Corbiere, S. Girard, P. Paillet, and C. Marcandella, "Radiation effects in pinned photodiode CMOS image sensors: Pixel performance degradation due to total ionizing dose," *IEEE Transactions on Nuclear Science*, vol. 59, pp. 2878–2887, Dec. 2012.

[133] S. Place, J. P. Carrere, S. Allegret, P. Magnan, V. Goiffon, and F. Roy, "Rad tolerant CMOS image sensor based on hole collection 4T pixel pinned photodiode," *IEEE Transactions on Nuclear Science*, vol. 59, pp. 2888–2893, Dec. 2012.

[134] M. Esposito, T. Anaxagoras, O. Diaz, K. Wells, and N. M. Allinson, "Radiation hardness of a large area CMOS active pixel sensor for bio-medical applications," in *Proc. IEEE Nuclear Science Symp. and Medical Imaging Conf. Record (NSS/MIC)*, pp. 1300–1304, Oct. 2012.

[135] A. BenMoussa, S. Gissot, B. Giordanengo, G. Meynants, X. Wang, B. Wolfs, J. Bogaerts, U. Schühle, G. Berger, A. Gottwald, C. Laubis, U. Kroth, F. Scholze, A. Soltani, and T. Saito, "Irradiation damage

tests on backside-illuminated CMOS aps prototypes for the extreme ultraviolet imager on-board solar orbiter," *IEEE Transactions on Nuclear Science*, vol. 60, pp. 3907–3914, Oct. 2013.

[136] V. Re, L. Gaioni, A. Manazza, M. Manghisoni, L. Ratti, and G. Traversi, "Radiation tolerance of devices and circuits in a 3D technology based on the vertical integration of two 130-nm CMOS layers," *IEEE Transactions on Nuclear Science*, vol. 60, pp. 4526–4532, Dec. 2013.

[137] V. Goiffon, M. Estribeau, P. Cervantes, R. Molina, M. Gaillardin, and P. Magnan, "Influence of transfer gate design and bias on the radiation hardness of pinned photodiode CMOS image sensors," *IEEE Transactions on Nuclear Science*, vol. 61, pp. 3290–3301, Dec. 2014.

[138] M. Cohen and J. P. David, "Radiation-induced dark current in CMOS active pixel sensors," *IEEE Transactions on Nuclear Science*, vol. 47, pp. 2485–2491, Dec. 2000.

[139] B. Hancock and G. Soli, "Total dose testing of a cmos charged particle spectrometer," *IEEE Transactions on Nuclear Science*, vol. 44, no. 6, pp. 1957–1964, 1997.

[140] J. Bogaert and B. Dierickx, "Total dose effects on cmos active pixel sensors," in *Sensors and Camera Systems for Scientific, Industrial, and Digital Photography Applications*, vol. 3965, pp. 157–168, International Society for Optics and Photonics, 2000.

[141] B. R. Hancock, T. J. Cunningham, K. P. McCarty, G. Yang, C. J. Wrigley, P. G. Ringold, R. C. Stirbl, and B. Pain, "Multi-megarad (si) radiation-tolerant integrated cmos imager," in *Sensors and Camera Systems for Scientific, Industrial, and Digital Photography Applications II*, vol. 4306, pp. 147–156, International Society for Optics and Photonics, 2001.

[142] V. Goiffon, "Radiation effects on cmos active pixel image sensors," in *Ionizing Radiation Effects in Electronics*, pp. 312–349, CRC Press, 2015.

[143] S. Dhombres, A. Michez, J. Boch, S. Beauvivre, J. R. Vaille, A. D. Touboul, P. C. Adell, F. Bezerra, E. Lorfevre, D. Kraehenbuehl, and F. Saigne, "Dose effects on CMOS active pixel sensors," in *Proc. 15th European Conf. Radiation and Its Effects Components and Systems (RADECS)*, pp. 1–3, Sept. 2015.

[144] W. Zujun, L. Changju, M. Yan, W. Zhijun, W. Ying, T. Benqi, L. Minbo, and L. Zhiyong, "Degradation of CMOS aps image sensors induced by total ionizing dose radiation at different dose rates and biased conditions," *IEEE Transactions on Nuclear Science*, vol. 62, pp. 527–533, Apr. 2015.

[145] J. Tan and A. Theuwissen, "Investigation of x-ray damage effects on 4t cmos image sensors," in *2012 International Semiconductor Conference Dresden-Grenoble (ISCDG)*, pp. 131–134, IEEE, 2012.

[146] V. Goiffon, C. Virmontois, P. Magnan, P. Cervantes, S. Place, M. Gaillardin, S. Girard, P. Paillet, M. Estribeau, and P. Martin-Gonthier, "Identification of radiation induced dark current sources in

pinned photodiode cmos image sensors," *IEEE Transactions on Nuclear Science*, vol. 59, no. 4, pp. 918–926, 2012.

[147] J. Tan and A. J. Theuwissen, "Total ionizing dose effects on 4-transistor cmos image sensor pixels," in *2010 IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC)*, pp. 1–4, IEEE, 2010.

[148] V. Goiffon, C. Virmontois, P. Magnan, S. Girard, and P. Paillet, "Analysis of total dose-induced dark current in cmos image sensors from interface state and trapped charge density measurements," *IEEE Transactions on Nuclear Science*, vol. 57, no. 6, pp. 3087–3094, 2010.

[149] F. Faccio, H. J. Barnaby, X. J. Chen, D. M. Fleetwood, L. Gonella, M. McLain, and R. D. Schrimpf, "Total ionizing dose effects in shallow trench isolation oxides," *Microelectronics Reliability*, vol. 48, no. 7, pp. 1000–1007, 2008.

[150] V. Goiffon, M. Estribeau, and P. Magnan, "Overview of ionizing radiation effects in image sensors fabricated in a deep-submicrometer cmos imaging technology," *IEEE Transactions on Electron Devices*, vol. 56, no. 11, pp. 2594–2601, 2009.

[151] X. Qian, H. Yu, B. Zhao, S. Chen, and K. S. Low, "Design of a radiation tolerant cmos image sensor," in *2011 International Symposium on Integrated Circuits*, pp. 412–415, IEEE, 2011.

[152] T. Watanabe, T. Takeuchi, O. Ozawa, H. Komanome, T. Akahori, and K. Tsuchiya, "A new radiation hardened cmos image sensor for nuclear plant," in *International image sensor workshop (IISW)*, 2017.

[153] S. Mahato, G. Meynants, G. Raskin, J. De Ridder, and H. Van Winckel, "Noise optimization of the source follower of a cmos pixel using bsim3 noise model," in *High Energy, Optical, and Infrared Detectors for Astronomy VII*, vol. 9915, p. 99151P, International Society for Optics and Photonics, 2016.

[154] N. Kawai and S. Kawahito, "Effectiveness of a correlated multiple sampling differential averager for reducing 1/f noise," *IEICE Electronics Express*, vol. 2, no. 13, pp. 379–383, 2005.

[155] V. Goiffon, S. Rizzolo, F. Corbière, S. Rolando, S. Bounasser, M. Sergent, A. Chabane, O. Marcelot, M. Estribeau, P. Magnan, *et al.*, "Total ionizing dose effects on a radiation-hardened cmos image sensor demonstrator for iter remote handling," *IEEE Transactions on Nuclear Science*, vol. 65, no. 1, pp. 101–110, 2018.

[156] A. Boukhayma, A. Peizerat, and C. Enz, "Noise reduction techniques and scaling effects towards photon counting cmos image sensors," *Sensors*, vol. 16, no. 4, p. 514, 2016.

[157] R. J. Baker, *CMOS: circuit design, layout, and simulation*, vol. 1. John Wiley & Sons, 2008.

[158] B. P. Ginsburg and A. P. Chandrakasan, "An energy-efficient charge recycling approach for a sar converter with capacitive dac," in *2005 IEEE International Symposium on Circuits and Systems*, pp. 184–187 Vol. 1, May 2005.

[159] C. Liu, S. Chang, G. Huang, and Y. Lin, "A 10-bit 50-ms/s sar adc with a monotonic capacitor switching procedure," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 731–740, April 2010.

[160] V. Hariprasath, J. Guerber, S. . Lee, and U. . Moon, "Merged capacitor switching based sar adc with highest switching energy-efficiency," *Electronics Letters*, vol. 46, pp. 620–621, April 2010.

[161] C. Yuan and Y. Lam, "Low-energy and area-efficient tri-level switching scheme for sar adc," *Electronics Letters*, vol. 48, pp. 482–483, April 2012.

[162] W.-L. Wu, Y. Zhu, L. Ding, C.-H. Chan, U. F. Chio, S.-W. Sin, U. Seng-Pan, and R. P. Martins, "A 0.6v 8b 100ms/s sar adc with minimized dac capacitance and switching energy in 65nm cmos," *2013 IEEE International Symposium on Circuits and Systems (ISCAS2013)*, pp. 2239–2242, 2013.

[163] A. Agnes, E. Bonizzoni, and F. Maloberti, "Design of an ultra-low power sa-adc with medium/high resolution and speed," in *2008 IEEE International Symposium on Circuits and Systems*, pp. 1–4, 2008.

Curriculum Vitae

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EDUCATION

- B.S., Microelectronics, Xi'an University of Post & Telecommunications, 2010.
- M.S., Electrical Engineering, University of Macau, 2013.
  Concentrations: Analog & Mixed-signal Integrated Circuit Design
  Dissertation: Monotonic Multi-Switching Method for Ultra-Low-Voltage Energy Efficient SAR ADCs
  Dissertation Advisors: Seng-Pan U, Ph.D., Sin Sai Weng, Ph.D.
- Ph.D., Electrical Engineering, University of Nevada, Las Vegas, 2019.
  Concentrations: CMOS image sensor design, Analog & Mixed-signal Integrated Circuit Design
  Dissertation: High-Speed Radhard Mega-Pixel CIS Camera For High-Energy Physics
  Dissertation Advisors: Russel Jacob Baker, Ph.D.

EMPLOYMENT

- State Key Laboratory of Analog and Mixed-Signal VLSI at University of Macau, 2010–2013.
- University of Nevada, Las Vegas, 2013–2016.
- Alphacore, Inc., Tempe, AZ, 2016–present.

PUBLICATIONS

Journal Articles

- Design and analysis of a feedback time difference amplifier with linear and programmable gain, *Analog Integrated Circuits and Signal Processing* 94, 357-367.

Conference Articles

- A linear high gain time difference amplifier using feedback gain control, *2016 IEEE Dallas Circuits and Systems Conference (DCAS)*, 2016.
- A 0.6V 8b 100MS/s SAR ADC with minimized DAC capacitance and switching energy in 65nm CMOS, *2013 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2013.
- A 13-bit 60MS/s split pipelined ADC with background gain and mismatch error calibration, *2013 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2013.
- A 10-bit SAR ADC with two redundant decisions and splitted-MSB-cap DAC array, *2012 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, 2012.

TEACHING EXPERIENCE

Teaching Assistant, University at Nevada, Las Vegas, 2013-2016

Courses: Analog Circuit Design Lab, Digital Circuit Design Lab

PROFESSIONAL MEMBERSHIP

Tau Beta Pi - The Engineering Honor Society

RELEVANT SKILLS

- Skillful of various EDA tools: Cadence (Virtuoso, Assura, PVS, Spectre/SpectreRF), LTspice, Hspice, Electric, Mentor Graphics (Pyxis, Calibre, Eldo), Altium, and KiCad
- Programming ability in Matlab, Verilog-A, Python, and LaTex
- Extensive knowledge of different operating system (UNIX, Linux, Windows)
- Fluent in English and Chinese

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