HIGH VOLTAGE CHARGE PUMP CIRCUIT

FOR AN ION MOBILITY SPECTROMETER

by

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The project submitted by Sandeep Pemmaraju entitled HIGH VOLTAGE CHARGE PUMP CIRCUIT FOR AN ION MOBILITY SPECTROMETER is hereby approved:

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I dedicate this work to my parents, without whom I would not be here, to my caring brother and to my friend Mr. Ravi Kumar (Late). My inexpressible gratitude to Ms. Sandhya Reddy who stood as a rigid support and always had a word of encouragement right from the beginning of my undergraduate degree.

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LIST OF SYMBOLS

V_{DD} ..... Supply voltage

V_{DS} ..... Drain to source voltage

V_{SD} ..... Source to drain voltage

V_{GS} ..... Gate to source voltage

V_d ..... Diode forward bias voltage

I_{DM} ..... Pulsed drain current

P_{tot} ..... Power dissipation

T_{amb} ..... Ambient temperature

T_j ..... Operating temperature range

T_{stg} ..... Storage tempeature range

A ..... amperes

V ..... volts

m ..... milli

p ..... pico

u ..... micro

n ..... nano

f ..... femto

V_F ..... Diode forward bias voltage

C_T ..... Total capacitance

V_{RRM} ..... Peak repetitive reverse voltage

I_{rr} ..... Maximum full load reverse current

P_D ..... Power dissipation

K ..... kilo

N ..... Number of stages

I_L ..... Load current

F_{osc} ..... Frequency of oscillation

C_{out} ..... Output or load capacitance

R_{load} ..... Load resistance

V_{output} ..... Load or output voltage

η ..... Efficiency

V_{load} ..... Load or output voltage

V_{in} ..... Input voltage

LIST OF ABBREVIATIONS

BSU .....Boise State University

EPA .....Environmental Protection Agency

IMS .....Ion Mobility Spectrometer

HRIMS .....High Resolution Ion Mobility Spectrometer

LTCC ..... Low Temperature Co-Fired Ceramics

CHEMFET .....Chemical Field Effect Transistor

PIC ..... Program Interrupt Controller

DC ..... Direct Current

MOS ..... Metal Oxide Semiconductor

PMOS ..... P-channel Metal Oxide Semiconductor

NMOS .....N-channel Metal Oxide Semiconductor

PCB .....Printed Circuit Board

SPICE ..... Simulation Program with Integrated Circuit Emphasis

HP .....Hewlett Packard

R ..... Resistance

C .....Capacitance

t ..... time

AC ..... Alternate current

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ABSTRACT

Overview of the Project

A high voltage power supply circuit is required for the Ion Mobility Spectrometer (IMS) to maintain a uniform electric field through out the sensing unit. The design of the power supply is achieved by using a voltage multiplier circuit. A primary level shifting circuit is also employed to produce high voltage clock pulses from a low voltage clock pulse source. Performance of the power supply with regards to power consumption, load resistance, frequency and efficiency besides low cost are of vital importance.

Project Goal

To build a low cost, low power, high voltage power supply, which is tolerant to variations in the load resistance and input clock frequency.

Project Organization

The project is divided in to six chapters:

- First chapter gives an overview of the project and an introduction to the IMS and its assembly. It also gives the project requirements and objectives.
- The second chapter gives a brief introduction to the different stages in the power supply circuit and a procedure to start the design.

- Chapter three describes the design of the charge pump.
- Chapter four describes the layout of the printed circuit board and the experimental results.
- Chapter five describes the performance of the power supply circuit.

Achievements

- A 2000V, 1.25W, power supply is built on a Printed Circuit Board (PCB) using discrete components.
- The power supply built was 1.2” x 6” in size.
- Prototype built was tolerant to loads between 20MΩ and 60MΩ with frequency ranging between 20KHz and 100KHz.
- The prototype was also tolerant to supply voltage variations, with power efficiency equal to 9%.

CHAPTER 1. INTRODUCTION

The Environmental Protection Agency (EPA) has contracted with Boise State University (BSU) researchers to develop a compact high voltage power supply and a sensing scheme to detect the electro chemicals from the IMS. Simultaneous work proceeds in developing a micro controller to control the voltage supply and to interact with the sensing scheme.

Figure 1.1 describes the basic components of the system.

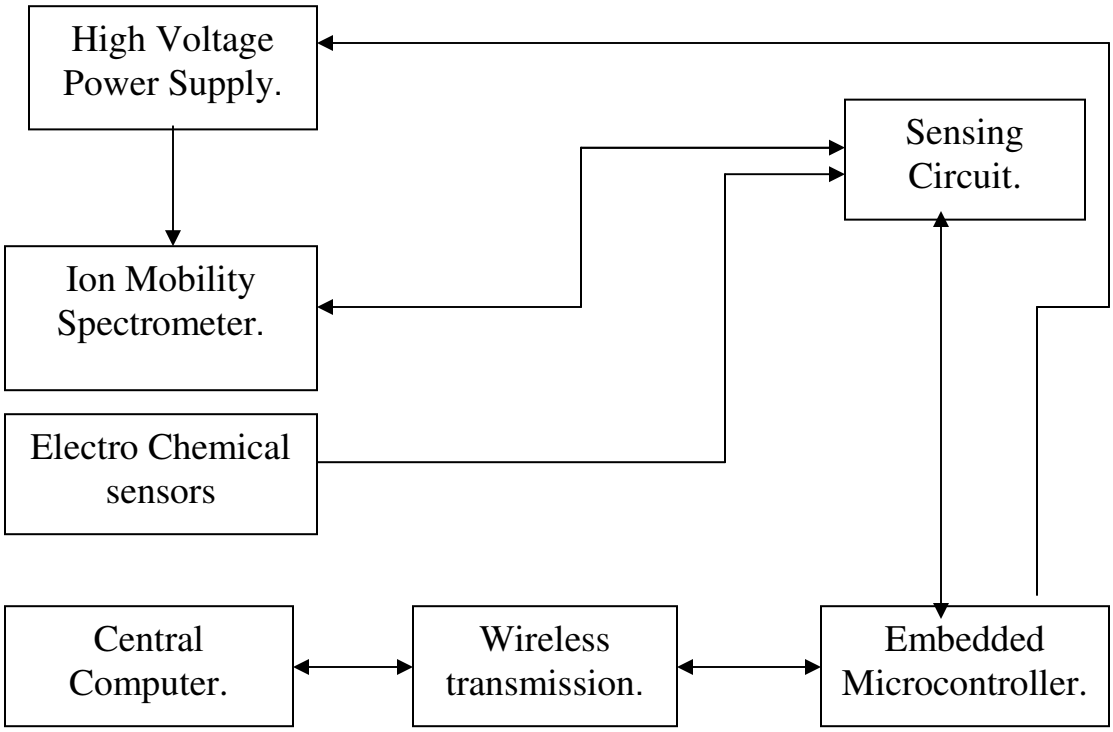

Figure 1.1: System representation.

The system consists of:

1) Ion mobility spectrometer.
2) Electro chemical sensors.
3) High voltage power supply.
4) Sensing circuit.
5) Embedded micro controller.
6) Wireless transmission network.
7) Central computer to control the whole equipment.

Ion Mobility Spectrometer

The IMS basically consists of the following parts:

1) Tyndall gate.
2) Aperture grid.
3) Collector plate.
4) Silicon membrane.
5) Nickel-63.

The section is known as the drift tube as shown in figure 1.2. The drift tube is made up of layers of Low Temperature Co-fired Ceramic (LTCC) in the project developed here at BSU [1].

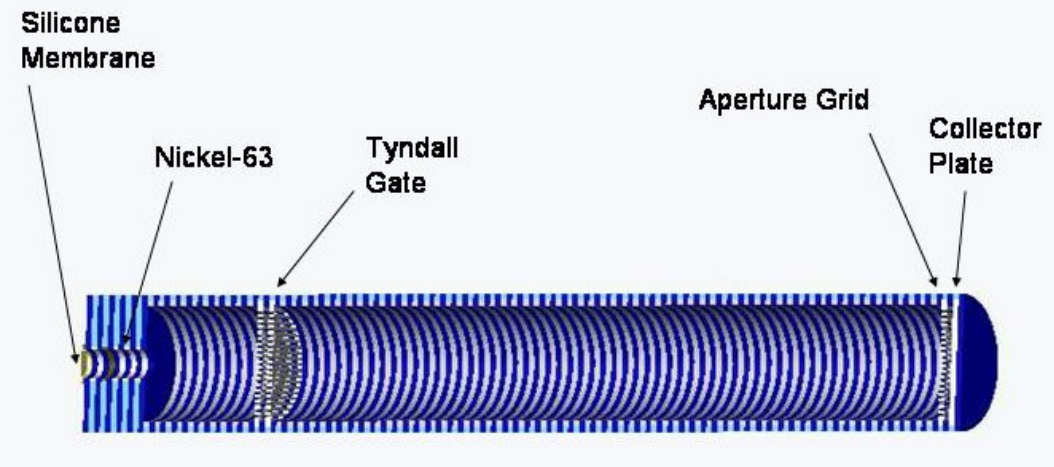

Figure 1.2: IMS drift tube

Basic Operation of the Ion Mobility Spectrometer

The Ion mobility Spectrometer (IMS) is based on the principle of separating ions as they travel through a purified gas in an electric field.

The chemical species enters the reaction tube. Nickle-63 is a beta multiplier and ionizes the chemical species. These ions enter the drift tube, which has a constant electric field applied across it. The function of the electronic shutter, which is the Tyndall Gate, is to allow the ions to flow through the tube in specific intervals of time. The ions are moved through the drift tube under the applied electric field. These Ions will travel at different velocities depending upon the strength of the electric field, the length of the drift

tube, temperature, atmospheric pressure, ion mass, ion weight, size and shape. The ions are collected at the collector, which is here a simple faraday cup. The signals are amplified and converted in to voltage signals.

The voltage signals are fed in to an embedded micro controller, which reads the data and outputs the averaged data signal. The final output value is transmitted using a wireless network and compared to a look up table to investigate the nature of the chemical species.

Embedded Microcontroller

The Embedded microcontroller system, here after called the microcontroller is the central subsystem of the multi-sensor system. It includes both hardware and software components for receiving and processing data from the sensors [2]. The microcontroller was built by a group here at BSU. It is a low cost system with a capability to collect and process information from different sensors like chemical sensors, pressure sensors and temperature sensors. The microcontroller sends the data representing the concentration of the detected chemicals to the central computer via wireless transmission.

High Voltage Power Supply

The electric field required for the IMS is provided by a high voltage charge pump circuit, which runs across the length of the drift tube. This helps in maintaining a constant Voltage difference per unit length along the drift tube of an IMS.

The present IMS is designed for an electric field of 500V/cm. The voltage required for the IMS therefore depends on the length of the drift tube. A typical design for the length of the drift tube in an IMS is 4 cm and thus the Voltage supply required to meet the specifications of the IMS is 2000V.

Requirements of the Power supply

1) Power rating - 1Watt
2) Voltage rating - 2000V for 4 cm length of the drift tube which means the electric field in the tube is 500V/cm.
3) Minimum sized printed circuit board.
4) High voltages cannot be implemented in chip level, so this is only possible by using discrete components.

Requirements for the IMS

1) Provide the desired electric field required for the IMS drift tube.
2) Low cost - $300 to $350.
3) Size constraint: 12cm by 6cm.
4) Power constraint: 1 Watt
5) A signal proportional to the output voltage must be sent to the (Program Interrupt Controller) PIC so that it controls the input clock signal and hence maintains the output voltage at the desired value.

6) Provide easy means to switch OFF and turn ON the supply for every 40 ms or whenever desired.
7) Trade-offs between the load resistance and the input clock frequency should be taken in to account.

There are many possible ways of supplying a high voltage required for the IMS.The low power and small size constraints decrease the number of available options. Many low power supplies are available in the market but do not produce such high voltages. For high voltage generation, a charge pump circuit, based on the principle of charge sharing is selected.

The proposed size of the circuit board by the mechanical engineers at BSU is shown figure 1.3. The figure shown includes the total size of the circuit board required for both the Power supply and the delta-sigma modulation circuits. The size of the board is 15cm x 3cm x 0.85cm.

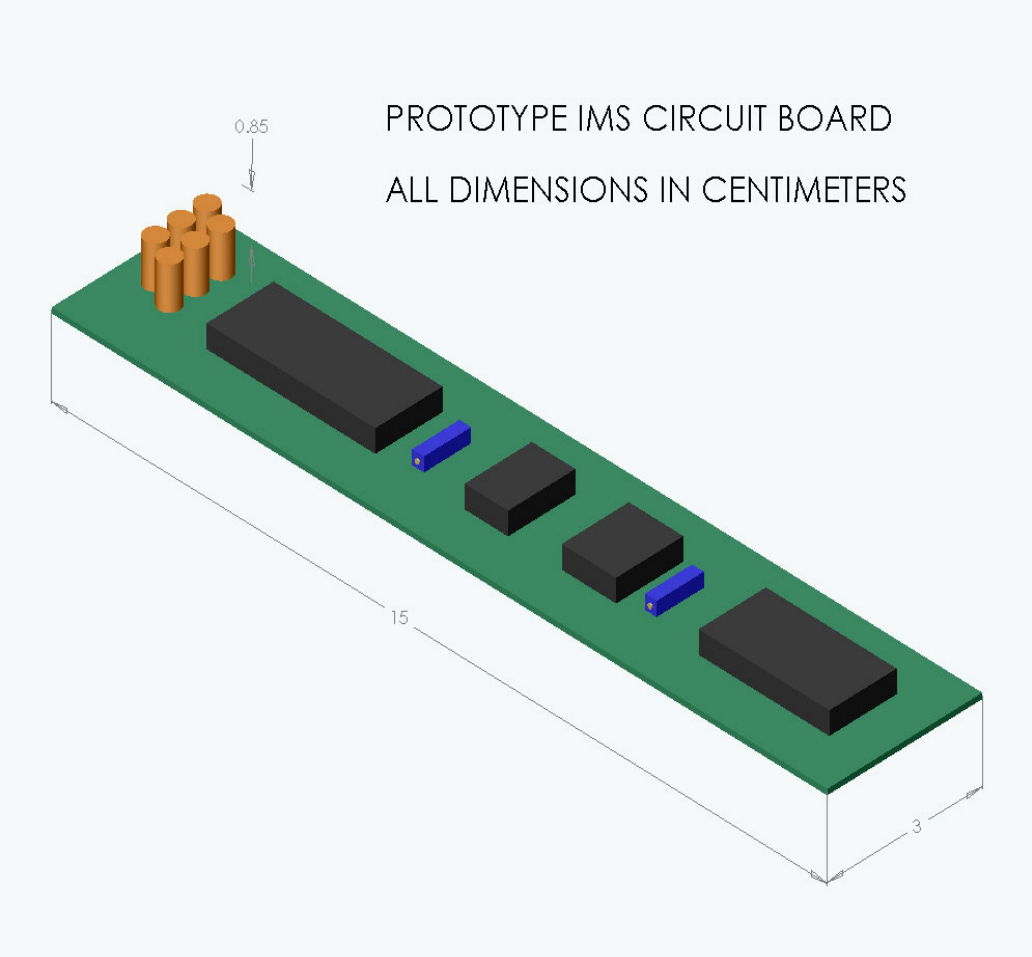

Figure 1.3: Proposed dimensions of the circuit board.

CHAPTER 2. COMPONENTS OF THE POWER SUPLLY

Sequential Procedure for Building the Power Supply

Building the prototype of the high voltage power supply includes a series of steps. Each step much be designed carefully [5]. The power supply was designed in accordance with the following sequential procedure:

1) Pick the appropriate devices with permissible device parameters and sizes which might meet the design specifications.
2) Simulate the circuit using the SPICE models of the chosen devices, H-SPICE was used as the simulation tool.
3) If the simulation results are not agreeable i.e. if they do not meet the design specifications, then go to step 1.
4) If the simulations results are good i.e. meet the design specifications, check out for the packaging type of each discrete component.
5) Design a printed circuit board with the respective packaging styles of each device. Express PCB software was used for laying out the PCB.
6) Check if the Layout of the PCB is more than the proposed dimensions.
7) If yes then rearrange the layout of the PCB to fit in the proposed size of the PCB. If it still does not fit, go to step 1.

8) Order the printed circuit boards and the devices.

9) Solder the devices in their respective positions to build the prototype.

10) Test the circuit.

11) Compare simulated and measured results.

Description of the High Voltage Power Supply

The high voltage power supply circuit can be divided in to five parts [3] as shown in the block diagram in figure 2.1.

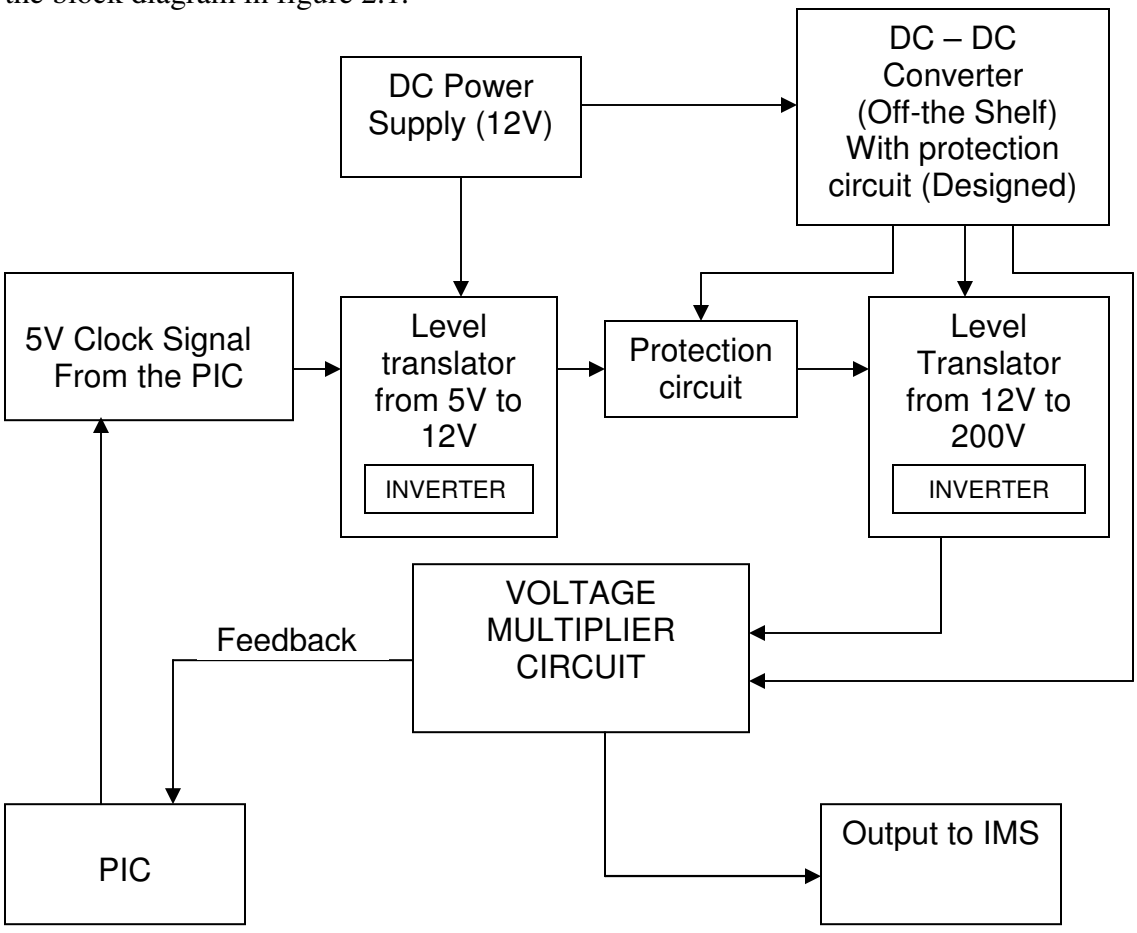

Figure 2.1: Block diagram of the High voltage power supply.

1) DC power supply: DC power supply of 12V is used as an input to the level translator block.
2) DC-DC converter with protection circuit: The 12V Dc supply is converter to an 200V DC supply by using a 12V-200V DC-Dc converter. A protection circuit is also included to protect the device from negative voltages.
3) 5V clock signal from the PIC: The clock is derived from the PIC and is used to create two non-overlapping clock signals.
4) Level translator: The level translator is used to translate the 5V clock signal in to a 200V clock signal. Figure 2.2 shows the schematic of the level translator circuit. It uses two stages of level translation as shown in the block diagram.
5) Protection circuit: In between the two level translators, a protection circuit is used to protect the second level translator (high voltage conversion) from breaking down.
6) Voltage Multiplier circuit: This forms the heart of the high voltage power supply circuit [4]. It basically multiplies the 200V available to produce a higher voltage. Any desired voltage can be obtained by changing the number of stages in the voltage multiplier circuit.
7) Output to IMS: The high voltage produced using the voltage multiplier is fed to the IMS drift tube.
8) PIC: The high voltage produced is now reduced to an acceptable value of voltage by the PIC. The reduced voltage, which is proportional to the high voltage, is

compared to a reference value. This forms the feed back circuit, which controls the frequency of the clock signal, and is fed as the input to the circuit.

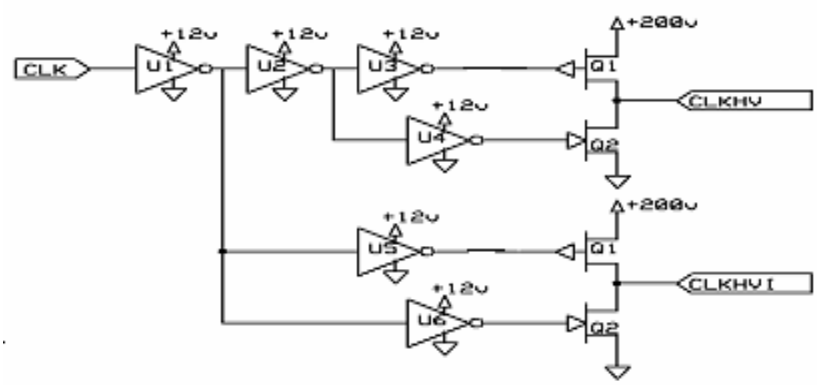

Figure 2.2: Schematic of the circuit used for the level shifting circuit.

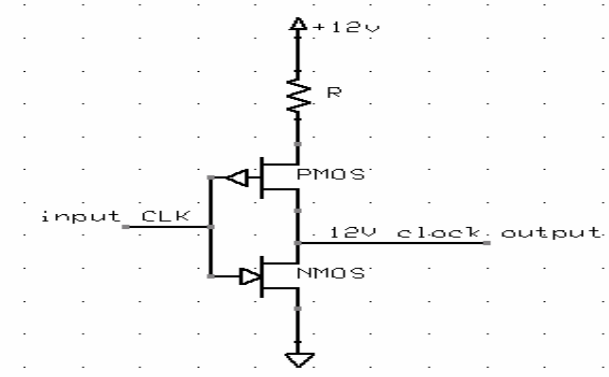

Figure 2.3: Schematic of the inverter labeled as 'U' in figure 2.2.

The level shifting circuit used for the high voltage power supply is shown figure 2.2. The "CLK" in the circuit of figure 2.3 is a clock pulse derived from the PIC. U1 to U6 are inverters with a 12V supply at their drains. U1 has a 5V clock signal from the PIC as its input. One of its other inputs is connected to a 12V supply. Thus by the inverter action the 5V clock signal is converted to a 12V clock signal. A second level translator

stage is used to convert the 12V clock pulse in to 200V clock pulse. An off-the shelf DC-DC converter is used as a 200V DC source.

The circuit in figure 2.4 is called the Dickson charge pump [11]. The elements labeled D1 to D7 are high breakdown voltages rating diodes and elements named C1 to C7 are capacitors. R1 and R2 represent the load of the IMS. They also form a voltage divider to cut down the high output voltage and this voltage is fed back to the PIC. The PIC compares this voltage to a reference value and regulates the clock frequency used as the input in figure 2.1. Thus a precise output voltage can be maintained.

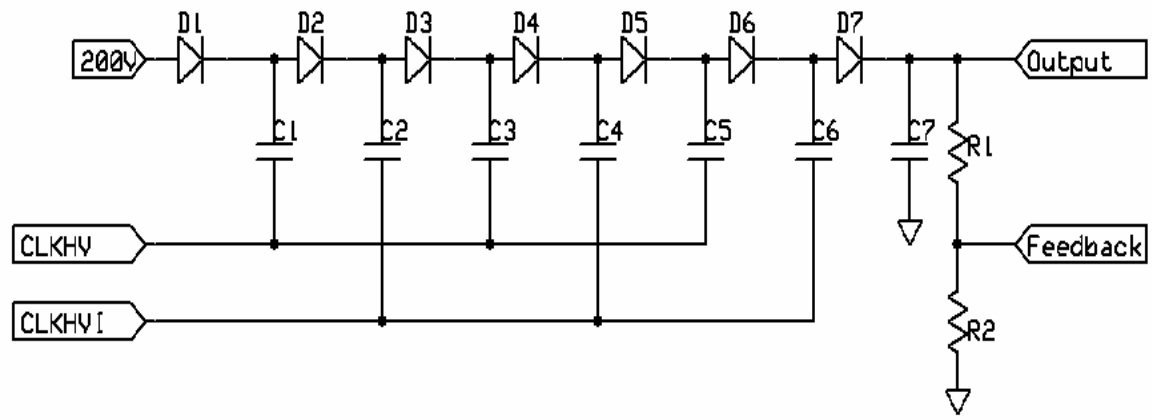

Figure 2.4: Dickson charge pump circuit.

The 200V supply in figures 2.1 and 2.2 are derived from a DC source. It is basically 12V DC/200V DC converter. A picture of the battery used is as shown in figure 2.5 [10].

Figure 2.5: A picture of the battery.

CHAPTER 3. DESIGN OF THE CHARGE PUMP

DC-DC Converter and Power Supply Protection

The Printed Circuit board is powered by a 12V external voltage source. The power supply voltage is not ideal and may have small variations. For this purpose, capacitors are connected across the power supply terminals to smoothen out the signal. They are called as decoupling capacitors. This also reduces the ground bounce. Ground bounce is the term used to determine the increase in the potential of ideal ground potential due to the resistance of the ground rail. When a current flows through the circuit, the resistance of the ground rail tends to change the effective potential to a potential higher than zero volts. Placing a capacitor pulls the node to zero. A schematic of this circuit is shown in figure 3.1.

A diode is placed on the input and the output to cut off the power supply if a negative voltage is applied.

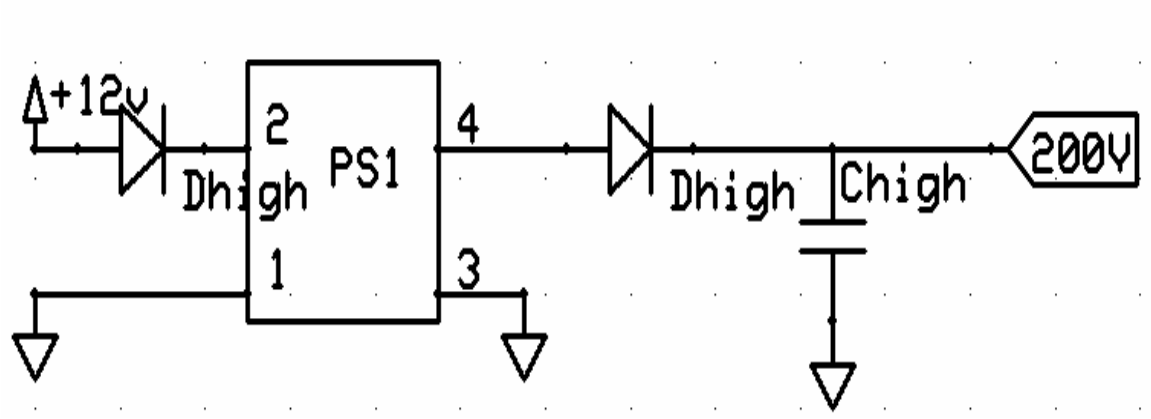

Figure 3.1: Power Supply protection circuit.

Level Translator and Inverter Characteristics

As seen in the previous section, the inverter is the major building block of the level translator circuit. The schematic of an inverter used for the first stage i.e. to convert the 5V clock signal to a 12V clock signal is shown in the figure 3.2.

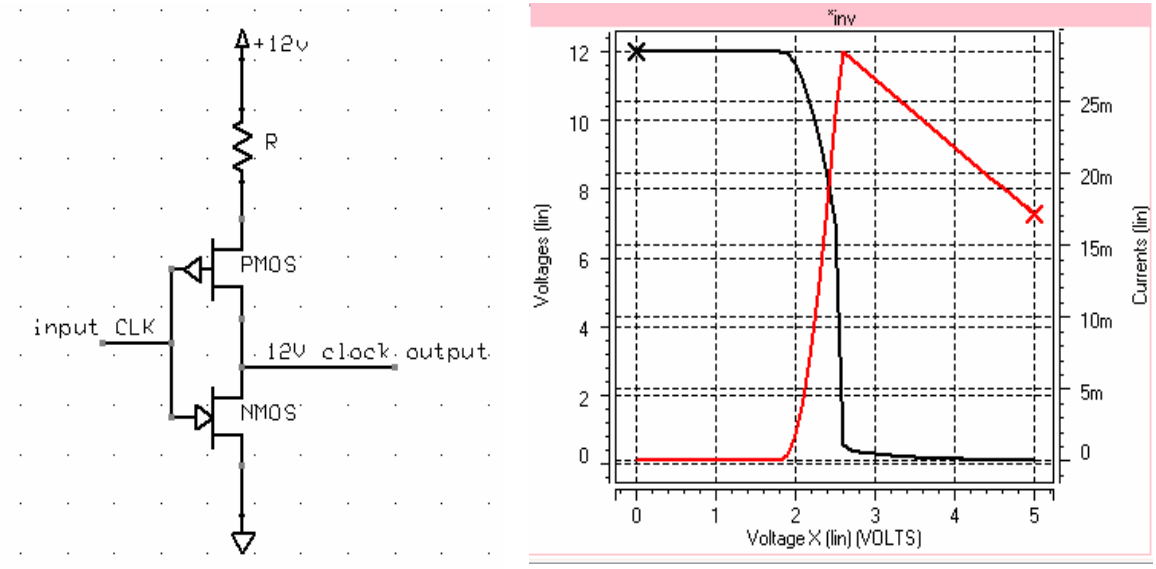

Figure 3.2: Inverter schematic and its output.

The inverter characteristics are also shown. The resistor 'R' is used to limit the current flowing through the circuit. Ideally either the PMOS or the NMOS are turned on depending on the input signal. Both are not turned on at the same time in an ideal inverter. In a practical circuit this is not the case, both the transistors are ON in a particular range of input voltages. There is a path from V_{DD} (i.e. 12V supply) to ground only when both the transistors are on and a contention current flows through the inverter circuit. This is a critical issue as the contention current reduces the power efficiency of

the overall circuit. The above inverter was simulated using the SPICE models of ZVP2106A and ZVN3306A. Details for using these transistors is shown in section 3.

The static current flowing through the inverter is around 15mA and this is an issue. The NMOS transistor should turn ON and the PMOS transistor should turn off when the input to the inverter is above 3V.But the PMOS does not turn off since the source is at 12V.So there is a considerable current flowing through the circuit. This is one of the future works.

A resistor of 200 ohms was connected with the inverter in figure 3.2. The average current flowing through the inverter is 20mA. The input CLK frequency is a 5V pulse, for which the output signal generated is a 12V pulse as shown in figure 3.3. Figure 3.4 and figure 3.5 shows the simulation results for the fall time and rise time of the output signal generated for the inverter shown in figure 3.3.

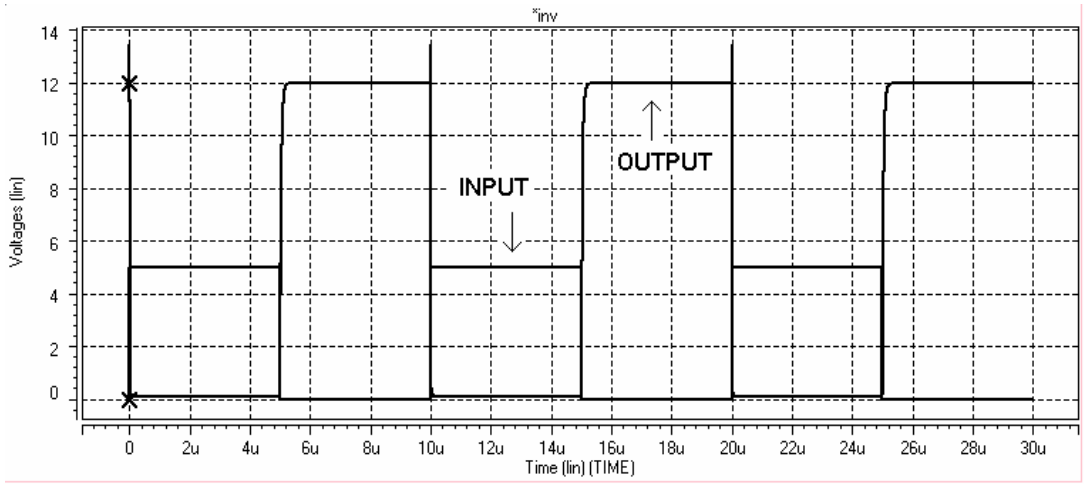

Figure 3.3: Simulations for CLK and output of U1 in figure 2.2.

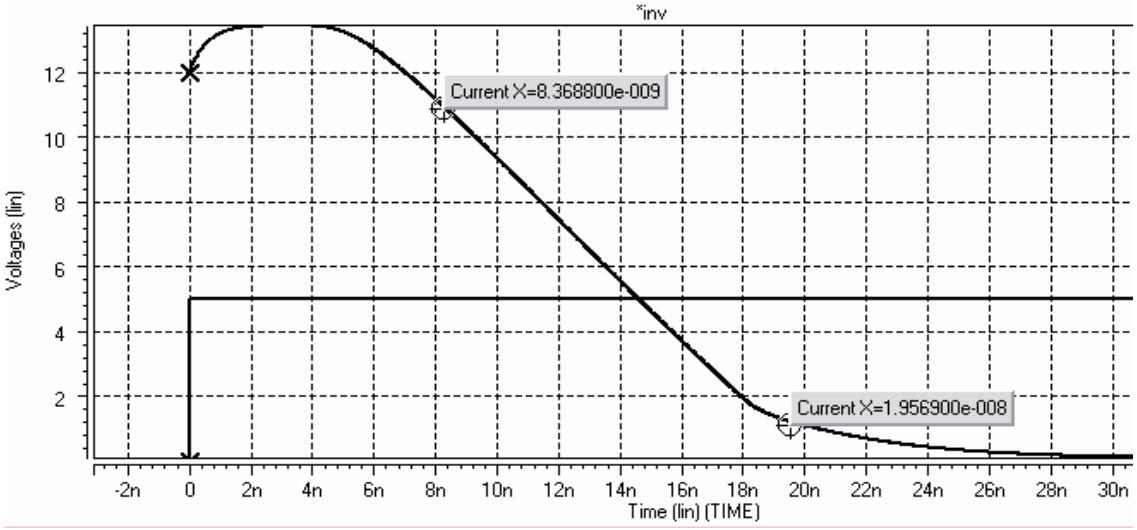

Figure 3.4: Simulations show that fall time of the inverter is around 8ns.

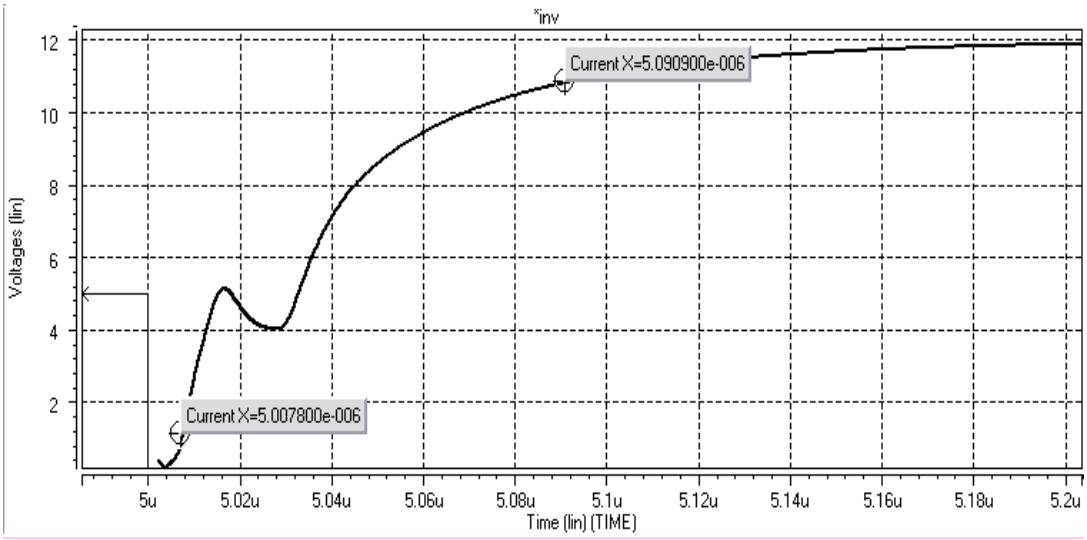

Figure 3.5: Simulation showing the rise time of the inverter (80ns).

Measured Results of the Inverter

Measured results for the fall times and rise times are shown in figures 3.6 and 3.7 respectively. Measured results are very close to the simulations done in H-SPICE . This shows that the models are good.

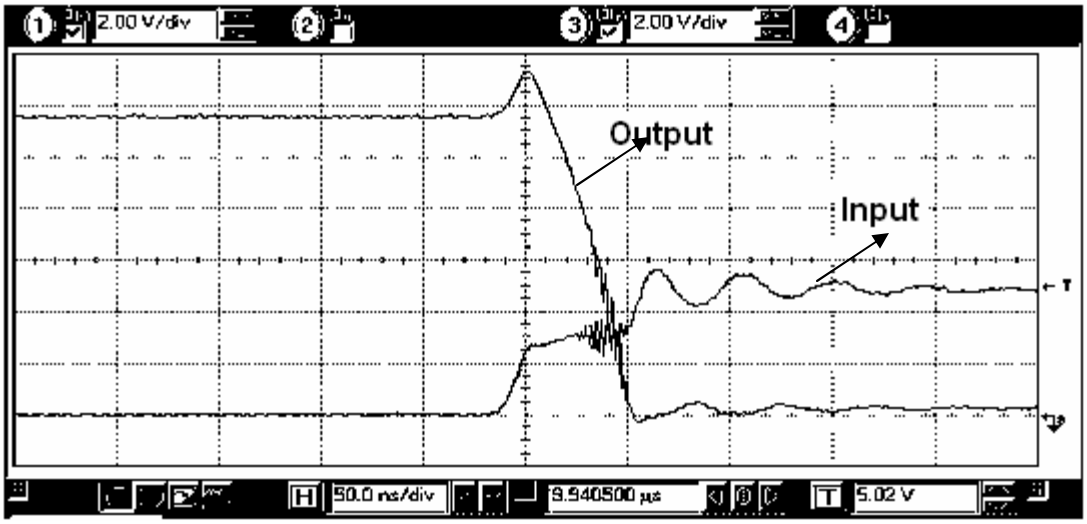

Figure 3.6: Measured results of the inverter fall time (20ns).

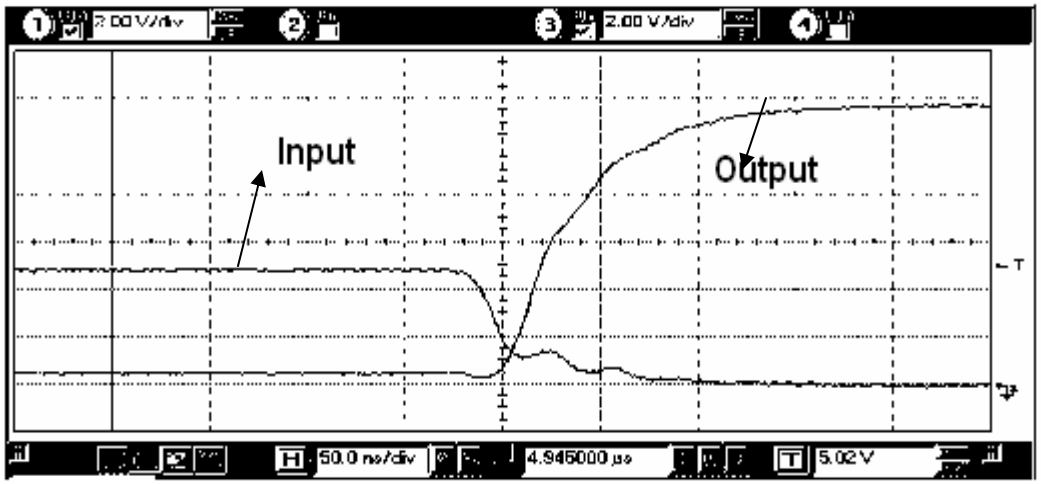

Figure 3.7: Measured results of the inverter rise time (90ns).

A resistor is placed in between the 12V supply and the drain of the PMOS device. The purpose of the resistor is to reduce the current flowing through the MOS devices and hence decrease the over all power drawn by the circuit. For better performance, a 200 ohms resistor is used for this particular circuit. It can be seen from the graph shown above that the output of the inverter is not pulled completely to 12V.This is because of a voltage drop across the resistor. Placing the resistor in pull up circuit increases the rise time. The above simulations clearly show that the rise time is more than the fall time. The resistance included, makes the rise time larger than the fall time.

Protection Circuit

Figure 3.8 shows the level translator circuit, which produces one phase of the clock. Initially the capacitor 'C' is charged to 200V through the 'R7' resistor. Here the capacitor value is 1000pF and the resistor R7 is 10MegΩ. The clock pulses from the PIC are applied to the circuit only after the capacitor has been given enough time to charge. This ensures that the PMOS device used in the second level translation does not breakdown. This is really very important for the circuit to function properly. This is explained in the next paragraph.

If the R-C circuit was not present and the 12V clock signal was applied directly to the ZVP2120A PMOS transistor, then the Source to Gate Voltage V_{SG} for the PMOS will be:

V_{SG}= 200-12 $\Rightarrow$ 200-0 =188V, or 200V depending on the input to the transistor is a 0 or a high. Referring to table 3.2. , the maximum gate to source voltage is 20V. Whatever

might be the input of the transistor (188V or 200V), both voltages are high enough to break the transistor.

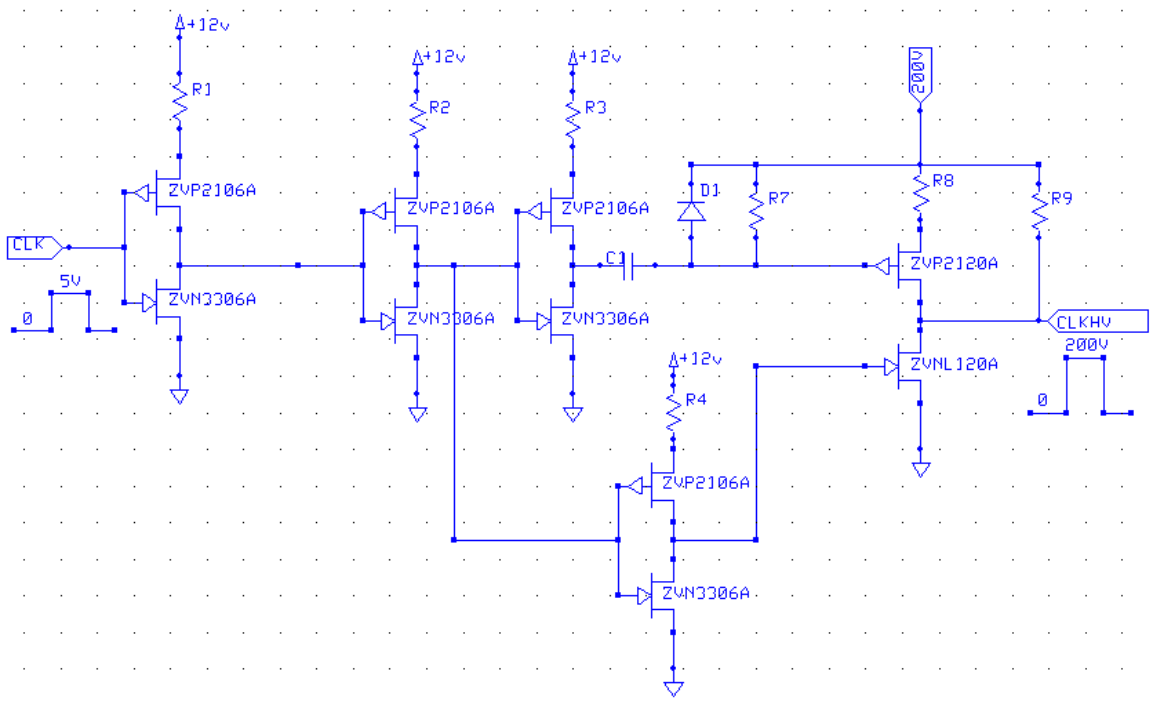

Figure 3.8: Expanded View of the Level Translator Circuit.

The NMOS transistor ZVNL120A does not require such protection circuit because the source is grounded and hence the gate to source voltage is nominal. When the protection circuit is introduced, the voltage on the gate of PMOS varies between 200V and 188V. When the clock is a low, the gate of the PMOS transistor is charged to 200V.Now when the clock goes high, the gate voltage also rises by the same amount i.e. 12V. So the gate voltage should be 212V, but meanwhile the diode clamps the voltage on the gate to V_d volts above 200V where V_d is the forward bias voltage of the diode (1V). The diode helps to clamp the node voltage to about 201V. The reason for selecting these devices is shown in page 20 and 21.

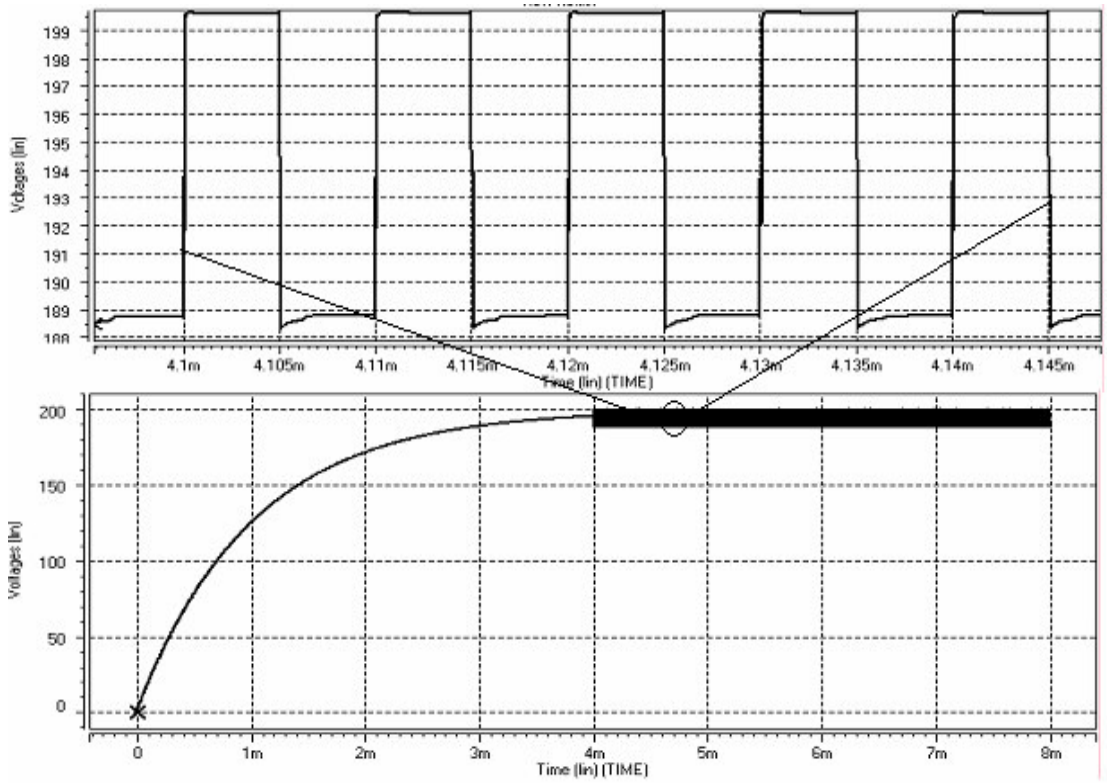

Figure 3.9: Node voltage at the gate of ZVP2120A transistor.

The gate to source voltage of the PMOS device is within the limits and the circuit functions properly. The clamping mechanism of the diode is very important to reduce the imperfections in the operation of the circuit when the clock time period is less than the discharging time of the R-C network. Figures 3.9 shows the outputs at the gate of ZVP2120A PMOS device.

The PMOS and NMOS devices used in U1 to U6 in figure 2.2 are ZVP2106A and ZVN3306A respectively [12], [13]. These are available as TO-92 packages. The maximum ratings of the PMOS and NMOS devices are as shown in Tables 3.1 and 3.2 .

Table 3.1: Maximum ratings of the PMOS and NMOS devices

PARAMETER	SYMBOL	VALUE		UNIT
		PMOS ZVP2106A	NMOS ZVN3306A	
Drain-Source Voltage	V_{DS}	-60	60	V
Continuous drain current at T_{amb}=25 ^{0}C	I_{DS}	-280	270	mA
Pulsed drain current	I_{DM}	-4	3	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Power dissipation at T_{amb}=25 ^{0}C	P_{tot}	700	625	mW
Operating and storage Temperature range.	T_j; T_{stg}	-55 to 150	-55 to 150	^{0}C

The devices Q1 and Q2 in figure 2.2 should be of higher breakdown voltage to withstand the higher voltages to produce the higher clock pulses. Q1 and Q2 are ZVP2120A and ZVNL120A respectively [14], [15].

Table 3.2: Maximum ratings of the high voltage PMOS and NMOS Devices.

PARAMETER	SYMBOL	VALUE		UNIT
		PMOS ZVP2120A	NMOS ZVNL120A	
Drain-Source Voltage	V_{DS}	-200	200	V
Continuous drain current at T_{amb}=25 ^{0}C	I_{DS}	-120	180	mA
Pulsed drain current	I_{DM}	-1.2	2	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Power dissipation at T_{amb}=25 ^{0}C	P_{tot}	700	700	mW
Operating and storage Temperature range.	T_j; T_{stg}	-55 to 150	-55 to 150	^{0}C

The clocks produced at CLKHV and CLKHVI nodes in the schematics of figure 2.2 are 200V clock pulses. These clocks are produced by using another level shifting circuit. A 12V- 200V DC/DC converter is used as a voltage source in this second level shifting circuit.

The simulated values for the high voltage clock signal are shown in figure 3.10:

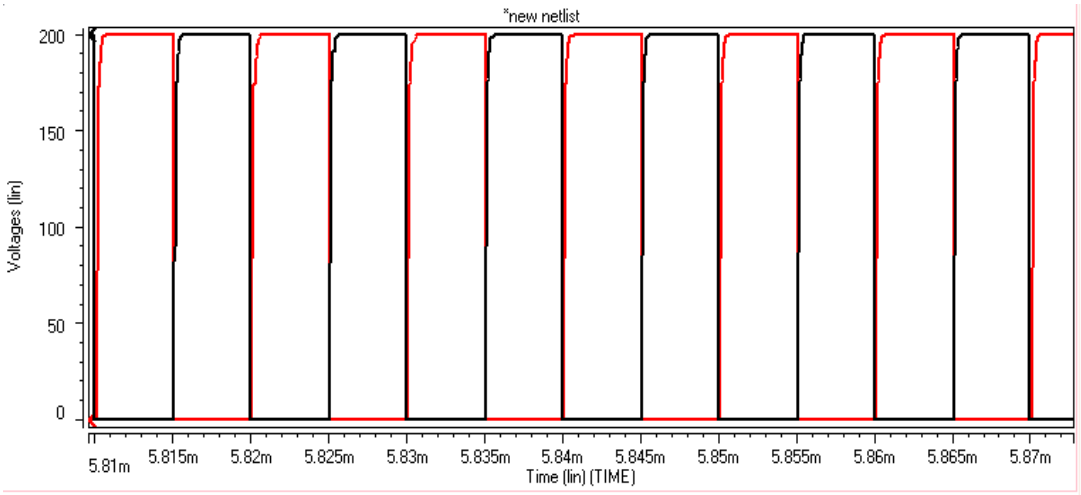

Figure 3.10: Simulated values of CLKHV and CLKHVI.

As seen in the figure above, the clocks produced are non-overlapping clocks. These complementary clocks are used with the voltage multiplier circuit to produce a high voltage. The non-overlapping clock generation is a critical issue as it can greatly affect the efficiency of the charge pump.

Charge Pump Circuit

Operation

The charge pump seen in figure 3.11 works on the principle of pumping the voltage through each stage of a diode-capacitor pair [6]. The number of stages required is dependent on the output voltage required. Initially when CLKHV is low diode D1 is forward biased and the voltage on node 1 is equal to V_{DD} - V_d (say it is around 199V, where V_d is the forward bias voltage of the diode). Now when CLKHV goes high from 0 to V_{DD}, then the voltage on node1 goes up to (V_{DD}-V_d) + V_{DD}, i.e. the voltage now rises up immediately to 399V. This makes the diode D2 forward biased. The voltage on node 2 becomes (V_{DD} - V_d) + V_{DD} – V_d. When CLKHVI goes high in the next cycle, then the voltage on node 2 goes to 2. (V_{DD} - V_d) + V_{DD} which is equal to 599V.So this cycle repeats until the voltage on the output capacitor reaches to N. (V_{DD} -V_d) + V_{DD}. The number of diode-capacitor pairs used in the circuit is 9. The load resistance used here are discrete resistors used in place of the load resistance in the IMS.

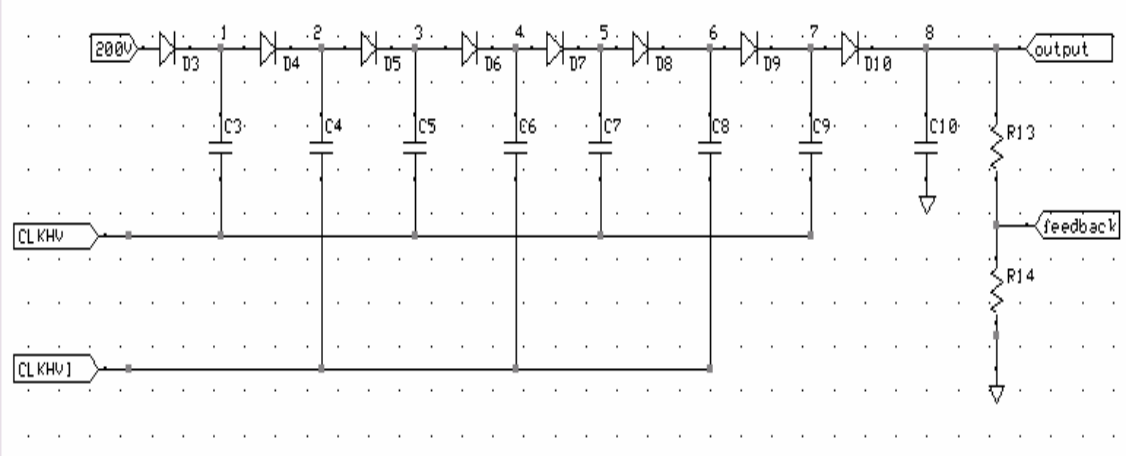

Figure 3.11: Charge pump circuit.

A voltage divider is used so as to cut the output signal down and is fed back to the PIC. The PIC controls the frequency of the input clock and hence the output voltage is well regulated at the desired value.

The diode used here is selected so as to have a high reverse bias breakdown voltage and a very low forward bias voltage so as to increase the efficiency of the charge pump circuit. The lower the forward bias voltage the higher the output voltage generated. Specifications of the diode are as shown in table 3.3 [16].

Table 3.3: Specifications of the diode 1N4004.

Parameter	Symbol	Value	Units
Forward voltage @ 1A	V_F	1.0	V
Total Capacitance V_R=4V and f=1MHz.	C_T	15	pF
Peak Repetitive reverse voltage	V_{RRM}	400	V
Maximum full load reverse current	I_{rr}	30	uA
Power Dissipation	P_D	3	W

The final output voltage derived from the circuit shown in figure 3.11 is 2000V and the simulation results are shown in figure 3.12 and 3.13. This signal is used as a feedback to the PIC.

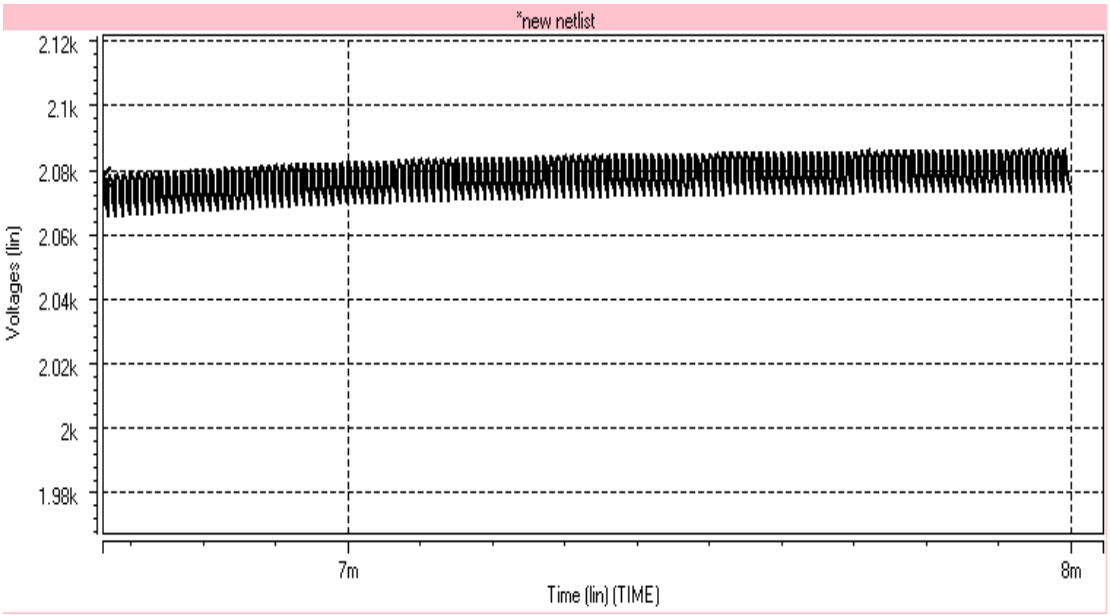

Figure 3.12: Output voltage of the charge pump circuit.

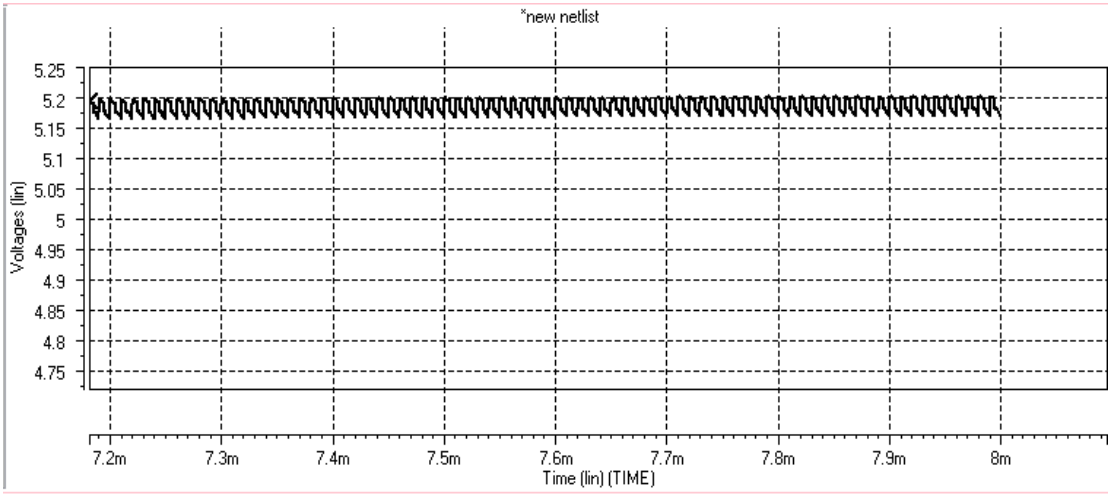

Figure 3.13: Output voltage at the voltage divider. (A 20meg: 50k divider).

CHAPTER 4. LAYOUT AND EXPERIMENTAL PROCEDURE

Layout of the Printed Circuit Board

Having done all the SPICE analysis for the circuit, the layout of the circuit was made using EXPRESS PCB software. This is free software available at www.expresspcb.com. The figure 4.1 is a plot of the lay out of the Printed Circuit Board (PCB) designed.

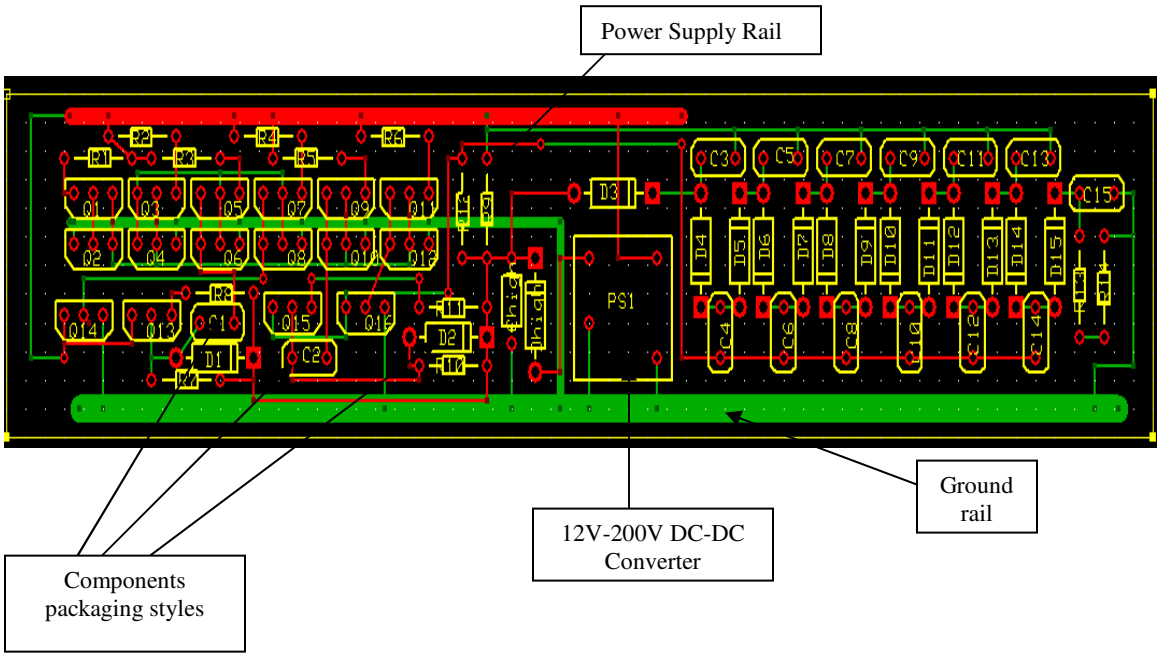

Figure 4.1: Layout of the Printed Circuit Board (PCB).

The ground strap at the bottom as labeled in figure 4.1 is laid on the rear side of the PCB. It is made wide enough to decrease the resistance and hence to eliminate ground bounce. The power supply rail at the top is placed on the front side of the PCB. The outlines of the components represent the packaging styles.

Packaging information of the components used is shown in table 4.1.The lay out of the PCB was designed using the packaging information.

Table 4.1: Packaging information of the components.

Component Type	Component used	Packaging type
NMOS	ZVN3306A	E-Line TO-92 Compatible
PMOS	ZVP2106A	E-Line TO-92 compatible
NMOS	ZVNL120A	E-Line TO-92 compatible
PMOS	ZVP2120A	E-Line TO-92 compatible
Diode	D1N4004	DO-41
Power Supply	PICO-12A200S	0.5" x 0.5" x 0.3" Height

The size of the PCB is 1.2 inches X 6 inches, which meets the design specifications of the IMS. There is also enough space at the end of the PCB, to increase the number of diode-capacitor stages if the chemical engineers require a higher voltage.

The final Printed Circuit Board (PCB) after printing looks as in figure 4.2.

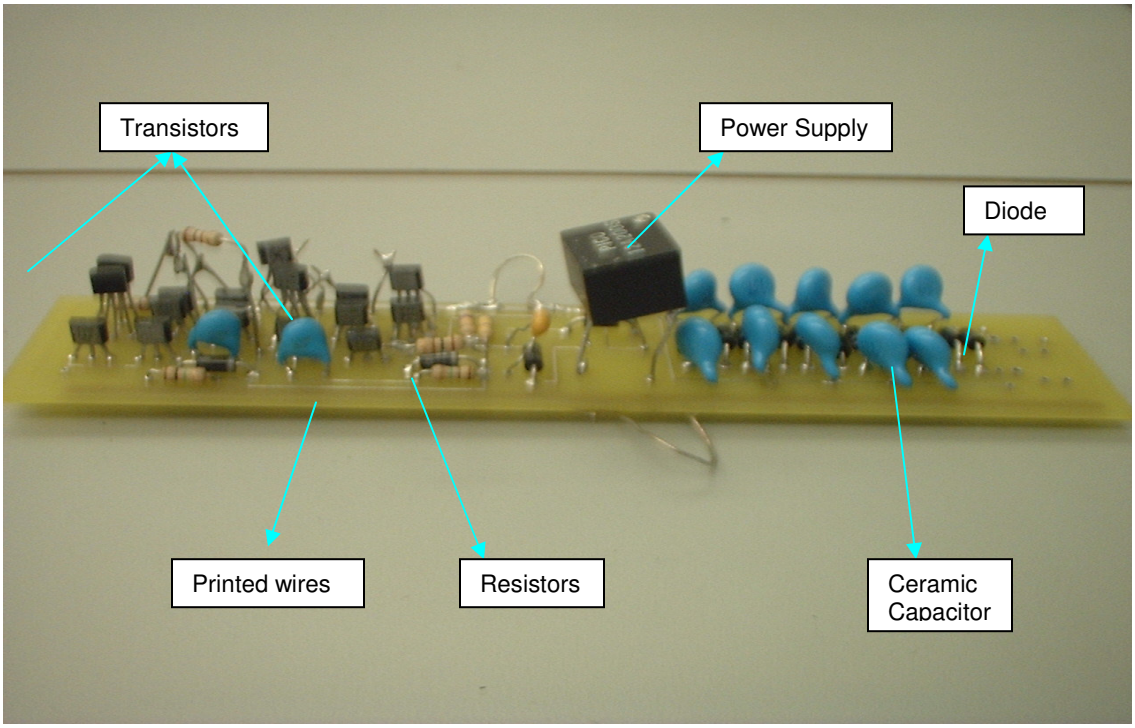

Figure 4.2: Picture of the final Printed Circuit Board with components.

The transistors to the left constitute the level shifting circuit.

The tall surface mounted device is the 12V-200V DC-DC converter power supply.

The ceramic capacitors together with the diodes to the right form the charge pumping circuit.

Experimental Procedure

The PCB tested has exhibited good results, which also agreed with the simulations. The testing procedure can be explained in the following steps:

(1) Set the output of the DC power supply to +12V before connecting it to the PCB voltage rails. After setting it to the correct value, turn off the output switch. This ensures that the voltage will not be applied to the rail even if it is connected.

(2) Set the frequency, offset, amplitude and the shape of waveform to 500KHz.2.5V, 5V and square wave in the function generator. After setting them to the correct value switch off the power button of the Function generator.

(3) Make sure the multimeter and oscilloscope are ready to use and test the circuit.

(4) The DC power supply and the function generator outputs are connected to the PCB.

(5) The 1 Meg probe of the oscilloscope is connected to the desired nodes.

(6) CAUTION: Proper care must be taken to not to connect the probes to high voltage nodes.

(7) High voltage nodes must be measured using only a high voltage probe with a very high output resistance.

(8) The respective voltages and reading are noted.

(9) Care should be taken to limit the frequency according to the supply current. The amount of current drawn by the supply can be read out directly from the DC supply source. Excess current means excess power (for a fixed voltage).

Table 4.2 describes the different components and their function. A picture of the apparatus used is shown in figure 4.3.

Table 4.2: Apparatus used to test the Printed Circuit Board.

Apparatus Name	Type	Function
Multimeter	HP 34401A	Used to probe and investigate voltage, currents and resistances between nodes.
Function generator	HP 33120A	To generate a pulse waveform which is used as the input of the PCB.
DC power supply	HP E3631A	To provide DC voltage.
Oscilloscope	HP infinium	Displays a waveform.
Soldering station	AUTO-TEMP 379	Used to solder lead and fix the components in the PCB.

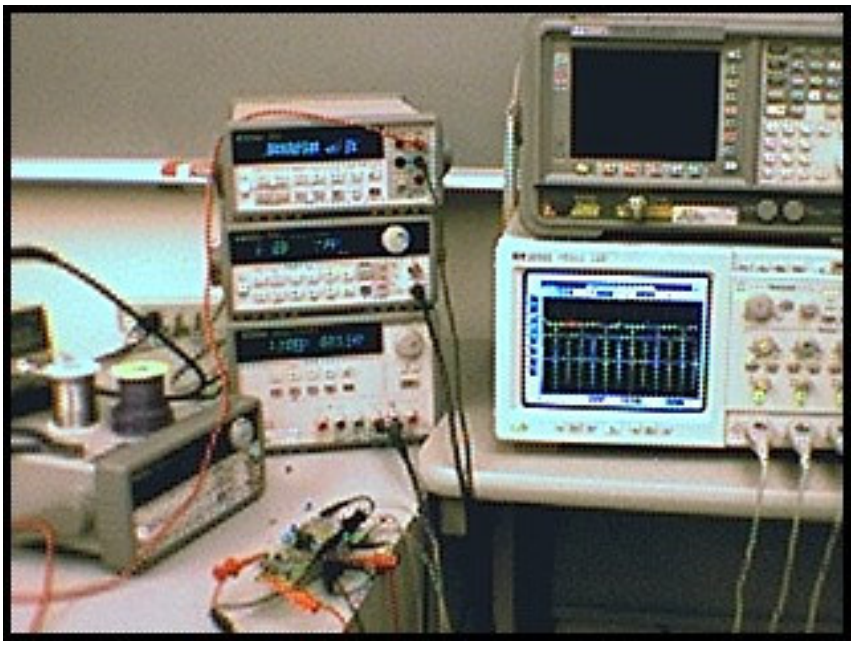

Figure 4.3: Picture showing the apparatus used to test the PCB.

Results

The results in figure 4.4 can be interpreted as:

2000V High voltage output: Since the oscilloscope cannot measure such a high voltage, a voltage divider was used to measure the output voltage.

Non-overlapping 200V clock pulses: The measurements shown in the figure are non-overlapping clock pulses. The input frequency from the function generator was set to 50KHz that is equal to a 20us time period as can be seen from the measurements shown below. As seen from figure 4.4, non-overlapping clock and 2000V output were generated. However non-overlapping clocks are not a critical issue for the Dickson charge pump.

As the load resistance increases, the input clock frequency must be decreased to obtain the same output voltage. The load resistances and the input frequencies were changed to obtain the same output voltage of 2000V. The plots for obtaining a 2000V and 1100V output are shown in figures 4.5 and 4.6 respectively.

The measured outputs are as shown in figure 4.4.

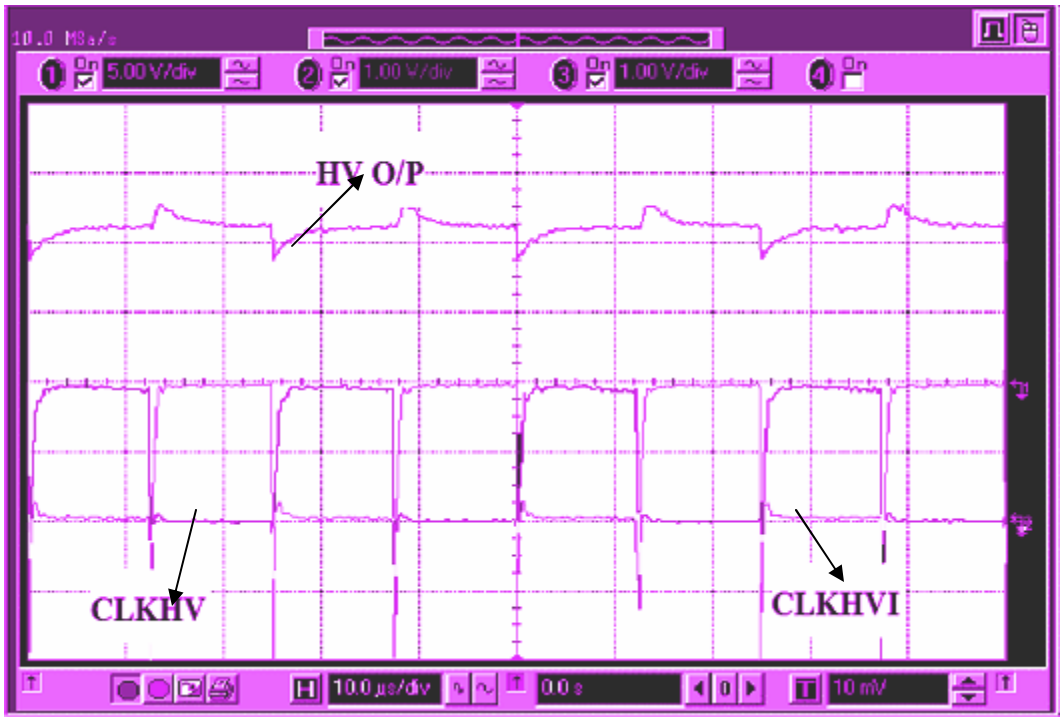

Figure 4.4: Snap shot of the measured results from the oscilloscope.

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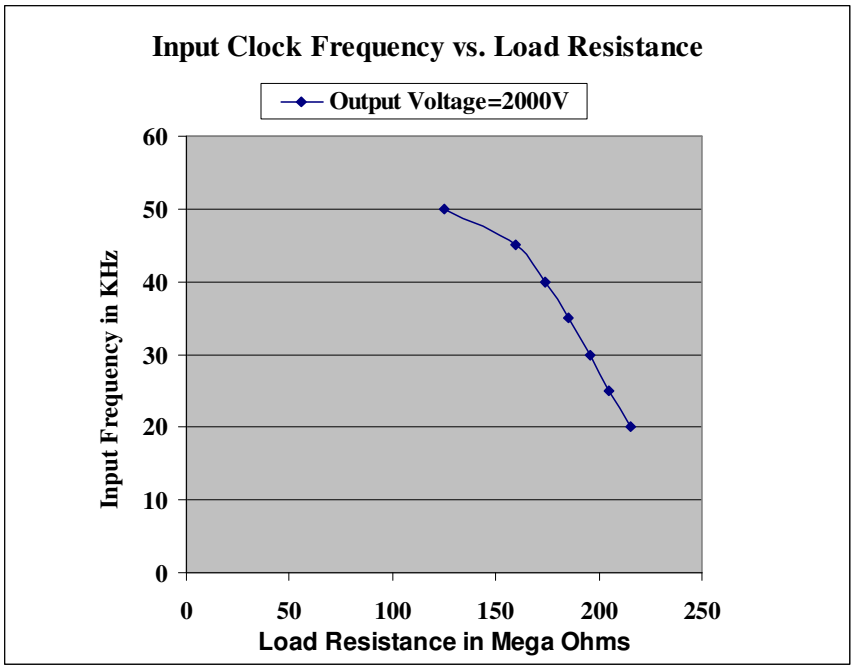

Figure 4.5: Load resistance versus frequency with 12 stages.

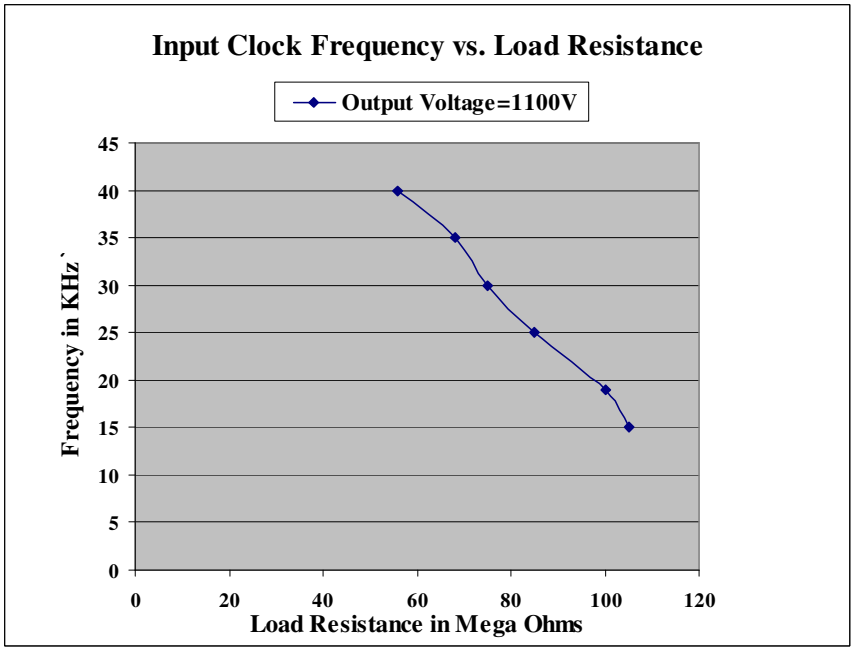

Figure 4.6: Frequency vs. load resistance with 7 stages.

CHAPTER 5. PERFROMANCE, DESIGN AND RESULTS

The charge pump discussed so far is a model of the Dickson's charge pump [11]. The output voltage generated for an 'N' stage charge pump is estimated in the following discussion.

For simplicity it is assumed that the forward voltage drop of the diodes is equal to zero and the power supply voltage is V_{DD} (V_{DD}=200V). It is also assumed that all the stages have equal capacitances. The calculations shown below are referred to figure 5.1.

When CLKHV is low, the diode D1 is forward biased and the voltage at node 1 is given by $V_{DD} - V_d$ where V_d is the forward bias voltage of the diode, but as it is assumed that the voltage drop would be zero, the voltage at node 1 can be estimated as V_{DD} (200V).

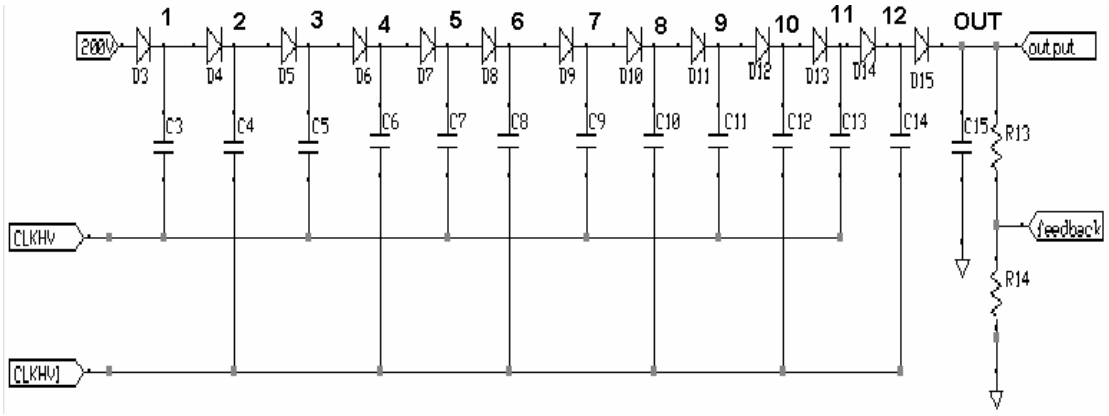

Figure 5.1: 12-stage charge-pump circuit.

When CLKHV goes high (from 0 to V_{DD}), the voltage at node 1 is now $2.V_{DD}$. This turns ON the diode D2; hence the voltage at node 2 is given by $2.V_{DD}$.

When CLKHVI goes high, the voltage at node 'N'is given by

Voltage at node 'N', $V_N = (N+1).V_{DD}$ .....(5.1)

Since there is a resistor at the output, which is in parallel to the output capacitor, there, is always a load current flowing at the output node. This is due to the discharging of the capacitor through the resistance when CLKHVI is low.

The voltage drop on the node of the capacitor for one clock cycle is given by:

$$V_{discharge} = \frac{N.I_L}{f_{osc}.C_{out}} \quad \text{.....(5.2)}$$

Where N= Number of stages

F_{osc} = Frequency of input clock

C_{out}= Output or load capacitance

I_L= Load current. The load current can be calculated as:

$$I_L = \frac{V_{output}}{R_{load}} \quad \text{.....(5.3)}$$

Where V_{output} = Output voltage

R_{load} = Load resistance.

So the overall or effective output voltage is given by:

$$V_{output} = V_N - V_{discharge} \quad \text{.....(5.4)}$$

$$V_{output} = (N+1).V_{DD} - \frac{N.I_L}{f_{osc}.C_{out}} \quad \text{.....(5.5)}$$

Substituting the below shown values in the above equation,

$V_{output} = 2000V$

$V_{DD} = 200V$

$$I_L = \frac{V_{output}}{R_{load}} \cong \frac{2000}{40Meg} \cong 50uA$$

F_{osc}=50KHz

C_{out}=100pF

The maximum input clock frequency is observed to be 75KHz at a load resistance of 48 MΩ and for a supply voltage of 12V. It is seen that a minimum of '9' stages is required to obtain the required output voltage of 2000V. Since there are many losses due to parasitic effects, here a 12-stage charge pump was built to make the design flexible according to the requirements.

From equation (5.5) the following conclusion can be made:

(1) The output voltage increases with increase in frequency. But it will stay almost a constant after the frequency has reached a threshold value because the second term is negligible for higher frequencies.

(2) Output voltage increases with an increase in the number of stages.

(3) Output voltage also increases with a decrease in the output capacitance. However, this increase the ripple voltage on the output due to quick discharge time of the R-C output network. Maintaining a low ripple voltage with a lower output capacitance can be achieved by increasing the load resistance.

(4) Increasing the supply voltage V_{DD} can also increase the output voltage but this in turn reduces the power efficiency of the circuit [9].

The simplicity in equation (5.5) was achieved by neglecting the forward bias voltage drop of the diode, which is around 1V, and also by neglecting the parasitic (stray) capacitances. In the case of the presence of the parasitic capacitances, the charge sharing between the capacitors at the rising and falling edges of the clocks is reduced and hence further degrades the performance of the circuit.

Output Voltage variation with Number of Stages

The output voltage is mostly dependent on the number of stages used in the multiplier circuit. As the number of stages increases, the output voltage also increases. The voltage increase is basically due to increase of the charge being stored in each capacitor. Figure 5.2 shows the output voltage variation with the number of stages. This mechanism is explained by the charge sharing principle explained in Appendix A.

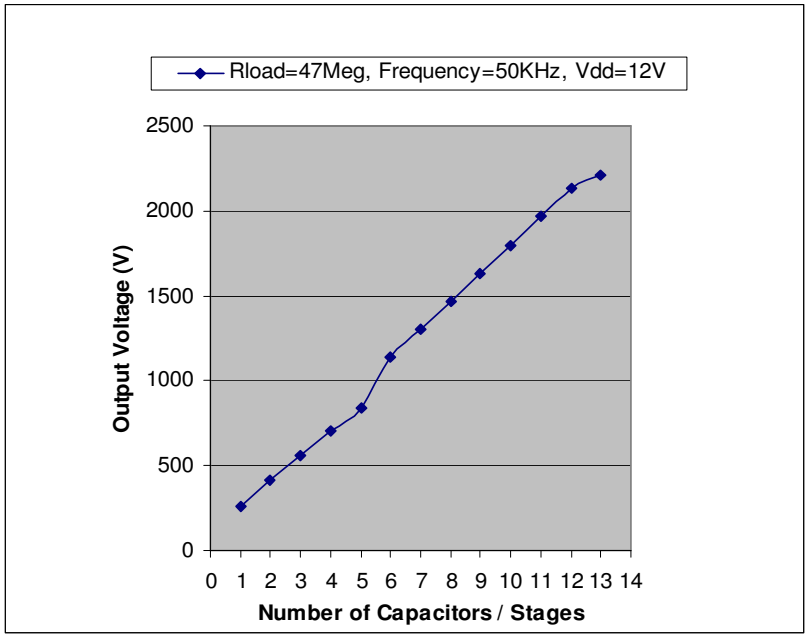

Figure 5.2: Output voltage vs. number of stages

Output Voltage Variations with Frequency

As the input clock frequency increases, the charge sharing in multiplier circuit becomes more prominent and hence the output voltage tends to increase initially [7]. Also the increased frequency accounts to compensate the decrease in voltage due to the discharging of the output capacitor through the load resistance.

As seen from equation (5.5), the output voltage increases with frequency up to a certain extent and there after remains a constant.

However if the frequency is very high, then if the finite rise time becomes more than the time period of the clock, the output of the inverter will not be charged to the supply voltage and hence the output clock generated will be lower in amplitude [3]. This results in a gradual decrease in the output voltage above a certain frequency. This can be seen in figure 5.3. The above discussion is presented in the plot shown below. The load resistance used is 38MΩ.

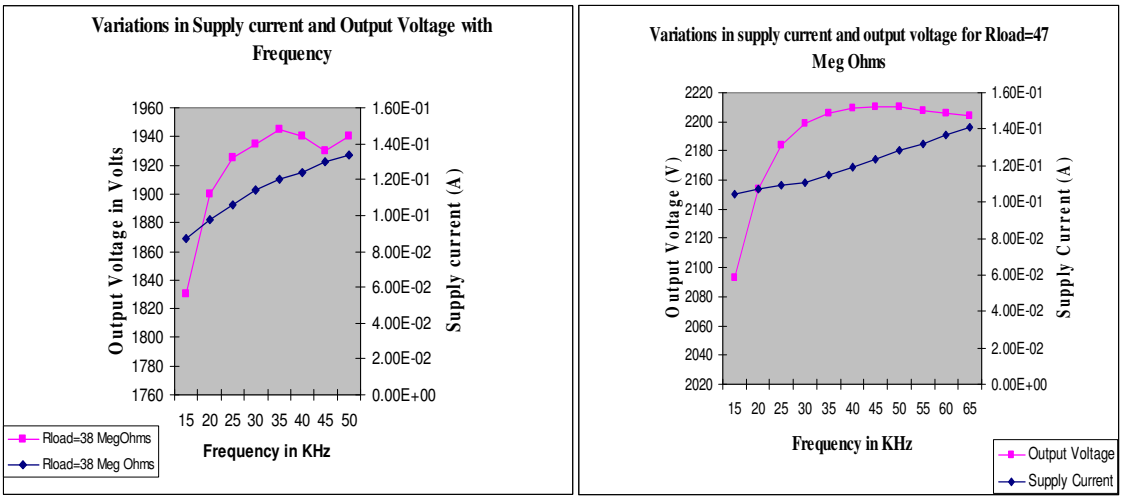

Figure 5.3: Variations in output voltage and supply current with frequency.

Output Voltage Variations with Supply Voltage and Switching Frequency

The 12A200S power supply, which needs a 12V input, produces a 200V output. As the input voltage to this supply is changed, the output voltage also changes proportionally. The plots in figure 5.4 show the change in overall output voltage of the circuit with changes in supply voltage. Decreasing the supply voltage tends to decrease the supply current through the circuit and hence the overall efficiency performance can be increased [10].

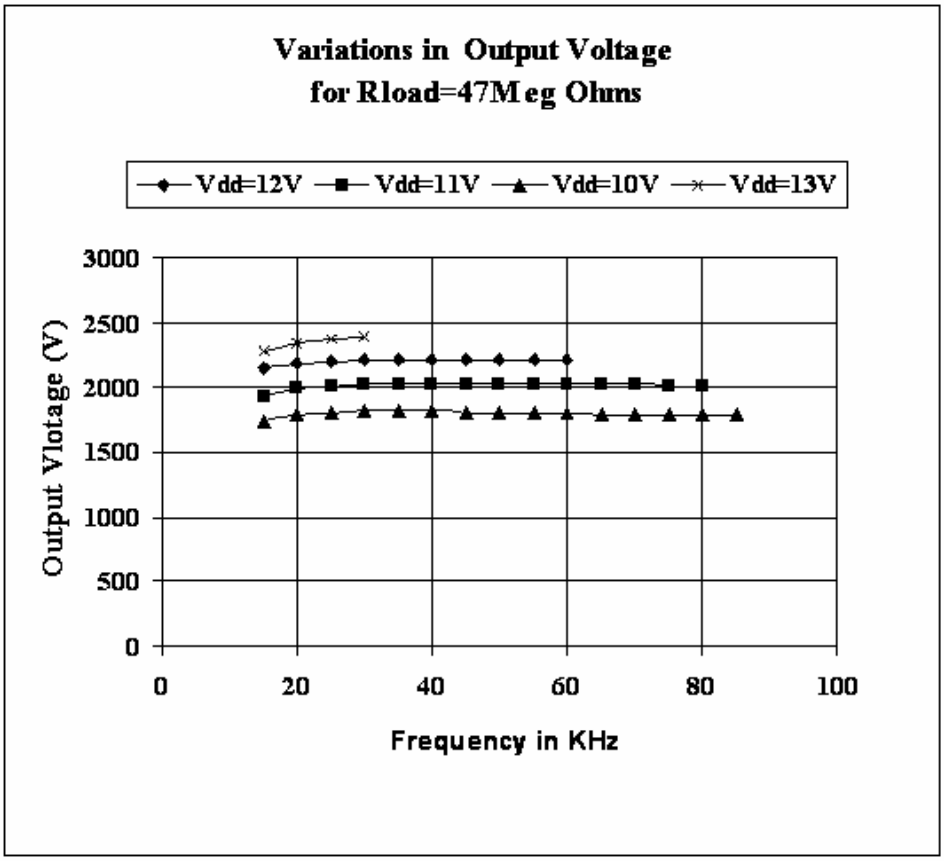

Figure 5.4: Variations in output voltage with frequency and Vdd.

Variations in Supply Current with Frequency and Supply Voltage

As the frequency is increased, the inverter switching frequency increases and the average current drawn by the inverters increases. Though an increase in frequency might lead to an increase in output voltage, the simultaneous increase in supply current may degrade the efficiency of the circuit. Changes in supply current with frequency are again shown in figure 5.3.

However if the supply voltage is changed, the current drawn by the external circuit also decreases which might lead to an increase in the efficiency. Changes in the supply current with supply voltage and frequency are shown in figure 5.5.

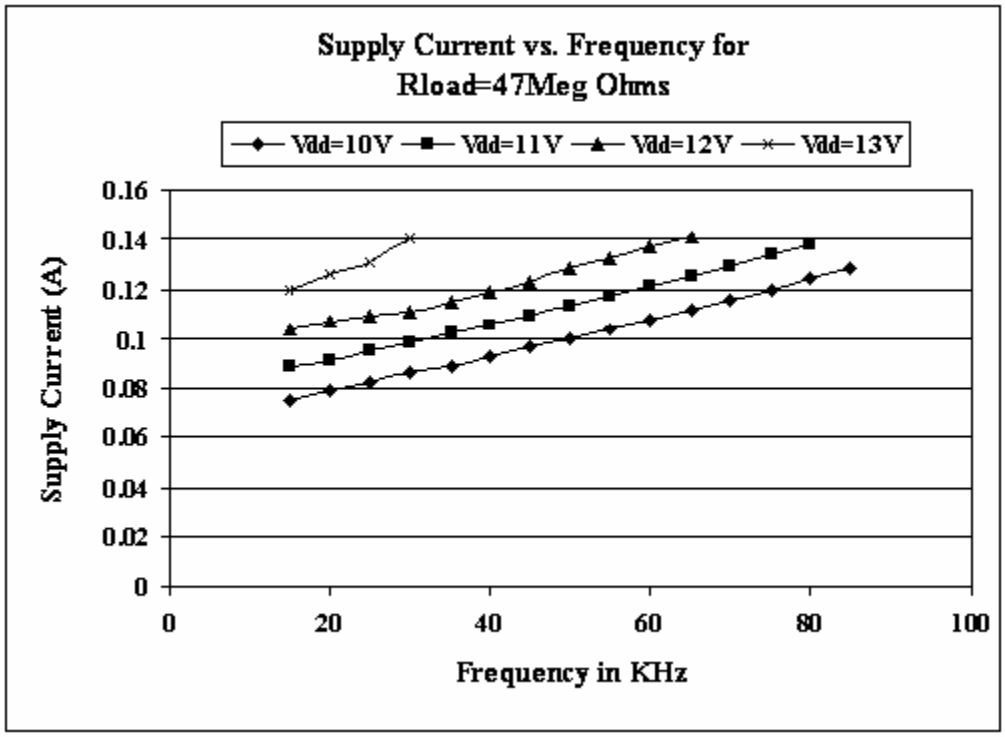

Figure 5.5: Supply current variations with supply voltage.

Power Efficiency of the Charge-Pump Circuit

The power efficiency of the circuit can be defined as the ratio of the power delivered to the load to the total power supplied by the source [7]. Mathematically it can be written as:

$$\%\eta = \frac{V_{load}.I_{load}}{V_{DD}.I_{DD}}.(100) \quad \text{.....(5.6)}$$

Where η=power efficiency

V_{load} = Output voltage at the load

I_{load} = Current supplied to the load

V_{DD} = Supply voltage

I_{DD} = Current supplied by V_{DD}

The power efficiency of the charge pump is also directly dependent on the 12V-200V DC-DC converter. The charge pump is powered by an off-the-shelf 200 V power supply. The power efficiency of this power supply is 78% at full-load [10]. The power supply used was a 12A200S device [10].

Figures 5.6 and 5.7 show the variation in power efficiency of the charge pump circuit with frequency at different load conditions. The power efficiency of the charge pump circuit with 12 stages for a load resistance of 38MΩ and 47MΩ are analyzed. It is seen that higher load resistance have higher efficiency when compared at the same input clock switching frequency.

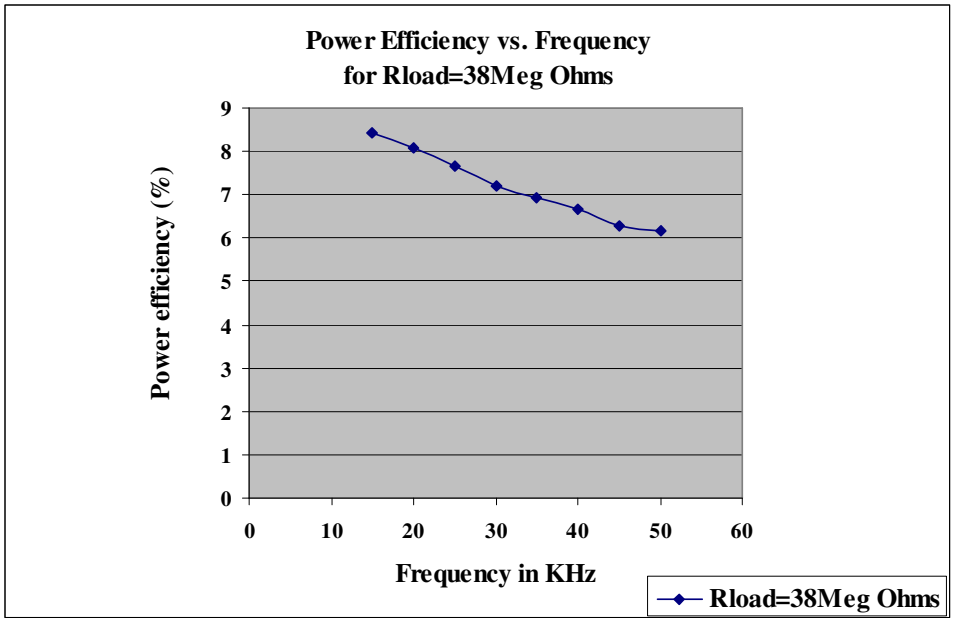

Figure 5.6: Power Efficiency vs. frequency for a load resistance of 38Mohms.

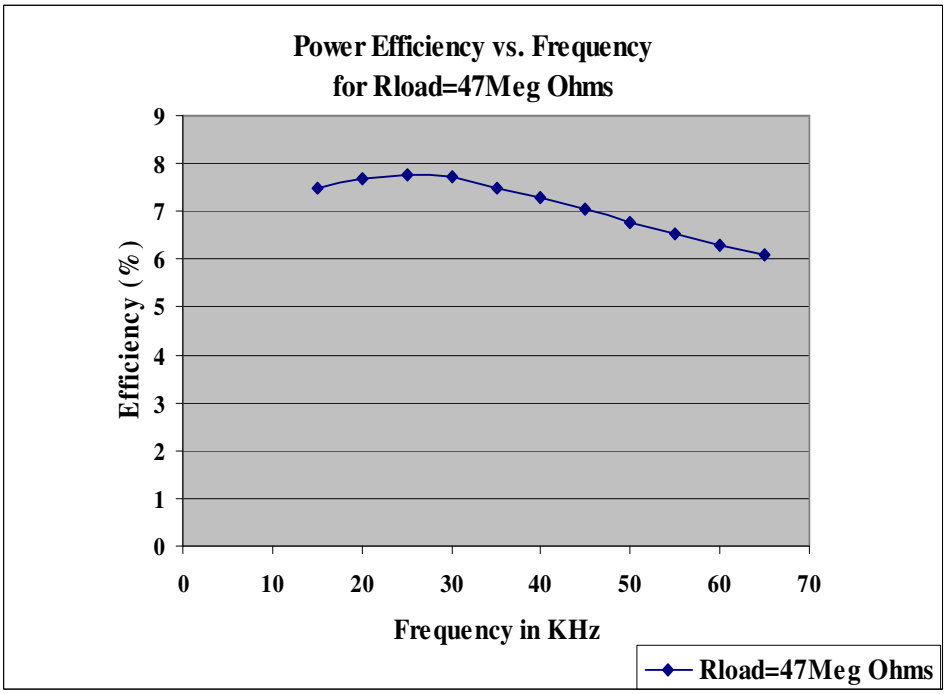

Figure 5.7: Power efficiency vs. frequency for a load resistance of 47Mohms.

Variations in Power Efficiency with Supply Voltage

It is seen form the plot in figure 5.8, that initially the lower supply voltages dominate the plot but eventually they all have the same power efficiency [8]. The draw back of using lower supply voltages is reduced output voltages. Since there is not much difference in the power efficiencies, the supply voltage can be fixed to 12V.With V_{DD}=13V, the power efficiency becomes more worse.

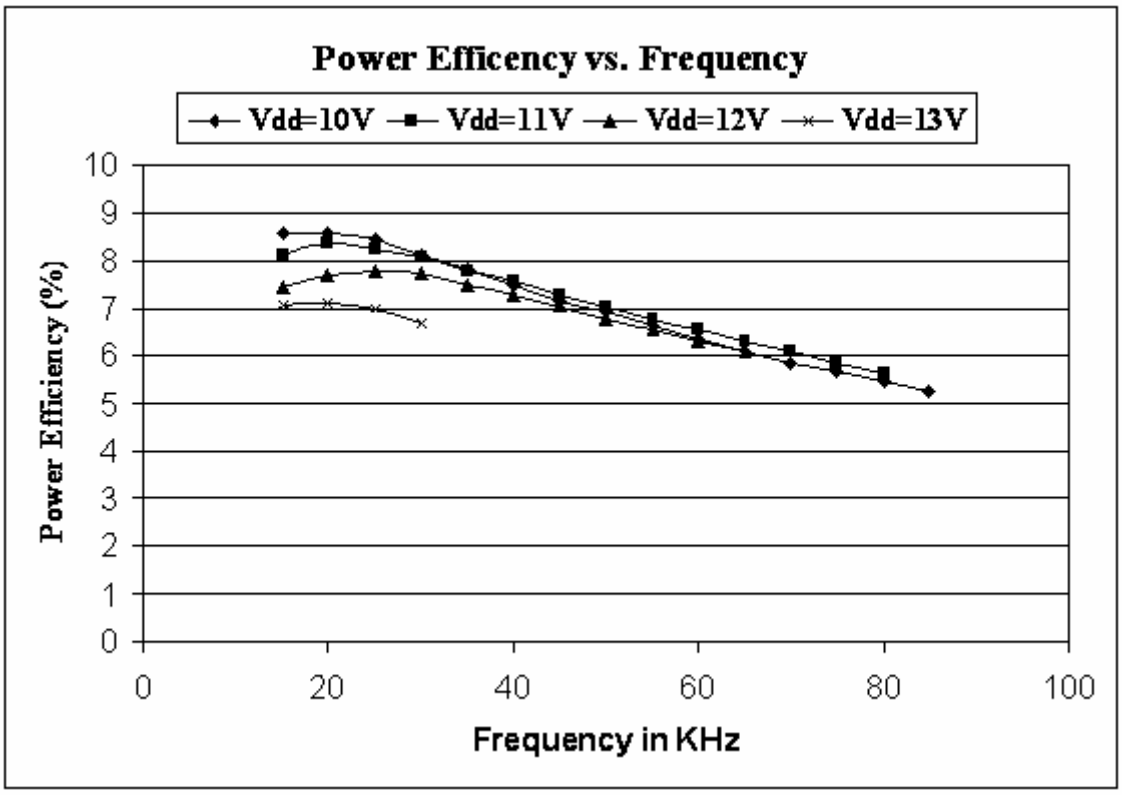

Figure 5.8: Variations in Efficiency with frequency and supply voltage.

Conclusion

A charge pump circuit with a size of 1.2" x 6" was built and tested. The voltage multiplier is based on simple Dickson charge pump principle. A level translator circuit is used to convert the 5V clock input to a 200V clock pulse.

The output voltage was linearly increasing with increase in number of stages (diode-capacitor pairs) as seen in figure 5.2. Power consumed by the circuit is 1.25W and the output voltage generated with this prototype is 2000V. Typical clock frequencies vary between 10-100KHz depending upon the load resistance. Power efficiency of the charge pump circuit is around 9%. Low power efficiency can be attributed to the power loss in the level translator circuit and 12A200S DC-DC converter. The charge pump circuit exhibited good tolerance to supply voltages and load resistances.

Future Work

Further modifications to the level translator circuit should be made to increase the overall power efficiency. Higher clock frequencies can be applied by decreasing the series resistance in the inverter block of the level translator circuit as seen in figure 2.3. The feedback circuit for the charge pump controlling the frequency of the input clock signal should be designed.

APPENDIX A

DEVICE CHARACTERISTICS AND R-C CIRCUITS

Characteristics of the ZVN3306A NMOS Device

Transconductance Characteristics

The simulations shown below were carried out in Win SPICE

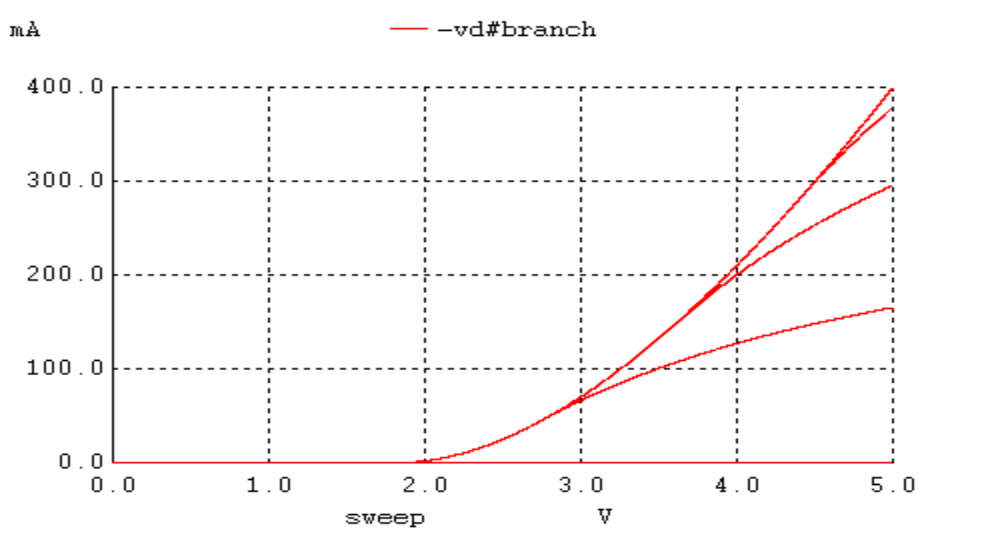

Figure A.1: Transconductance characteristics of the ZVN3306A device for V_{GS}=0,1,2,3,4 and 5V.

Output Characteristics

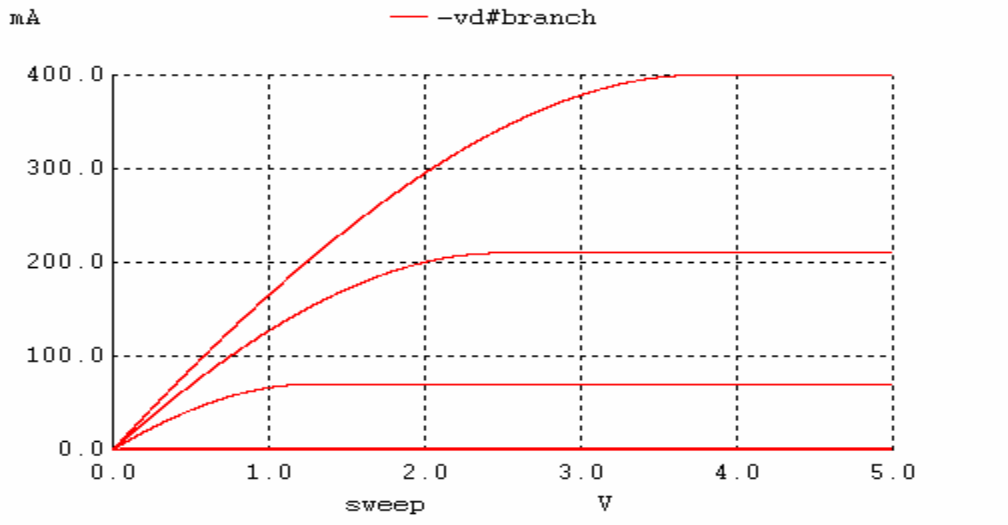

Figure A.2: Output characteristics of the ZVN3306A for V_{DS}=0,1,2,3,4 and 5V.

Characteristics of the ZVP2106A PMOS Device

Transconductance Characteristics

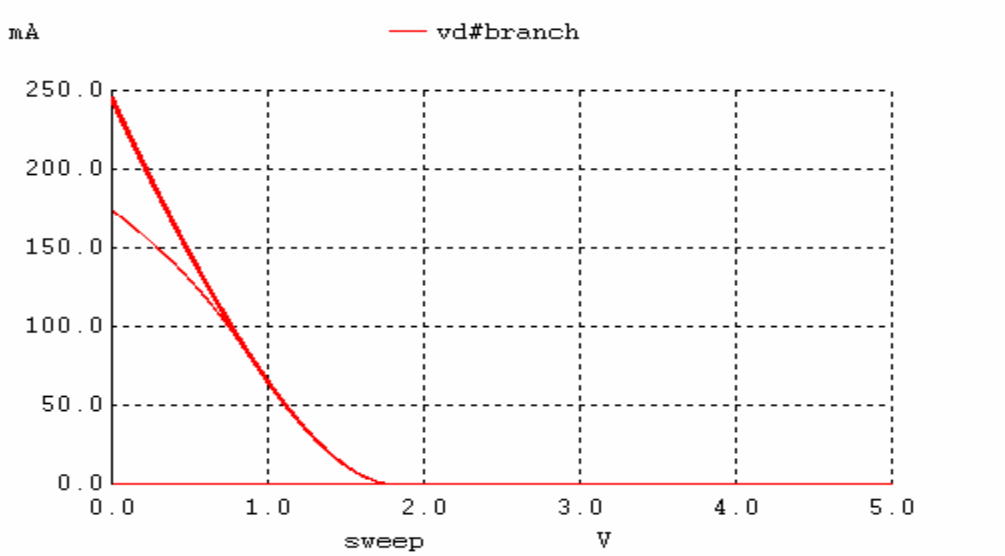

Figure A.3: Transconductance characteristics of ZVP2106A PMOS device for V_{SD}=0,1,2,3,4 and 5V.

Output Characteristics

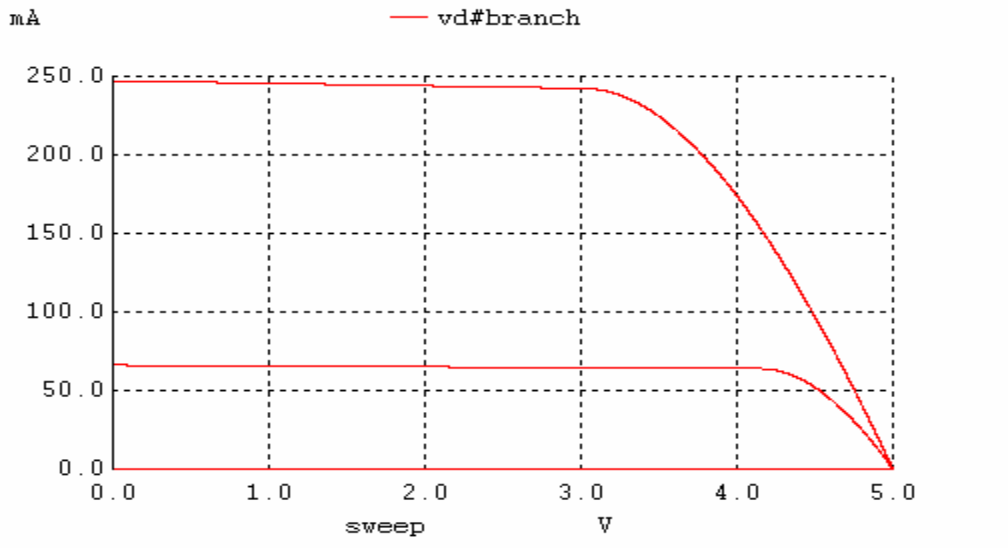

Figure A.4: Output characteristics of the ZVP2106A for V_{SG}=0,1,2,3,4 and 5V.

Characteristics of the ZVP2120A PMOS Device

Transconductance Characteristics

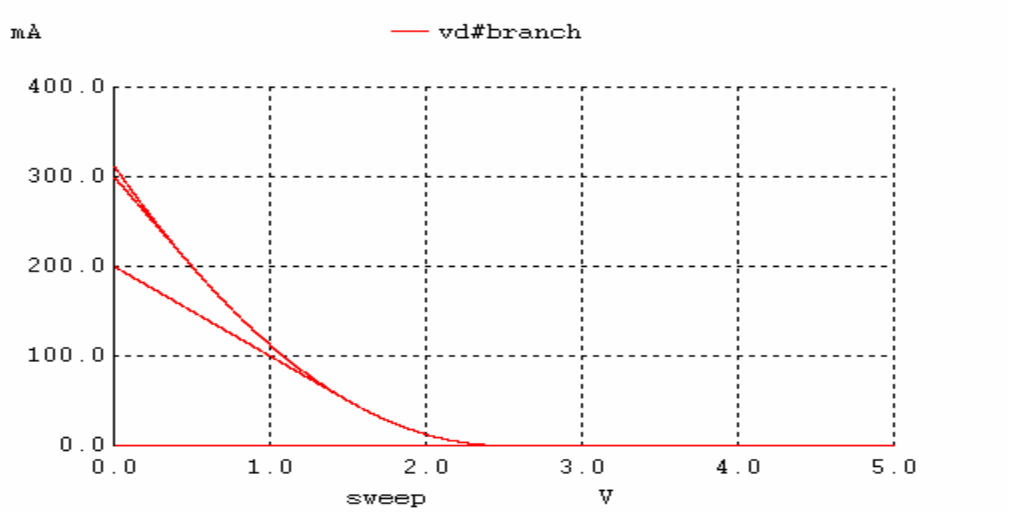

Figure A.5: Transconductance characteristics of the high voltage PMOS device for V_{SG}=0,1,2,3,4 and 5V.

Output Characteristics

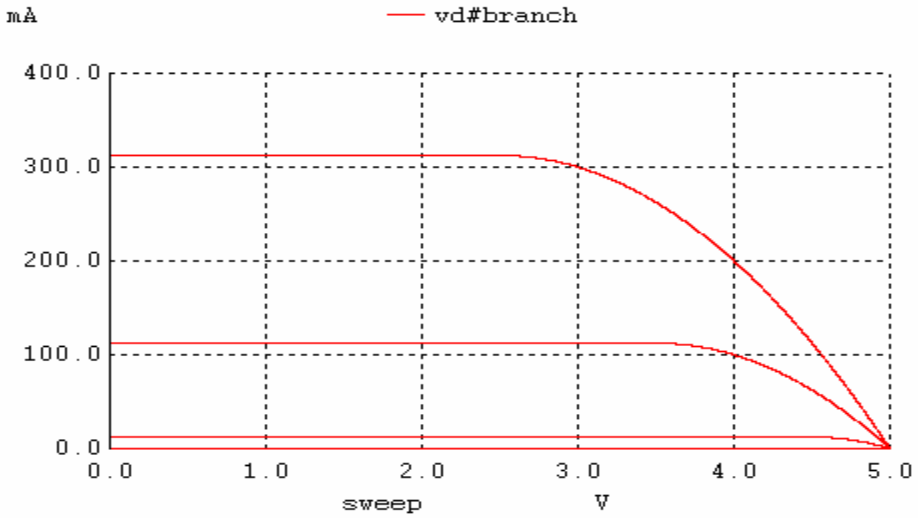

Figure A.6: Output characteristics of the ZVP2120A device for V_{SG}=0,1,2,3,4 and 5V.

Characteristics of the ZVNL120A NMOS Device

Transconductance Characteristics

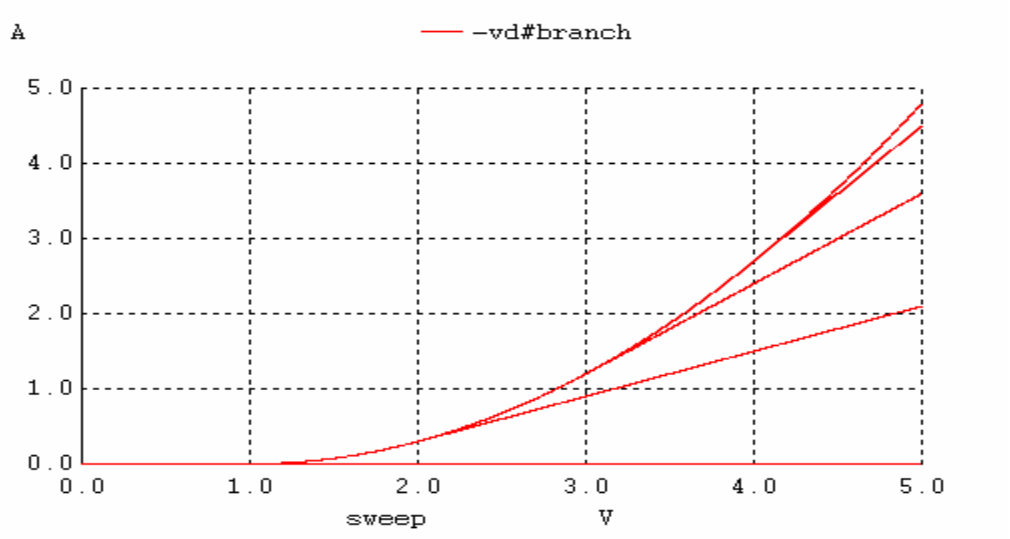

Figure A.7: Transconductance characteristics of the ZVNL120A for V_{DS}=0,1,2,3,4 and 5V.

Output Characteristics

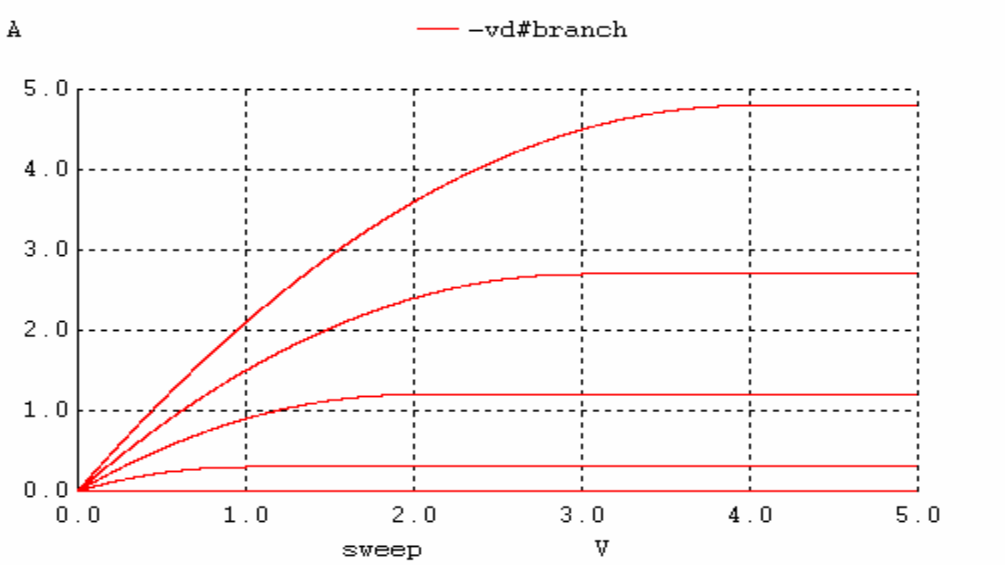

Figure A.8: Output Characteristics of the ZVNL120A NMOS device for V_{GS}=0,1,2,3,4 and 5V.

R-C Networks

Rise Time: Time taken for the output voltage to rise from 10% to 90% of the input voltage is defined as the rise time [3].

Fall Time: The fall time is defined as the time taken for the output to fall from 90% of the input value to 10% of the input value [3].

Time Constant: The product of the resistance and the capacitance value is called the time constant of the simple R-C network. The time constant for a circuit varies depending on the network components [3].

Equation governing charging of the capacitor:

$$V_{out} = V_{in}.(1 - e^{-\frac{t}{R.C}}) \quad \text{.....(A.1)}$$

Equation governing the discharging of the capacitor:

$$V_{out} = V_{in}.e^{-\frac{t}{R.C}} \quad \text{.....(A.2)}$$

Where V_{in}= input voltage, t=time in seconds, R=Resistance in ohms, C=Capacitance in Farads.

Consider the R-C network as shown in the figure A.9.The output of the circuit for R=10K and C=100pF is also shown in the same figure to the right.

In this case Rise time=Fall time=2.5us.

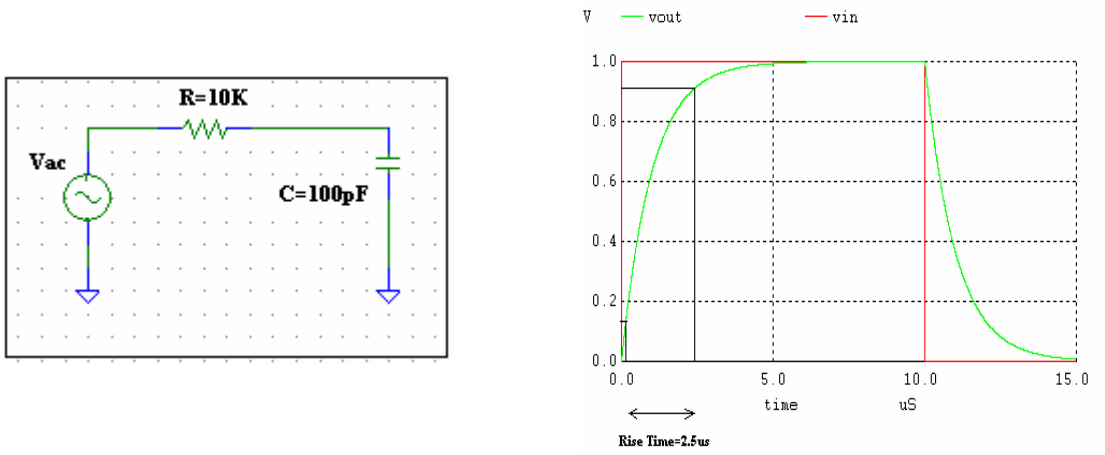

Figure A.9: R-C network to the left and transient response to the right.

Charge Sharing Principle

The charge sharing principle is basically dependent on charge between two capacitors [3]. To better understand this, consider two capacitors in parallel with a switch in between them as shown in figure 44.Assuming voltage on C1 is V1 and C2 is V2 before closing the switch. So the total charge on the capacitors before the switch closes is given by:

$$Q_{before} = C1.V1 + C2.V2 \quad \text{.....(A.3)}$$

Lets say the voltage on the capacitors after the switch closes is V_{final}.

By the law of conservation of charge:

$$Q_{before} = Q_{after} \quad \text{.....(A.4)}$$

$$\Rightarrow \; C_1.V_1 + C_2.V_2 = (C_1 + C_2).V_f \quad \text{.....(A.5)}$$

$$V_f = \frac{(C_1.V_1 + C_2.V_2)}{C_1 + C_2} \quad \text{.....(A.6)}$$

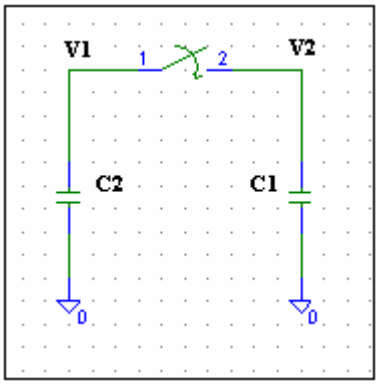

Figure A.10: Charge sharing phenomena between two capacitors**.**

APPENDIX B

SPICE MODELS AND NETLIST

SPICE MODELS

ZVN3306A NMOS DEVICE**:**

```
. SUBCKT    ZVN3306A   3      4      5
*                      D      G      S
M1    3     2     5     5     N3306M
RG    4     2     270
RL    3     5     1.2E8
C1    2     5     28E-12
C2    3     2     3E-12
D1    5     3     N3306D
*
. MODEL N3306M NMOS VTO=1.824 RS=1.572 RD=1.436 IS=1E-15 KP=.1233
+CBD=35E-12 PB=1

. MODEL N3306D D IS=5E-12 RS= 0.768

. ENDS
```

ZVP2106A PMOS DEVICE:

```
. SUBCKT    ZVP2106A   3      4      5
*                      D      G      S
M1    3     2     5     5     MP2106
RG    4     2     160
RL    3     5     1.2E8
C1    2     5     47E-12
C2    3     2     10E-12
D1    3     5     DP2106
*
. MODEL MP2106 PMOS VTO=-3.193 RS=2.041 RD=0.697 IS=1E-15 KP=0.277
+CBD=105E-12 PB=1 LAMBDA=1.2E-2
. MODEL DP2106 D IS=2E-13 RS=0.309
. ENDS
```

ZVNL120A High Voltage NMOS Device:

```
. MODEL     nmoshv     nmos   vt0=1   KP=600u     tox=3e-9
```

ZVP2120A High Voltage PMOS Device:

```
. MODEL      pmoshv      pmos   vt0=-2.5      KP=100u      tox=3e-9
```

High Voltage Diode D1N4004:

```
. MODEL      D1N4004      D
+  IS = 3.699E-09      RS = 1.756E-02      N = 1.774      XTI = 3.0      EG = 1.110
+  CJO = 1.732E-11   M = 0.3353    VJ = 0.3905   FC = 0.5      ISR = 6.665E-10
+  NR = 2.103          BV = 400      IBV = 1.0E-03
```

H-SPICE NETLIST

```
*New   net list

. SUBCKT     INVERTER    VIN    VOUT         VDD
X1      vout     vin      vdd1     ZVP2106A
X2      vout     vin      0        ZVN3306A
R1      vdd      vdd1     200


. SUBCKT     ZVN3306A    3        4        5
*                                 D        G        S
M1      3        2        5        5        N3306M
RG      4        2        270
RL      3        5        1.2E8
C1      2        5        28E-12
C2      3        2        3E-12
D1      5        3        N3306D
*
. MODEL N3306M NMOS VTO=1.824 RS=1.572 RD=1.436 IS=1E-15 KP=.1233
+CBD=35E-12 PB=1
.MODEL N3306D D IS=5E-12 RS=.768
.ENDS

. SUBCKT     ZVP2106A    3        4        5
*                                 D        G        S
M1      3        2        5        5        MP2106
RG      4        2        160
RL      3        5        1.2E8
C1      2        5        47E-12
C2      3        2        10E-12
D1      3        5        DP2106
```

```
*
 . MODEL MP2106 PMOS VTO=-3.193 RS=2.041 RD=0.697 IS=1E-15 KP=0.277
CBD=105E-12 PB=1 LAMBDA=1.2E-2
 . MODEL DP2106 D IS=2E-13 RS=0.309
 . ENDS

. ENDS

Vlow   low    0      dc     12
Dlow   LOW    VDD    D1N4004
CLOW          VDD    0      1UF


VCLOCK       CLOCK  0 DC 0 AC 0 0       PULSE (0 5 4m 1N 1N 5U 10U)


X1     CLOCK        OUTPUT       vdd0   inverter
Xb1    OUTPUT       clk     VDD1        INVERTER
Xb2    clk    clki   VDD2   INVERTER
Xb3    clk    ng     Vdd3   INVERTER
Xb4    OUTPUT       ngp     vdd4        INVERTER
Xb5    OUTPUT       ngn     vdd5        INVERTER

VB0    VDD    VDD0         0
VB1    VDD    VDD1         0
VB2    VDD    VDD2         0
VB3    VDD    VDD3         0
VB4    VDD    VDD4         0
VB5    VDD    VDD5         0

M1     clkhv  n3     hv0    hv     pmoshv       L=1u   W=1000u
M2     clkhv  ng     0      0      nmoshv       L=1u   W=1000u
R2     hv     n3     1MEG
Vd6    hv     hv1    0v
r11    HV1    HV0    200
D100   n3     hv     D1N4004
C2     n3     clki   1000P
R3     hv     clkhv  500k


M3     clkhvi n4     hv3    hv     pmoshv       L=1u   W=1000u
M4     clkhvi ngn    0      0      nmoshv       L=1u   W=1000u
R4     hv     n4     1MEG
Vd7    hv     hv4    0v
R12    HV4    HV3    200
```

```
D101   n4      hv      D1N4004
C3     n4      ngp     1000p
R5     hv      clkhvi  500k

Vhv    High    0       DC      200
DHIGH          high    HV      D1N4004
Cmain  hv      0       10u

*VOLTAGE MULTIPLIER
 Vd5   HV      HV5     0v
 D1    HV5     A       D1N4004
 D2    A       B       D1N4004
 D3    B       C       D1N4004
 D4    C       D       D1N4004
 D5    D       E       D1N4004
 D6    E       F       D1N4004
 D7    F       G       D1N4004
 D8    G       H       D1N4004
 D9    H       I       D1N4004
 D10   I       J       D1N4004
 D11   J       K       D1N4004
 D12   K       L       D1N4004


 C4    A       CLKHV       100PF IC=0
 C5    B       CLKHVI      100PF       IC=0
 C6    C       CLKHV       100PF       IC=0
 C7    D       CLKHVI      100PF       IC=0
 C8    E       CLKHV       100PF       IC=0
 C9    F       CLKHVI      100PF       IC=0
 C10   G       CLKHV       100PF       IC=0
 C11   H       CLKHVI      100PF       IC=0
 C12   I       CLKHV       100PF       IC=0
 C13   J       CLKHVI      100PF       IC=0
 C14   K       CLKHV       100PF       IC=0
 C15   L       0           100PF       IC=0
 R6    L       M           20MEG
 R7    M       0           50K


*. IC   V (n3)=200
*. IC   V (n4)=200

. Tran  1000n  8M      UIC
```

```
. MODEL       D1N4004       D
+ IS = 3.699E-09       RS = 1.756E-02          N = 1.774       XTI = 3.0       EG = 1.110
+ CJO = 1.732E-11  M = 0.3353       VJ = 0.3905    FC = 0.5         ISR = 6.665E-10
+ NR = 2.103             BV = 400       IBV = 1.0E-03


. Model nmoshv nmos vt0=1 KP=600u tox=3e-9
. Model pmoshv pmos vt0=-2.5 KP=100u tox=3e-9
. Model nmoslv nmos vt0=1 KP=60u tox=30e-9
. Model pmoslv pmos vt0=-2.5 KP=10u tox=30e-9

. End
```

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