HIGH SPEED FAST TRANSIENT DIGITIZER DESIGN AND SIMULATION

by

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ABSTRACT

In microelectronics, analog-to-digital converters (ADCs) are used as interfaces to convert analog inputs into discrete time or digital values that can be read via microcontrollers. As speed requirements and processing times in electronics continue to increase, high speed ADCs are increasingly critical components in the design of application-specific integrated circuits (ASICs). However, high speed ADCs introduce quantization error and are inefficient relative to size, cost, and power dissipation when compared to a High Speed Fast Transient Digitizer (HSFTD).

This thesis presents the design, layout, and simulation of a HSFTD designed to sample, in time at a fast rate, a high-speed analog input signal. The reconstructed, captured signal can then be readout at a much slower rate, for example, around three orders of magnitude. This approach eliminates quantization error in the captured signal and allows slow, low cost, analog-to-digital converters to be used such as those found in microcontrollers. The design uses four interleaved sampling banks, each containing 64 unit cells acting as sequentially triggered capture and hold stages with a typical maximum sampling frequency of 17.1 GHz. The capture stages are initiated via four trigger signals separated by a time delay equal to one-fourth of a unit cell propagation delay. The sampling rate can also be adjusted by tuning a bias generator's external control voltage or changing the value of an off-chip bias resistor. The effective sampling rate of 17.1 GHz results in data captured at 58 ps per unit cell with a minimum capture window of 15 ns for all 256 unit cells. The typical analog input voltage range is from 0 V to 2.2 V with an output range from 2 V to 4.8 V. At room temperature, the RMS value of the thermal noise in the design is limited by an

85.75 fF hold capacitor with kT/C noise resulting in a thermal noise floor of 220 µV,RMS. The amount of degradation of the unit cell hold capacitor's voltage over time due to leakage is 2.5 mV/100 µs.

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DEDICATION

To my wife, Wendy.

Thank you for your unconditional love, support, and all the sacrifices you made.

You are mine and I am yours.

I love you.

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CHAPTER 1: INTRODUCTION

1.1 FOUNDATION

High-speed analog waveforms or transient signals are often captured and analyzed for various purposes in a variety of scientific disciplines or application specific electronic designs, including but not limited to laser measurement systems, radar systems, and other high-speed measurement systems. Analyzing the captured high-speed data via electronic components, such as processors or microcontrollers, requires digitization of the analog or transient data via the use of costly, high power analog-to-digital converters (ADCs) capable of converting high frequency signals. ADCs convert analog or transient signals into useful digital values via discretization and quantization.

Discretization, as defined relative to the present discussion, is a process within the ADC that assigns discrete values to externally received analog signals by capturing, or sampling, the signals at periodic intervals, thus allowing a physical system to be modeled digitally [1]. For simplicity, analog signals will be referenced for the remainder of this thesis with the implication that the discussion is also applicable to transient signals, unless noted otherwise. As a general example, consider Figure 1 showing a sinusoidal input signal sampled at a frequency, f_s, with sampled discrete values of 3.6 V, 2.8 V, and 2.0 V. The discrete values are typically compared to a reference value and assigned a digital value, either logic 1, or VDD, or logic 0, or ground, based upon the results of the comparison. This process, known as quantization, allows the discrete values to be precisely represented digitally, but also results in the unfortunate consequence of introducing noise into the discrete value due to inherent rounding during the analog-to-digital

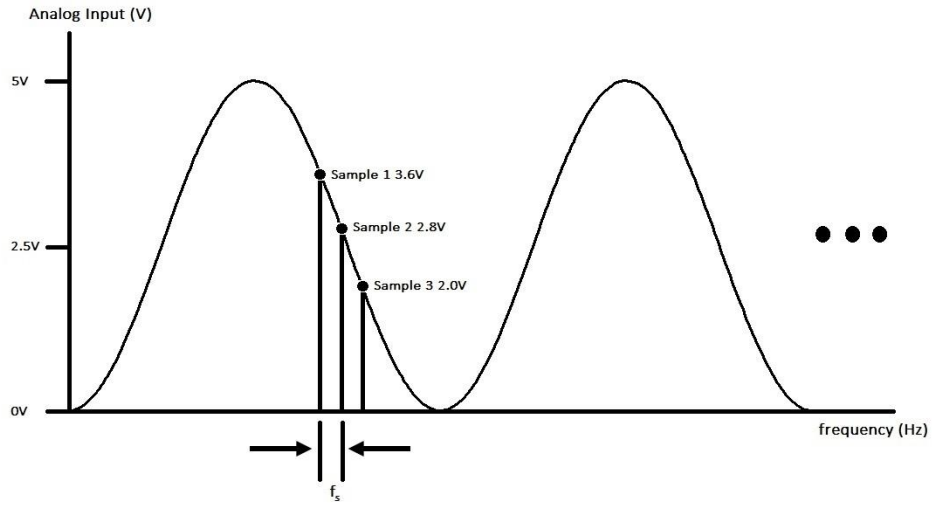
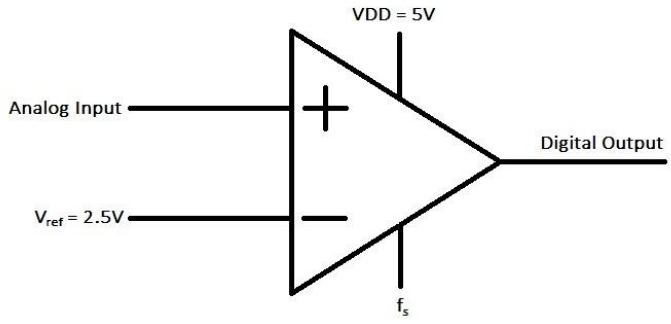


Figure 1 - ADC discretization example

conversion [2]. To demonstrate this effect, consider the basic clocked comparator block diagram in Figure 2 with a 5 V power supply, a 2.5 V reference on the negative terminal, and an analog input signal on the positive terminal.



Digital Output - Analog Input = Added Noise			
Sample 1:	5V - 3.6V	= +1.4V	Logic 1: Analog In > V_{ref}
Sample 2:	5V - 2.8V	= +2.2V	Logic 0: Analog In < V_{ref}
Sample 3:	0V - 2.0V	= -2.0V	

Figure 2- ADC quantization added noise example

If the analog input is a sinusoid and the comparator is clocked at f_s, the output of the comparator will produce either a logic 1 or a logic 0 on each clock cycle based on the comparison. Analog inputs greater than the 2.5 V reference result in a logic 1 output and inputs less than 2.5 V result in a logic 0 output. Therefore, using the sequential discrete values discussed earlier, a 3.6V sample results in a logic 1 output, 2.8 V results in a logic 1, and finally 2.0 V results in a logic 0. The quantization noise added to each signal is represented by the simple relationship

$$Digital\ Output - \ Analog\ Input = Added\ Noise \tag{1.1}$$

such that the quantization noise added from the three samples is +1.4 V, +2.2 V, and -2.0 V, respectively. This added noise is a source of error introduced into the captured analog signal when an ADC is used as discussed above. This error can be bypassed by capturing and storing samples of a high-speed analog signal and later reading out the sampled signal at a slower rate so the output looks like a stretched, reconstructed version of the original signal.

1.2 MOTIVATION

A low power and low-cost CMOS Fast Transient Digitizer (FTD) with a measured sampling frequency of 4 GHz was initially presented by Buck and Baker [3] to effectively sample, in time, single-shot, high-speed analog signals. A series of 128 sequential unit cells were designed to act as both capture and storage devices and later a microprocessor was used to reconstruct the signal at a slower rate. The FTD's ability to capture high-speed analog events and later output a slowed version of the captured signal to be converted by an inexpensive, low power ADC at speeds

microcontrollers could process introduced an alternative to traditionally cost prohibitive and power inefficient high-speed ADCs. Additionally, the FTD also eliminated the need for additional circuitry or components, such as reconstruction filters (RCFs) and digital-to-analog converters (DACs), further reducing cost and power requirements while decreasing overall design size.

As a point of reference, a 3 Gsps, 7-Bit ADC designed by Texas Instruments currently retails for $168.70 with a typical active power consumption of 1.9 W [4]. Another 3 Gsps, 14-Bit ADC designed by Analog Devices, Inc. retails for $1,723.64 with typical active power dissipation of 3.3 W [5]. As ADC speed requirements decrease, cost and power consumption also decrease with slower, low power ADCs costing as little as $0.72 with typical active power consumption in the low milliWatts [6]. The advantages of using the FTD combined with a slower ADC versus a single high-speed ADC become more apparent when cost, power consumption, and layout area are compared.

After capturing the original analog signal, the reproduced signal coming out of the FTD can later be digitized via a microcontroller or processor by the end user according to application specific requirements. The net result is the captured and reproduced signal allows application specific analysis to occur. For example, the captured signal could be a fast transient voltage generated from the current created by a photodiode and amplified by a transimpedance amplifier. An on-chip decoder could read out the slowed, reproduced transient to then be used with a comparator measuring for a given threshold with the resulting output logic fed into a microprocessor for further application specific purposes.

The proposed CMOS High-Speed Fast Transient Digitizer (HSFTD) design requires a 5V power supply and aims to expand upon the FTD design using two different methods. The FTD is limited to a fixed sampling frequency set by the propagation delay through a buffer consisting of two basic inverters in each sequential unit cell. The first difference in the proposed HSFTD involves replacing the first inverter in each unit cell with a current-starved inverter controlled by a variable bias generator to allow the sampling frequency to be varied via an external control voltage. This adds an additional element of control to the FTD by allowing for faster or slower capture rates in each unit cell governed by the controllable delay through a current-starved inverter plus a fixed basic inverter delay.

The second difference involves the use of four interleaving banks of unit cells designed to increase the FTD's effective sampling frequency by a factor of four. The FTD is limited to a single unit cell capturing at any given point in time due to the iteration of a single trigger signal propagating through 128 consecutively ordered unit cells. Effectively, the FTD's second unit cell cannot begin sampling until the first unit cell is finished sampling. Similarly, the third unit cell cannot begin sampling until the second stage is finished sampling. This limits the FTD speed to the product of the delay through the two basic inverters in each unit cell and the total number of cells.

The interleaving technique, discussed in detail in Chapter 4, allows the sampling frequency to increase by increasing the number of unit cells actively capturing at any given point in time to four. The technique involves placing sequential unit cells in each of four separate banks with each bank receiving separate triggers separated in time by equally spaced delays. The triggers initiate

each successive individual bank to begin capturing in the proper sequential order such that all four banks contain one active unit cell at any given time.

The only times there are less than four unit cells active are during the latency periods between the first and fourth triggers entering and exiting the banks, equivalent to approximately one FTD unit cell time delay. This technique minimizes the delay between sequential unit cells and results in a theoretical sampling frequency four times that of the FTD. An additional note of interest is the HSFTD will implement four banks of 64 unit cells for 256 total capture stages, rather than the 128 stages in the FTD. However, the unit cell comparisons between the FTD and HSFTD are identical aside from the change in scale. The HSFTD IC design, layout, and simulation was completed using Cadence Design Systems electronic design automation (EDA) software with the ams AG 0.35 μm SiGe-BiCMOS Process Design Kit (PDK).

1.3 THESIS STRUCTURE

The contents of this thesis include the theoretically calculated and simulated results relevant to the design and simulation of the proposed CMOS HSFTD. The thesis takes a top down approach by first introducing a general overview of the HSFTD design and layout in Chapter 2 before moving on to discussing the individual design components in the following chapters. Chapter 3 discusses the design components comprising the unit cell, as well as the voltage controlled bias generation circuit. Next, Chapter 4 details the design of banks, the trigger generator, interleaving banks, and the decoders used to read out the reproduced signal. Top level design schematics, simulations, and a summary of calculated versus simulated results are covered in Chapter 5 followed in Chapter

6 by a design discussion and suggestions for future improvements for the HSFTD. Lastly, Chapter 7 concludes the thesis.

CHAPTER 2: HSFTD OVERVIEW

The HSFTD design and general theory will be introduced in this chapter with the theory behind individual building blocks and their functions presented in later chapters. The purpose of this chapter is to provide a general overview of the HSFTD operation, briefly mention the components comprising the design, and present the HSFTD design and layout. This top down approach aims to develop an intuitive perception of the design before moving on to the next several chapters for a more thorough discussion of the fundamentals driving the design.

2.1 HSFTD OPERATION

To begin, consider the basic block diagram of the HSFTD displayed in Figure 3. The analog input signal, *Analog In*, is seen at the top of 4 separate banks each consisting of 64 sequential unit cells and a 6:64 decoder. Prior to capturing, *Analog In* feeds into the banks and passes directly through to the output, *Output Signal*, such that these signals are identical. To initiate the HSFTD capture process, the Trigger Generator receives an externally generated high-to-low signal, *Trigger In*, resulting in an output consisting of four separate high-to-low trigger signals, *Trigger In 0-3*. At the fastest sampling rate, these signals are spaced evenly apart in time by approximately 60 ps. The timing between these signals is set by external control voltages *Vinvc 0-3* and *Bias Generators 0-3*. Each control voltage is set to a different, fixed value to control the 60 ps delays between *Trigger In 0-3*. The delays are set such that *Trigger In 0* reaches *Bank 0* first, followed 60 ps later by *Trigger In 1* into *Bank 1*, then after another 60 ps. *Trigger In 2* into *Bank 2*, and finally 60 ps later *Trigger*

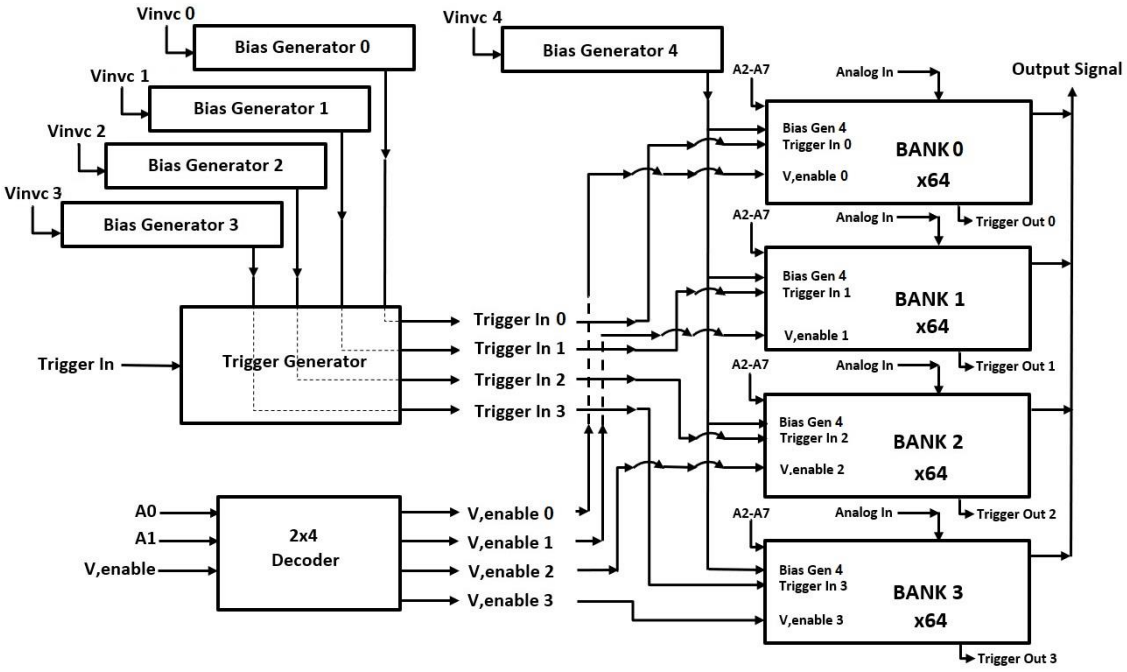


Figure 3 - HSFTD block diagram

In 3 into *Bank 3*. This timing initiates a sequential chain of 64 unit cell capture stages per bank capturing at a rate set by the external control voltage *Vinvc 4* and *Bias Generator 4*.

The entire HSFTD capture window is defined by the time between *Trigger In 0* reaching *Bank 0* and *Trigger Out 3* exiting *Bank 3*. Triggering the banks in this manner allows four separate unit cells to actively sample the signal in time during a period equivalent to one unit cell delay versus the FTD design only allowing a single cell to actively sample over the same period. In this manner, the sampling frequency of the HSFTD is increased by a factor of four versus the FTD resulting in a theoretical maximum effective sampling rate of approximately 16.5 GHz.

Once the input signal has been captured and stored in the unit cells, the 6:64 decoders in the banks are used to reconstruct the sampled high-speed signal at a slower rate via external control logic. At this point in the operation, *Analog In* has been isolated from the output and *Output Signal* is now dependent upon the decoders and captured samples of *Analog In*. The 2:4 decoder receives three external control signals, $V_{,enable}$, and the two least significant bits (LSBs), *A0* and *A1*, of the 8-bits required to decode 256 stages. $V_{,enable}$ activates the 2:4 decoder and *A0* and *A1* are used to create the logic required to toggle between *Banks 0-3* via the output signals $V_{,enable0-3}$. External control signals *A2-A7* connect directly to the 6:64 decoders in each bank and represent the remaining logic required to sequentially read out all 256 unit cells at a rate set by an off-chip 8-bit counter. *Output Signal* is connected to an off-chip pull-up resistor that creates a current controlled voltage drop proportional to the sampled signal. In this manner, the HSFTD samples high-speed analog signals in time and reads them out as slower, stretched reconstructions of the original.

2.2 HSFTD SCHEMATIC AND LAYOUT

Next, the top level Cadence schematic view of the HSFTD IC is shown below in Figure 4. The 4 x 64 FTD block represents the HSFTD circuit and includes all the components seen in Figure 3. Additionally, the schematic includes bonding pads with Electrostatic Discharge (ESD) protection for VDD, ground, and both analog and digital input and output signals. There are also three decoupling capacitors placed between VDD and ground to help reduce noise and smooth out the power supply voltage. The top level design simulation results will be detailed later in Chapter 5.

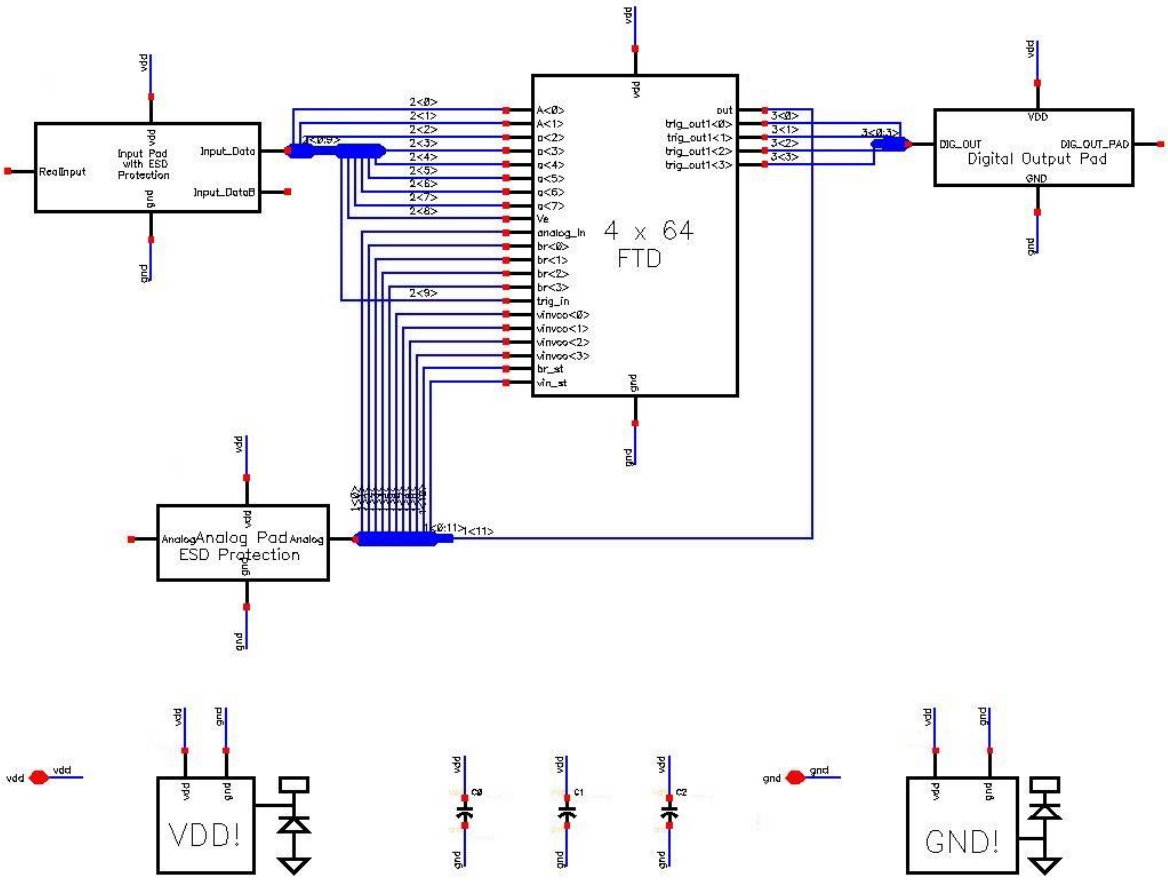


Figure 4 - HSFTD top level schematic

The top level layout view of the HSFTD IC as designed in Cadence is displayed in Figure 5. The HSFTD design is limited to the components within the black rectangle with the additional circuitry outside the rectangle related to various other research projects. The layout was completed and submitted to MOSIS [7] for fabrication on April 9, 2018.

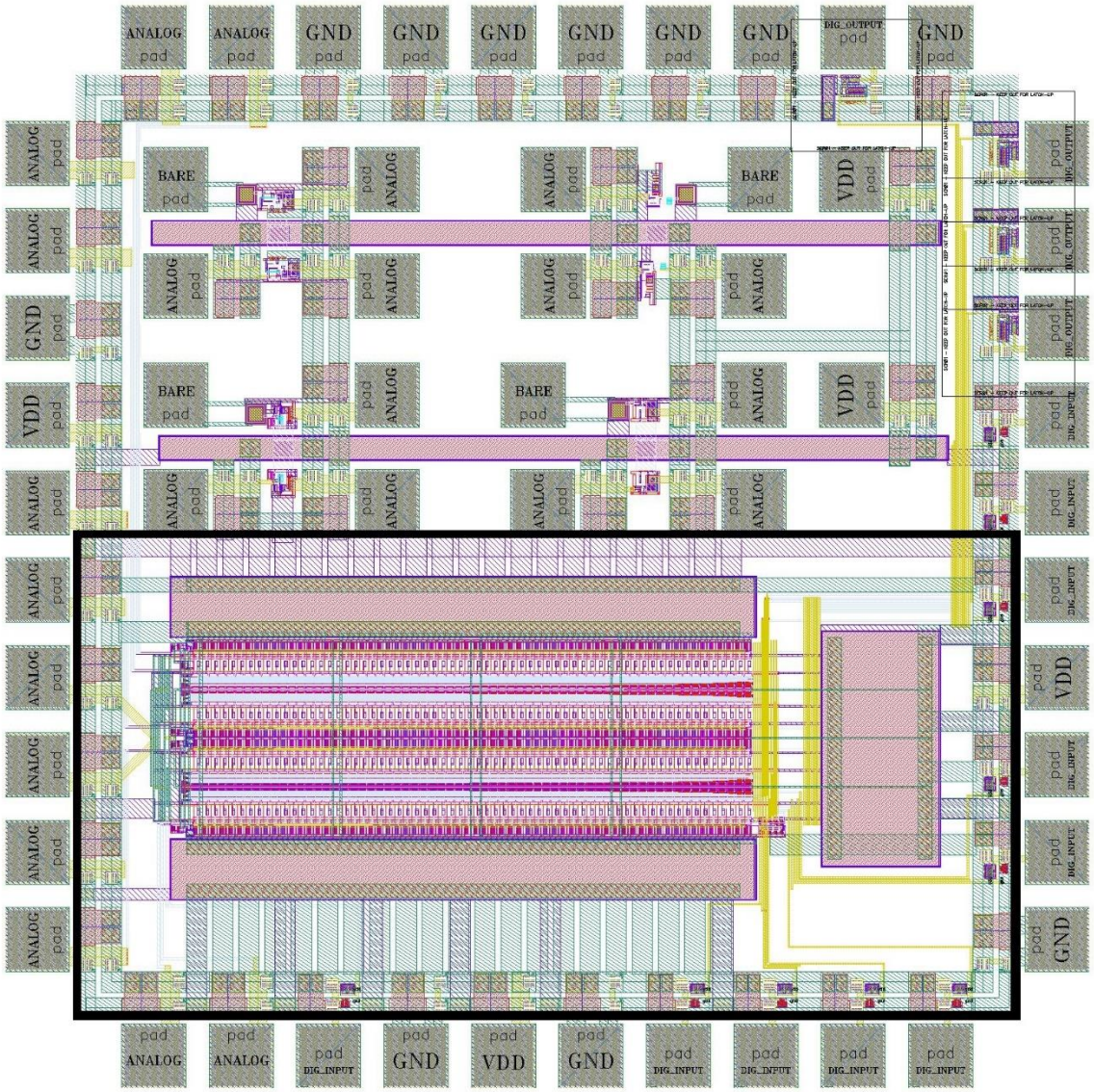


Figure 5 - HSFTD 2mm x 2mm IC layout

Figure 6 displays a closer view of the 256 stage HSFTD layout. Starting on the bottom left, a single bank consisting of a 6:64 decoder and 64 sequential unit cells is outlined in black with the 2:4 decoder to the right of the bank. Singular examples of the bias generator, trigger generator, 6:64 decoder, and 64 unit cells are also outlined to clarify the individual blocks comprising the sum

layout of 256 total stages. These components are populated throughout the layout such that the layout matches the block diagram seen earlier in Figure 3. Detailed versions of all individual components are included in later chapters with additional layouts and schematics included in the Appendix.

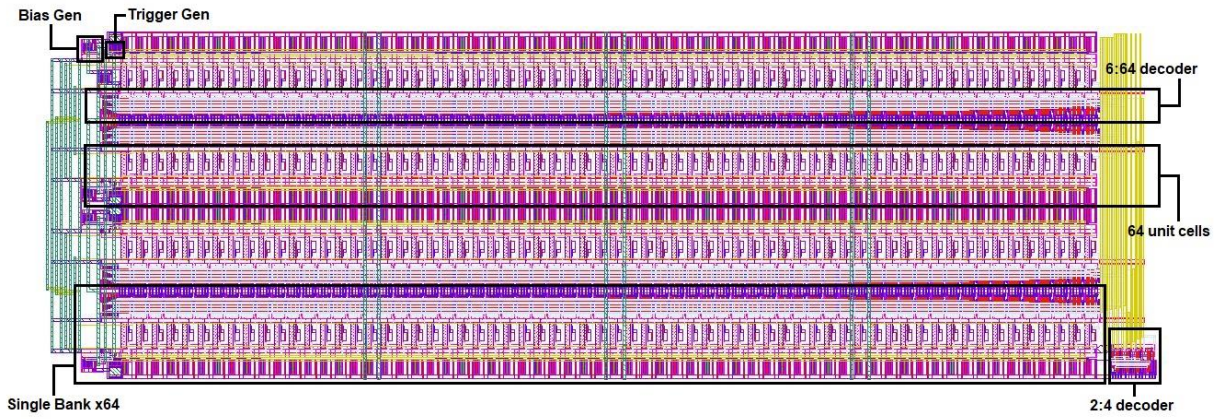


Figure 6 - HSFTD close up view of IC layout

CHAPTER 3: THE UNIT CELL

Chapter 3 incorporates and expands upon the material discussed in Chapter 2 as the operation of the components comprising the unit cell are detailed and characterized. The goal is to develop an intuitive comprehension for the design by first providing a synopsis of the cell operation before moving on to detailing each component individually. Section 3.1 discusses the unit cell operation before moving on to the bias generator in Section 3.2, inverters in Section 3.3, and the capture stage in Section 3.4.

3.1 UNIT CELL DESIGN AND OPERATION

The unit cell, schematic view in Figure 7 and layout view in Figure 8, is the fundamental building block of the HSFTD with each cell consisting of a current-starved inverter, a basic inverter, and a capture stage. The first part of the unit cell operation involves sampling in time the high-speed analog signal, *analog in*, connected to the drain of NMOS *N4*, and storing the sample on the capacitor connected to *N4*'s source. Prior to sampling, the trigger input signal, *trig in*, is set high such that after a propagation delay the signal *trig out* is also high, *N4* is switched on, and *analog in* is passing through *N4*. The propagation delay through the inverters is adjustable due to the bias voltages, *Vbiasp* and *Vbiasn,* coming from a DC bias generator. When *trig in* transitions from high-to-low, the signal *trig_out* also transitions from high-to-low after a propagation delay and *N4* switches off. At this point, a sample of *analog in* has been captured and stored as charge on a poly-poly capacitor. The signal *trig out* propagates as the input to the next unit cell in the

sequence and the process repeats iteratively until all the cells are finished capturing.

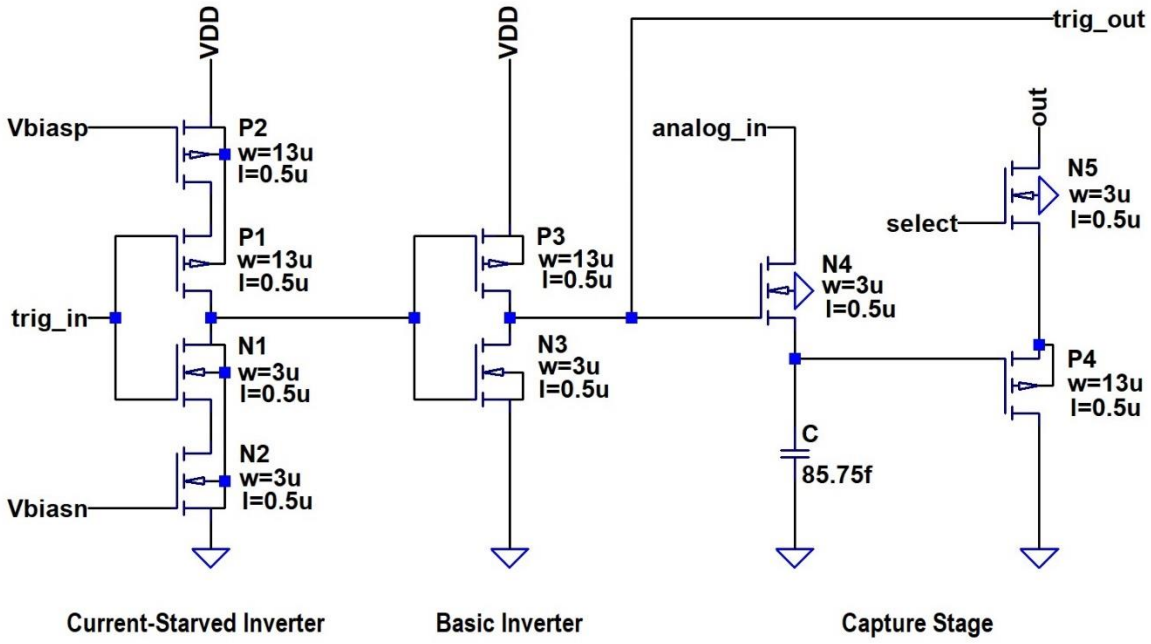


Figure 7 - HSFTD Unit Cell

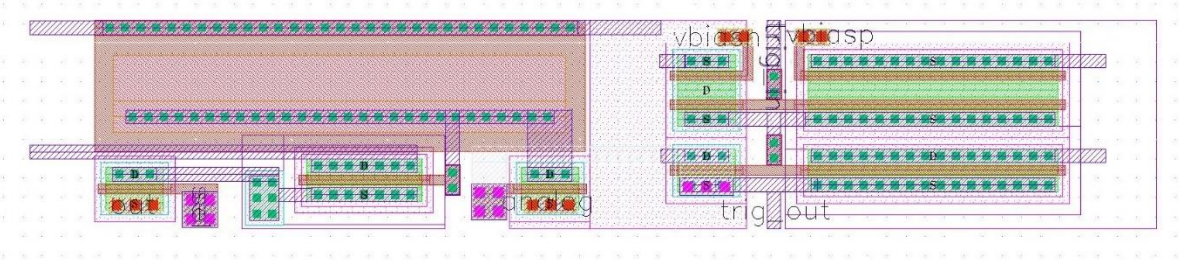


Figure 8 - Unit cell layout in Cadence

The second part of the unit cell operation involves readout of the sampled data via the PMOS, *P4*, the NMOS, *N5*, acting as a switch controlled by a *select* signal from a 6:64 decoder,

and an off-chip pull-up resistor connected to the drain of *N4* on one end and VDD on the other end. *P4* is in a source follower configuration with the gate biased via the hold capacitor, the drain connected to ground, and the source connected to the source of *N5* [8]. To readout the captured data, *select* transitions from low-to-high, *N5* switches on, and the biasing set by the capacitor controls the current flowing through *P4* and therefore, the current through the output node, *out*. The end result is a current controlled voltage drop across the pull-up resistor that represents a scaled version of the captured sample of *analog in* [8].

3.2 BIAS GENERATOR

The DC bias voltages, *Vbiasp* and *Vbiasn,* are generated via a voltage-controlled beta-multiplier voltage reference and are used to control the current through the current-starved inverters , detailed later in Section 3.3. The ability to adjust *Vinvc* externally and control the current through

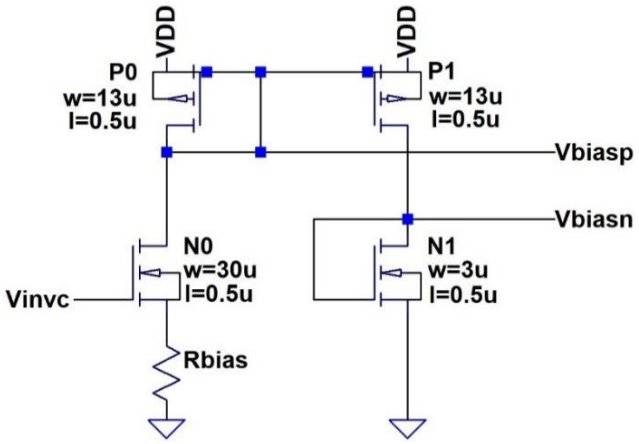


Figure 9 - DC bias generator schematic view

the inverters is what allows the sampling rate of the HSFTD to vary. The bias generator design, schematic view in Figure 9, aims to create stable DC reference voltages that are resistant to process, supply voltage, and temperature (PVT) variations. NMOS *N0* is biased by the external control voltage, *Vinvc*, and acts as a proportional to absolute temperature reference (PTAT) such that the reference voltages increase with increasing temperature. Conversely, the bias resistor acts as a complementary to absolute temperature reference (CTAT) such that increases in temperature result in decreases in the reference voltages. The two PMOS devices, *P0* and *P1*, serve as a current mirror with NMOS *N1* gate-drain connected to ensure the current through *P1* and *N1* are equal. *Vbiasp* and *Vbiasn* are connected on the gate-drain connected nodes of *P0* and *N1*, respectively. The bias generator layout view as designed in Cadence is seen in Figure 10.

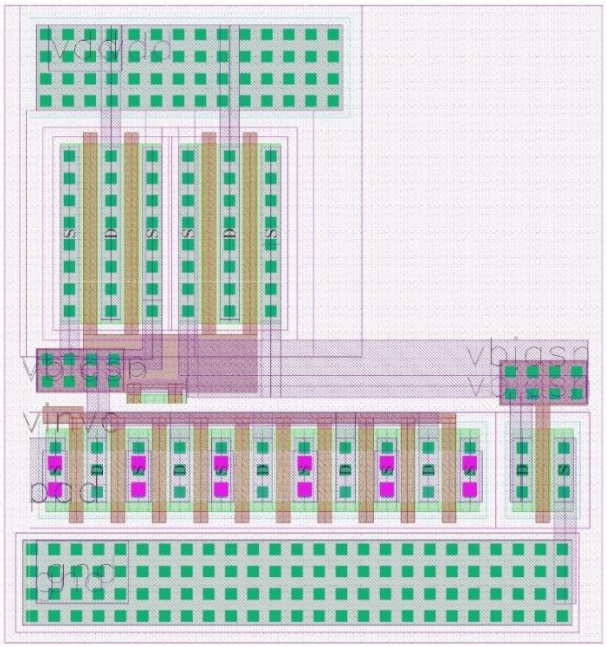


Figure 10 - Bias generator layout view in Cadence

Five separate bias generators are used in the HSFTD design with one used to create the biasing for all 256 unit cells and four more used to set DC bias voltages for the trigger generator detailed later in Chapter 4. The value of the bias resistor, *Rbias*, is determined based upon the desired range of linearity required for an application relative to adjustments of *Vinvc*. To illustrate the operation of the bias generator in creating a wide range of DC bias voltages, simulation results for a DC sweep of *Vinvc* for *Rbias* values of 4 kΩ, 2 kΩ, and 0.1 Ω are included in Figure 11. Note, the inclusion of a negligible 0.1 Ω bias resistor is effectively modeling zero resistance and may be thought of as a placeholder for a larger resistor, such as a 4 kΩ resistor, that may be used to slow the capture rate. Therefore, the 0.1 Ω resistor may hereafter be thought of as having no bias resistor. The results, summarized in Table 1, demonstrate as *Rbias* decreases the linear region

Resistance (Ω)	4 kΩ	2 kΩ	No Resistor
Vinvc 800 mV			
Vbiasp (V)	3.75	3.72	3.63
Vbiasn (V)	0.992	1.02	1.11
Vinvc 5 V			
Vbiasp (V)	2.34	1.88	0.197
Vbiasn (V)	2.72	3.37	4.10
Linear Range	0.800 - 4.00	0.800 - 3.40	0.800 - 1.40

Table 1 - Bias Generator *Vinvc* DC Sweep

decreases while *Vbiasp* and *Vbiasn* increase. As *Rbias* decreases, *N0*'s source voltage also decreases, thus allowing more current to flow. This enables the device to saturate more quickly

with a resulting decrease in the linear region. Referencing Table 1, the linear region extends approximately 3.2 V for 4 kΩ, 2.6 V for 2 kΩ, and 600 mV for no bias resistor.

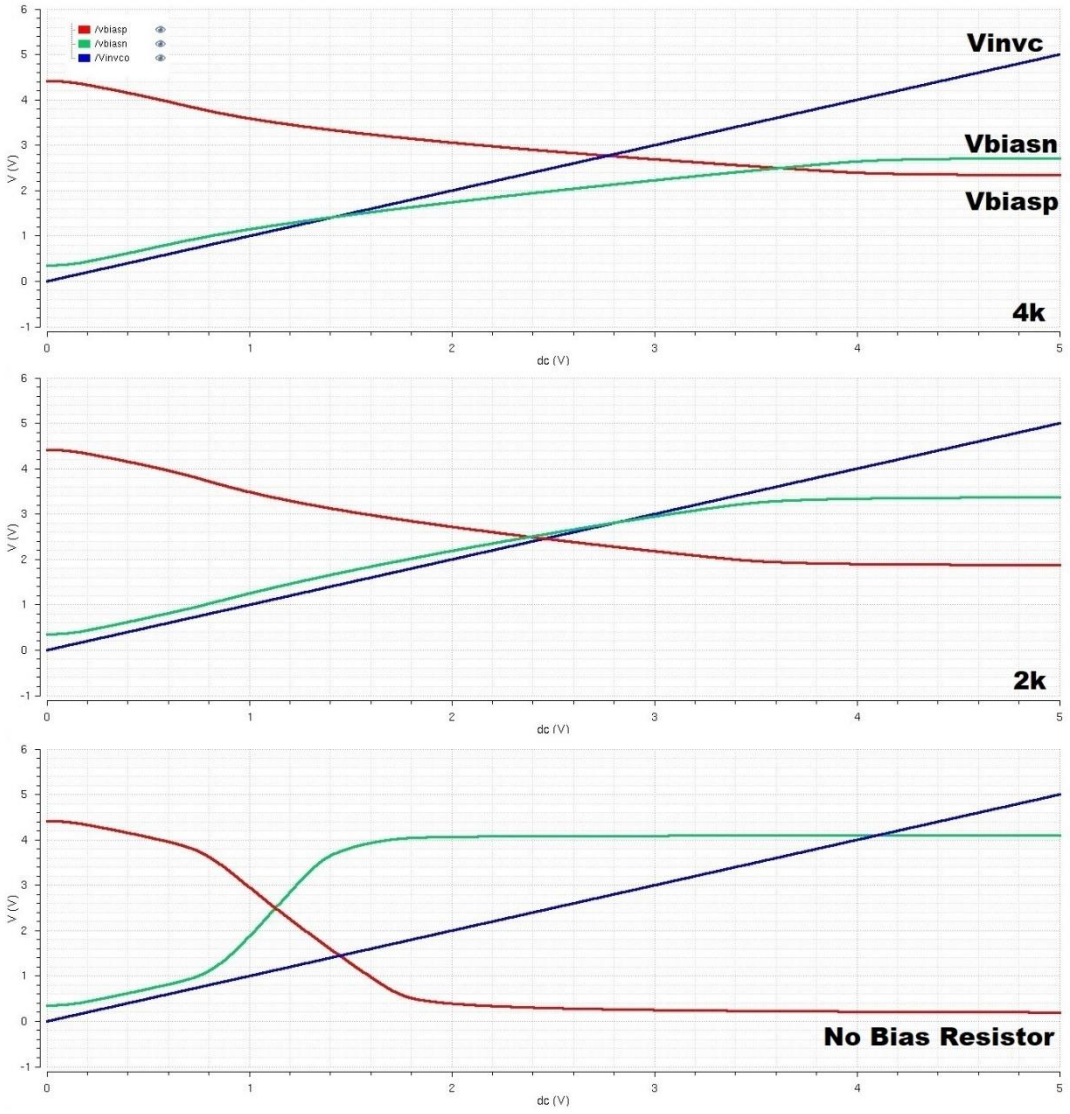


Figure 11 - Bias generator DC sweep simulation results for 4 kΩ, 2 kΩ, and no bias resistors

The bias voltages increase with decreasing *Rbias* due to the drain voltage of *N0*, or *Vbiasp*, being pulled down such that *P0* and *P1* are turned on more and the drain of *N1* is pumped up to a

higher voltage. Due to process variations that could result in on-chip resistor values differing from desired values, the bias generators in the HSFTD were designed to use off-chip resistors as an additional element of control for tuning the HSFTD.

Including both PTAT and CTAT references in the design serves to stabilize the drain current due to the cancellation of temperature effects related to *N0* and *Rbias*. For example, as temperature increases, N0's threshold voltage decreases and electron mobility increases, thus enabling more current to flow. Simultaneously, the resistance of the bias resistor increases due to increasing temperature and consequently limits additional current flow. In this manner, the PTAT and CTAT references serve to cancel temperature effects and create a relatively constant drain current.

To demonstrate this characteristic, DC simulations were performed sweeping *Vinvc* and stepping temperature from 0° C to 100° C with *Rbias* set to fixed values. Figures 12 and 13 display the results for simulations using two cases, a 4 kΩ resistor and no bias resistor, respectively. Note, the current in both figures remains relatively constant throughout the linear region and across temperature variations. This ensures the same amount of current is available to charge and discharge the inverter capacitances such that the propagation delay through the inverters remains constant across temperature variations. As an application note, when the HSFTD is used in a feedback loop within a system, the temperature change effects are removed because the feedback loop will adjust the control voltage to set the required range and operation.

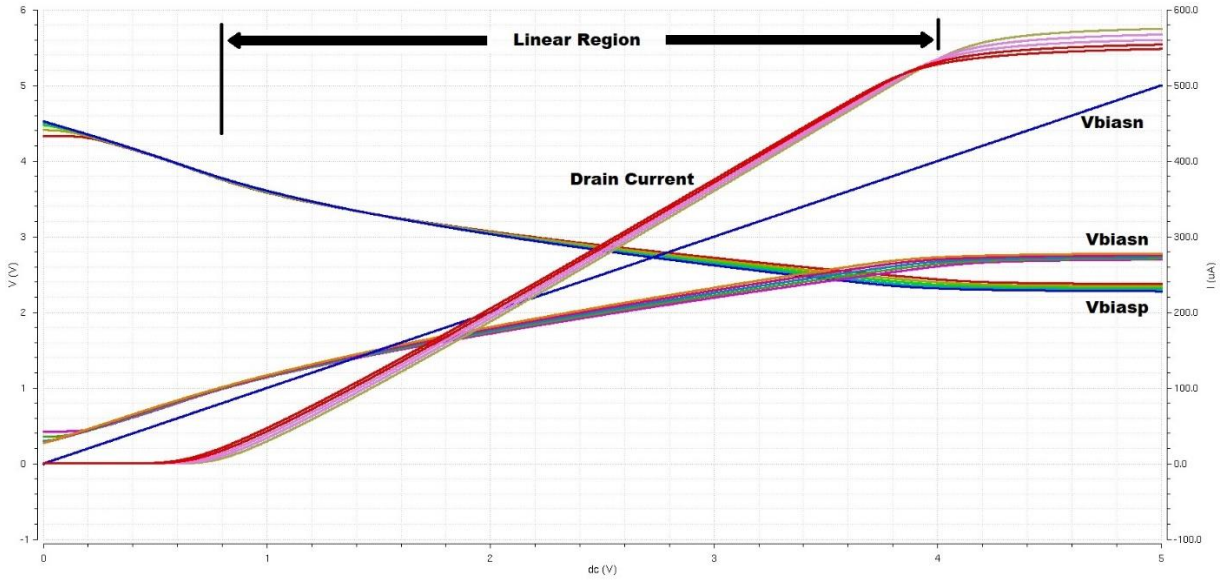


Figure 12 - Bias generator temperature simulation results for 4 kΩ

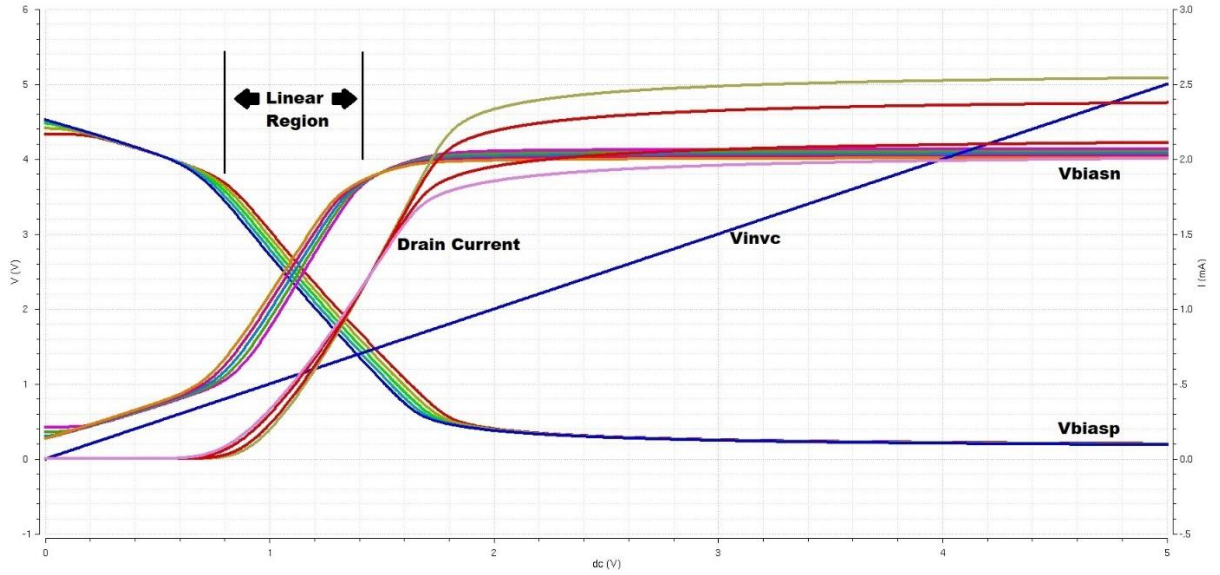


Figure 13 - Bias generator temperature simulation results for no bias resistor

	0° C		100° C	
Resistance (Ω)	4 kΩ	No Resistor	4 kΩ	No Resistor Ω
Vinvc 800 mV				
Vbiasp (V)	3.75	3.68	3.77	3.43
Vbiasn (V)	986 m	1.05	1.01	1.34
Vinvc 5 V				
Vbiasp (V)	2.37	203 m	2.28	188 m
Vbiasn (V)	2.70	4.10	2.77	4.01
Linear Range	0.900 - 4.10	0.800- 1.40	1.00 - 3.80	0.700 - 1.30

Table 2 - Bias generator *Vinvc* and Temperature Sweep

The simulation results for both cases demonstrate the linear regions shift down slightly with increasing temperature, as expected, due to a correlating decrease in the threshold voltage of *N0*. However, the range of these regions remains approximately the same. Additionally, the decrease in threshold voltage with increasing temperature results in minor variations in *Vbiasp* and *Vbiasn* as summarized in Table 2.

Lastly, simulations were performed to demonstrate the response to variations in power supply voltage to further confirm the voltage reference is resistant to PVT variations. The simulations assumed a 2% variation in the power supply voltage with results displayed in Figures 14 and 15 and summarized in Table 3. Once again, *Vinvc* was swept with both cases, 4 kΩ and no bias resistor, used in the simulations.

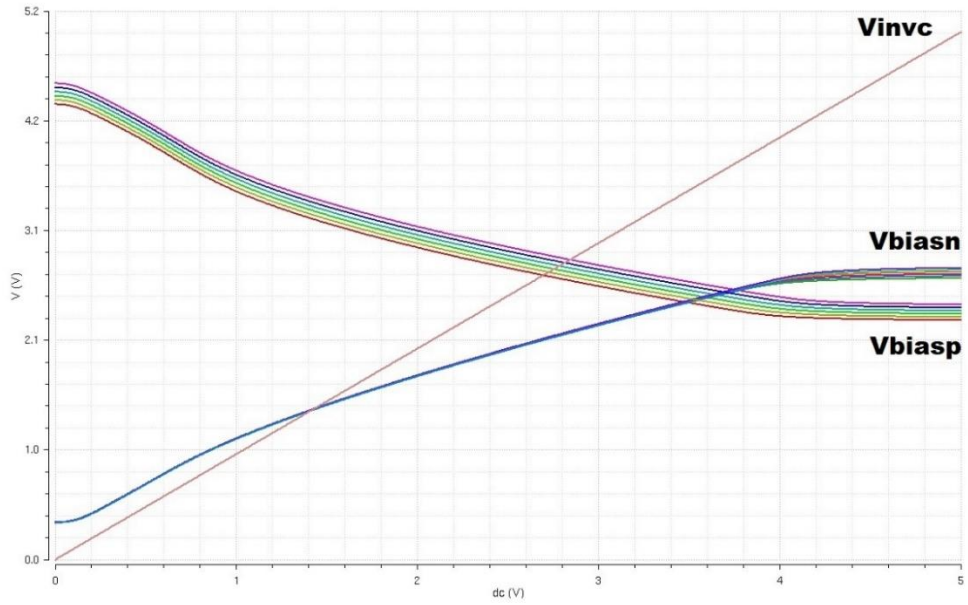


Figure 14 - Bias generator power supply simulation results for 4 kΩ

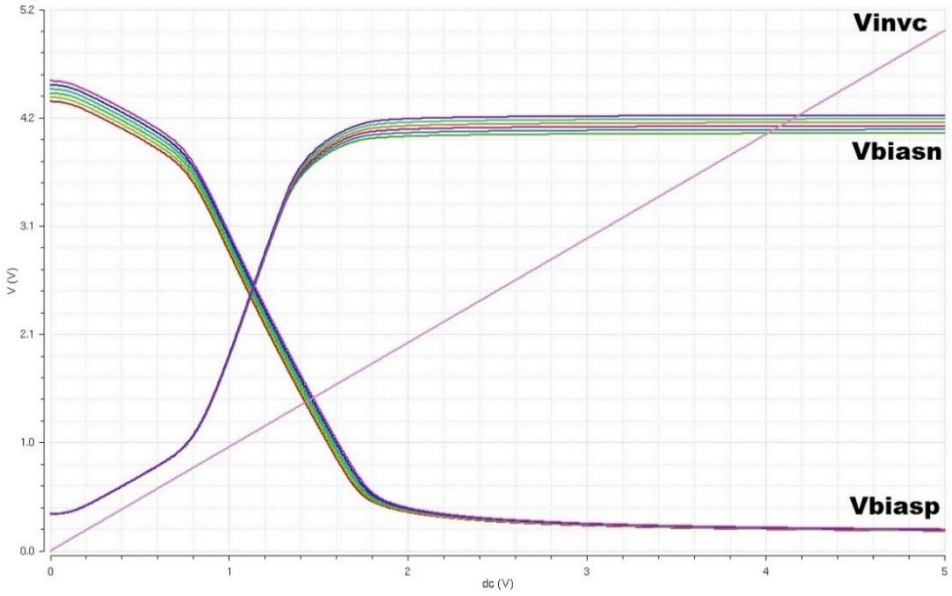


Figure 15 - Bias generator power supply simulation results for no bias resistor

VDD	4.9 V		5.0 V		5.1 V	
Resistance (Ω)	4 kΩ	No Resistor	4 kΩ	No Resistor	4 kΩ	No Resistor
Vinvc 800 mV						
Vbiasp (V)	3.66	3.53	3.76	3.63	3.86	3.72
Vbiasn (V)	989 m	1.10	992 m	1.11	995 m	1.12
Vinvc 5 V						
Vbiasp (V)	2.27	189 m	2.34	197 m	2.41	205 m
Vbiasn (V)	2.66	4.01	2.72	4.10	2.76	4.18
Linear Range	0.8 - 4.1	0.8 - 1.4	0.8-4.0	0.8-1.4	0.8 - 4.0	0.8 - 1.4

Table 3 - Bias generator 2% Variation in Power Supply Sweep

The simulation results for different *Rbias* values, temperature ranges, and power supply variations demonstrate the bias generator is able to provide relatively stable DC voltage references and maintain linearity with adjustments in *Vinvc* relative to different resistor values.

3.3 INVERTERS

The fundamental building blocks of the HSFTD design are the inverters enabling the four triggers created by the trigger generator to propagate sequentially through four separate banks of 64 unit cells. The significance of the basic inverter is it propagates a single-shot, high-to-low input pulse through the unit cells with a predictable time delay while also driving the MOS capacitances of the next sequential unit cell. Additionally, the output of the basic inverter drives one extra NMOS per unit cell, *N4* in Figure 7, used in the capture stage detailed later in Section 3.4. As discussed in

Chapter 1, the first difference in the HSFTD design versus the FTD design is the use of current-starved inverters. The significance of the current-starved inverter is it provides a degree of variability that allows the propagation delay through each inverter to be increased or decreased, thus allowing the sampling rate to be varied.

Therefore, the main limitation regarding the speed of the HSFTD design is the time delay through a basic CMOS logic inverter, seen in Figure 16. An inverter is a circuit that receives an input pulse, V_{in}, and inverts it such that the output, V_{out}, is a time-delayed inversion of the input. The area of interest regarding the HSFTD is the time difference, or propagation delay, between V_{in} switching logic levels and V_{out} switching logic levels. The propagation delay is typically measured at 50% of the V_{in} to V_{out} transition.

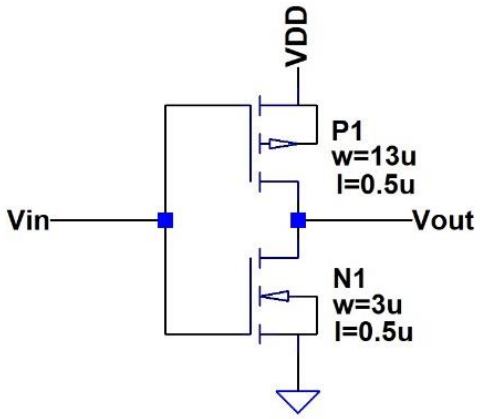


Figure 16 - Basic inverter

To clarify, consider the inverter transfer characteristics seen in Figure 17 where the x-axis represents V_{in} and the y-axis represents V_{out} [9]. Regarding V_{in}, a logic 0 is any input voltage less

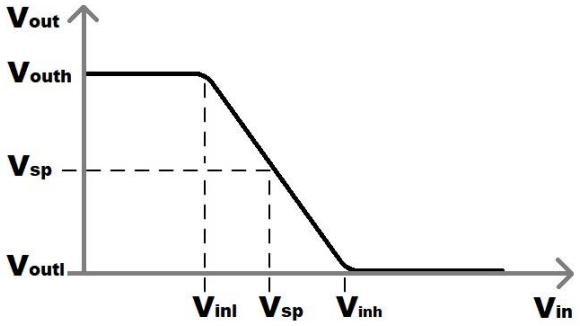


Figure 17 - Inverter transfer characteristics

than V_{inl} and a logic 1 is any input voltage greater than V_{inh}. Referencing V_{out}, inputs less than V_{inl} result in a logic 1 output, noted as V_{outh}. Inputs greater than V_{inh} result in a logic 0 output, noted as V_{outl}. An additional point of interest is the point where V_{in} equals V_{out}, known as the *inverter switching point*, V_{sp}. This represents the point where both the PMOS and NMOS are on and operating in the saturation region as opposed to a single device being on while the other device is off. To minimize the impact of noise on the circuit, the ideal V_{sp} is centered around VDD/2, thus ensuring equal noise margins.

Next, the current-starved inverter, Figure 18, adds an upper PMOS, *P2*, acting as a current source, and lower NMOS, *N2*, acting as a current sink, to the basic inverter comprised by *P1* and *N1*. *P2* and *N2*, controlled by bias voltages, *Vbiasp* and *Vbiasn* respectively, serve to control the current sourcing and sinking capability of the inverter and therefore enable the time delay through the inverter stage to be varied. As noted in Table 1, using *Vinvc* set to 5 V with no bias resistor generates the lowest *Vbiasp,* 197 mV, and highest *Vbiasn,* 4.1 V, resulting in the

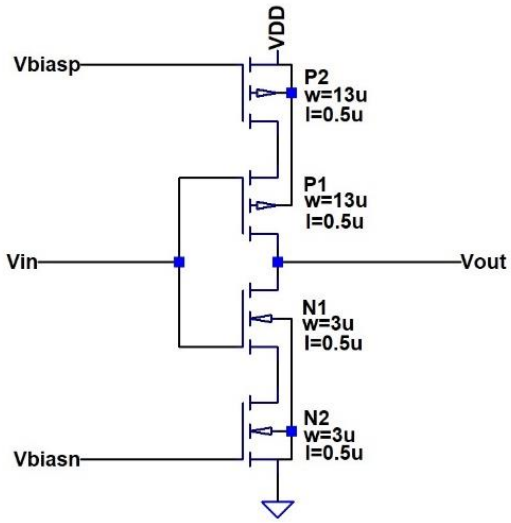


Figure 18 - Current-starved inverter

fastest propagation delay through the current-starved inverter. As the reference voltages decrease with adjustments of *Vinvc*, the propagation delay will increase due to a decrease in the ability of *P2* and *N2* to source and sink current, respectively.

The inverters in the HSFTD are driven by a trigger in the form of a voltage pulse, therefore these devices can be modeled as simple switches with an 'on' state and an 'off' state. To develop a model to approximate the time delay through an inverter, a basic RC circuit can be used as a starting point. Figure 19 displays a basic RC circuit driven by a low-to-high voltage pulse. When

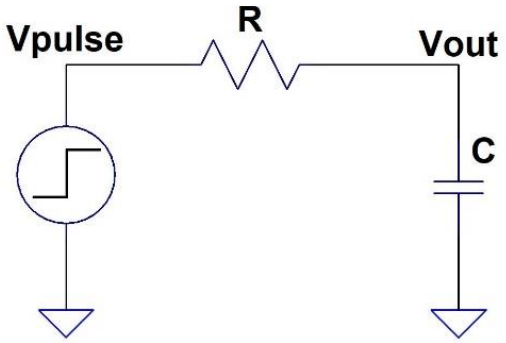


Figure 19 - RC circuit

the input transitions from low-to-high, the voltage across the capacitor, V_{out}, is defined by

$$V_{out}(t) = V_{pulse}\left(1 - e^{\frac{-t}{RC}}\right) \tag{3.1}$$

The time delay, t_d, for the circuit is defined as the time required for the output to reach 50% of V_{pulse}, making the point of interest

$$V_{out}(t) = \frac{V_{pulse}}{2} = V_{pulse}\left(1 - e^{\frac{-t_d}{RC}}\right) \tag{3.2}$$

Solving for t_d results in the following

$$t_d = -\ln\left(\frac{1}{2}\right) * RC = 0.693 * RC \approx 0.7RC \tag{3.3}$$

To make this result useful requires the continued development of an RC model for the basic MOSFET inverter. This starts with developing a model for both the NMOS and the PMOS to characterize the effective switching resistances, or the resistances between the drain and the

source, for each device. However, the devices in this design are short-channel devices and therefore are not governed by the square-law equations used for long-channel devices [9].

To calculate the effective switching resistances, Cadence simulations can be used to determine the current that flows when *VDD*, V_{GS}, and V_{DS} are all equal in strong inversion, known as the *on current*, I_{on}. To develop a relationship for I_{on} and the switching resistance, first consider the drain current, I_D, of a short channel MOSFET operating in saturation. I_D for a short channel process is given by

$$I_D = W * v_{sat} * C'_{ox}\left(V_{GS} - V_{THN} - V_{DS,sat}\right) \tag{3.4}$$

where *W* is the device width, v_{sat} is the saturation velocity of an electron in an electric field, and $V_{DS,sat}$ represents the point where the MOSFET enters saturation [9]. The oxide capacitance per unit area, C'_{ox}, is given by

$$C'_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{3.5}$$

with units of Farads per meter squared (F/m^2). An additional parameter of merit that will be useful later is the total capacitance between the channel and the gate, C_{ox}, defined as

$$C_{ox} = C'_{ox}WL \tag{3.6}$$

with units of Farads. ε_{ox} is the permittivity of the insulator, silicon dioxide (SiO_2), and t_{ox} is the process dependent oxide thickness, 15 nm in this process [10]. ε_{ox} is given as follows

$$\varepsilon_{ox} = \varepsilon_r * \varepsilon_o = 3.9 * 8.85 \times 10^{-18} F/\mu m \approx 34.515 \times 10^{-12}\ F/\mu m \tag{3.7}$$

where $\mathcal{E}_r$ is the dielectric constant of SiO_2 and $\mathcal{E}_o$ is the permittivity of free space. Therefore, C'_{ox} is determined to be

$$C'_{ox} = \frac{3.9 * 8.85 \times 10^{-18} F/\mu m}{0.015 \mu m} \approx 2.301\ \frac{fF}{\mu m^2} \tag{3.8}$$

I_{on} is given in units of Amp-meters (A/m) and represents the drive current per width of a MOSFET. This is defined by [9]

$$I_{on} = v_{sat} * C'_{ox}\left(V_{GS} - V_{THN} - V_{DS,sat}\right) \tag{3.9}$$

Using Eq. (3.4) and Eq. (3.9) leads to the following

$$I_D = I_{on} * W \tag{3.10}$$

Finally, via Ohm's Law, the effective switching resistances are governed by the following

$$R_{n,p} = \frac{VDD}{I_{D,sat}} = \frac{VDD}{I_{on} * W} = R'_{n,p}\frac{L}{W} \tag{3.11}$$

Note, as device width increases the effective resistance decreases. Conversely, minimum length results in less resistance and faster propagation of signals. Solving for $R'_{n,p}$ gives

$$R'_n = \frac{VDD}{I_{D,sat}} * \frac{W_n}{L_n}\ and\ R'_p = \frac{VDD}{I_{D,sat}} * \frac{W_p}{L_p} \tag{3.12}$$

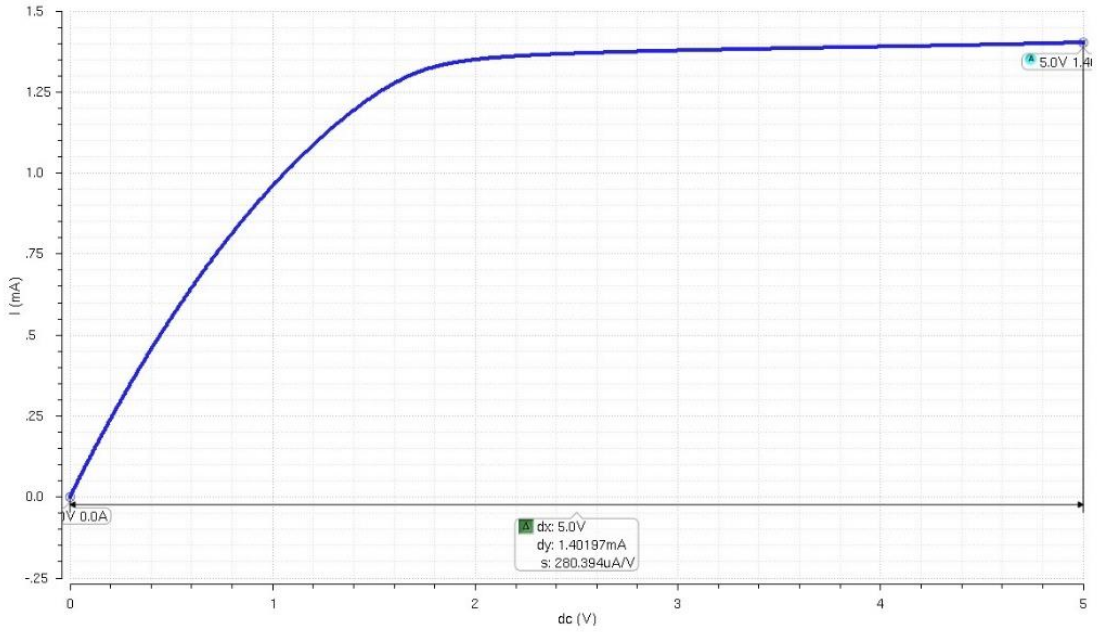


Figure 20 - NMOS effective switching resistance via Cadence simulation

Due to the failure of the square-law to accurately model the devices, estimates for the switching resistances were obtained via Cadence simulations with the NMOS simulation results included in Figure 20.

The inverters used in the unit cells were sized 13 µm/0.5 µm and 3 µm/0.5 µm for the PMOS and NMOS, respectively, giving a ratio of 4.333:1 to achieve an ideal switching point of VDD/2, or 2.5 V. Using Eq (3.12) with these sizes and the values from Figure 20 results in

$$R'_n = \frac{5V}{1.4019mA} * \frac{3\mu m}{0.5\mu m} \approx 21.4\ k\Omega \tag{3.13}$$

and

$$R'_p = 4.333 * 21.4k\Omega \approx 92.7\ k\Omega \tag{3.14}$$

The next step in creating the inverter time delay model from Eq. (3.3) is to develop governing equations for the inverter capacitances. To accomplish this requires deriving the capacitances of the switching MOSFETS. However, it is useful to briefly discuss *Miller's theorem* as it relates to the HSFTD design before moving on to the basic MOS capacitances. *Miller's theorem* states an impedance, *Z*, isolated between two circuit nodes that are also connected to other parts of the circuit, node 1 and node 2, may be replaced by an equivalent model with two impedances, Z_1 , connected to node 1 and ground, and Z_2, connected to node 2 and ground, as seen in Figure 21 [10]. Additionally, Z_1 and Z_2 are adjusted in size such that the circuit in Figure 21 (b) is an equivalent model for the circuit in Figure 21 (a).

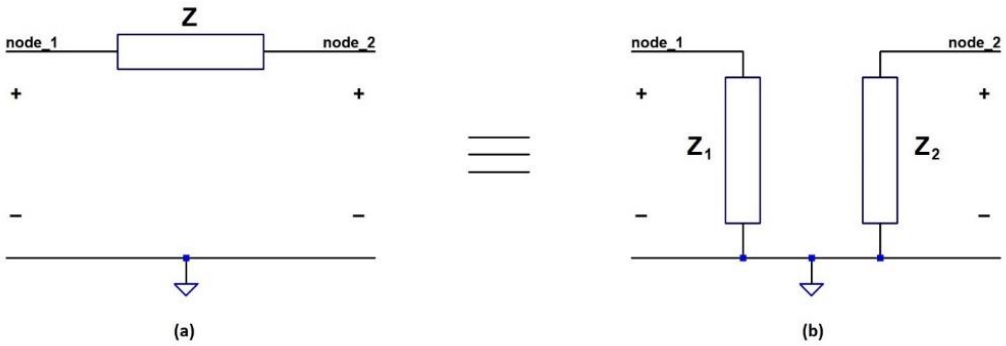


Figure 21 - Miller's Theorem: (a) original circuit; (b) Miller equivalent circuit

A general mathematical proof of Miller's theorem is absent in favor of a design specific explanation. Figure 22 displays NMOS and PMOS switching circuits with relevant capacitances. The gate-drain and gate-source capacitances are overestimated to be $C_{ox}/2$, as occurs when the

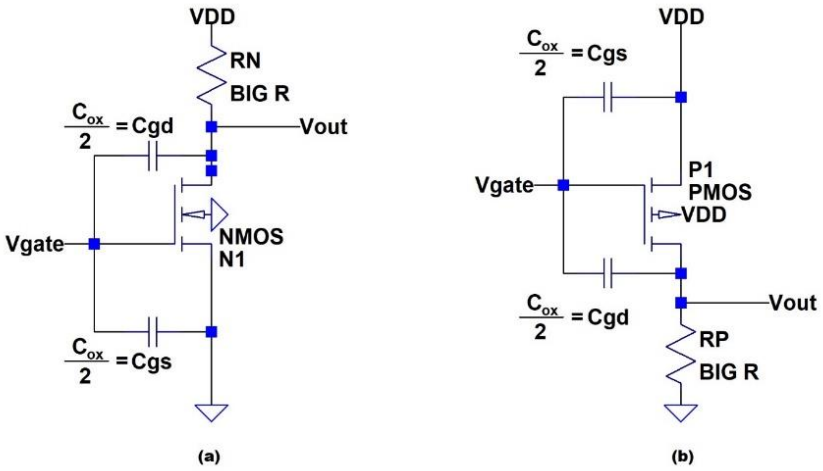


Figure 22 - MOSFET capacitances: (a) NMOS; (b) PMOS

devices are in the triode region and the source and drain are resistively connected through the channel. In the saturation-region the capacitances will be smaller due to pinching-off of the channel at the drain, therefore the overestimate allows the source, drain, and gate to substrate depletion capacitances to be neglected for the general model being developed [9].

Miller's theorem can be applied to the MOSFET capacitances, and later to the basic inverter model, to separate the input and output capacitances into two separate capacitances, C_{in} and C_{out}. However, the model requires setting the two capacitor values such that each capacitor takes the same amount of charge and the input and output see the same effective capacitance. Referencing Figure 22 (a), consider the capacitance C_{gd} as the impedance Z seen in Figure 21 (a). Using Miller's theorem as it pertains to an NMOS receiving an input pulse from low-to-high and assuming the output is initially set to VDD to mimic basic inverter operation, C_{gd} can be modeled as seen in Figure 23 [9].

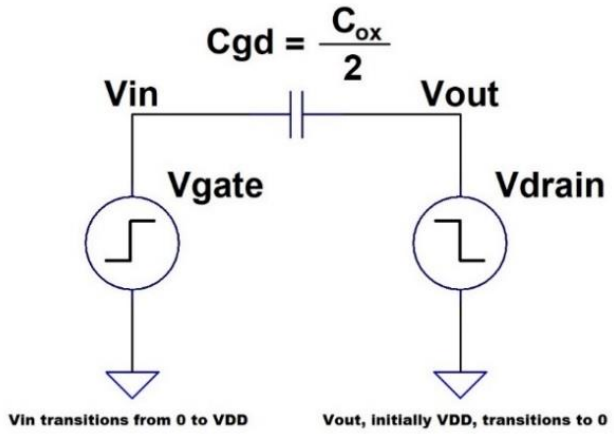


Figure 23 - Using Miller's theorem to model C_{gd}

The total charge supplied to C_{gd} via the voltage sources, Q_{total}, can be calculated using Q_1 to define the charge on C_{gd} prior to transitioning and using Q_2 to define the charge on C_{gd} after the transition, as follows

$$Q_1 = C_{gd} * (0 - VDD) = -C_{gd} * VDD \tag{3.15}$$

$$Q_2 = C_{gd} * (VDD - 0) = C_{gd} * VDD \tag{3.16}$$

$$Q_{total} = Q_2 - Q_1 \tag{3.17}$$

$$Q_{total} = C_{gd} * VDD - \left(-C_{gd} * VDD\right) = 2C_{gd} * VDD \tag{3.18}$$

The resulting charge Q_{total} reveals the value of C_{gd} must be adjusted to $2C_{gd}$ to accurately model the capacitances seen on the input and the output, C_{in} and C_{out}, respectively. The capacitor in Figure 23 can then be modeled as two separate capacitors drawn as seen in Figure 24 [9].

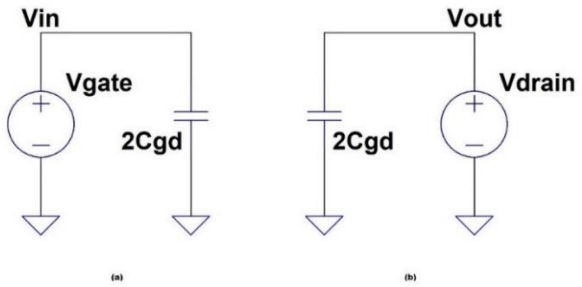


Figure 24 - Equivalent model for capacitor in Fig. 23 using Miller's theorem

Returning to Figure 22 and applying Miller's theorem results in the equivalent MOSFET models seen in Figure 25 (a) and the equivalent RC model for the inverter in Figure 25 (b) [9].

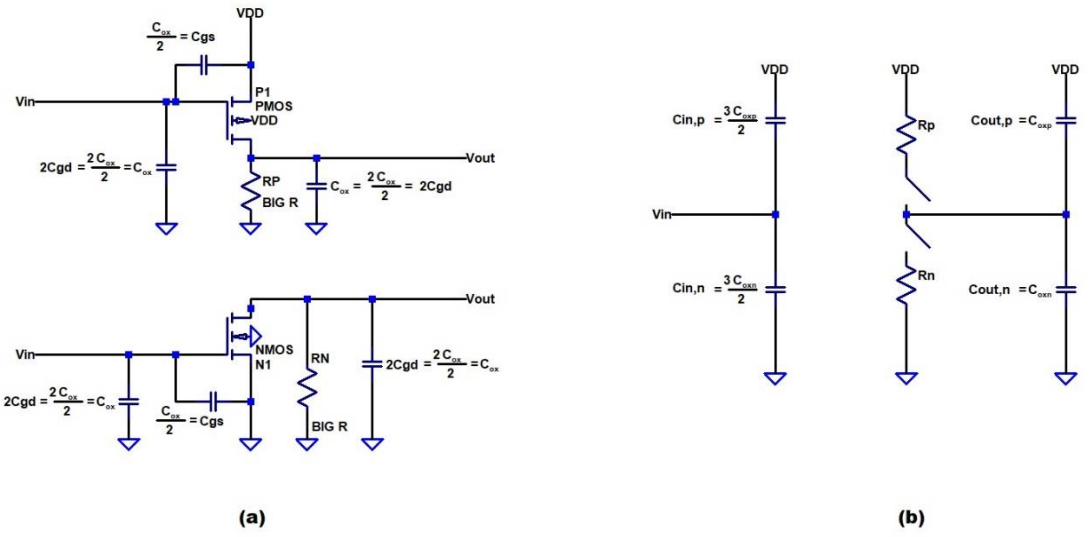


Figure 25 - (a) Equivalent MOSFET models using Miller's theorem; (b) Inverter RC model

The input and output capacitances of the unit cell inverters are defined by the following [9]

$$C_{in} = \frac{3}{2} * \left(C_{oxn} + C_{oxp}\right) = C_{in,n} + C_{in,p} \tag{3.19}$$

$$C_{out} = C_{oxn} + C_{oxp} = C_{out,n} + C_{out,p} \tag{3.20}$$

Using identically sized inverters results in the capacitances seen on the input or output of any given inverter to be defined as the sum of the inverter input and output capacitances. This leads to a total capacitance of

$$C_{tot} = C_{in} + C_{out} = \frac{3}{2} * \left(C_{oxn} + C_{oxp}\right) + C_{oxn} + C_{oxp} = \frac{5}{2} * \left(C_{oxn} + C_{oxp}\right) \tag{3.21}$$

Referencing Eq. (3.6) and Eq. (3.8) leads to

$$C_{oxn} = 2.301 \frac{fF}{\mu m^2} * 3\mu m * 0.5\mu m \approx 3.4515\ fF \tag{3.22}$$

$$C_{oxp} = 2.301 \frac{fF}{\mu m^2} * 13\mu m * 0.5\mu m \approx 14.9565\ fF \tag{3.23}$$

such that

$$C_{tot} = \frac{5}{2} * (3.4515 fF + 14.9565 fF) \approx 46.02\ fF \tag{3.24}$$

Returning to the basic RC model developed earlier allows for determining the time delay between the input and output signals of the inverter. Referencing Eq. (3.3) and the basic inverter model seen in Figure 25 (b), the times the signal takes to transition from low-to-high and from high-to-low are defined by

$$t_{plh} = 0.7\ R'_p \frac{L_p}{W_p} C_{tot} = 0.7 * 92.7k\Omega * \frac{0.5\mu m}{13\mu m} * 46.02fF \approx 114.8553\ ps \quad (3.25)$$

$$t_{phl} = 0.7\ R'_n \frac{L_n}{W_n} C_{tot} = 0.7 * 21.4k\Omega * \frac{0.5\mu m}{3\mu m} * 46.02fF \approx 114.8966\ ps \quad (3.26)$$

respectively. The additional NMOS used in the capture stage has a delay given by

$$t_{n,stage} = 0.7\ R'_n \frac{L_n}{W_n} * \frac{3}{2}\ C_{oxn} \quad (3.27)$$

$$t_{n,stage} = 0.7 * 21.4k\Omega * \frac{0.5\mu m}{3\mu m} * \frac{3}{2} * 3.4515fF \approx 12.9259\ ps$$

Therefore, the total delay through an individual unit cell can be approximated as

$$t_d = t_{plh} + t_{phl} + t_{n,stage} \approx 115\ ps + 115\ ps + 13\ ps \approx 243\ ps \quad (3.28)$$

This results in a theoretical sampling frequency of

$$f_{sample} = \frac{1}{t_d} = \frac{1}{243\ ps/4} \approx 16.5\ GHz \quad (3.29)$$

where the time delay is divided by a factor of four to account for the increase in sampling frequency discussed earlier in Chapter 2.

To validate this approximation, a Cadence simulation modeling the inverter delays was completed with sample results for *Vinvc* set to 1.25 V and 5 V seen in Figures 26 and 27, respectively, and summarized in Table 4. The simulation used no bias resistor and stepped *Vinvc* to accurately model the expected biasing and to determine the fastest range of the time delay, as

well as the corresponding sampling frequency. However, an important point of note is to remember the sampling frequency decreases with increasing *Rbias*. The emphasis here is on the fastest speed possible, but changing *Rbias* to a larger value, for example 4 kΩ, results in a slower sampling frequency. Referencing Eqs. (3.25) - (3.29), the results from Table 4 indicate the RC model serves to approximate the behavior of the delays through the unit cells.

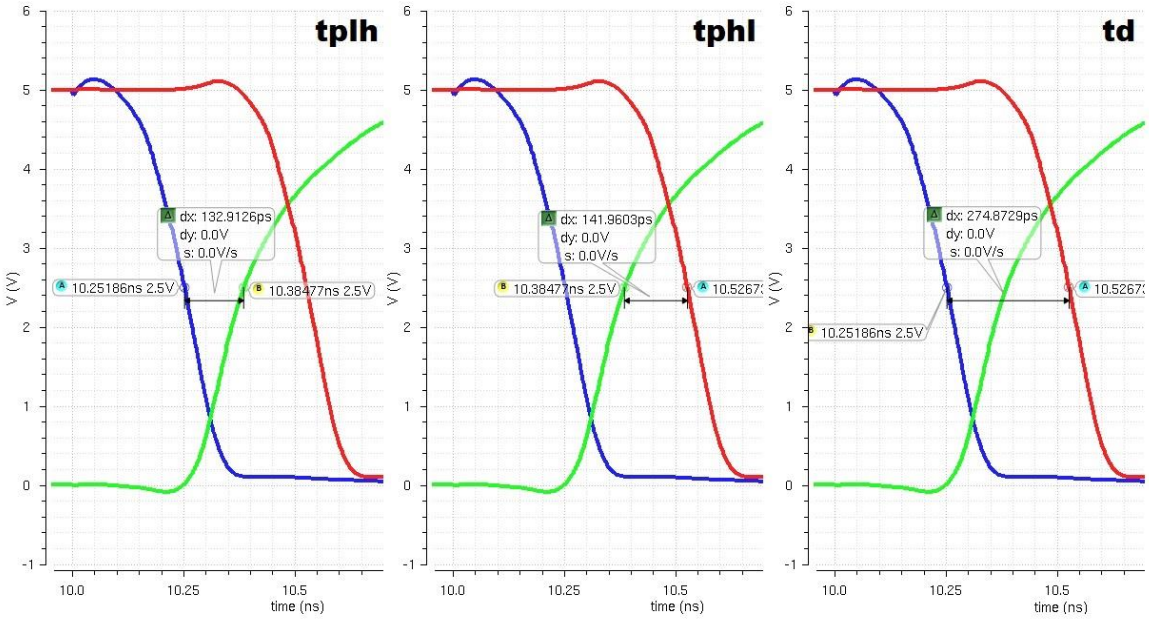


Figure 26 - Unit cell propagation delays for 1.25 V *Vinvc*

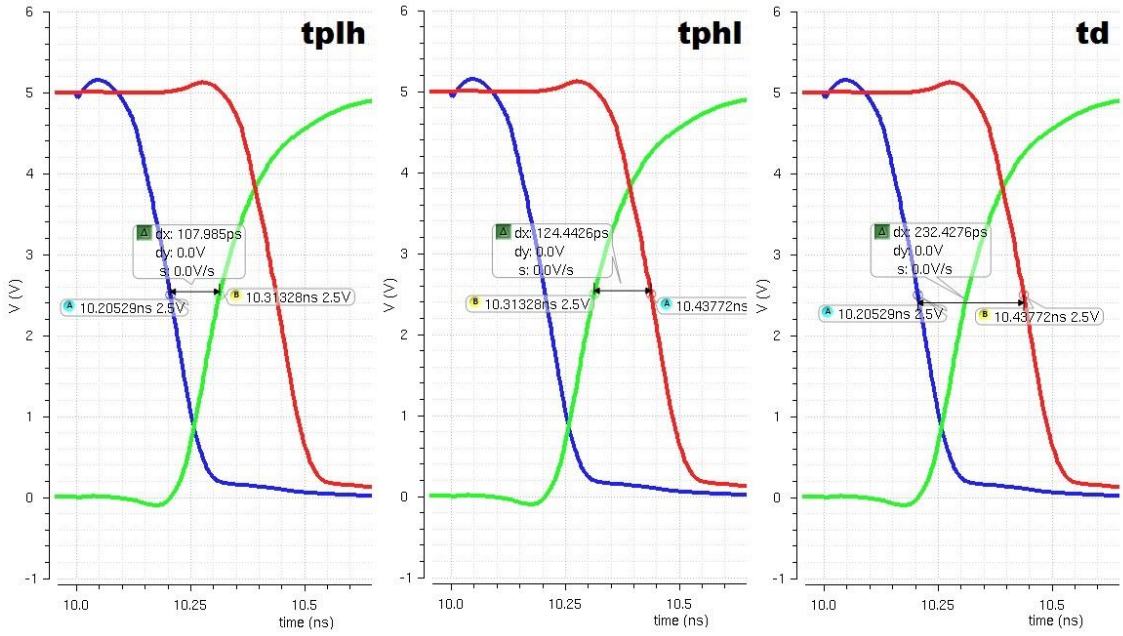


Figure 27 - Unit cell propagation delays for 5 V *Vinvc*

Vinvc	t_{plh} (ps)	t_{phl} (ps)	t_d (ps)	f_{sample} (GHz)
1.10	168.32	168.85	337.17	11.86
1.25	132.91	141.96	274.87	14.55
1.50	116.31	129.70	246.01	16.26
1.75	110.21	125.77	235.98	16.95
2.00	109.29	125.85	234.89	17.03
2.50	108.48	124.73	233.22	17.15
3.00	108.34	124.61	232.95	17.17
5.00	107.99	124.44	232.43	17.21

Table 4 - Unit cell sampling frequency for varying *Vinvc*

The fastest simulated sampling frequency, 17.2 GHz, compares favorably to the theoretical 16.5 GHz determined via the RC model. The simulations indicate an expected range of sampling

frequency from 11.8 GHz up to 17.2 GHz for the case of no bias resistor. Figure 28 displays a line diagram of the time delay versus *Vinvc* for a 4 kΩ resistor and for no resistor. Notice how the delays initially decrease linearly with increasing *Vinvc* before reaching the point where increasing *Vinvc* results in marginal increases in the sampling frequency. This result is expected as it mirrors the behavior of the bias generator as it is swept through its linear region of operation, as seen earlier in Figures 14 and 15. Note, increasing the delay time is a key element of this design, however it is critical that the delay changes linearly. Now that the unit cell time delay has been characterized, the capture stage will be detailed.

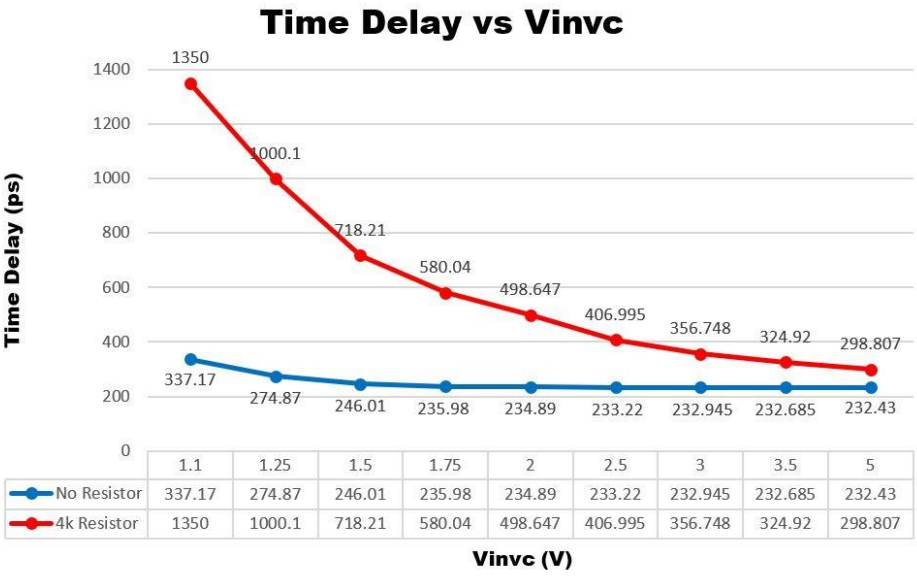


Figure 28 - Time delay versus *Vinvc* for no resistor and a 4 kΩ resistor

3.4 CAPTURE STAGE

The capture stage operation was presented earlier in Section 3.1, however this brief description did not discuss the limitations on the analog input signal, *analog in*, or the range of the output voltage. Figure 29 displays a single capture stage and includes the threshold voltages of NMOS *N5* and PMOS *P4*. To create a scaled representation of *analog in*, two conditions must be satisfied such that *P4* operates in the saturation region.

The first condition requires the source-gate voltage, V_{SG}, of *P4* to exceed the threshold voltage, V_{THP}, such that the device is turned on. This is given by

$$V_{SG} \geq V_{THP} \tag{3.30}$$

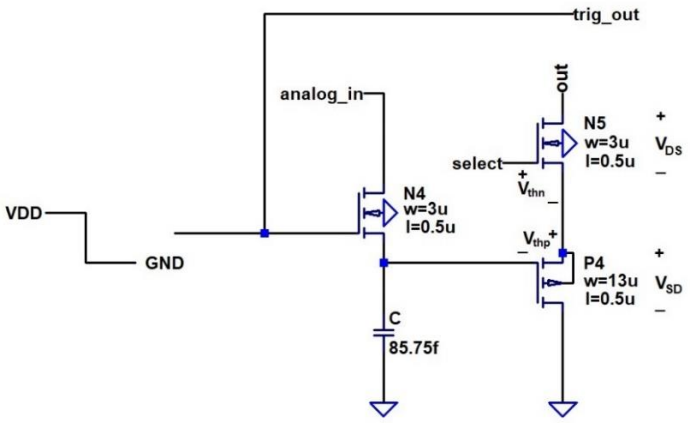


Figure 29 - Unit cell capture stage

Looking at Figure 29, the maximum source voltage of *P4* can be estimated as the difference between the select signal, VDD during readout, and NMOS *N5*'s threshold voltage, V_{THN} , given by

$$V_{S,max} = VDD - V_{THN} \tag{3.31}$$

A point of note is V_{THN} will vary due to body effect resulting from the source and bulk of N5 being at different potentials. *P4* was fabricated in its own well, thus there is no body effect for V_{THP}.

To determine the values of V_{THP} and V_{THN}, a DC operating point simulation of a single capture stage was performed with *analog in* swept from 0 V to 5 V and the operating point fixed at 2.2 V. The simulation schematic and results are displayed in Figures 30 and 31, respectively.

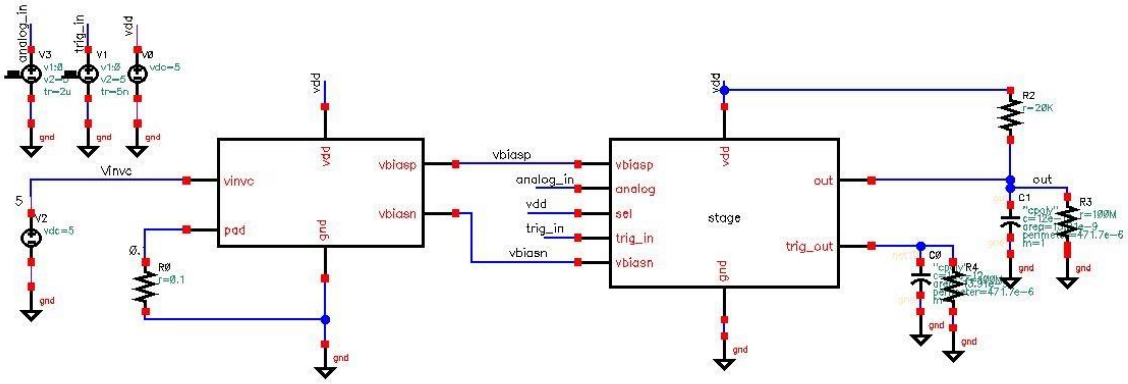


Figure 30 - Individual capture stage simulation schematic

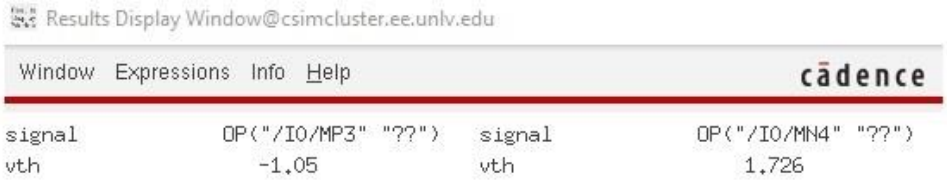


Figure 31 - Operating point simulation results for threshold voltage

Substituting Eq. (3.31) into Eq. (3.30) and rearranging results in

$$VDD - V_{THN} - V_{THP} \geq V_G \tag{3.32}$$

Therefore, the maximum gate voltage allowed for the first condition to be satisfied is

$$5\,V - 1.726\,V - 1.05\,V \approx 2.22\,V \approx 2.2\,V \tag{3.33}$$

Knowing P4's gate can be pulled all the way to ground gives an input signal range of 0 V to 2.2 V.

The second condition to ensure *P4* remains in saturation requires the source-drain voltage, V_{SD}, to be larger than the difference between V_{SG} and V_{THP}, or

$$V_{SD} \geq V_{SG} - V_{THP} \tag{3.34}$$

Knowing the drain of *P4* is tied to ground allows Eq. (3.34) to be rewritten

$$V_S \geq V_S - V_G - V_{THP} \tag{3.35}$$

$$0 \geq -V_G - V_{THP} \tag{3.36}$$

Substituting for the maximum value V_G from Eq. (3.32) results in

$$0 \geq -(VDD - V_{THN} - V_{THP}) - V_{THP} = 0 \geq -VDD + V_{THN} \tag{3.37}$$

These results indicate both conditions for P4 to remain in saturation are satisfied for analog input signals up to approximately 2.2 V.

Next, the maximum and minimum output voltage ranges were calculated and verified via simulations. Reviewing Figure 29, the output voltage range for *analog in* from 0 V to 2.2 V is defined by

$$V_{out} = V_{SD} + V_{DS} \tag{3.38}$$

Simulation results for operating points of 2.2 V and 0 V for V_{DS} and V_{SD} are displayed in Figure 32.

Figure 32 - DC operating points for 0 V and 2.2 V analog input signals

Using the values from Figure 32 in Eq. (3.38) results in the following

$$V_{out,max} = 3.292\ V + 1.688\ V\ \approx 4.98\ V \tag{3.39}$$

$$V_{out,min} = 2.169\ V + 183\ mV\ \approx 2.35\ V \tag{3.40}$$

The capture stage simulation results for a DC sweep of *analog in* confirm the approximations determined in Eq. (3.33), Eq. (3.39), and Eq. (3.40). Figure 33 displays the results with the blue trace representing *analog in* and the green trace representing the output. At 2.2 V, *P4* is at the edge of saturation and entering triode for larger input voltages. The output voltages

of *analog in* at 0 V and 2.2 V are seen to be 2.352 V and 4.98 V, respectively. This means there will be an offset voltage ranging from 2.352 V to 2.78 V. Later in Chapter 5, all simulations will be performed using a maximum 2 V analog input signals to ensure the HSFTD is operating within the limits of its range.

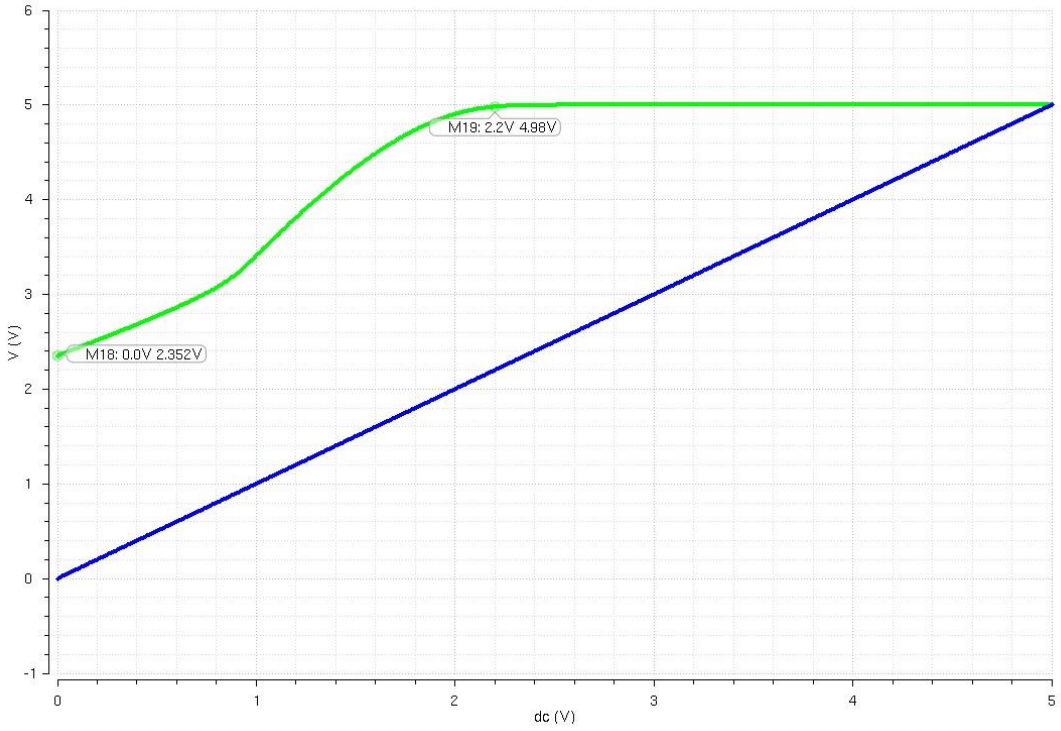


Figure 33 - Capture stage analog input and output voltage range

Another important parameter of interest is the degradation of the unit cell hold capacitor's voltage over time. In simple terms, after the analog input signal is sampled in time and stored on the hold capacitor there will be some amount of loss, or droop, of the sampled data. Some of this loss is due to the off current comprised of leakage through the NMOS switch controlling the capture stage. Leakage occurs through the source and drain implants to substrate, source-to-

drain leakage current, and at the edges of the poly at the edge of the field oxide [9]. Additionally, the source of the capture NMOS will be tied to a positive voltage via the hold capacitor, resulting in some leakage through the reverse biased source to substrate PN junction. The off current for the maximum possible analog input magnitude of 2.2 V was determined to be approximately 2.1 pA via a Cadence simulation. The leakage can then be modeled by

$$\frac{dV}{dt} = \frac{I}{C} = \frac{2.1\ pA}{85.75\ fF} = \frac{24.49\ V}{1\ s} \approx \frac{2.5\ mV}{100\ \mu s} \tag{3.41}$$

This ratio can be used to find the amount of output error in the reconstructed signal by using the amount of time the decoder requires to readout the stages and solving for the voltage over that interval.

The last point of interest in the capture stage is the sizing of the off-chip pull-up resistor connected to VDD. The resistor needs to be sized to allow changes in the output proportional to current such that changes in the current will not result in too much or too little variation in the output. If the pull up resistor is too large, the RC time constant becomes too high and the signal cannot be read out quickly enough. If the resistor is too small, there is not enough swing on the output node to detect variations. To clarify, if the resistor is too small, for example 100 Ω, and the current in the output branch of three consecutive stages is 92 µA, 95 µA, and 98 µA, the voltage drops across the resistor are 9.2 mV, 9.5 mV, and 9.8 mV, respectively. The variations in the output are in the microvolts. If the resistor is too large, for example 50 kΩ, the voltage drops for the same three stages increase to 4.6 V, 4.75 V, and 4.9 V with variations in the hundreds of millivolts. However, the 20 kΩ resistor used in the simulations results in voltage drops of 1.9 V, 2 V, and 2.06

V. This compromise between too small and too large provides a better range for detecting variations in the output voltage.

Using the minimum output voltage, 2.35 V, allows the maximum value pull-up resistor to be determined. The drain current through the PMOS in the capture stage for a 0 V gate voltage can be solved for using Ohm's Law as

$$I_D = \frac{5\ V - 2.35\ V}{20\ k\Omega} = 132.5\ \mu A \tag{3.42}$$

Knowing the minimum voltage allowable on the source for the device to be on is V_{THP}, or 1.062 V, gives the maximum allowable pull-up resistor as

$$R_{pull-up} = \frac{5\ V - 1.062\ V}{132.5\ \mu A} = 29{,}720\ k\Omega \tag{3.42}$$

Resistances larger than 29.7 kΩ do not increase the output swing and only serve to increase the RC time constant and consequently, decrease the maximum rate the signal can be readout.

CHAPTER 4: INTERLEAVING

Chapter 4 focuses on the second difference in the HSFTD design versus the FTD design, specifically the design technique known as interleaving. Recall, the goal of interleaving is to minimize the delay between successive unit cells such that the theoretical sampling frequency of the HSFTD is four times faster than the FTD rate. Section 4.1 details the arrangement of a bank of 64 unit cells and Section 4.2 focuses on the design of the trigger generator. Section 4.3 explains the fundamental concept of interleaving relative to the HSFTD design and lastly, Section 4.4 discusses the on-chip decoder designs used to sequentially read out the 256 capture stages.

4.1 BANKS

Now that the unit cell design and operation has been presented, the next step is to discuss how the banks are designed. A bank consists of a 6:64 decoder and 64 unit cells routed such that an input pulse, *trig_in*, received by the current-starved inverter in the first unit cell propagates sequentially through all 64 stages in the bank. As an example, consider the two unit cells in Figure 34. The signal *trig_in* propagates through the two inverters in unit cell 1 before reaching the gate of NMOS, *N3*, acting as the switch for the capture stage. The gate of *N3* is also tied to the input of the current-starved inverter in unit cell 2, therefore the signal serves as *trig_in* for unit cell 2 at the same time it is switching *N3* off and sampling *analog_in*. In this manner, the capture sequence repeats itself for unit cell 2 with *N8* switching off and the signal *trig_out* serving as the trigger input for the next iterative unit cell.

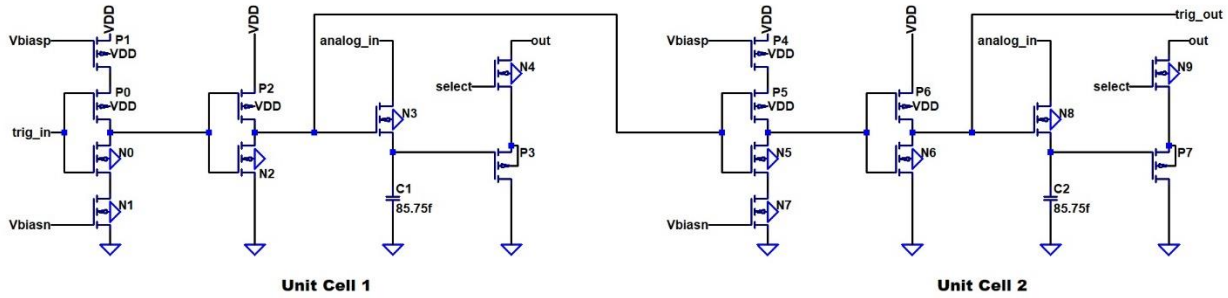


Figure 34 - Bank connection of two unit cells

Earlier in Chapter 3, the time delay for a single unit cell was determined to be approximately 243 ps, Eq. (3.28). The time delay through a bank of 64 unit cells is then given by

$$t_{d,bank} = 243\ ps * 64 \approx 15.55\ ns \tag{4.1}$$

To confirm this approximation, the simulation performed earlier to determine the propagation delay for an individual unit cell was repeated for a bank of 64 cells with results shown in Figure 35. The results confirm a 15.59 ns time delay.

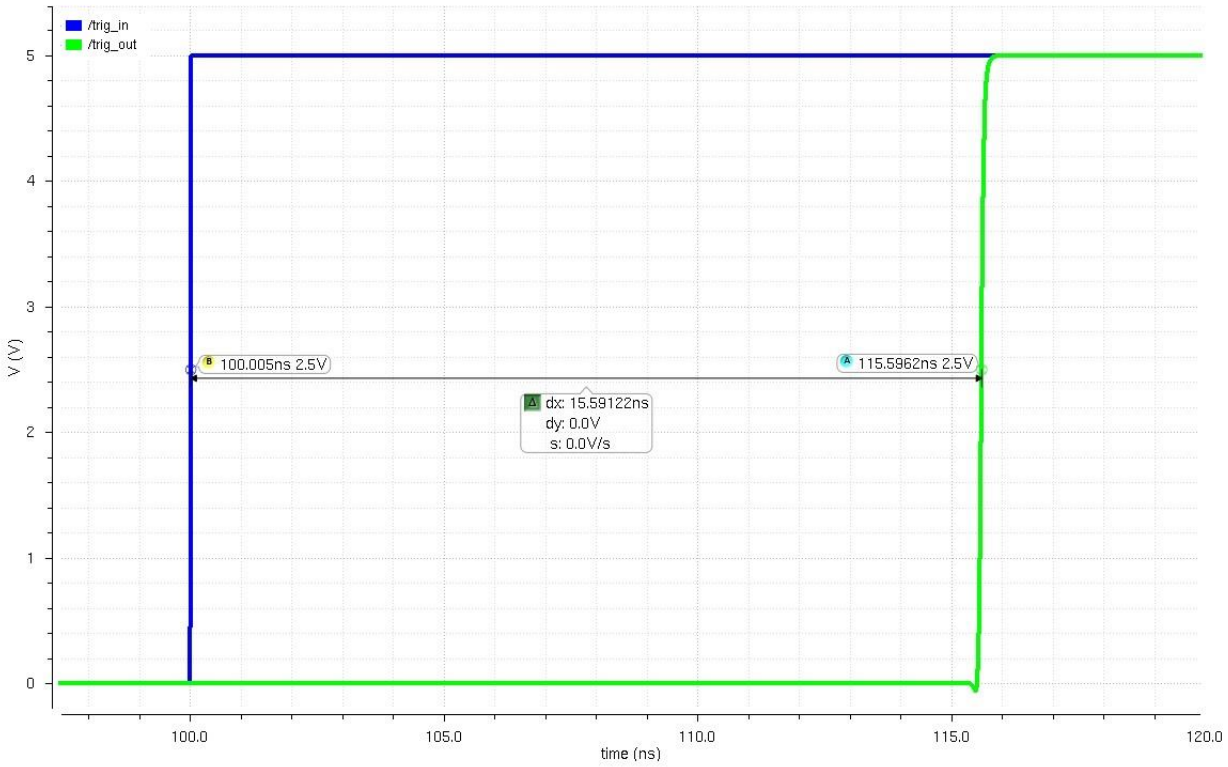


Figure 35 - Simulation results for the time delay through a bank of 64 unit cells

The Cadence layout view of the full bank of 64 unit cells is displayed in Figure 36 and includes the 6:64 decoder. Figure 37 shows a closer view of the first few unit cells in the layout and identifies the components seen in the full view in Figure 36.

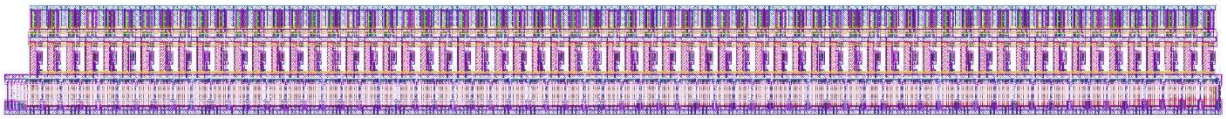


Figure 36 - Bank layout in Cadence

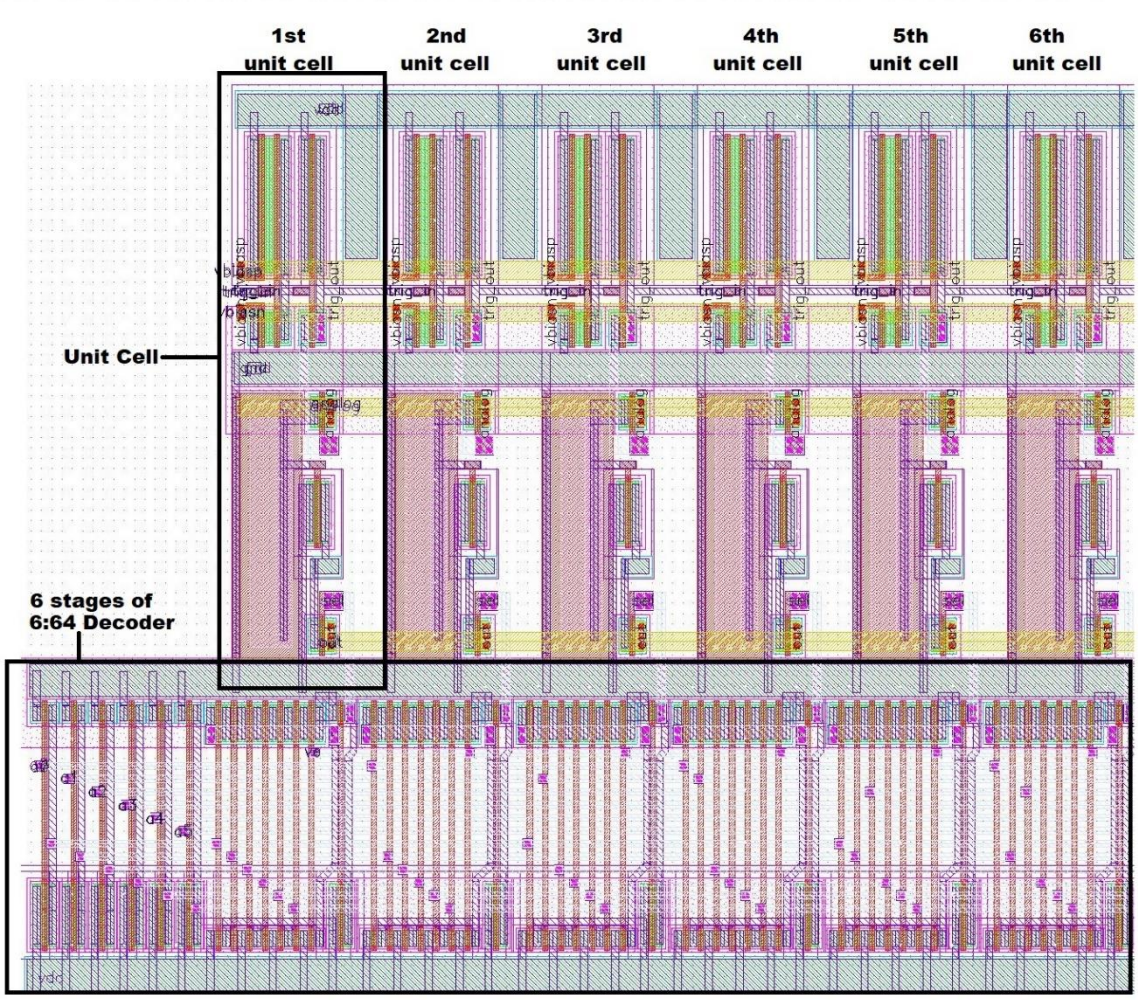


Figure 37 - Close view of bank layout

4.2 TRIGGER GENERATOR

Using four banks requires the creation of four separate, single-trigger events with a precise time delay between each trigger to start the iterative capture process. The trigger generator is designed to receive a single, externally generated high-to-low signal and output four separate high-to-low trigger signals spaced evenly apart in time. The trigger generator unit cell, schematic

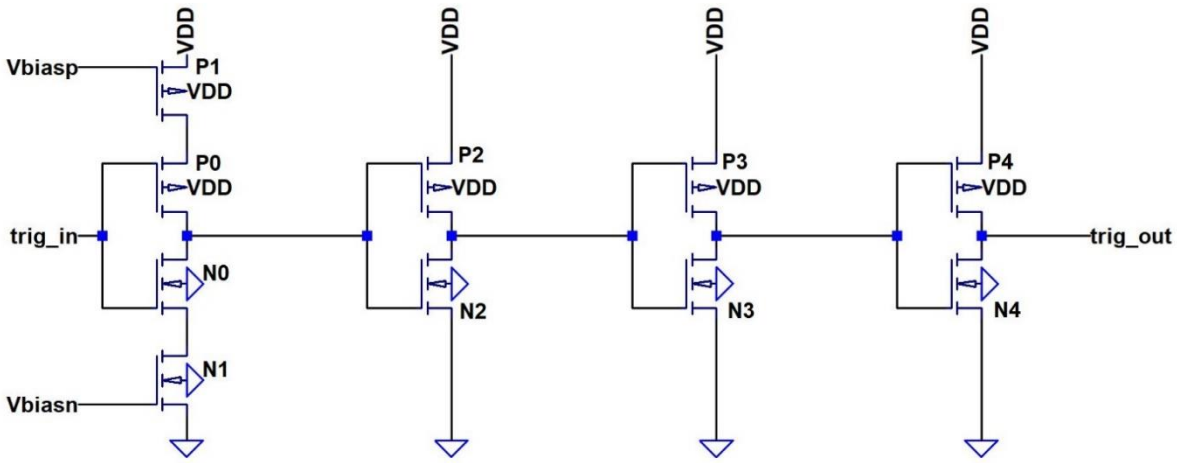


Figure 38 - Trigger generator unit cell

view seen in Figure 38, consists of a single current-starved inverter and three additional basic inverters included to both add delay and sharpen the signal. The Cadence layout view of the trigger generator unit cell is displayed in Figure 39. The same characteristics developed for inverters in Chapter 3 govern the behavior of the trigger generator and therefore will not be included here.

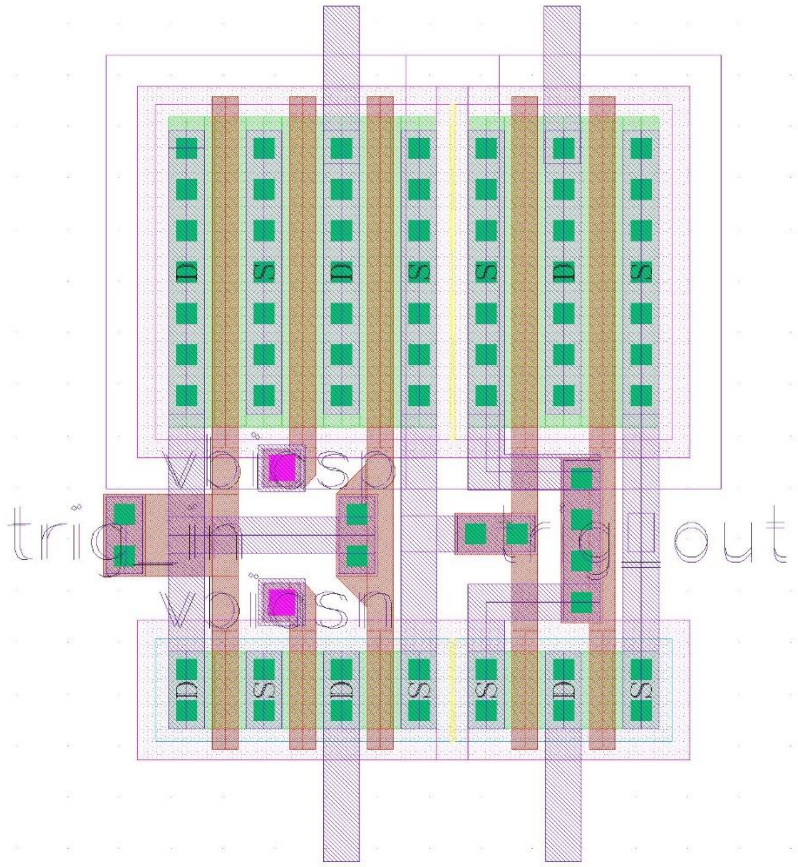


Figure 39 - Trigger generator unit cell layout in Cadence

Generating four separate triggers requires the use of four trigger generator unit cells, each with a separate bias generator and a separate external control voltage, *Vinvc*. Figure 40 displays a schematic view of the composite trigger generator circuit as a reference. Each unit cell shares the same input signal, *trig_in*, a high-to-low pulse feeding into each current-starved inverter. *Trig_in* propagates though the three basic inverters in each path such that the outputs, *trig_out 0-3*, all have the same logic as the input pulse. The control voltages, *Vinvc 0-3*, are set to four different DC voltages that are descending in magnitude starting with *Vinvc 0* as the largest and ending with *Vinvc 3* as the smallest. All four bias resistors are of equal value.

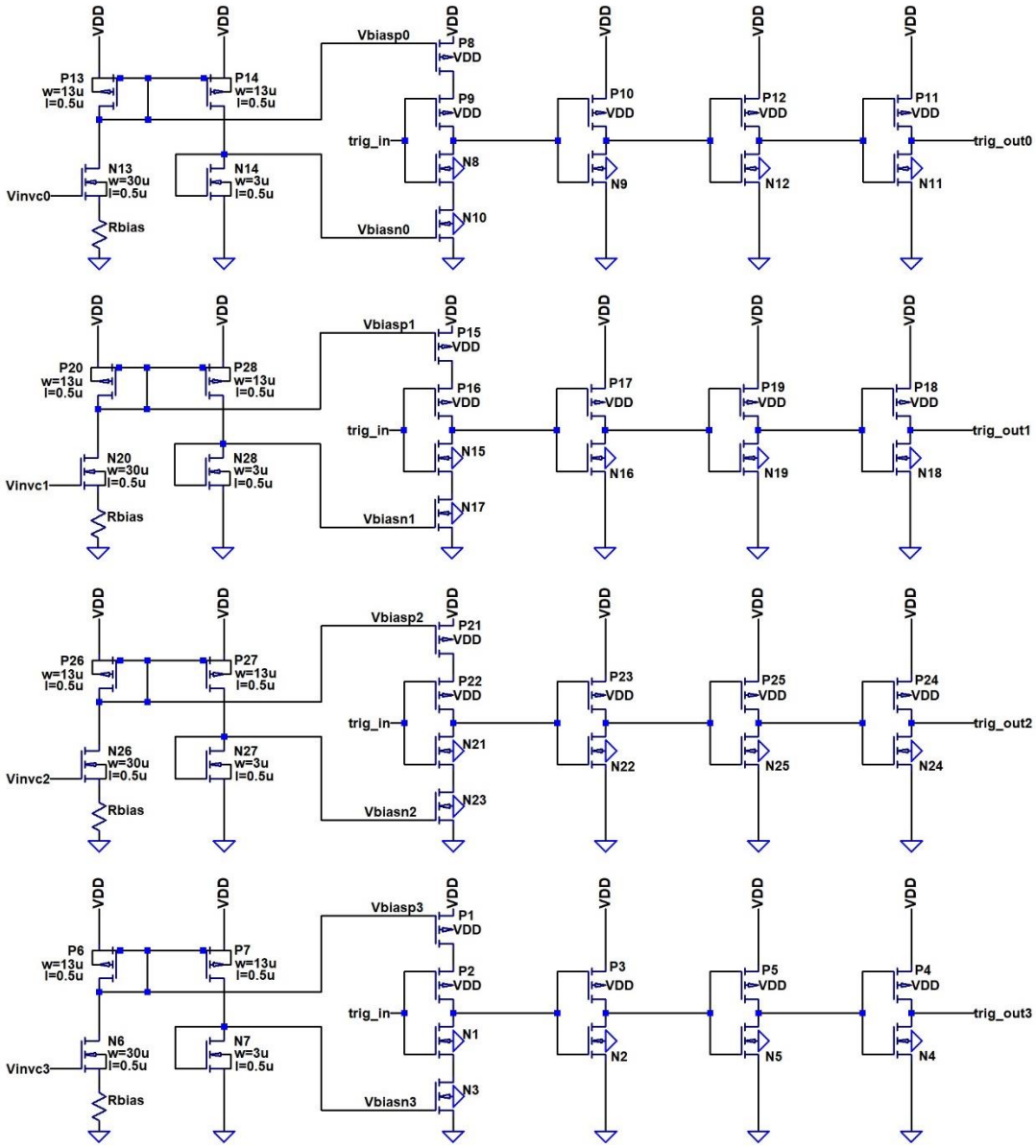


Figure 40 - Trigger generator schematic

Decreasing the magnitudes of each successive *Vinvc* has the effect of slowing the propagation delay through each path due to each current-starved inverter having different bias voltages, *Vbiasp* and *Vbiasn*. The time delay between the four output signals is therefore

dependent upon the value of *Vinvc* and the size of the bias resistors. Assuming proper tuning of *Vinvc 0-3*, the output signals exit the cell in the order *trig_out 0, trig_out 1, trig_out 2,* and *trig_out 3,* with an equivalent delay between each signal.

The desired time delay between trigger signals is dependent upon the capture rate through a single unit cell as set by the control voltage biasing the banks, *Vinvc 4*. As discussed in Chapter 3, Eq. (3.28), the minimum time delay between unit cells is approximately 243 ps for *Vinvc 4* set to 5 V. To achieve a sampling rate four times this speed requires four triggers separated by approximately 60.75 ps, or one-fourth of 243 ps.

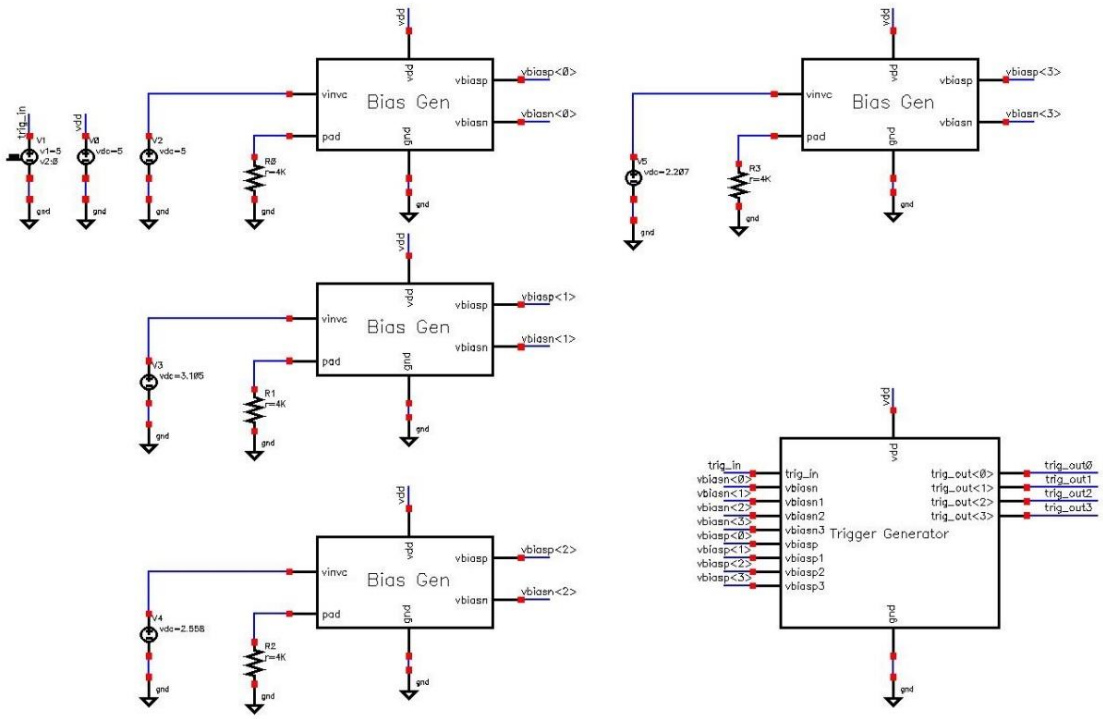


Figure 41 - Trigger generator simulation schematic

To confirm the theory behind the trigger generator, simulations were performed with *Vinvc 4* set to 5 V and *Vinvc 0-3* tuned to the voltages required to create equivalent 60 ps delays between the output signals. The simulation schematic and results are displayed in Figures 41 and 42, respectively. Note the tuned bias generator voltages *Vinvc 0-3* are included on the schematic at values of 5 V, 3.105 V, 2.558 V, and 2.207 V, respectively. If *Vinvc 4* is adjusted such that the

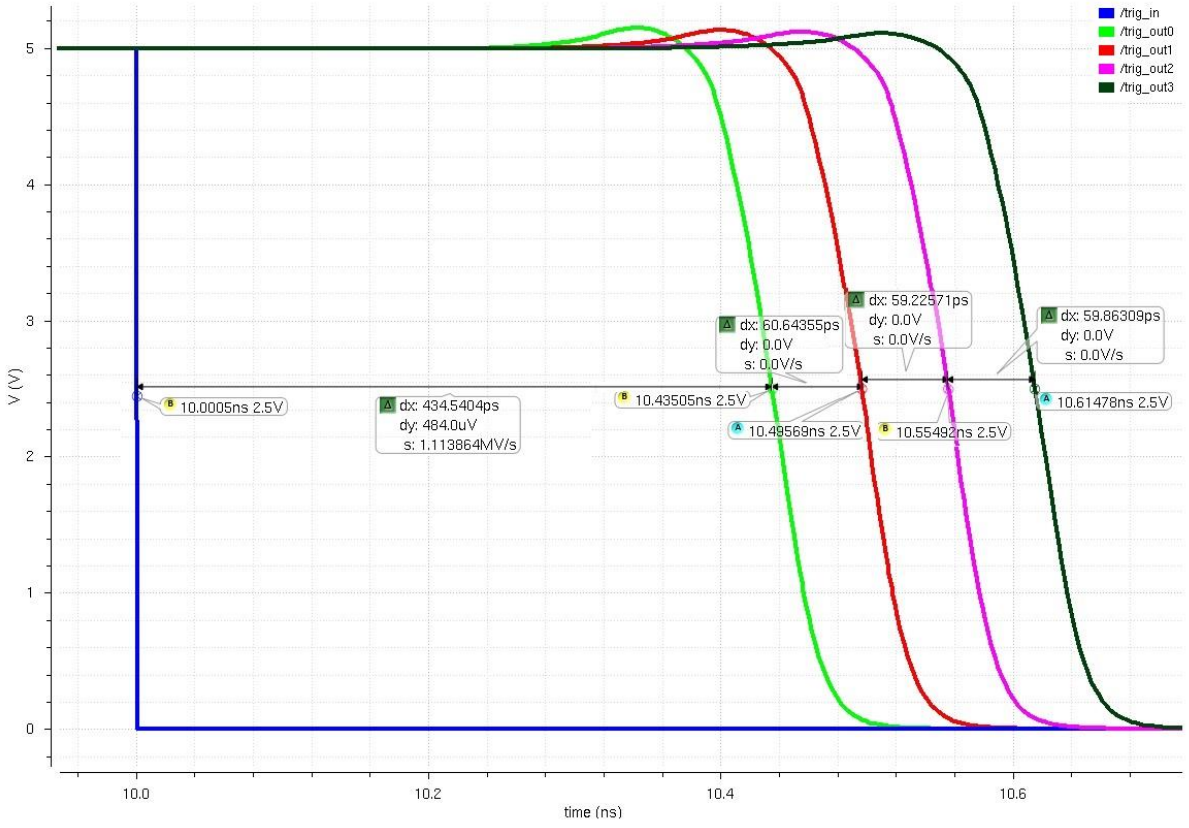


Figure 42 - Trigger generator simulation results for 16.6 MHz capture rate

capture rate through the unit cells changes, then *Vinvc 0-3* need to be retuned until the delay between each trigger signal is one-fourth the time delay between unit cells. The results in Figure 42 show there are four separate *trig_out* signals with an approximate delay of 60 ps ±800 fs

between each output signal. This results in an approximate sampling rate of 16.6 GHz. An additional point of interest is the 434 ps delay between *trig_in* transitioning high-to-low and the first trigger output, *trig_out 0,* transitioning. For specific applications, such as measurement or radar systems, accounting for this latency period is required for proper timing.

Recall the unit cell sampling rate is set by *Vinvc 4*, therefore the trigger generator needs to be tunable for slower capture rates, as well. As an additional verification, a simulation was performed with *Vinvc 0* arbitrarily lowered to 4 V and *Vinvc 1-3* tuned to create equivalent delays for each trigger at approximately 2.26 V, 2.06 V, and 1.75 V, respectively. The simulation results demonstrating four separate triggers with a delay of approximately 104 ps$\pm$400 fs, or a sampling frequency of 9.6 GHz, are displayed in Figure 43. In Chapter 3, the theoretical range for the sampling frequency using no bias resistor for bias generator 4 was determined to be between 11.8 GHz and 17.2 GHz, so the trigger generator is capable of operating across the range of focus. However, it is important to remember the range of operation varies with both changes in *Vinvc* and the value of *Rbias.*

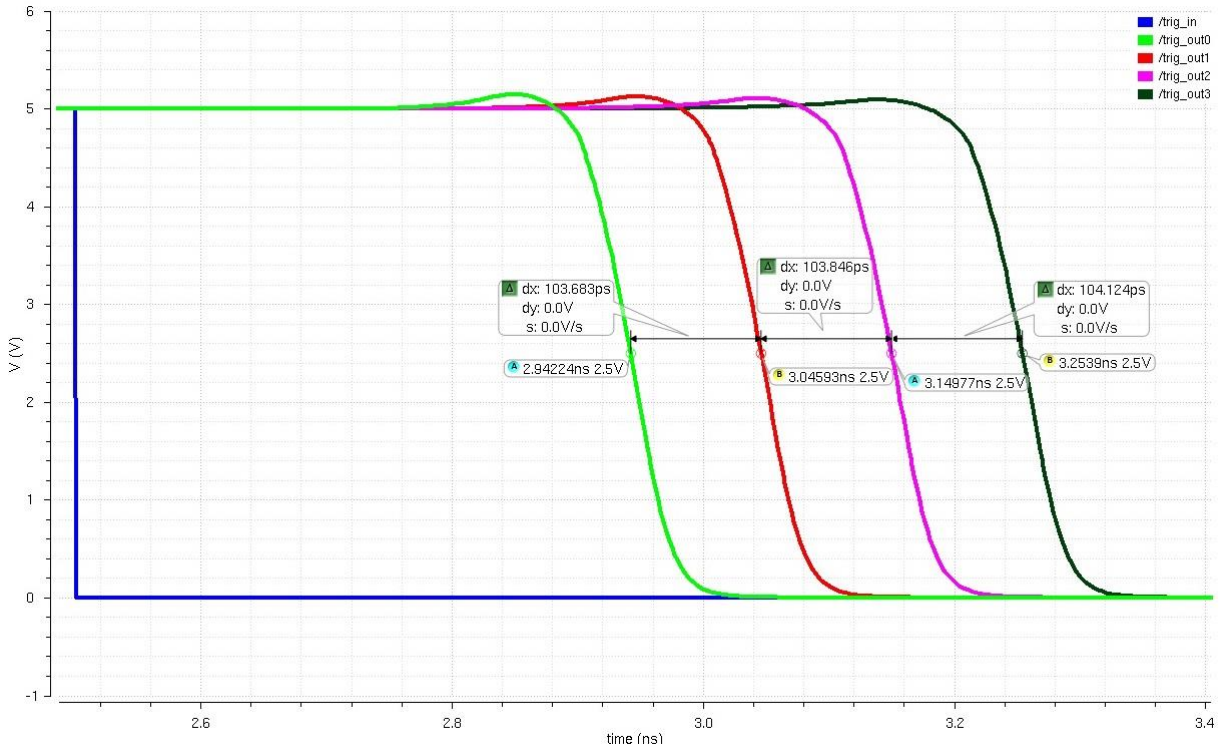


Figure 43 - Trigger generator simulation results for 9.6 GHz sampling frequency

4.3 INTERLEAVING

Interleaving was introduced in Chapter 1 as the second difference between the HSFTD and the FTD designs with the first difference being the HSFTD's ability to vary the sampling frequency. The goal of interleaving using four banks is to minimize the time delay between successive unit cells in the HSFTD, thus resulting in a theoretical sampling frequency approximately four times the FTD rate. A qualitative understanding of interleaving is required prior to demonstrating how the sampling frequency increases using this technique.

To begin, consider a HSFTD designed with 256 sequential unit cells, as in the FTD, and a

total delay from the trigger input pulse to the trigger output after passing through all 256 unit cells defined by

$$t_d = t_{d,unit\ cell} * 256 = 240\ ps * 256 \approx 61.44\ ns \quad (4.2)$$

This means only one unit cell is operational at any given point in time with the overall speed limited by the time delay through the unit cell and the number of stages. Therefore, using our fastest calculated time delay from Chapter 3 of approximately 240 ps, the total delay through all 256 unit cells would be 61.44 ns for a sampling frequency of 4.2 GHz. Figure 44 uses a block diagram of 256 successive unit cells within the same bank to illustrate this point.

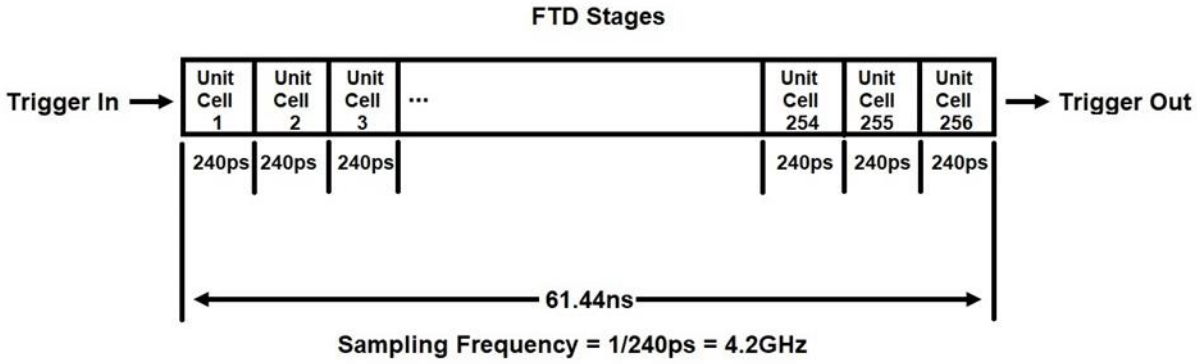


Figure 44 - Block diagram illustrating the FTD sequential capture sequence

In practical terms, unit cell 2 is unable to sample the analog input signal until unit cell 1 is finished sampling, or 240 ps after unit cell 1 receives the *Trigger In* signal. Similarly, unit cell 3 cannot sample until unit cell 2 is finished sampling, or 480 ps after unit cell 1 receives *Trigger In*. In this manner, the FTD design is limited to a maximum sampling rate of 4.2 GHz, or 240 ps per

unit cell, since only one cell can be active at any given time.

Using interleaving banks allows for multiple unit cells to be active over a single 240 ps delay and results in an increase in sampling frequency relative to the number of banks used in the design. Since the HSFTD design uses four interleaving banks of 64 unit cells, an example of the technique using four banks is included to provide clarity. Figure 45 displays a block diagram illustrating the fundamental concept of interleaving. The first unit cell is denoted unit cell 0 to account for the

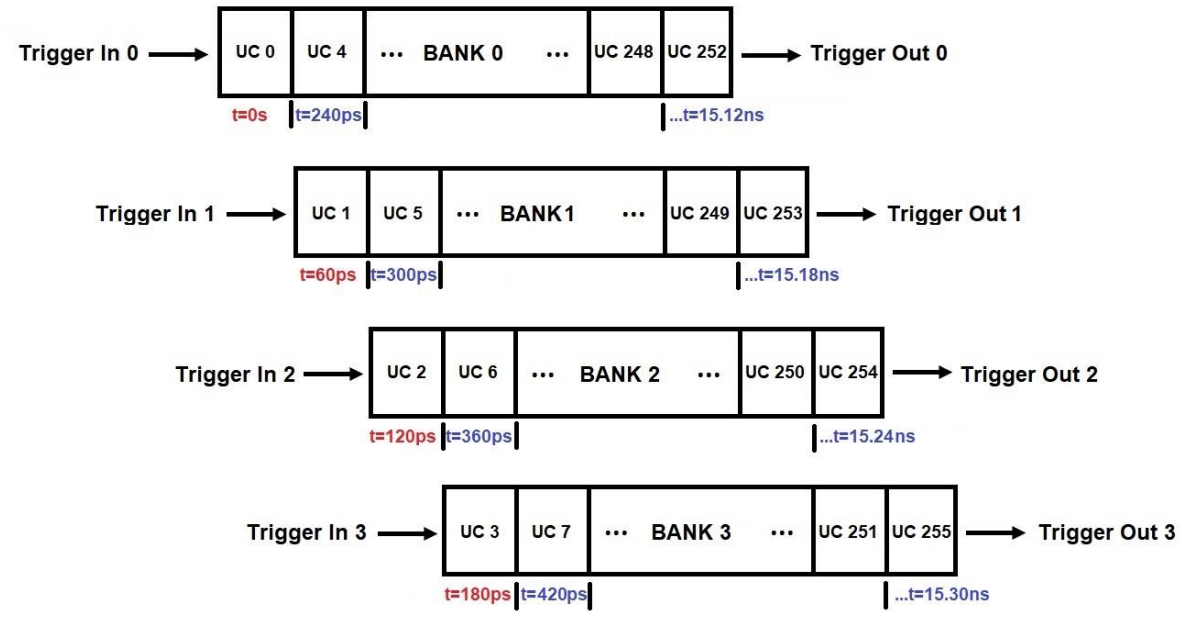


Figure 45 - Block diagram conceptualizing interleaving

use of the number 0 in logic design. This means the unit cells are numbered sequentially from 0, the first unit cell, to 255, the last cell, for 256 total sampling stages.

The interleaving technique requires sequential unit cells to be placed in separate banks such that unit cell 0, denoted *UC 0*, is the first cell in *Bank 0*, the next sequential unit cell, *UC 1*, is

the first cell in *Bank1*, *UC 2* is the first cell in *Bank 2*, and *UC 3* is the first cell in *Bank 3*. Since there are only four total banks being used in the design, the next sequential unit cell, *UC 4*, starts the process over again as the second unit cell in *Bank 0.* It is important to clarify *UC 4* is the second unit cell in *Bank 0*, but relative to sampling the analog signal, *UC 4* is the fifth sequential cell in the capture process following unit cells 0-3. The process iterates with *UC 5, UC 6*, and *UC 7* placed in *Bank 1, Bank 2,* and *Bank 3*, respectively. *UC 8* returns the sequence to *Bank 0* and the process continues until all four banks have 64 unit cells for a total of 256 capture stages.

Returning to the trigger generator, each bank receives a separate trigger signal starting with *Trigger In 0* into *Bank 0* at a reference time of 0 s, followed by *Trigger In 1* into *Bank 1* at 60 ps, then *Trigger In 2* into *Bank 2* at 120 ps, and lastly, *Trigger In 3* into *Bank 3* at 180 ps. Recalling there is a 240 ps delay between successive unit cells within a bank highlights the point of interleaving. Specifically, after an initial 180 ps latency period, each bank has a single unit cell actively capturing at any given point in time. This results in four total unit cells active at any given time versus one active cell using only a single sequential bank. At 180 ps, *UC 0*, *UC 1*, *UC 2*, and *UC 3* are all active and separated in time by 60 ps. When *Trigger In 0* propagates through *UC 0* and triggers *UC 4* at 240 ps, *UC 1*, *UC 2*, *UC 3* and *UC 4* are all active and *UC 0* has finished capturing the first sample of the analog input signal. At 300 ps, *Trigger In 1* has propagated through *UC 1* and captured the second sample and triggered *UC 5* such that *UC 2*, *UC 3*, *UC 4* and *UC 5* are active. The process repeats with the end result being each sequential unit cell is now separated in time by 60 ps, rather than 240 ps, thus effectively increasing the sampling rate by a factor of four.

The total delay through all 256 unit cells using interleaving is defined by

$$t_d = t_{d,unit\ cell} * \frac{256}{4} + 180ps = 240\ ps * \frac{256}{4} + 180\ ps\ \approx 15.54\ ns \tag{4.3}$$

Referencing Figure 45, the signal *Trigger In 3* enters the last unit cell, *UC 255*, at 15.30 ns and exits 240 ps later at 15.54 ns. This means the effective time delay per unit cell is

$$t_{d,unit\ cell,interleave} = \frac{15.54\ ns}{256\ stages} \approx 60.7\ ps \tag{4.4}$$

for an effective sampling rate of

$$f_{sample} = \frac{1}{60.7\ ps} \approx 16.5\ GHz \tag{4.5}$$

Interleaving effectively enables the HSFTD design to encompass approximately the same layout area as the FTD with marked improvements in speed. The main drawback to interleaving is the requirement of trigger signals precisely separated in time by the tens of picoseconds to avoid multiple unit cells sampling the same portion of the analog input signal at the same time. The success of interleaving in the HSFTD design is therefore dependent upon the precision of the bias generator control voltages and bias resistors in creating precisely separated trigger signals.

4.4 DECODERS

Once the analog signal input signal has been sampled in time and stored, the HSFTD design uses a single 2:4 decoder and four 6:64 decoders to enable readout of the captured signal. The sampled signal can be readout at a frequency set by an off-chip 8-bit counter enabling the decoders. This

allows the sampled high-speed signal to be slowed, or stretched, as desired upon reconstruction. The schematic and layout views of the 2:4 decoder are included in Figures 46 and 47, respectively.

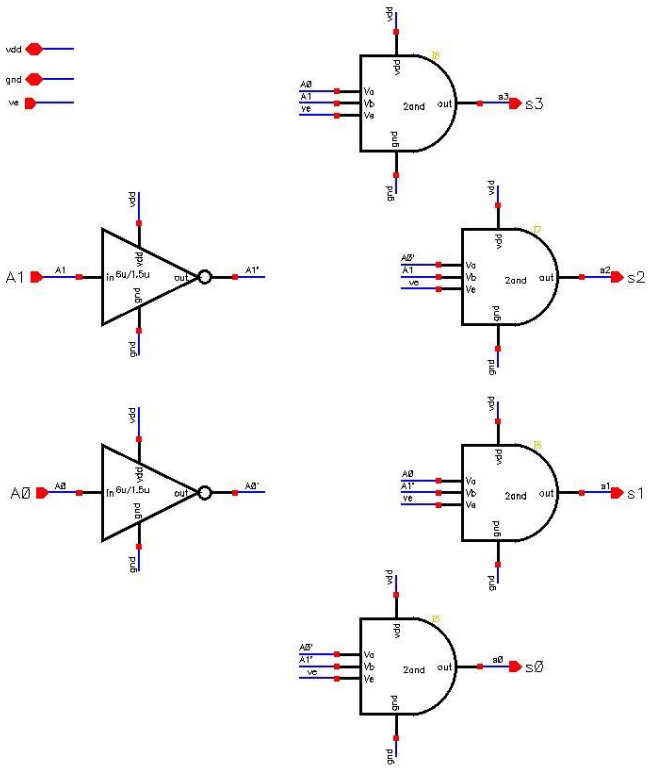


Figure 46 - 2:4 decoder schematic

The two LSBs coming in from the counter, *A0,* the lowest bit, and *A1,* each feed into an inverter to create the necessary logic signals for each of four separate 3-input AND gates. The AND gate outputs, *S0-S3,* serve as enable signals for the 6:64 decoders in the four banks and are therefore used to toggle between the four banks. The input 00 results in a high signal output at *S0* with outputs *S1-S3* all low, thus enabling the 6:64 decoder in bank 0. Similarly, a 01 input enables bank 1, 10 enables bank 2, and 11 enables bank 3. Using the LSBs for this purpose ensures

the sequential readout of capture stages from the four banks. As an extra note, the third input on the AND gate is simply an enable signal set high during readout.

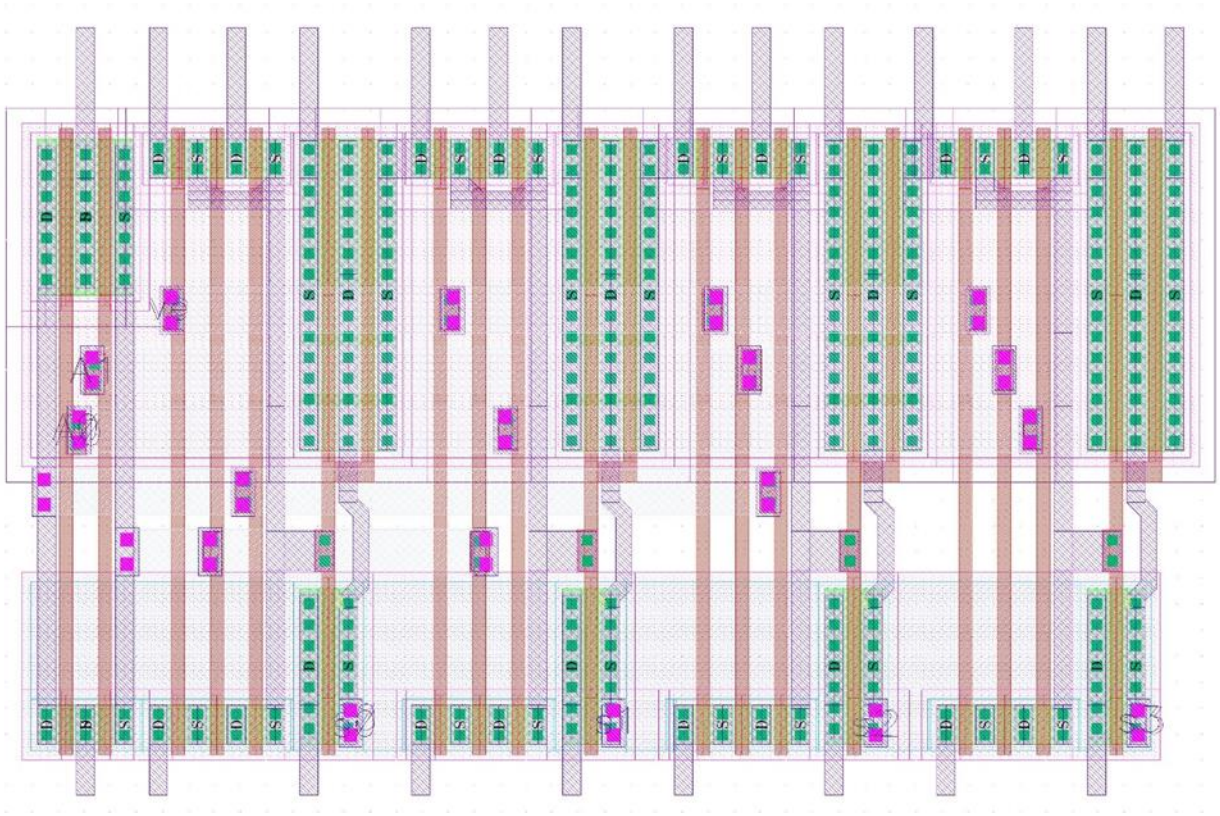


Figure 47 - 2:4 decoder layout view in Cadence

The four 6:64 decoders use the remaining 6 bits from the 8-bit counter to readout the data from the 64 unit cells within each bank. Figure 48 demonstrates how the 8-bits are applied to each bank such that the readout results in sequential reconstruction of the sampled signal. The inputs *A7-A0* are given as decimal values next to their binary equivalents for the numbers 0-8 to demonstrate how the decoders read through the banks and unit cells sequentially. Recalling *U0*

Decoder Readout Sequence

Decimal Value	Binary Value A7-A2	A1-A0	
0	000000	00	represents the 1st cell in bank 0 U0
1	000000	01	represents the 1st cell in bank 1 U1
2	000000	10	represents the 1st cell in bank 2 U2
3	000000	11	represents the 1st cell in bank 3 U3
4	000001	00	represents the 2nd cell in bank 0 U4
5	000001	01	represents the 2nd cell in bank 1 U5
6	000001	10	represents the 2nd cell in bank 2 U6
7	000001	11	represents the 2nd cell in bank 3 U7
8	000010	00	represents the 3rd cell in bank 0 U8.....
	6:64	2:4	

Figure 48 - Decoder readout process

represents unit cell 0 located in bank 0, it is clear the counter starting at 000000 00 results in the first cell in bank 0, *U0*, being readout first. Next, the 8-bit counter increments to binary 1, 000000 01, and *U1* in bank 1 is readout. This sequence continues until the counter reaches binary 111111 11, or 255, resulting in *U255* in bank 3 being readout and the process ends with a stretched, reconstructed sample of the original analog input signal.

The 6:64 decoder uses the same design structure as the 2:4 decoder scaled to six inverters and six AND gates with the same fundamental operation. Figure 49 displays the Cadence layout view of the full 6:64 decoder with a closer view provided earlier in Figure 37.

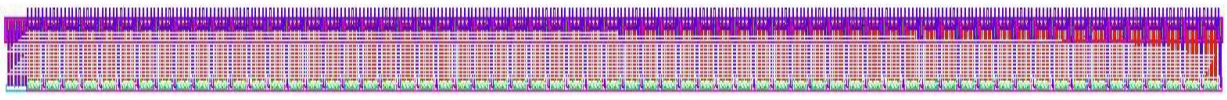


Figure 49 -- 6:64 decoder layout view in Cadence

CHAPTER 5: HSFTD SCHEMATICS AND SIMULATIONS

Now that the components and operation of the HSFTD have been explained in the preceding chapters with theoretical expectations calculated, the next step is to detail the top level design simulation results. Recall, the goal of the HSFTD is to receive an analog input signal, capture samples of the signal in the unit cells, and reconstruct a copy of the sampled signal at a slower rate set by the speed of an off-chip counter tied to the on-chip decoders. The simulation results will serve as a comparative model for the calculated results with a summary of both included at the end of the chapter.

A point of note regarding the decoder readout rate for the simulations is required for clarity. All simulations were performed with the decoder readout at an unreasonably fast rate of 400 MHz. This was intentionally done due to the excessive length of time required for simulations performed at slower rates. For example, the simulations performed in Section 5.1 were 1 µs transient simulations at a 400 MHz readout rate and took in excess of 24 hours, thus increasing the probability of Cadence crashing sometime during simulations. Additionally, decoding at the faster rate allowed for the input signal and stretched output to be scaled and shown on the same plots. However, the drawback to decoding at this rate is the high speed results in a lack of settling and distortion in the output signal. For example, the RC constant on the output with a 500 fF output capacitance and a 20 kΩ pull-up resistor would be 10 ns. Additionally, there exists a nonlinear RC constant associated with the pulldown resistances of the NMOS and PMOS devices

in the capture stages. These factors impact the settling time and add distortion and nonlinearities to the output signal, but were considered a necessary compromise to provide simulated results.

5.1 SINUSOIDAL INPUT

The simulation results discussed in this section all use a sinusoidal *analog_in* signal to demonstrate the HSFTD operation. Two simulations were performed with a sinusoid using a 1 V amplitude and a 1 V offset voltage to remain within the 2.2 V input signal range determined earlier in Section 3.4. The two simulations included *analog_in* at frequencies of 20 MHz and 320 MHz to demonstrate the ability of the HSFTD to perform as designed over different frequencies. Another important note is the adjustable control voltage used to set the sampling frequency, *Vinvc 4*, was set to 5 V for the maximum sampling rate. The simulation schematic for all simulations performed in Chapter 5 is seen in Figure 50. The five bias generators are seen on the left, the trigger generator and 2:4 decoder are seen in the middle and the four banks are seen on the right with all the bank outputs tied to a 20 kΩ pull-up resistor on the top right.

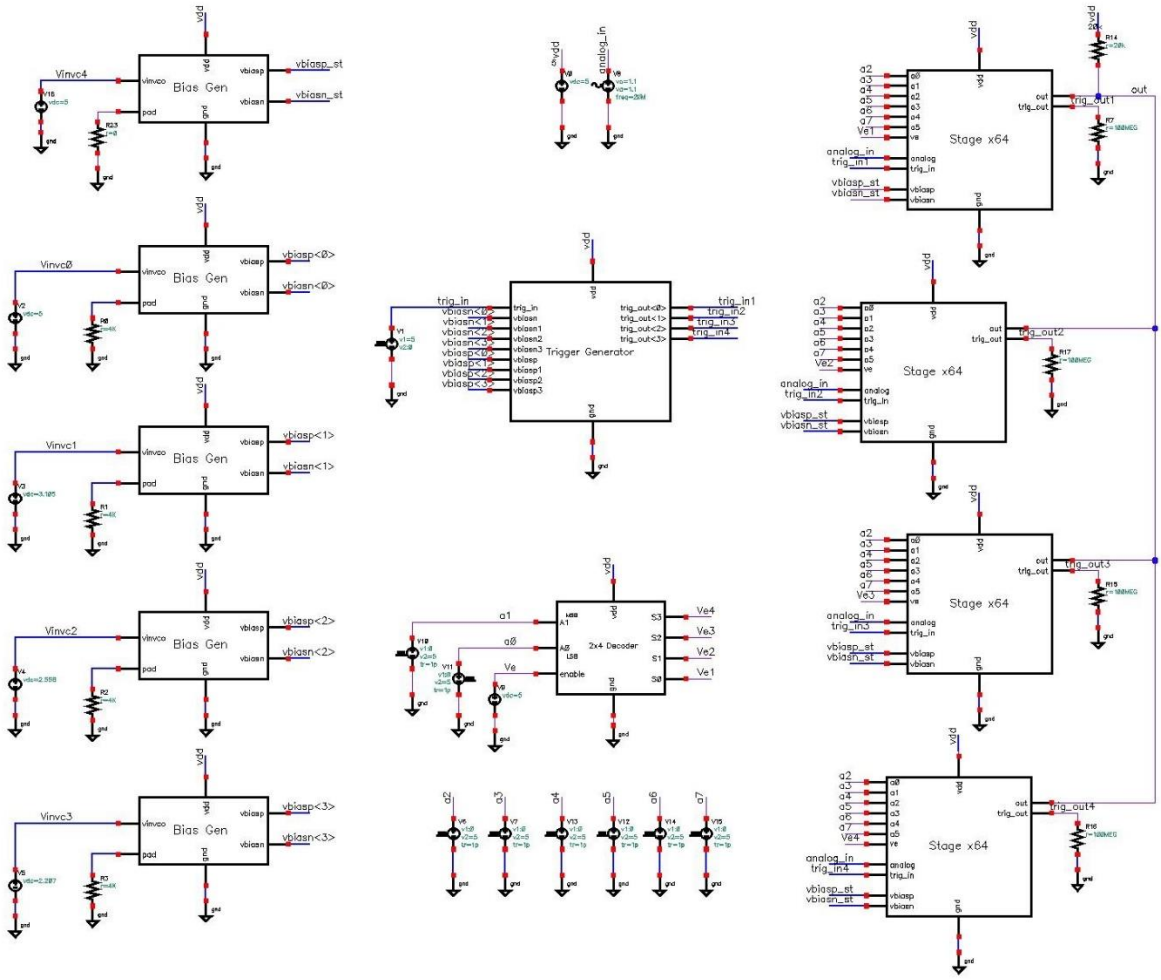


Figure 50 - Top level HSFTD simulation schematic

Figure 51 displays the capture window, defined between *trig_in 1* and *trig_out 4*, and *analog_in* at 20 MHz centered around 1 V. Note the capture window is 14.99 ns for 256 unit cells resulting in a sampling frequency of 17.1 GHz. This compares favorably to the 15.55 ns calculated in Eq. (4.1) for a corresponding sampling frequency of 16.4 GHz. Next, the stretched, reconstructed output signal, *out*, is added in Figure 52. The output signals for all simulations in this chapter are decoded at a rate of 2.5 ns per stage, or 400 MHz starting at 50 ns. Accounting

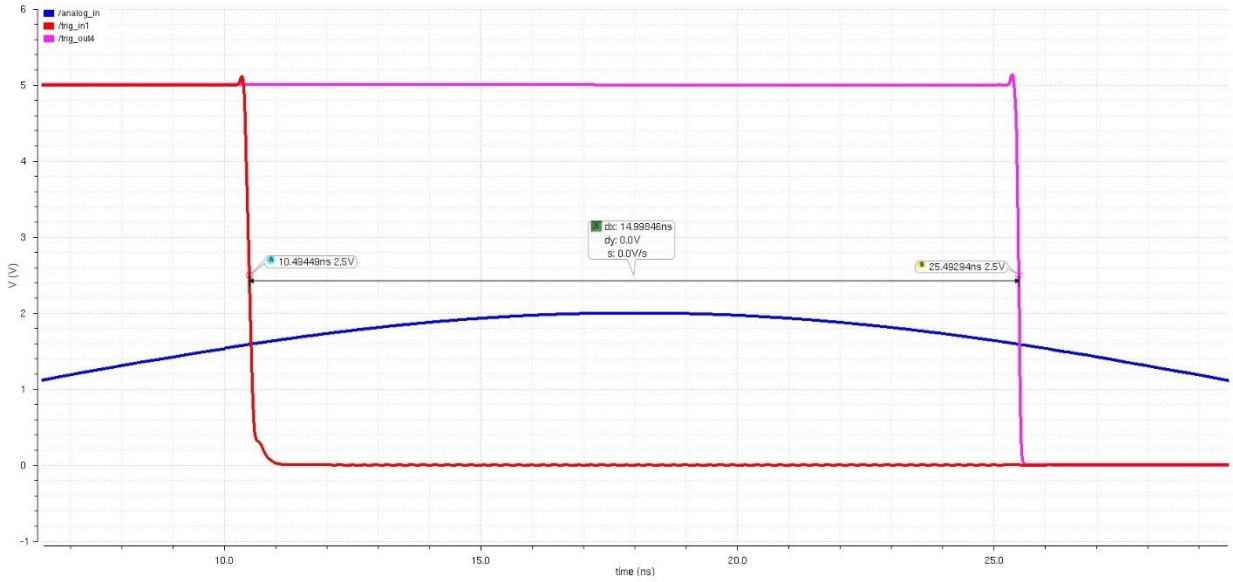


Figure 51 - *Analog_in* sample within capture window for 20MHz simulation

for unit cell 0 being decoded at 50 ns, the total time to decode 256 stages is given by

$$255 * 2.5ns = 637.5\,ns \tag{5.1}$$

Looking at the results in Figure 52, the reconstructed sample is seen starting at 50 ns and ending at 687.5 ns. At this time, the counter returns to zero and the sample is decoded again. The reconstructed sample is a stretched representation of the sample seen in the capture window in Figure 51 and proportionately scaled down in Figure 52. In Chapter 3, the amount of droop, or loss of data, was calculated in Eq. (3.41) to be approximately 2.5 mV/100 µs. At a total readout time of 637.5 ns, this equates to an output error of approximately 16 µV.

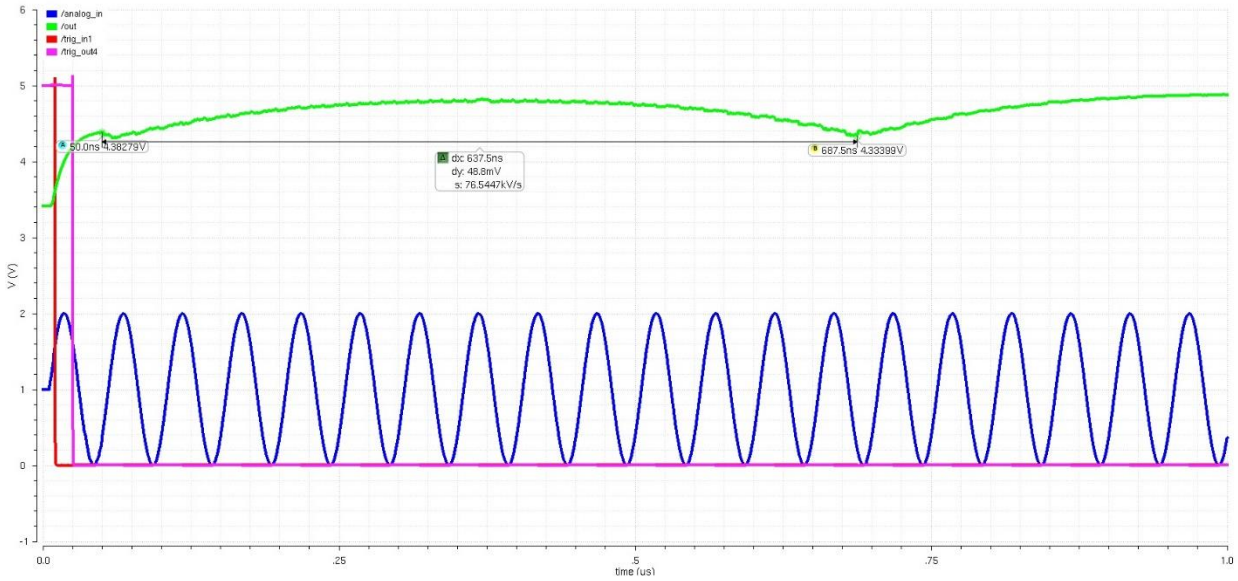


Figure 52 - Reconstructed sample of *analog_in* at 20 MHz

Simulation results demonstrating the trigger signals and the signals enabling the interleaving banks function as designed are included in Figures 53 and 54, respectively, and will hereafter be assumed to be functioning for the remaining simulations. Note in Figure 53 the signals are separated by approximately 60 ps, as intended. Referencing Figure 54, the signals *Ve 1-4* represent the two LSBs controlling the 2:4 decoder toggling between the banks in succession such that each sequential unit cell is read out properly. *Ve 1* enables bank 0, *Ve 2* enables bank 1, *Ve 3* enables bank 2, and *Ve 4* enables bank 3.

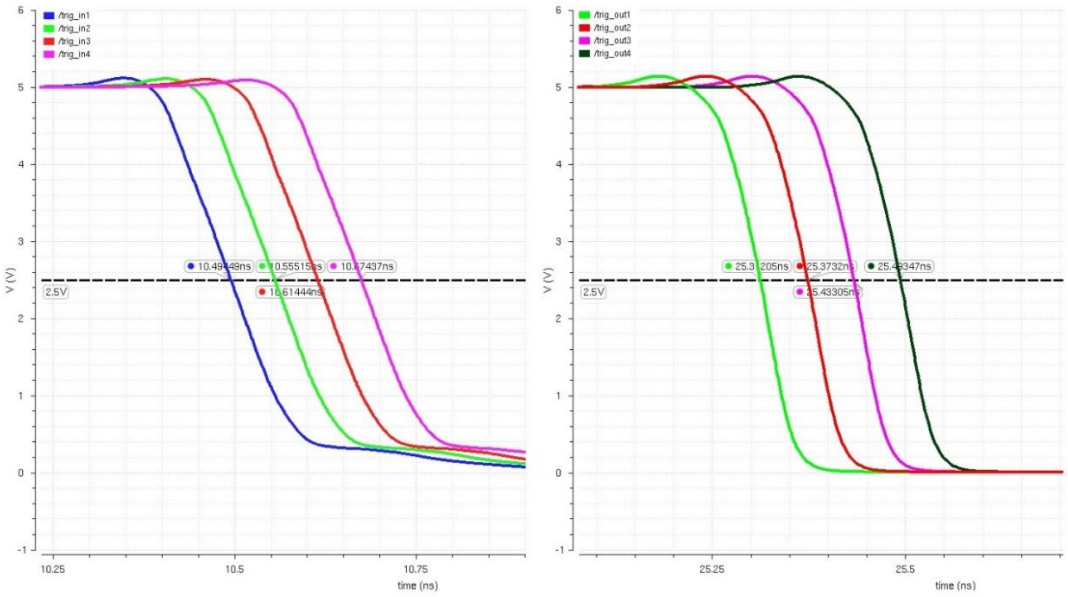


Figure 53 - Trigger input (left) and output (right) signals separated by 60 ps

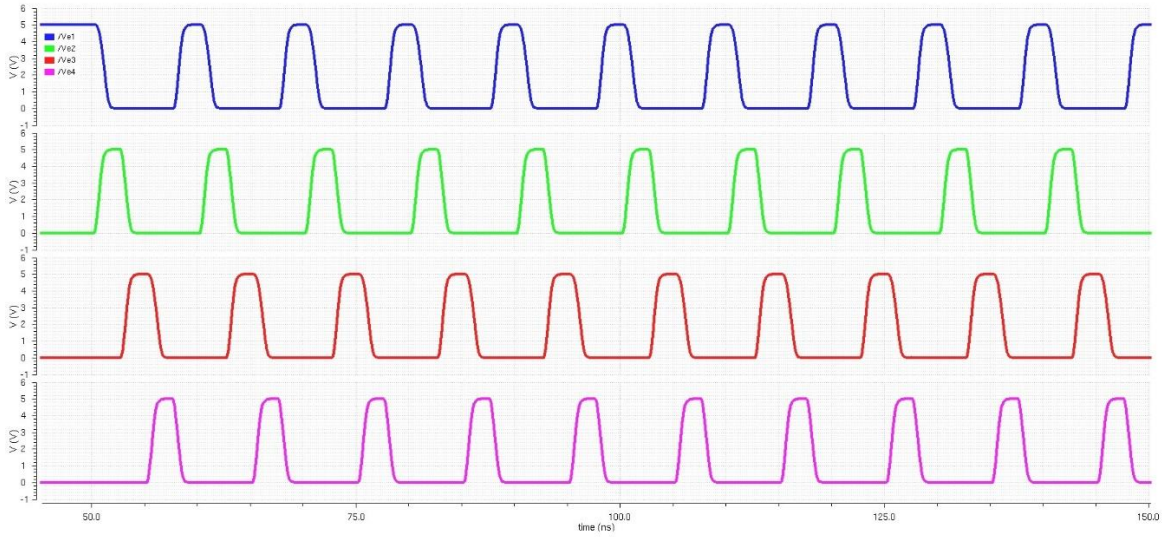


Figure 54 - Interleaving bank enable signals

The next simulation increased the frequency of *analog_in* to 320 MHz and is included to demonstrate the HSFTD works at faster frequencies and will fully reconstruct a sinusoidal input. A

320 MHz sinusoid has a period of 3.125 ns, therefore there are approximately five periods within the capture window. Figure 55 displays the portion of *analog_in* sampled during the 15 ns capture window.

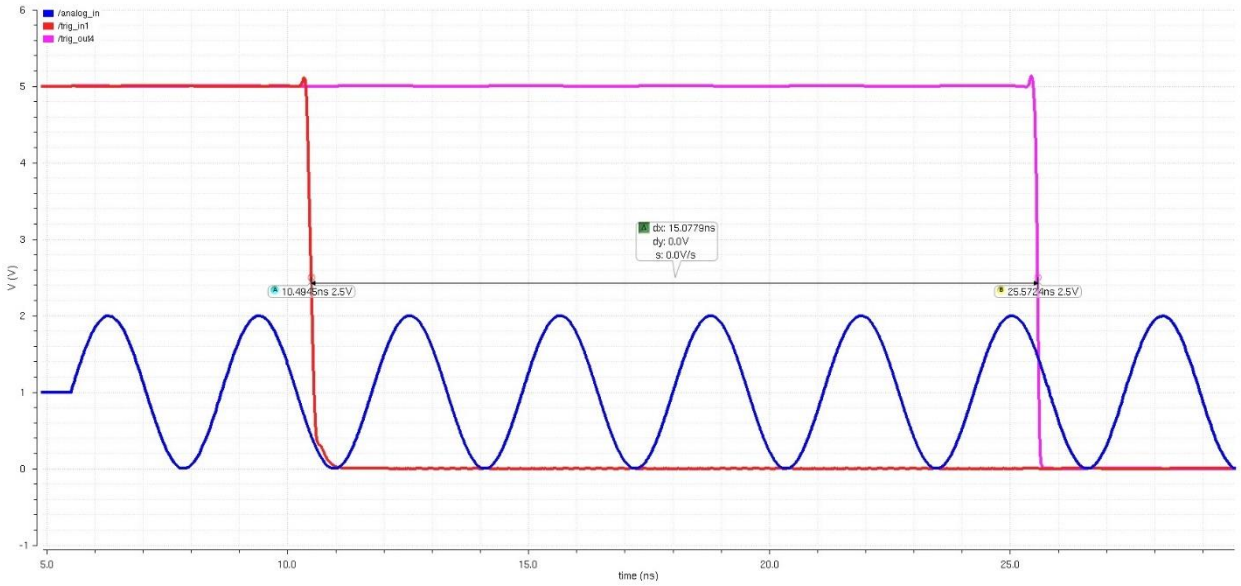


Figure 55 - *Analog_in* sample within capture window for 320 MHz simulation

Next, Figure 56 displays the reconstructed signal decoded at a rate of 2.5 ns per capture stage. The output signal definitively represents a stretched reconstruction of the sample seen in Figure 55, however the signal clearly shows the distortion mentioned earlier due to reading out at such a high rate. Reading out at this high rate also allows the signals to be scaled and included on the same waveform. If the rate were slowed, the sinusoidal input would appear as a solid color bar across the plot. A discontinuity occurs at 687.5 ns when the decoder resets to zero and begins reconstructing the sample again. Increasing the frequency of *analog_in* makes the slowed reconstruction more apparent when compared to the initial 20 MHz signal.

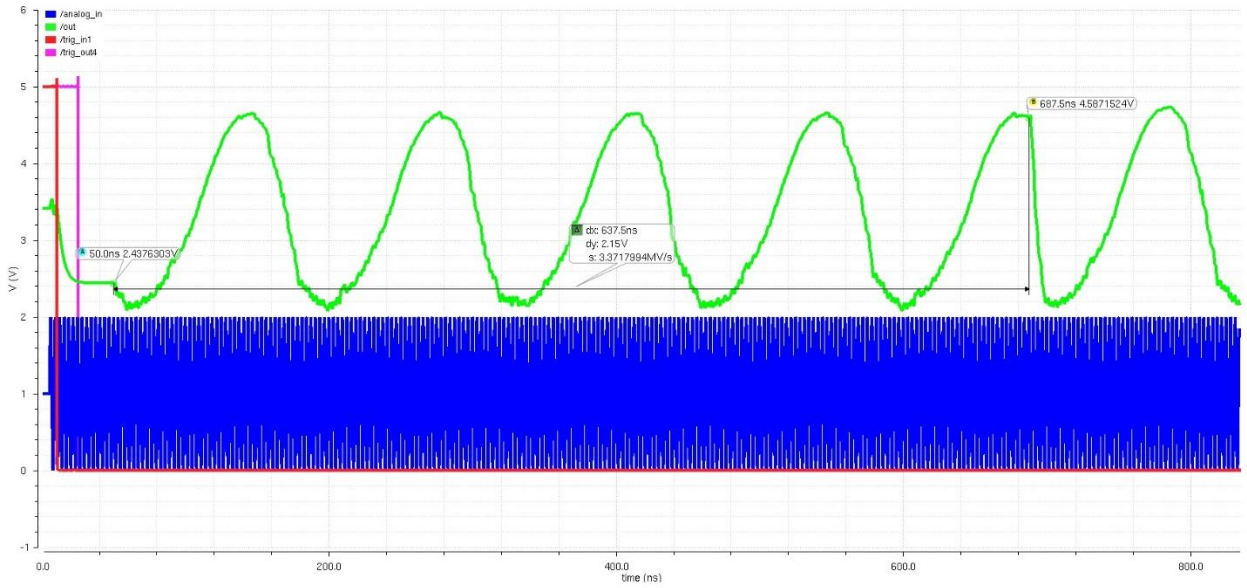


Figure 56 - Reconstructed sample of *analog_in* at 320 MHz

5.2 VARIABLE CAPTURE WINDOW

The simulations in this section were designed to demonstrate the ability of the HSFTD to provide a variable capture window. In Section 4.2, variability within the trigger generator was demonstrated for an arbitrary sampling rate of 9.6 GHz, or a 104 ps delay between trigger signals. This requires setting *Vinvc 4* to approximately 3.71 V and *Rbias* to 7.5 kΩ for a 416 ps time delay between unit cells and a total capture window of 27 ns. The results seen in Figure 57 display the 20MHz *analog_in* signal and a 27 ns capture window between *trig_in 1* and *trig_out 4*. Next, the reconstructed version of the sample of *analog_in* is added to the waveform in Figure 58. The reconstructed sample is once again a stretched representation of the original sample seen inside the capture window in Figure 57. The results demonstrate the ability of the HSFTD to vary the capture window and consequently, the sampling rate.

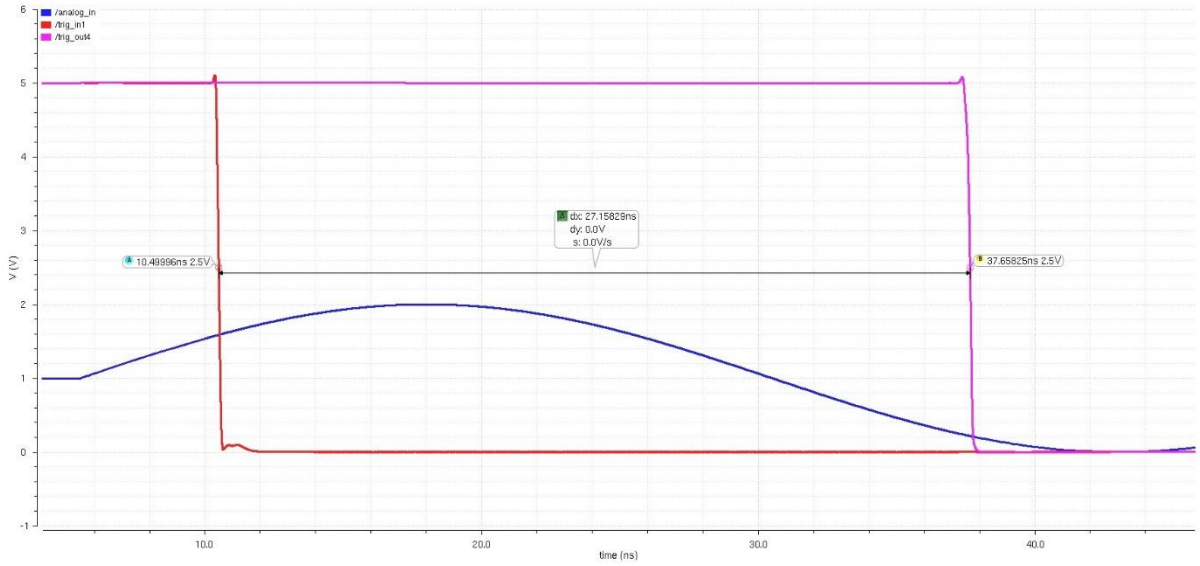


Figure 57 - 20 MHz sample of a*nalog_in* within 27 ns capture window

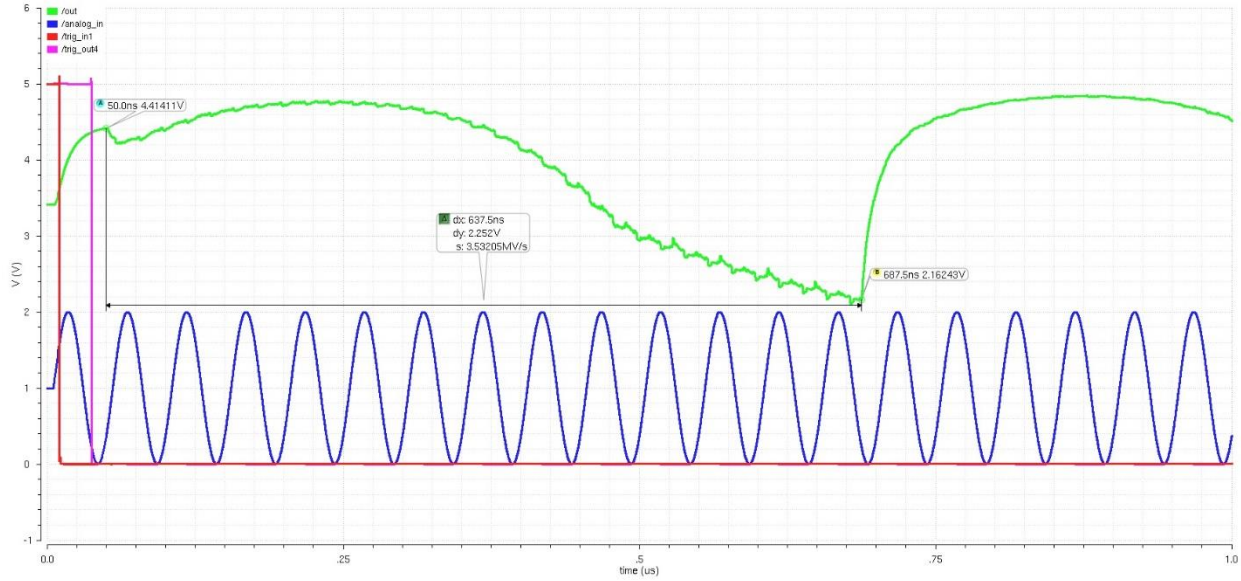


Figure 58 - Reconstructed 20 MHz sample of *analog_in* with 27 ns capture window

The same simulation was repeated for a 320 MHz *analog_in* signal with the results displayed in Figure 59. The capture window is again approximately 27ns and the captured signal

is stretched and reconstructed with distortion once again present due to the high readout rate.

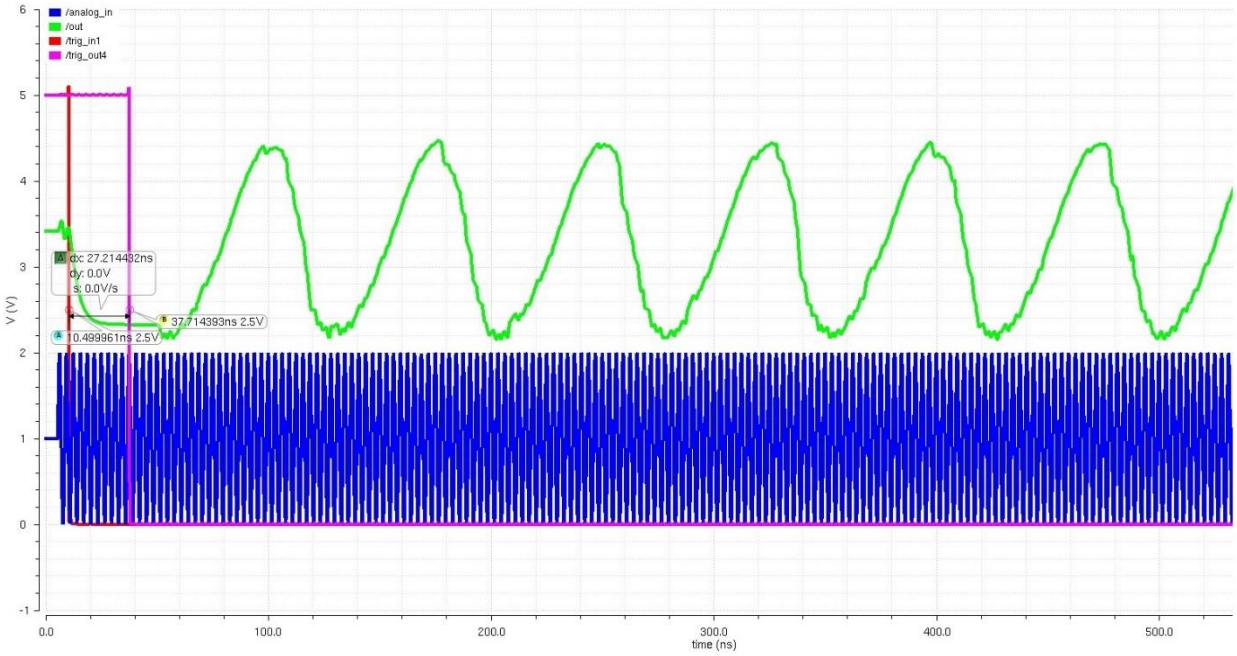


Figure 59 - Variable capture window and reconstructed sample of 320 MHz *analog_in* signal

5.3 PIECEWISE LINEAR FUNCTION

The next simulations performed used piecewise linear functions for *analog_in* to demonstrate the HSFTD functions for arbitrary transient signals. The input signal for the first simulation is essentially a triangle wave that takes 7 ns to rise from 0 V to 2 V and another 7 ns to fall back to 0 V. The sampling frequency was set to the maximum rate with *Vinvc 4* at 5 V. Figure 60 displays the sample of *analog_in* within the 15 ns capture window. Moving to Figure 61, the reconstructed sample is added for comparison to the scaled sample and demonstrates the HSFTD was able to reconstruct and stretch the transient input. As a point of clarity, the nonlinearities seen in the

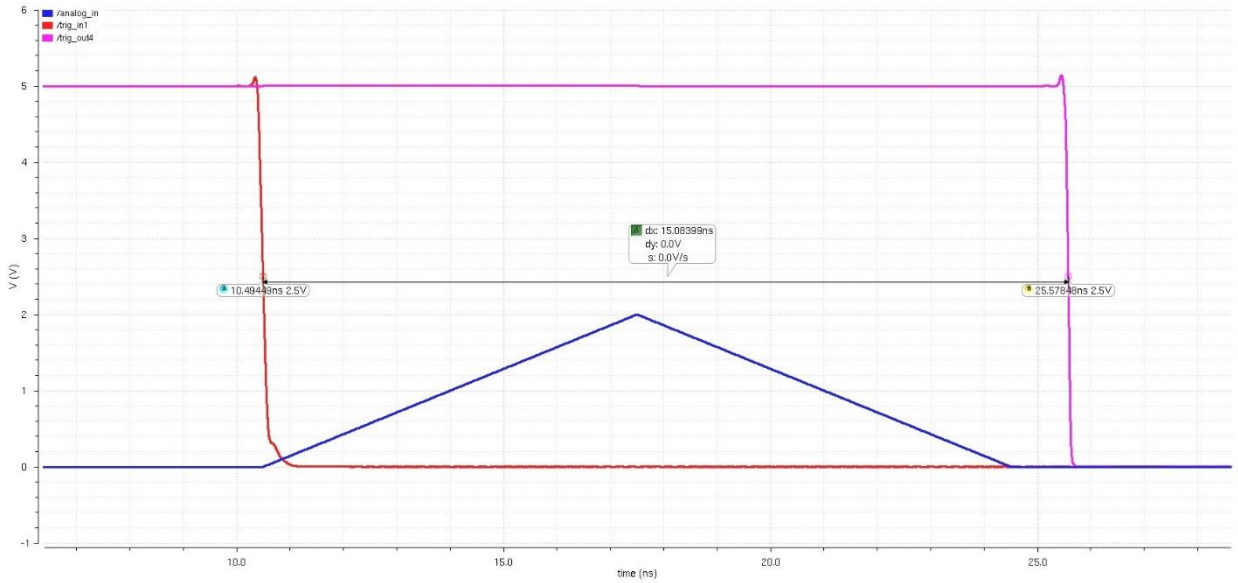


Figure 60 - Sample of *analog_in* as a piecewise linear function within 15 ns capture window

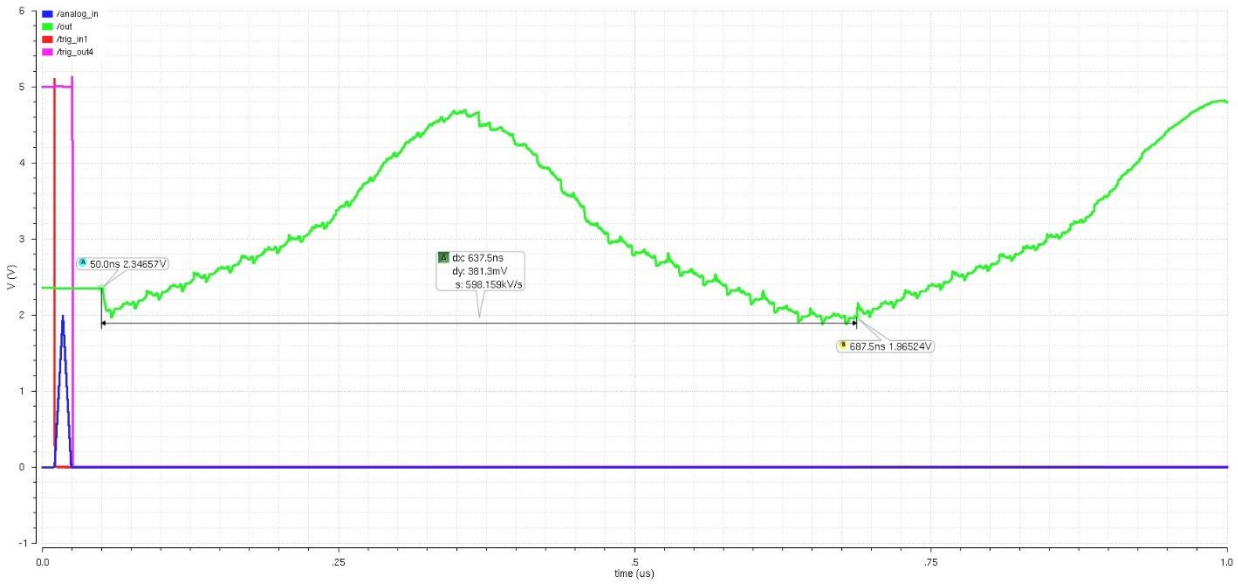


Figure 61 - Reconstructed sample of *analog_in* with 15ns capture window

reconstructed signal are related to the high rate of readout. The next simulation modified the signal slightly with a quick ramp up over 3 ns, a step for 3ns, and a slower ramp down over 8ns.

Figure 62 shows the sample of *analog_in* within the 15 ns capture window and Figure 63 shows the successfully reconstructed sample.

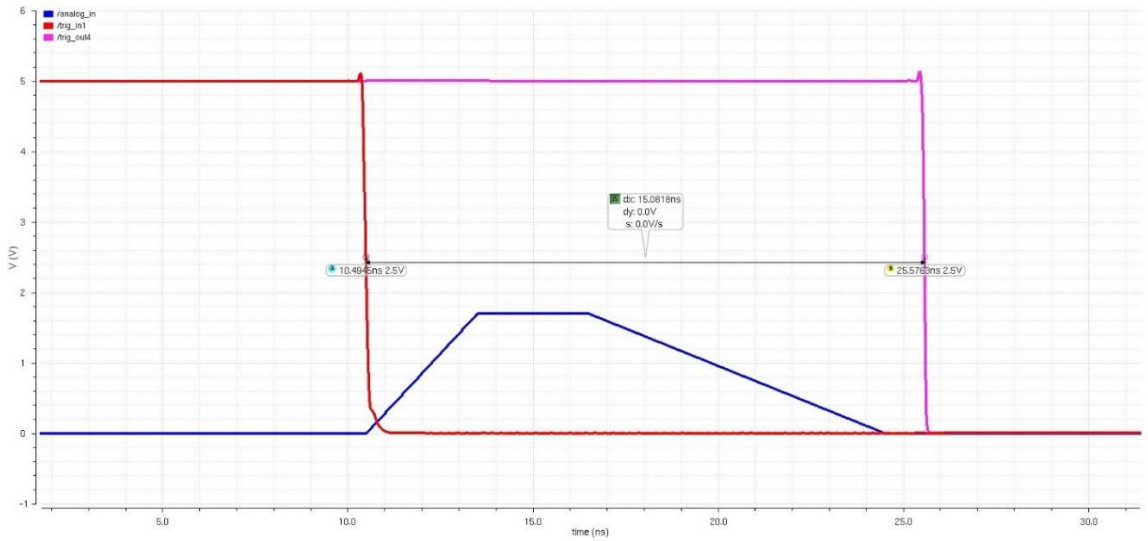


Figure 62 - Sample of modified piecewise linear function within 15ns capture window

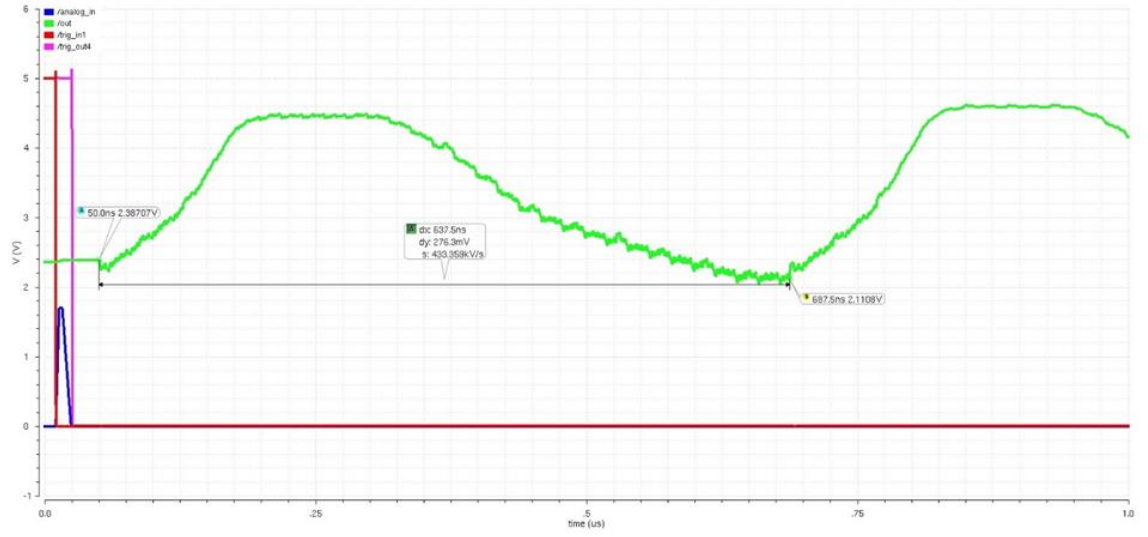


Figure 63 - Reconstructed sample of modified piecewise linear function

To demonstrate the nonlinearities in the reconstructed signal are removed when the decoder is readout at a more reasonable rate, a simulation was performed starting at 0.25 V with a ramp up to 0.75 V over 3 ns, a step for 3 ns, and a slower ramp back down to 0.25 V over 8 ns. The decoder readout was reduced to 4 ns per stage, or 250 MHz, for a total readout time of 1.02 µs. Figures 64 and 65 display the captured sample and reconstructed signal, respectively. Looking at Figure 65, the reconstructed signal no longer shows any nonlinearities.

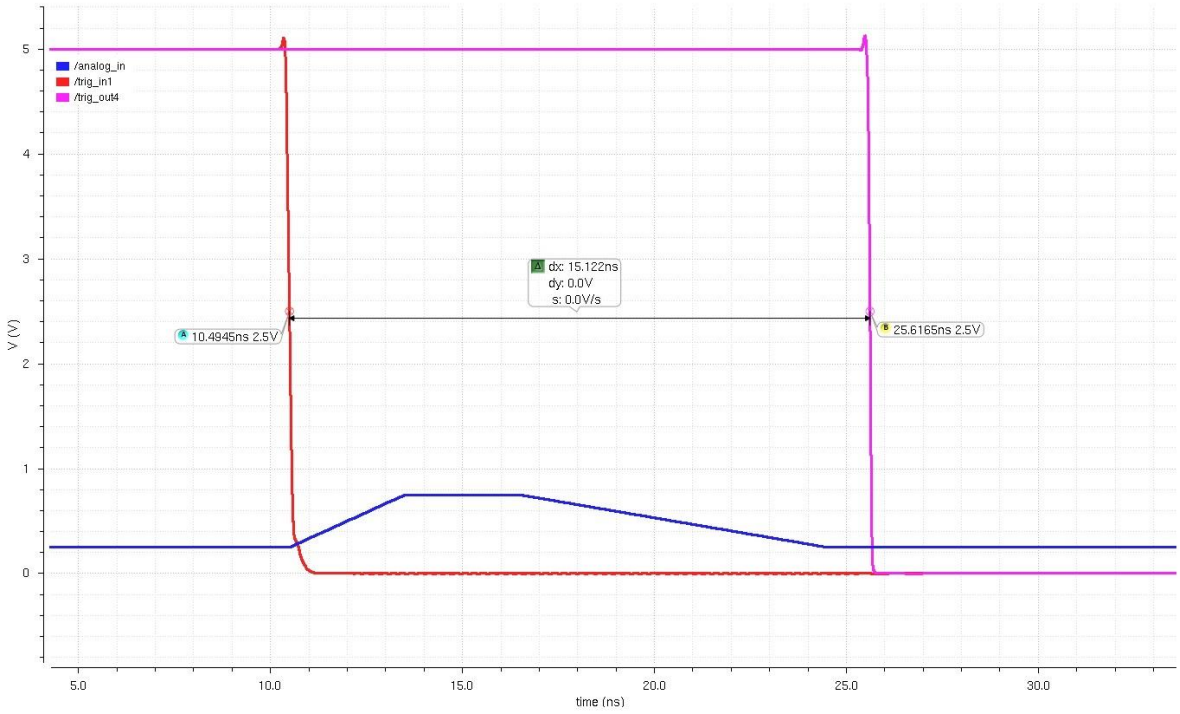


Figure 64 - Sample of piecewise linear function between 0.25 V and 0.75 V

To further demonstrate the reconstructed signal is now a linear representation of the captured sample, Figure 66 displays a scaled version of the output. The initial ramp up, the step, and the final ramp down are all linear when readout out at a reduced rate of speed.

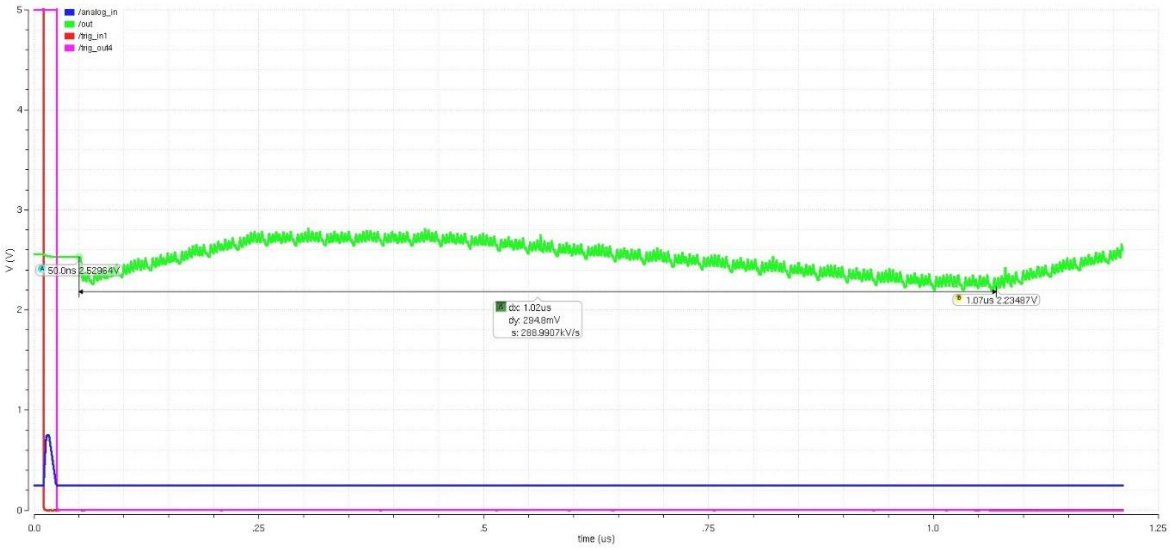


Figure 65 - Linear reconstruction of piecewise linear function at 4 ns per stage

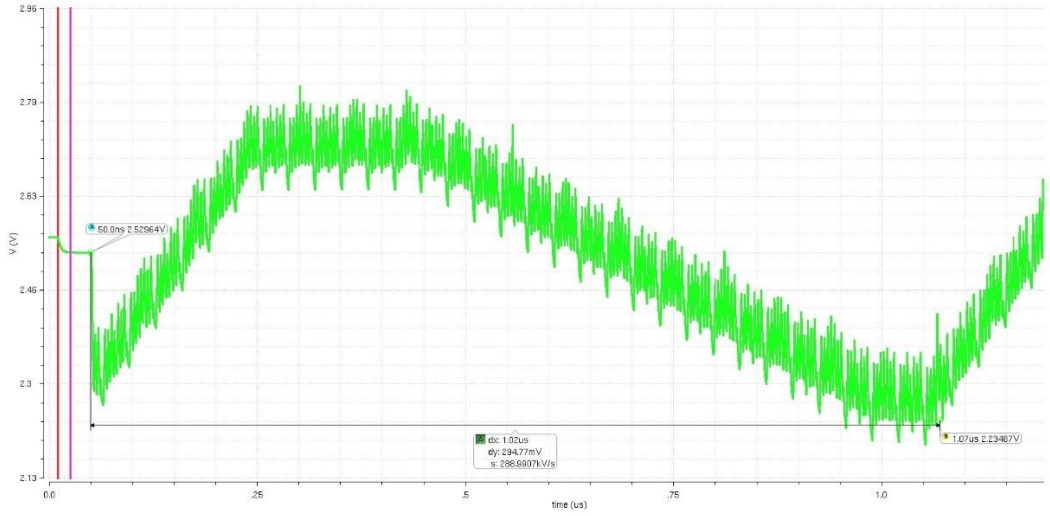


Figure 66 - Scaled reconstruction of piecewise linear function at 4 ns per stage

Lastly, the output was run through a simple, low-pass RC filter to further eliminate distortion in the reconstructed signal. The results are displayed in Figure 67 with the unfiltered output shown

on top and the filtered output displayed on the bottom. These simulations were included to confirm how decoding at a slower rate removes nonlinearities in the reconstructed signal.

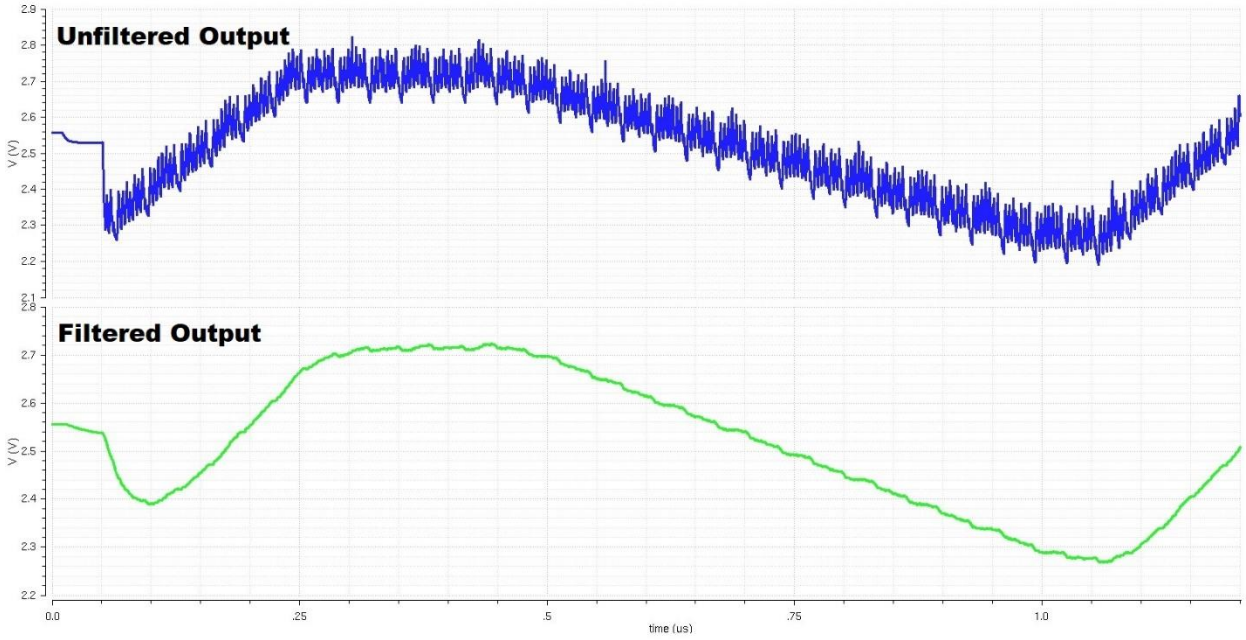


Figure 67 - Low-pass filtered output signal

5.4 OUTPUT RANGE

The last simulation performed used a signal that extended outside the range of the analog input signal to determine the minimum and maximum range for the output voltage. In Section 3.4, these were calculated to be a minimum of 2.35 V and a maximum of 4.98 V. Figure 64 displays the results of the simulation with a minimum of approximately 1.99 V and a maximum of roughly 4.83 V.

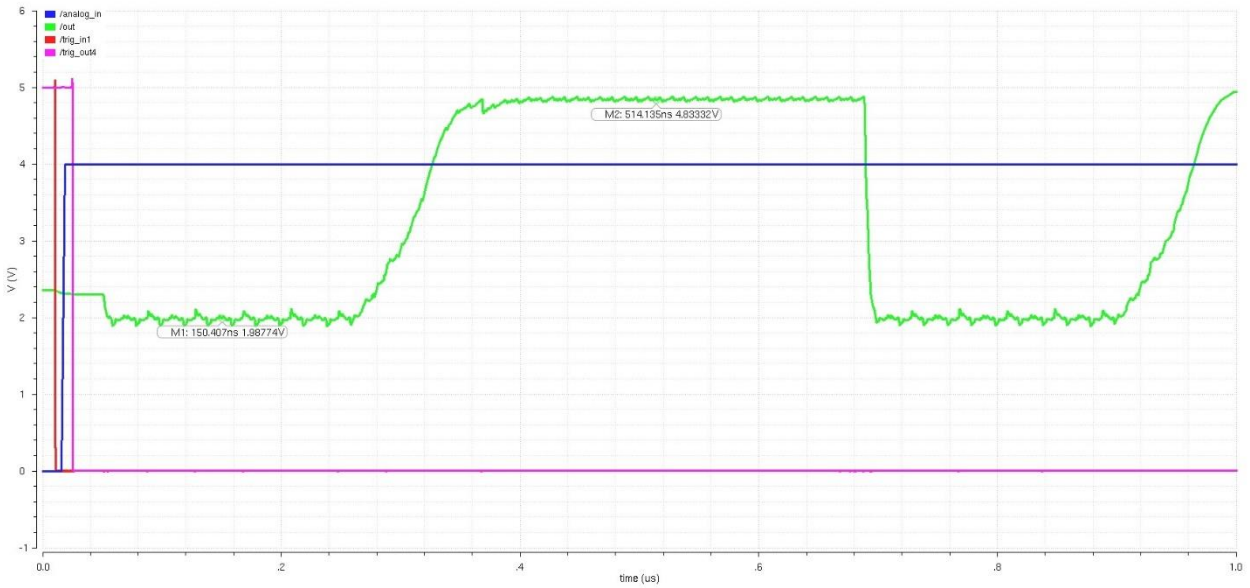


Figure 68 - Minimum and maximum output voltages

5.5 CALCULATED VERSUS SIMULATED SUMMARY

The HSFTD has been designed, simulated, and demonstrated to perform as intended in comparison to the theoretically derived calculations. A summary of the calculated versus simulated results for the fastest possible sampling frequency is included in Table 5.

Summary	t_{plh} (ps)	t_{phl} (ps)	Unit cell t_d (ps)	Minimum Capture Window (ns)	f_{sample} (GHz)	Minimum Output Voltage (V)	Maximum Output Voltage (V)
Calculated	114.9	114.9	242.7	15.5	16.5	2.35	4.98
Simulated	107.9	124.4	234.2	15.0	17.1	1.99	4.83

Table 5 - Summary of calculated versus simulated results

As discussed in Chapter 1, the stimulus for the design presented in this thesis was the FTD. A side-by-side comparison of simulation results for the FTD [3] versus the HSFTD is included in Table 6 as a final point of interest. Note the capture window is almost twice as long for the FTD for only 128 stages versus 256 stages for the HSFTD. The simulated sampling frequency of the HSFTD is approximately 3.8 times faster than the FTD's sampling frequency.

Summary	Minimum Capture Window (ns)	Unit Cell t_d (ps)	f_{sample} (GHz)	Minimum Output Voltage (V)	Maximum Output Voltage (V)
FTD	28.3	221.1	4.5	2.11	4.00
HSFTD	15.0	234.2	17.1	1.99	4.83

Table 6 - Comparison of FTD versus HSFTD simulation results

CHAPTER 6: DESIGN ANALYSIS AND FUTURE WORK

6.1 TRIGGER GENERATOR

The operation of the HSFTD is highly dependent upon the trigger generator design detailed in Chapter 4. Generating four separate triggers separated in time by a minimum of 60 ps presented a unique design challenge. Although simulations indicate the trigger generator can be precisely controlled to perform as designed, the simulations do not account for several potential sources of failure. These include the following:

- The control voltages *Vinvc 0-4* need to be precise to within the tens of millivolts or the trigger input signals will not be spaced evenly in time. This can result in the same portion of the analog input signal being sampled in time and reconstructed by multiple sequential stages simultaneously. Additionally, the four trigger input signals need to sum to the time delay through a single unit cell or the possibility exists that multiple non-sequential stages will be sampling the signal at the same time.
- Off-chip bias resistors with tolerances as low as 1% can still result in enough variation to cause the signal to be sampled in time by multiple stages simultaneously. The simulations used 4kΩ, and 7.5kΩ resistors with the bias generators. This is a small variation, but with precision required within the tens of picoseconds, even resistors with 1% tolerances could cause uneven trigger signals. If the control voltages are accurate enough, these may be tuned to account for resistor tolerances.

- Process variations can result in transistor attributes, such as length or width, differing from the estimations provided by the models used during simulations. In submicron design these variations represent larger percentages of the device and may result in actual values differing from simulated values. In the trigger generator design, process variations could affect the threshold voltages of transistors within close proximity of each other. This could cause improper biasing of a single branch or multiple branches of the trigger generator and result in uneven spacing of the trigger signals. Once again, the control voltages may be tuned to compensate for these variations assuming they are within the required precision discussed earlier.

All of the above potential sources of failure were considered during the design of the trigger generator such that the design includes multiple options for tuning the signal if testing were ever performed on a fabricated IC. This includes adding pads for the signals *trig_out 0-3,* intended to allow the time delay between the signals to be probed such that the effects of tuning the control voltages can be observed. Off-chip resistors for the bias generators were selected to provide an additional element of control versus fixed value, on-chip resistors. To ensure control voltages are accurate to within the tens of millivolts, it is suggested that 16-bit digital-to-analog converters (DACs) be used for testing to provide a least significant bit of approximately

$$1LSB = \frac{5V}{2^{16}} \approx 76\mu V \tag{6.1}$$

The DACs should be used to provide precise control voltages that would be difficult to replicate with typical laboratory power supplies.

Researchers seeking to expand upon this design may use the trigger generator as a starting point for improvement. The use of five bias generators with five separate resistors may be reduced to one such that the need for multiple control voltages is eliminated. The goal would be to design a single generator with multiple bias voltages that increase or decrease linearly with adjustments of the control voltage.

6.2 INPUT AND OUTPUT VOLTAGE RANGE

The input and output voltage ranges are limited due to the reasons presented earlier in Section 3.4 with the input signal limited to a range of approximately 0 V to 2 V and simulations indicating an output range from approximately 2 V to 4.83V. The main limitation is due to the PMOS used in the capture stage entering the triode region for input voltages above 2.2V. Additionally, the PMOS also acts as a level shifter for the reconstructed signal resulting in a 2.35V offset. A simple method for increasing the range of the output voltage would be to increase the value of the off-chip pull-up resistor, however this comes with the tradeoff of a larger RC constant during readout with potential loss of data due to signal droop.

Future work on the HSFTD design could include a redesign of the original FTD capture stage to extend the range of the input and output signals. One idea is to replace the two NMOS devices in the capture stage with transmission gates (TGs) and replace the PMOS with a unity buffer. This concept comes at the cost of increased design size and would require the generation of precisely timed, inverted trigger signals to propagate the capture and readout sequences. Figure 65 displays a possible schematic for the capture stage.

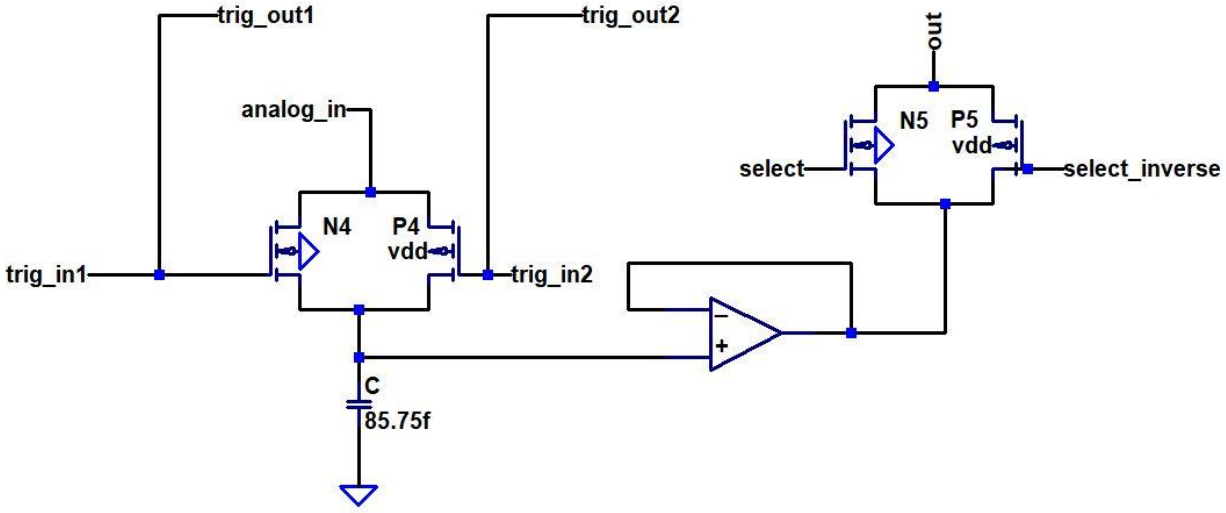


Figure 69 - Theoretical redesign of FTD capture stage

6.3 COUNTER

An off-chip counter is suggested for use in conjunction with the on-chip decoders to readout the reconstructed sample of the analog input signal. An alternative solution that would reduce the number of off-chip interfaces would be to design and implement an on-chip counter. The advantages would be decreased parasitics, lower noise, lower power consumption, lower costs, and smaller PCB design size.

CHAPTER 7: CONCLUSION

The goal of this thesis was to present a design that improved upon the inherent limitations of the FTD [3]. The FTD samples high-speed analog signals in time and later reconstructs these samples at a slower rate for application specific analysis while reducing noise, power consumption, and costs when compared to high-speed ADCs. The proposed HSFTD aimed to expand upon the FTD by adding the ability to vary the length of the capture window and via the use of interleaving banks of unit cells.

The HSFTD design and layout were performed using Cadence EDA tools with simulations demonstrating the following results:

- The ability to vary the capture window and consequently, the sampling frequency. The HSFTD design allows for flexibility in controlling the sampling frequency via the use of current-starved inverters and bias generators. The current-starved inverters act to limit the propagation delay through the unit cells via adjustable bias voltages. The bias voltages are controlled via both an external control voltage requiring resolution in the tens of millivolts and an off-chip bias resistor. This design provides two degrees of control when tuning the HSFTD.
- Increased sampling frequency range via the use of interleaving banks of unit cells. The maximum simulated sampling frequency of the FTD is 4.5 GHz versus 17.1 GHz for the HSFTD. The trigger generator design is the critical component to successful operation of the interleaving banks during the sampling process.

- The HSFTD was successful in sampling and reconstructing different high-speed input signals, including sinusoidal signals and piecewise linear functions modeling transient signals. The output range of the device is limited from approximately 2 V to 4.8 V. The on-chip decoders functioned as designed and allowed the captured sample to be reconstructed at a slower rate.

The proposed HSFTD design met the initial goal of expanding upon the applicability of the FTD by improving upon its limitations. The HSFTD design also presents an opportunity for future researchers to investigate alternate topologies that may eliminate limitations in the trigger generator design and expand the useful range of operation to the power supply rails.

APPENDIX: ADDITIONAL SCHEMATIC AND LAYOUTS

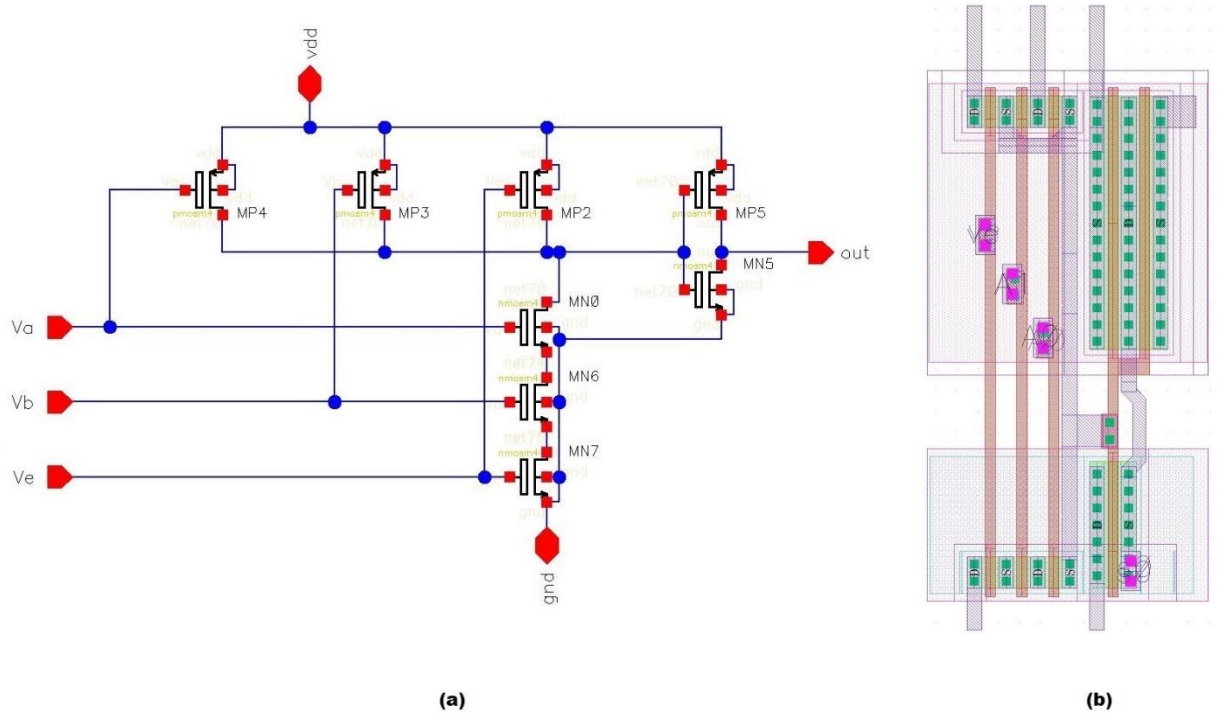


Figure 70 - 3-input AND gate: (a) schematic view; (b) layout view

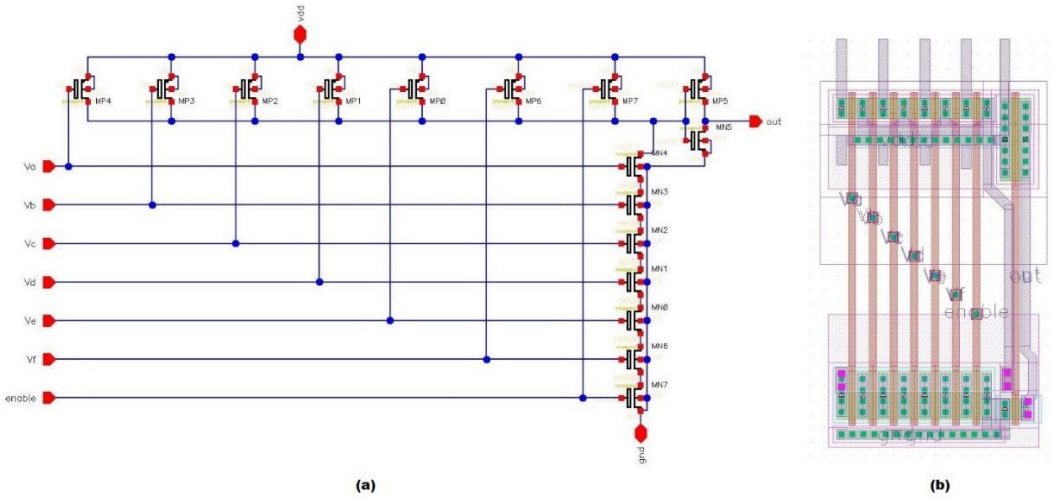


Figure 71 - 6-input AND gate: (a) schematic view; (b) layout view

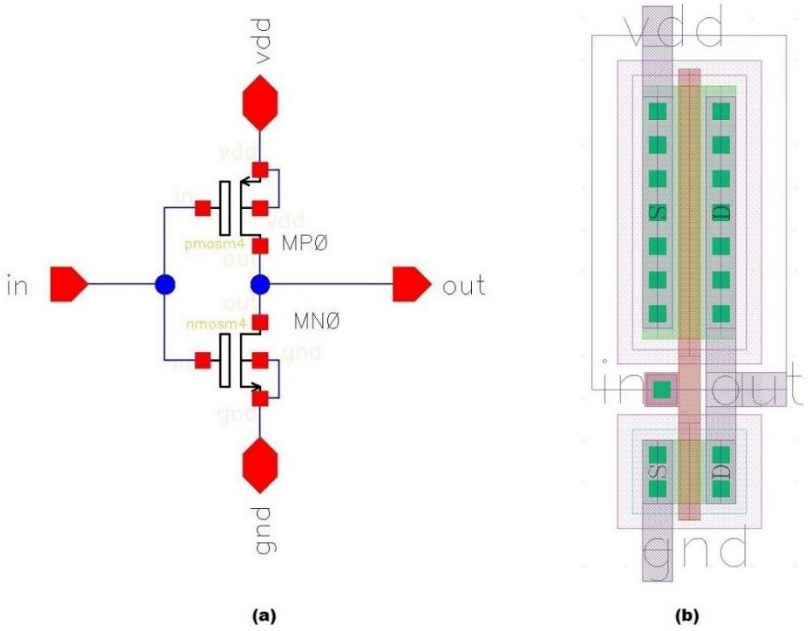


Figure 72 - Basic inverter: (a) schematic view (b) layout view

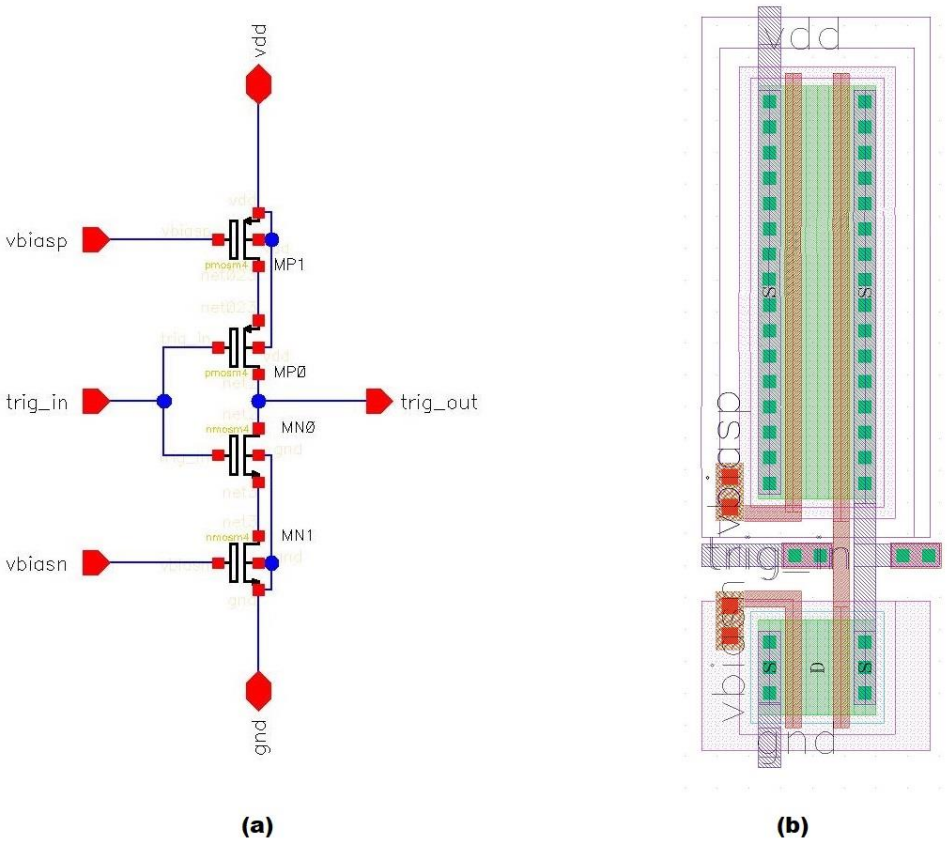


Figure 73 - Current-starved inverter: (a) schematic view (b) layout view

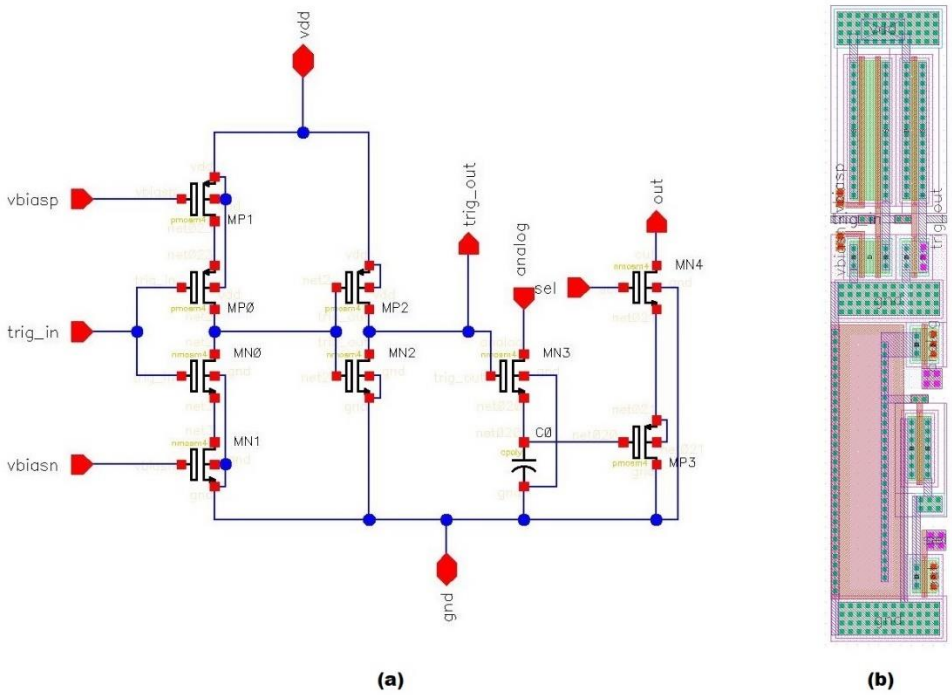


Figure 74 - Unit cell: (a) schematic view (b) layout view

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