HIGH SPEED DIGITAL CMOS INPUT BUFFER DESIGN

By

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A project

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The project submitted by Krishna Duvvada entitled “HIGH SPEED DIGITAL CMOS INPUT BUFFER DESIGN” is hereby approved:

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It is my privilege to do my Masters in Electrical Engineering Department at Boise State University. I would like to take this opportunity to thank my Professors for providing me with quality and technical education, guidance and motivation. The special courses and the research have induced valuable concepts and good understanding of the subject.

I would like to thank MURI (Multidisciplinary University Research Initiative Program) for funding this project. Very special thanks to my advisor, Dr. Jacob Baker who has provided me with high quality education, guidance and motivation through out my graduation.

I dedicate this work to my parents, without whom I wouldn't be here. I would also like to thank Mr. Vishal Saxena for his support during this project and my graduate studies.

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LIST OF SYMBOLS

V_{DD} ..... Supply Voltage.

V_{DS} ..... Drain to Source Voltage.

V_{SD} ..... Source to Drain Voltage.

V_{GS} ..... Gate to Source Voltage.

I_D ..... Drain Current.

A ..... amperes.

V ..... volts.

m ..... milli.

p ..... pico.

u ..... micro.

n ..... nano.

f ..... femto.

C_T ..... Total Capacitance.

P_D ..... Power Dissipation.

K ..... kilo.

C_{out} ..... Output or load capacitance.

R_{load} ..... Load resistance.

V_{output} ..... Load or output Voltage.

V_{in} ..... Input voltage.

LIST OF ABBREVATIONS

BSU .....Boise State University.

MURI .....Multidisciplinary University Research Initiative Program.

DC .....Direct Current.

MOS .....Metal Oxide Semiconductor.

PMOS .....P-channel Metal Oxide Semiconductor.

NMOS .....N-channel Metal Oxide Semiconductor.

SPICE .....Simulation Program with Integrated Circuit Emphasis.

R .....Resistance

C .....Capacitance.

t .....time.

AC .....Alternate current.

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ABSTRACT

Overview of the Project

High speed digital Input buffer circuits are used in a wide variety of digital applications. One of the common applications of these input buffers is in memory devices. Memory circuits needs clean and full level digital data in the memory array. The digital data traveling through various digital circuitry gets distorted by adding delays in the signals like low voltage signal levels, slow rise and fall times, etc. The buffer circuits take these input signals with imperfections and convert them in to full digital logic levels by 'slicing' the data signals at correct levels which depends upon the switching point voltage. In this project, all the input buffer topologies employ self biased differential amplifiers because for buffers employing inverters in series, the switching point of the inverter varies due to the attenuation of the amplitude of the input signal. This project presents design, simulation, fabrication and characterization of novel, differential high-speed input buffers which mitigate all the above mentioned problems. The design of these input buffers has been processed in AMI's CMOS processes with a die size of 1.5 x 1.5 mm^2.

Project Goal

- To design, simulate, fabricate and characterize the novel, digital, differential high-speed input buffer circuits in AMI's CN5 process.

Project Organization

The project is divided in to five chapters

- First chapter gives an overview of the project and an introduction to the Input buffer circuits. Project requirements and objectives are also stated.
- The second chapter discusses various buffer topologies, their design, simulation, layout and fabrication.
- Chapter three discusses the MOSFET digital model. The switching resistance and capacitance of the MOS devices are calculated.
- Chapter four discusses the various test setups and the corresponding results. It mainly compares between the simulated and characterization results for the three topologies (NMOS, PMOS and Parallel input buffers).
- Chapter five describes the layout and fabrication of the full chip and also the project conclusion.

Achievements

- Design, simulation, layout and characterization of High speed digital Input buffer circuits in AMI's CN5 process.
- The chip was fabricated with ground-signal-ground pads for characterization and with a die size of 1.5 x 1.5 mm^2 .
- The test results demonstrated that the designed input buffers operate well for high-speed input signals.
- The delays were virtually independent of power supply voltage, input common mode reference and voltage swing.

CHAPTER 1: INTRODUCTION

Input Buffer Circuits

High speed input signals travel through the various digital circuits and gets distorted when it reaches the chip i.e. the digital data traveling through various digital circuitry gets distorted by adding delays in the signals like low voltage signal levels, slow rise and fall times, etc. Input buffers circuits are present at a chip's input and convert input signals with the above mentioned imperfections in to clean, full logic level digital signals for use inside the chip by 'slicing' the data signals at correct levels which depends upon the switching point voltage. The 'switching point' voltage is defined as the voltage at which the input and the output transitions from logic high to logic low or vice versa. If the switching point is too high, the output data has good low noise margin and if the switching point is too low, the output data has high noise margin. If the input signal is triangle wave with slow rise and fall times, the bits at the output of the buffer will have variations in the pulse width transitioning either too fast or too slow [1].

Input buffer circuits are used in a wide variety of digital applications. One of the common applications of the input buffers is in the memory devices. Generally input buffers employing differential amplifiers couple the data signals between the input terminals and the main memory array. If the buffer doesn't slice the data at the correct time instants, timing errors can occur i.e., the bits of data at the output of the buffer gets distorted. If the input signal is sliced too high or low, the output signal's width is

incorrect. This can be depicted in the figure 1.1 shown below. Typically these input buffers are used after the ESD protection circuit.

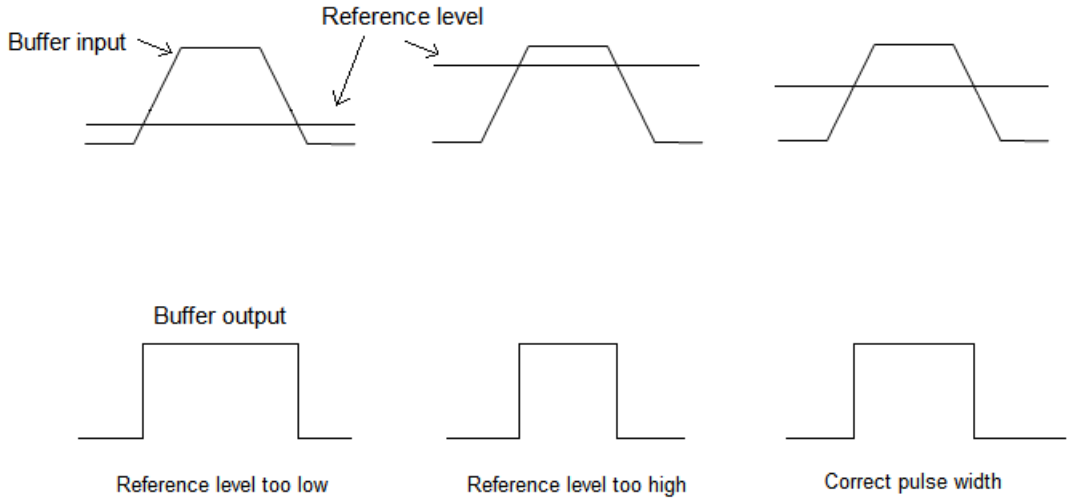


Figure 1.1 Variation in the pulse width of the digital data due to incorrect slicing.[1]

Differential amplifier Input buffers: -

There are many types of input buffers used in the digital circuits. For buffers employing inverters in series, the switching point of the inverter varies due to the attenuation of the amplitude of the input signal. To overcome this problem, the mean of the input signal is given to the reference input of the differential amplifier. In order to precisely 'slice' the input data, the data is transmitted differentially as an input and its complement. A differential amplifier input buffer amplifies the difference between the two inputs. All the buffer topologies used in this design employ self biased differential amplifiers as no external reference is used to set the bias current in the differential amplifier [1].

The design of these input buffers has been processed in 0.5um CMOS processes with a die size of 1.5 x 1.5 mm^2 and a supply voltage of 5V with a scale factor of 0.3um.

CHAPTER 2: Buffer Topologies- Design, Simulation, Layout and Fabrication

This project describes input buffer designs using NMOS, PMOS and parallel combination of both the topologies. The buffer topologies used in this design, have a differential amplifier which amplifies the difference between the reference voltage, transmitted on a different signal path, along with data and input pulse on other signal path. It is a self-biased circuit because no external references are used to set the current in the circuit.

NMOS Input Buffer Design: -

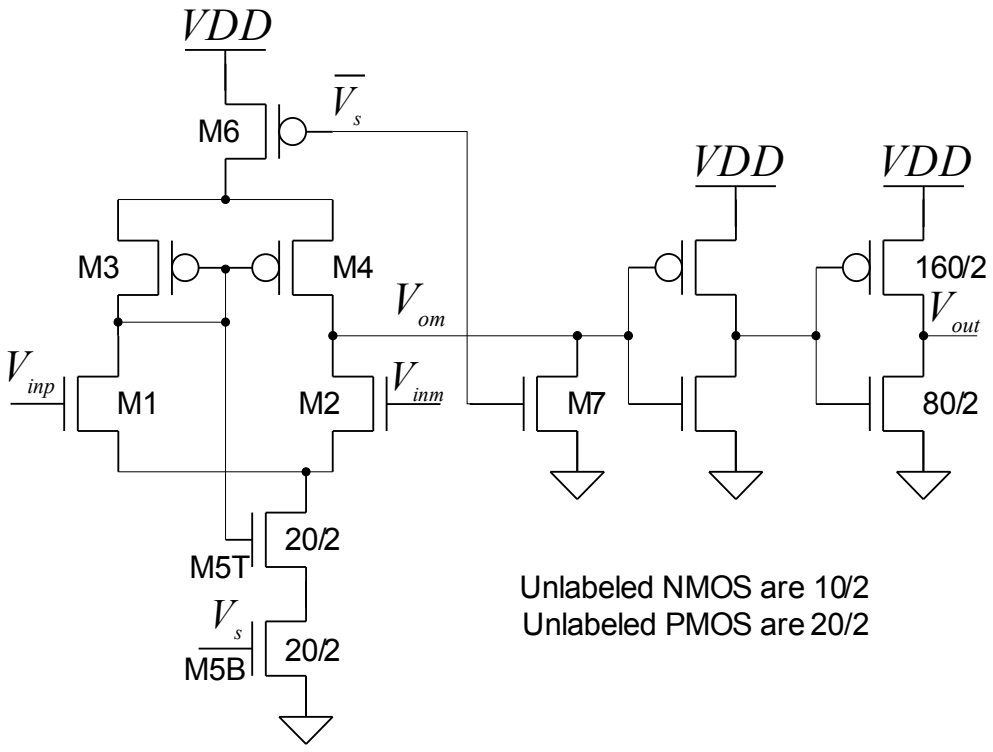


Figure 2.1 Schematic of the NMOS input buffer [1]

Figure 2.1 shows an NMOS version of the input buffer. When the input falls below V_{THN}, then the circuit will not work very quickly as the NMOS devices are moved into subthreshold region. This will result in an increase in the delay. When the input is just above the reference voltage, the output transition will be logic high. If the input is below the reference voltage, the output will be logic zero. It also has an enable circuit having a PMOS and NMOS as seen in the schematic. When these transistors are OFF, the output of the circuit will be in high impedance state and the input to the inverter driving the signal will not have a valid logic. Vref is the average of the pulses and the circuit for averaging the signals is peak detector and valley detector.

In the above figure 2.1, when Vinp is larger than Vinm, the current in M2 is greater than the current in M1. Due to the current mirror action, the currents in M3 and M4 are same i.e. M1, M3 and M4 have same currents. In order to have the same currents in M4 and M2 the transistor M2 pulls the output Vom to ground giving a good logic at the output of the buffer [1, 2].

When these transistors are OFF, the output of the circuit will be in high impedance state and the input to the inverter driving the signal will not have a valid logic. So there is a large amount of current flows in the circuit which might damage the chip. This can be explained with the simulations below. The output of the differential amplifier in high-z state is compared with the output of a '20/10' inverter when both the transistors are 'ON'. Figure shows the I-V curve and its corresponding crossing current of the inverter which flows in the inverter when both the transistors are conducting.

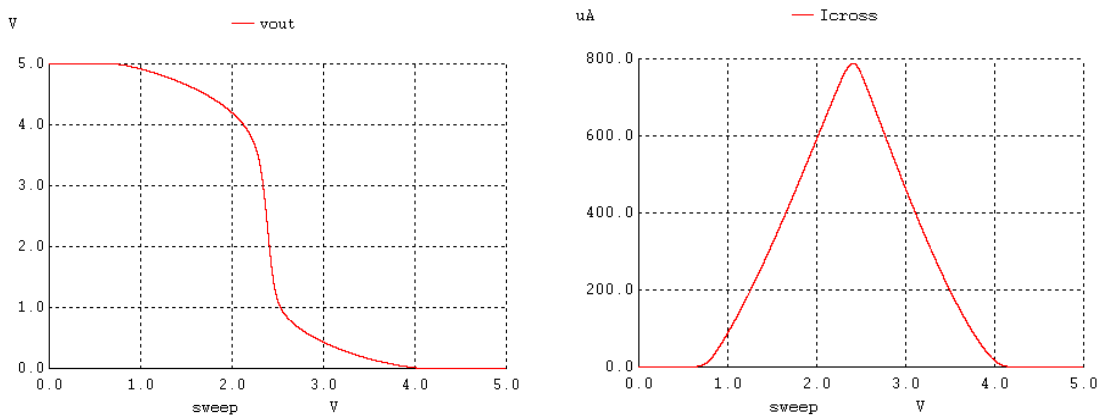


Figure 2.2 Inverter voltage transfer characteristics and crossing current.

To eliminate this problem, an NMOS switch M8 is connected at the output of the differential amplifier. The gate of the NMOS switch is connected to VSbar as shown in figure 2.1. A 160/80 size inverter is added to drive the large capacitive load. 30pF load capacitor is used in parallel with 10MEG resistor taking the probe cable and oscilloscope in to consideration. GSG (ground-signal-ground) pads are used in the layout with a pitch of 150um. Ideally, the delay of the buffer should be independent of the power supply voltage, temperature, input signal amplitudes or pulse shape [3]. In order to obtain better performance for lower input level signals, a PMOS version of input buffer can be used.

Simulation results for NMOS input buffer: -

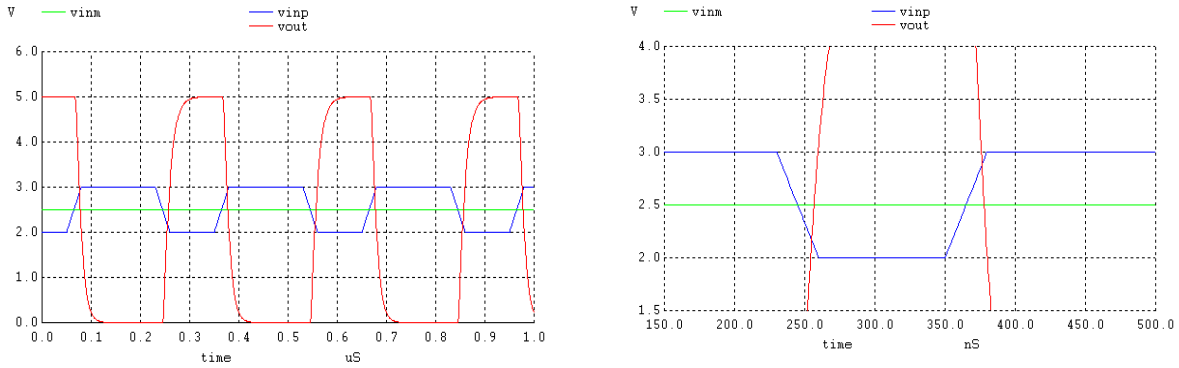


Figure 2.3 Simulations showing the output of the NMOS input buffer and its zoomed in view

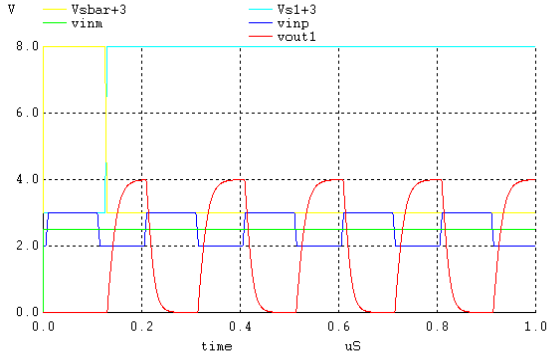


Figure 2.4 Simulations of the buffer with enable across VDD

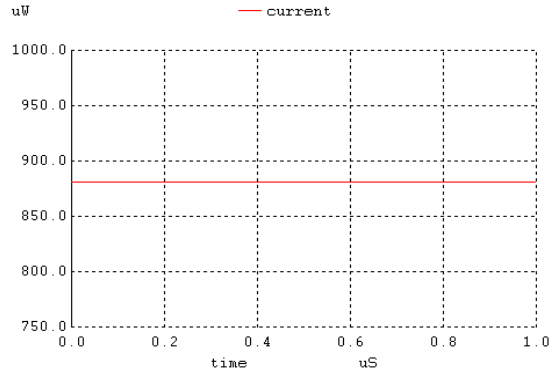


Figure 2.5 Switching current of NMOS buffer

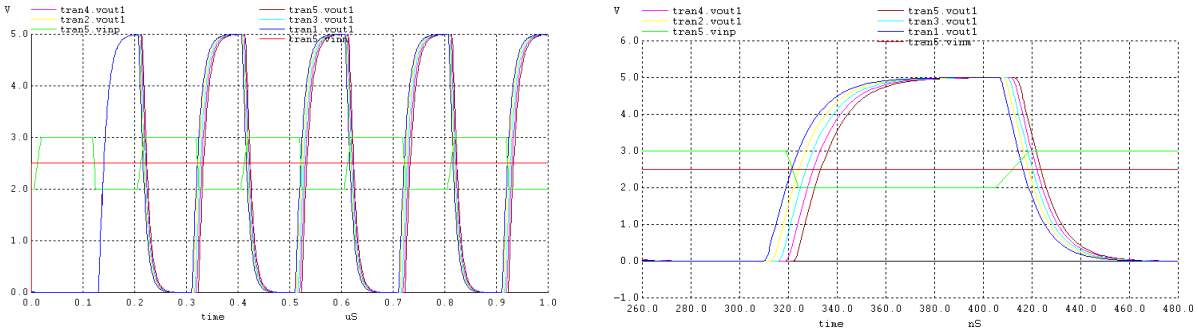


Figure 2.6 Simulations results by varying rise time of the buffer with enable and corresponding zoomed in view.

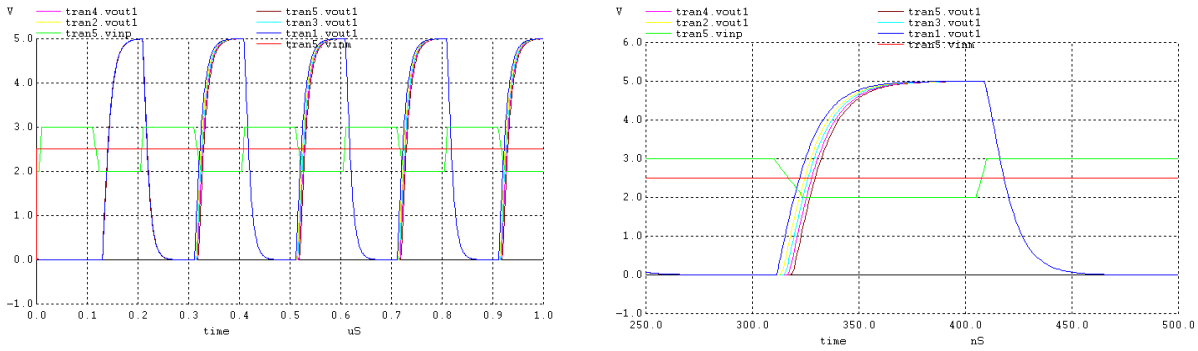


Figure 2.6 Simulations results by varying rise time of the buffer with enable and corresponding zoomed in view.

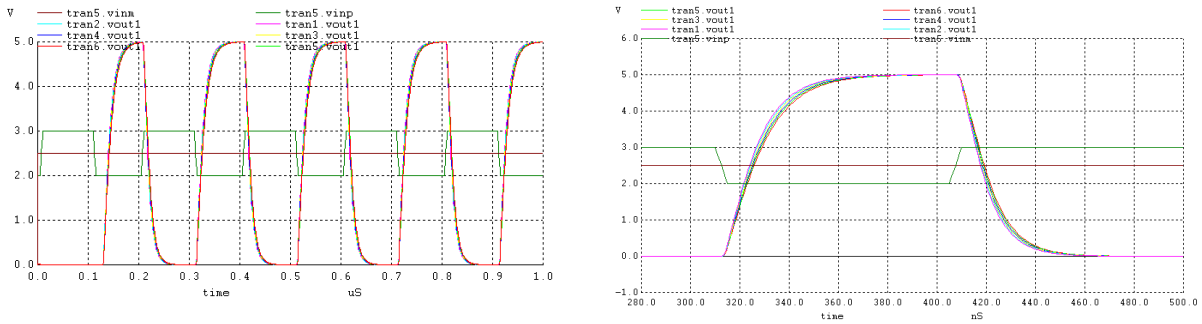


Figure 2.7 Cross temperature simulation results and corresponding zoomed in view.

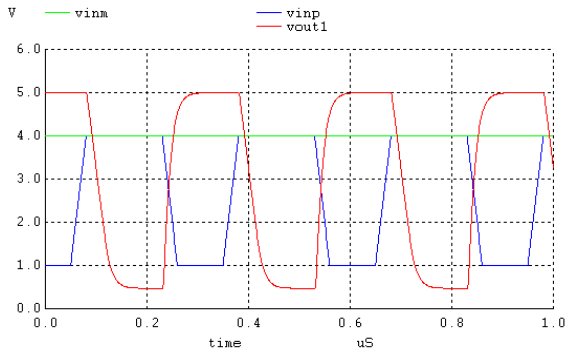


Figure 2.8 Simulations by changing vref

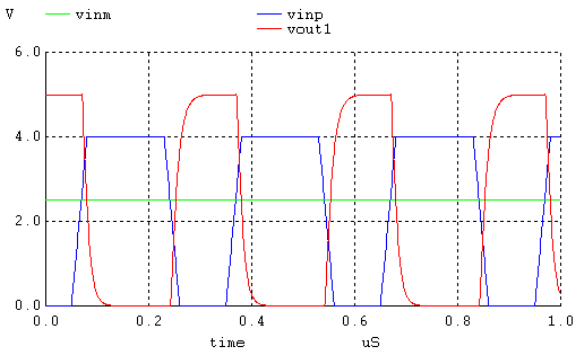


Figure 2.9 Simulations by changing vinp

NMOS Input buffer layout: -

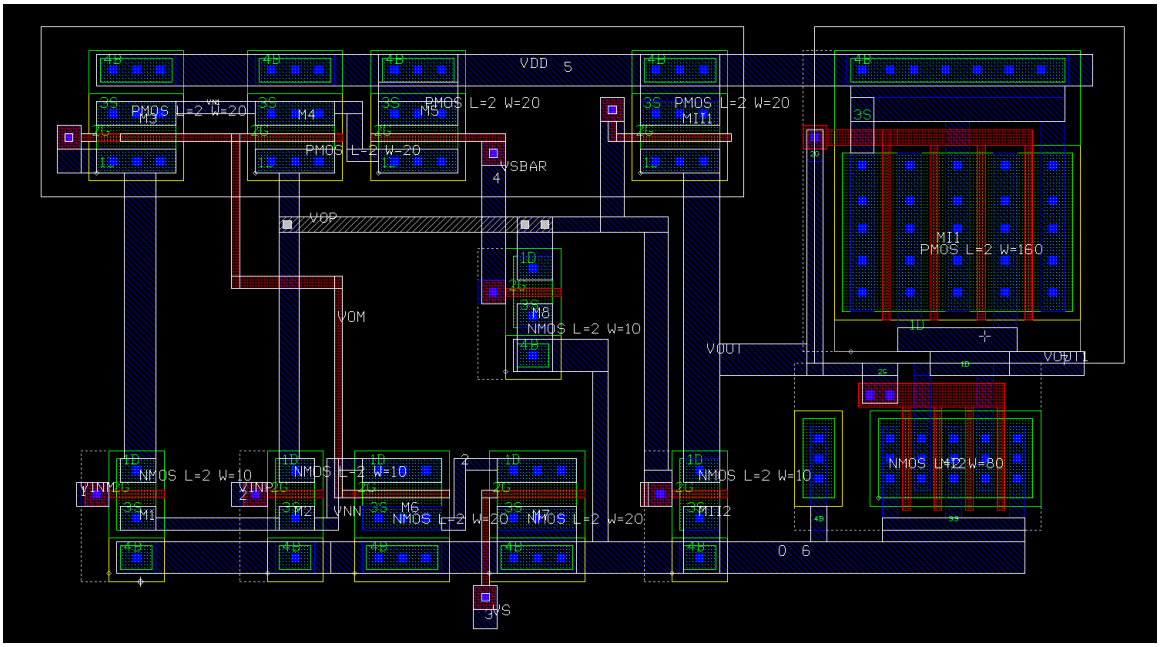


Figure 2.10 Layout of NMOS buffer

Micrograph showing the NMOS input buffer: -

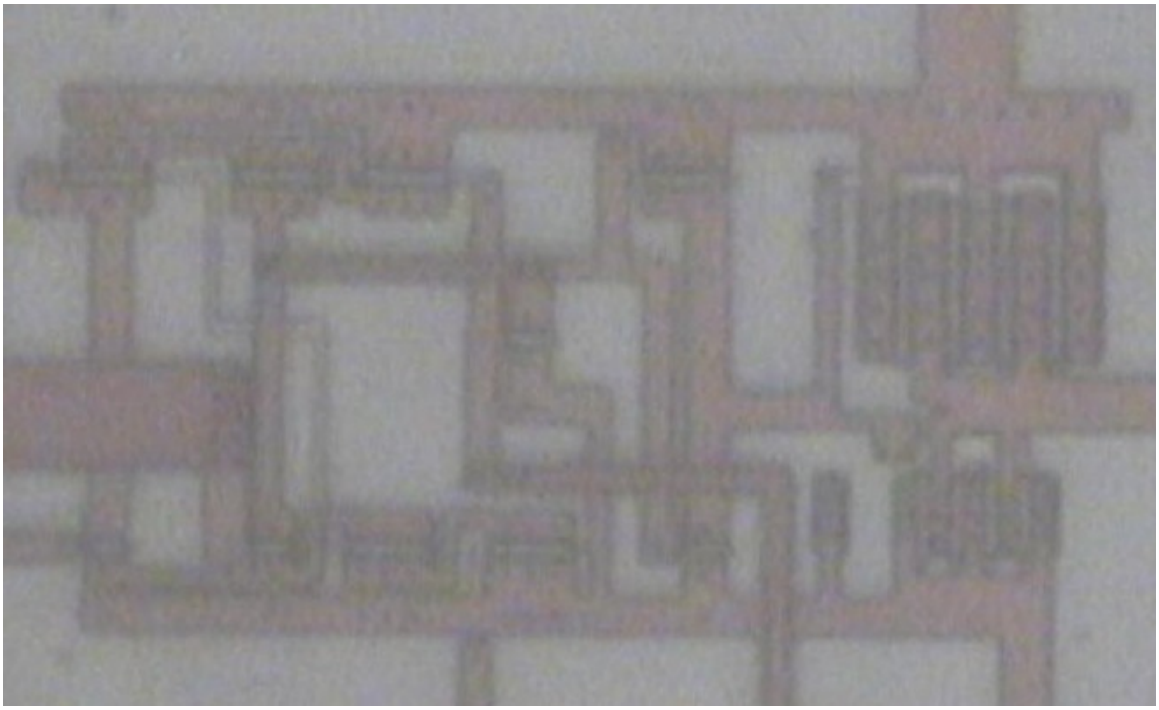


Figure 2.11 Image of NMOS input buffer

PMOS Input Buffer Design: -

A PMOS version of the Input buffer is used for achieving better performance for lower input level signals.

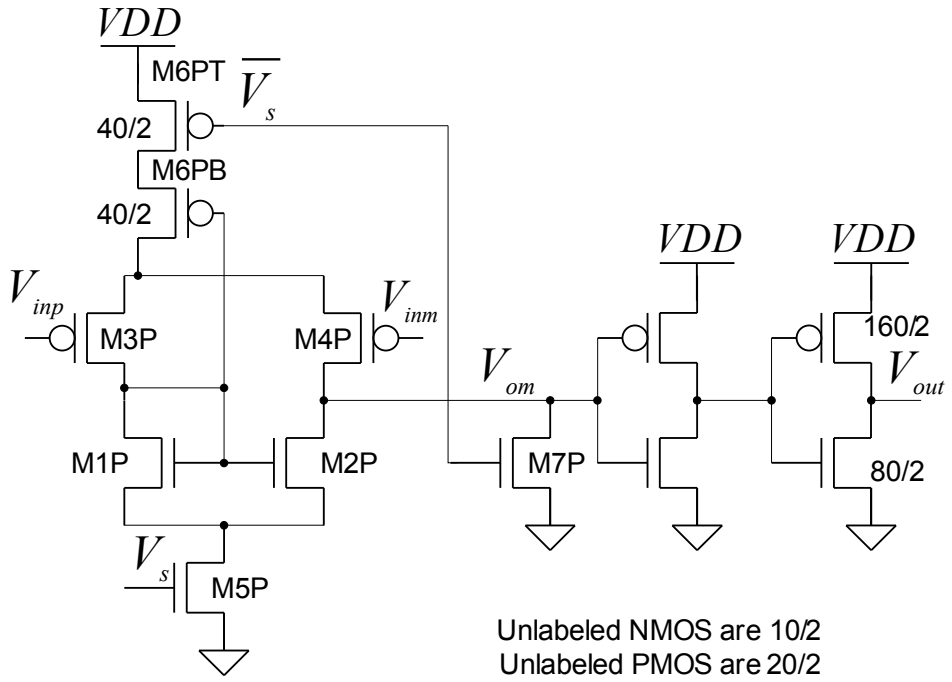


Figure 2.12 Schematic of the PMOS input buffer [1]

PMOS version of the buffer can be used for lower input signal amplitudes. But with PMOS buffers, there is a problem with offset which can be eliminated by using NMOS in parallel with PMOS version shown in the schematic. The parallel buffer works over a wide range of operating voltages in which NMOS for offsets and PMOS for operating when the signals are low or VDD.

Simulation results for PMOS input buffer: -

All the PMOS buffers (with and without enable circuits) are simulated with a load of 30pF by considering the probe load.

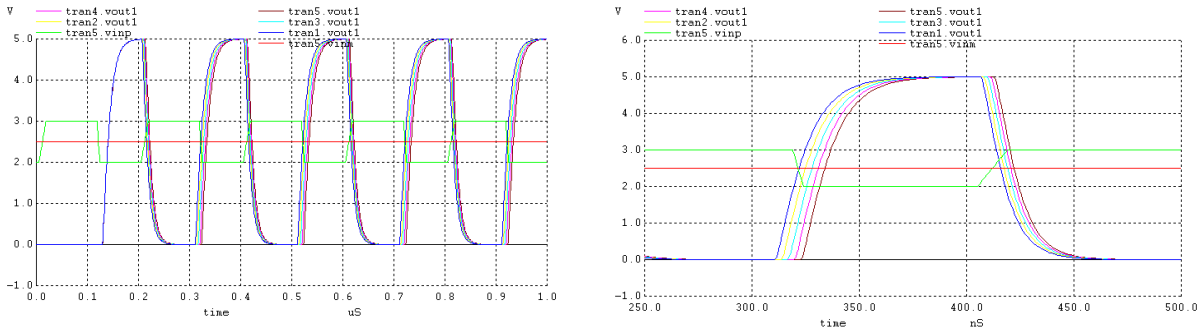


Figure 2.14 Simulations for Rise time sweep with enable (tran1-2ns, tran2=5ns, tran3=8ns,tran4=11ns and tran5=14ns)

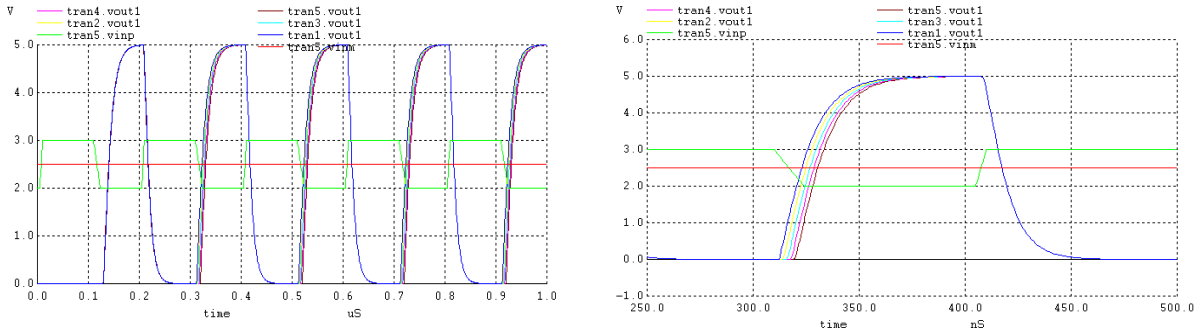


Figure 2.15 Simulations for Fall time sweep with enable (tran1-2ns, tran2=5ns, tran3=8ns,tran4=11ns and tran5=14ns)

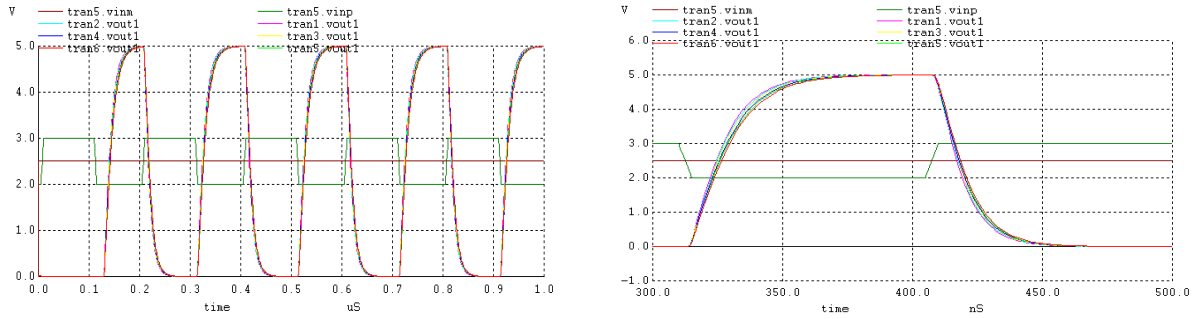


Figure 2.16 Cross temperature simulation results and corresponding zoomed in view.

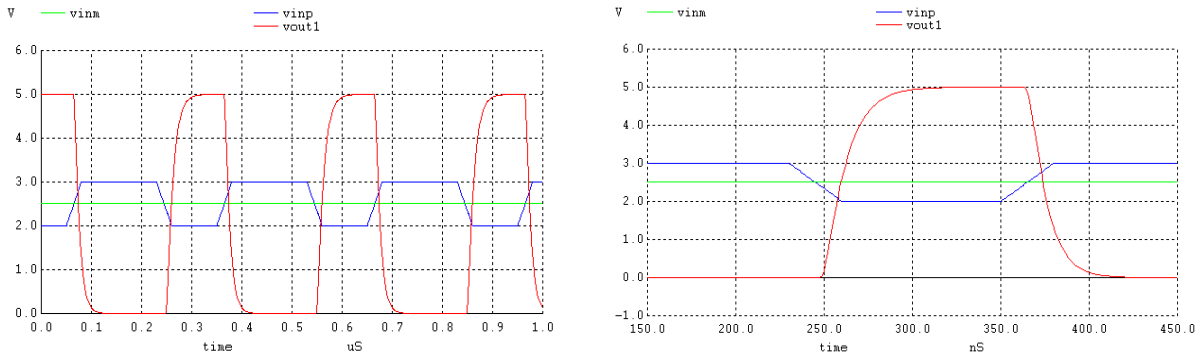


Figure 2.17 Simulations showing the output of the PMOS input buffer and its zoomed in view

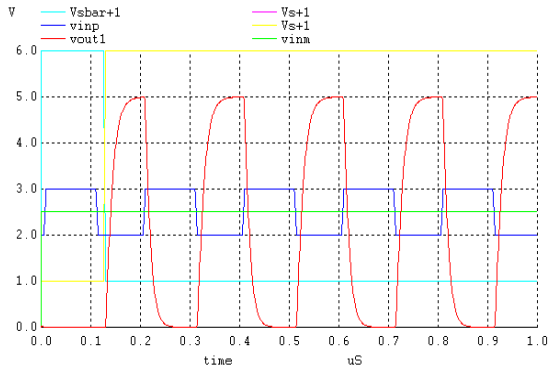


Figure 2.18 Sweeping Vdd with enable

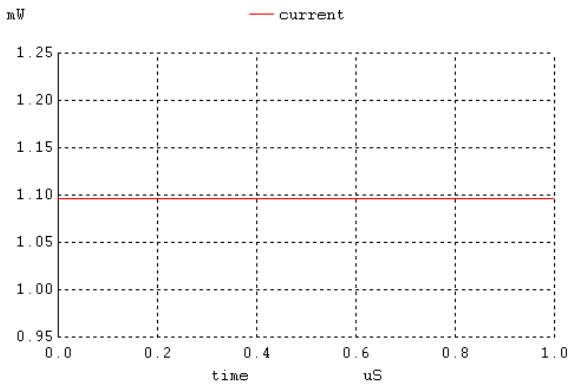


Figure 2.19 Current when switching

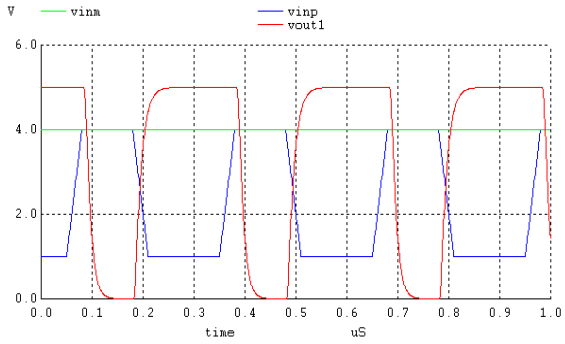


Figure 2.20 Sweeping vref with enable

Layout-PMOS input buffer: -

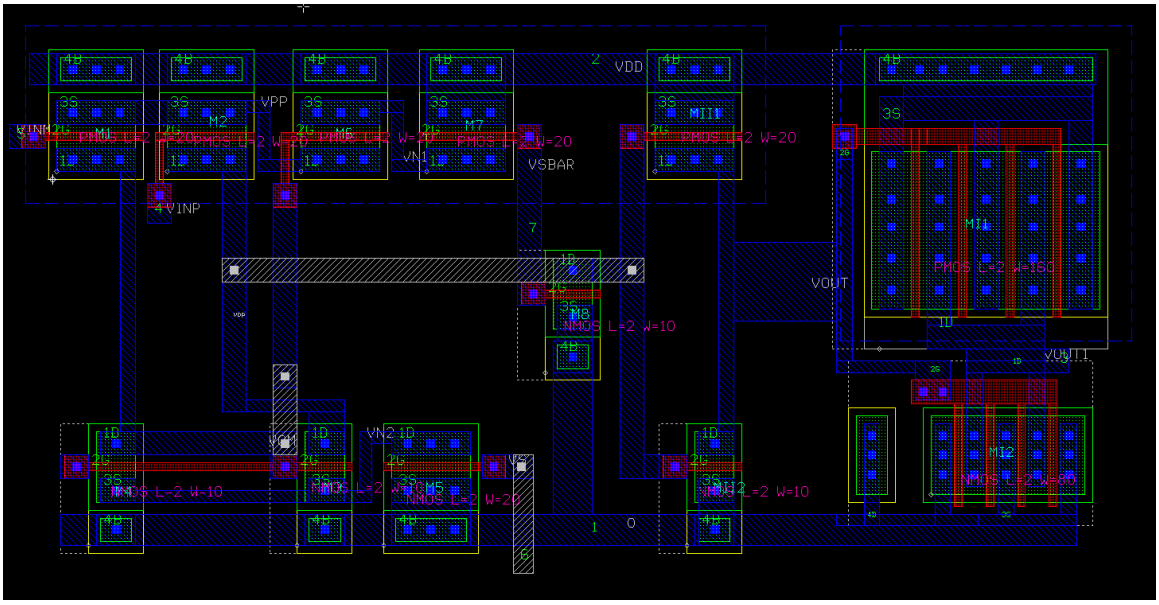


Figure 2.21 Layout of PMOS buffer

Micrograph showing the PMOS input buffer: -

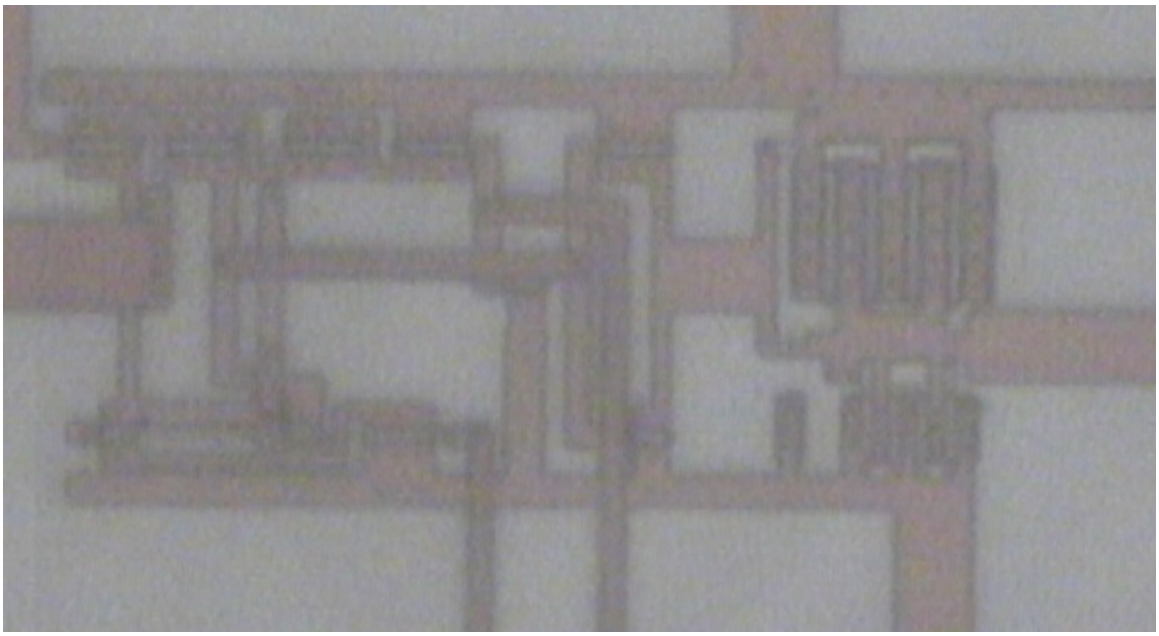


Figure 2.22 Fabricated image of PMOS buffer

Parallel Input buffer design: -

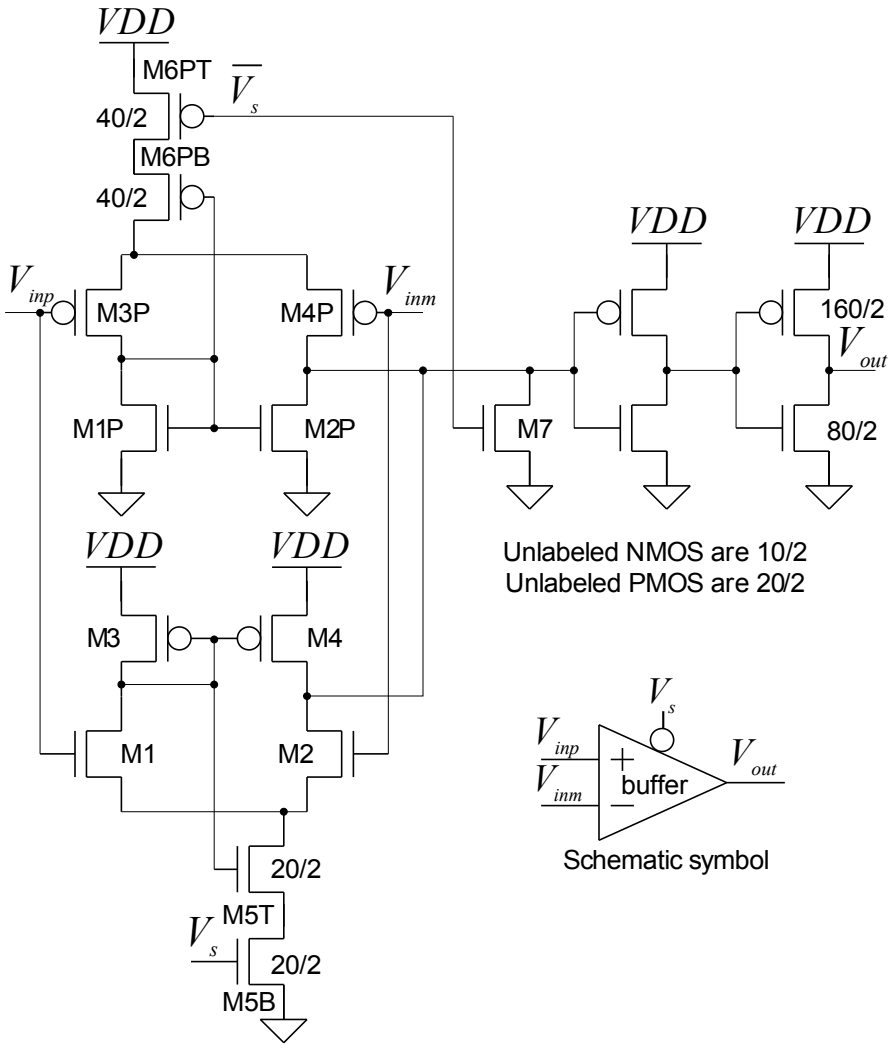


Figure 2.23 Schematic diagram of a rail to rail input buffer [1]

To avoid the offset from PMOS version, the NMOS buffer can be used in parallel with a PMOS buffer show in figure 2.23, to form an input buffer that operates well with input signals approaching ground and VDD. The topology with the buffers in parallel provides a robust input buffer that works for a wide range of input voltages.

Simulation results of parallel buffer: -

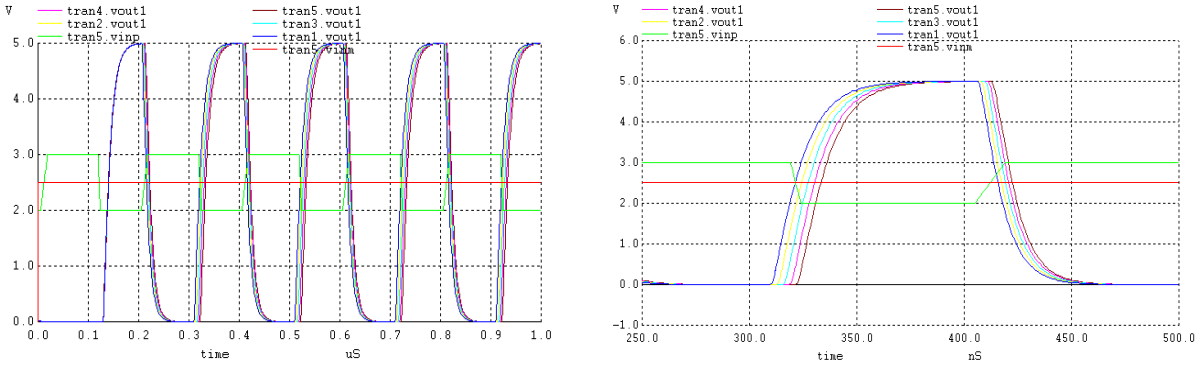


Figure 2.24 Simulations for Rise time sweep with enable (tran1-2ns, tran2=5ns, tran3=8ns,tran4=11ns and tran5=14ns)

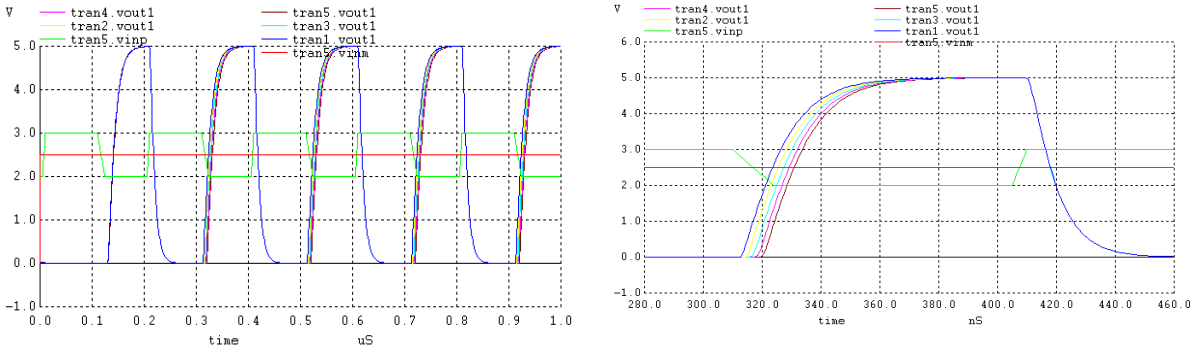


Figure 2.25 Simulations for Fall time sweep with enable (tran1-2ns, tran2=5ns, tran3=8ns,tran4=11ns and tran5=14ns)

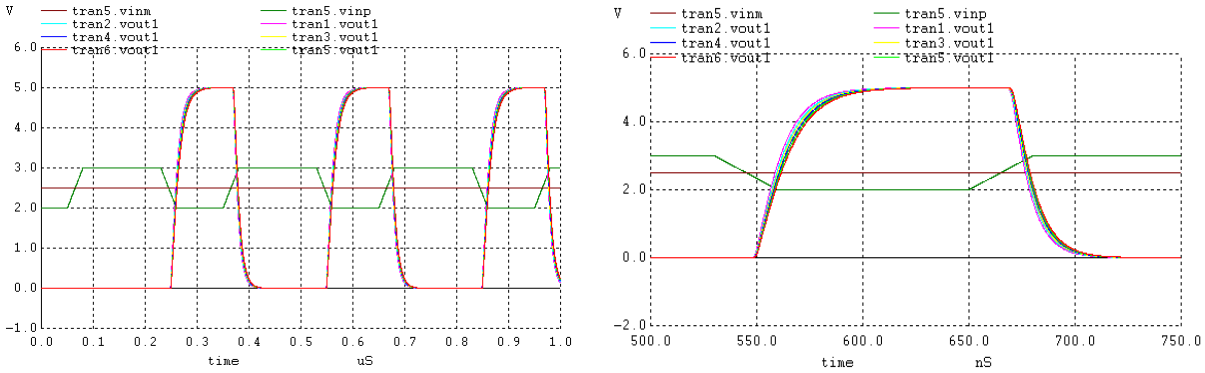


Figure 2.26 Cross temperature simulation results and corresponding zoomed in view.

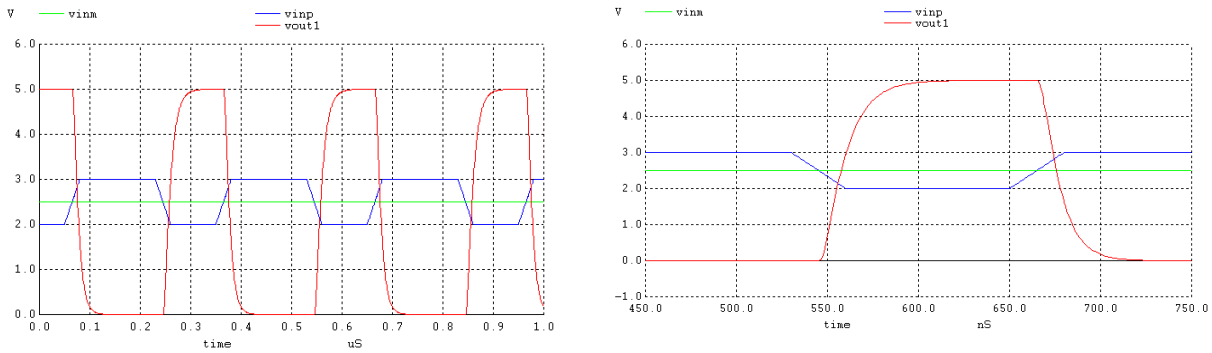


Figure 2.27 Simulations showing the output of the Parallel input buffer and its zoomed in view

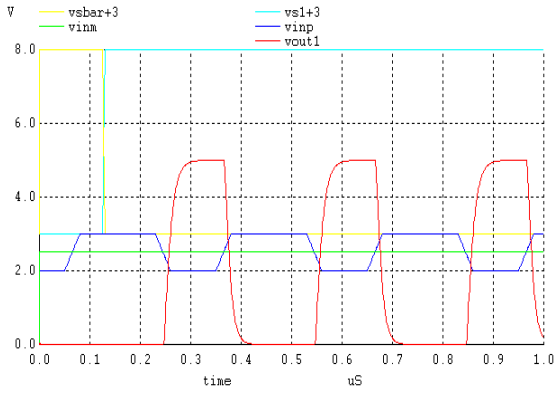


Figure 2.28 Sweeping Vdd with enable

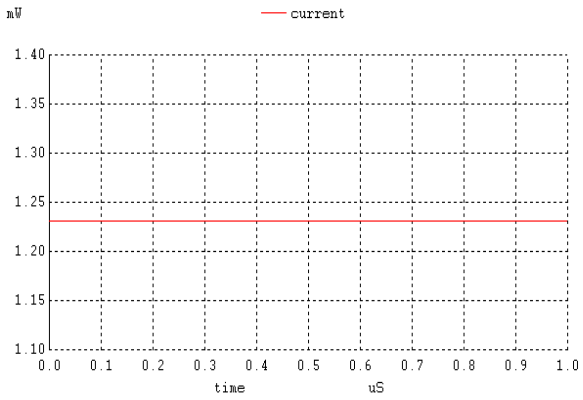


Figure 2.29 Current when switching

Layout of a parallel input buffer: -

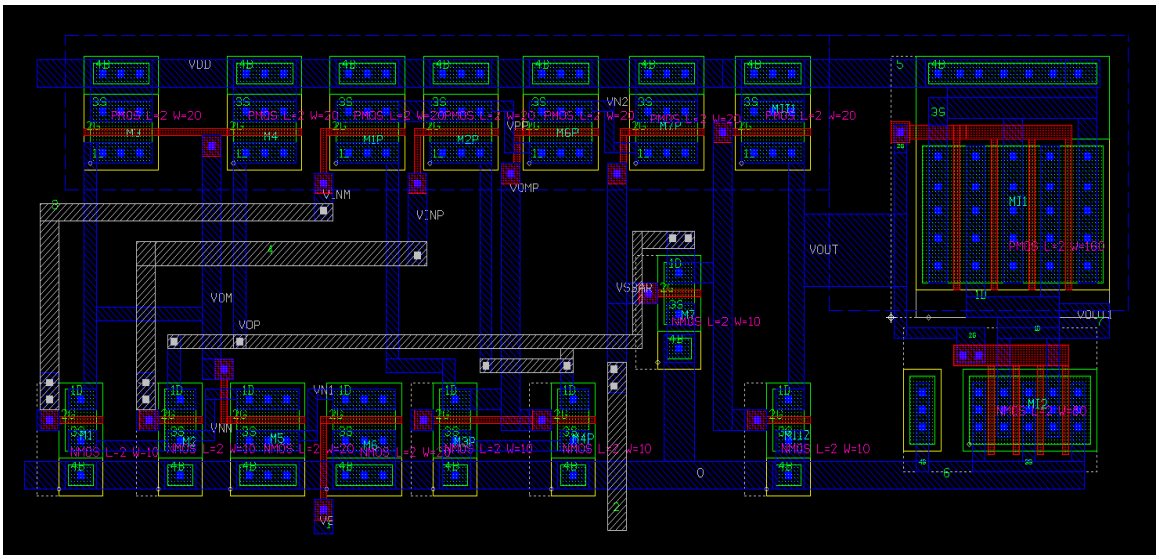


Figure 2.30 Layout of parallel buffer circuit

Micrograph showing the Parallel input buffer: -

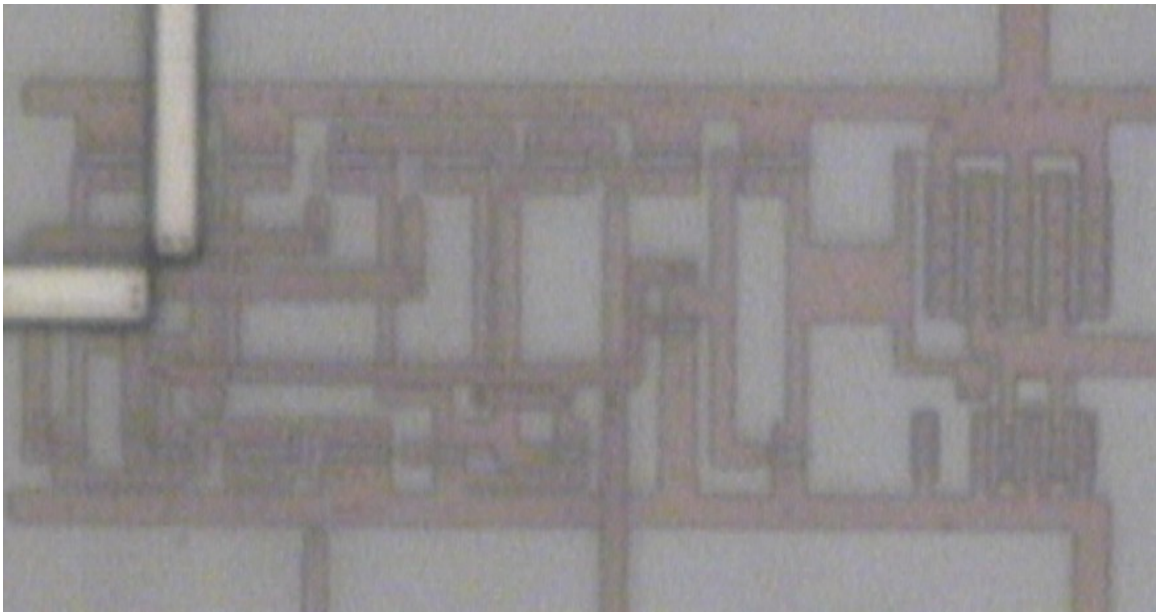


Figure 2.31 Image showing the fabricated parallel buffer

CHAPTER 3: MOSFET Digital Model and Delay calculations

Switching Resistance Calculation: -

The switching resistance in the digital circuits is estimated by using the following approximation. In the following figure 3.1, the capacitor is initially charged to VDD. When the NMOS switch is closed i.e. when V_{GS} is zero, then the drain of the MOSFET is at VDD. When V_{GS} is taken to VDD, the drain current in the NMOS switch is given by equation 1.

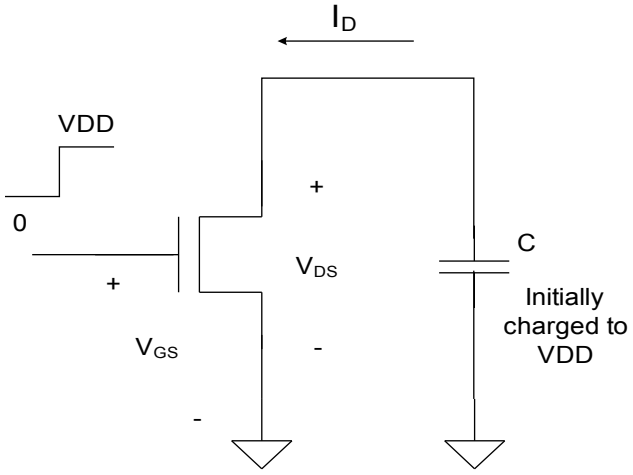


Figure 3.1 NMOS switching circuit [1]

$$I_D = \frac{KP_n}{2} \cdot \frac{W}{L} \cdot (VDD - V_{THN})^2 = \frac{b}{2} \cdot (VDD - V_{THN})^2 \qquad (1)$$

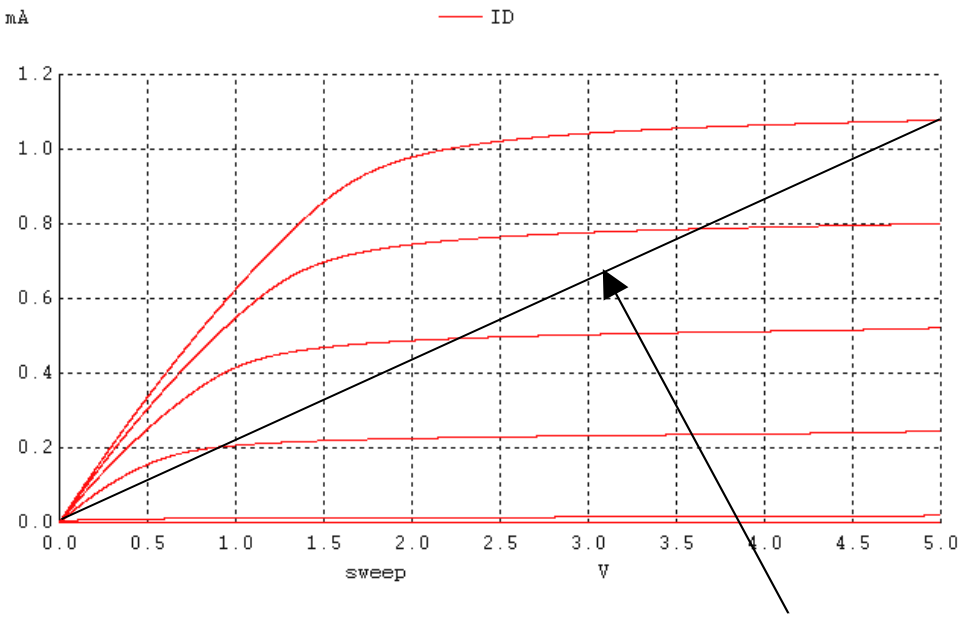


Figure 3.2 IV plot for 10/2 NMOS device for estimating the switching resistance of the current design.

From the above simulation results, the current obtained for a 10/2 NMOS device with a VDD of 5V is around 1.08mA.

$$R_n = \frac{VDD}{I_D} = \frac{VDD}{\frac{KP_n}{2}.\frac{W}{L}.(VDD - V_{THN})^2} = R_n'.\frac{L}{W}$$

$$R_n = \frac{VDD}{I_{D,sat}} = \frac{5}{1.08mA} \text{ Þ } 4.6k\text{W}$$

Therefore, the switching resistance for an NMOS device in this design is

$R_n \text{ » } ٤.٦k.\frac{L}{W}$, and the switching resistance for a PMOS device is estimated as

$R_p \text{ » } ١٣.٨k.\frac{L}{W}$

The oxide capacitance in this design is estimated as $C_{ox} = C'_{ox} WL.(scale)^2$

$C'_{ox} = \frac{e_{ox}}{t_{ox}} = 2.52\, fF/\mu m^2$, where t_{ox}=139 A^0.

Based upon the above calculated values, tables 1 and table2 summarizes the effective switching resistances and oxide capacitances for CN5 CMOS processes used in this design.

Table 1: Device characteristics summary for AMI s CN5 CMOS process

MOSFET parameters for present design with VDD=5V and a scale factor of 300nm (scale =300nm)			
Parameter	**NMOS**	**PMOS**	**Comments**
V_{THN} and V_{THP}	770mV	870mV	Typical
KP_n and KP_p	115 μA/V^2	38 μA/V^2	t_{ox}=139 A^0
$C'_{ox} = \frac{e_{ox}}{t_{ox}}$	$2.52\, fF/\mu m^2$	$2.52\, fF/\mu m^2$	t_{ox}=139 A^0
l_n and l_p	0.024 V^{-1}	0.023 V^{-1}	at L=2
C_{ox}	4.5 fF	9 fF	$C_{ox} = C'_{ox} WL.(scale)^2$
R_n and R_p	$R_n \gg 4.6k.\frac{L}{W}$	$R_p \gg 13.8k.\frac{L}{W}$	Scale=0.3 μm

Table 2: Digital Model parameters for calculating the delay times

Technology	R_n	R_p	**Scale factor**	$C_{ox} = C'_{ox} WL.(scale)^2$
AMI CN5	$R_n \gg ٤.٦k.\frac{L}{W}$	$R_p \gg ١٣.٨k.\frac{L}{W}$	0.3 μm	(2.52 fF).WL

CHAPTER 4: Results

Test Setup: -

The input buffers were tested using the setup shown in the figure below. The common mode reference voltage Vref was nominally kept at 2.5V and the input differential signal Vp (clock pulses with 1MHz frequency) was applied at the positive terminal of the buffer. The net delay was measured as the sum of charging and discharging delays (i.e. tpLH + tpHL).

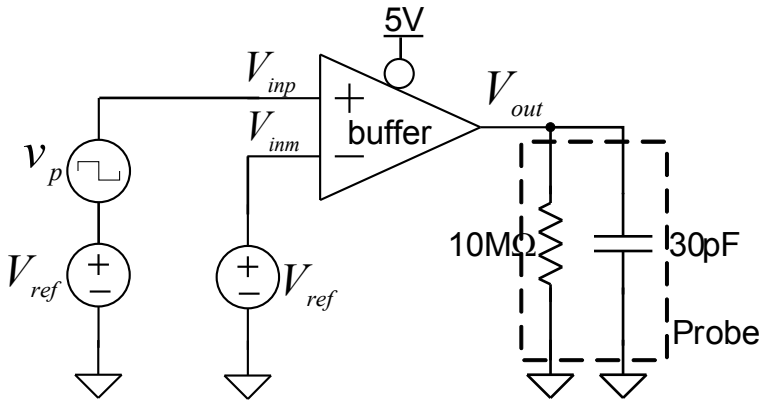


Figure 4.1: - Test setup for the input buffers

Simulations have been performed using the SPICE simulator to check the changes in delays with the variations of supply voltage, temperature, reference voltage, and rise and fall times.

Different spice model parameters in AMI's CN5 processes like fast-fast, slow-slow and typical are used and simulated to see the performance of the input buffers. The net delays are less sensitive to variation in processing, temperature and supply voltages which are

desirable in several applications in digital CMOS integrated circuits where precision, high speed and high production yields are required. Ideally these delays are independent on these performance issues.

The change in delay with the change in supply voltage, reference voltage, rise time, fall time and temperature for the input buffer circuits are shown below. For the Delay Vs VDD graph shown below, the delays are calculated using fast, typical and slow model parameters. The simulation results and the test results are shown side by side for the three topologies for comparison.

(1) **Delay Vs supply voltage (VDD): -**

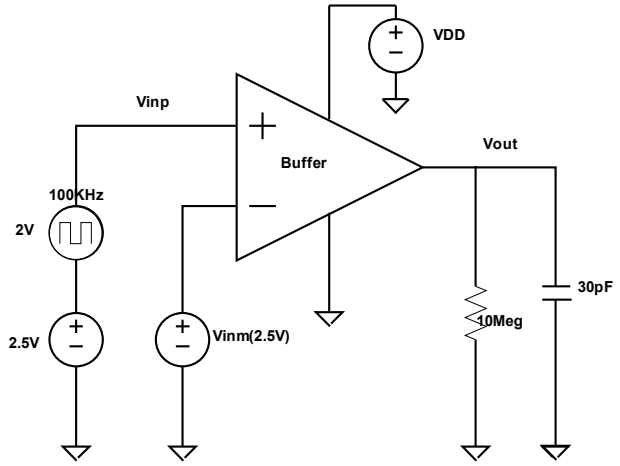


Figure 4.2: - Block diagram for simulating delay Vs supply voltage.

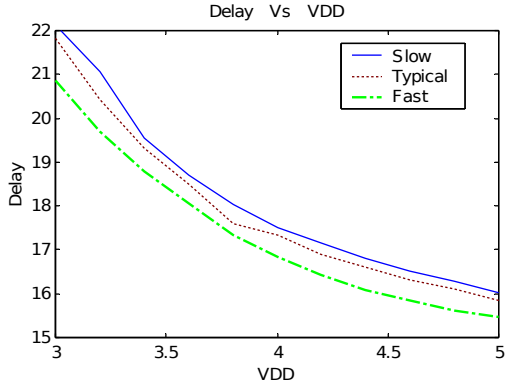
The below graphs are plotted to see the variation of the delay (ns) with respect to the supply voltage for three different spice parameter models (slow, typical and fast). The delay times is less for fast parameters when compared with the slow and typical corner parameters. Since the Differential amplifier is self biased, the bias current is proportional

to VDD. When VDD is increased, the bias current increases, which in turn increases the transconductance (gm). Thus the increase in VDD increases the differential amplifier's speed and reduces the delay.

The test results are shown adjacent to the simulation results for the variation of delay times with respect to the change in the supply voltage (VDD) for (a) NMOS (b) PMOS and (c) PARALLEL input buffers respectively.

(a) **NMOS Input buffer: -**

Simulation results



Test results

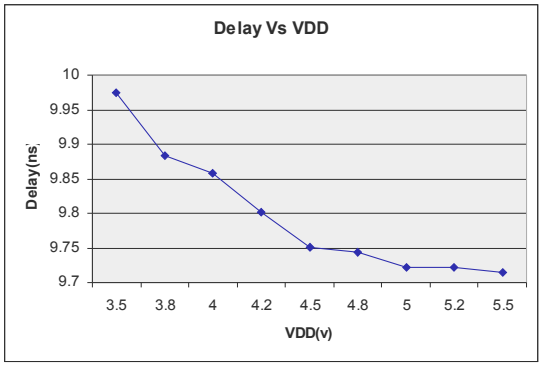
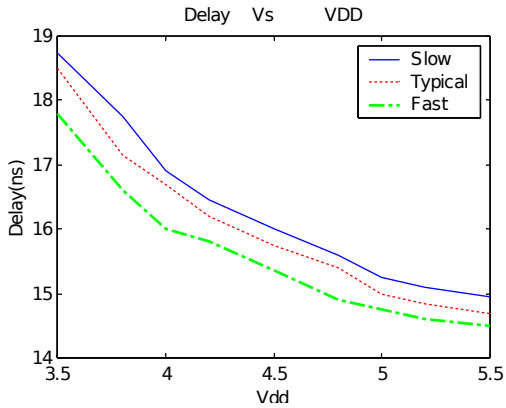


Figure 4.3: -Simulation and test results of NMOS buffer for delay plotted against VDD

(b) **PMOS Input buffer: -**

Simulation results

Test results



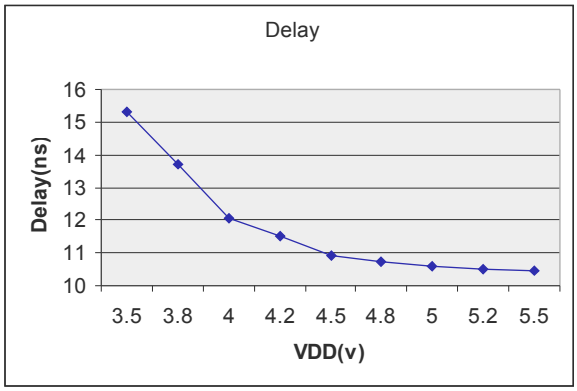
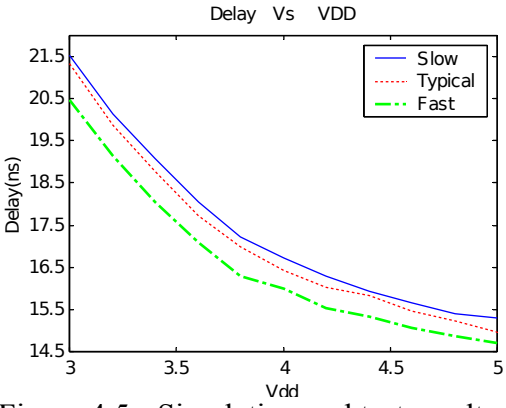


Figure 4.4: -Simulation and test results of PMOS buffer for delay plotted against VDD

(c) **Parallel Input buffer: -**

Simulation results



Test results

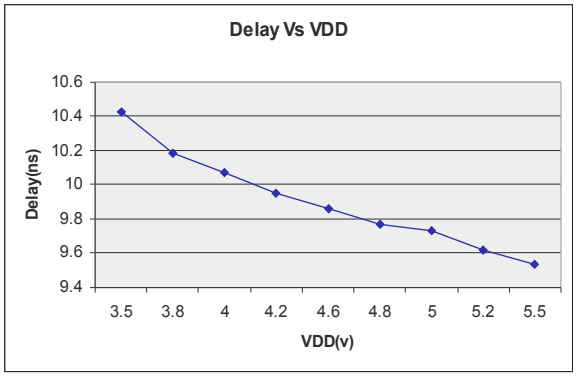


Figure 4.5: -Simulation and test results of NMOS buffer for delay plotted against VDD

Following figure shows the delay times with respect to the variation of supply voltage (VDD) for NMOS, PMOS and Parallel input buffers. The delay times are characterized on the fabricated circuits. The delay times for PMOS buffer is less when compared with the NMOS because PMOS has higher resistance than that of the NMOS. The parallel buffer has optimal delay times when compared with the other two topologies.

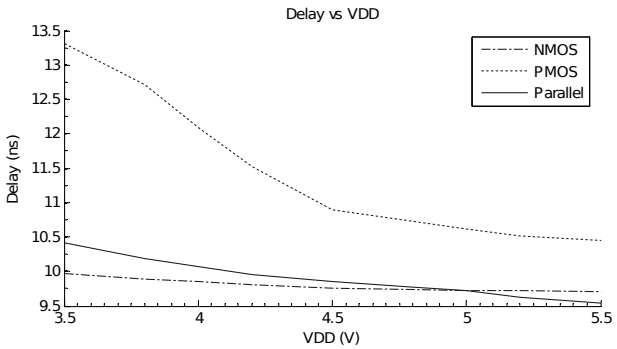


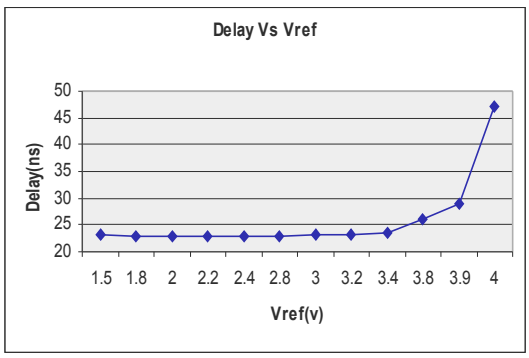
Figure 4.6: - Delay vs supply voltage (*VDD*) plot for the input buffers

(2) Delay Vs Reference voltage: -

Graph below shows the variation of delay times (ns) with respect to the variation of the reference Voltage (Vref).

(a) NMOS Input buffer: -

Simulation results



Test results

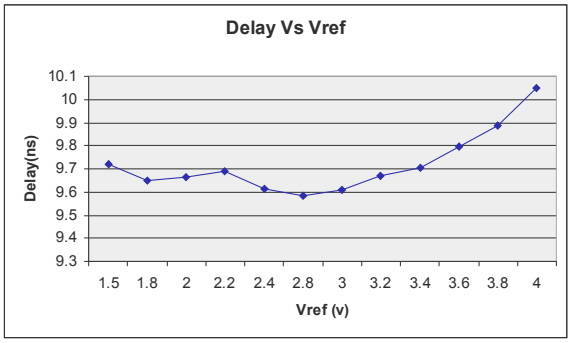


Figure 4.7: -Simulation and test results of NMOS buffer for delay plotted against Vref

(b) PMOS Input buffer: -

Simulation results

Test results

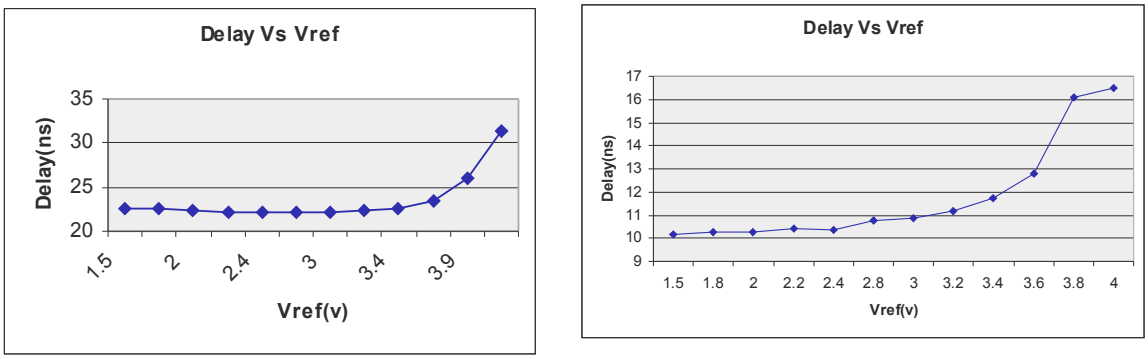


Figure 4.8: -Simulation and test results of NMOS buffer for delay plotted against VDD

(χ) **Parallel Input buffer: -**

Simulation results

Test results

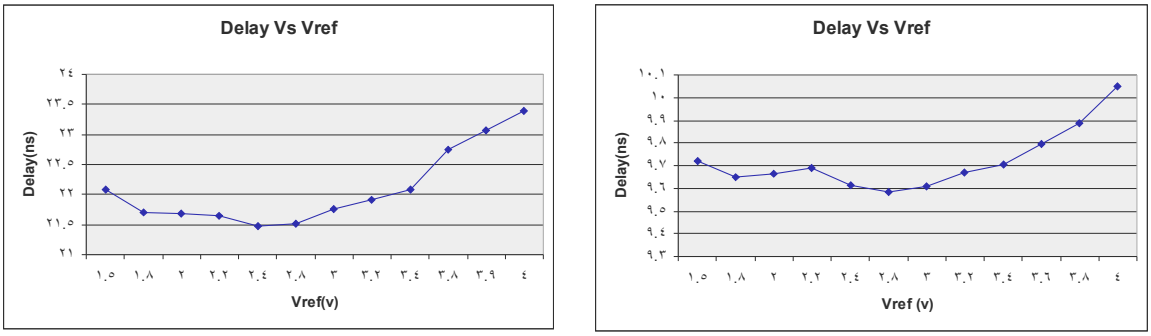


Figure 4.9: - Simulation and test results of delay versus vref for parallel buffer

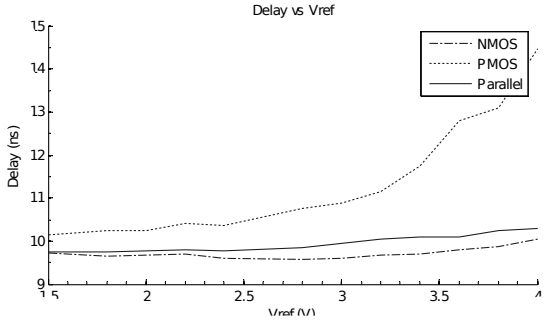


Figure 4.10: -Test results of delay vs common mode reference (*Vref*) plot for the input buffers.

(3) Delay Vs temperature: -

Plots below are the simulation results showing the variation of delay times (ns) with respect to the variation of the temperature.

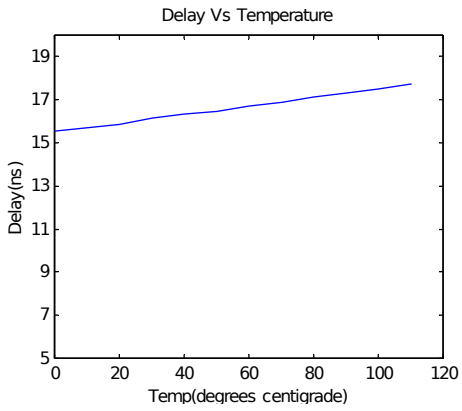


Figure 4.11 Delay vs temperature (NMOS)

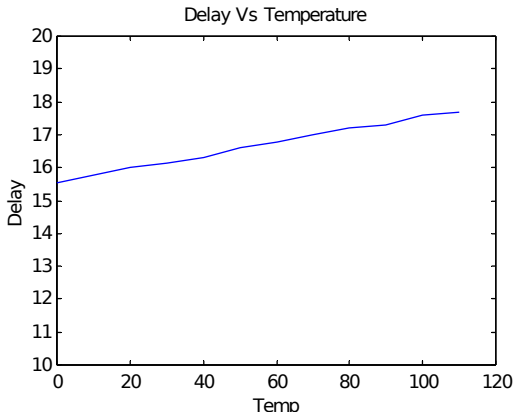


Figure 4.12 Delay vs temperature (PMOS)

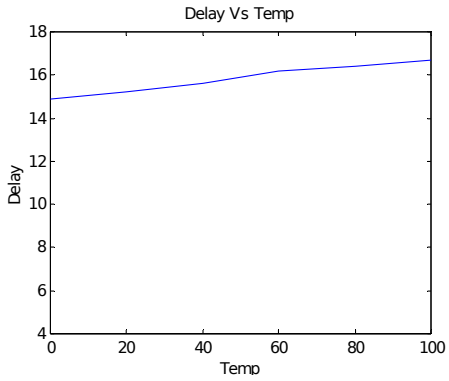


Figure 4.13 Delay vs temperature (parallel)

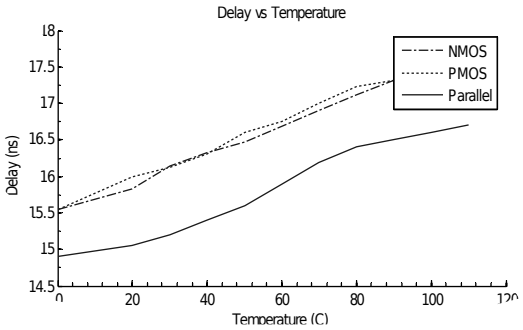


Figure 4.14 Simulated delay vs temperature plot for the input buffers.

(4) Plots below shows the delay Vs rise time and fall times

Delay Vs Rise time **Delay Vs Fall time**

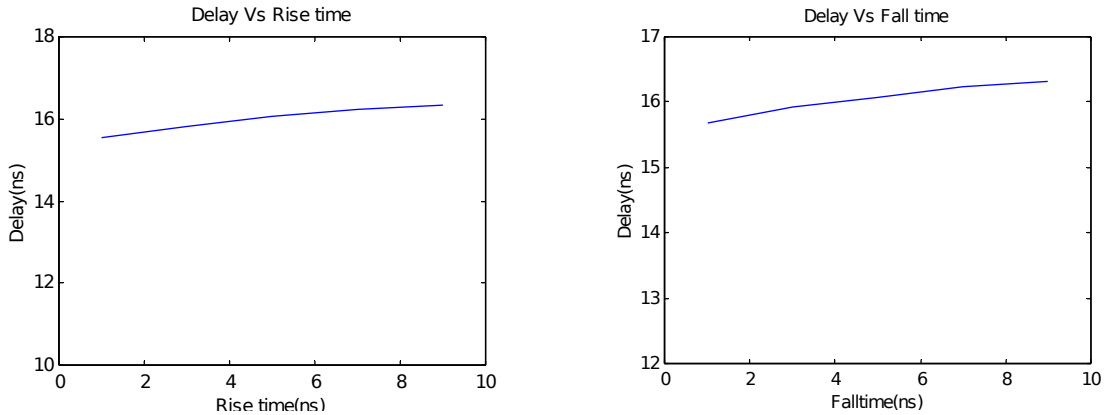


Figure 4.15 Simulation results for delay vs rise time and fall times for NMOS buffers

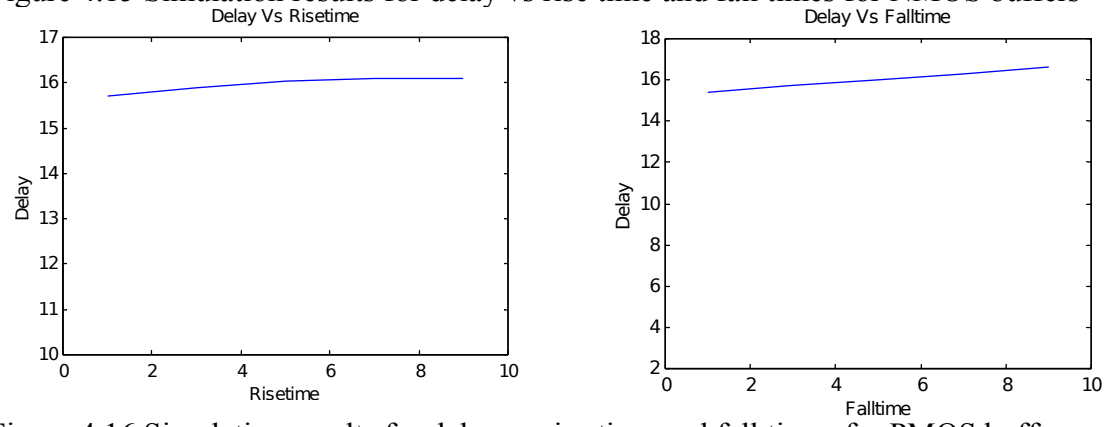


Figure 4.16 Simulation results for delay vs rise time and fall times for PMOS buffers

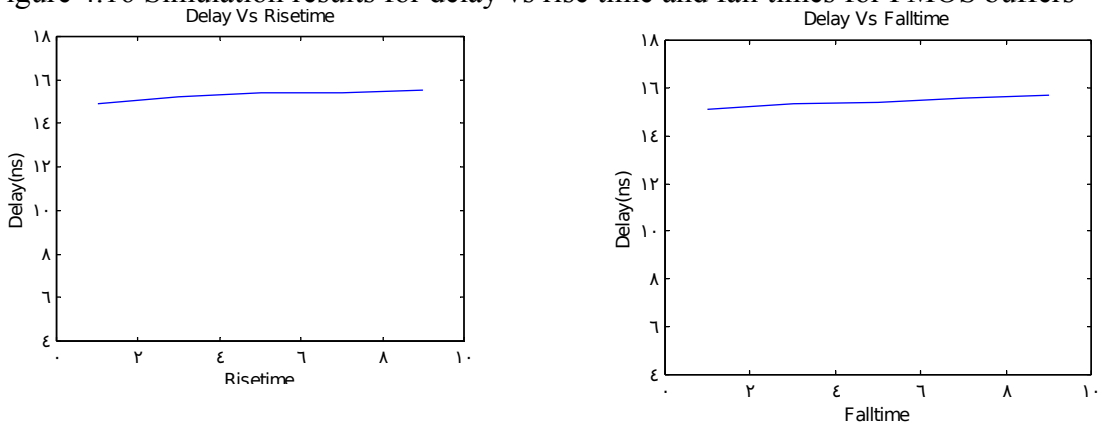


Figure 4.17 Simulation results for delay vs rise time and fall times for parallel buffers

(5) Test results showing the delay times Vs input signal swing: -

Plots shown below are the block diagram and test results determining the change in the input signal swing (Vinp) with peak to peak voltage varying around an offset of 2.5V and with the reference voltage (Vinm) of 2.5V. For low input voltage, the delay times of

NMOS are greater than the PMOS and for higher voltages; PMOS delay is greater than the NMOS delay.

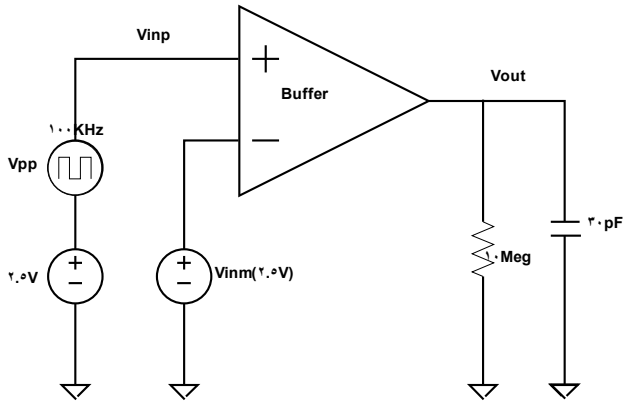


Figure 4.18 Block diagram for delay Vs input signal swing.

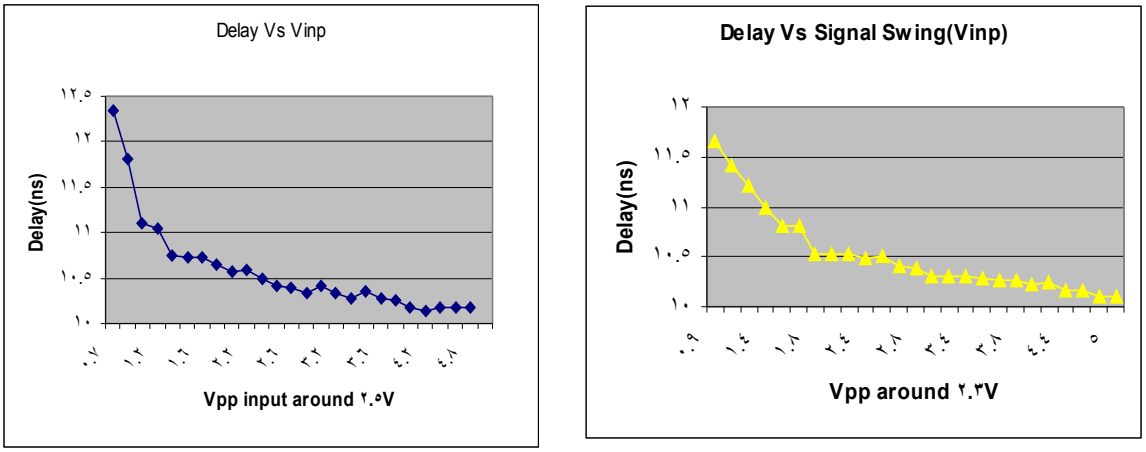


Figure 4.19 Test results -delay vs vinp for NMOS (vpp=2.5V) and for PMOS (vpp=2.3V)

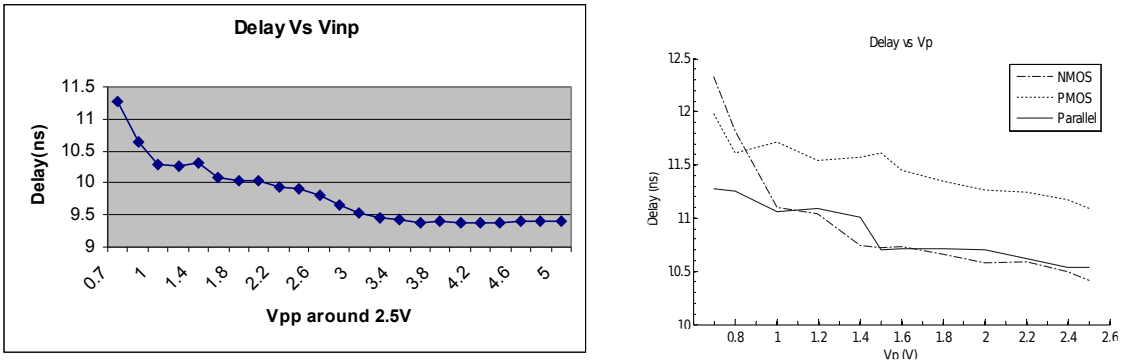


Figure 4.20 Test results-delay vs vinp (vpp=2.5) for parallel

Figure 4.21 Delay vs input signal swing (*Vp*) plot for the input buffers.

The test results demonstrate that the designed input buffers operate well for high-speed input signals. The delay is virtually independent of power supply voltage, input common mode reference and voltage swing. The output pulse is highly symmetric and skew is absent. The parallel buffer topology provides the optimal performance for wide range of input voltages.

CHAPTER 5: Conclusion

Layout and Fabrication of Input Buffer circuits: -

Figure 5.1 shows the layout of the full chip. LASI CAD software is used for the circuit layout. Ground- signal –ground pads are used in the layout with a pitch of 150um. Other pads are VDD, Vref and enable pads. Test structures are used in testing the chip. Open, short and with a 50 ohm load. One row is buffer circuits (PMOS, NMOS and parallel) with enable circuits and the other row is without enable circuits. Figure 5.2 is the micrograph of the input buffer circuits fabricated on a chip. The buffer circuits are fabricated in AMI's CN5 (0.5um) process with a VDD of 5V. The buffers are designed to drive a load of 30pF which accounts for the load offered by the probe setup. A large inverter is used to drive the large load with optimal delay.

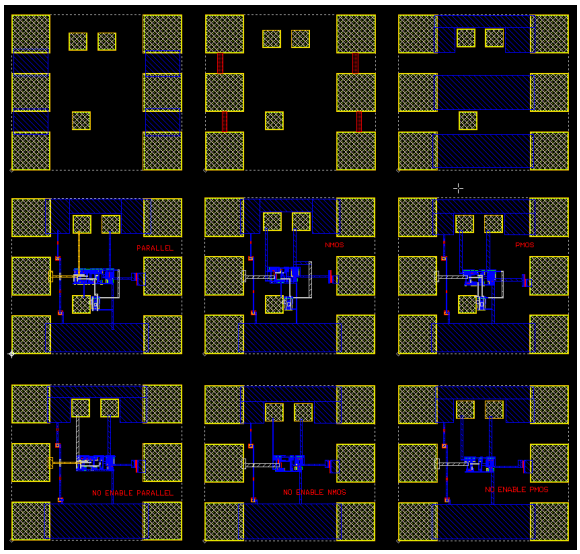


Figure 5.1 Layout of the chip

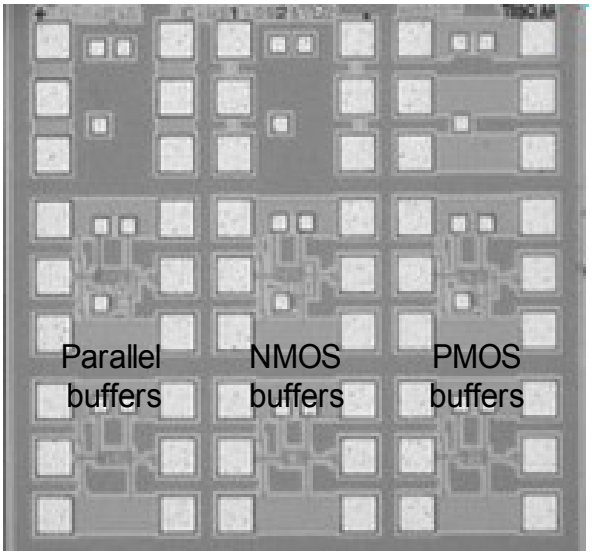


Figure 5.2 Micrograph of the chip

Conclusion

A set of differential high-speed input buffers have been designed, fabricated and tested. The designed input buffers have been processed in AMI's CN5 (0.5um) CMOS processes with a die size of 1.5 x 1.5 mm^2 and a supply voltage of 5V with a scale factor of 0.3um. NMOS buffer doesn't work quickly when the input falls below V_{THN}.

PMOS version of input buffer can be used for lower input signal levels but has a larger offset. To avoid the offset, the NMOS buffer can be used in parallel with a PMOS buffer. Parallel buffer topology provides a robust input buffer that works for a wide range of input voltages. The buffer circuits are designed to drive a load of 30pF which accounts for the load offered by the probe setup. A large inverter (160/80) is used to drive the large load with optimal delay. All the buffers circuits are designed and fabricated with an enable circuit and employs self biased differential amplifier as no external reference voltage is need to set the bias current in the circuit.

The designed input buffers provide high frequency operation with lower delays. The delays are nearly independent of variations in power supply, input signal common mode and differential voltages, and temperature.

APPENDIX A

DEVICE CHARACTERISTICS AND R-C CIRCUITS

Threshold Voltage of the Devices: -

The threshold voltage of NMOS and PMOS is determined by the simulations shown in the figures A1 and A2.

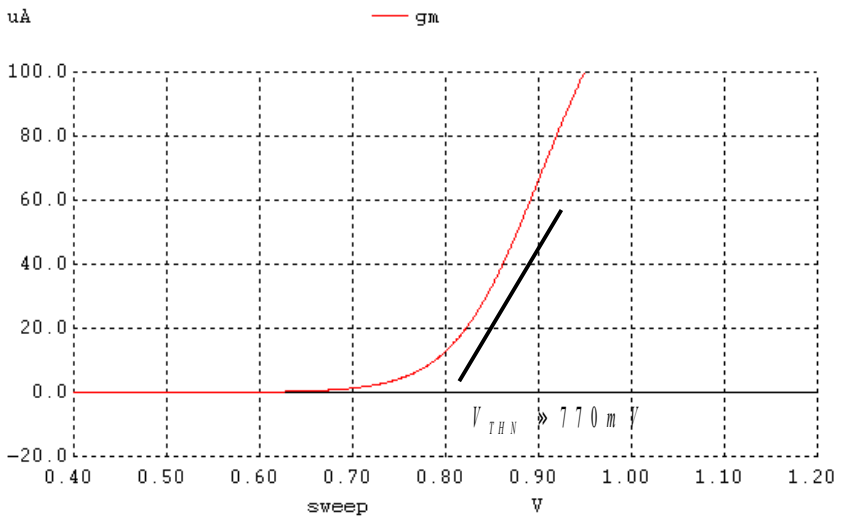


Figure A1 Transconductance (gm) plotted against V_{GS} for NMOS device

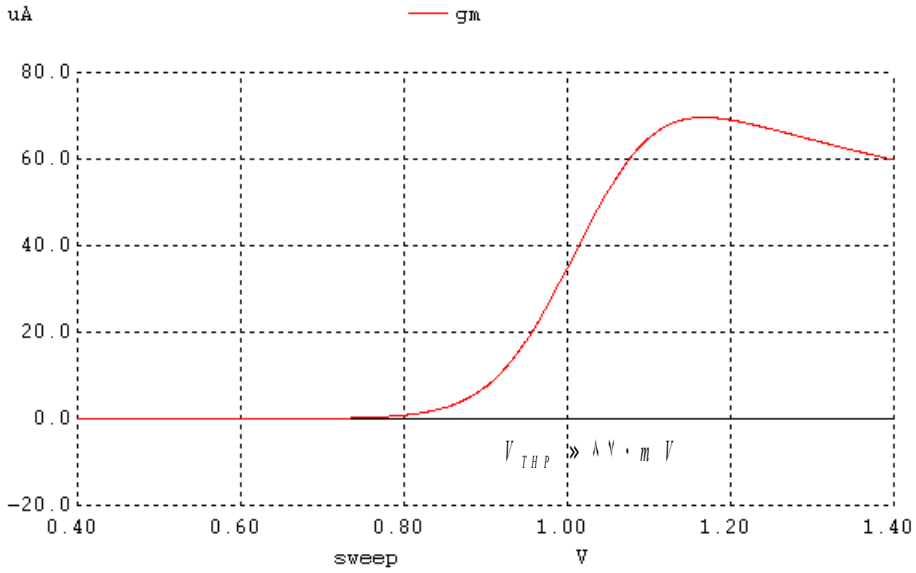


Figure A2 Transconductance (gm) plotted against V_{SG} for PMOS device

R-C NETWORKS

Rise Time: The time taken for the output voltage to rise from 10% to 90% of the input voltage is defined as the rise time.

Fall Time: The fall time is defined as the time taken for the output to fall from 90% of the input value to 10% of the input value.

Time Constant: The product of the resistance and the capacitance value is called the time constant of the simple R-C network. The time constant for a circuit varies depending on the network components.

Equation governing charging of the capacitor:

$$V_{out} = V_{in}.(1 - e^{-\frac{t}{R.C}}) \quad \text{.....(A.1)}$$

Equation governing the discharging of the capacitor:

$$V_{out} = V_{in}.e^{-\frac{t}{R.C}} \quad \text{.....(A.2)}$$

Where V_{in}= input voltage, t=time in seconds, R=Resistance in ohms, C=Capacitance in Farads.

Consider the R-C network as shown in the figure A.3.The output of the circuit for R=10K and C=100pF is also shown in the same figure to the right.

In this case Rise time=Fall time=2.5us.

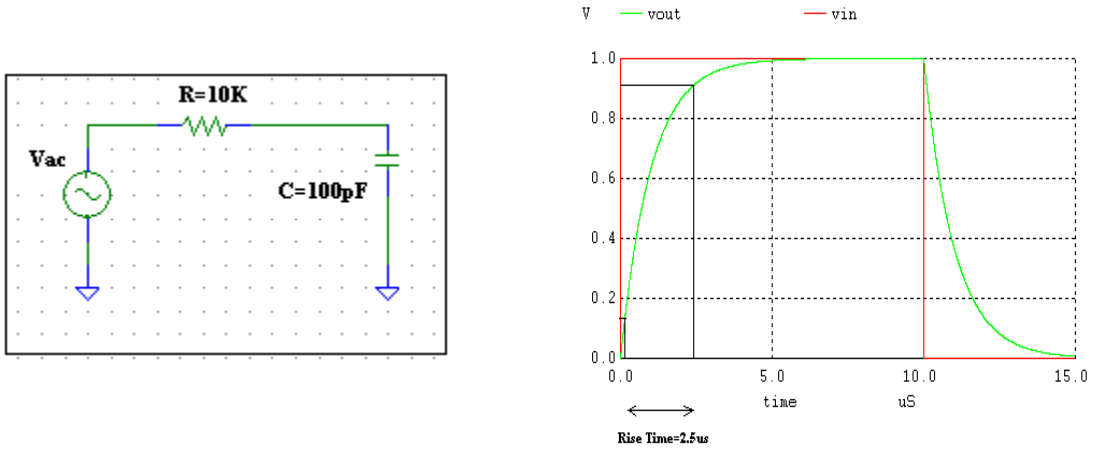


Figure A.3: R-C network to the left and transient response to the right.

Charge Sharing Principle

The charge sharing principle is basically dependent on charge between two capacitors To better understand this, consider two capacitors in parallel with a switch in between them as shown in figure A4.Assuming voltage on C1 is V1 and C2 is V2 before closing the switch. So the total charge on the capacitors before the switch closes is given by:

$$Q_{before} = C1.V1 + C2.V2 \quad \text{.....(A.3)}$$

Let's say the voltage on the capacitors after the switch closes is V_{final}.

By the law of conservation of charge:

$$Q_{before} = Q_{after} \quad \text{.....(A.4)}$$

$$\Rightarrow C_1.V_1 + C_2.V_2 = (C_1 + C_2).V_f \quad \text{.....(A.5)}$$

$$V_f = \frac{(C_1.V_1 + C_2.V_2)}{C_1 + C_2} \quad \text{.....(A.6)}$$

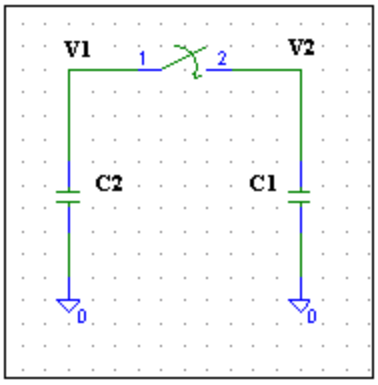


Figure A.4: Charge sharing phenomena between two capacitors.

Compensation technique for the scope probes

In this project, the input buffers are designed and simulated with an output load of 30pF in parallel with a 10Meg resistor. This is because the capacitances of the input buffer circuits are very small (generally in femtofarads) and while micro probing the input buffers, there will be an addition of extra capacitance. This is explained with the figure shown below.

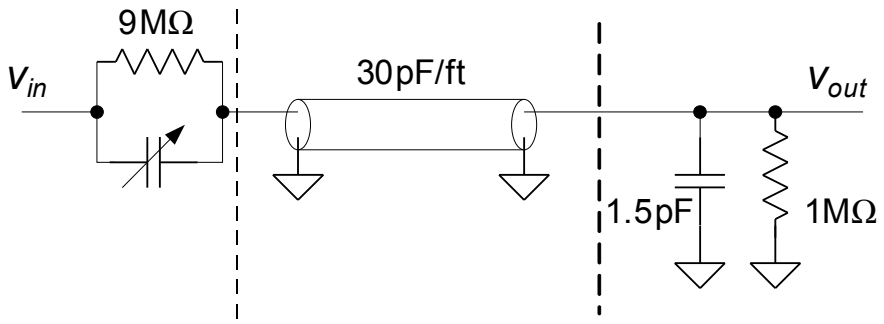


Figure A5 Schematic representation of the scope probe setup.

Generally, the oscilloscope has an input impedance of 1Mohm resistor in parallel with a 10pF capacitor. The probe cable (co-axial cable) has a capacitance of 100pF/m when connected between the input of the oscilloscope and the Device under test (DUT). The total capacitance of the probe cable and the oscilloscope is around 110pF. This adds 100pF of capacitance in parallel with 1Mohm resistor to the circuit which increases the delays and might cause the circuits to fail. The probe cable capacitance is compensated by adding a series resistor and a capacitor in between the cable and the probe tip which is called as 'compensated scope probe'. The total probe cable capacitance and the input capacitance of the scope can be lumped together as C_1. R_1 is the input resistance of the

scope which is typically equal to 1MΩ. R_2 is the series resistance in the probe tip while C_2 is the tunable compensation capacitance in the probe tip.

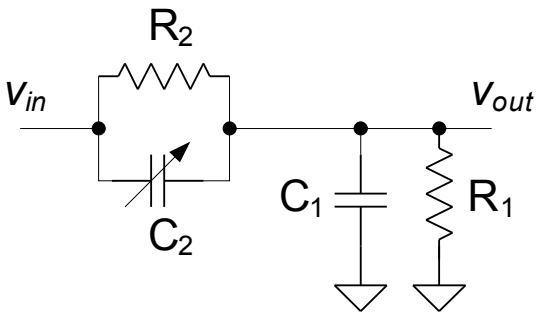


Figure A6 Equivalent circuit for the scope probe.

Due to the compensated scope probe, a 10:1 voltage divider is exist between the probe tip and the input of the oscilloscope i.e. the RC time constant is adjusted such that it is nine times the impedance of the RC of probe cable and the oscilloscope. The overall loading after the compensation is greatly reduced to around 10pF in parallel with 10Mohm.

APPENDIX B

SPICE MODELS AND NETLIST

NETLIST

```
.control
destroy all
run
plot current
plot vout1 vinm vinp
.endc

.option scale=0.3u
.tran 1n 1u

VDD     VDD     0       DC      5
Vinp    Vinp    0       DC      0       pulse 2 3 50n 30n 30n 150n 300n
Vinm    Vinm    0       DC      2.5
VSBAR   VSBAR   0       DC      0       PULSE 5 0 125n 5n 5n 1u 1u
VS1     VS1     0       DC      0       PULSE 0 5 125n 5n 5n 1u 1u

M1p     Vomp    Vinm    Vppp    VDD     PMOS L=2 W=20
M2p     Vop     Vinp    Vppp    VDD     PMOS L=2 W=20
M5p     Vppp    Vomp    Vn2     VDD     PMOS L=2 W=40
M6p     Vn2     VSBAR   VDD     VDD     PMOS L=2 W=40

M3p     Vomp    Vomp    0       0       NMOS L=2 W=10
M4p     Vop     Vomp    0       0       NMOS L=2 W=10

M1      Vom     Vinm    Vnn     0       NMOS L=2 W=10
M2      Vop     Vinp    Vnn     0       NMOS L=2 W=10
M5      Vnn     Vom     Vn1     0       NMOS L=2 W=20
M6      Vn1     VS1     0       0       NMOS L=2 W=20
M3      Vom     Vom     VDD     VDD     PMOS L=2 W=20
M4      Vop     Vom     VDD     VDD     PMOS L=2 W=20
```

M7	Vop	VSBAR	0	0	NMOS L=2 W=20
MI1	Vout	Vop	0	0	NMOS L=2 W=10
MI2	Vout	Vop	VDD	VDD	PMOS L=2 W=20
MII1	Vout1	Vout	0	0	NMOS L=2 W=80
MII2	Vout1	Vout	VDD	VDD	PMOS L=2 W=160

SPICE MODELS

* DATE: May 23/02

```
* Tech: AMI_C5N
* LOT: T22Y_SS (SLOW-SLOW)              WAF: 3102
* Temperature_parameters=Optimized
.MODEL nMOS NMOS (                          LEVEL   = 49
+VERSION = 3.1              TNOM    = 27            TOX     = 1.39E-8
+XJ      = 1.5E-7           NCH     = 1.7E17        VTH0    = 0.7087481
+K1      = 0.9382905        K2      = -0.1120562    K3      = 23.0789213
+K3B     = -7.3398981       W0      = 1E-8          NLX     = 1E-9
+DVT0W   = 0                DVT1W   = 0             DVT2W   = 0
+DVT0    = 3.3388333        DVT1    = 0.4283914     DVT2    = -0.0952143
+U0      = 459.674806       UA      = 1E-13         UB      = 1.503507E-18
+UC      = 1.325863E-11     VSAT    = 1.682969E5    A0      = 0.4784067
+AGS     = 0.0995613        B0      = 2.644452E-6   B1      = 5E-6
+KETA    = -5.808373E-3     A1      = 1.027068E-4   A2      = 0.3400289
+RDSW    = 1.329687E3       PRWG    = 0.0432392     PRWB    = 0.0149808
+WR      = 1                WINT    = 2.420178E-7   LINT    = 3.239617E-8
+XL      = 0                XW      = 0             DWG     = -1.396728E-8
+DWB     = 5.6316E-8        VOFF    = -2.57933E-3   NFACTOR = 0.8759425
+CIT     = 0                CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0                ETA0    = 0.0152264     ETAB    = -1.058244E-3
+DSUB    = 0.2005917        PCLM    = 2.6613926     PDIBLC1 = -0.7606454
+PDIBLC2 = 2.593415E-3      PDIBLCB = -0.0326937    DROUT   = 0.6688818
+PSCBE1  = 5.85807E8        PSCBE2  = 7.988657E-5   PVAG    = 0
+DELTA   = 0.01             RSH     = 81.9          MOBMOD  = 1
+PRT     = 8.621            UTE     = -1            KT1     = -0.2501
+KT1L    = -2.58E-9         KT2     = 0             UA1     = 5.4E-10
+UB1     = -4.8E-19         UC1     = -7.5E-11      AT      = 1E5
+WL      = 0                WLN     = 1             WW      = 0
+WWN     = 1                WWL     = 0             LL      = 0
+LLN     = 1                LW      = 0             LWN     = 1
+LWL     = 0                CAPMOD  = 2             XPART   = 0.5
+CGDO    = 2.02E-10         CGSO    = 2.02E-10      CGBO    = 1E-9
+CJ      = 4.198358E-4      PB      = 0.99          MJ      = 0.4516115
+CJSW    = 3.241716E-10     PBSW    = 0.1000811     MJSW    = 0.1152935
+CJSWG   = 1.64E-10         PBSWG   = 0.1000811     MJSWG   = 0.1152935
+CF      = 0                PVTH0   = 0.0681426     PRDSW   = 188.2442761
+PK2     = -0.0295712       WKETA   = -0.0264969    LKETA   = -2.950307E-5
+AF      = 1            KF      = 0)
*
.MODEL pMOS PMOS ( LEVEL   = 49
+VERSION = 3.1              TNOM    = 27            TOX     = 1.39E-8
+XJ      = 1.5E-7           NCH     = 1.7E17        VTH0    = -0.9223355
+K1      = 0.5769702        K2      = 9.039555E-3   K3      = 6.34861
+K3B     = -0.6383676       W0      = 1E-8          NLX     = 4.747861E-8
+DVT0W   = 0                DVT1W   = 0             DVT2W   = 0
+DVT0    = 2.4578035        DVT1    = 0.576459      DVT2    = -0.1206691
```

```
+U0      = 211.8308394        UA      = 2.824327E-9    UB      = 1E-21
+UC      = -5.66493E-11       VSAT    = 1.622935E5     A0      = 0.8712138
+AGS     = 0.1383793          B0      = 7.726776E-7    B1      = 5E-6
+KETA    = -5.205201E-3       A1      = 2.378013E-5    A2      = 0.3
+RDSW    = 3E3                PRWG    = -0.0454944     PRWB    = -2.13823E-4
+WR      = 1                  WINT    = 2.849786E-7    LINT    = 5.529217E-8
+XL      = 0                  XW      = 0              DWG     = -1.840088E-8
+DWB     = 2.185555E-8        VOFF    = -0.0684347     NFACTOR = 0.9119466
+CIT     = 0                  CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0                  ETA0    = 0.3751245      ETAB    = -0.0827039
+DSUB    = 1                  PCLM    = 2.2966371      PDIBLC1 = 0.0365228
+PDIBLC2 = 3.733251E-3        PDIBLCB = -0.0621219     DROUT   = 0.2123397
+PSCBE1  = 7.499863E9         PSCBE2  = 7.328296E-10   PVAG    = 4.584372E-6
+DELTA   = 0.01               RSH     = 101.9          MOBMOD  = 1
+PRT     = 59.494             UTE     = -1             KT1     = -0.2942
+KT1L    = 1.68E-9            KT2     = 0              UA1     = 4.5E-9
+UB1     = -6.3E-18           UC1     = -1E-10         AT      = 1E3
+WL      = 0                  WLN     = 1              WW      = 0
+WWN     = 1                  WWL     = 0              LL      = 0
+LLN     = 1                  LW      = 0              LWN     = 1
+LWL     = 0                  CAPMOD  = 2              XPART   = 0.5
+CGDO    = 2.84E-10           CGSO    = 2.84E-10       CGBO    = 1E-9
+CJ      = 7.235521E-4        PB      = 0.9527404      MJ      = 0.4955303
+CJSW    = 2.692736E-10       PBSW    = 0.99           MJSW    = 0.295843
+CJSWG   = 6.4E-11            PBSWG   = 0.99           MJSWG   = 0.295843
+CF      = 0                  PVTH0   = 5.98016E-3     PRDSW   = 14.8598424
+PK2     = 3.73981E-3         WKETA   = 4.75772E-3     LKETA   = -6.715425E-3
+AF      = 1            KF      = 0)
*
* DATE: May 22/02
* Tech: AMI_C5N
* LOT: T22Y_FF (FAST-FAST)              WAF: 3110
* Temperature_parameters=Optimized
.MODEL nMOS NMOS (                          LEVEL   = 49
+VERSION = 3.1          TNOM    = 27            TOX     = 1.39E-8
+XJ      = 1.5E-7       NCH     = 1.7E17        VTH0    = 0.6252608
+K1      = 0.8530381    K2      = -0.0937042    K3      = 25.5736581
+K3B     = -7.2969383   W0      = 1E-8          NLX     = 1E-9
+DVT0W   = 0            DVT1W   = 0             DVT2W   = 0
+DVT0    = 3.4153341    DVT1    = 0.4318353     DVT2    = -0.1001188
+U0      = 461.2276323  UA      = 1E-13         UB      = 1.46812E-18
+UC      = 1.421961E-11 VSAT    = 1.555424E5    A0      = 0.7155223
+AGS     = 0.1483817    B0      = 2.54418E-6    B1      = 5E-6
+KETA    = 1.388284E-5  A1      = 7.294903E-5   A2      = 0.3921052
+RDSW    = 1.305357E3   PRWG    = 0.0488517     PRWB    = 0.0366783
+WR      = 1            WINT    = 2.274256E-7   LINT    = 3.776271E-8
```

```
+XL     = 0          XW     = 0          DWG    = -8.845179E-9
+DWB    = 6.105959E-8   VOFF   = 0          NFACTOR = 0.5636274
+CIT    = 0          CDSC   = 2.4E-4      CDSCD  = 0
+CDSCB  = 0          ETA0   = 0.0345642   ETAB   = -1.428288E-3
+DSUB   = 0.3127341   PCLM   = 2.6236271   PDIBLC1 = -0.3319738
+PDIBLC2 = 2.390366E-3   PDIBLCB = -0.0300257   DROUT  = 0.6600306
+PSCBE1  = 5.488078E8   PSCBE2  = 4.431797E-5   PVAG   = 0
+DELTA  = 0.01       RSH    = 81.8       MOBMOD = 1
+PRT    = 8.621      UTE    = -1         KT1    = -0.2501
+KT1L   = -2.58E-9   KT2    = 0          UA1    = 5.4E-10
+UB1    = -4.8E-19   UC1    = -7.5E-11   AT     = 1E5
+WL     = 0          WLN    = 1          WW     = 0
+WWN    = 1          WWL    = 0          LL     = 0
+LLN    = 1          LW     = 0          LWN    = 1
+LWL    = 0          CAPMOD = 2          XPART  = 0.5
+CGDO   = 1.98E-10   CGSO   = 1.98E-10   CGBO   = 1E-9
+CJ     = 4.198358E-4   PB     = 0.99       MJ     = 0.4516115
+CJSW   = 3.241716E-10   PBSW   = 0.1000811   MJSW   = 0.1152935
+CJSWG  = 1.64E-10   PBSWG  = 0.1000811   MJSWG  = 0.1152935
+CF     = 0          PVTH0  = 0.1033668   PRDSW  = 59.9594347
+PK2    = -0.0304166   WKETA  = -0.0144288   LKETA  = 3.115505E-3
+AF     = 1          KF     = 0)
*
.MODEL pMOS PMOS (                   LEVEL  = 49
+VERSION = 3.1       TNOM   = 27         TOX    = 1.39E-8
+XJ     = 1.5E-7     NCH    = 1.7E17     VTH0   = -0.8880096
+K1     = 0.533922   K2     = 3.259424E-3   K3     = 4.9517158
+K3B    = -0.6918832   W0     = 1.515912E-8   NLX    = 3.554945E-9
+DVT0W  = 0          DVT1W  = 0          DVT2W  = 0
+DVT0   = 2.4926947   DVT1   = 0.530833   DVT2   = -0.1185572
+U0     = 211.6791804   UA     = 2.785001E-9   UB     = 1E-21
+UC     = -5.76365E-11   VSAT   = 1.732495E5   A0     = 0.9378784
+AGS    = 0.1630399   B0     = 7.147395E-7   B1     = 5E-6
+KETA   = 1.410441E-4   A1     = 0          A2     = 0.3
+RDSW   = 3E3        PRWG   = -0.0490272   PRWB   = 8.254155E-5
+WR     = 1          WINT   = 2.696991E-7   LINT   = 6.103973E-8
+XL     = 0          XW     = 0          DWG    = -1.293462E-8
+DWB    = 2.202201E-8   VOFF   = -0.0500647   NFACTOR = 0.8235545
+CIT    = 0          CDSC   = 2.4E-4      CDSCD  = 0
+CDSCB  = 0          ETA0   = 0.4342722   ETAB   = -6.780063E-3
+DSUB   = 1          PCLM   = 2.3221049   PDIBLC1 = 0.036845
+PDIBLC2 = 3.86901E-3   PDIBLCB = -0.0457025   DROUT  = 0.1909189
+PSCBE1  = 1.678442E10   PSCBE2  = 1.640115E-9   PVAG   = 0.0133488
+DELTA  = 0.01       RSH    = 101.7      MOBMOD = 1
+PRT    = 59.494     UTE    = -1         KT1    = -0.2942
+KT1L   = 1.68E-9    KT2    = 0          UA1    = 4.5E-9
```

```
+UB1    = -6.3E-18      UC1    = -1E-10        AT     = 1E3
+WL     = 0             WLN    = 1             WW     = 0
+WWN    = 1             WWL    = 0             LL     = 0
+LLN    = 1             LW     = 0             LWN    = 1
+LWL    = 0             CAPMOD = 2             XPART  = 0.5
+CGDO   = 2.75E-10      CGSO   = 2.75E-10      CGBO   = 1E-9
+CJ     = 7.235521E-4   PB     = 0.9527404     MJ     = 0.4955303
+CJSW   = 2.692736E-10  PBSW   = 0.99          MJSW   = 0.295843
+CJSWG  = 6.4E-11       PBSWG  = 0.99          MJSWG  = 0.295843
+CF     = 0             PVTH0  = 5.98016E-3    PRDSW  = 14.8598424
+PK2    = 3.73981E-3    WKETA  = 5.10041E-3    LKETA  = -1.725699E-3
+AF     = 1             KF     = 0)
*
* LOT: T22Y_TT (TYPICAL)                WAF: 3104
* Temperature_parameters=Optimized
.MODEL nMOS NMOS (                             LEVEL  = 49
+VERSION = 3.1          TNOM   = 27            TOX    = 1.39E-8
+XJ     = 1.5E-7        NCH    = 1.7E17        VTH0   = 0.6696061
+K1     = 0.8351612     K2     = -0.0839158    K3     = 23.1023856
+K3B    = -7.6841108    W0     = 1E-8          NLX    = 1E-9
+DVT0W  = 0             DVT1W  = 0             DVT2W  = 0
+DVT0   = 2.9047241     DVT1   = 0.4302695     DVT2   = -0.134857
+U0     = 458.439679    UA     = 1E-13         UB     = 1.485499E-18
+UC     = 1.629939E-11  VSAT   = 1.643993E5    A0     = 0.6103537
+AGS    = 0.1194608     B0     = 2.674756E-6   B1     = 5E-6
+KETA   = -2.640681E-3  A1     = 8.219585E-5   A2     = 0.3564792
+RDSW   = 1.387108E3    PRWG   = 0.0299916     PRWB   = 0.0363981
+WR     = 1             WINT   = 2.472348E-7   LINT   = 3.597605E-8
+XL     = 0             XW     = 0             DWG    = -1.287163E-8
+DWB    = 5.306586E-8   VOFF   = 0             NFACTOR = 0.8365585
+CIT    = 0             CDSC   = 2.4E-4        CDSCD  = 0
+CDSCB  = 0             ETA0   = 0.0246738     ETAB   = -1.406123E-3
+DSUB   = 0.2543458     PCLM   = 2.5945188     PDIBLC1 = -0.4282336
+PDIBLC2 = 2.311743E-3   PDIBLCB = -0.0272914    DROUT  = 0.7283566
+PSCBE1 = 5.598623E8    PSCBE2 = 5.461645E-5    PVAG   = 0
+DELTA  = 0.01          RSH    = 81.8          MOBMOD = 1
+PRT    = 8.621         UTE    = -1            KT1    = -0.2501
+KT1L   = -2.58E-9      KT2    = 0             UA1    = 5.4E-10
+UB1    = -4.8E-19      UC1    = -7.5E-11      AT     = 1E5
+WL     = 0             WLN    = 1             WW     = 0
+WWN    = 1             WWL    = 0             LL     = 0
+LLN    = 1             LW     = 0             LWN    = 1
+LWL    = 0             CAPMOD = 2             XPART  = 0.5
+CGDO   = 2E-10         CGSO   = 2E-10         CGBO   = 1E-9
+CJ     = 4.197772E-4   PB     = 0.99          MJ     = 0.4515044
+CJSW   = 3.242724E-10  PBSW   = 0.1           MJSW   = 0.1153991
```

```
+CJSWG   = 1.64E-10      PBSWG   = 0.1          MJSWG   = 0.1153991
+CF      = 0             PVTH0   = 0.0585501    PRDSW   = 133.285505
+PK2     = -0.0299638    WKETA   = -0.0248758   LKETA   = 1.173187E-3
+AF      = 1             KF      = 0)
*
.MODEL pMOS PMOS (                              LEVEL   = 49
+VERSION = 3.1           TNOM    = 27           TOX     = 1.39E-8
+XJ      = 1.5E-7        NCH     = 1.7E17       VTH0    = -0.9214347
+K1      = 0.5553722     K2      = 8.763328E-3  K3      = 6.3063558
+K3B     = -0.6487362    W0      = 1.280703E-8  NLX     = 2.593997E-8
+DVT0W   = 0             DVT1W   = 0            DVT2W   = 0
+DVT0    = 2.5131165     DVT1    = 0.5480536    DVT2    = -0.1186489
+U0      = 212.0166131   UA      = 2.807115E-9  UB      = 1E-21
+UC      = -5.82128E-11  VSAT    = 1.713601E5   A0      = 0.8430019
+AGS     = 0.1328608     B0      = 7.117912E-7  B1      = 5E-6
+KETA    = -3.674859E-3  A1      = 4.77502E-5   A2      = 0.3
+RDSW    = 2.837206E3    PRWG    = -0.0363908   PRWB    = -1.016722E-5
+WR      = 1             WINT    = 2.838038E-7  LINT    = 5.528807E-8
+XL      = 0             XW      = 0            DWG     = -1.606385E-8
+DWB     = 2.266386E-8   VOFF    = -0.0558512   NFACTOR = 0.9342488
+CIT     = 0             CDSC    = 2.4E-4       CDSCD   = 0
+CDSCB   = 0             ETA0    = 0.3251882    ETAB    = -0.0580325
+DSUB    = 1             PCLM    = 2.2409567    PDIBLC1 = 0.0411445
+PDIBLC2 = 3.355575E-3   PDIBLCB = -0.0551797   DROUT   = 0.2036901
+PSCBE1  = 6.44809E9     PSCBE2  = 6.300848E-10 PVAG    = 0
+DELTA   = 0.01          RSH     = 101.6        MOBMOD  = 1
+PRT     = 59.494        UTE     = -1           KT1     = -0.2942
+KT1L    = 1.68E-9       KT2     = 0            UA1     = 4.5E-9
+UB1     = -6.3E-18      UC1     = -1E-10       AT      = 1E3
+WL      = 0             WLN     = 1            WW      = 0
+WWN     = 1             WWL     = 0            LL      = 0
+LLN     = 1             LW      = 0            LWN     = 1
+LWL     = 0             CAPMOD  = 2            XPART   = 0.5
+CGDO    = 2.9E-10       CGSO    = 2.9E-10      CGBO    = 1E-9
+CJ      = 7.235528E-4   PB      = 0.9527355    MJ      = 0.4955293
+CJSW    = 2.692786E-10  PBSW    = 0.99         MJSW    = 0.2958392
+CJSWG   = 6.4E-11       PBSWG   = 0.99         MJSWG   = 0.2958392
+CF      = 0             PVTH0   = 5.98016E-3   PRDSW   = 14.8598424
+PK2     = 3.73981E-3    WKETA   = 5.292165E-3  LKETA   = -4.205905E-3
+AF      = 1             KF      = 0)
*
. End
```

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