FRONT-END CMOS TRANSIMPEDANCE AMPLIFIERS ON A SILICON PHOTOMULTIPLIER RESISTANT TO FAST NEUTRON FLUENCE

By

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ABSTRACT

Radiation hard electronics are indispensable in providing reliable diagnostics in fast radiation detection, which are necessary for new fundamental science research. In the case of radiation detection, transimpedance amplifiers are needed to magnify low photodetector signals to readable levels reliably. This thesis investigates a way to design a transimpedance CMOS-front-end transimpedance amplifier (TIA) as a first stage front-end amplifier. The TIA is to be mounted on silicon photomultiplier (SiPM), as a photodetector in fast neutron scintillation experiments capable of sustaining up to 10^{15} n/cm of fast neutrons in the range of 0.1 to 20 MeV. The proposed TIA was designed using "ON's C5 process" (a 600 nm CMOS process). It has a ~300 kΩ gain, a bandwidth minimum of 250 MHz, noise below 5 pA/√Hz, an output swing of 1.5–2 V, and a power consumption less than 25 mW. The TIA is expected to sustain reliable performance (<50%) up to a total integrated fluence of 10^{15} n/cm^2. Neutron damage is mainly knock out atoms that cause cascades of displaced atoms and trap creation in SiO_2 passivation layers and is not problematic as it is in ionizing radiation and not taken into account in this investigation. Therefore, a design of a transimpedance amplifier with the capacity to amplify low current from a SiPM, with a fast-transient response for single-photon detection and with high radiation hardness for reliable performance under fast neutron irradiation was designed and simulated.

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CHAPTER 1 INTRODUCTION

In 1986, a nuclear accident occurred when the Chernobyl power plant exploded. A flawed reactor design that was operated with inadequately trained personnel resulted in a steam explosion and fires released at least 5% of the radioactive reactor core into the environment, depositing radioactive material on various parts of Europe. Two Chernobyl plant workers died due to the explosion on the night of the accident, and a further 28 people died within a few weeks as a result of acute radiation syndrome [1]. Years later, another accident occurred in a nuclear power plant in Fukushima. Plant ruins have retained high radiation unhospitable to humans. Robots that were deployed to these areas failed within several hours because of the high radiation [2]. Therefore, the question arises as to whether electronics with high radiation tolerance could be used to investigate these high radioactive areas. Even though we cannot accurately predict the future, one may believe that radiation hard electronics could help decrease the probability of future accidents. One type of radiation essential to consider is neutron radiation, which is known to produce displacements in semiconductor devices that are difficult to anneal by themselves without a high energy input such as high temperature.

Neutron radiation damage on silicon semiconductors is an area of interest in space exploration, fusion studies, nuclear reactors, and atomic bomb stewardship. These applications require reliable and predictable device performance. For specific applications, changing the electronics used is difficult, and making simulation on how a device will work in high neutron-radiation environments results in an important step before fabrication. Fast neutrons, because of their high energy and neutral coulomb charge, damages electronics circuitry by direct interaction with the atomic nucleus. The primary defects they provoke are Frenkel pairs, which are a pair of a vacancy and an interstitial in the semiconductor lattice. These defects are formed by primary knock out atoms, that if energy high enough, form a cluster of displaced atoms. Such damage reduces mobility and

modifies doping levels in the semiconductor through the creation of traps that can become donors or acceptors. Besides, some fast neutrons might interact with impurities in the semiconductor or the package producing Frenkel pairs; on rare occasions, they can lose energy and be absorbed by the semiconductor nucleus producing a nuclei transmutation and create a different doping level [3]. Even more, the pairs might create traps or dislocations in the insulator affecting the transistor capacitances. Such defects can change the built-in voltage, as well as remove carriers affecting the drain-source current; however, the advantage of metal oxide semiconductor field effect transistors (MOSFETs) is that they seem insensitive to such defects and only sensitive to changes in transconductance [4] [5].

Scintillation enables the measurement of the number of high energy neutrons through the detection of photons by a photodetector coupled with a transimpedance amplifier. A transimpedance amplifier is an amplifier capable of amplifying input current signals and then outputting them as voltage signals. The sensors and transimpedance amplifiers involved in these measurements must be able to hold large neutron radiation fluences. Complementary metal oxide semiconductor (CMOS) transistors have shown to be radiation hard up to 10^{16} n/cm^2 [6]; therefore, CMOS transimpedance amplifiers can be used in harsh radiation environments and easily adapted on front-end designs (AFE), which are analog circuitries like analog amplifiers, filters needed to interface a variety of sensors. A CMOS process in an amplifier can reach high-speed amplification with high gains. CMOS transistors are superior to low power bipolar junction transistors (BJTs) on radiation hardness [6]. Nevertheless, the irradiation effects and the hardness level of metal oxide (MOS) transistors have shown to decrease transconductance and drain saturation current by removing majority carriers [5] [4]. Based on these reasons, a front-end transimpedance amplifier made with CMOS to amplify the signal of a silicon photomultiplier is proposed in this thesis.

CHAPTER 2 RADIATION ENVIRONMENTS

Fast neutron radiation is present in a variety of environments and applications since the discovery of the neutron in 1932 [7]. Scientists have been studying its nature and effects. Neutron technologies became widely used for a range of reasons as varied as medical imaging or therapies and producing a small "sun" on Earth. Nevertheless, neutron radiation is known to damage electronics and living organisms, and to cause transmutation of materials of stable radionuclides (when an element absorbs a neutron and becomes another element) [3]. Therefore, reviewing environments where neutron radiation predominates and might cause damage to semiconductor devices is important, and this is the topic of this work.

Some of the most revolutionary uses based on neutron radiation are in the medical field. Douglas et al. (2003) found that fast neutron irradiation is an effective way to treat patients with salivary gland neoplasms who have gross residual disease [8]. They used a cyclotron to produce protons, which then interacted with beryllium (Be) to produce neutrons. Another use is the measurement of fluoride content in human bones. To provide an alternative to painful bone biopsies, Chamberlain et al. (2012) developed a technique to measure bone-fluorine with low risk, by using neutron activation analysis via a $^{19}F(n,\gamma)^{20}F$ reaction, where n are neutrons, and γ are gamma rays [9]. Importantly, fast neutrons are also used in cancer therapy. In some cases, neutron therapy is better than gamma rays for cancer therapy, as described by Catterall et al. [10]. A portable fast neutron irradiation system was developed by Jing et al. in 2020 [11] for this reason.

Space is a source of many types of high energy particles, protons, gamma rays, alpha particles, muons, and neutrons, which are present from a variety of sources during space flights. Examples of these sources include terrestrial albedo, produced by neutrons when cosmic rays and other high energy particles interact with the Earth's atmosphere; secondary particles, which are

produced by the interactions between the same high energy particles and spacecraft materials; and solar flares [12]. Neutrons are an important consideration for space stations. The health of the crew members and the lifespan of the micro-electronics in a space station is related to the neutron flux passing through, and the altitude and latitude of a space station are also directly associated with the neutron-flux amplitude passing through it. The Russian scientists Litvak et al. have published measurements of neutron flux based on BTN-Neutron space experimental data acquired in 2007–2014, which ranged from 0.1 $n/cm^2/s$ in equatorial regions to 50 $n/cm^2/s$ in the South Atlantic anomaly region, in the energy range of 0.4 eV–15 MeV [13]. Therefore, electronics engineers must consider neutron fluence in designing reliable systems to be integrated into space applications.

Even though there is no more testing of nuclear weapons, many diagnostics in this field are exposed to large neutron fluence. Nuclear weapons made from plutonium-239 (^{239}Pu) produce high amounts of energy through fission. Diagnostics disintegrate after nuclear explosions. Consequently, whenever these tests are performed, having the largest number of working diagnostics possible is imperative to limit the number of experiments and, therefore, costs. Fissile material emits a large fluence of fast neutrons during an explosion, which destroys electronics. Thus, neutron fluence must be reduced. For example, Ebert reported to maintain scintillators functioning correctly, linear fluence must be less than 10^{11} n/cm^2 [14].

In fusion, a new type of technology that might provide a solution for our future energy needs, a large fluence of fast neutrons are emitted through deuterium and tritium (D-T) reactions. This arduous process is being researched in specialized laboratories worldwide, such as the Joint European Torus (JET) and the Mega Amp Spherical Tokamak (MAST) in the U.K., the ITER (International Thermonuclear Experimental Reactor) in France and The Chinese Fusion Engineering Test Reactor (CFETR), which is expected to be constructed in a few years. In the U.S.,

Sandia National Laboratory and Lawrence Livermore National Laboratory, among others, have large facilities, called the Z machine and the National Ignition Facility, respectively, to research the development of fusion. In these facilities, some experiments have indicated a neutron fluence yield on the order of 10^{12} (Z machine) [15] and 10^{16} n/cm^2 (NIF) [16]. Such large fluences result in high damage to diagnostics; however, they are low in comparison to unclear reactor fluence (10^{20} n/cm^2). Therefore, neutron shielding, and radiation hard electronics are difficult to achieve but are nonetheless relevant

CHAPTER 3 FAST NEUTRON SCINTILLATOR DETECTORS

Radiation detection through scintillation detection is used in fields such as homeland security, computed tomography, particle detectors, fusion research, nuclear cameras, space exploration, and tomography, among many others. TSA members are trained to use scintillation detectors to examine suspicious packages that might contain radiation contamination or nuclear explosives. Scintillation in fusion research is used to measure the D-T neutron yield to categorize the fusion process. Neutron detectors in fission reactors measure the fast neutron yield of ^{235}U (uranium). Fast neutron radiation detectors are necessary for many recent technologies, and electronic circuits must be reliable to be able to be used with them.

Scintillation is a process in which photoluminescence occurs when a scintillator material is excited by ionizing radiation. Scintillator materials absorb energy from incident particles and then expel the energy in the form of a photon, usually in the visible electromagnetic spectrum. Scintillation detectors are commonly used to measure high energy radiation in nuclear applications. These devices comprise a scintillator coupled photonic sensor, such as a photomultiplier tube (PMT), avalanche photodiode (APD), or silicon photomultiplier (SiPM). The scintillator absorbs energy from a high energy particle and then emits the absorbed energy as a photon with a visible wavelength. Emitted photons are absorbed by a photosensor, which outputs a voltage signal. Finally, the signal is measured and correlated to the number of particles irradiating the scintillator.

Neutron spectrum is categorized by its energy. Neutron categories range from low energy, cold neutrons to high energy, fast neutrons, through which ^{235}U, ^{239}Pu, ^{241}Pu, undergo fission. Such particles are difficult to measure because of their neutral charge. Therefore, a scintillator with a high visible light yield containing and specific isotopes, such as the commonly used ^{3}He, ^{6}Li, ^{10}B,

are necessary for neutron detection. Kahn and Machrafi from the University of Ontario Institute of Technology have found that a scintillator composed of Cs_2LiYCl_6 (CLYC) can overcome the challenges of low detection fast neutron detection efficiency, owing to the presence of the ^{35}Cl isotope [17]. They argue that the reaction of $^{35}Cl(n,p)^{35}S$ is useful for fast neutron detection because the energy from the emitted proton has a distinct peak in the detector response function. The high energy incident neutron would interact with the ^{35}Cl isotope through the following reaction:

$$ {}^{1}_{0}\mathrm{n} + {}^{35}_{17}\mathrm{Cl} \rightarrow {}^{35}_{16}\mathrm{S} + {}^{1}_{1}\mathrm{p} \qquad (1) $$

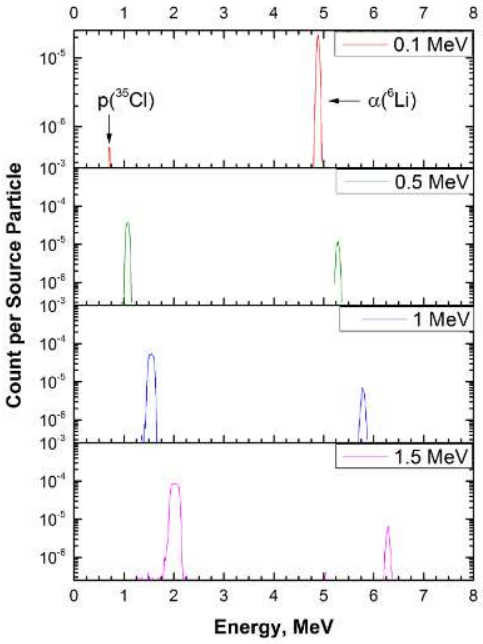

Figure 3.1 Detector response function to different neutron energies [17]

The authors have stated that "the Q-value of this reaction is 0.615 MeV. The emitted photon has an energy equal to the Q-value of this reaction plus the incident neutron energy; therefore, the incident neutron energy can be deduced using this full energy peak." Figure 3.1 shows a plot of count vs. neutron energy [17]. In contrast, Fisher et al. have reported the development of a fast neutron detector by using a liquid scintillator doped with ^{6}Li [18]. They used a technique called capture-gated neutron spectroscopy, which produces scintillation through recoil protons produced by scattered neutrons, as illustrated in Figure 2. The authors suggest that among the typical neutron capture isotopes, gadolinium, boron, and lithium, ^{6}Li is the best dopant because of its large Q-value and production of two energetic charge-particles. The isotope ^{6}Li has the following reaction with fast neutrons:

$$^{6}\mathrm{Li} + \mathrm{n} \rightarrow \mathrm{t}(2.05\ \mathrm{MeV}) + \alpha(2.73\ \mathrm{MeV}) \qquad (2)$$

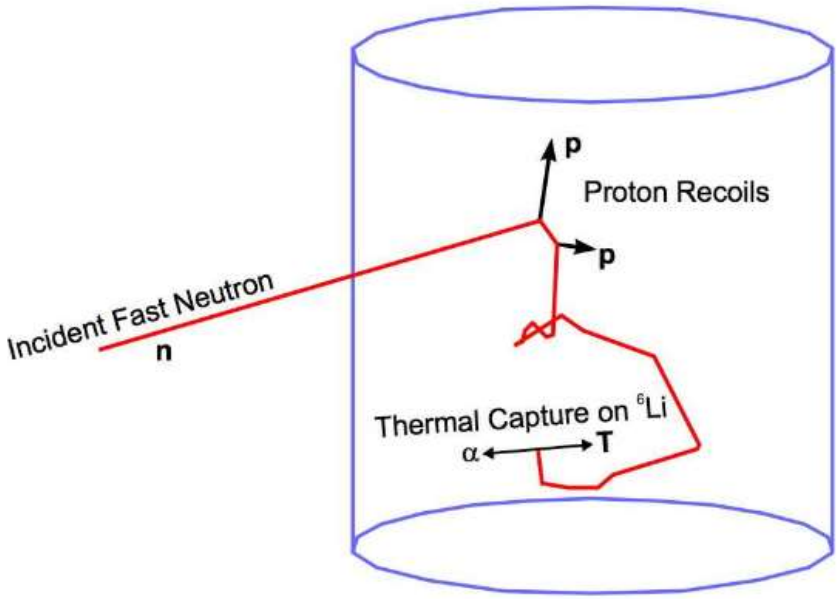

Figure 3.2 is an illustration of the principle of capture-gated detection. A fast neutron impinges on the detector. It rapidly gives up its energy through nuclear collisions, primarily with protons, in the moderation process. The thermalized neutron diffuses in the medium until it is captured on a material with a high capture cross-section [18]

To design a transimpedance amplifier with the capacity to amplify the signal output from scintillator photons, it is necessary to know the decay time of the scintillator material. Decay time indicates the maximum frequency bandwidth for which a circuit must amplify the signal composed of the maximum number of attainable pulses. Because neutron scintillation changes depending on the material and particle energy, specific material decay times must be studied to inform design. One of the most common materials used for fast neutron scintillation is $Cs_2LiYCl_6:Ce^{3+}$, which may be a potential candidate to replace LiI:Eu, which is currently a commonly used material for thermal neutron detection. The Li-content per cm^3 of Cs_2LiYCl_6 is 5.3 times lower than that of LiI, thus making neutron/gamma discrimination less efficient; nevertheless, Cs_2 $LiYCl_6:Ce^{3+}$ photon conversion is approximately 20 000 photons/MeV, and one-third of the emission decays within 600 ns (1.7 MHz) [19].

CHAPTER 4 PHOTODETECTORS

4.1 SOLID STATE PHOTODECTORS

Photodetectors are sensors that convert photons into electric current. Solid-state photodetectors are made from p-n junctions that convert photons into electron-hole pairs in the depletion region. This process occurs when a semiconductor is illuminated by photons with energy greater than or equal to the bandgap photons. The absorbed energy then excites electrons from the valence band to the conduction band, which then behave as free electrons. Electron-hole pairs created in this manner are called photocurrent. The most common photodetectors consist of a finite length semiconductor layer with ohmic contacts at each end and a fixed build-in voltage V.B. An example diagram of a photoconduction is shown in Figure 4.1.

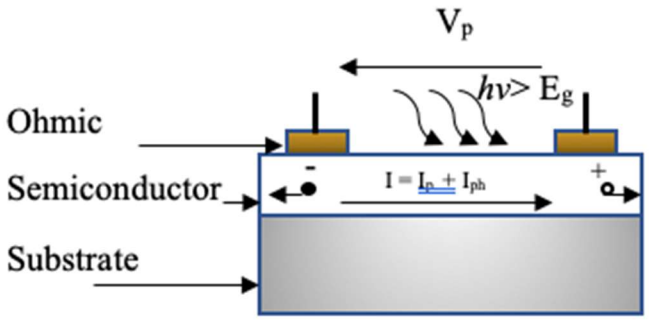

Figure 4.1 Diagram of a photoconducting device

Another typical photodetector is the p-n junction, which forms a depletion region with no free charge carriers. When a photon hits the semiconductor, an electron-hole pair is produced and separated by the force exerted by the internal field of the junction. Electrons and holes then flow

in opposite directions, thereby producing a photocurrent. Figure 4.2 shows the energy band of a p-n junction when a photon with energy greater than the bandgap is absorbed.

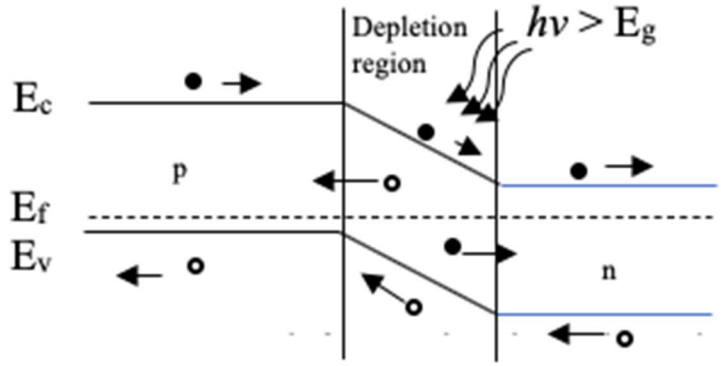

Figure 4.2 Curvature of the energy bands and mechanisms of photocurrent generation in a p-n junction [30]

Solid-state photodetectors are commonly made from silicon because of their response to a wide range of wavelengths. The wavelength of silicon detectors can be modulated easily by doping changes. Consequently, this silicon is the leading material in most industries and research. Furthermore, silicon-based devices are also used in high energy imaging. For example, many industries use it in X-ray imaging. However, detection of X-rays at high energies is not efficient using silicon, and often other materials or schemes such gallium arsenide (GaAs) and gallium nitride (GaN) are used. Figure 4.3 shows a plot demonstrating that the X-ray absorption decays with increasing photon energy, and thicker material is needed to detect the X-rays. However, because the thickness decreases the speed of detection, other materials are being researched to substitute for silicon photodetectors [20].

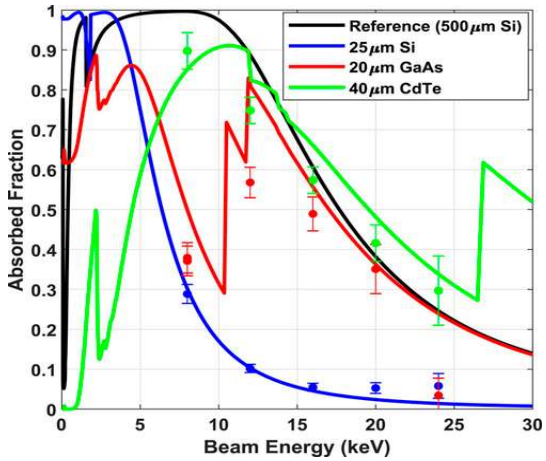

Figure 4.3 Measured detector quantum efficiency for three test detectors and a reference detector. The data points are the measured values from the study. The curves are predictions based on transmission through the detector layer and absorption in the dead layer. [20]

4.2 AVALANCHE PHOTODIODES

Avalanche photodiodes (APDs) are solid-state photodetectors that offer a broad combination of benefits unmatched among other undoped intrinsic semiconductor region between a p-type semiconductor and an n-type semiconductor (PIN) detectors, owing to their structure and inherent properties. APDs have better speed and sensitivity than PIN detectors, and, as compared with most photomultiplier tubes (PMTs), they have better quantum efficiency. Therefore, they are used in many high energy applications and are being actively researched.

APD structures offer many advantages over traditional PMT systems. They allow for lighter, simpler detector systems that can perform imaging in the U.V. operating region, which is solar blind. Ionizing radiation can be detected with a scintillating material and APD instead of a PMT. Shielding from electromagnetic ambient noise and high energy radiation tends to be easier for an APD than for a PMT, which sometimes requires thousands of kilograms of shielding

material, like lead. Normally, APD structures are built with GaAs, InP, and Si, among other materials, but Si is typically preferred.

APDs have many favorable qualities that distinguish it from other types of photodetectors. In contrast to regular PIN detectors, APDs provide inherent current gain. This gain provides a significant advantage in applications in which noise must be kept to a minimum, because the signal to noise ratio is improved before being augmented by an amplifier. A possible disadvantage is that in APDs, the reverse bias voltage applied is higher than that with regular detectors; however, as a result, the electron and hole pair are greatly accelerated by the intense electric field present. These high energy carriers collide with atoms, which are ionized, thereby producing more carriers. This process is known as impact ionization or avalanche multiplication. Therefore, a single photogenerated carrier pair can ultimately generate many more carriers, thus resulting in a very high current gain

An APD structure commonly consists of highly doped p + and n + regions on either side of a lightly doped and an almost intrinsic region in the middle. There is also an additional p-layer sandwiched between the n+ and p+ regions. When the structure is reverse biased, most of the voltage drop is observed across the n+p junction. The photons enter from the p+ side and are absorbed in the intrinsic region, where they generate electrons and holes. The holes drift back toward the p side. In a reverse bias junction, the width of the depletion region on either side of the junction is inversely proportional to the doping level. Therefore, in this structure, the depletion region extends to the p side, and with enough reverse bias, reaches through to the intrinsic region. After the electrons enter the high electric field region, they accelerate and cause avalanche multiplication through impact ionization. These secondary carriers are the main contributors to the overall APD current. Of note, in these devices, only electrons migrate toward the high field area

and initiate avalanche multiplication. This aspect is beneficial for noise purposes, because the noise performance of devices that rely on one primary carrier is better than that of devices relying on both carriers. Figure 4.4 shows the process of a carrier multiplication for a generic APD.

The current gain of an APD, denoted by M, is a function of the reverse bias voltage. As the reverse bias voltage approaches the breakdown voltage, V_{BR}, the gain begins to increase, and a linear relationship is observed between the applied voltage and current gain. An empirical description of this behavior can be given by the following formula:

$$M = \frac{1}{1-\left(\frac{V}{V_{BR}}\right)^n} \tag{3}$$

where V is the reverse bias voltage, and n is an empirical parameter that varies between 2 and 7. For long wavelength detectors based on InGaAs, typical breakdown voltages can range from 30 to 100 V, and gains of 10–30 are achievable. Gains of 100 and above can be achieved by silicon-based APDs, but the breakdown voltage is higher, and they cannot be used for long-wavelength applications.

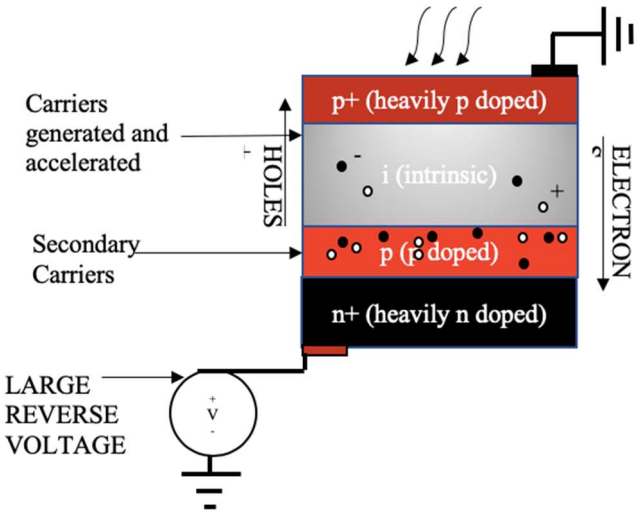

Figure 4.4 Representation of how carrier multiplication is produced on an APD

CHAPTER 5 RADIATION EFFECTS

5.1 NEUTRON DAMAGE MECHANISMS SILICON

The effects of fast neutrons on silicon devices are important for understanding the lifetime of a circuit or device in a harsh environment, such as in space, or inside a nuclear reactor or a fusion chamber. The effects result in electrical performance issues in single devices, thus affecting the entire electronic circuitry; this process is mainly due to the creation of crystal lattice defects, specifically Frenkel pairs. Some knock out atoms create a cascade of defects and consequently increase the damage in the lattice. Understanding the basics of how these defects are formed is important so that a good model can be simulated to predict the behavior of my transimpedance amplifier after a fluence, Φ (n/cm^2).

Vavilov, in the book "Effects of Radiation in Semiconductors," describes how fast neutron damage can be understood through a basic elastic scattering model [21]. Energy transfer from a flying neutron (fast neutron) varies, and if it is described with elastic collision theory, the maximum energy transfer can be calculated with equation (4):

$$E_{Amax} = \frac{4M_n M_A}{(M_n + M_A)^2} E_n \quad , \quad E_{Amin} = 0 \tag{4}$$

where M_n is the mass, and E_n is the kinetic energy of a neutron; M_A and E_A are the mass of the recoil atom and the recoil energy; E_{Amax} is the maximum energy transfer; and E_{Amin} is the minimum energy transfer. If neutron scattering is assumed to be isotropic, then all values of the recoil energy from 0 to E_{Amax} are equally probable, and the differential cross-section, dσ, for the energy transfer in the region of $E_A + dE_A$, is:

$$d\sigma = \frac{\sigma_t}{E_{Amax}} dE_A \tag{5}$$

where σ_T is the total neutron cross-section, which is assumed to be wholly due to elastic scattering. Importantly, the cross-section, σ(E), which is dependent on energy and is expressed in units of cm^2, is the probability that a neutron will interact with the atomic nuclei. The average energy transfer is assumed to be:

$$\overline{E_A} = \frac{1}{2} E_{Amax} \tag{6}$$

from a high energy neutron, higher than that of α particles and protons because the scattering process of neutrons has only non-ionization losses.

Furthermore, the damage that neutrons cause in silicon crystals is directly correlated with the number of interactions that they will have. A neutron with energy E_n will have a number of interactions or collisions $N_c = \sigma(E)v(E)N_m$, of the type characterized by σ(E), where v(E) is the neutron velocity, and N_m is the number density of the atom with which the neutron interacts. N_m is calculated as follows [4]:

$$\mathrm{N_m} = \frac{\rho \mathrm{N_0}}{\mathrm{A}} \tag{7}$$

In this equation, ρ is the density of the medium, A is the atomic or molecular weight, and N_0 is Avogadro's number. To calculate the number of interactions of neutrons with the medium, in my case silicon, N_c is multiplied by $n_0(E)$, which is the number of the density of incident neutrons per cm^3 per second d of energy E, as follows:

$$\mathrm{I_t} = \int \mathrm{n_0(E)\sigma(E)v(E)N_m t_0 dE} = \mathrm{N_m} \int \sigma(e)\varphi(E)\mathrm{dE} \tag{8}$$

I_t is the total number of interactions, $\varphi = n_0(E)v(e)t_0$ is the spectral fluence, and t_0 is the pulse of width t_0 seconds; in addition, φ is the number of neutrons per cm^2 with energy E during a pulse t_0, which are incident on and penetrating the medium (crystal). Fluence (n/cm^2), in contrast, is the total number of particles from all directions and all energies, and can be calculated as follows:

$$\Phi = \int \varphi(E)dE \tag{9}$$

Neutrons do not have any charge, and the main type of damage that they generate in electronic devices is displacement damage, in which high energy neutrons collide with a lattice atom, thus displacing them from their position within the crystal. This displacement creates a vacancy where the atoms were removed in interstitials where the atoms are now positioned. The pair of a vacancy and interstitial is commonly known as a Frenkel pair or Frenkel defect [4]. Furthermore, if the energy of the incident neutron is sufficiently high, it can impart sufficient energy to an atom to allow it to displace more atoms, and these displaced atoms (with high enough energy) can in turn displace even more atoms, thus creating defects in a cascading manner throughout the lattice structure.

From "The Effects of Radiation on Electronic Systems," [4] one obtains a relation of neutron damage to the lattice. The number of displaced atoms per cm^3, $N_{d,}$ is given by:

$$N_d = N \int_{E_{th}}^{E_{max}} dE \int_{E_d}^{E_{rmax}} N_s(E_r)\sigma(E, E_r)\varphi_n(E)dE_r \tag{10}$$

Where N is the number of atoms per cm^3, $\varphi_n(E)dE$ is the neutron spectral fluence in the energy increment dE (cm^{-2} eV), $\sigma_D(E,E_r)$ is the collision cross-section per recoil atom by which an incident neutron of energy E produces a recoil atom of energy E_r (cm^2), $N_s(E_r)$ is the number of displaced atoms per unit energy interval that result per recoil atom expending all its energy E_r, E_{th} is the threshold energy required by the incident neutron to dislodge an atom from its site in the lattice, E_d is the head-on (maximum) energy that can be transferred to a recoil atom by an incident neutron of energy E_{th}, E_{rmax} is the head-on (maximum) energy received by a recoil atom from an incident neutron of energy E, E_{max} is the maximum available incident neutron energy. However, this equation can be rewritten by defining neutron mean free path as $\lambda(E, E_r) = [N\sigma(E,E_r)]^{-1}$ which is

the probability a primary recoil atom of energy E_r is produces by an atom with energy E, and rewrite equation (11) as:

$$N_d = \int_{E_{th}}^{E_{max}} \varphi_n(E)dE \int_{E_d}^{E_{rmax}} \frac{N_s(E_r)dE_r}{\lambda(E, E_r)} \tag{11}$$

With $N_s(E_r)dE_r/\lambda(E,E_r)$ being the expected number of defects produced with energy E_r an in dE_r per incident neutron of energy per cm^3. Equation 12 can then be approximate by the product to single integrals as follow:

$$N_d = \int_{E_{th}}^{E_{max}} \varphi_n(E)dE \int_{E_d}^{E_{rmax}} \frac{N_s(E_r)dE_r}{\lambda} \tag{12}$$

this can be done because $\lambda(E,E_r)$ can be approximated by $\lambda = (N\sigma_D)^{-1}$ the neutron mean free path variation is low over incident neutron energies of concern. If the integrals are a factor, so neutron fluence is $\Phi_n = \int_{E_{th}}^{E_{max}} \varphi_n(E)dE$ and the mean number of primaries produces per primary recoil is $\bar{n}_s = \int_{E_d}^{E_{rmax}} N_s(E_r)dE_r$ or using Kinchin Pease model [22] for recoil atoms with energies greater than the displacement threshold energy, $\bar{n}_s = \frac{E_r}{2E_d}$. $\bar{n}_s$ can then be calculated with equation (13) assuming E_r is mean energy calculated from equation (5) and (6).

$$\bar{n}_s = \frac{E_n}{E_d} \frac{2M_n M_A}{(M_n + M_A)^2} \tag{13}$$

An equation asserting the total number of displaced atoms per cm^3 can be written as:

$$N_d \cong \Phi_n \cdot \frac{\bar{n}_s}{\lambda} \tag{14}$$

Where N_d is is the total number of displaced atoms for fluence of Φ_n, $\bar{n}_s$ are the primary knock out atoms (mean), and $\lambda = (N\sigma)^{-1}$ is the neutron mean free path for a material with number of atoms N and neutron cross section σ. For energies of interest, a λ is very large in comparison to chip and transistor dimensions, thus it is possible to consider homogeneity of damage throughout the chip,

and possible to calculate an approximate number of displaced atoms. If we consider that the threshold for the mean displacement energy is 20 eV, it is possible to perform an estimation for a range of energies. Two important energies to consider are the mean fission neutron energy of ~2 MeV and D-T fusion neutron energies of ~14 MeV. Electronics are used in these neutronic environments that have to survive. Therefore, it is possible to used equation 12 to calculate the number of atoms being displaced per cm^3. For fluence of $\Phi = 10^{15}$ n/cm^2, $\bar{n}_s \approx 500$ displaced atoms per primary knock out atom (mean), and $\lambda = (N\sigma)^{-1} = (5x10^{22})(4.8x10^{-24}) = 4$ cm, for N as the number of atoms of silicon per cm^3 and σ of 14 MeV . Then using equation 12, we obtain an approximate equivalent number of displaced atoms. Table 1 presents the number of displaced atoms per fluence of interest. These displacements provoked damage to devices, and if they are not annealed, they become permanent defects.

Table 1 Number of displaced atoms by 14 MeV neutron fluence

Fluence (n/cm^2)	N_d (Displaced atoms/cm^3)
$1x10^{11}$	$12.5x10^{12}$
$1x10^{14}$	$12.5x10^{15}$
$1x10^{15}$	$125x10^{15}$
$1x10^{16}$	$1.25x10^{18}$

5.2 NEUTRON DAMAGE IN MOSFETS

What makes CMOS (MOSFETS) an excellent candidate to be used on neutron radiation applications is the way they operate. MOSFETS are majority carrier devices; therefore, minority lifetime is no as relevant as in bipolar junction transistor (BJTs). Majority carriers are trap in inter-

bandgap levels created by atomic displacements reducing the number of available carriers, changing the device transconductance. Because the traps are created by atomic displacements, the damage is proportional to the neutron fluence and doping levels.

Increasing charge trapping through the introductions of defects such as vacancies, divacancies, and donor-vacancy complexes caused by neutrons explain the increase in resistivity on majority carrier devices. Messenger writes that these damaging effects capture electrons, reducing conductivity [4]. The rate at which each type of defect varies and depends on many variables, for example, neutron incident fluence, doping level, type doping atoms, temperature. Therefore, it is necessary to experiment to acquire an empirical equation to which can be used as guidance for the electronic designer.

Though the years, many scientists and engineers have developed equations to model the neutronic radiation effects on silicon devices. These researches have made similar equations to simplify and understand what is happening inside the crystal structure, which can directly affect the electrical properties of the devices. Most of these researches perform irradiation experiments to create a relation between incident neutrons and its effects, in mobility, resistivity, and number of carriers. Messenger wrote an equation for removal rate as follows [22]:

$$\frac{dn}{d\Phi} = -n_0(K_1 + K_{DV}) \tag{15}$$

Where K_1 is a constant obtained experimentally, and K_{DV} is the rate coefficient for donor-vacancy complexes. Curtis, Bass, and Germano found measured carrier removal rates varying from 1.5 to 3 and 1 to 4 carries/n-cm for p-type and n-type, respectively [23] [24]. While Buehler, through a collection of data, made an empirical equation for the removal of majority carriers as follows [5]:

$$-\left(\frac{dp}{d\Phi}\right)_{\lim\Phi\to 0} = p_0^{0.23}K_p \tag{16}$$

$$-\left(\frac{dn}{d\Phi}\right)_{\lim\Phi\to 0} = n_0^{0.23} K_n \tag{17}$$

Where (16) is for holes, and (17) is for electrons, $dp/d\Phi$ is the carrier removal rate, p_0, n_0 is the initial number of majority carriers, and K_p and K_n are the removal coefficient rates. These rates vary from 387 and 3300 for a reactor neutron spectrum. Therefore, based on these empirical equations that take into account type of doping, doping density, neutron energy, and neutron fluence, a design for a rad-hard transimpedance amplifier can be done.

Neutron irradiation Experiments on MOSFETs reveal that they are radiation hard. Messenger, Buehler deduce that mobility is not significantly changed and that the most important damage is carrier removal [4] [5]. Gillberg, et all, irradiation experiments on power MOSFETS, confirms these assumptions by demonstrating that none of the electrical characteristics changed significantly until fluence higher of 10^{15} n/cm^2 [25]. Figure 5.1 shows threshold voltage relatively stable until fluences larger than 10^{15} n/cm^2. Therefore, to simulate neutron effects on MOSFETS, this thesis will take into account only the removal of majority carriers.

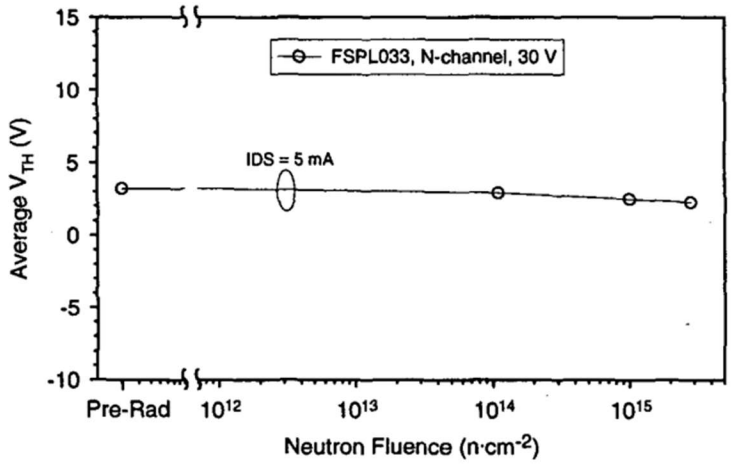

Figure 5.1 V_{th} response of tested devices from the FSP family [25].

5.3 NEUTRON DAMAGE IN BIPOLAR JUNCTION TRANSISTORS (BJTS) AMPLIFIERS

MOSFETS are majority carrier devices, making them inherently radiation hard, BJTs are minority carrier devices making them more susceptible to radiation damages [4]. Displacement damage, in addition to the creation of traps, creates recombination sites reducing minority carrier lifetimes. These changes, in turn, make the current gain deteriorate in proportion to fluence. Messenger demonstrates how an NPN transistor with common emitter voltage, V_{CE} = 2.0 V, decreases in current gain by incremental fluence levels. Figure 5.2 shows how current gain on 2N2222 diminishes as neutron fluence increases [26].

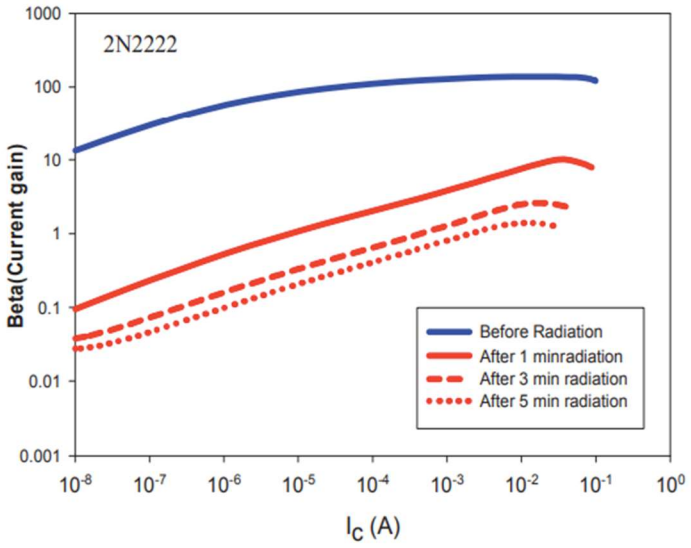

Figure 5.2 Plot of current gain (beta) versus collector current (Ic) at different irradiation time for Si NPN 2N2222 [26]

CHAPTER 6 TRANSIMPEDANCE AMPLIFIER

6.1 INTRODUCTION

Analog front end (AFE) devices are used as sensitive amplifiers for integrated circuits and sensors. AFE devices are hardware modules used as interface sensors or systems providing hardware modularity. Some examples are operational amplifiers, and in the case of this thesis, a transimpedance amplifier, which will be used to interface a silicon avalanche photodetector fabricated in ON Semiconductor's C5 process. The purpose of this system is to immediately amplify signals detected from the APD to minimize power loss in the communication process. In this chapter, an AFE TIA capable of transforming an ON C5 processed APD [27] current signal to a readable voltage driving a load of 1 pF will be introduced.

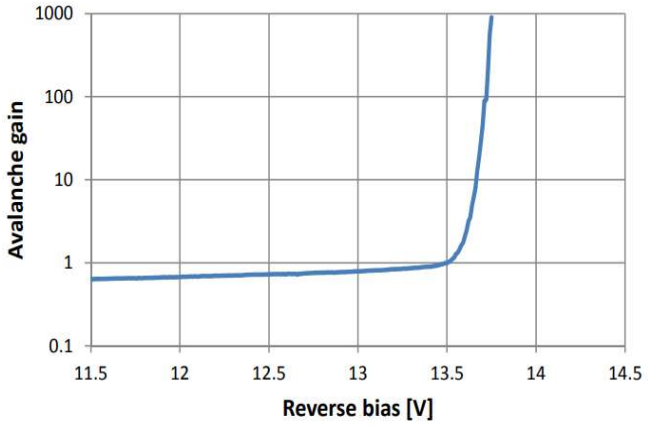

Figure 6.1 APD 1 gain by reverse voltage [27]

APDs have higher gain than regular photodiodes as a result of their structure, discusses in chapter 4. This higher gain makes them ideal for applications where high sensitivity and high

frequency is needed. Some of those applications are for radiation detection, LIDAR, and fiber optic telecommunication, among others. Therefore, if the APD will be used to detect scintillation light, the TIA needs to be able to amplify signals with a minimum frequency at least as fast as the scintillator scintillates.

TIA input current is the APD output current. Figure 6.2 shows the APD I-V characterization when it is both illuminated and when it is dark. It is seen that after 13.5 V, dark current becomes as high as light current. It can be seen that an APD gain of 1000 is obtained until a maximum reverse voltage of 13.75 V is used. Also, as seen in the graph, the current for an illuminated APD is $I_{LAPD}(13.75\ V) = 5\ \mu A$, and the dark current is $I_{dark}(13.75\ V) = 10\ nA$. These parameters were used in design of the TIA design in this thesis (move figure to follow the paragraph) .

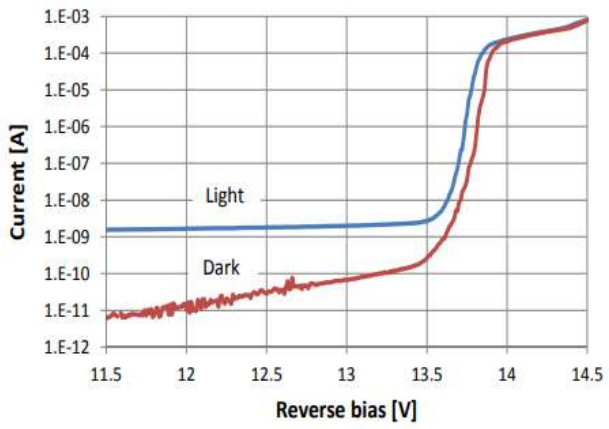

Figure 6.2 Current vs reverse bias for On C5 APD [27]

6.2 DESIGN APPROACH

For an AFE with a low number of transistors, low power consumption, low noise, and simplicity of design, the TIA with a feedback resistor was used in a differential amplifier on the as the first stage of the TIA. An advantage of using a TIA differential amplifier is its high bandwidth in comparison to other high impedance topologies. Also, differential amplifier has a higher dynamic range than that of a high input impedance amplifier. This is due to the use of negative feedback. However, disadvantages include stability issues and input-referred noise in comparison with other topologies.

The APD has higher gain than a regular photodetector, which is needed to convert small currents into usable voltages. Even so, the TIA will still require multiple amplifying stages. The amplification stages used for this TIA include a first stage with a transimpedance gain of 30K A/V. The output of the first stage is then amplified using a second stage voltage amplifier with a gain of 10 V/V. Finally, a buffer or amplifier with a gain of 1 is added, so the TIA can drive a smaller load; for example, 50 W. A diagram of this design is shown in Figure 6.3 and the gain calculation is given by equation (18). The first stage is shown in Figure 6.4.

$$A_{total} = A_{TIA} * A_{\frac{V}{V}} * A_{buffer} = 30k * 10 * 1 = 300k \quad (18)$$

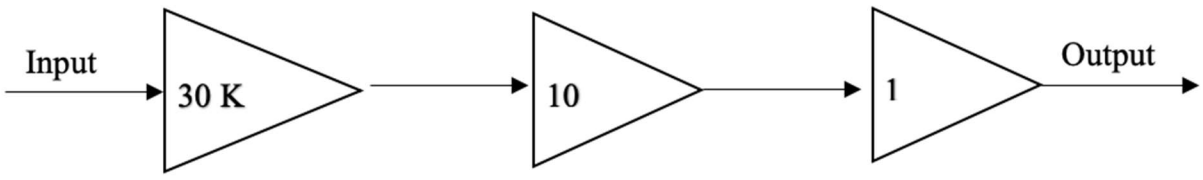

Figure 6.3 Three stage amplifiers consisting of a TIA with 30 kΩ, 10 V/V and a buffer

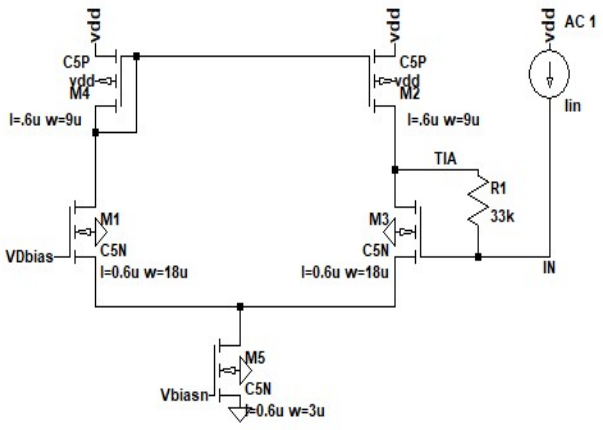

Figure 6.4 Differential amplifier in transimpedance topology. Parallel transistors were not used, for ease of design visualization. g_m and r_o were previously calculated, as shown in schematic file

It is well known that transconductance (g_m) and output resistance (r_o) are the main components to calculate gain in CMOS amplifiers. From a SPICE simulated model, these two components were obtained to perform calculations. Table 2 displays the simulated values obtained for two transistors in the TIA. Based on the simulated values, the TIA was designed with minimum length (L) and parallel transistors for larger width (W) to keep noise to the lowest, bandwidth the highest and consistent g_m and r_o. Moreover, by choosing this parameter, an I_D of ~55 µA was achieved allowing low power consumption. A biasing circuit, as shown in Figure 6.5, was used to obtain a reference current of ~55 µA. This biasing circuit does not perform as well as a beta multiplier for power supply changes or temperature changes. However, it provides correct overdrive voltage to obtain to bias the amplifiers and obtain the designed gain and bandwidth in this project.

Table 2 D.C. characteristics of biasing circuit

Name:	M2	M3
Model:	C5P	C5N
$\mathbf{I_d}$	-31.6 µA	31.6 µA
$\mathbf{V_{gs}}$	-1.15 V	1.01 V
$\mathbf{V_{ds}}$	-2.42 V	1.01 V
$\mathbf{V_{bs}}$	0.00 V	-1.56 V
$\mathbf{V_{th}}$	-882 mV	863 mV
$\mathbf{V_{dsat}}$	-244 mV	124 mV
$\mathbf{g_m}$	208 $\mu\Omega^{-1}$	551 $m\Omega^{-1}$
$\mathbf{g_{ds}}$	4.67 $\mu\Omega^{-1}$	9.56 $\mu\Omega^{-1}$
$\mathbf{g_{mb}}$	50.6 $\mu\Omega^{-1}$	56.9 $\mu\Omega^{-1}$
$\mathbf{C_{bd}}$	0.00 F	0.00 F
$\mathbf{C_{bs}}$	0.00 F	0.00 F
$\mathbf{C_{gsov}}$	2.45 fF	3.50 fF
$\mathbf{C_{gdov}}$	2.45 fF	3.50 fF
$\mathbf{C_{gbov}}$	0.489 fF	0.528 fF

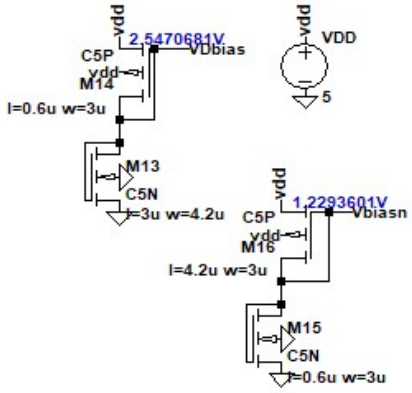

Figure 6.5 Biasing circuit for current sources, displaying bias voltage for PMOS (2.55 v) and NMOS (1.23 v)

From the schematic seen in Figure 6.4. It is possible to evaluate the output by calculating the gain as [28]:

$$A_{CL} = \frac{v_2}{i_s} = \frac{A_{OL}}{1 + A_{OL}\beta} = -\frac{gm_3\left(ro_3 \| ro_2 \| R_1\right)R_1}{\left(1 + gm_3\left(ro_3 \| ro_2 \| R_1\right)R_1\left(\frac{1}{R1}\right)\right.} = 33\,\mathrm{k} \qquad (19)$$

Where R is a resistor value; therefore, the expected closed-loop value is A_{CL} = 30 k; however, a gain of $A_{CL} \approx 33$ kΩ was calculated from the simulated g_m and r_o. Thus, the open-loop gain can be calculated by equation (20), which results in a 408 kA/V gain. Using the same values, the cut-off frequency for open-loop gain is calculated in (21) to be 3 GHz. A plot of the TIA frequency response is shown in Figure 6.6. It shows a cut-off frequency near 3 times lower than calculated but with the expected gain of ~90 dB. The first stage has a bandwidth greater than the required 167 MHz from chapter 2 and a gain of 89.5 dB A/V, ~30 K A/V. Therefore, the TIA has all the necessary qualities to be used as the first stage of the amplifier.

$$A_{OL} = g_{m3}\left(ro_3 \| |ro_2| \| R_1\right)R_1 \approx 408\ \text{k}\Omega \tag{20}$$

$$f_{3dB} = \frac{g_{m3}}{2\pi(C_{gs}+C_{dg})} \approx 3\ \text{GHz} \tag{21}$$

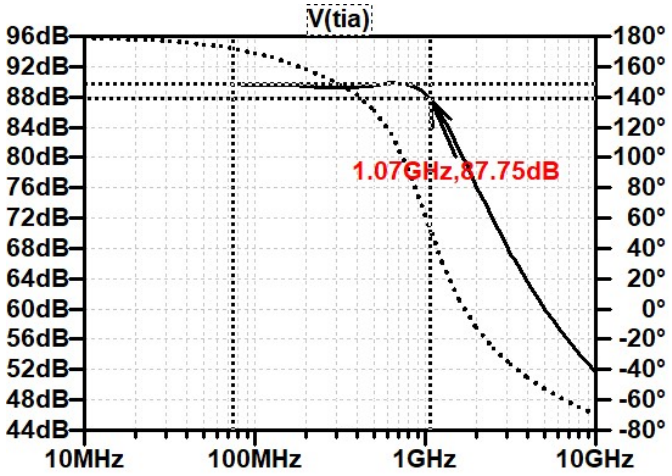

Figure 6.6 Open loop gain cut-off frequency f3 dB is approximately 1.18 GHz

For the second stage, a simple common-source amplifier for a voltage to voltage gain of 10 V/V was designed. Nevertheless, when implemented, it was not adequate for high bandwidth.

Therefore, a second topology was designed consisting of a second differential amplifier with resistor load was investigated. However, the gain provided by this new amplifier design was not satisfactory. Lastly, a differential amplifier with active load was considered. This design met the specifications and worked well. Moreover, the addition of the second differential amplifier cancels or reduces, the common-mode noise produced on the output of the first-stage amplifier. Therefore, a second differential amplifier, as shown in Figure 6.7 Transimpedance amplifier with 30 k ohms of gain, was used with parameters displayed in Table 3. Its gain is calculated in equation (22). Figure 6.8 shows simulation results of the second stage amplifier to an expected gain of ~15 V/V.

$$A_{OL} = g_{m10}(r_{o6} || r_{o10}) \approx 15 \frac{V}{V} \tag{22}$$

$$f_{3dBsecondstage} \approx \frac{g_{m3}}{C_L} \approx 550 \text{ MHz} \quad \text{with } C_L = 1\text{pF} \tag{23}$$

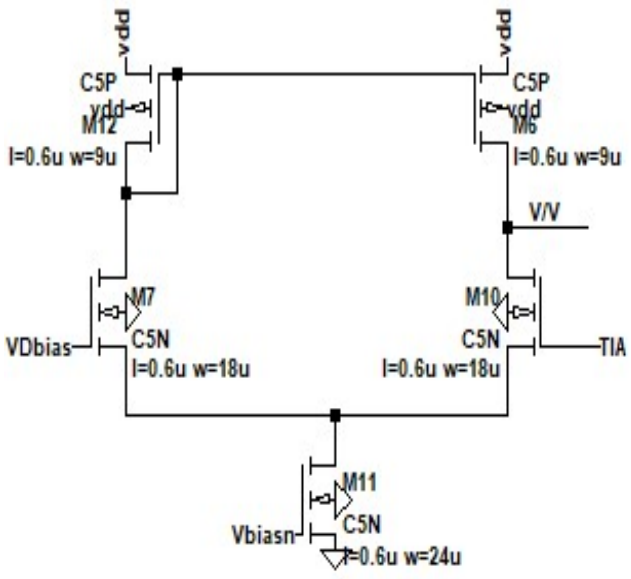

Figure 6.7 Transimpedance amplifier with 30 k ohms of gain

Table 3 Main transistor characteristics for second stage gain

Name:	M6	M10
Model:	C5P	C5N
I_d	-424 µA	4.24 µA
V_{gs}	-2.19 V	1.33 V
V_{ds}	-2.77 V	9.83 V
V_{bs}	0.00 V	-1.25 V
V_{th}	-880 mV	827 mV
V_{dsat}	-886 mV	353 mV
g_m	486 $\mu\Omega^{-1}$	138 $m\Omega^{-1}$
g_{ds}	26.3 $\mu\Omega^{-1}$	64.1 $\mu\Omega^{-1}$
g_{mb}	112 $\mu\Omega^{-1}$	163 $\mu\Omega^{-1}$
C_{bd}	0.00 F	0.00 F
C_{bs}	0.00 F	0.00 F
C_{gsov}	2.45 fF	3.50 fF
C_{gdov}	2.45 fF	3.50 fF
C_{gbov}	0.489 fF	0.528 fF

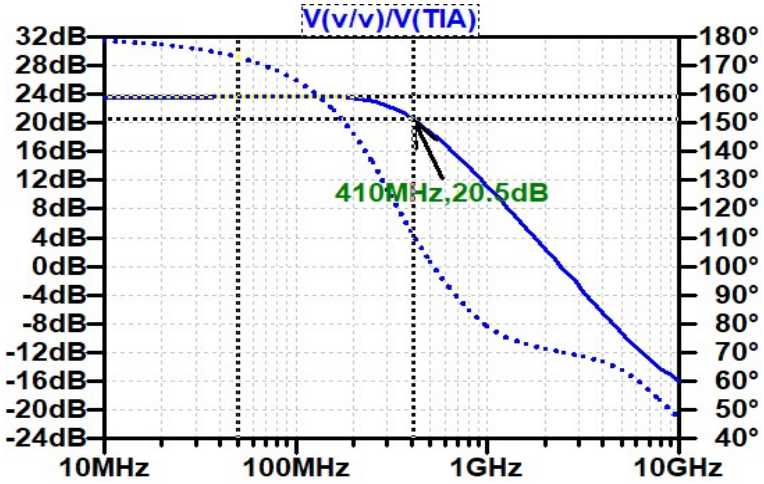

Figure 6.8 Simulation results of the second stage amplifier, showing ~24 dB, which is ~15 V/V

Since the circuit will be driving a capacitor load or perhaps a resistance, a higher output current, that is, lower output resistance was needed at the output of the two-stage amplifier. So a third-stage, a source follower, with a gain near 1 V/V, was used to increase the amplifiers outputted drive current capability. This addition also helped to input the slew rate. A schematic

of the complete amplifier with the three stages is shown in Figure 6.9. The frequency response is shown in Figure 6.10.

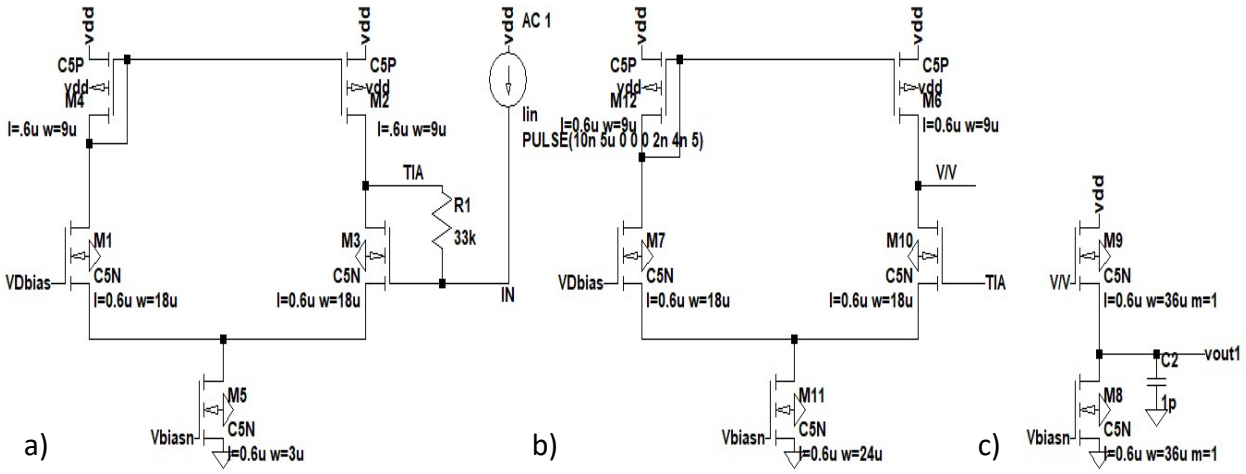

Figure 6.9 Transimpedance amplifier (a), output of TIA is labeled (TIA) and is connected to the (b) second stage on transistor M10. The output of the second stage is then connected to the output buffer (c).

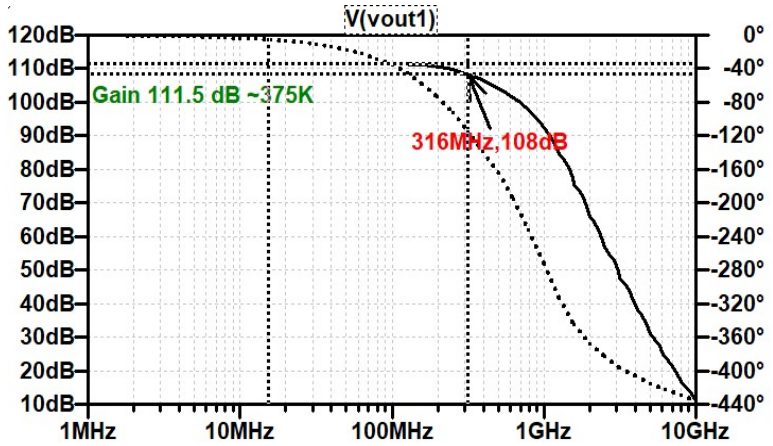

Figure 6.10 shows that the AFE TIA amplifier has a gain larger than ~375 k and a cutoff frequency at ~316 MHz, which is larger than the 167 MHz required.

6.3 OUTPUT SWING

The output voltage swing is used to determine how much current the amplifier can accept to keep the operation and linear for a given TIA gain. Based on the amplifier design gain of about 450 K A/V, it is possible to determine the input current range from an APD. The current input range is obtained by establishing an output range (in this case, 1.5 – 2 V) and solving equation (24). Because the output buffer will not be ideal, there is an acceptable error of up to 15% that adequately provides an output swing of less than 2 V.

$$\frac{V_{outmin}}{Gain} = I_{inmin} \leq I_{in} \leq I_{inmax} = \frac{V_{outmax}}{Gain} \tag{24}$$

$$\frac{1.5\ V}{450\ k\Omega} = 3.3\ \mu A \leq I_{in}\ \leq 4.4\ \mu A = \frac{2\ V}{450\ k\Omega} \tag{25}$$

Understanding that the voltage in the buffer will swing around 1.5 – 2 V, it is possible also to assume the second stage will swing around same voltage range, while the first will swing on a lower magnitude. Output swing calculations for the 2nd stage result in a range greater than 2 V greater as shown in equation (26); however, because the output buffer has a gain less than 1, the swing has an adequate range. Equation (26) and (27) demonstrates how to calculate the output voltage swing for the second stage and output buffer, respectively. The simulation results are shown in Figure 6.11. Hence, if 5 μA is assumed to be the maximum current input, the transimpedance amplifier will then provide an output voltage swing range of 1.7 V, which is in the range of the planned 1.5–2 V output swing range.

$$V_{2ndstageswing} = V_{vdd} - 2V_{DSsat} - V_{SDsat} = 5 - 2 \times .0.561 - 1.27 = 2.61\ V \tag{26}$$

Output swing for buffer below:

$$V_{bufferswing} = V_{vdd} - 2V_{DSsat} = 5 - 2 \times .0.561 = 3.88\ V \tag{27}$$

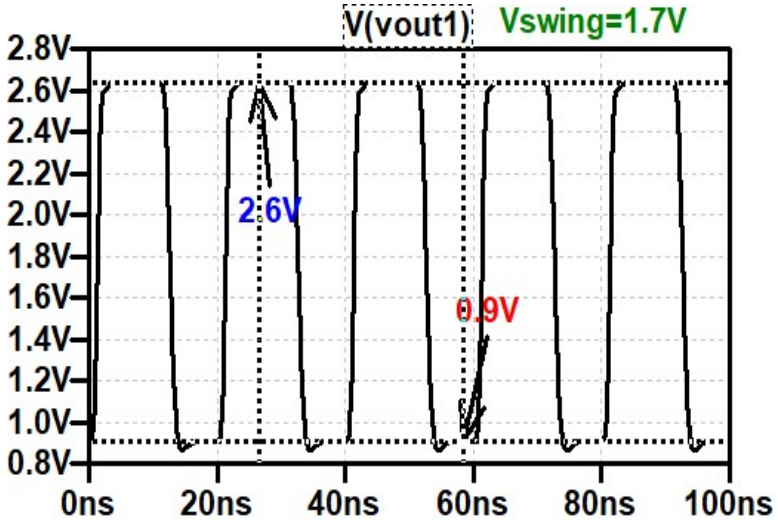

Figure 6.11 Output swing with a maximum current of 5 µA with a input frequency of ~50 MHz. Voltage output swing range is 1.7 V.

6.4 NOISE PERFORMANCE

Noise is a crucial consideration for amplifier design, and MOSFETs are advantageous in this area. MOSFETs are inherently less noisy than their BJT counterpart for the present design in an environment with high radiation. Even more, circuits made with MOSFETS can be optimized to reduce their noise. For example, by choosing minimum transistor length and using a differential amplifier as it was designed in the thesis, Table 2 shows the circuit input-referred noise performance, without a source integration capacitor. The proposed first stage amplifier has an input-referred noise lower than 850 fA/Hz$^{1/2}$ at the f_{3dB} = 250 MHz.

On the other hand, Figure 6.12 shows an integrator capacitor in parallel with the APD model (current source). The power spectral noise increases as capacitor values increases. This deterioration can be seen in

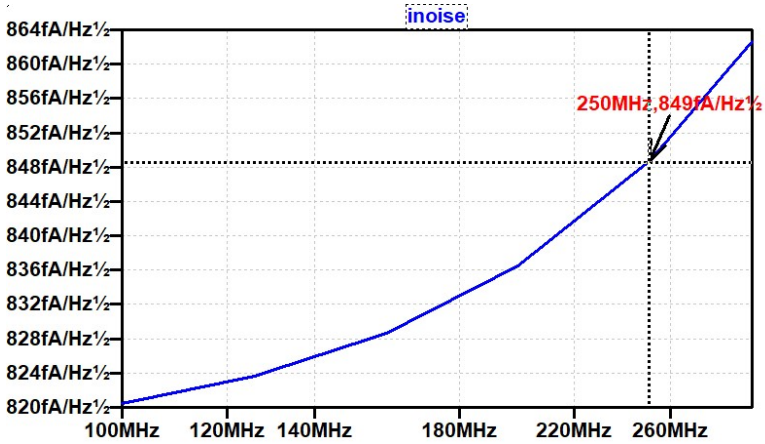

Figure 6.12 Amplifier input referred noise spectral density without integrator capacitor at the input. RMS noise was 11 nA/Hz1/2 integrated from 100 – 300 MHz.

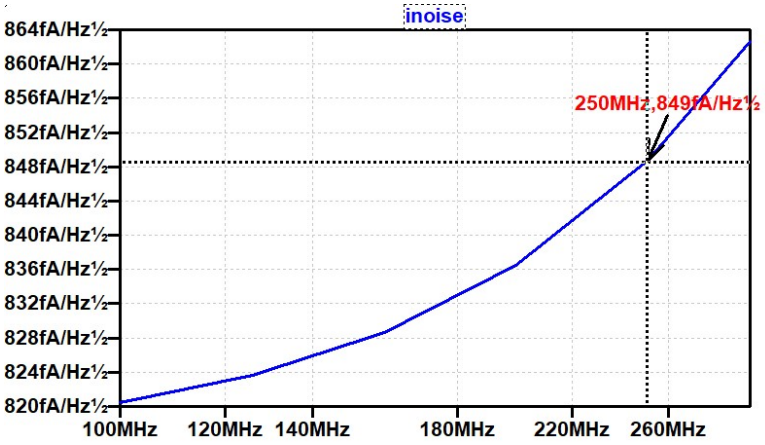

Figure 6.12 Amplifier input referred noise spectral density without integrator capacitor at the input. RMS noise was 11 nA/Hz1/2 integrated from 100 – 300 MHz.

Table 4, which displays capacitor values, and input-referred noise at f_{inoise} = 250 MHz.

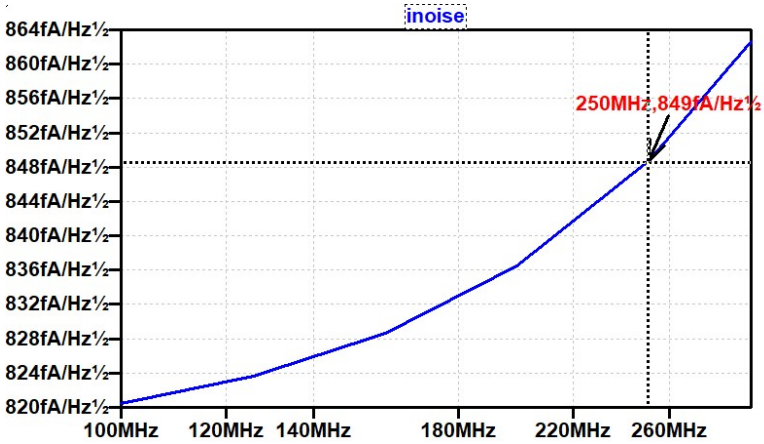

Figure 6.12 Amplifier input referred noise spectral density without integrator capacitor at the input. RMS noise was 11 nA/Hz1/2 integrated from 100 – 300 MHz.

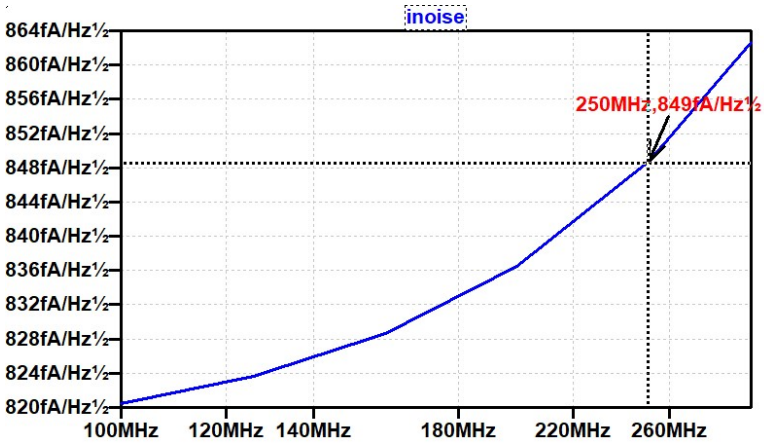

Figure 6.12 Amplifier input referred noise spectral density without integrator capacitor at the input. RMS noise was 11 nA/Hz1/2 integrated from 100 – 300 MHz.

Table 4 Capacitor and input-referred noise relation

Input capacitor (F)	50	100	250	500
Input referred noise (pA/Hz$^{1/2}$)	1.35	2.05	4.60	8.98

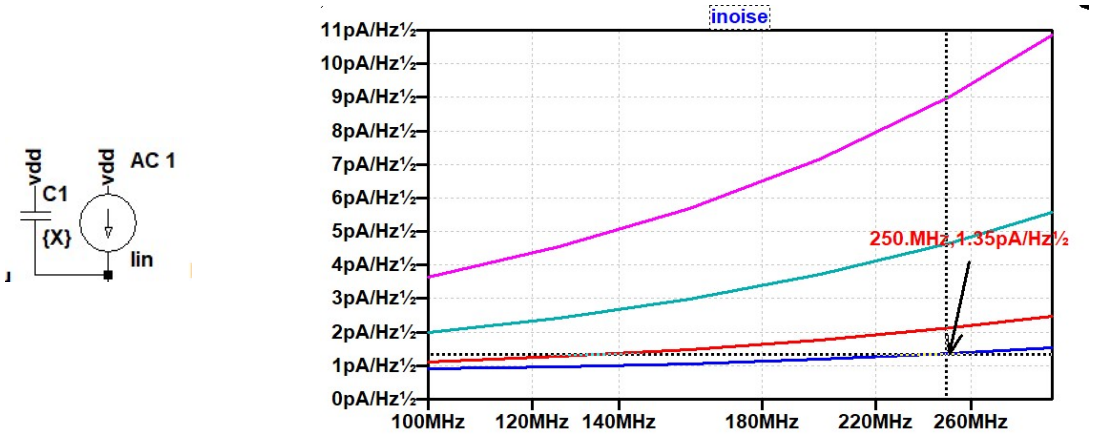

Figure 6.12 Power spectral noise for different capacitor values (right) and schematic of how the capacitor was connected (left)

6.5 SETTLING TIME AND SLEW RATE

Settling time and slew rate are important parameters of the TIA, and needs to be taken into account, especially when the input signal is stepped. Settling time is the time the output takes to settle into the final value. While slew rate (S.R.)is the change of voltage or current per time. The higher the slew rate the larger and/or faster the change of voltage or current. The TIA designed in this thesis has a S.R. > 100 mV/ns. The slew-rate may be determined for the present design using:

$$\text{Slew rate} = \frac{\Delta V_{out}}{\Delta \text{Time}} = \frac{V_{out90\%} - V_{out10\%}}{t_{90\%} - t_{10\%}} = \frac{1.7 \times .9 - 1.7 \times .1}{\Delta t} = \frac{1.36\ \text{V}}{\Delta t} > \frac{100\ \text{V}}{\mu\text{s}} \qquad (28)$$

Where the change of time is:

$$\Delta t = 13.6\ \text{ns} \qquad (29)$$

Output current is calculated from expected reference current as:

$$I_{outE} = I_{ref} * \frac{W_{m8}}{W_{m5}} = 55\ \mu\text{A} * 11 = 605\ \mu\text{A} \qquad (30)$$

where I_{ref} = 55 µA, W is the transistor width. This value, in turn, is used to calculate slew rate as:

$$\frac{dv}{dt} = \frac{i}{C} = \frac{605\ \mu\text{A}}{1\ \text{pF}} = 6.05 \times 10^8 \frac{\text{V}}{\text{s}} = 605 \frac{\text{mV}}{\text{ns}} \qquad (31)$$

However, simulation values demonstrate output current is I_{outS} = 1.23 mA, which is almost double from I_{outE}, giving a slew rate:

$$\frac{dv}{dt} = \frac{i}{C} = \frac{1.23\ mA}{1\ pF} = 1.23\ \times 10^{9}\frac{V}{s} = 1.23\frac{V}{ns} \tag{32}$$

A simulated plot demonstrates the amplifier slew rate in Figure 6.13. It shows S.R = 1.08 V/ns which is almost twice as better than expected using equation (31), but smaller than in equation (32).

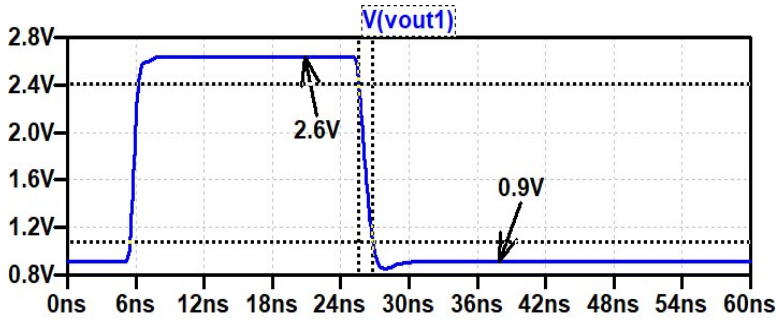

Figure 6.13 Slew rate shows a 1.08 V/ns

After the slew rate is obtained, settling time can be determined using simulations. Again, the settling time is the time from a signal takes to reach its final value. Figure 6.14 shows high to low settling time without any load present, nor interface capacitor. It was found that the settling time is t_{set} = 3.1 ns. In addition, an interface capacitor can be included as an APD signal integrator. Figure 6.15 shows settling time of the TIA for various capacitor values, and it clearly shows that any interface capacitance greater than 1 pF will have a large effect on the transmitted signal.

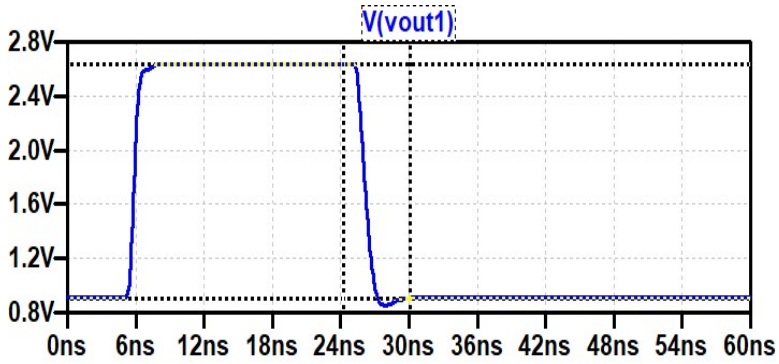

Figure 6.14 Settling time of 3.1 ns without load

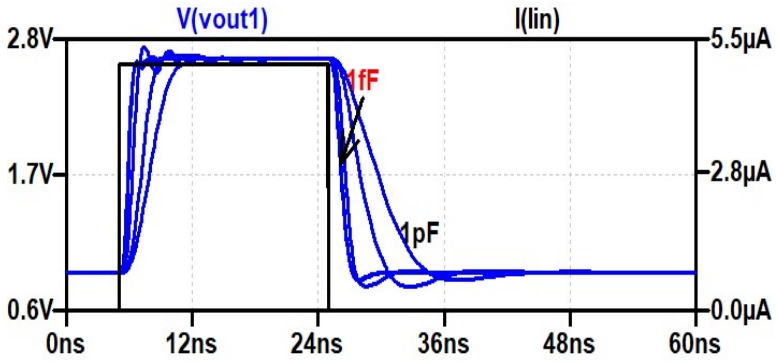

Figure 6.15 Settling time with different APT-AFE interface load capacitance (1 fF, 10 fF, 100fF, 1pF)

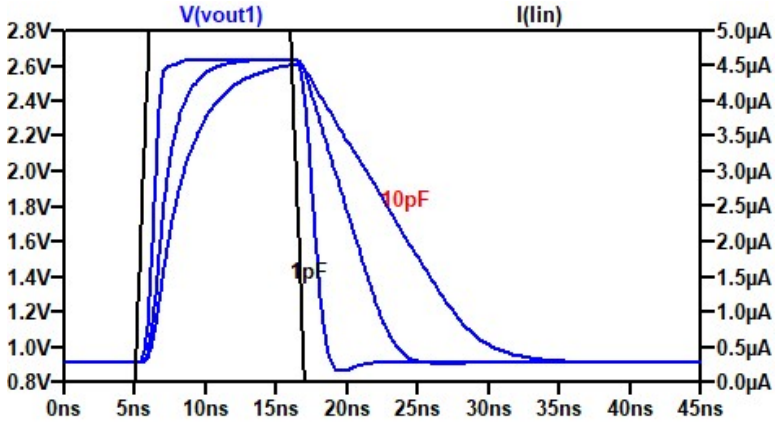

Figure 6.16 Different load capacitance simulation (capacitances are 1 pF, 5 pF and 10 pF)

Finally, plots on how the settling time changes by load capacitance are shown in Figure 6.16. It is clearly shown that after 10 pF the settling time is too large, but load values of 5pF, or less, are drivable by the TIA; however, by changing load capacitance, the frequency response also changes. Figure 6.17 shows how the cut-off frequencies are reduced by increasing capacitance. Table 5 is a summary of the capacitor load effects on the slew rate, settling time, and cut-off frequency of the amplifier.

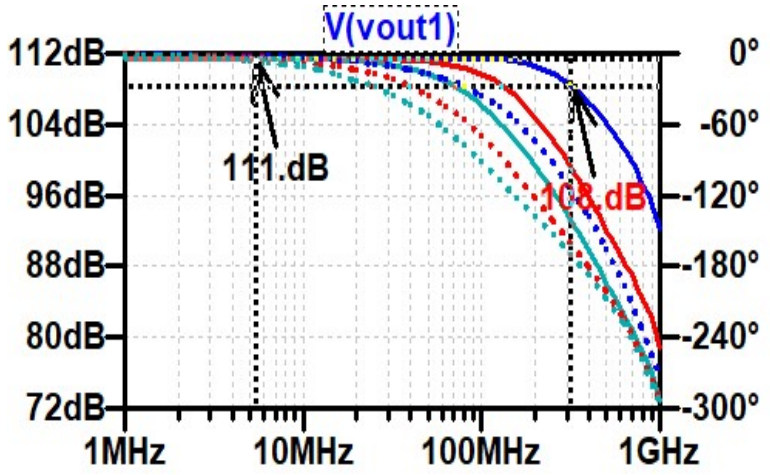

Figure 6.17 A capacitor greater than 10 pF produces a large distortion in the circuit by decreasing the slew rate. Small signal AC analysis.

Table 5 Summary of the capacitor load effects on the slew rate, settling time and cut-off frequency of the amplifier

Capacitor (F)	**1p**	**5p**	**10p**
Slew rate falling (mV/nm)	1,087	210	108
Slew rate rising (mV/nm)	1,802	547	286
Settling time falling (ns)	5.02	9.42	19.85
Settling time rising (ns)	3.27	7.88	14.85
3 dB frequency (MHz)	330	110	108

6.6 POWER CONSUMPTION

CMOS power saving technology is a one of the greatest advantages of using CM, and this can be seen in the designed TIA. Power consumption of the TIA can be easily calculated by adding the current sources of the three amplifying stages. A practical way to perform the addition is to add the multiples from the reference current as in equation (33):

$$I_{TIA} = I_{ref} + 11I_{ref} + 8I_{ref} + 3I_{ref} = 55 * 23 * 10^{-6} = 1.27\ mA \quad (33)$$

Simulated current value was discovered to be I_{TIA} = 2.32 mA, which is still lower than the maximum expected consumption of 5 mA.

The power of the TIA can then be calculated easily by multiplying the voltage source, V_{DD} by the TIA current, I_{TIA} as follows:

$$TIA_{power} = V_{DD} * I_{TIA} = (2.32\ mA)(5\ V) = 11.6\ mW \quad (34)$$

6.7 RESISTOR IMPACT TO AFE PERFORMANCE

An APD can be biased in many ways, and one of those ways is to connect the anode to ground via a resistor. However, by doing so it will reduce the amount of amplified current if its resistance is low, and at the same time it will increase noise by approximate N_R = 4ktR*A is the noise resistor, k is Boltzmann constant, R is the resistor value and A is amplifier gain. The input resistance of the TIA should be much, much, smaller than the biasing resistor so that all of the APD current goes into the input of the TIA and little goes through the resistor. With this method, the input resistance, R_{bias}, can be calculated by equation (33), which shows that a bias resistor would be, as a rule of thumb, at least 10 to 100 times larger than R_{input}. D.C. gain as function of input current with resistors (42 MΩ, 500 kΩ and 420 kΩ) is shown in Figure 6.18 demonstrating larger input current is needed for lower biasing resistors. Whilst, Figure 6.19 shows the frequency response with constant input current and variable resistor values (42 MΩ, 500 kΩ and 420 kΩ). In

these simulations, the interface and load capacitors were omitted. Therefore, by analyzing frequency response and gain vs I_{in} plots, a resistor of 42 MΩ will be the most adequate to bias the APD. However, choosing such large resistor will introduce larger noise. Figure 6.20 demonstrates how the input inferred noise increases largely by using a 42 MΩ resistor. Hence, depending on the application and the noise surrounding the circuit a lower resistor might be chose.

$$R_{input} = R_{feedback} \approx 30k \quad \text{therefore } R_{bias} > 300k \tag{35}$$

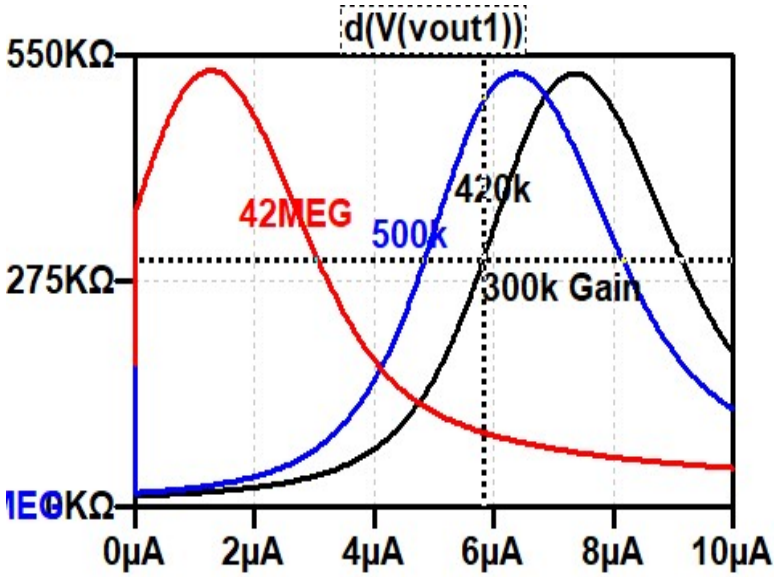

Figure 6.18 Amplifier gain by grounding APD through a variable resistor. It shows the DC gain with the horizontal line showing where the 300k gain. (Resitstors 42 MΩ - red, 500 kΩ - blue and 420 kΩ -black)

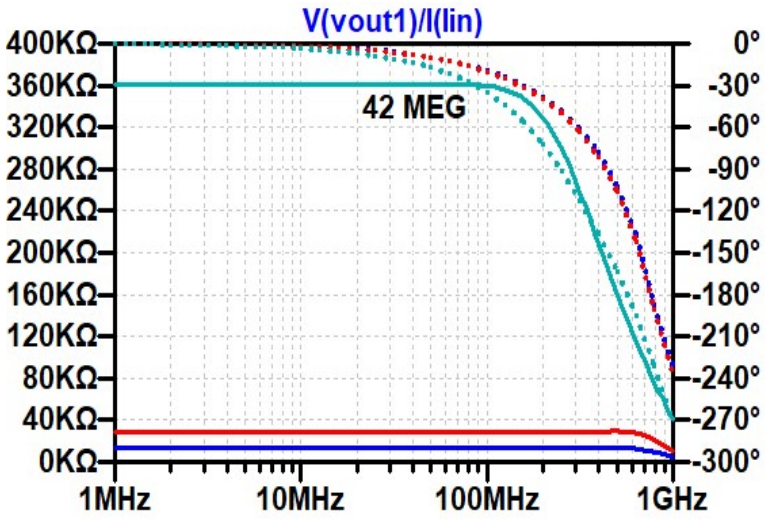

Figure 6.19 Amplifier gain by grounding APD through a variable resistor. It shows the frequency response to be ~360k gain

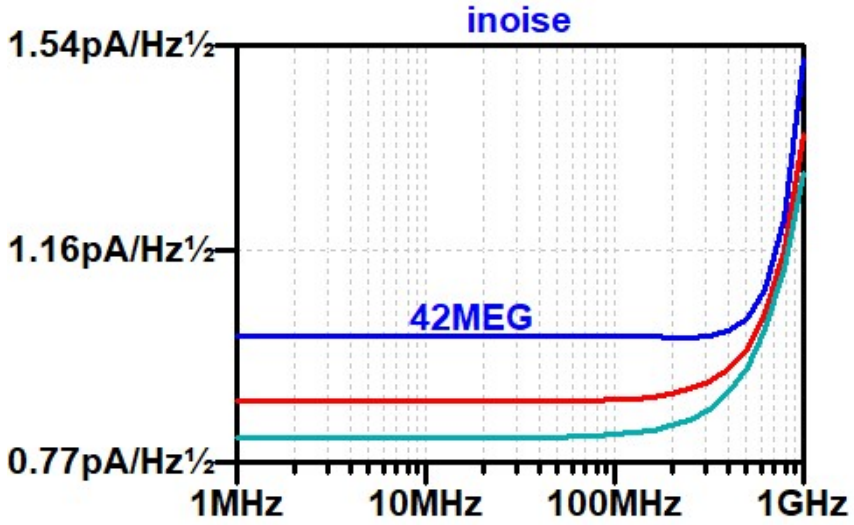

Figure 6.20 Power spectral density for input referred noise based on APD bias resistor, noise gets higher as resistor value increases, but stays under the maximum 5pA/Hz1/2

6.8 TEMPERATURE AND VOLTAGE SOURCE CHANGES

High magnitude temperature changes can change the operation of the TIA. Since, the amplifier does not have a beta multiplier temperature and VDD changes might become a concern. However, a simulating circuit performance under various temperature presents no concerns. As shown in Figure 6.21 Changes in the output voltage by temperature changes 10, 20, 27, 30, 40 and 100 degrees Celsius, with sweeping input current changes in output voltage from 10 to 100 °C are not significant. Also, variations in voltage source (VDD) of about ±200mV does not cause significant changes in the output voltage as shown in Figure 6.22 Changes in output voltage by step changes 4.8 V, 5V and 5.2 V while sweeping Input current from 0 to 5uA One possible explanation is might of the high overdrive voltage use in amplifier current sources and the inherent property of the differential amplifiers. Therefore, the TIA is expected to work as expected under temperatures of interest and hold its operation throughout voltage source variation of less than 5%.

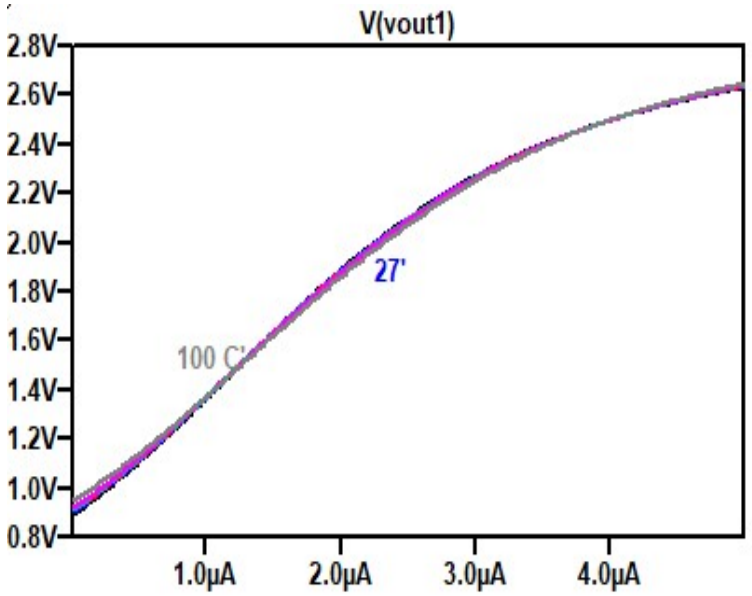

Figure 6.21 Changes in the output voltage by temperature changes 10, 20, 27, 30, 40 and 100 degrees Celsius, with sweeping input current

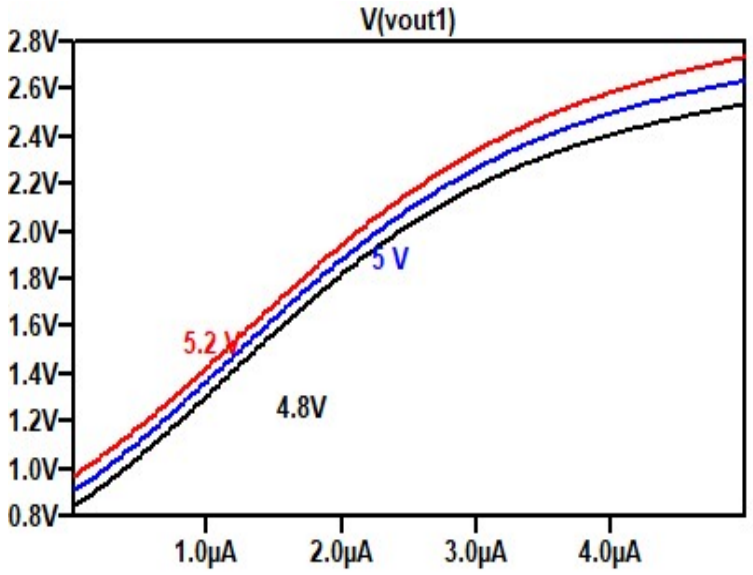

Figure 6.22 Changes in output voltage by step changes 4.8 V, 5V and 5.2 V while sweeping Input current from 0 to 5uA

6.9 NEUTRON EFFECTS

Neutron effects on CMOS technology were discussed back in section 5.2. It was stated back in this section that the main neutron defects produced are displacement damage that causes vacancies and interstitials in the SiO_2, which become carrier traps. These traps then remove carriers proportionally to the amount of neutron damage degrading the MOSFET devices; however, because MOSFET devices are majority carriers, they are capable of sustaining large neutron fluences. After a significant number of majority carries are removed transconductance and output resistance become affected. Since these two parameters are the main components for the TIA gain, variations in their values will cause gain change.

Damages in MOSFETS by neutron depends on a lot of variables that makes modeling a hard task. Changes in type and quantity of a silicon dopants will create a different rate of vacancies, divacancies, donor-vacancies and other complexes changing the carrier removal rate. Therefore, as discussed in chapter 5, an empirical model can be used; however, there are many empirical

models in the literature. So, in order to simulate neutron damage in the TIA a model with the most accumulated data was selected. Buehleer model describes a removal rate for reactor neutrons (fast neutron) for different doping levels [5]. Buehleer removal rate consist in equations (36) and (37) for electrons and holes respectively:

$$\frac{dp}{d\Phi_{\lim\Phi\to 0}} = \frac{p_0^{0.23}}{K_p} \tag{36}$$

$$\frac{dn}{d\Phi_{\lim\Phi\to 0}} = \frac{{n_0}^{0.23}}{K_n} \tag{37}$$

where p are holes, n are electrons, Φ is neutron fluence, n_0 and p_0 are the initial doping levels of electron and holes respectively, K_n and K_p are n and p type coefficients. The coefficients that were used are K_p= 387 and K_n= 444, which are assumed to be valid for doping levels 10^{17}, which the C5 process has. Then, using these values in equations (38) and (39) the carrier removal rates can be determined as:

$$-\frac{dp}{d\Phi_{\lim\Phi\to 0}} = \frac{p_0^{0.23}}{K_p} = \frac{(10^{17})^{0.23}}{387} = 21 \tag{38}$$

$$-\frac{dn}{d\Phi_{\lim\Phi\to 0}} = \frac{{n_0}^{0.23}}{K_n} = \frac{(10^{17})^{0.23}}{444} = 18.3 \approx 18 \tag{39}$$

After obtaining the carrier removal rates, equation (40) and (41) is used to calculate the number of new of carriers after irradiation.

$$n = n_0 - \frac{dn}{d\Phi}\Phi = 10^{17} - 18\,(10^{15}) = \ 82\text{x}10^{15} \tag{40}$$

$$p = p_0 - \frac{dp}{d\Phi}\Phi = 10^{17} - 21\,(10^{15}) = \ 79\text{x}10^{15} \tag{41}$$

It can be seen that even after a neutron fluence of 10^{15} n/cm^2 the majority carriers are not even cut in two. This is why MOSFET transistors are well suited for neutron radiation applications for

fluences of up to 10^{15} n/cm^2. In addition, MOSFETs made with ON C5 Process have an extra advantage because their doping levels are in the range of 10^{17} carriers/cm^3.

In order to simulate neutron damages, carrier density was diminished accordingly to equation (40) and (41). It is important to note that changes in mobility and threshold voltage were not taken into account, because they are not significant for fluences lower than 10^{15} n/cm^2 [5] [25] [4]. Table 6 displays values of carrier density for various fluences. In Figure 6.23 TIA demonstrates gain for 0 neutron fluence, Figure 6.24 for 10^{14} n/cm^2, Figure 6.25 for 10^{15} n/cm^2, and Figure 6.26 for $5x10^{15}$ n/cm^2. It is visible that TIA gain does suffer damage after $5x10^{15}$ neutron/cm^2. For fluences greater than $5x10^{15}$ n/cm^2 another model should be used. Messenger proposed models with a more fundamental approach that can be used for higher fluences than $5x10^{15}$ n/cm^2.

Table 6 Carrier density after device is irradiated with fast neutron fluence and its respective gain.

Fluence (n/cm^2)	hole density (carr/cm^3)	Electron density (carr/cm^3)	TIA Gain (dB A/V)
0	$1.17x10^{17}$	$1.17x10^{17}$	110
10^{14}	$115x10^{15}$	$115x10^{15}$	110
10^{15}	$96x10^{15}$	$99x10^{15}$	107
$5x10^{15}$	$12x10^{15}$	$27x10^{15}$	96

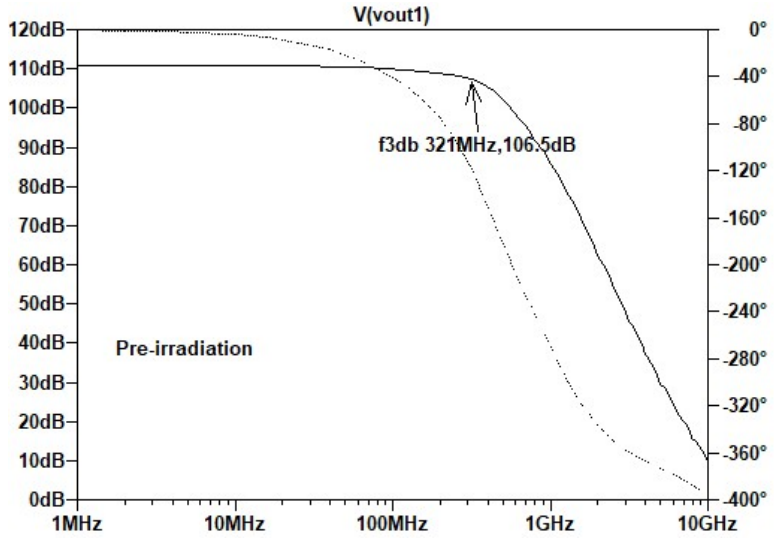

Figure 6.23 TIA gain before neutron irradiation gain is 110 dB

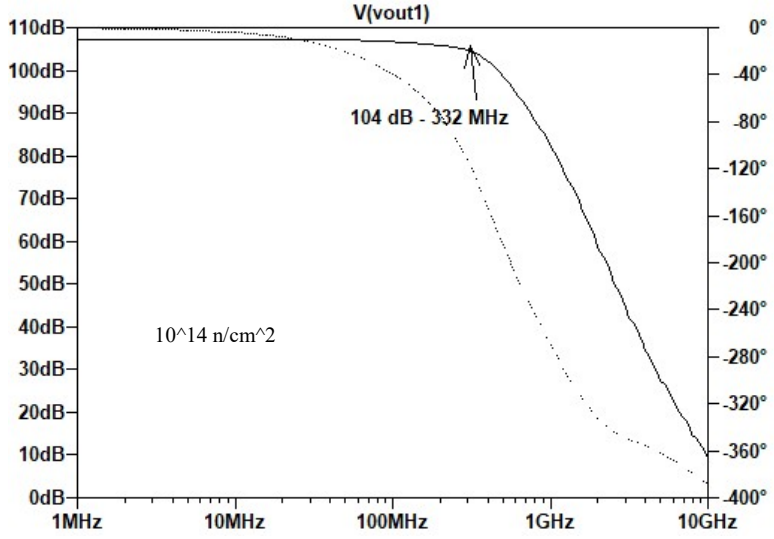

Figure 6.24 TIA irradiated by 10^{14} n/cm^2, gain remained the same

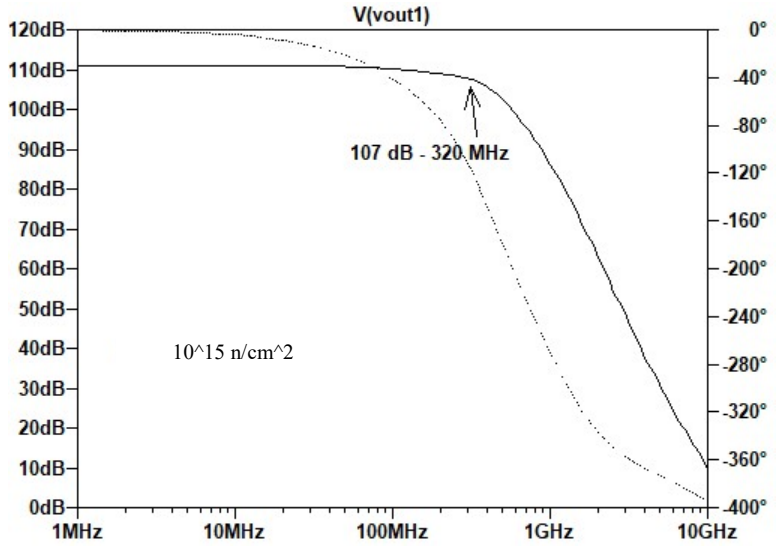

Figure 6.25 TIA irradiated by 10^{15} n/cm^2, gain was reduced to 107 dB

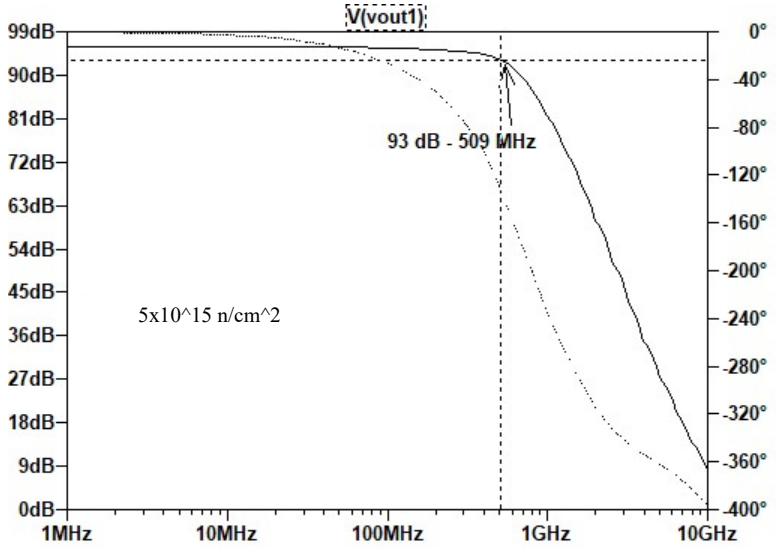

Figure 6.26 TIA irradiated by $5x10^{15}$ n/cm^2, gain was reduced to 93 dB and cut-off frequency moved to f_{3db} =509 MHz

CHAPTER 7 CONCLUSION

A transimpedance amplifier is designed to be front-end device to an avalanche photodiode (APD) or silicon photomultipler (SiPM) resistant to neutron fluence up to 10^{15}. The amplifier met all specifications needed to be used as a front-end device. The amplifier has a gain larger than ~375 k and a cutoff frequency at ~316 MHz, which is larger than the 1.67 MHz required for Cs_2LiYCl_6 (CLYC) scintillation pulses. It can amplify signals outputted by an APD made by C5 process [27]. This transimpedance amplifier demonstrate to have low noise with an RMS noise was 11 $nA/Hz^{1/2}$ integrated from 100 – 300 MHz. Amplifier simulation show a slew rate as high as 1.08 V/ns, allowing to drive relatively large loads. Power consumptions is low, approximately 11.6 mW, because of CMOS technology. Output voltage show low variation within temperature range from 0-100 °C. Neutron radiation effects simulation for a fluence of 10^{15} n/cm^2 of reactor neutrons (fast neutrons) show a low voltage output decrease of only 29%. The transimpedance amplifier is designed and simulated for a variety of conditions to verify it can operate as expected and it shows resistance to temperature, neutron effects, while maintaining high frequency gain and large output swing. Therefore, it can be considered that a design of a front-end transimpedance amplifier capable of sustaining 10^{15} n/cm^2 is achieved as theorized.

Further experiments and research with this TIA will be performed to show reliability for on real circuits. Fast neutron irradiation experiments must be performed to calculate lifetime and reliability performance. Investigation of suitable packaging rated for rad-hard should be done for this device. Finally, empirical electrical characterization must be performed on the fabricated chip to verity all the specifications are met. Future research can evaluate if doping could improve irradiation hardness. If that is the case, a researcher can decide whether to use more doping to make the TIA harder to radiation, add a voltage reference or add another amplifying stage that is

activated when gain drops to less than 50%. Finally, even though there are other semiconductor materials that people are researching for their high binding energy [29], silicon-based devices are still far from being replaced.

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CURRICULUM VITAE

Mario Valles Montenegro

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EXORDIUMS

I am a motivated, team player and ingenious electrical engineer with four years of experience working as an experimental physics researcher. Some of my skills include public speaking, creative problem solving, and project management. I have made presentation in technical conferences and to multiple stakeholders. Moreover, I have coauthored accepted proposals for LANSCE and LBL. I can communicate effectively with a team and I am very keen to develop more professional skills.

PROFESSIONAL SKILLS

IC analog, digital and RF circuit design, radiation effects engineering, high power lasers and project management, LabView, MATLAB, Inventor, SolidWorks, PCB Design

EDUCATION

University of Nevada, Las Vegas

Master of Science Degree in Electrical Engineering Graduating May 2020

- Heavy semiconductor and electromagnetics curriculum.
- Studies focused on radiation hard compound semiconductor devices (Transistors, HEMTs and LED devices composed GaN and SiC) and their utility for radiation detection.
- Characterized several semiconductor devices: electrical, optical, and gamma emission spectroscopy vs gamma irradiation.

University of Nevada, Las Vegas

Bachelor of Science Degree in Electrical Engineering Graduated: August 2015

- Focused on semiconductor and CMOS circuit design courses.
- Designed a CMOS audio amplifier with the minimum layout area and 20 gain.
- Designed an optogenetic stimulator for my senior design project. It consisted of stimulation of implanted proteins on a specimen cerebrum by temporal, spatial, and power modulated light guided through an optical fiber for neural switching control.

EMPLOYMENT HISTORY

Los Alamos National Laboratories

M-9 Graduate Research Assistant May 2019 – Present

- Developed and programmed standalone MATLAB graphical user interface (GUI) applications for photonic doppler velocimetry (PDV) and temporal magnetic gauge signal data processing.
- Designed and implemented a data acquisition system with a LabVIEW GUI, adding easy control of multiple instrumentations, enabling communication through TCP/IP, and including HDF5 (heriarchical) , WFM (bin) and DIG (bin) formats.
- Conducted 2-stage gas gun experiments on intrinsic materials to estimate the time an insensitive high explosive (IHE) setting will reach thermal equilibrium (LA-UR-19-27296).

University of Nevada, Las Vegas

Teaching Assistant January 2019 – May 2019

- Provided tutoring and laboratory mentoring to students in laboratory exercises and experiments for EE221L and EE420L courses (Circuits I and Analog Circuits) .
- Graded student reports providing feedback to increase the quality of their result discussions and their experimental procedure description.

University of Nevada, Las Vegas

Experimental Physics researcher November 2015 – January 2019

- Studied radiation effects on SiC power transistors, GaN optoelectronics, and HEMT devices, irradiated by high fast and thermal neutron fluences at LANSCE.
- Mentored and supervised 10 students in my professor's group.
- Designed electrical circuits and PCBs for experimental setups.
- Created remote automated data acquisition systems (LabView, Arduino, and MATLAB Programming).
- Processed large data sets for publication and research proposals.

Pride Communications

RF Technician September 2015 – November 2015

- Installed cable in ~8 houses per day for Cox Communications.
- Troubleshooted RF systems by increasing SNR on coaxial lines and network hardware.
- Eliminated ingress & egress from transmission lines to reduce noise and ambient interference.

PROJECTS

- **Front-end transimpedance amplifier:** Designed a C5-CMOS process amplifier circuit, with 300 MHz cut off frequency and 300 kΩ gain in a two-stage topology, to be integrated with a silicon APD.
- **Switching Power Supply:** Designed and layout a switching power supply on Cadence with C5-CMOS process, with efficiency larger than 90%, and low frequency for non-IME interference, capable to boost DC voltage to 7.5 V and supply current of < 50 mA with an input voltage of. 3.75 V to 7.5 V.

- **Automated optoelectronic platform:** Designed an automatic robotic manipulator for high radiation environments. It was composed of several electrical actuators and a mechanical arm, controlled by Arduino and LabVIEW, able to switch between multiple PCBs with several samples, for electrical and optical characterizations carried inside a light tight enclosure made from steel and polyethylene for the attenuation of gamma rays and neutron flux. Programmed high precision instrumentation for long term continuous characterization of multiple UV LEDs capable to acquire I-V curves continuously and indefinitely.

PUBLICATIONS

Sun, K.-X., Valles, M., Valencia, H. and Nelson, R. "Gallium Nitride (GaN) Devices as a Platform Technology for Radiation Hard Inertial Confinement Fusion Diagnostics." Review of Scientific Instruments 89, no. 10 (2018). doi:10.1063/1.5039407.

Svingala, F. R., Valles M. “A Plate Impact Target Design for 25.4 mm Diameter Samples Heated up to 250 C” Los Alamos National Laboratory internal report (2019), LA-UR-19-29257

LANGUAGES

Spanish with native fluency, fluent English, beginning Japanese and French

Desired to be able to communicate with various people and cultures around the world

EXTRACURRICULAR ACTIVITIES

Member of the Tau Beta Pi Honor Society.

Member of the Golden Key Honor Society.

Co-Founder of SPIE and OSA chapter at UNLV.

Founder and president of the Society of Engineers and Entrepreneurs at UNLV