ELECTROSTATIC DISCHARGE (ESD)
PROTECTION IN CMOS

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By
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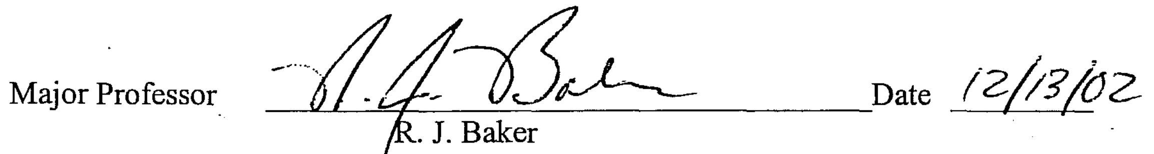

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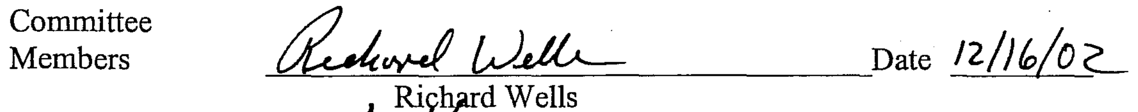

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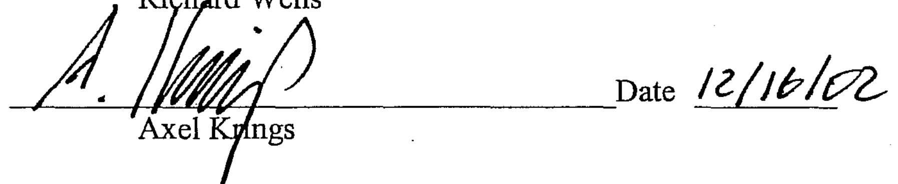

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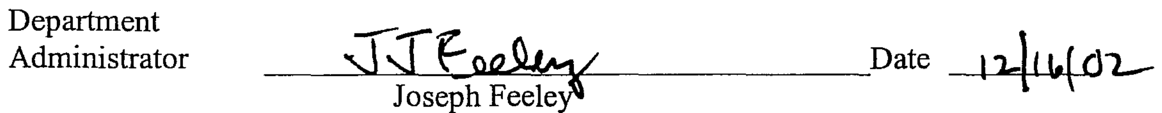

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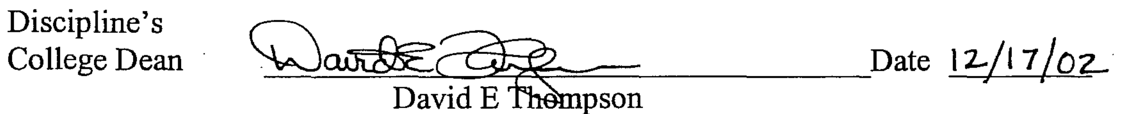

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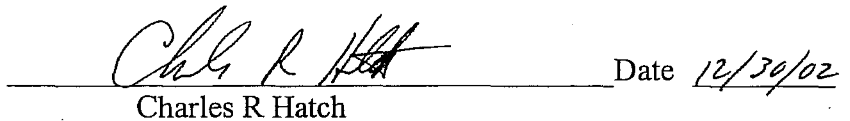

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ABSTRACT

In order to optimize the ESD performance of products in a CMOS 0.50um process, an ESD test chip was designed, fabricated, assembled, tested to the Human Body Model (HBM), characterized and evaluated.

This thesis begins with a brief overview of Electrostatic Discharge (ESD) and its reliability impacts on modern integrated circuits. The common ESD Device testing methods are outlined, with a strong emphasis placed on the current Human Body Model (HBM) test method. The Transmission Line Pulse (TLP) method of device characterization is introduced and explained in detail. The three basic ESD failure mechanisms are introduced: junction burnout, oxide breakdown and metallization burnout. The elementary ESD protection devices are discussed, these include Diodes, Field Devices, N-channel MOSFETs and Silicon Controlled Rectifiers. The HBM results and TLP characterization of the ESD test chip are included. Due to the presence of undesirable parallel paths, a technique is developed to determine the peak current flowing through a two path ESD circuit at the point of HBM failure. Lastly, a critical review is done of the test structures and test methods used so that future ESD test chips may be designed and tested with a higher probability of success.

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CHAPTER 1 - ELECTROSTATIC DISCHARGE (ESD) & INTEGRATED CIRCUITS

1.1 BACKGROUND OF ELECTROSTATIC DISCHARGE

Electrostatic Discharge (ESD) events occur in nature all the time. They are as natural as nature itself. Mechanical devices are exposed to ESD events routinely and damage is rarely, if ever, observed. This transfer of charge, however, can be dangerous, often fatal, to integrated circuits. As a general rule, unprotected MOS (Metal-Oxide Semiconductor) devices can only handle 100V of ESD. The average person can feel ESD events that exceed 3000V or 30 times the damage level of an unprotected modern integrated circuit. As the amount of charge generated by the average human or assembly machine can reach voltages in the range of thousands of volts, ESD protection circuits are vital to the long term reliability of integrated circuits.

The financial impacts of ESD failures are difficult to determine. It has been reported that between 25% and 75% of all field returns are due to damage caused by ESD or EOS (Electrical Overstress). The cost of field failures can be devastating, depending on the product the device is designed into. Process advances have often had the side effect of degrading the performance of the ESD protection devices. The introduction of LDD (Lightly Doped Drains), STI (Shallow Trench Isolation), ultra thin oxides, shallow diffused layers and silicided junctions have enhanced the performance of the ever shrinking CMOS device. These process enhancements have also correspondingly degraded the robustness of ESD protection devices. The ESD protection elements in a new process must be critically evaluated in order to achieve the required ESD objectives. Each new process brings new ESD challenges; a new battlefield, if you will, for the on going war against the damaging effects of ESD.

1.2 RELIABILITY AND THE BATH TUB CURVE

First proposed by the military in the 1950s, the bathtub curve, in figure 1, describes the failure rate of devices over time [1]. The failure rate is often defined using FITs, or Failures In Time. One FIT is defined as one failure in a billion (10^9) hours. There are three regions of the bathtub curve: infant mortality, operating life and wearout. Infant mortality begins in the factory and ends when the failure rate reaches a minimum, fairly constant value. The second region is the operating life portion, the region with the lowest failure rate, typically 10 to 100 FITs. The last region is wearout. In the wearout region, the FIT value begins to increase as the devices begin to reach the end of their life cycle. Typical failures in wearout are metal electromigration and oxide failures. Studies have indicated that a large number of "infant mortality" failures can be attributed to electrical overstress (EOS) or electrostatic discharge (ESD). In a survey by Sandia National Laboratory, over 1600 damaged devices were analyzed and 25.8% of the failures were attributed to EOS or ESD [2]. In 1992, Texas Instruments reported a 50% decrease in field failures on product after the part was re-designed and the ESD performance improved from 600V to 2000V [3].

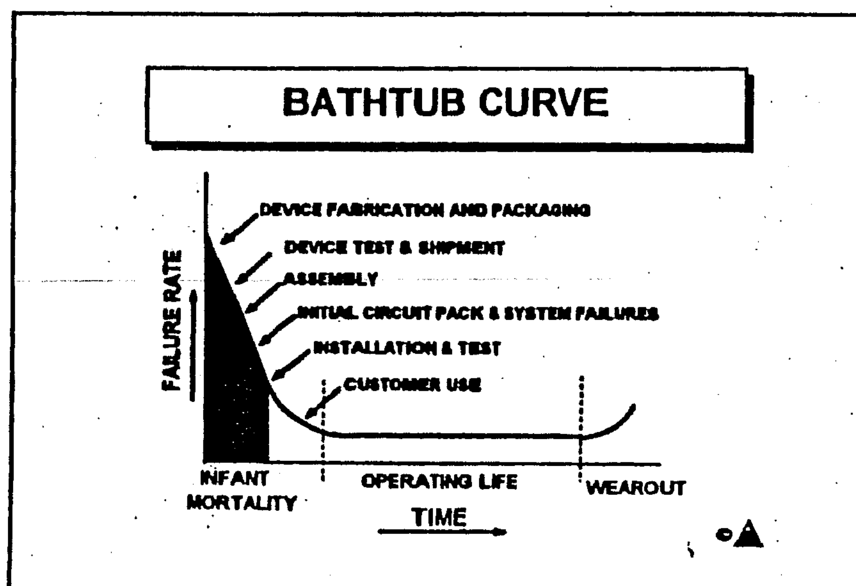

Figure 1 - Bathtub curve for device reliability [1].

1.3 Rent's Rule

As the complexity and circuit size of integrated circuits increases, the number of I/O pins to support these circuits must increase as well. The number of I/O pins, N_p, can be estimated from Rent's rule,

$$N_p = k \cdot N_{gates}^{\beta} \tag{1}$$

where k and β are constants depending on the product type and N_{gates} is the number of gates on the integrated circuit [4]. The values of k and β for a collection of integrated circuit types are listed in table 1. The number of I/O pins is plotted against the number of integrated circuit gates in figure 2. The general trend for all integrated circuit types is products with increasing number of I/O pins, with the chip and module type having the most dramatic increase in I/O pins. At the complexity level of a million gates, the pin counts for 3 out of the 5 product families are expected to have devices exceeding 1000 I/O pins.

Increasing the number of gates on the integrated circuit is accomplished by shrinking the physical size of the devices. As shown by Rent's Rule, increasing the number of devices corresponds to an increase in the required number of I/O pins. This results in a two-fold increase in the ESD vulnerability of future integrated circuits. Physically smaller devices are more susceptible to ESD damage than larger devices. Increasing the total number of pins, I/O and power supply, increases the chance of an ESD weakness existing between the large amount of pin combinations. For these reasons, ESD is expected to be a major concern for integrated circuit designs in the foreseeable future.

Circuit	β	k	Comments
SRAM	0.12	6	Memory
Microprocessor	0.45	0.82	Logic
Gate Array	0.50	1.9	Programmable Logic
Chip and Module	0.63	1.4	Package
Board	0.25	82	System

Table 1 - Constant values for Rent's Rule

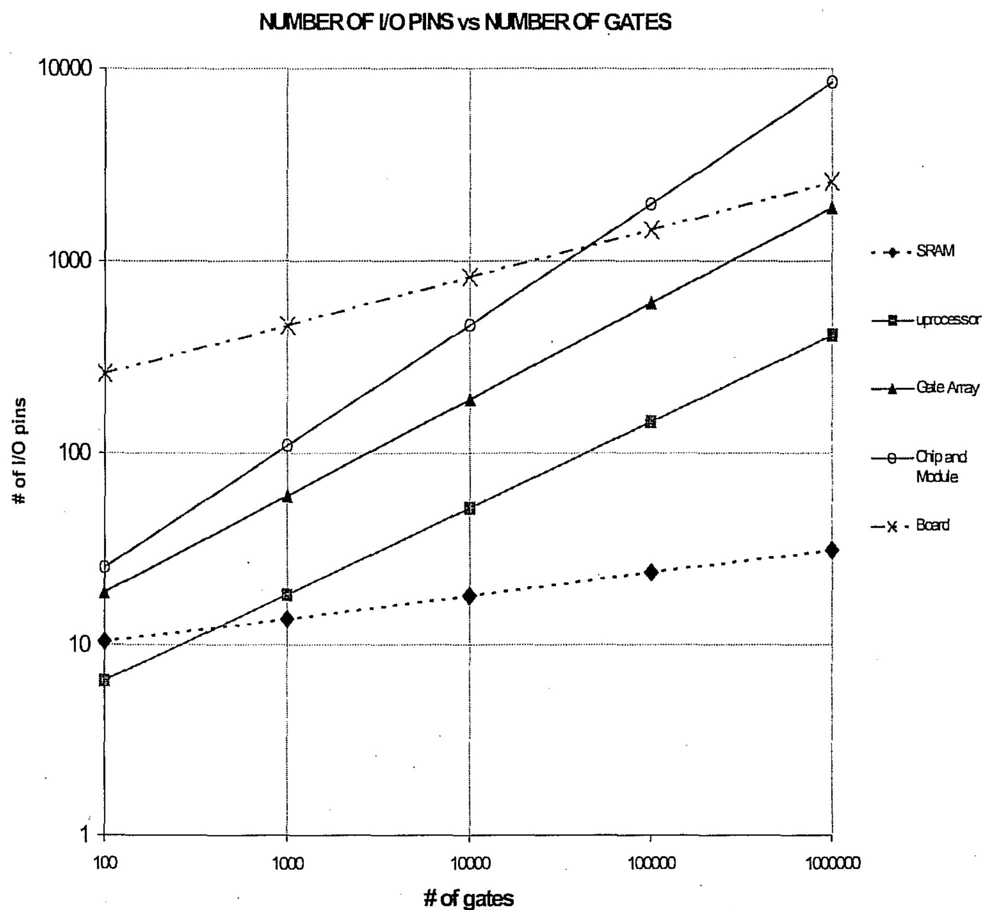

Figure 2 – # of I/O pins vs # of Gates using Rent's Rule [1].

The 1997 Semiconductor Industry Association (SIA) Roadmap, published by SEMATECH, declared the following statement regarding reliability of advanced CMOS processes:

"Below 0.18um, the key reliability issues will be the quality of very thin gate oxides and very shallow junctions, hot carrier reliability and adequate protection against ESD failures or latch-up"[5].

CHAPTER 2 - DEVICE LEVEL ESD TESTING

There are two basic mechanisms for an ESD event to occur with an integrated circuit. A charged body may contact a grounded integrated circuit or the integrated circuit may be charged and contact a grounded body. The first mechanism is emulated by both the Human Body Model (HBM) and the Machine Model (MM). In both of these models, charge is transferred to the integrated circuit. The second mechanism is simulated by the Charge Device Model (CDM). In this model the integrated circuit is charged and allowed to discharge to a grounded body. Although the word "model" is used, these are actually different ESD tests to determine the robustness (i.e. ESD hardness) of a particular design. These tests are used by the Semiconductor industry to qualify products to be saleable. A number of standards exist to outline each testing methods. The standards document the testing procedure, test equipment calibration and routine verification.

2.1 DEVICE TESTING MODELS

2.1.1 Human Body Model (HBM)

The HBM (Human Body Model) is the oldest and most widely accepted ESD test. This test is often considered "The ESD Model". The HBM model was originally developed for the mining industry. The mining industry was concerned about electrostatic discharges in mine shafts. The National Bureau of Mines first published human body capacitance values in 1962 [6]. The HBM model consists of a 100-picofarad capacitor, charged to the desired test voltage and discharged through a 1500-ohm resistor. This model was established as a Military approved Standard (Mil-Std), by the Navy in 1980. The minimum HBM withstand voltage is typically 2000V.

2.1.2 Machine Model (MM)

The Machine Model, which is often called the "Japanese Model", is quite similar to the HBM. This model is considered a worst case HBM test. Developed in Japan, this model uses a 200-picofarad capacitor with zero series resistance. This circuit attempts to model the ESD generated by sitting person, while using a metallic object to contact the integrated circuit. This circuit models the entire human body as a 200-picofarad capacitor with the metal object having no series resistance. One problem with this model is the requirement of zero resistance existing between the 200-picofarad capacitor and the PUT (Pin Under Test). As is it impossible to design test equipment with zero resistance, 5-ohms is allowed. Another, more serious, problem with the MM is the fact that the series inductance plays a major role in the discharge waveform. Correlation between different testers is often difficult, since the parasitic series inductance may vary from machine to machine. This "correlation" problem is among the reasons that this test is receiving less consideration in Japan and worldwide. As a general rule, integrated circuits found to fail at 200V or less are considered ESD vulnerable and devices found to pass at 400V are considered ESD robust. Due to the similarities to the Human Body Model, a correlation factor (typically 10 to1) is sometimes used when comparing MM to HBM results. The correlation factor is only valid if the two devices were found to have the same failure mechanism. For different failing mechanisms, no correlation can be made. Generally speaking, the Machine Model is a high current, low voltage ESD test, whereas HBM is a high voltage, low current ESD test.

2.1.3 Charged Device Model (CDM)

The Charged Device Model is now considered to be the primary cause of ESD failure in modern circuits. This testing method is very different than HBM or MM, as the integrated circuit is the source of the charge. During testing, the package is charged to the desired test voltage and then discharged through one of the pins. Unlike HBM or MM, this testing method is quite package dependent. Due to the lack of a generally accepted standard, CDM

was divided into two categories: socketed and non-socketed. In 1999 the ESDA released an official standard, ESD STM5.3.1-199, and socketed CDM was re-classified as Socketed Discharge Model or SDM. The standard covers non-socketed CDM, which is now the official CDM test method. This was important as most experts agree that the testing methods of CDM and SDM are very different. In CDM, the package is placed on test plane upside down, with the package pins facing up as in a "dead bug" position. A grounded pogo probe is used to discharge the package through a single pin. In SDM, the package resides in a socket and is charged through one of the pins. As with CDM, the device is discharged through one of the pins. Due to the parasitic capacitances associated with the relays inside the test system, the test system itself is a significant part of the model. Numerous recent papers have concluded that a strong correlation can not be made between CDM and SDM results, further proof that these are indeed unique testing methods. Of the two methods, CDM is the most common and has a stronger correlation to field ESD failures. No official standard exists for SDM, thus the future of SDM testing is unknown.

2.2 DEVICE TESTING PROCEDURES

In the semiconductor industry, the Human Body Model and the Charged Device Model are the widely accepted testing methods. The Machine Model and Socket Device Model are being used, but they are often supplemental tests. Both the Machine Model and Socket Device Model suffer from machine-to-machine calibration problems. The Machine model is highly susceptible to stray inductance and parasitic series resistance. The nature of the Socket Device Model is such that the system is an integral part of the test. Parasitic capacitances and series resistances in the relays create mismatched results between different machines. The Human Body Model and Charged Device Model are tests that can be correlated from machine-to-machine, even machines from different vendors. This has increased their acceptance by the semiconductor industry.

As real world ESD events are difficult to measure, ESD protection circuits are designed to pass the minimum acceptance levels of each test. It is often difficult to

determine if a failure was due to ESD or EOS. Electrical overstress is generally caused by voltages applied to pins above the maximum ratings stated on the product data sheet. In general EOS failures are quite severe and can often be observed with an optical inspection of the die. ESD failures can be difficult to find. Liquid crystal (LC) or photoemission techniques are often necessary to determine the location of the failure. Distinguishing EOS failures from ESD failures is beyond the scope of this thesis.

2.2.1 Human Body Model (HBM) Testing

It is important to remember that HBM is just a model. Real world human body discharges do not necessarily behave like the HBM model. The model was formulated by averaging a large sample of capacitance and resistance measurements on humans. A real human electrostatic discharge is a strong function of humidity, with low humidity environments being more prone to generate large electrostatic voltages.

In general, an ESD event can occur between any pin combination. For a complete, all-inclusive, ESD evaluation of a device, every possible pin combination would need to be tested. Under most circumstances, the worst case scenario would be to test one pin with only a single pin tied common as this would create the fewest current paths enabling larger current values to flow. The total number two-pin combinations is

$$C_{2,n} = \frac{n!}{2! \cdot (n-1)!} = \frac{n \cdot (n-1)}{2} \qquad (2)$$

where n is the total number of pins on the part. The number of pins involved in the combination has been fixed to 2, one test pin and one pin common.

For a 120-pin package, the total number of combinations would be 7,140. Using the Mil-Std HBM testing method (i.e. 6 pulses with a one second delay), each combination would take approximately 6 seconds to test. Testing a single sample to a single voltage level

would take 42,840 seconds or 13.8 hours. For a 208-pin package using the same test method, 21,528 HBM combinations exist and testing time is estimated to be 35.9 hours. The testing time for high pin count devices can be quite long using this method. For this reason testing standards have been developed to balance the need to reduce ESD testing time and at the same time provide an adequate evaluation of an integrated circuit's ESD susceptibility.

2.2.1.1 Mil-Std Human Body Model Test Method

The oldest Human Body Model ESD standard is the MIL-STD-883, Method 3015.7, titled: "Electrostatic Discharge Sensitivity Classification". All other HBM testing methods are based on this method.

Before testing, all of the pins on the device must be classified as one of the following:

1. Power Supply pins (i.e. VDD, VCC, VSS, GND, Vref, etc.);
2. I/O pins. This includes all input, output, I/O, test mode and programming (i.e. Vpp) pins;
3. N/C (No Connect) pins.

Each pin is classified based on the pin names on the integrated circuit data sheet. Since power supply pins are often internally connected, like-named (on the data sheet) pins are grouped together in separate power supply groups. Pins labeled as No connect (N/C) are not to be tested. The total number of combinations for single sample is

$$C_{milstd} = (n - I) \cdot (m + 1) - 2 \cdot S \quad (3)$$

where n is the total number of package pins, I is the number of N/C pins (ignored), m is the number of power supply pin groups and S is the total number of power supply pins.

Each pin combination is subjected to a series of three positive pulses followed by three negative pulses, with a minimum of one second delay between pulses. This series of

pulses is often named a "VZAP" and this terminology will be used from this point forward. Including the mechanical movement of the HBM system, a VZAP is estimated to have a 6 second duration. The HBM pulse is always subjected to a single pin, but one or more pins may be common. The Mil-Std HBM method requires each pin to be tested to each power supply group and each non-supply pin to be tested to all other non-supply pins collectively tied common. Supply pins in the same group are not tested to each other. Like-named supply pins are assumed to be metallically connected together, either inside the package or on the die, thus the ESD risk is thought to be low.

A common method of defining the HBM combinations is to group them into three test conditions as shown in table 2. Condition 1 is an HBM pulse to a pin with a GND pin or set of GND pins tied common. Condition 2 is an HBM pulse to a pin with a VDD pin or set of VDD pins tied common. The Condition 3 test is slightly different as the power supply pins are left floating. Each I/O pin (i.e. all non-supply pins) is exposed to an HBM pulse with all other I/O pins collectively tied common. This is one weakness in all of the standards as each I/O pin is not tested to all other I/O pins individually.

For HBM debugging, it is helpful to list the pulse polarity and the test condition. For example, a positive HBM pulse to an I/O pin with a GND pin connected common, would be classified as Condition 1+, or simply Cond 1+.

The number of pin combinations for Cond 1 will depend on the number of like-named GND pin sets that exist on the product. The same is true for the number of like-named VCC pin sets and the number of Cond 2 pin combinations. The number of Cond 3 pin combinations is simply the number of I/O pins (i.e. all non-supply and non-N/C pins) as each pin is tested once with all other I/O pins collectively tied common.

	PINs Tested	PINs not tested
Cond 1	All pins to each GND supply group	N/C pins
Cond 2	All pins to each Power Supply group	N/C pins
Cond 3	All signal pins to all other signal pins	N/C pins, All VCC and GND pins

Table 2 – Definition of HBM test conditions

Once the pins are classified, the HBM testing begins at the initial voltage value. The samples should have passed pre-HBM functionality tests. After all pin combinations have been tested with a complete VZAP (i.e. 3 positive followed by 3 negative pulses). The unit is ready to be evaluated by post-HBM functional tests. The company is allowed to choose the test voltage levels, but a minimum sample size of three units is required for HBM compliance at that withstand voltage level.

To determine the failing pin combination and polarity, isolated tests are necessary. Of the two, the failing pin combination is generally more useful. For reasons explained later, the most severe test conditions are Cond 1+ (a positive pulse to a GND pin) or Cond 2- (a negative pulse to a VCC pin).

The failure criteria for the Mil-Std HBM test is defined as a failure to the meet the data sheet specification values. The parts are generally tested to the same automated test program (i.e. ATE) before and after HBM stress.

To compare the HBM testing from the previous example to the combinations defined in the Mil-Std, the same 120-pin package is used. The part is found to have 20 supply pins, divided into 8 supply pin groups and no pins labeled as N/C; the total number of combinations would be 1,040. Each combination would take about 6 seconds to test. Testing a single part to a single voltage value would take 6,240 seconds or 1.7 hours. This is compared to 7,140 combinations and 13.8 hours calculated in the previous example. For a 208-pin package, with 40 supply pins, 16 supply pin groups and no pins labeled as N/C pins; 3,456 combinations exist with an estimated test time of 5.8 hours. This is compared to 21,528 combinations and 35.9 hours for the 208-pin package in the previous example.

2.2.1.2 JEDEC and ESDA HBM testing methods

The Mil-Std HBM testing standard, Mil-Std 883 - Method 3015.7, has been the industry standard for many years. Despite this wide spread acceptance, the standard does have some shortcomings. These shortcomings have not been addressed, nor are they expected to as the standard has not been updated since March of 1989. Two commercial HBM testing standards, one by JEDEC and one by the ESDA, are currently the most accepted HBM testing standards in the industry. The ESDA standard is STM5.1 and the JEDEC standard is 22-A114-B. Both of these standards were originally based on the Mil-Std, but have been revised at a rate of once every three years. In 2000, an effort was made to align the two HBM testing standards and they are aligned in most aspects [7].

One shortcoming with the Mil-Std method is the criteria for grouping like-named power supply pins. Pins with the same name on the data sheet may or may not be metallically connected. The JEDEC and ESDA standards have comprehended this and have placed a stricter requirement on grouping power supply pins. In the JEDEC and ESDA standards, supply pins are grouped by electrical properties not simply by the name. Supply pins in the same group must be metallically connected together, on the die or in the package, otherwise they are considered isolated supply pins. The ESDA standard places an additional requirement that the resistance between metallically connected pins must be under 2 ohms, otherwise the pins are considered part of isolated supply pin groups.

The other shortcoming of the Mil-Std method is the clause that allows for labeled N/C pins not to be tested. Test mode pins are often labeled as N/C on the data sheet to encourage them to be left floating in the customer application. As test mode circuitry uses the same supply and ground pins as functional circuits, ESD damage to these pins can cause a functional failure. Even non-bonded pins have been found to cause on-chip ESD damage [8]. The JEDEC standard specifically states that bonded No Connect (N/C) pins are classified as I/O pins and must be tested accordingly. Non-bonded No Connects (N/C) are package pins

that have no electrical connection to the encapsulated silicon die. The JEDEC standard explicitly states that these pins should not be tested. The ESDA standard makes no specific comment regarding these pins, implying that they should be tested as an I/O pin. Basically the ESDA standard requires all pins on the package to be tested, as all pins are classified as an I/O or power supply pin.

In attempt to reduce the overall testing time of high pin count packages, the JEDEC and ESDA standards have reduced the number of pulses and the delay between pulses in the VZAP. These standards only require one pulse of each polarity with a 0.3 second delay between pulses. This will reduce the ideal VZAP time from about 6 seconds to about 1.5 seconds (0.6 seconds for the delays, allocating 0.9 seconds for the pulses and mechanical relay repositioning time). This results in a 4X reduction in total testing time from the Mil-Std testing method. A VZAP, or series of pulses, are graphically shown in figure 3.

Although the ideal VZAP time was estimated to be 6 seconds for Mil-Std testing, actual time measurements on HBM systems indicate that VZAP times are generally on the order of 8 to 10 seconds. For JEDEC or ESDA testing, the VZAP time is on the order of 3-4 seconds. Most of the delays are included in the mechanical movement between pulses, tc in figure 3. The HBM systems also need more settling time between pulses of different polarities, this adds delay to the tb parameter. These increases are significant for large pin count devices, where a HBM testing a single device may take several hours.

As predicted by Rent's Rule, the number of package pins on future devices is expected to increase dramatically. This will present a problem for HBM testing in the future.

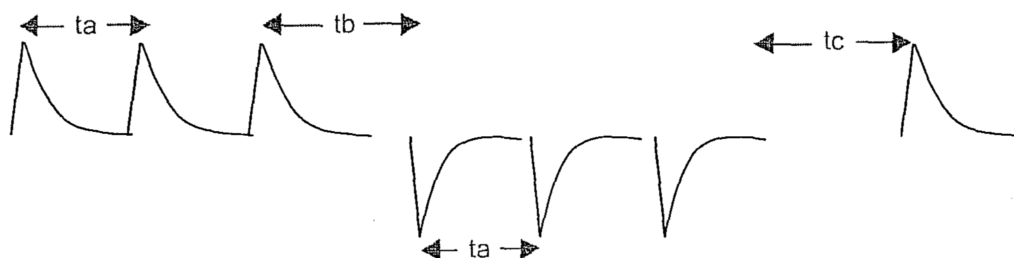

Figure 3 – Graphical representation of a VZAP, a series of HBM

Currently, the commercial system with the highest pin count testing ability can only test up to 1024 pins. For higher pin count devices, multiple custom test fixtures are required to properly conform to the testing standards.

2.2.2 Charged Device Model (CDM) Testing

The most CDM test systems charge the device using the Field Induced Method. This set up is shown in figure 4. The device is charged by first applying the test DC test voltage to the charging plate (the "Field Charging Electrode"). The packaged device is then charged to the test voltage. The grounded pogo probe is then placed on the discharge pin and the

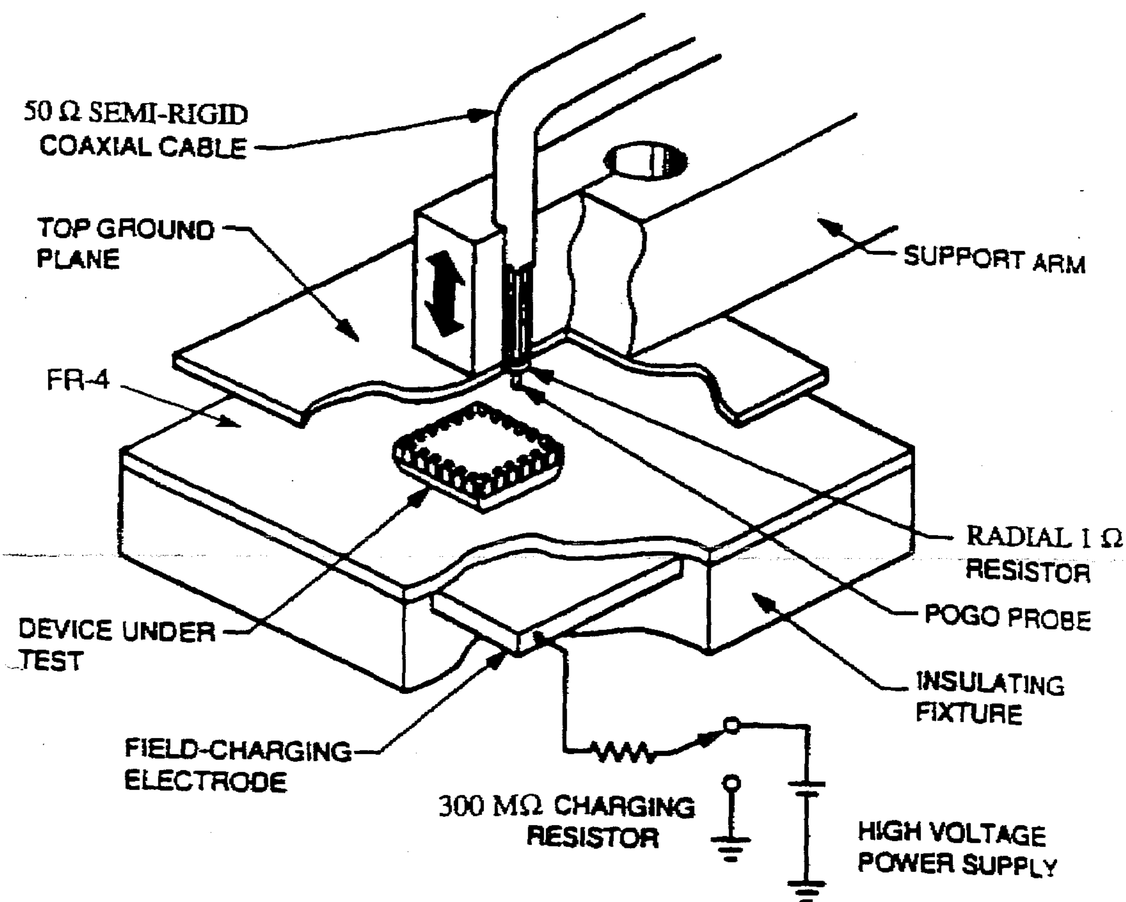

Figure 4 – Field Induced CDM Configuration [10].

positive CDM pulse is observed. The pogo probe is lifted off the discharge pin and the charging plate switch is move to GND. As the voltage across the capacitor (between the charging plate and the packaged device) must remain constant, the device is charged to the negative test voltage. The pogo probe is returned to the discharge pin and a negative CDM pulse is observed. This method allows dual polarity testing with only a single polarity voltage supply. To analyze CDM induced failures, a negative supply is used for single polarity testing. The coaxial cable allows for an oscilloscope to be connected in order for the peak discharge current, I_{cdm}, to be measured. This is also used for machine calibration.

Total testing time is not a major issue with CDM, as the number of discharge combinations is equal to the number of package pins. For evaluating failures induced during CDM testing, it is critical to determine the voltage, polarity and the discharge pin or set of pins that caused the failure.

As package units are tested in dead bug mode, CDM systems do not require package fixtures. As they don't use fixtures, CDM systems are not pin count limited like HBM systems. The only limitation on a CDM system is the area of coverage and the pin, or ball, pitch. Older CDM systems may need to be replaced as the ball and pin pitches become very fine on high pin count packages.

Testing the units in dead bug mode also requires the top of the package to be flat. This is a problem for engineering samples as the units are sometimes assembled in open cavity packages. Open cavity units can be CDM tested if the bond wires don't extend above the top of the cavity.

CDM is a package dependent test. The same die assembled in different packages may have different CDM results [9]. A product assembled in multiple packages, will require CDM testing for each package type.

CHAPTER 3 - ESD DEVICE CHARACTERIZATION

3.1 TRANSMISSION LINE PULSE (TLP)

The most widely accepted method of ESD device characterization is square pulse testing, more commonly known as Transmission Line Pulse (TLP) testing. TLP enables designers to model the device operation of circuits or devices under HBM-like stress. TLP testing extracts an I-V (current vs. voltage) curve for the device by subjecting the device to a series of short duration pulses. After each pulse, a DC leakage measurement is done to verify the integrity of junction. This test method was developed by T. Maloney and N. Khurana of Intel in 1985 [10].

Most TLP system use a 100ns pulse, although, as shown in figure 5 (a), the ideal pulse width is 75ns. At 75ns the energy of the square TLP pulse equals the energy in the HBM pulse. The equivalent TLP (b) and HBM (c) circuit schematics are also included in figure 5. The TLP rise-time is often variable, but is typically near 10ns to emulate the rise-time of the HBM pulse.

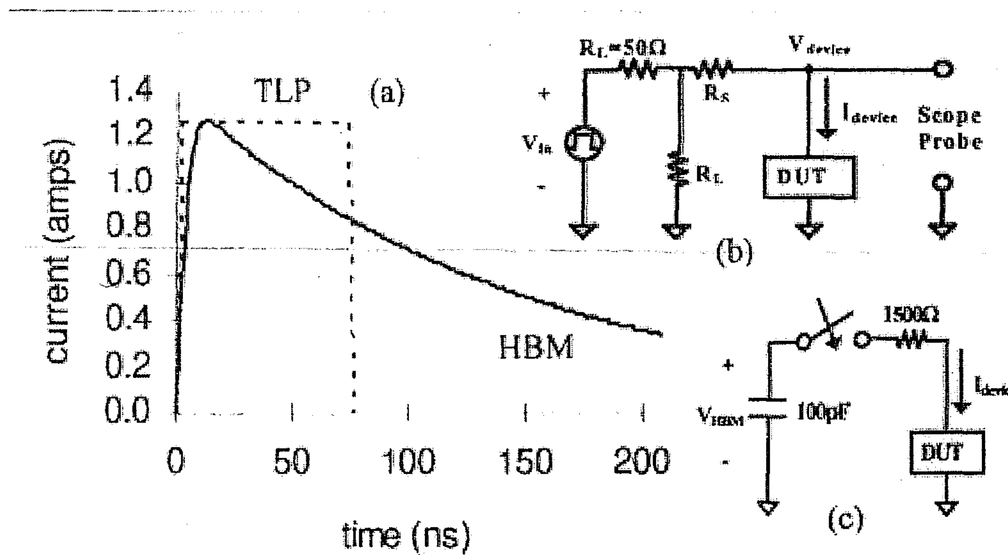

Figure 5 - HBM and TLP Waveforms [6]

The operation of the TLP system is as follows. A coaxial cable is charged to DC voltage level and then discharged, through a low impedance switch, into the device under test (DUT). The reflection current and voltage are measured to determine the amount of energy dissipated by the device. The voltage level is increased until device failure is observed. More advanced TLP systems measure the junction leakage of the device under test between pulses. The I-V and leakage curves are generated on the screen in real-time. Some systems allow the voltage step size to be modified while the test is in progress. Many TLP testing systems have been developed for laboratory use throughout the semiconductor industry.

For increased accuracy, the reflected voltages and currents are often measured during the last 20ns of the pulse. The rise time of the pulse can typically be adjusted as well. For HBM-like pulses, the rise time (10-90% method) is set to a value close to 10ns. The ESDA (Electrostatic Discharge Association) currently has a work group, Transmission Line Pulsing WG-5.5, developing a draft standard for TLP testing. Although numerous homemade TLP testers have been developed only a handful of companies currently offer a commercial version.

As the TLP system measures devices with a series of transient pulses, they can be used to measure just about any device. Although ESD protection devices are the intended devices to be measured with TLP, many other on-chip elements have been measured. This includes resistors, metal lines and gate oxides.

3.2 PARAMETRIC ANALYZER

Semiconductor parametric analyzers, like the HP-4156, can be used to generate I-V curves for ESD devices. This is a quasi-static DC measurement, closer to an EOS event than ESD, however. This measurement is done by forcing current into the device and measuring the voltage. An I-V waveform generated with an HP-4156 is shown in figure 6. The parametric analyzer is able to measure the trigger voltage and snap-back values with good accuracy. In figure 6, the trigger voltage is about 11V and the snap-back voltage is 6.5V.

Standard parametric analyzers are limited to source currents of 100mA, which is quite low for ESD analysis, where current values from up to 3A are expected. The on-resistance is often inaccurately measured. As the figure illustrates, the slope is almost vertical.

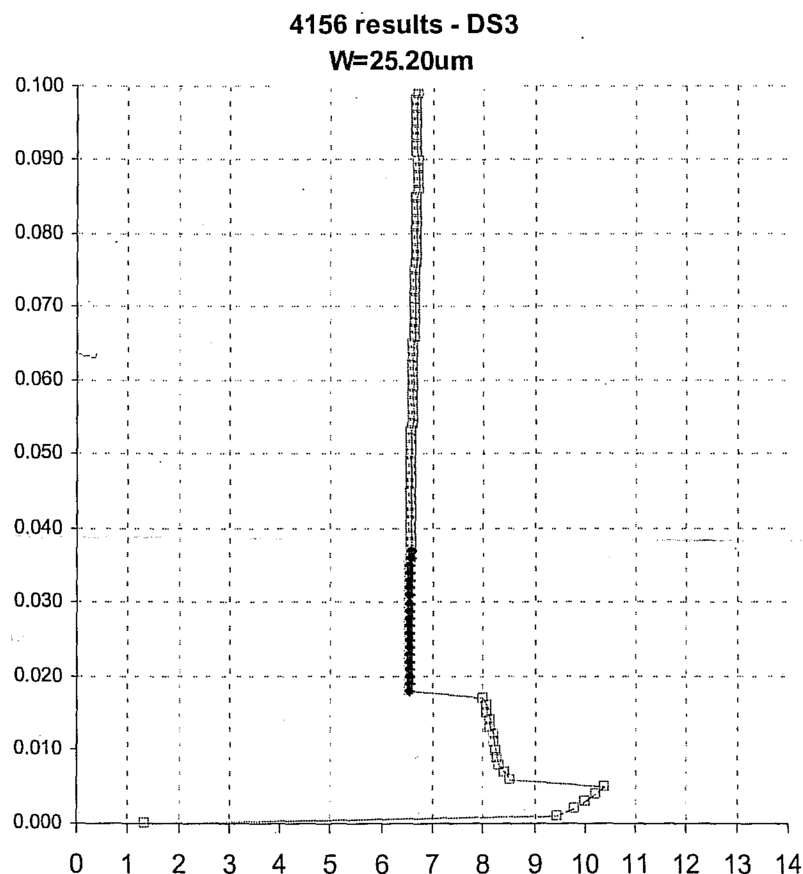

Figure 6 - Snap-back curves of 0.6um NMOS device using a Curve Tracer.

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3.3 CURVE TRACER (CT)

A curve tracer is an excellent tool for extracting device I-V curves. The Tektronics 575 or 576 models, despite their age, are wonderful instruments for ESD device characterization. Like the semiconductor parametric analyzers however, the I-V curve is extracted for an EOS-like waveform not ESD. Curve tracers do not have the power limitations of parametric analyzers and they are able to measure the region between triggering and snap-back than standard TLP systems, which are limited by a 50 ohm load line. Due to the DC nature of the curves and the high currents necessary to achieve NPN snap-back, the It2 value can not be measured with either a parametric semiconductor analyzer or a curve tracer. Figure 7 illustrates an I-V curve generated with a curve tracer.

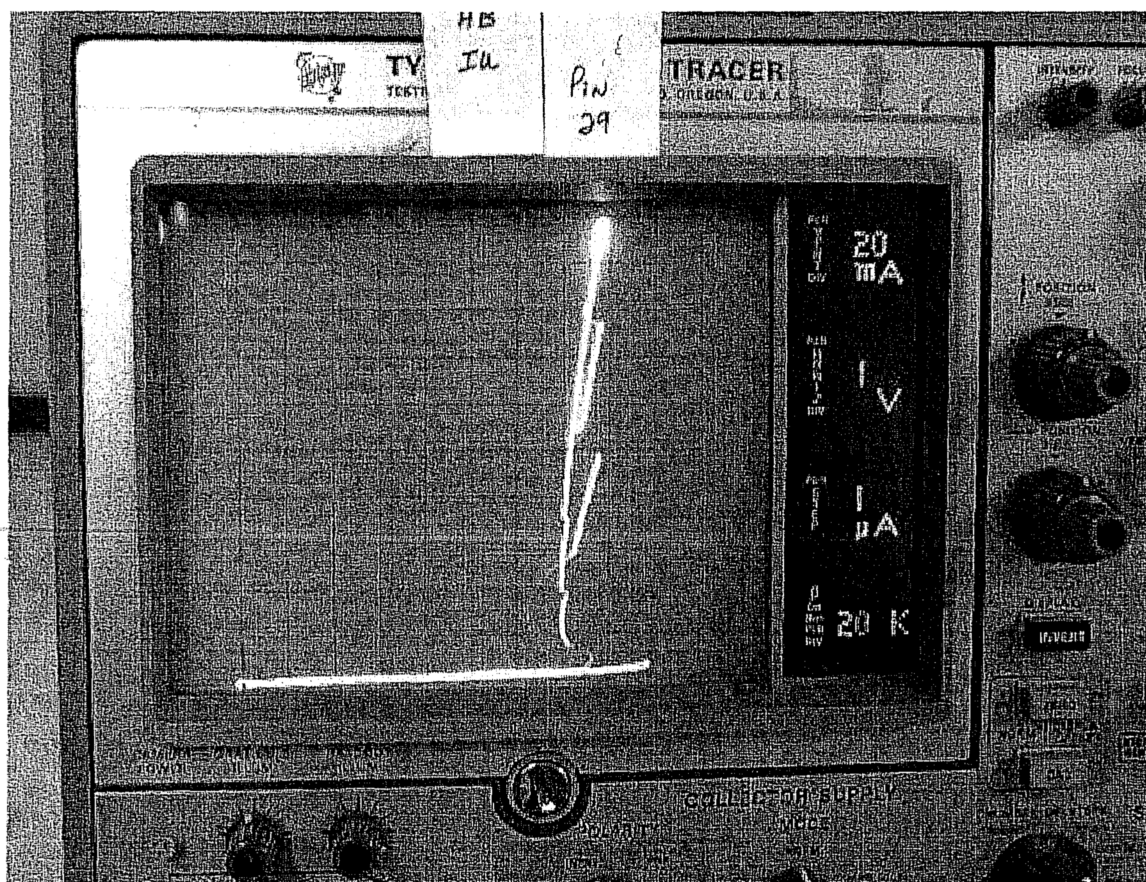

Figure 7 - Snap-back curves of 0.6um NMOS device using a Curve Tracer.

Depending on the robustness and the type of the device, I-V curves up to 500mA can be analyzed on a curve tracer. Due to the high power dissipation involved, these measurements need to be taken quickly (within a few seconds) to avoid damage to the device during testing.

CHAPTER 4 - ESD INDUCED FAILURE MECHANISMS

In semiconductor devices, three (3) basic mechanisms exist for ESD induced damage: junction burnout, oxide punchthrough and metallization burnout. These failures are thermally induced, indicating that the damage occurs once the local temperature of the region exceeds a critical value, often the melting point of the material.

4.1 JUNCTION BURNOUT

By far, the most common HBM failure mechanism is Junction Burnout. Junction Burnout is caused by the injection of an ESD transient of sufficient energy and duration to force the junction into secondary breakdown. Junction burnout is often characterized by high reverse bias leakage current or a total short. The first junction burnout model was developed by Wunsch & Bell [11]. Using rectangular EOS pulses, Wunsch and Bell developed a relationship between the area of the junction and the power dissipation level at the onset of junction failure.

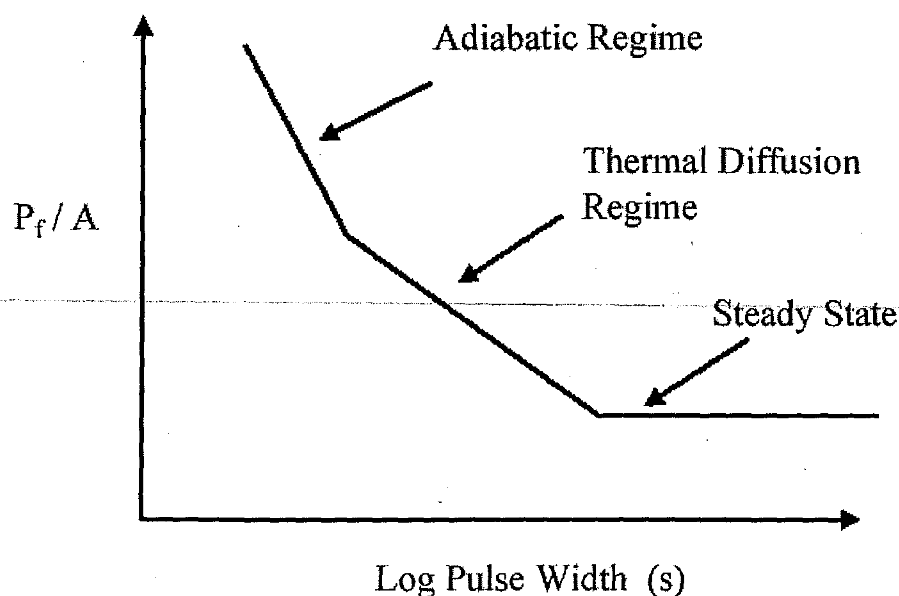

Figure 8 – Wunsch-Bell power to Failure curve versus log pulse width.

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The Wunsch-Bell curve, shown in figure 8, is divided into three time regimes: adiabatic, thermal diffusion and steady state. The proportionality of the power to failure to the pulse width is different for each regime. The adiabatic regime is proportional to the inverse of the pulse width ($1/\tau$), the thermal diffusion regime is proportional to the inverse of the square root of the pulse width ($1/\tau^{1/2}$) and the steady state regime is independent of pulse width. The duration of HBM pulses lies in the thermal diffusion regime.

The Wunsch & Bell equation (7) assumes that all of the power is dissipated in the junction, neglecting joule heating in the bulk silicon. The junction is assumed to fail when the temperature reaches the melting point of the semiconductor. The Wuncsh-Bell equation, normalized to the cross sectional localized area, is

$$\frac{P_f}{A} = \sqrt{\pi\kappa\rho C_p}\left(T_m - T_0\right)\frac{1}{\sqrt{t_p}} \tag{7}$$

where A is area, κ is the thermal conductivity, ρ is density and C_p is the specific heat. T_m is the melting point of the material, T_o is the initial temperature and τ_p is the width of the pulse. Although the equation looks complex, most of the variables are material constants. These values have been listed for both Silicon and Galium-Arsenide [12].

The right hand side of the equation (7) is constant for each ESD test. The difficult aspect of the equation is determining the cross-sectional area of the device under test. More accurate and more complex thermal equations have been developed since the Wunsch-Bell work was published, most recently by Dwyer, et al [13]. This will not be discussed as solving analytical equations is not common place for most ESD designers. Measuring test

	ρ	Tm	Cp	κ	C1
	[g/cm^3]	[C]	[J/g-C]	[W/cm-C]	(@ 25C)
Si	2.33	1415	0.70	1.31	3601
GaAs	5.32	1236	0.35	0.46	1986

Table 3 – Si and GaAs constants for the Wunsch-Bell Equation.

devices, as explained later, is the method used by most ESD designer to evaluate the robustness of a device under ESD.

As mentioned previously, Junction burnout is often characterized by an increase in junction leakage. Failure analysis of damage junctions has revealed that two types of junction burnout failures exist: hard failure and soft failures [14]. Both of these failures are observed in the SEM (Scanning Electron Microscope) photo in figure 9. The soft failures are the small spikes along the gate edge. The Hard failure is the severe damage site extending completely across the channel length of the device. Soft failures exhibit a slight increase in junction leakage, but the transistor is still functional. Devices experiencing hard failures are often not functional, exhibiting very high leakages. The electrical signature of the failure is often a resistive short across the drain and source terminals of the device.

During electrical measurements, soft failures will often pass data sheet leakage specifications (typically under 1uA), while hard failures will have measured leakages typically in the mA range.

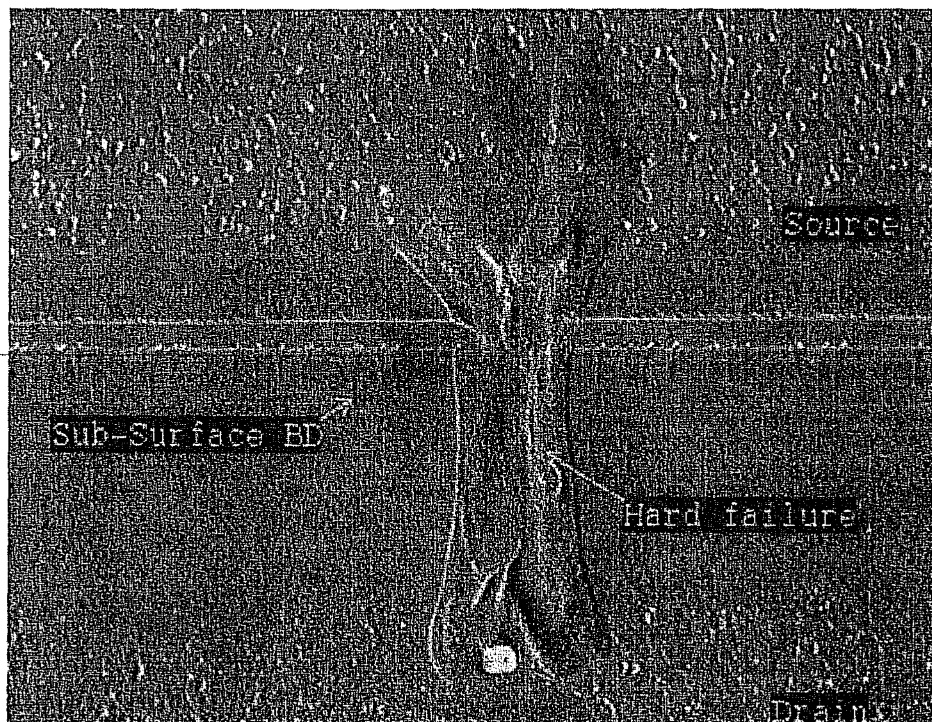

Figure 9 – Hard and Soft junction failures on an NMOS device

The junction leakages of two devices are shown in figure 10. Each leakage measurement was taken immediately after the junction was exposed to square pulses of increased power magnitude. The devices were a field oxide device (FOX) or TFO, represented with open circles, and a grounded gate NMOS (GOX), represented with solid circles. The current measured after each pulse is indicated on the x-axis of the plot. The GOX device is observed to have only one data point classified as a "Soft Failure". The FOX device, on the other hand are observed to have a number of "Soft Failure" data points, 8 in this plot, before a "hard failure" is observed.

Hard failures are often caused by melt filaments from the drain to source, due to the thermal effects of second breakdown. Hard failures generally can be detected on the TLP I-V waveform. These failures also have high leakage values. Soft failures are due to sub-surface breakdown, characterized by the needle-like structures shown in figure 9. These failures are not visible on the TLP I-V waveform. Soft failures often observed just prior to the creation of a hard failure.

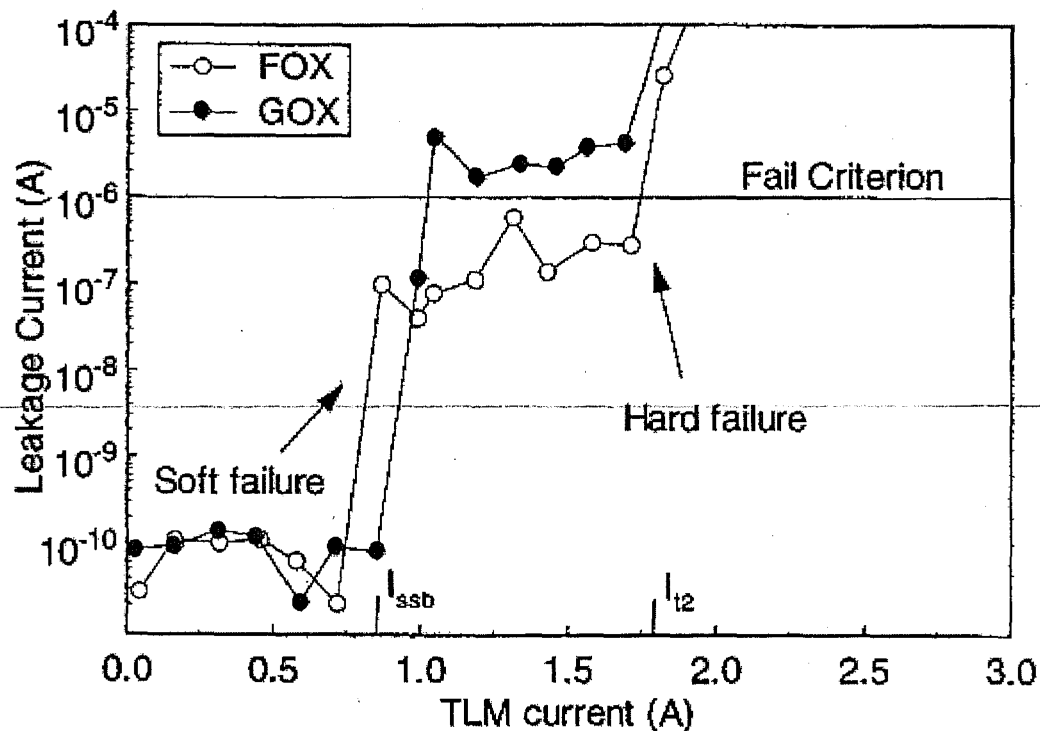

Figure 10 – TLP Leakage Currents on TFOs and NMOS devices [13].

4.2 OXIDE PUNCHTHROUGH

The primary goal of an ESD protection device or network is to protect ESD vulnerable circuits. ESD Vulnerable circuits consist of junctions and oxides. Junction Burnout has already been discussed. Oxide punchthrough is the other major category of ESD damage. Oxide punchthrough occurs when an oxide is subjected to an ESD pulse of a high enough magnitude to cause the oxide to breakdown. Experiments have shown that oxide breaks down in the area where the oxide is subjected to the greatest electric field strength. On defect-free devices, the oxide breakdown is on the corner or edge of the device. If the oxide breaks down in another location, this location is assumed to have an oxide defect such that the effective electrical oxide thickness in that location is less than the rest of the structure.

Oxide breakdown, initiated by oxide punchthrough during human body-like ESD events, is a rare in modern products. In the past, HBM induced oxide failures were more common as pins were designed without ESD protection. In the short transient domain of an ESD event, the voltage applied the gate oxide must be very large to initiate oxide breakdown. For a field return, oxide breakdown is probably a symptom of a CDM (Charged Device Model) ESD event. A more common event under HBM is the accumulation of trapped charge in the gate oxide, leading to a change in the threshold voltage (Vt) of the MOSFET device.

For long term operation, it is recommended to keep the direct current (DC) oxide electric field strength less than 7 MV/cm [15]. This equation is valid for oxide thickness values greater than 4nm. For thinner oxides, $T_{ox} < 4nm$, the electric field is expected to be slightly higher, perhaps as high as 8 or 9 MV/cm.

Oxide punchthrough and the introduction of trapped charges are a function of the oxide thickness, the magnitude of the applied stress and the duration of the stress. For transient events, such as ESD, the oxide can handle higher electric field values. For a 100ns

pulse, the electric field can be as high as 38MV/cm before the oxide breaks down. ESD induced trapped charges have the effect of shifting the Vt of the device.

A plot showing the effects of 100ns pulses on devices with various oxide thickness values is shown in figure 11 [16]. The oxide breakdown voltage and 10mV shift in the measured Vt of the devices are shown. For comparison, the clamping voltage of a grounded gate NMOS device is also included. The graph indicates that with thinner oxides, 5nm in the plot, the difference between the oxide breakdown voltage and a 10mV Vt shift is reducing with oxide thickness.

A slight, 10mV, increase in the Vt of digital circuits such as the gate of an input buffer, may not have any adverse effects. Most digital devices are designed with enough margin that a small change in Vt may be virtually unnoticeable to the rest of the circuit.

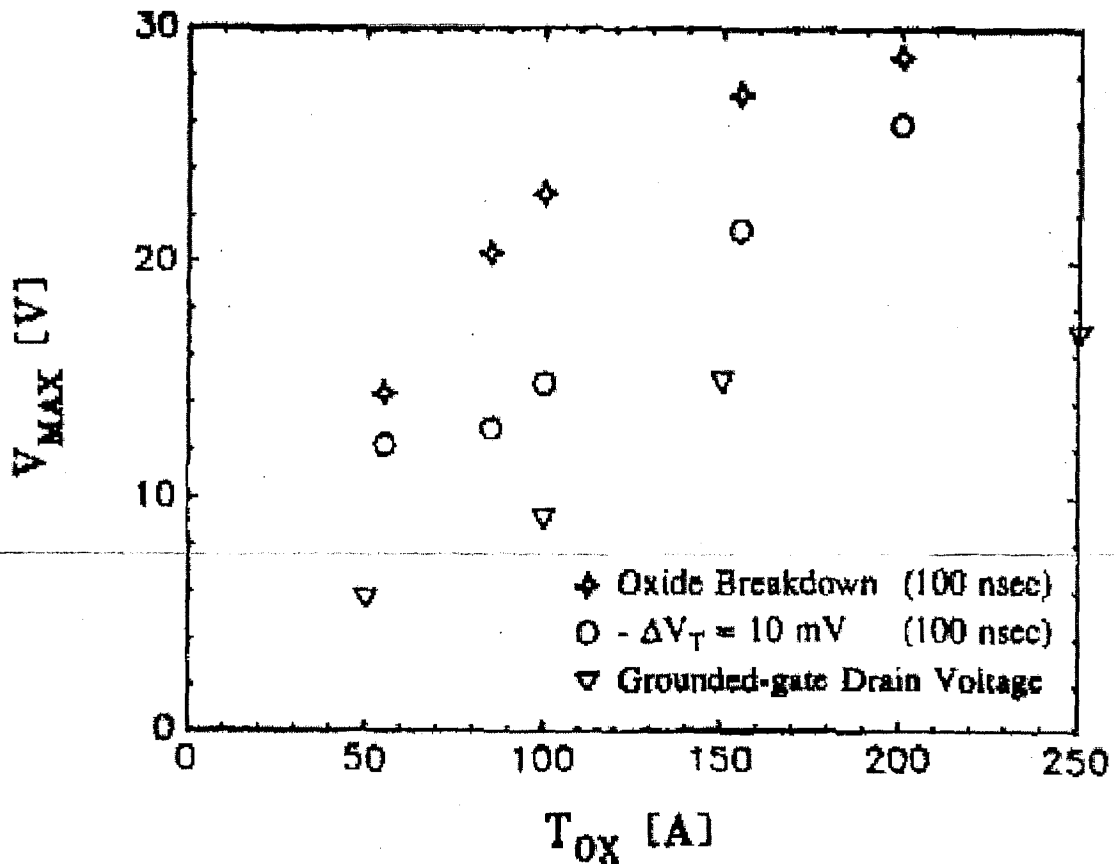

Figure 11 - Oxide Breakdown and Vt shifts for various oxides [15].

Analog circuits, such as matching inputs of a differential amplifier, are typically quite sensitive to a shift in Vt. A shift of 10mV may cause a functional failure.

Oxide failures are the most common failure observed during CDM events. The high currents involved can develop large voltage drops across gate oxides, near the bond pads or on the interior devices. Output pads with drivers connected to “quiet” independent supplies are quite vulnerable to CDM events [17].

4.3 METALLIZATION BURNOUT

The last basic ESD failure mechanism is metallization burnout. Metallization burnout exists in metal interconnects or, in older technologies, flowed vias or contacts. Metallization burnout occurs if the current flowing through the metal forces the temperature to rise, due to the I^2R power calculation, high enough to reach the melting point of the material. The melting point of Aluminum (Al) is about 650°C, compared to 1415°C for silicon. Metallization burnout is often a secondary effect, occurring after the initial junction or oxide failure took place. Flowed contacts, on Spin on Glass (SOG) metal deposit processes, is the location of the thinnest metal layer and are a common location for metallization burnout. The wide use of Tungsten plug technology for interlayer contacts, is expected to reduce the risk of contact metallization burnout.

Layout mistakes with regards to metal widths and the number of contacts or vias are the common cause of metallization burnout in today’s devices. Wide metal interconnects along with ample contacts and vias should prevent metallization failures due to ESD.

CHAPTER 5 - BASIC ESD PROTECTION DEVICES

The following section introduces the common devices available to an ESD designer in a CMOS process. These devices can generally be designed without adding additional processing or masking steps. These are devices are often used as the building blocks to create the complex ESD circuits used on modern integrated circuits.

5.1 DIODES

"I've never met a forward biased diode I didn't like", said TLP co-developer and ESD pioneer Timothy Maloney of Intel during the 1998 EOS/ESD Symposium. Diodes operating under forward bias are, quite possibly the best ESD protection elements available. They have a low turn-on voltage (Vbi), low on-resistance and are very robust (high ESD current handling ability). Under reverse bias, the diode is not an efficient ESD protection device. The turn-on voltage is quite high, with a high on-resistance and low ESD robustness.

Most diodes designed in a CMOS process are PIN diodes, as a lightly doped region often separates the highly doped diffusion regions. Placing two highly doped diffusion regions, of opposite polarity, in an abutting connection will create a zener diode with a very low breakdown voltage. The ideal PN diode equation is

$$I_D = I_0\left(\exp(\frac{V_D}{n \cdot V_T}) - 1\right) \tag{8}$$

where I_0 is the saturation current, V_D is the voltage across the diode, n the ideality factor and V_T the thermal voltage. Diode SPICE models, extracted for CMOS processes, are generally optimized for low current values, typically under 100 mA. These models are generally not accurate enough in the ESD domain as the series resistance of the lightly doped intrinsic material may have a significant influence on the I-V curve.

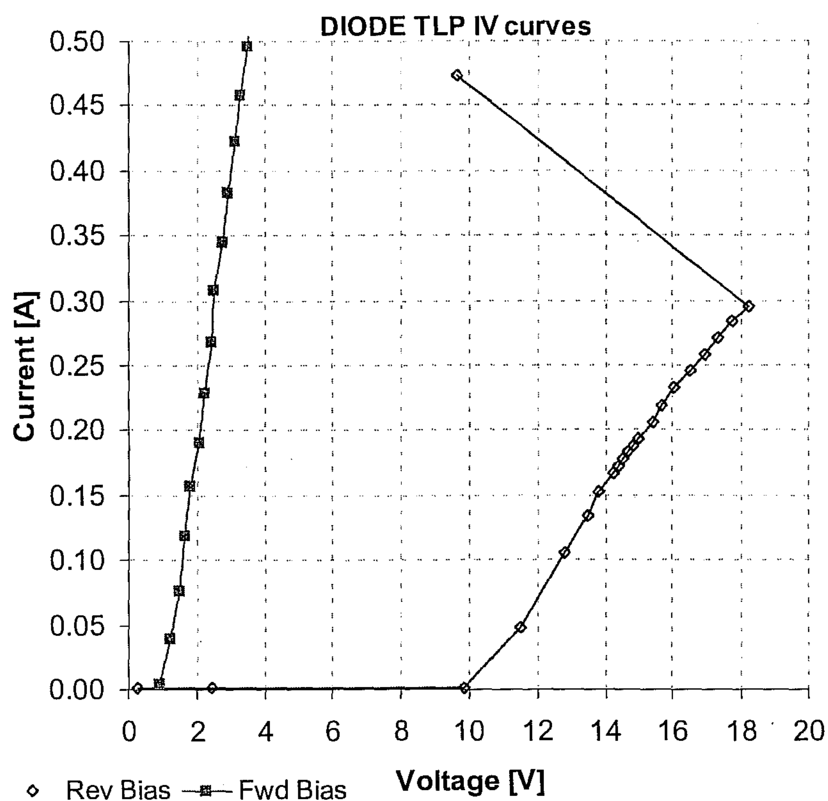

Figure 12 – Diode IV curves under forward and reverse bias.

The I-V curves under both forward bias and reverse bias conditions are shown in figure 12. The magenta line (solid squares) is the diode under forward bias and the blue line (open diamonds) is the diode under reverse bias. Comparing the two waveforms, the forward bias waveform has a lower clamp voltage (1.3V compared to 10V) and a lower on-resistance (1.3 ohms compared to 4.1 ohms). The robustness factor of a diode is often determined by the maximum current flow in the junction at the onset of second breakdown. This current value is called It2. For the diode curves, the It2 value under forward bias was measured to 5A, which is not shown in figure 12. Under reverse bias, the It2 value is observed to be about 300mA. On the reverse bias waveform, after the device reaches It2 (300mA, 18.2V) the current is observed to dramatically increase with drop in the voltage (470mA, 9.5V), indicating a melt filament has been formed across the PN junction. The junction has been permanently damaged.

5.2 NMOS PROTECTION DEVICES

NMOS devices can be used as ESD protection devices in active or snap-back modes. In active mode, the device functions as a standard NMOS device. The device must be very wide to conduct the large ESD current and a gate bias is necessary to turn on the device. Active clamps operate in saturation and must be thousands of microns wide [18]. Active clamps have a low normalized ESD rating, typically 1.2 to 1.5 mA/um. This is due to the high current density flowing across the narrow channel region of the device. One advantage to active clamps is the ability to layout the device using minimum design rules, allowing a large device to be designed with minimum area. Another advantage to active clamps is the ability to simulate the devices with the BSIM (Berkeley SIMulation) SPICE model.

The most common mode of operation for NMOS ESD devices is in parasitic bipolar snap-back mode. The primary layout parameters of a snap-back NMOS ESD protection device is shown in figure 13. The key layout parameters are the width of the device (W), the channel length of the device (L) and the Drain Contact to Gate space (CGSd). The large Contact to gate space is one feature that differentiates an ESD device from a standard CMOS device. Inherent to every NMOS device is a parasitic lateral NPN bipolar device. A cross

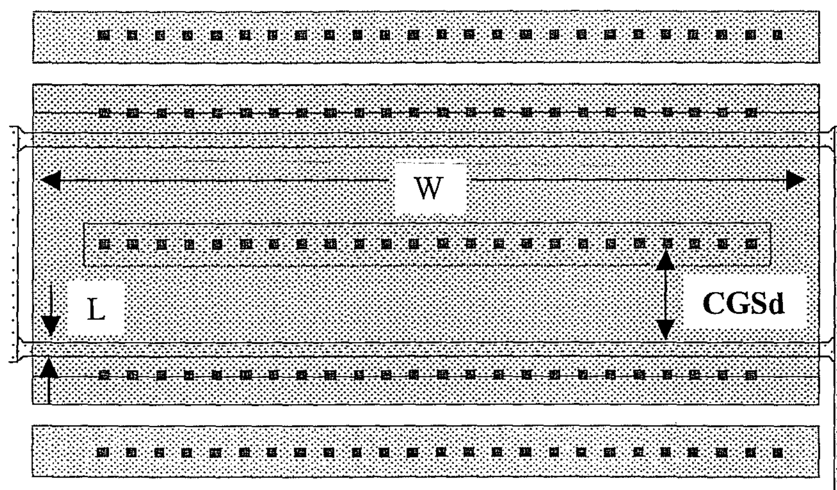

Figure 13 – Layout of an NMOS ESD Protection Device.

section of a grounded gate NMOS device (GGNMOS) is shown in figure 14, including the parasitic lateral NPN device. The drain of the NMOS is also the collector of the NPN device, the source is also the emitter and the P-substrate forms the base. The channel length of the NMOS device defines the base width of the NPN device. A series base resistor (Rsub) exists between the P+ substrate tap and the NMOS channel.

Under normal operating conditions, the base-emitter voltage of the device is near zero and the device remains dormant. If the substrate current flow (across Rsub) is large enough to forward bias the base-emitter junction, the NPN device turns on and begins to conduct current. Once the NPN device is on, the NPN device enters snap-back and the device can be modeled as a diode with a built-in voltage, often called the snap-back voltage Vsp, and an on-resistance, Ron.

The most important layout parameter of an NMOS protection device is the width (W). In order to conduct the large currents of an ESD pulse, often in the several amp range, the ESD protection device must be quite wide. NMOS ESD devices are often designed with multiple devices in parallel. These small devices are often called "fingers". The device in Figure 13 is a two-finger device. These fingers should be uniformly designed, with all fingers having the same width, length, contact-to-gate space and aligned drain and source contacts. The contacts are aligned to avoid current crowding, which encourages uneven

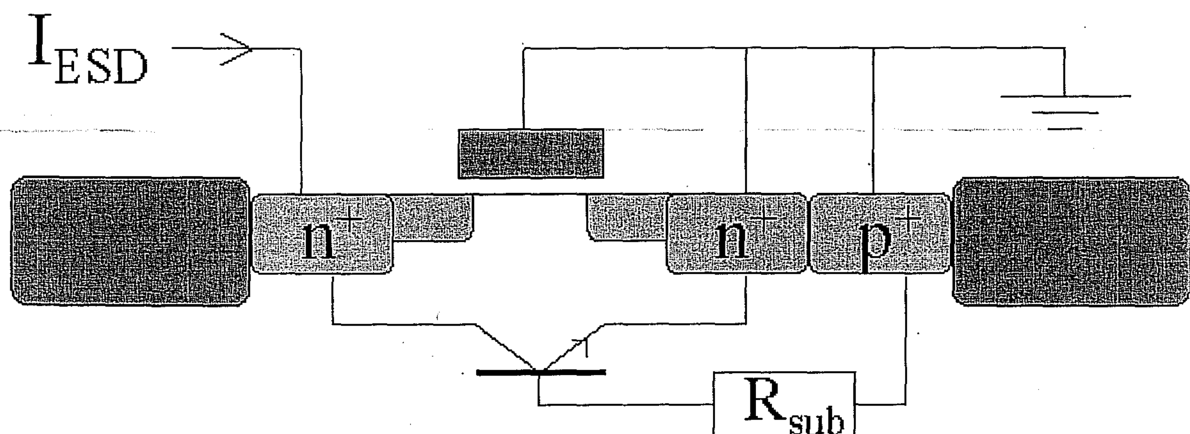

Figure 14 – Cross section of a GGNMOS device [14].

power dissipation and low ESD robustness. Similar to analog devices, ESD devices should be described by the finger width and the total number of fingers, not by their total width.

The ESD performance, often normalized to the device width in terms of ESD V/um or mA/um, generally does not scale with finger width. As the length of the finger increases, the ESD V/um rating often decreases. Each process will have an optimum finger width to achieve the maximum ESD robustness.

The channel length (L) of the device is important because it sets the base width of the parasitic bipolar device. The NPN base width sets the snap-back voltage (Vsp) of the device. Smaller channel lengths will enable lower snap-back voltages and reduced on-resistance. As CMOS ESD protection devices are often used as pad output drivers, the channel length is often designed 10-20% larger than the process minimum design rule.

The last critical parameter of the device is the Drain Contact to Gate Space (CGSd). In silicided processes, with silicide block, this space is defined as the space between the silicide block layer and the polysilicon gate. Increasing the contact to gate space increases the robustness of the device in two ways. Adding series resistance between the contacts and the junction promotes more uniform heat dissipation, reducing localized heating. This effect tends to saturate at a certain value, often between 4-6um on a non-slilided or silicide block process. This series resistance is called " ballasting". Ballasting effectively increases the on-resistance of a single finger such that the Vt2 (the voltage at the onset of second breakdown) for each finger is increased. This encourages the uniform turn-on of a single finger and helps in turning on multiple fingers during the ESD pulse. Increasing the Vt2 point has the negative effective of increasing the on-resistance of the device, reducing the effectiveness of the ESD device.

The TLP I-V (solid line) and junction leakage (dotted line) curves for a snap-back mode NMOS device are shown in figure 15 with the critical ESD parameters labeled. The NPN trigger voltage of the device is called Vt1, about 11V for this device. Once the parasitic

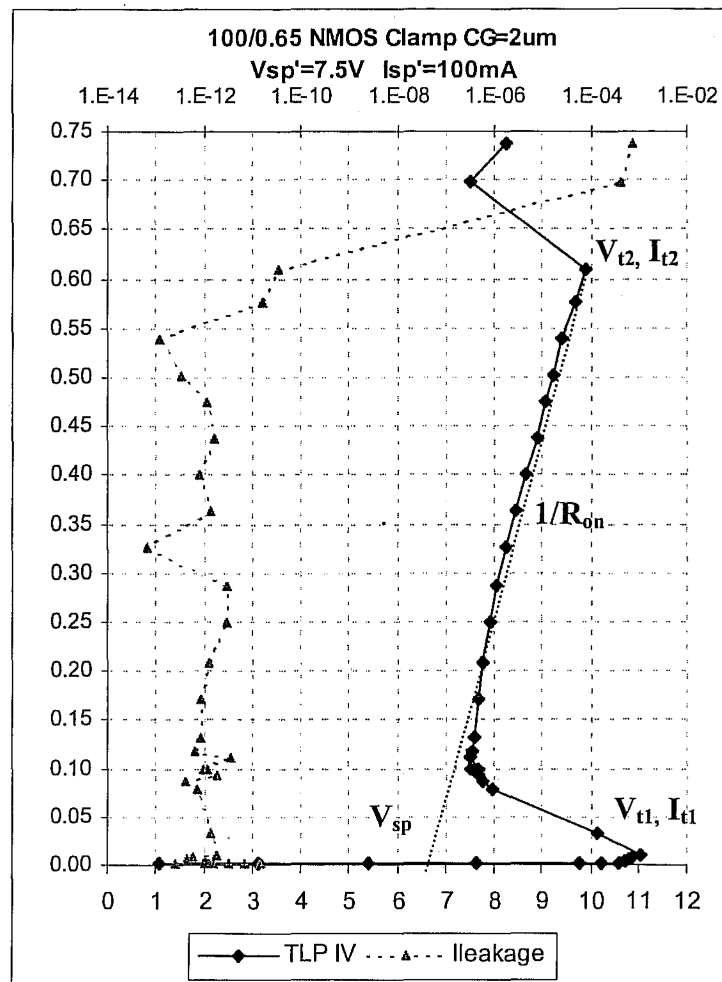

Figure 15 - Typical TLP I-V and leakage curves for a GGNMOS device.

NPN device triggers, the device enters snap-back and conducts current with a linear on-resistance. This is the operation mode of the device under ESD conditions. The snap-back voltage is interpolated back to the x-axis, 6.4V for this device. The on-resistance of the device is the inverse of the slope of the curve in the snap-back region. The (Vt2, It2) point is the voltage and current values at the onset of second breakdown, 10V and 610mA respectively for this device. Second breakdown leads to thermal run away and catastrophic junction failure. Junction failure can be determined by the leakage current measurement. The leakage at the (Vt2, It2) point was 0.1 nA, increasing to1 mA after the next pulse.

5.3 THICK FIELD OXIDE DEVICES (TFOS)

Back in the 1980s, before the introduction of sub-micron processes, Thick Field Oxide devices (TFOs) were the dominant ESD protection devices. These devices are also called Thick Field Devices (TFDs), Field MOSFETs or simply Field Devices. With the introduction of Lightly Doped Drain (LDD) technologies, Shallow Trench Isolation (STI) and ultra thin gate oxides into sub-micron processes, the performance of this device was found to decrease significantly. In modern processes, particularly on high voltage pins, these devices are still being used. As many parasitic devices in the interior section of the integrated circuit are actually field devices, characterizing these structures is still a useful exercise. The layout of a typical metal gate Thick Field Oxide (TFO) device is shown in figure 16, including the critical ESD layout parameters.

These devices are designed by placing two N+ diffusion regions adjacent to each other. This forms a parasitic NPN transistor with the N+ regions forming the collector and source regions with the P-substrate forming the base. The width of the TFO is the width of

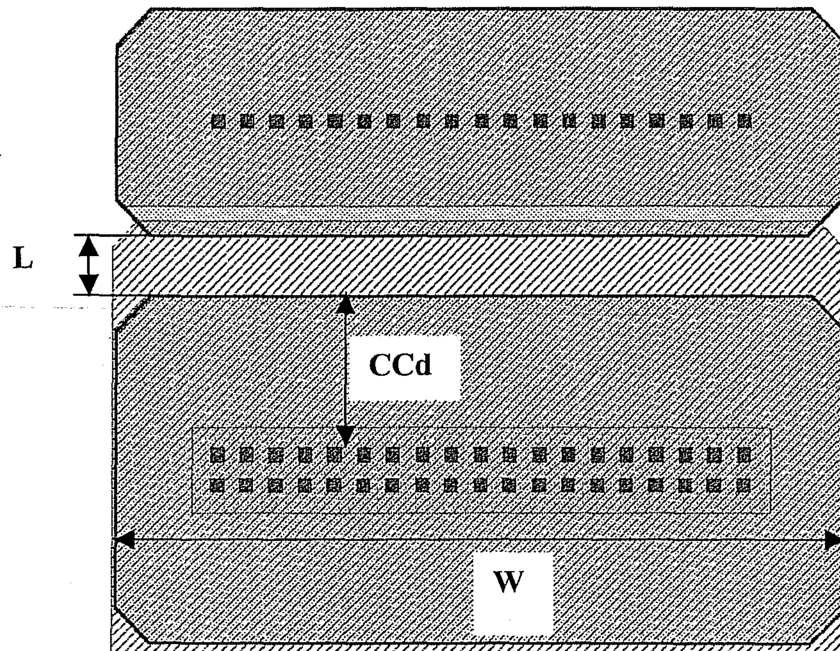

Figure 16. Layout of a Metal Gate TFO.

the diffusion, defined by "W". The channel length, "L", is the distance between the two diffusion regions. The Drain Contact to Channel space, "CC_d", is also critical to the ESD performance of the device. This TFO has a metal gate extending over the channel to source region. These devices can also be designed with a Polysilicon gate or no gate (as shown in figure 17). The TFO in figure 16 has a double row of drain contacts with an N-well contact plugs. The N-wells are called "N-well contact plugs" and help extend the P-N junction deeper into the substrate.

The cross section of the TFO is shown in figure 17. This figure is quite similar to the cross section diagram on the grounded gate NMOS device. The only difference is field oxide separation between the drain and source on the TFO, where gate oxide was used on the NMOS device.

The operation of this device is similar to the NMOS device described previously. As the current must flow beneath the field isolation, the current flow is deeper than in the NMOS device. This device generally has higher snap-back voltage, Vsp, due to the effectively longer base width (channel space is generally longer than the length of the NMOS device). Higher on-resistance, Ron, but ultimately higher I_{t2} values.

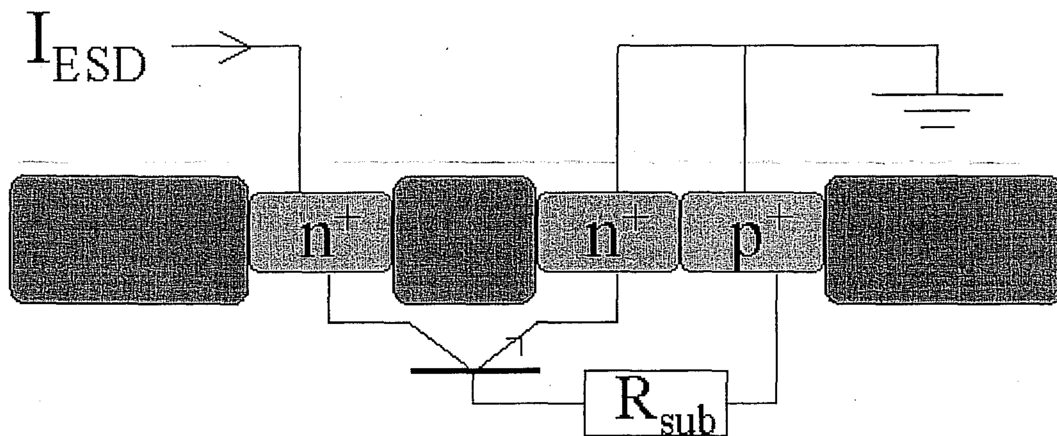

Figure 17 – Cross section of a Thick Field Oxide device (TFO) [14].

The TLP I-V and leakage curves for the TFO are shown in figure 18. All the ESD parameters defined for the NMOS ESD protection device are applicable for TFOs. The device has a trigger voltage (Vt1) of 13.4V, a snap-back voltage (Vsp) of 7V, an on-resistance of 10 ohms and a (Vt2, It2) point of (19V, 1.5A). Comparing this curve to the NMOS curve in figure 15 reveals some interesting data. The It2 value is twice as large for the TFO, even though the device width is less (80um vs 100um). The snap-back voltage (Vsp) is also larger as expected, 7.2V to 6.5V.

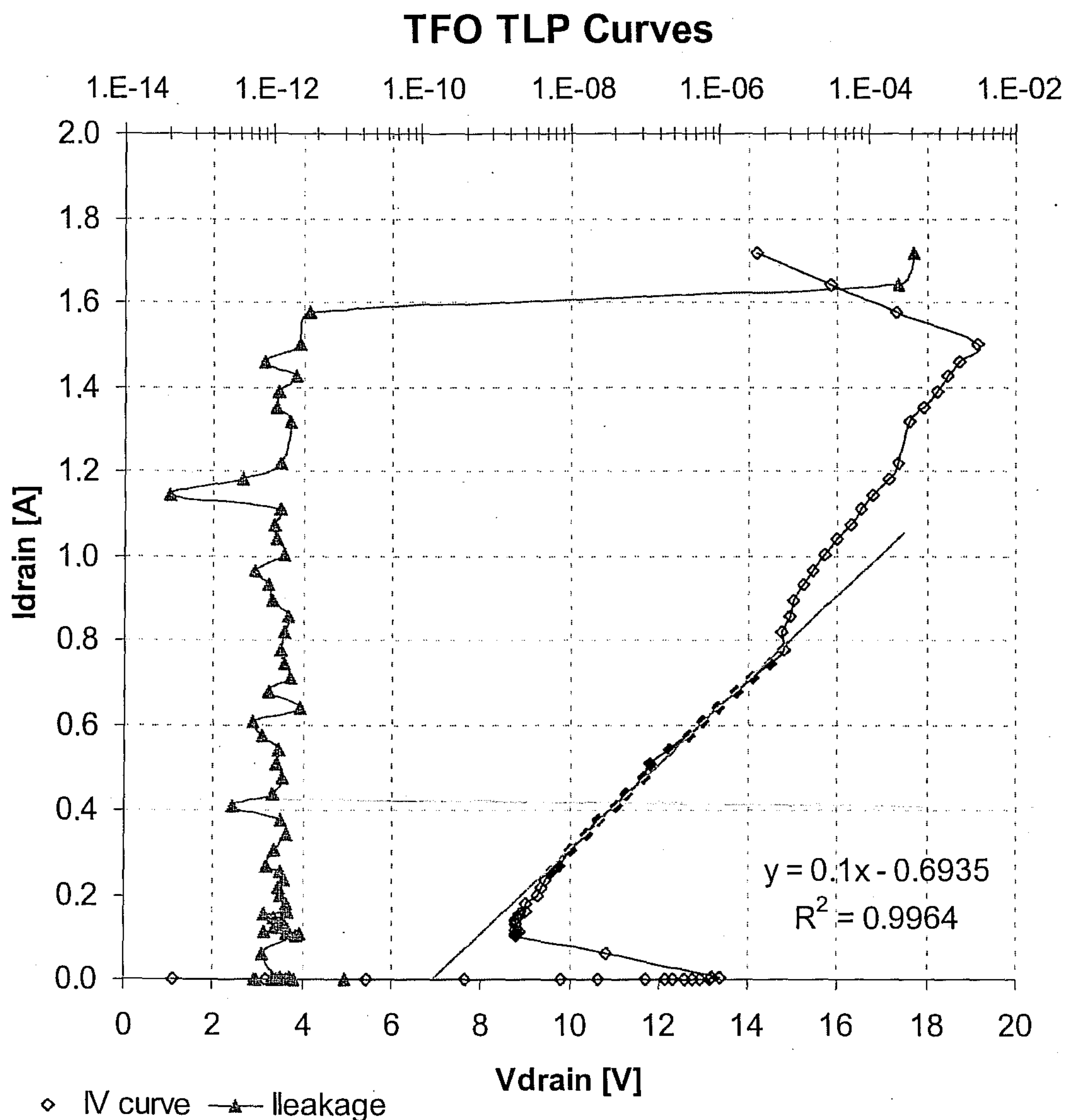

Figure 18 – TLP curves of a W=80um, L=2um TFO.

5.4 SILICON CONTROLLED RECTIFIER (SCR)

The most efficient ESD protection device, in terms of V/um, is the silicon controlled rectifier or SCR. Ironically, these devices have been the source of countless latch-up problems that have plagued CMOS processes since their inception. Properly designed, these devices can be safely implemented to provide excellent ESD performance at an acceptable latch-up risk.

Unlike NMOS devices, which are generally designed as multiple finger devices, SCRs are designed as a single finger device. Once an SCR triggers, the voltage snaps low very quickly, not allowing other fingers of the SCR to trigger. Fortunately, SCRs have high HBM performance such that a single finger device is sufficient. SCRs have a low clamp voltage (Vh) and low on-resistance (Ron), the reason for their high robustness per area. The drawback to the standard SCR is the unacceptably high self-trigger voltage. Self-triggering, for a standard SCR is enabled by the avalanche breakdown of the N-well/P-substrate junction. As these regions are both lightly doped, the breakdown voltage can exceed 20 V.

To reduce the self-trigger voltage of the standard SCR, two design variants have been developed. The first variant is the modified lateral SCR (MLSCR) shown in figure 19. A region of N+ "trigger" diffusion was placed across the N-well edge in between the anode (P+ in N-well) and the cathode (N+ in P-substrate) terminals. This trigger diffusion forms an N+/P-substrate junction electrically connected to the anode. The N+/P-substrate junction will avalanche at a lower voltage level than the N-well/P-well junction, thus lowering the trigger voltage of device. Once triggered, the device will operate as a standard SCR with current flowing from the anode (P+/N-well) to the cathode (N+/P-substrate). Not shown in figure 19 is the grounded P-substrate tap.

A slight enhancement to the MLSCR is the low voltage triggered SCR (LVTSCR). In this design the field oxide device formed between the N+ trigger diffusion and the grounded N+ cathode is replaced with a grounded gate NMOS device. The drain of the

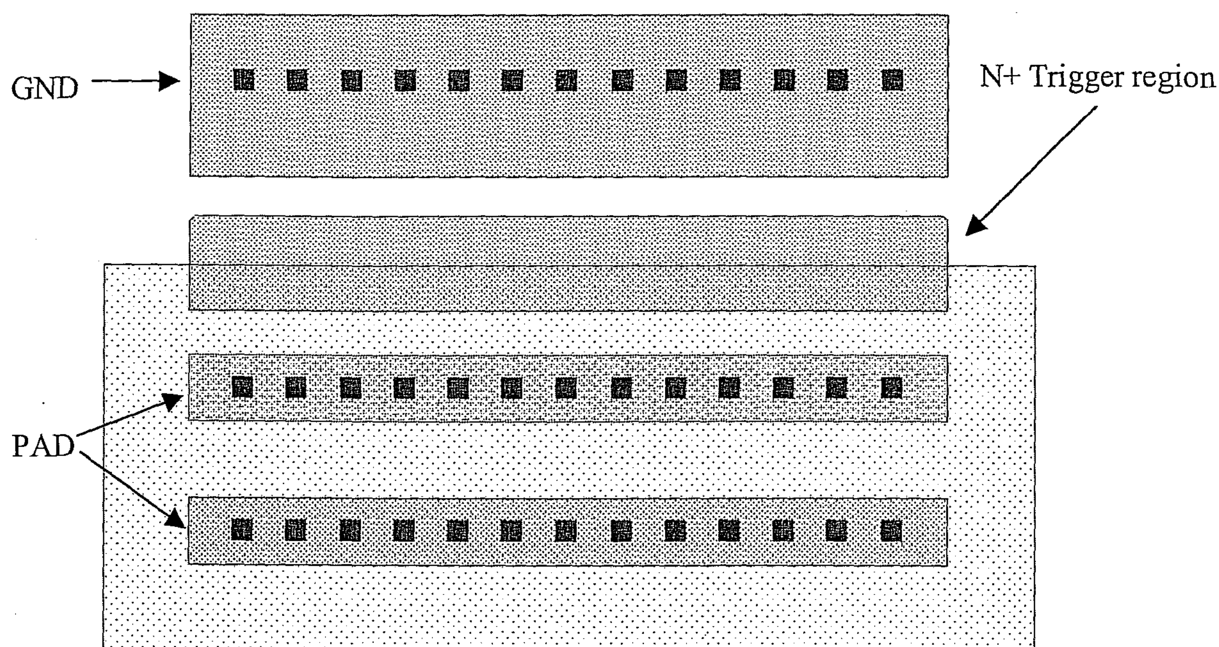

Figure 19 – Layout of a Modified Lateral SCR (MLSCR).

NMOS device is effectively the N+ trigger diffusion of the MLSCR and the source is the grounded N+ cathode. This device will be triggered by gated diode breakdown, which is often a few volts less than the avalanche breakdown voltage of the N+/P-well junction.

The basic SCR structure is unchanged in either the MLSCR or LVTSCR designs. Careful design practices should be followed to avoid the risk of latch-up in CMOS bulk processes. Due to the risk of latch-up, the use of SCRs for power supply pin protection is not recommended.

CHAPTER 6 - BASICS OF ON-CHIP ESD PROTECTION

6.1 PAD CELL DESIGN CHALLENGES

The design of bond pad cells presents an interesting challenge to designers. While most of the integrated circuit is designed for low current drive to reduce power consumption, the pad cell circuits must be designed to handle large currents and voltages. The pad cells are the exposed to the outside world and represent the only region on the integrated circuit where voltages and currents are uncontrolled. Excessive voltages, transient or DC (Direct Current), can be subjected to the bond pads. If the pulse duration is short, under a microsecond, the exposure is defined as ESD. If the pulse duration is long, over a microsecond, the exposure is defined as electrical overstress or EOS. Bond pad cells must be carefully designed to avoid latch-up due to output driver overshoot or undershoot signals. Proper guard rings are required to prevent latch-up, the triggering of parasitic NPN and PNP devices inherent to CMOS processes.

General guidelines for good ESD performance are:

- ESD is an electrothermal phenomenon with damage initiated by localized heating. To increase robustness, it is best to dissipate the power (i.e. heat) over a large area;

- ESD devices with lower power dissipation (i.e. lower clamp voltages and on-resistances) typically have higher ESD robustness;

- Place ESD devices close to the bond pad to prevent excessive voltages from reaching internal devices;

- ESD is about amps and ohms, the effective clamp voltage will also include the voltage drop across the interconnect between the ESD device and the pad.

6.2 CHARACTERISTIC OF GOOD ESD PROTECTION

There are four aspects to a successful ESD protection device or network [19]:

1. Robustness;
2. Effectiveness;
3. Speed;
4. Transparency.

Every ESD protection device must be properly designed to conduct the required ESD current without being damaged. The term "robustness" is used to characterize the ESD hardness of the protection device. If an ESD protection device is damaged due to an ESD event, the device would be classified as not having the required robustness. The only reason for introducing an ESD protection on to an integrated circuit is to protect functional devices. If functional device was to be damaged during an ESD event, the ESD device or network was ineffective. An effective ESD network must shunt the ESD current away from functional devices. Strongly related to the effectiveness is the speed of the protection device. An effective and robustness ESD protection device will not be successful if it reacts (i.e. triggers) slower than the functional devices in parallel. The ESD device should turn on faster, in voltage and in time, than the devices it is protecting. The last aspect of a successful ESD protection system is transparency. An ESD protection system should not adversely affect the functional performance of the integrated circuit. A gross example of this would be to design each bond pad with a large series resistor between the bond pad and internal circuitry. Although this scheme would meet the other three aspects of good ESD protection, the I/O and inputs would probably not achieve the speed requirements of the integrated circuit.

6.3 ESD PROTECTION NETWORK SCHEMES

ESD protection schemes are generally classified in two categories: pad-based networks and rail-based networks. Both protection schemes have been in use for some time, but pad-based methods have been the more popular method of the two.

Pad-based ESD protection schemes are designed to clamp the ESD voltage directly at the bond pad. This is often done with diodes and snap-back devices (NMOS snapback devices or an SCR). In Rail-based ESD protection schemes, the ESD current is directed to the power rails, where the ESD voltage is clamped. This method is implemented using diodes and active clamps, such as NMOS device. The diodes are placed at the bond pad and steer the ESD current to the power or ground rail. The power to ground active clamp ensures that the voltage drop across the rails is kept to a safe level. Dual diodes are used, namely a diode to power rail and a diode to the ground rail, and designed to operate in forward-bias mode. Active clamps are large NMOS devices operating in saturation and must be driven by a rise-time triggered circuitry. The major difference between pad-based and rail-based methods is the ESD approach to the NMOS output driver. In pad-based methods, this device is generally the primary ESD protection device. Every effort is made to design this device to be both effective and robust. In rail-based methods, this device is treated as the weak element in the ESD network. Every effort is made to keep this device from triggering.

Both protection schemes have their advantages and disadvantages. Pad-based networks can be difficult to design, due to the complexity involved in analytical modeling of the snap-back region of NMOS devices. Snap-back devices are also very process and wafer FAB dependent. An ESD test chip is typically required for each new CMOS process. Well designed pad-based networks typically will have higher ESD robustness than well designed rail-based networks, due to the large area required for active clamps. Pad-based networks are also less susceptible to the adverse effects of parasitic rail resistance. This research will focus on pad-based protection devices. This will include diodes, thick field oxide devices, NMOS snap-back devices and silicon controlled rectifiers (SCRs).

CHAPTER 7 - CMOS ESD TEST CHIP

To evaluate the performance of a 0.50um, double metal, double poly, N-well bulk CMOS process, an ESD test chip was designed, fabricated, assembled and characterized. The test chip consisted of three individual pad rings, each with 28 pads. Each pad ring contained two GND and two VCC pins, uniformly placed in the pad ring to minimize the effects of series metal interconnect resistance. The test chips: ESD01, ESD02 and ESD03; were assembled in 28-pin SOIC packages as shown in figure 20.

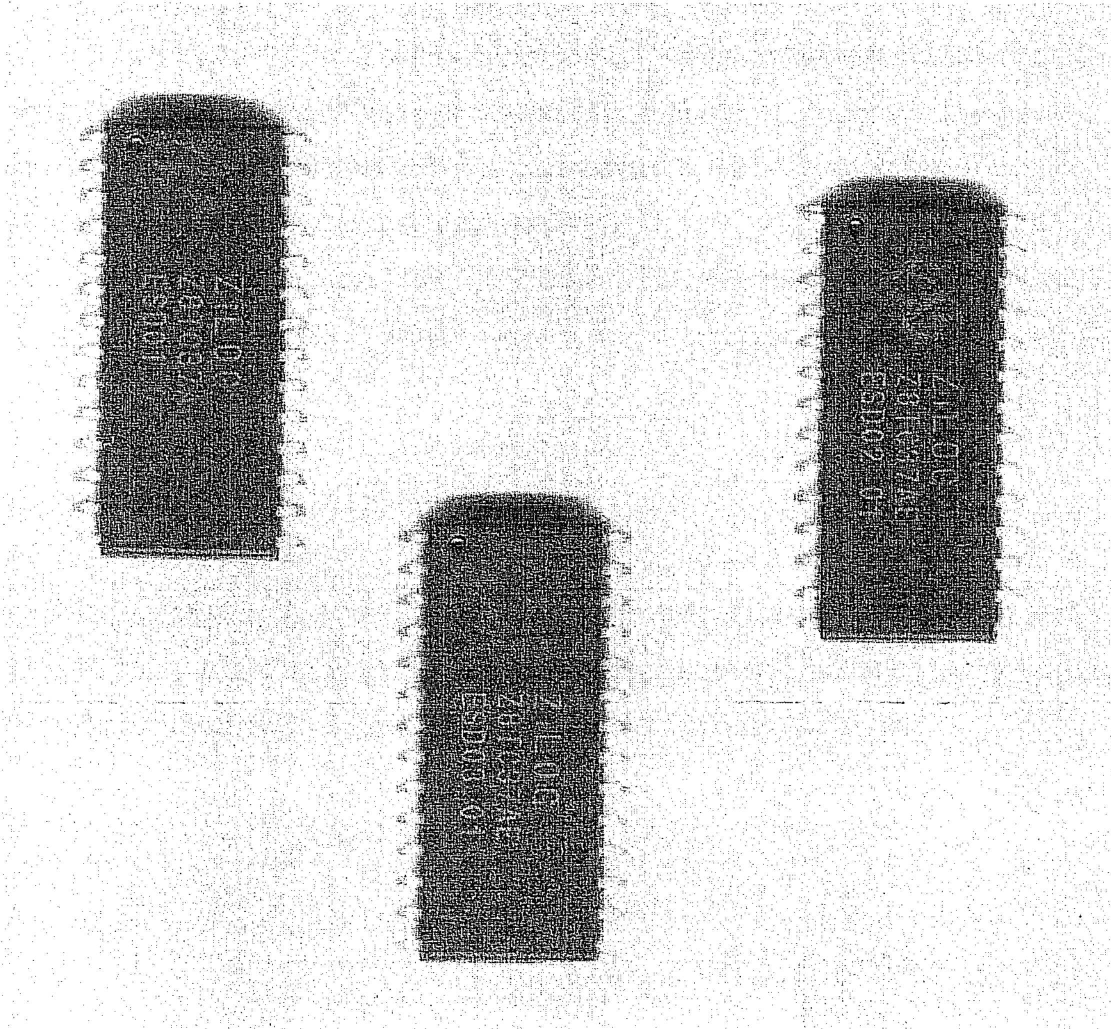

Figure 20 – ESD test chips assembled in a 28-pin SOIC package.

The process utilized retrograde N-wells. LOCUS field isolation, polycide gates and unsilicided diffusions. The gate oxide thickness was designed for reliable operation with a 5V power supply and is 12nm, nominally. The process uses aluminum (Al) interconnects using chemical mechanical polishing (CMP) with tungsten plug contacts and vias.

The devices were ESD tested using the HBM (Human Body Model) method, using junction leakage as the failure criteria. An ESD stress (i.e. a VZAP) consisted of three pulses of the same polarity with a one second delay between each pulse, in accordance with the Mil-Std 803 – Method 3015.7. After each VZAP the junction leakage was measured using a Tektronix 575 series curve tracer. The failure criteria was set to 5uA, or greater, of leakage with an applied voltage of 0.5V. The initial test voltage was set to 200V. Each pin was subjected to the VZAP series of pulses, measured and compared against the failure criteria. For each failing pin, the HBM test voltage and measured leakage currents were recorded. Once all pins were tested, the voltage was incremented to the next voltage step and all passing pins were tested to the next higher voltage. This procedure continues until all pins fail or the maximum test voltage, 10kV, is reached. Between 200V and 2kV, 200V steps were used. From 2kV to 10kV, the voltage step was increased to 500V.

To aide in the analysis of the various test structures, each unit was HBM tested to a single test condition under a single pulse polarity. Table 4 provides a list of the test conditions for each unit tested. This research will concentrate on the condition 1 results under positive polarity. The power supply pins were not included in the condition 1 or condition 2 tests. All of the HBM testing was done using an IMCS-700 manual system at an offshore facility. A few of the units were tested under my direct supervision.

Test Cond	# units	Description
1+	1	All pins to GND, + polarity
1+	3	All pins to GND, + polarity
2+	1	All pins to VDD, + polarity
2 -	1	All pins to VDD, - polarity

Table 4 – HBM test conditions for the ESD test chip.

Many of the structures were analyzed using TLP (transmission line pulse). The TLP measurements were at the package level, using samples from the same assembly lot as the units tested under HBM. The TLP testing failure criteria was defined as a significant increase in leakage current or a dramatic change in the I-V curve. The TLP testing was done with 100ns pulses using a 10ns rise time. After each TLP pulse, the junction leakage current was measured with an applied voltage of 0.5V.

7.1 DIODE TEST STRUCTURES

Five different diode structures were designed on the ESD02 module. Each pad contained an N+/P-substrate diode to the GND rail and a complementary P+/N-well diode to the VDD rail. The two diodes have identical layouts. The diodes were designed with different area and perimeter (PER) values as shown in table 5. All of the N+/P-substrate diodes were designed with N-wells placed under the N+ contacts, except for DIO-5 where the N-wells were omitted.

Only four layout parameters were investigated on the diode structures: area, perimeter, layout style (i.e. block or finger) and N-wells under the N+ contacts. The smallest diode, DIO-1, was designed in a block style with an area of 25um^2 and a perimeter of 20um. DIO-2 was also designed in a block style with twice the area as DIO-1, with only a slight increase in perimeter. DIO-5 is identical to DIO-2, without the N-wells under the N+ contacts. The P+/N-well DIO-2 and DIO-5 devices are identical. DIO-3 was designed to have the identical area, but a larger perimeter than DIO-4, designed using the finger style. The test diode layouts are shown in figure 21.

NAME	Chip-pin#	DESCRIPTION	AREA [um^2]	PER [um]	PER2 [um]
DIO-1	E02 #04	Block style	25.0	20.0	-
DIO-2	E02 #03	Block style	51.8	28.8	-
DIO-3	E02 #02	3 Fingers *	1275.0	351.0	100.0
DIO-4	E02 #27	Block style *	1274.5	142.8	71.4
DIO-5	E02 #26	Block style- No Nwl	51.8	28.8	-

Table 5 – Description of diode test devices.

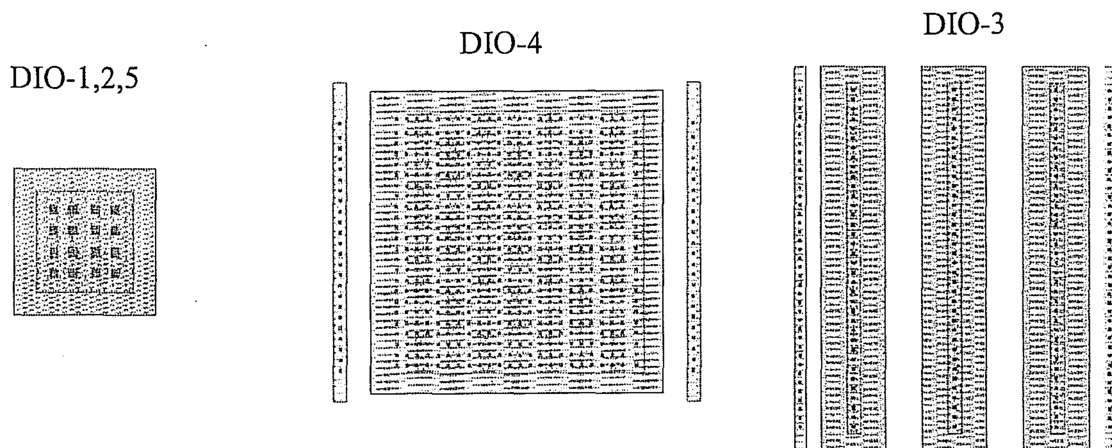

Figure 21 – Diode layout styles used on the test chip.

Due to a design error, the placement of the substrate and N-well taps was not consistent. As shown in figure 21, taps were located near some of the diffusion edges on DIO-3 and DIO-4; but quite far away, about 30um, from the edges of DIO-1, DIO-2 and DIO-5. The PER2 parameter was added to table 5 to indicate the diode edge in close proximity to a tap. No value is given for DIO-1, DIO-2 or DIO-3 as the diffusion edge to tap space is very large.

The objective of the diode test structures was to characterize each diode type under forward and reverse bias conditions. The P+/N-well diodes would be tested to the VCC pin and the N+/P-substrate diodes tested to the GND pin. The results of the diodes would be compared to evaluate the impact of the various layout parameters on the diode I-V curve.

The HBM results under condition 1+ and condition 2+ are listed in table 6 and graphically displayed in figure 22. The condition 1+ measurements were done on four units with a positive polarity pulses applied to the pins with the GND pin tied common. The condition 2+ tests were done on one unit with the VCC pin tied common. The average failing voltage, along with the individual data points for each unit are shown. As expected, the larger diodes, in area and perimeter (DIO-3 and DIO-5), had the higher ESD results.

Cond 1+		HBM fail voltage [kV] Cond 1+					Cond 2+
NAME	Chip-pin#	AVG	B1	B2			D
DIO-1	E02 #04	1.45	1.4	1.6	1.4	1.4	1.4
DIO-2	E02 #03	3.25	5.0	2.0	2.5	3.5	5.0
DIO-3	E02 #02	10.00	10.0	10.0	10.0	10.0	10.0
DIO-4	E02 #27	9.88	10.0	9.5	10.0	10.0	10.0
DIO-5	E02 #26	5.38	6.0	4.0	6.0	5.5	5.5

Table 6 – Cond 1+ and Cond 2+ diode HBM results.

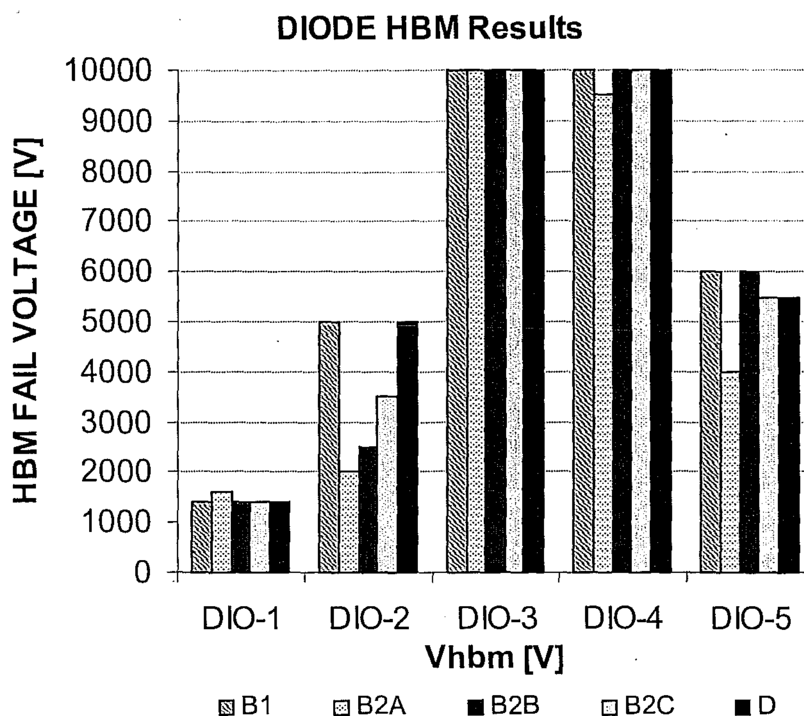

Figure 22 –HBM diode results for Cond 1+ and Cond 2+.

The B1, B2A, B2B and B2C bars represent the ESD results of the condition 1+ units, while the D bars represent the condition 2+ results. The high ESD performance under condition 1+ was not expected. The condition 1+ units (B set) were expected to have low ESD performance as the primary conduction path was anticipated to be through the N+/P-substrate diodes under reverse breakdown. The condition 2+ units (D) were expected to have high ESD performance as the primary conduction path was anticipated to be the P+/N-well diode under forward bias. As comparable performance is observed for both test conditions,

the same primary conduction path may exist for both test conditions. It is appropriate to note that all of the DIO-3 devices and majority of the DIO-4 devices, 3 out of 4 samples, did not meet the failure criteria at the maximum HBM test voltage, 10kV.

The schematic for the diode test structures is shown in figure 23. This schematic includes the complementary diodes (D1 and D2) directly connected to the pad, the parasitic vertical PNP (Qvpnp) inherent to the P+/N-well diode, the supply bus resistances (Rvdd, Rvss1 and Rvss2) and the power supply NMOS clamp (M1). During the condition 1+ (pad to GND pin) HBM test, three possible paths exist for the ESD current. Path A is the path through the reverse biased diode (D1). Path B is through the forward biased diode (D2), along the VDD rail and across the power supply NMOS clamp (M1). Path C is through the vertical PNP device, created by the P+ drain connected to the pad, the N-well and the grounded P-substrate.

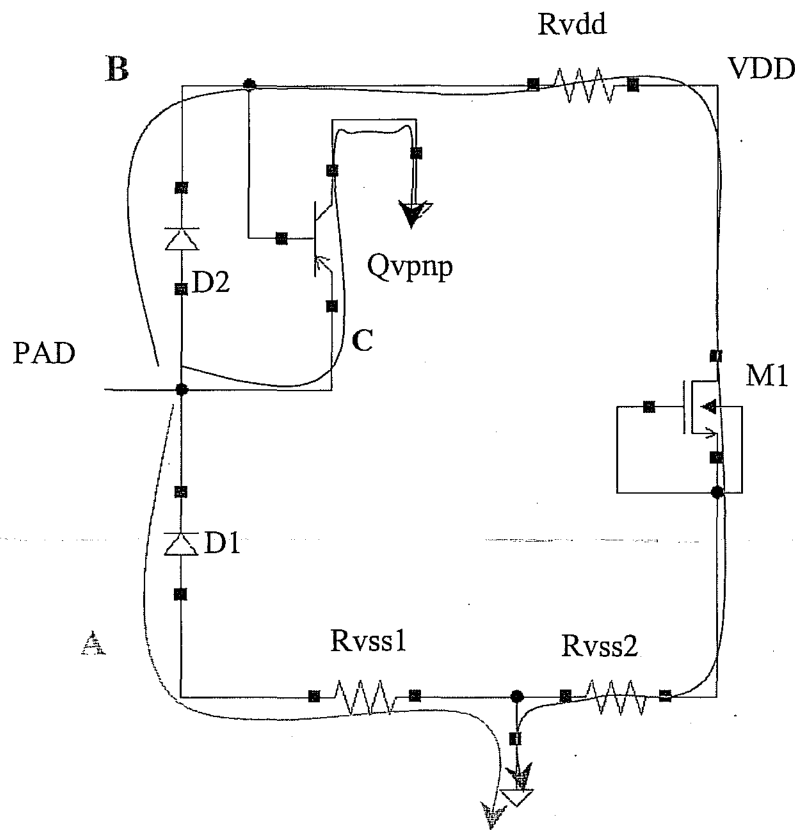

Figure 23 - Complete Diode test circuit schematic.

The presence of the power supply clamp (M1), creates the parallel paths B and C. With the power clamp removed, the impedance between the VDD and GND rails would be very high and almost no current would flow through path B. Path C would still exist with the power clamp removed, but without current path B the vertical PNP (Qvpnp) would not have sufficient base current to conduct a measurable amount of ESD current.

The TLP curves for all five diodes are shown in figure 24. The measurements were taken by applying the TLP pulses to the diode test pins with the GND pin common. All of the I-V curves are observed to have very high effective built-in voltages (Vbi). For DIO-3 and DIO-4, the effective built-in voltages are about 6V, compared to about 11V for DIO-1, DIO-2 and DIO-5. The effects of the large intrinsic space on DIO-1, DIO-2 and DIO-5 are also shown. As expected, the diode with the highest perimeter, DIO-3, had the best clamp voltage and the diode with the lowest perimeter, DIO-1, had the highest clamp voltage.

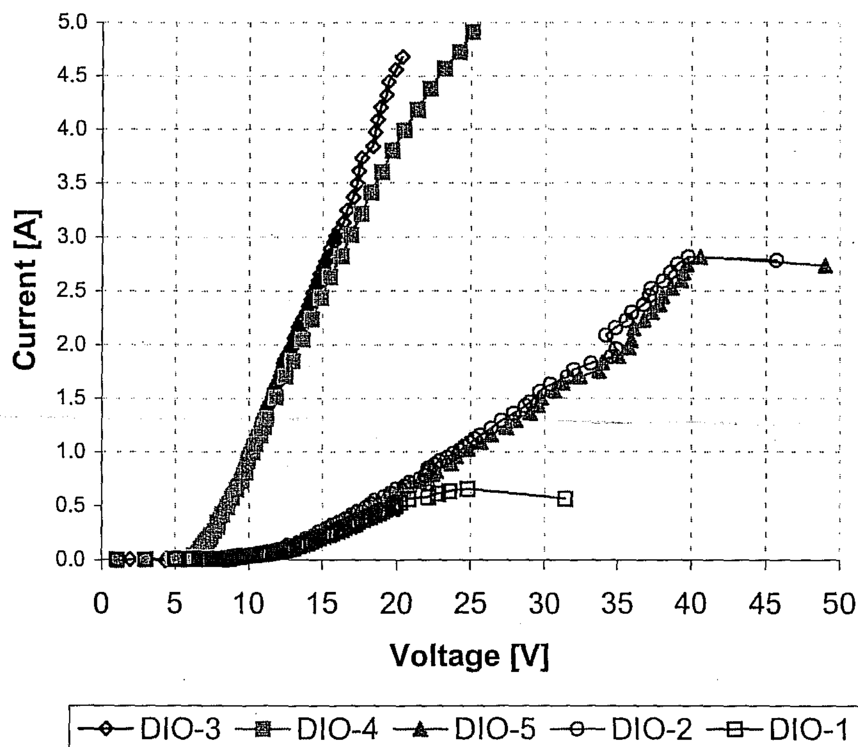

Figure 24 – TLP curves of Diodes to the GND pin.

The I-V curves for DIO-1 and DIO-5, to both the GND and VDD pins, are shown in figure 25. A voltage offset is observed between the I-V curves to the GND pins compared to the I-V curves to the VDD pins, labeled “A” and “B” in the figure. The voltage offset for DIO-4 (“A”) and DIO-1 (“B”) is about 6V and 6.5V respectively. These values are close to the NMOS snap-back voltage in this process. An analysis of the NMOS devices will be discussed in section 7.3. This voltage offset is expected to increase at higher currents, due to the on-resistance of the supply clamp (M1). The I-V curves to the VDD pins do show typical diode curves, with built-in voltages under 1V. These results do support the hypothesis that the primary current path, under both test conditions, is through the P+/N-well

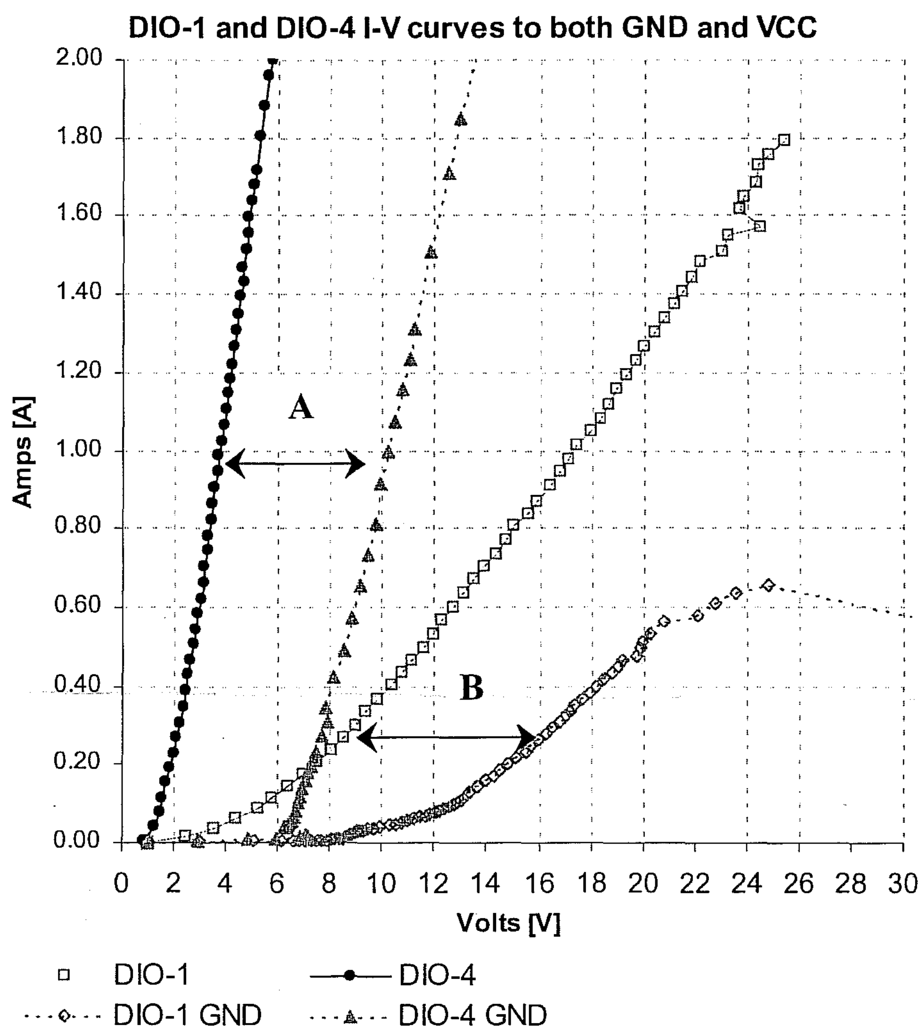

Figure 25 – IV curves of DIO-1 and DIO-4 to the GND and VCC pins.

diodes under forward bias. Under condition 2+, the path only includes the P+/N-well diode, while under condition 1+, the path includes the P+/N-well diode and the NMOS power supply clamp (M1).

Due to the presence of the parasitic paths, neither diode type can be accurately characterized under reverse biased conditions. Only the P+/N-well diodes will be characterized under forward bias. The test structures will be limited to DIO-4 and DIO-5. The N+/P-substrate diodes are still present in the circuit and may impact the results if the pad voltage exceeds 13V, the breakdown voltage of the N+/P-substrate junctions.

The forward-bias I-V and leakage curves for DIO-4 and DIO-5 are shown in figure 26. The larger diode, DIO-4, is able to handle TLP currents up to 7.4A, while DIO-5 was

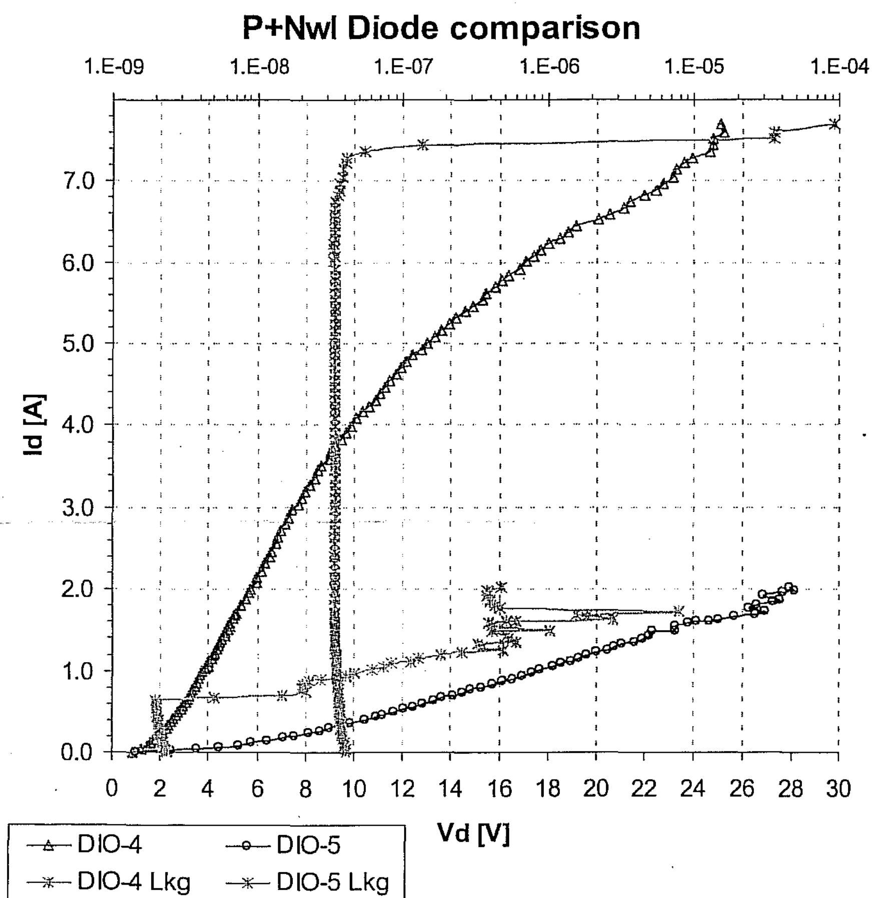

Figure 26 – TLP curves of DIO-1 and DIO-4 to the VCC pin.

found to fail at a TLP current of 1.6A. For both diodes the voltage at the point of failure was greater than 13V, indicating current flow in the N+/P-substrate diode. Neither I-V curve is observed to have a noticeable change in on-resistance at 13V, suggesting that very little current is flowing through the reverse-biased N+/P-substrate diode.

The TLP results are summarized in table 7. The current rating of the diodes, It2p, were calculated by dividing the It2 value by the perimeter. Both devices were found to have a current rating exceeding 50mA/um. The large diode, DIO-4, was found to have an on-resistance (Ron) of 1.98 ohms and a clamp voltage (Vclamp) of 1.8V. In contrast, the small diode, DIO-5, had an on-resistance of 11.3 ohms and a clamp voltage of 6V. Both parameters are believed to negatively affected by the large N-well intrinsic space, the space between the anode and the N-well tap. For the large diode, the on-resistance was calculated for current values under 4A. Above 4A, the on resistance was observed to increase. This region of operation has not been investigated.

NAME	TC - Pin#	Perimeter [um]	It2 [A]	It2p [mA/um]	Vclamp [V]	Ron [ohms]
DIO-4	ESD02-27	142.8	7.4	51.8	1.8	1.98
DIO-5	ESD02-26	28.80	1.6	55.6	6.0	11.3

Table 7 –TLP summary of P+/N-well diodes.

7.2 Thick Field Oxide devices (TFOs)

Various TFO ESD protection elements were designed on the test chip. The primary layout parameters are the device width (W), the channel length (L) and the contact to channel spacing (CC). The channel length of the device is defined as the diffusion to diffusion space. The devices were designed with a double row of contacts and a metal "gate" connected to the drain terminal, as shown in the TFO layout in figure 27. For added device hardness to EOS and ESD stress, N-well contact plugs were added below the drain contacts. It is observed that contacts are not placed along the entire width of the device. The effective width, W_{eff}, is defined as the width of the row of contacts [20], which will always be less than the diffusion width. Removing the contacts at the edge of the device decreases the possibility of ESD current flow in a direction away from the channel, perhaps through a parasitic device. This definition is required as most of the current is expected to flow in the region directly between the drain and source contacts. One layout parameter not investigated was the space between the N+ diffusion and the P+ substrate tap.

The design matrix for the TFO device was centered around an 80um wide (W) device, with a 2um channel length (L) and a 5um contact to channel (CC) space. The devices were HBM tested and TLP characterized under Condition 1+, positive polarity referenced to the GND pin. The devices are expected to operate in snap-back under this test condition.

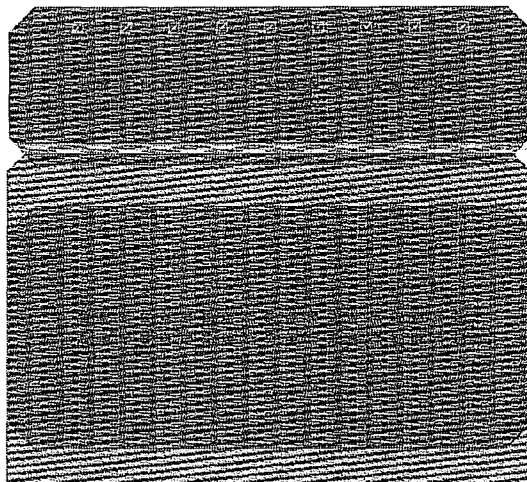

Figure 27 – Layout of 25um wide TFO with the Metal "gate".

7.2.1 Width Parameter analyzed

The first layout parameter analyzed was the width of the thick field oxide device. Three devices of widths 25, 50 and 80um were designed. All of the devices had a channel length (L) of 2.0um and a Contact to Channel (CC) space of 5.0um.

The values listed in table 8 are the HBM failing voltages for the condition 1+ test. Condition 1+ is the HBM test to the GND pin with a positive polarity pulse. Under Condition 1+, the device is expected to conduct current in bipolar snap-back mode between the drain and the source. The results are shown in the bar graph in figure 28. As expected the wider devices were observed to have higher HBM performance.

TC - Pin#	Width	B1	B2A	B2B	B2C	AVG
	[um]	[V]	[V]	[V]	[V]	[V]
ESD02-11	25	3500	3500	1800	3500	3075
ESD02-10	50	4500	6000	2500	6000	4750
ESD02-09	80	6500	5500	8000	7500	6875

Table 8 – W TFO Cond 1+ HBM results.

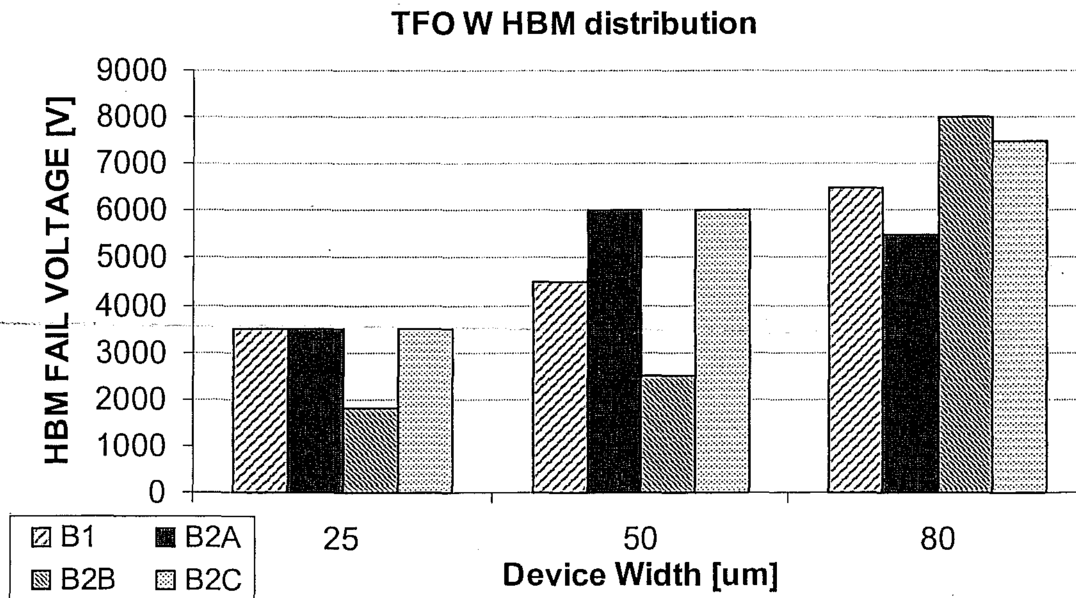

Figure 28 – W TFO Cond 1+ distribution bar graph.

An important factor is the width normalized HBM rating of the device, Vhbm. This parameter is the ESD failing voltage divided by the effective width (Weff). The parameter has units of Volts per unit width (V/um).

In table 9, the maximum and minimum HBM ratings have been calculated for each device. The minimum ratings are calculated using the lowest HBM passing voltage and the maximum ratings are calculated using the highest HBM threshold voltage. The 25um wide device was reported to have a much larger HBM rating, roughly 190V/um. The reason for this higher rating is not known. One hypothesis for this higher rating is that the TFO is not catastrophically damaged once the device enters second breakdown.

The TLP I-V and leakage waveforms for three identical 25um wide TFOs are shown in figure 29. The I-V curves are using open symbols as data point markers and the leakage measurements are using a filled or solid version of the same symbol. The The It2 values, as defined by the kink in the I-V curve, are observed to have about the same value, just under 400mA. In contrast, the leakage measurements of the three devices are not consistent. The It2 values, as defined by junction leakage, for the devices would range from under 400mA to almost 700mA. Although an increase in junction leakage is observed, none of the devices were found to exceed the HBM leakage failure criterion of 5uA. During the TLP testing, the I-V curves provided strong evidence that the device under test had entered second breakdown, thus, the TLP testing was halted before any device was found to exceed 1uA of leakage. For device A (green dashed line, triangles), the leakage is observed to remain at just under 1uA for the last seven data points.

			1+ HBM		HBM rating	
TC - Pin#	W	Weff	Min	Max	Min	Max
	[um]	[um]	[V]	[V]	[V/um]	[V/um]
ESD02-11	25	18.5	1600	3500	86	189
ESD02-10	50	43.5	2000	6000	46	138
ESD02-09	80	72.5	5000	8000	69	110

Table 9 –W TFO Cond 1+ HBM ratings

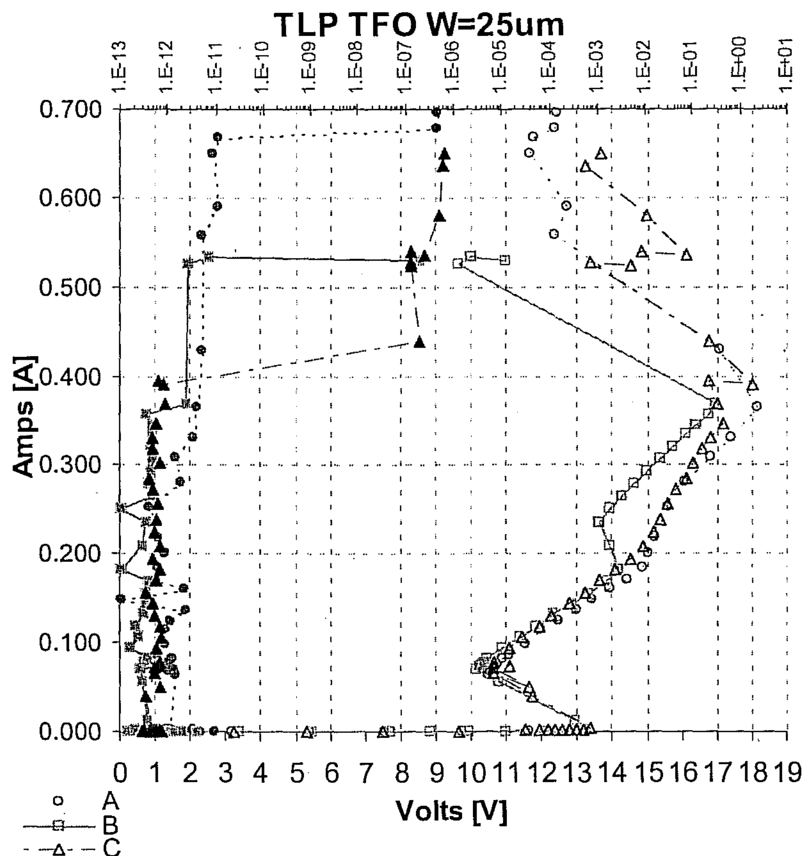

Figure 29 – 25um wide TFO TLP I-V curves.

The observation that TFO devices have been found to have an IV "kink", prior to a noticeable increase in junction leakage was also reported by R. Ashton of Agere [21]. This phenomena is most visible on device A, where the kink occurs at a current value of 380mA, but a noticeable increase in leakage current does not occur until a current level of 680mA. As the HBM testing was done manually, using a fixed leakage failure criterion of 5uA, leakage evolution data is not available.

The TLP I-V and leakage curves for the 50um and 80um wide devices can be found in figure 30 and figure 31, respectively. These devices, as with the 25um wide device, the TLP testing was halted due to I-V kink, suggesting the device entered second breakdown. Two devices were found to exceed the HBM failure criterion value of 5uA: 50um device B and 80um device B. The fact that these devices were conducting more current after entering second breakdown may explain the high HBM rating for all of the devices.

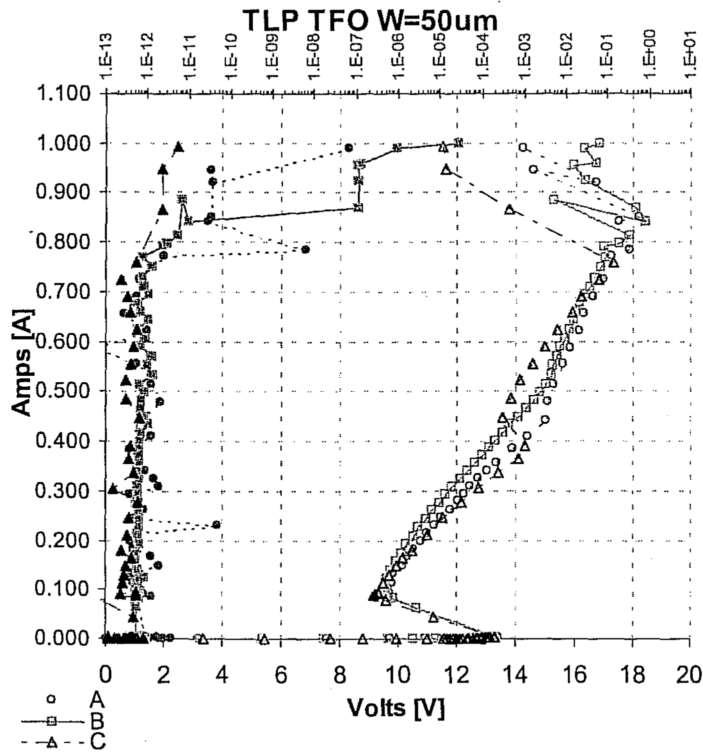

Figure 30 – 50um wide TFO TLP I-V curves.

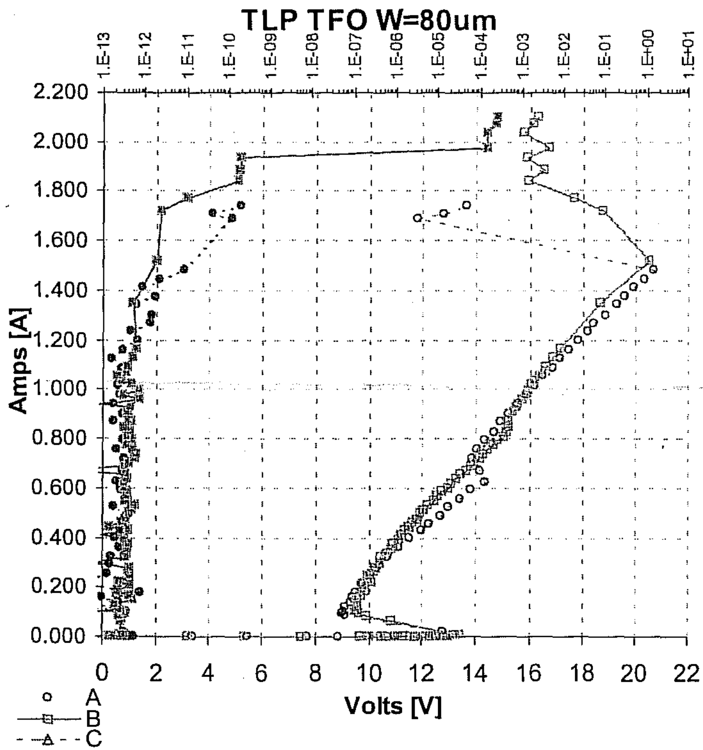

Figure 31 – 80um wide TFO TLP I-V curves.

The TLP parameters for the 25, 50 and 80um wide TFO devices are summarized in table 10. The trigger voltages (Vt1) are very consistent across all of the devices, ranging from a low of 13.3V to a high of 13.5V. Though difficult to see on the I-V plot, a very small step size (Vstep<=0.02V) was used to measure the trigger voltage. All of the dice in this experiment, both for HBM and TLP measurements, were taken from the same wafer. The exact wafer location for each sample was not recorded.

The snap-back voltage (Vsp) values were also found to be quite consistent, ranging from a low of 7.4V to a high of 7.9V. The device on-resistance (Ron) values decreased with the device width as expected. The 80um wide devices were found to have Ron values around 10 ohms, while the 25um wide devices were measured to have a Ron value of 37 ohms. These "effectiveness" parameters: Vt1, Vsp and Ron; can not be measured during HBM testing.

As shown in the TLP I-V plots, figures 29-31, the It2 values were identified by the "kink" second breakdown criteria. The normalized It2 values using Weff, seem to predict the It2 value better than the width driven normalized It2 (It2w). The It2p values range from a low of 18 mA/um to a high of 21.4 mA/um. The It2w values range from 14.6mA/um to 19mA/um.

TC - Pin #	W	Vt1	Vsp	It2	Ron	It2w	Weff	It2p
	[um]	[V]	[V]	[A]	[ohms]	[mA/um	[um]	[mA/um]
ESD02 -11a	25	13.4	7.8	0.365	37.9	14.6	18.5	19.7
ESD02 -11b	25	13.4	7.9	0.395	34.0	15.8	18.5	21.4
ESD02 -11c	25	13.3	7.4	0.369	37.6	14.8	18.5	19.9
ESD02 -10a	50	13.4	7.4	0.851	15.3	17.0	43.5	19.6
ESD02 -10b	50	13.4	7.6	0.842	14.3	16.8	43.5	19.4
ESD02 -10c	50	13.3	7.4	0.783	17.5	15.7	43.5	18.0
ESD02 -09a	80	13.4	7.9	1.52	8.6	19.0	72.5	21.0
ESD02 -09b	80	13.5	7.8	1.48	10.0	18.5	72.5	20.4

Table 10 – TLP Summary of TFO Width devices.

7.2.2 CC Parameter analyzed

The Contact to Channel space (CC) was varied from 0.25 to 5um with the channel length (L) and width (W) fixed at 2.0um and 80um respectively. The HBM results are summarized in table 11 and plotted in figure 32. The HBM thresholds are observed to increase as the CGS value increases, as expected. All of the devices do exhibit a large spread in the HBM results, similar to the TFO width devices.

The TLP I-V curves are shown in figure 33. The It2 values are also observed to increase with an increase in CC. The It2 values were determined by IV kink for all five devices. None of the leakage measurements, not shown in figure 33, displayed a significant increase around the I-V kink points. The TLP results are summarized in table 12.

TC - Pin#	CC	B1	B2A	B2B	B2C	AVG
	[um]	[V]	[V]	[V]	[V]	[V]
ESD03-23	0.25	3000	3000	1600	3000	2650
ESD03-24	1.50	3500	2000	7000	5000	4375
ESD03-20	2.50	3500	4000	5500	6500	4875
ESD03-19	3.50	7000	8000	5000	7500	6875
ESD02-09	5.00	6500	5500	8000	7500	6875

Table 11 – HBM results of TFO CC devices.

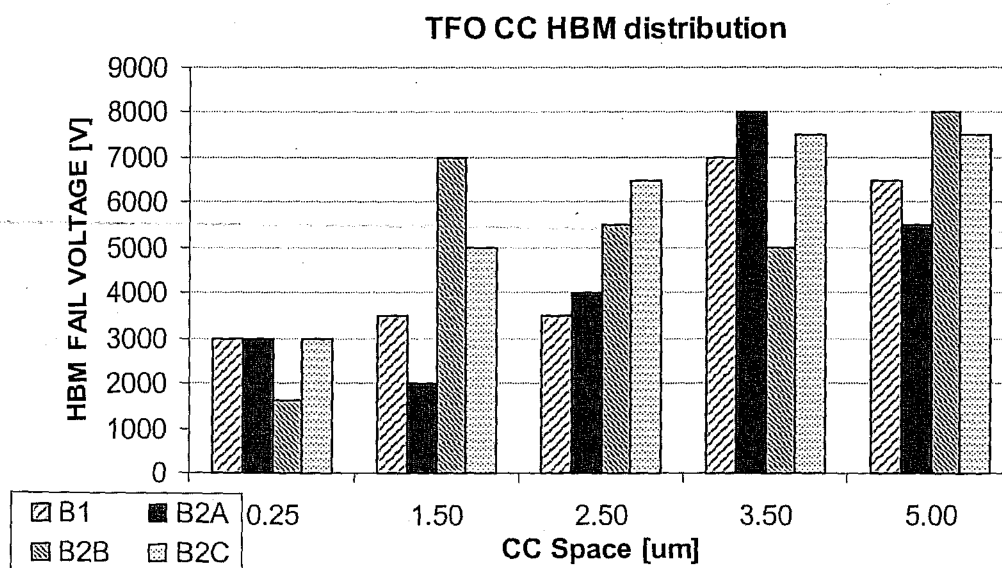

Figure 32 – HBM results of TFO CC devices.

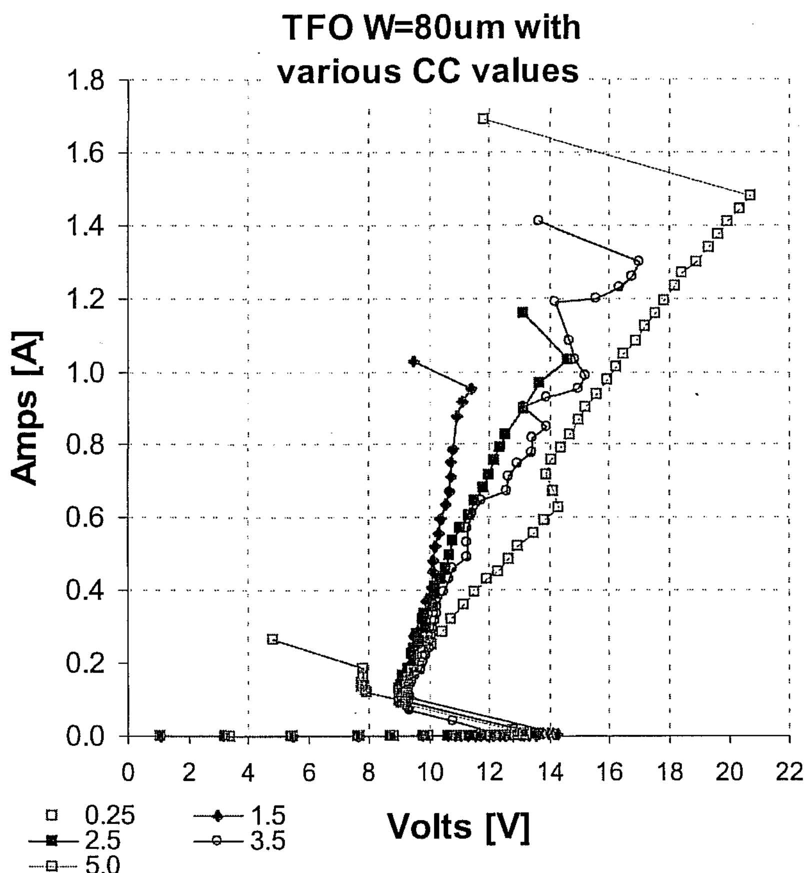

Figure 33 – TLP I-V curves for TFO CC devices.

TC Pin#	CC	Vt1	Vsp	It2	Ron	Weff	It2p
	[um]	[V]	[V]	[A]	[ohms]	[um]	[mA/um]
ESD03-23	0.25	13.6	7.62	0.188	1.15	72.5	2.6
ESD03-24	1.5	13.5	8.91	0.952	2.57	72.5	13.1
ESD03-20	2.5	13.2	8.32	1.03	5.01	72.5	14.2
ESD03-19	3.5	12.5	8.13	1.30	6.45	72.5	17.9
ESD02-09	5.0	13.5	7.80	1.48	9.97	72.5	20.4

Table 12 – TLP summary of TFO CC devices.

As all of the devices were 80um wide, the normalized It2, It2p, values also increase with an increase in and increase in the contact to channel (CC) space. The measured snap-back voltages are expected to decrease with an increase in on-resistance. The inherent snap-back voltage of the device, defined as Vsp0, is the snap-back of a device with zero on-resistance. This value is calculated by plotting Ron to the measured snap-back values, as shown in figure 34. The TLP parameters are summarized in table 12.

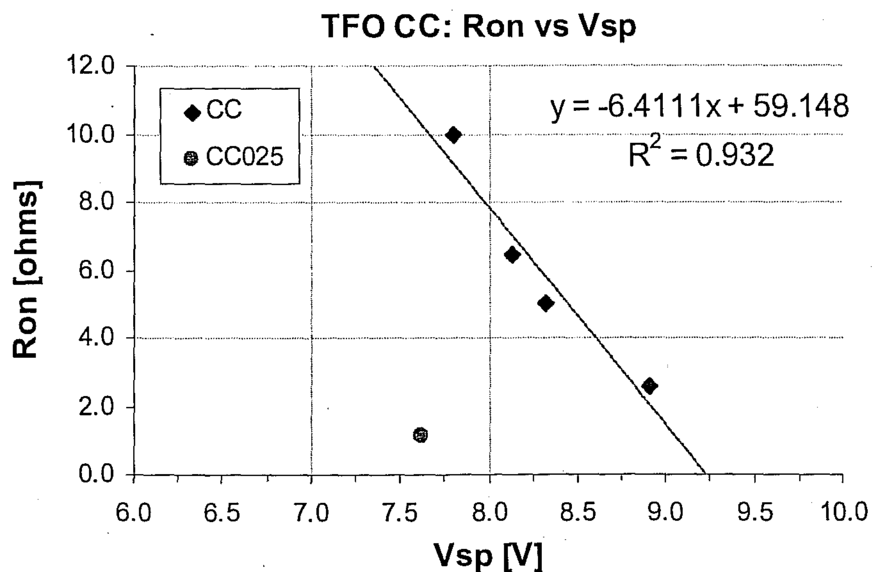

Figure 34 – Ron vs Vsp for the TFO CC devices.

Nearly all of the data falls along the linear regression line, with the only exception being the 0.25um CC device. The snap-back and on-resistance values of this device, indicated on the figure by the magenta circle. The 0.25 CC device as the lowest on-resistance value, 1.15 ohms, it is expected to have the highest snap-back value. The reason for the variance from the other devices is not known. The inherent snap-back voltage, Vsp0, is calculated as 9.23V.

The leakage evolution plots for the TLP measurements are shown in figure 35. The vertical bar represents the HBM failure criterion of 5uA of leakage. Only one of the devices, the 3.5um CC device, was observed to achieve that failure criteria. The other devices were found to have higher leakage currents at higher TLP currents, but the leakage values remained under 1uA, a typical data sheet I/O pin leakage parameter. This characteristic could be attributed to sub-surface breakdown [22], but this can not be confirmed without the samples examined with failure analysis. As the HBM samples were lost shortly after testing, failure analysis results are not available.

Sub-surface breakdown failures have described as being a second class of failures, separate from second breakdown induced catastrophic failures. One difference between these failures and sub-surface breakdown failures is the state of the TLP I-V curve. Sub-surface failure have been described as failures that cause slight increases in leakage currents, but are not detectable on the TLP I-V curve. A noticeable "kink" in each I-V curve can be seen in figure 33, indicating the devices did enter second breakdown.

A plausible hypothesis is that the device does enter second breakdown during the pulse, either HBM or TLP, but sufficient ballasting prevents the damage from being severe enough to cause large junction leakage currents. This hypothesis will be expanded upon during the analysis of the NMOS devices.

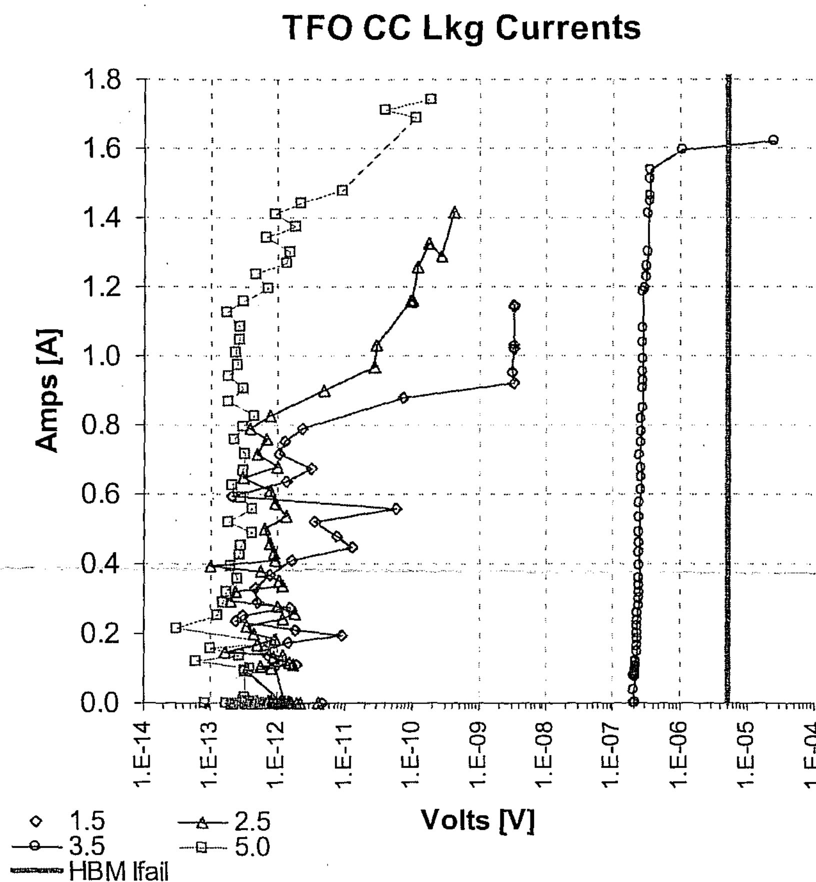

Figure 35 – TFO leakage evolution plot.

7.2.3 Length Parameter analyzed

The last TFO parameter investigated was the channel length. The channel length was varied from 0.875um, the process diffusion to diffusion space limit, to 2.0um. The other layout parameters were fixed, with the CC space set to 5um and the width (W) fixed at 80um.

The HBM results are listed in table 13 and displayed in figure 36. The HBM performance is high for nearly all of the devices, except for a 1.50um device found to fail at 3500V. Figure 36 does show some spread in the data, most noticeably on the devices with a longer channel length, longer than 1um.

TC - Pin#	Length [um]	B1 [V]	B2A [V]	B2B [V]	B2C [V]	AVG [V]
ESD03-10	0.875	7500	7500	7500	7500	7500
ESD03-11	1.00	7500	7500	7000	6500	7125
ESD03-12	1.25	8000	7000	7500	4500	6750
ESD03-13	1.50	6500	3500	7000	8000	6250
ESD02-09	2.00	6500	5500	8000	7500	6875

Table 13 – HBM results of TFO L devices.

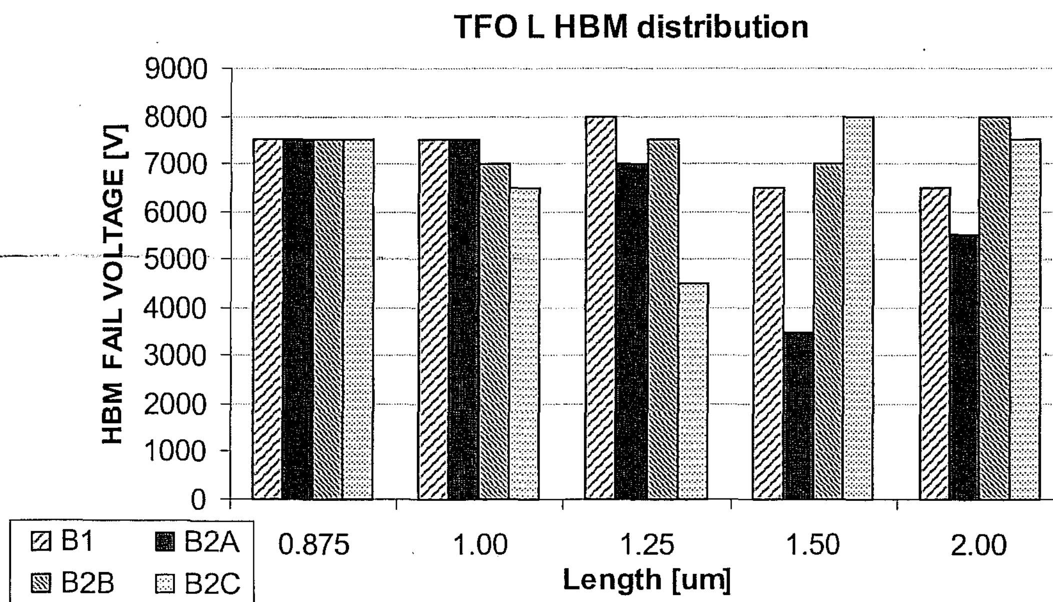

Figure 36 – HBM results of TFO L devices.

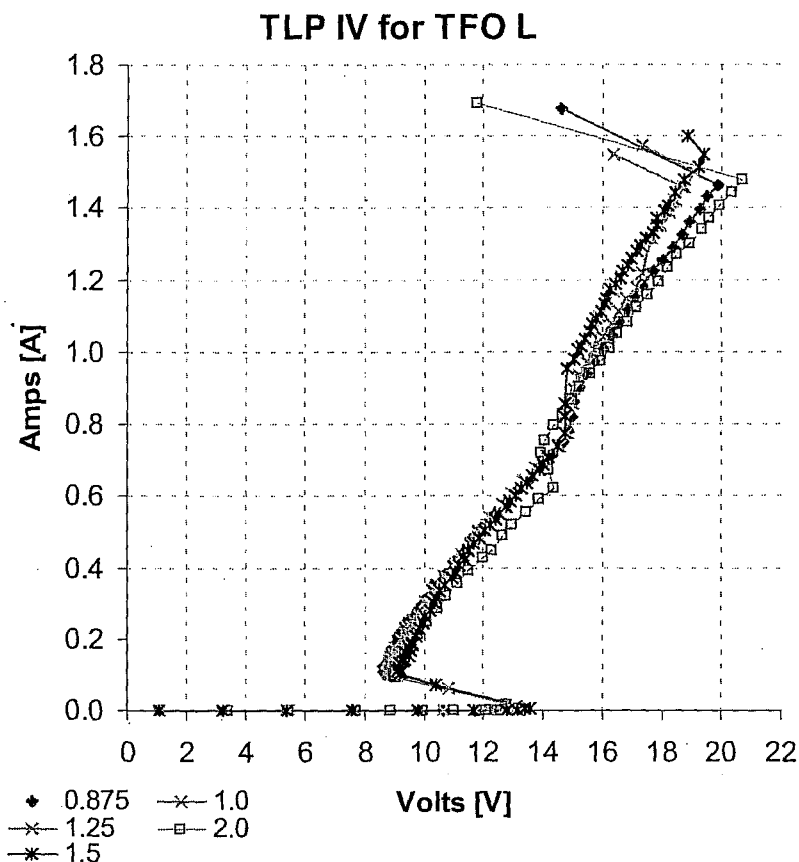

Figure 37 – TLP results of TFO L devices.

The TLP results of the TFO devices with various channel lengths are shown in figure 37. The It2 values, are expected to slightly decrease with an increase in channel length. The It2 values in figure 37 appear to be independent to the channel length. However, the range of channel lengths examined may not be large enough to detect a slight fall off of It2. The TLP parameters are summarized in table 14.

The trigger voltage for the 0.875um device appears to be slightly less the trigger voltages of the larger channel devices. The difference is only 0.2V and may not be sufficient. As expected the snap-back voltages does decrease with lower channel lengths. As all of these devices have the same width and contact to channel (CC) space, extracting the Vsp0 is not necessary. One interesting results is the apparent increase in on-resistance with a

TC- Pin#	L	Vt1	Vsp	It2	Ron	Weff	It2' eff
	[um]	[V]	[V]	[A]	[ohms]	[um]	[mA/um]
ESD03-10	0.875	13.2	6.95	1.46	10.1	72.5	20.1
ESD03-11	1.00	13.4	7.27	1.50	9.4	72.5	20.7
ESD03-12	1.25	13.5	7.57	1.46	9.0	72.5	20.1
ESD03-13	1.50	13.5	7.81	1.55	8.7	72.5	21.4
ESD02-09	2.00	13.4	7.86	1.48	8.6	72.5	20.4

Table 14 – TLP parameters of TFO L devices.

decrease in channel length. The on-resistance was expected to be independent of channel length. The reason for this on-resistance dependence on channel length is not known.

Nearly all of the TFO devices were found to have a slight kink in the TLP I-V curve around 14 to 15V. It is not known what is causing this kink, but appears as if an additional device is turning at this voltage. As all of the devices have N-wells under the drain contacts, which could create a second NPN device between the N-well and the N+ source. This device would have a longer channel length, resulting in a higher snap-back voltage. More research is needed to investigate this issue further. One possible experiments is to design a set of TFO devices with and without N-well contact plugs to see if the kink is visible on the devices without N-wells.

7.3 NMOS PROTECTION DEVICES

As NMOS devices operating in snap-back are the most widely used protection devices, a large array of NMOS test structures were designed on the test chip. The test array included devices with various widths (W), drain Contact-to-Gate Spacings (CGSd) and channel lengths (L). All of these devices were designed using two fingered devices with one common drain and two sources. To investigate the effects of non-uniform finger triggering, large devices with multiple fingers were also designed. The number of drain and source contacts were matched and perfectly aligned. The layout parameter matrix was centered around a "control" device designed with W=50um, L=0.65um and CGSd=4.0um. Most of the NMOS devices were designed with a gate bias circuit that actively ties the gate to ground with a voltage applied to VCC. This scheme has also been called a "floating gate" design.

The NMOS test structures also contain a complementary PMOS device to the VCC rail. The VCC rail contains an NMOS ESD device to the ground rail. This creates a parallel ESD current path through the parasitic P+/N-well diode, formed by the drain of the PMOS device. This shown in the circuit schematic in figure 38. Effectively, this is the same problem that was observed on the diode test structures. This path shunts current away from the device being tested and produces inflated HBM and TLP results. Fortunately, the supply protection device is larger than most of the devices being tested, such that the eventual failure is believed to occur on the device under test. Using the extracted on-resistance and snap-back values, Kirchoff's laws are used to calculate the amount of current flowing through the device under test at the secondary breakdown point (i.e. the predicted point of failure).

Device M1 is the NMOS device to be tested, M2 is the PMOS device to the VCC rail and M3 is the VCC to GND clamp. Current flow through the parasitic vertical PNP (PMOS drain/N-well/P-substrate) is expected be low due to very low current gain at high current densities. Current flow through the vertical PNP will be neglected in this analysis. Path A is the intended current path through the device under test and path B is the parallel path through the PMOS drain and body terminals and the power clamp (M3).

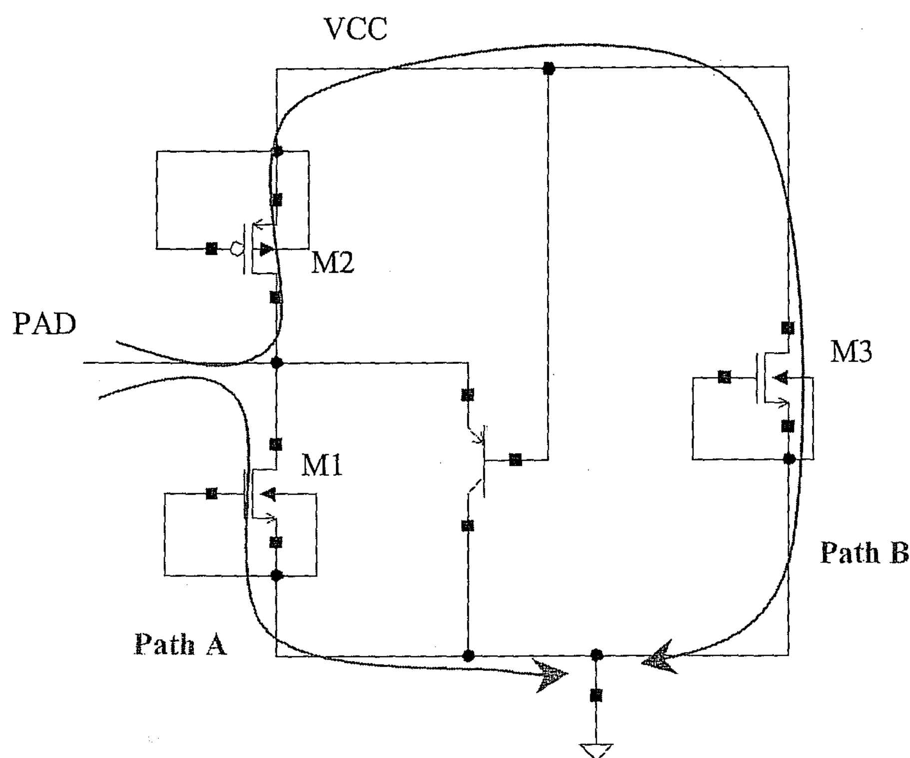

Figure 38 –Complete schematic for the NMOS devices.

Whether the power clamp (M3) conducts ESD current or not depends on the second breakdown voltage (Vt2) of the NMOS device under test (M1). If theVt2 value of M1 exceeds the trigger voltage of path B, path B will become conductive and shunt ESD current away from the device under test. The effective Vt1 of path B can be approximated by the trigger voltage of the power clamp (M3), plus a diode drop.

Due to the design flaw on the NMOS test structures, the analysis of each device will depend on the TLP I-V curve. Devices found to exhibit a second snap-back behavior, suggesting current flow in path B, will be treated as an ESD test circuit. For these circuits, the ESD current is expected to flow through both path A and path B, thus the HBM rating of the device is not known. Using Kirchoff's laws, the device It2 will be estimated based on the on resistance and snap-back values of the device under test and the devices in path B.

7.3.1 Width Parameter Analyzed

The width of the NMOS finger was the first layout parameter investigated. Using two finger structures, devices with total widths of 20, 50, 70, 100 and 140um were analyzed. The channel length was fixed at 0.65um and the Contact to Gate space (CGS) was set to 4.0um.

The reported HBM failing voltages, under Condition 1+, are shown in table 15. The HBM threshold values are higher than expected, suggesting that path B was conducting a significant amount of the HBM current. The TLP I-V curves in figure 39 are observed to have a second snap-back for all five devices, implying current flow in path B. As a result, these test structures will be analyzed as a circuit and the HBM threshold voltage will be compared to the measured TLP It2 current. From the TLP I-V curves, the on-resistance and snap-back parameters will be extracted for ESD circuit analysis. The circuit analysis will be done to estimate the TLP current flowing through the device under test at the point of failure, the device level It2 value.

The TLP I-V curves for all five devices are shown in figure 39. As suggested by the HBM results, each device exhibits a second snap-back at a voltage about a volt above the trigger voltage of the device under test. These snap-back points, marked with blue arrows and a code for the width of the device, indicate the point at which path B becomes conductive. With a parallel path conducting current, the circuit's effective on-resistance is reduced. Path B contains the large, 720um wide NMOS power clamp in series with the parasitic P+/N-well diode formed by the drain of the PMOS and the N-well.

Width	TC - Pin #	B1	B2 +1	B2 +2	B2 +3	Avg
[um]		[V]	[V]	[V]	[V]	[V]
20	ESD01-04	1600	1600	1400	1400	1500
50	ESD01-03	2000	2000	2500	3500	2500
70	ESD01-02	3000	2500	2500	2500	2625
100	ESD01-24	3500	3000	3500	3500	3375
140	ESD01-06	4000	3000	3000	3000	3250

Table 15 –HBM results of the NMOS W circuits.

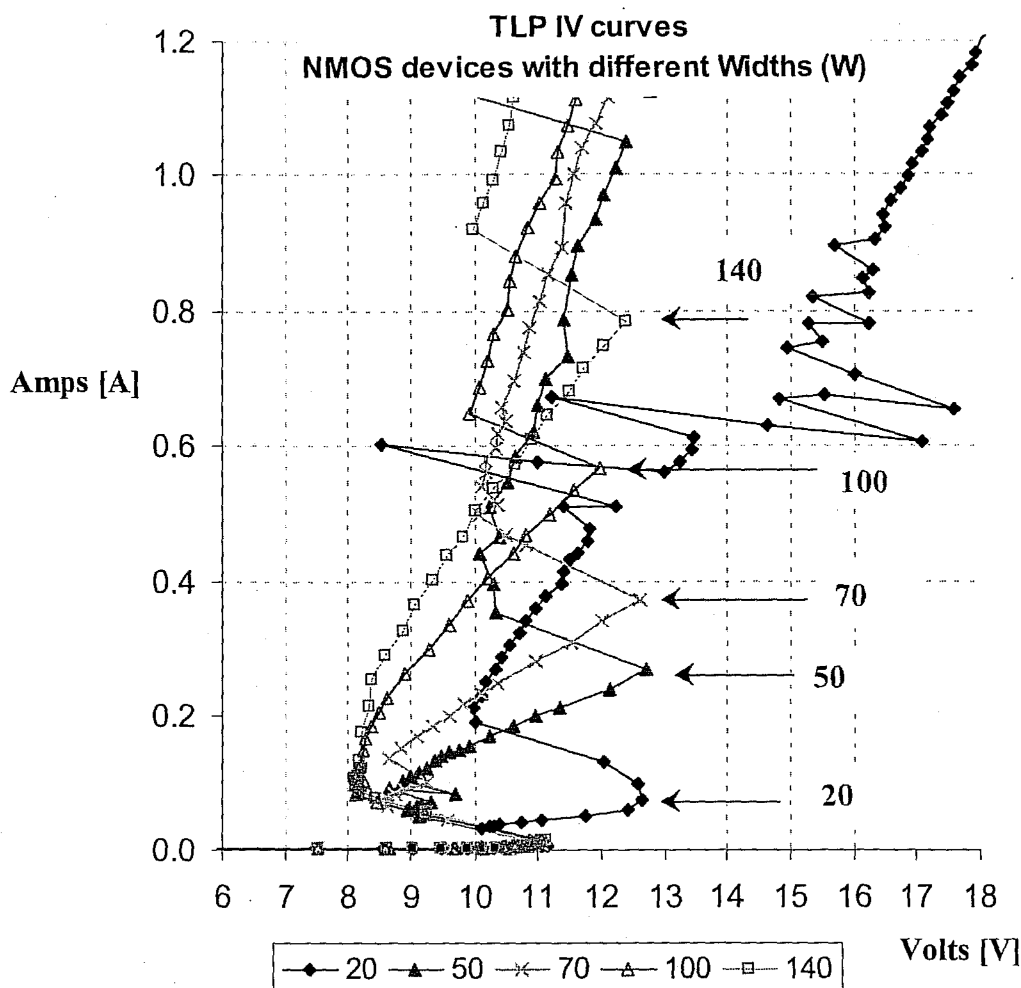

Figure 39 – W NMOS I-V with supply clamp trigger points.

					Circuit	Path B	device	device
W	TC - Pin #	Ron	Vsp	Vt1	It2	Vt1	It2	It2p
[um]		[ohms]	[V]	[V]	[A]	[V]	[A]	[mA/um]
20	ESD01-04	93.5	6.95	11.2	2.05	12.6	0.184	21.65
50	ESD01-03	26.3	5.73	11.0	1.45	12.7	0.327	8.49
70	ESD01-02	17.8	5.94	11.0	1.65	12.6	0.463	7.91
100	ESD01-24	9.72	6.25	11.0	1.65	12.0	0.722	8.16
140	ESD01-06	8.03	6.32	11.1	2.08	12.4	0.972	7.56

Table 16 – TLP results for W NMOS devices.

The TLP results are summarized in table 16. The on-resistance (Ron), snap-back voltage (Vsp) and trigger voltages (Vt1) are derived for the device under test prior to current conduction in path B.

The trigger voltage of path B is listed in the table as "Path B Vt1". The TLP current found to induce failure in the circuit, has been listed as "Circuit It2". The estimated It2 for the device is listed, calculated using the two path ESD circuit solved described in the appendix. Using the effective Width values, the width defined by the contact to contact distance, the normalized It2 value, It2p is also listed.

As expected, the on-resistance of the device is inversely proportional to the finger width. The on-resistance values range from 93.5 ohms to 8.03 ohms. The snap-back values range from 5.73 to 6.95V. With the exception of the 20um test structure, the snap-back voltage is observed to increase with finger width, or more appropriately, decrease with the measured on-resistance. The snap-back voltage has been defined as the holding voltage of the device at zero current. As a certain amount of current is necessary to put the device in bipolar mode, TLP I-V curves can't directly measure the snap-back voltage. Linear regression is used to extract the slope and x-axis intercept of the I-V curve in bipolar, or snap-back, mode. The effective snap-back voltage is determined for a theoretical device with no on-resistance. This value is determined by plotting the on-resistance vs the snap-back voltage as shown in figure 40. The effective snap-back voltage is 6.57V.

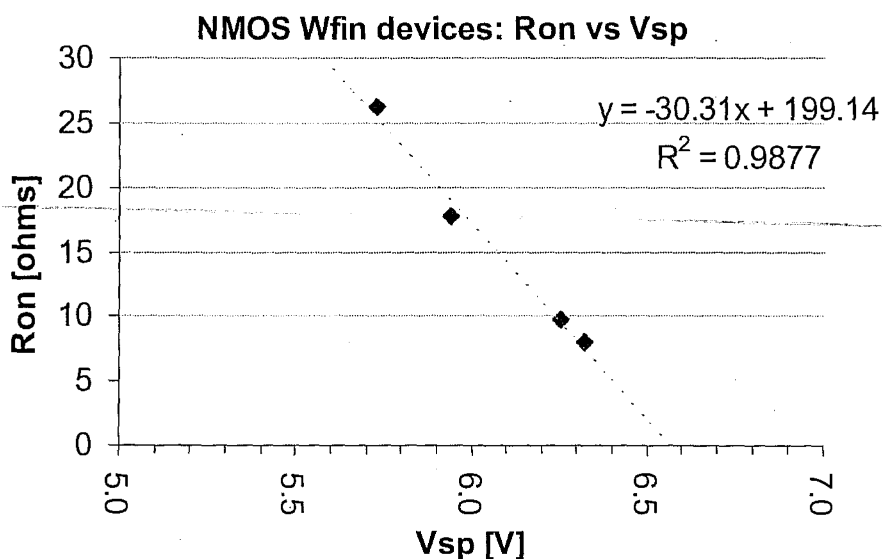

Figure 40 – Ron vs Vsp for various NMOS widths.

For the 20um test structure, only eight data points exist between the device trigger voltage (Vt1) and the trigger voltage of path B (Path B Vt1). This may be the reason that this device doesn't follow the trend of the wider devices (i.e. large Ron equates to lower Vsp). More data is needed to investigate this issue.

As expected, the device trigger voltage values were found to be independent of finger width. The trigger voltage was found to be between 11 and 11.1V for all devices. The path B trigger voltages (Path B Vt1) were found to be close to the same value for all of the devices, ranging from 12.0V to 12.7V. Measurement error is possible as the TLP voltage step size was somewhat large during this portion of the I-V curve. Devices measured in this region were expected to be in the bipolar mode and not experiencing a second snap-back event.

7.3.2 Multiple finger devices analyzed

Using 50um wide fingers, NMOS devices of 100, 200, 300 and 400um were analyzed. The channel length was fixed at 0.65um and the Contact to Gate space (CGS) was set to 4.0um. The Condition 1+ HBM results are shown in table 17. The HBM threshold values tend to increase with an increase in the number of fingers, effectively increasing the total width of the protection device.

The TLP I-V curves are shown in figure 41. All of the devices are observed to have a second snap-back at around 12V indicated with the blue solid arrows. The 200 and 300um devices are observed to have a potential uniform finger turn-on problem, evidenced by the the zig zag nature of the I-V curve after the second snap-back. The uniform finger turn-on problem may be inherent to the large NMOS VCC clamp as the zig zaging I-V curve occurs once the power clamp is triggered. The TLP results are summarized in table 18.

As expected the on-resistance decreases for wider devices. The snap-back voltages, however, are not as predictable as what was observed on the NMOS finger widths. The holding voltage for the 200, 300 and 400um devices is about 1.6V lower than that of the 100um device. The results suggest that a narrower channel length was used on the wider devices. A review of the layout confirmed that the channel length of devices was the same: 0.65um. The reason for this lower snap-back is not known. If the 100um wide device is ignored, the snap-back voltage does increase with a decreasing on-resistance. The trigger voltages are observed to slightly lower than the two fingered NMOS devices. The trigger voltages are still relatively consistent, ranging from 10.3 to 11V.

Width [um]	TC - Pin#	**B1 [V]**	**B2 +1 [V]**	**B2 +2 [V]**	**B2 +3 [V]**	**Avg [V]**
100	ESD01-24	3500	3000	3500	3500	3375
200	ESD01-23	4500	3500	4000	4000	4000
300	ESD01-05	4500	4500	5000	4000	4500
400	ESD01-20	5500	6000	5500	5000	5500

Table 17 – HBM results for Multiple Finger NMOS.

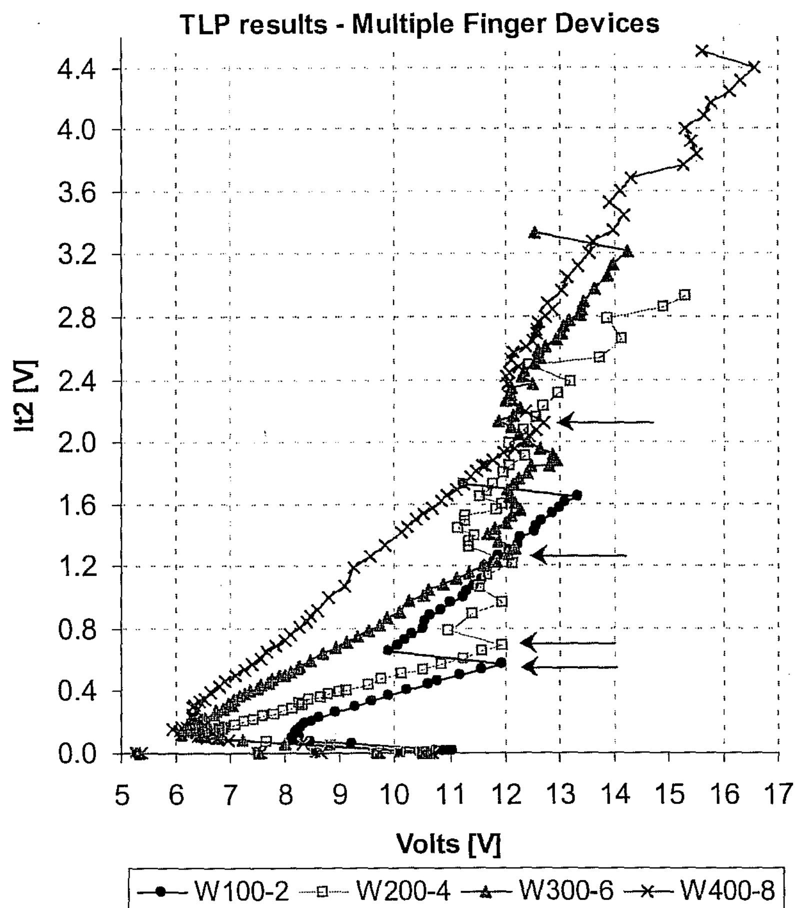

Figure 41 – TLP I-V curves for the FIN NMOS devices.

W	TC - Pin #	Ron	Vsp	Vt1	Circuit It2	Path B Vt1	device It2	device It2p
[um]		[ohms]	[V]	[V]	[A]	[V]	[A]	[mA/um]
100	ESD01-24	9.72	6.25	11.0	1.65	12.0	0.722	8.16
200	ESD01-23	7.12	5.29	10.3	2.91	12.3	1.450	8.19
300	ESD01-05	5.20	5.33	10.6	3.22	12.2	1.725	6.50
400	ESD01-20	3.34	5.43	10.7	4.32	12.7	3.056	8.63

Table 18 – TLP summary for Multiple Finger NMOS Devices.

The circuit It2 value for the 300um wide device was lower than expected. The device It2p values were 20% lower than the other multiple finger devices, 6.50mA/um compared to 8.2mA/um. If one were to assume that only 5 of 6 fingers triggered, the effective It2p value would improve to 7.80mA/um. Another hypothesis is that the NMOS supply clamp had a uniform finger turn-on problem. This is a more complicate scenario as the on-resistance of path B may not be constant, depending on the number of fingers conducting.

Further analysis on the uniform finger turn-on would require a large sample size for HBM testing and TLP analysis.

7.3.3 CGS parameter analyzed

The drain contact to gate space, or CGS parameter, has been a distinguishing layout feature of ESD devices for many years. To investigate the effect of the CGS parameter on ESD performance, devices with CGS values of 0.25, 0.50, 1, 2, 4, 5 and 6um were designed. Some of the devices, due to lack of space, did not have N-well contact plugs. These devices are listed in the table with a '#' symbol. A pair of devices were designed with a 2um CGS, one with and one without N-well contact plugs. These devices were designed with a pair of 50um wide fingers and a channel length of 0.65um. The source contact to gate space was fixed at 0.50um.

The HBM performance, shown in table 19, indicates a gradual increase in HBM threshold up to a CGS value of 2um. A dramatic increase in HBM performance is observed between the 2um CGS device and the 4um CGS device. At 2um, the HBM performance is between 1800 and 2000V, while at 4um the HBM values are between 3000 and 3500V. The results suggest that path B is conducting current for devices with CGS values 4um or greater. At CGS values at or above 4um, the HBM performance saturates at about 3500V.

CGS	TC - Pin #	B1	B2 +1	B2 +2	B2 +3	Avg
[um]		[V]	[V]	[V]	[V]	[V]
0.25 #	ESD03-04	1200	800	600	1400	1000
0.50 #	ESD01-12	1200	1000	1000	1000	1050
1.00 #	ESD01-16	1400	1400	1400	1400	1400
2.00 #	ESD01-25	1400	1400	1600	1200	1400
2.00	ESD01-26	1800	1800	1800	2000	1850
4.00	ESD01-24	3500	3000	3500	3500	3375
5.00	ESD01-11	3500	4000	3500	3000	3500
6.00	ESD01-10	3000	3500	3500	3500	3375

Table 19 – Cond 1+ HBM results for CGS NMOS devices.

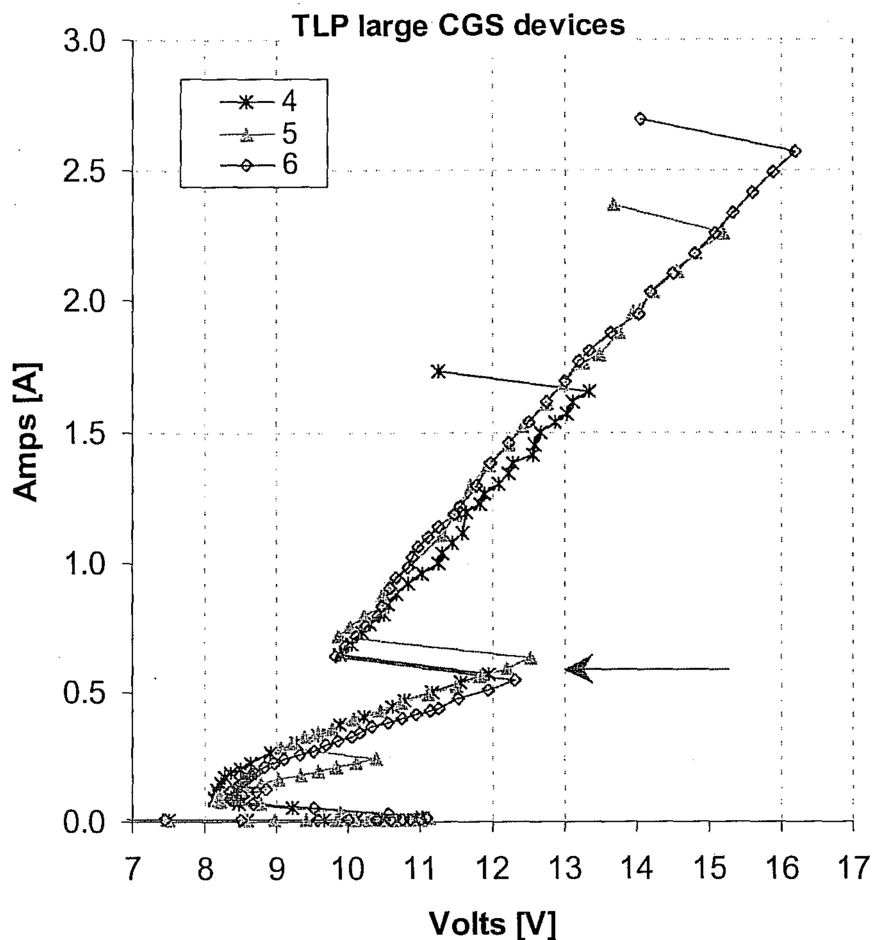

Figure 42– TLP results for the large CGS NMOS Devices.

The TLP curves for the large CGS devices: 4, 5 and 6um; are shown in figure 42. As suggested by the HBM results, all of the devices have a second snap-back point around 12.5V, marked with the blue, solid line, arrow. Beyond this point, current begins to flow in path B.

The TLP curves for the small CGS devices are shown in figure 43. Due to an oversight during the TLP analysis, the 0.25um and 1.0um CGS devices were not measured. These I-V curves, as predicted by the HBM results, are shown to fail at voltages under 12V, as a result the power clamp did not trigger and no current flowed in path B.

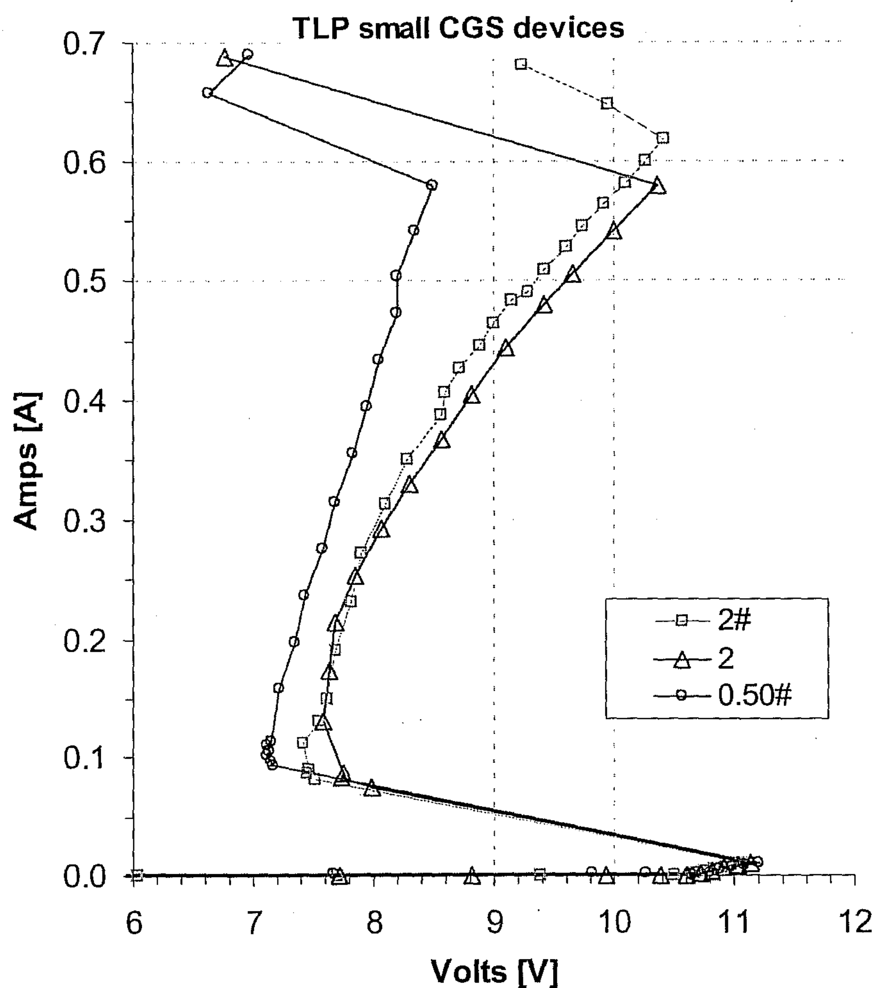

Figure 43– TLP Results for the Small CGS NMOS Devices.

The 2um and 2um# devices appear to have bout the same It2 value, roughly 610mA. This is interesting as the 2um device, the device with drain N-well contact plugs, was found to have higher HBM results than the same device without N-well contact plugs, 2um#.

The TLP results are summarized in table 20. As expected, the devices with the larger CGS values had the highest Ron values. The Vsp values range from 6V to 6.6V. The Vt1 values are nearly constant at about 11V. The measure It2 value for each test structure is listed in the table. For the large CGS devices, CGS values greater than 3um, the device It2, labeled It2d, value was calculated using the two path ESD solver, previously described.

CGS	TC - Pin #	Ron	Vsp	Vt1	It2	It2d	It2p
[um]		[ohms]	[V]	[V]	[A]	[A]	[mA/um]
0.50 #	ESD01-12	2.97	6.75	11.2	0.58	---	6.55
2.00 #	ESD01-25	5.19	6.63	11.0	0.610	---	6.89
2.00	ESD01-26	5.49	6.41	11.0	0.618	---	6.98
4.00	ESD01-24	9.88	6.25	11.0	1.73	0.722	8.16
5.00	ESD01-11	10.32	6.04	11.1	2.26	0.874	9.88
6.00	ESD01-10	10.56	6.57	11.1	2.57	0.914	10.33

Table 20– TLP results for the CGS NMOS Devices.

The normalized It2 values, It2p, are observed to steadily increase with an increase in the CGS value.

7.3.4 Length Parameter Analyzed

The last critical layout parameter is the channel length. Only three (3) structures were designed, with channel lengths of 0.50, 0.65 and 0.75um. Each device was designed with a pair of 50um wide fingers and a 4um CGS value.

The TLP extracted I-V curves are shown in figure 44. Each of the three devices appeared to have a second snap-back around 12V, indicated by the solid blue arrows on the figure. The TLP extracted parameters are shown in table 21. As expected, the snap-back voltages, Vsp, are related to the channel length. This result seems logical as the channel

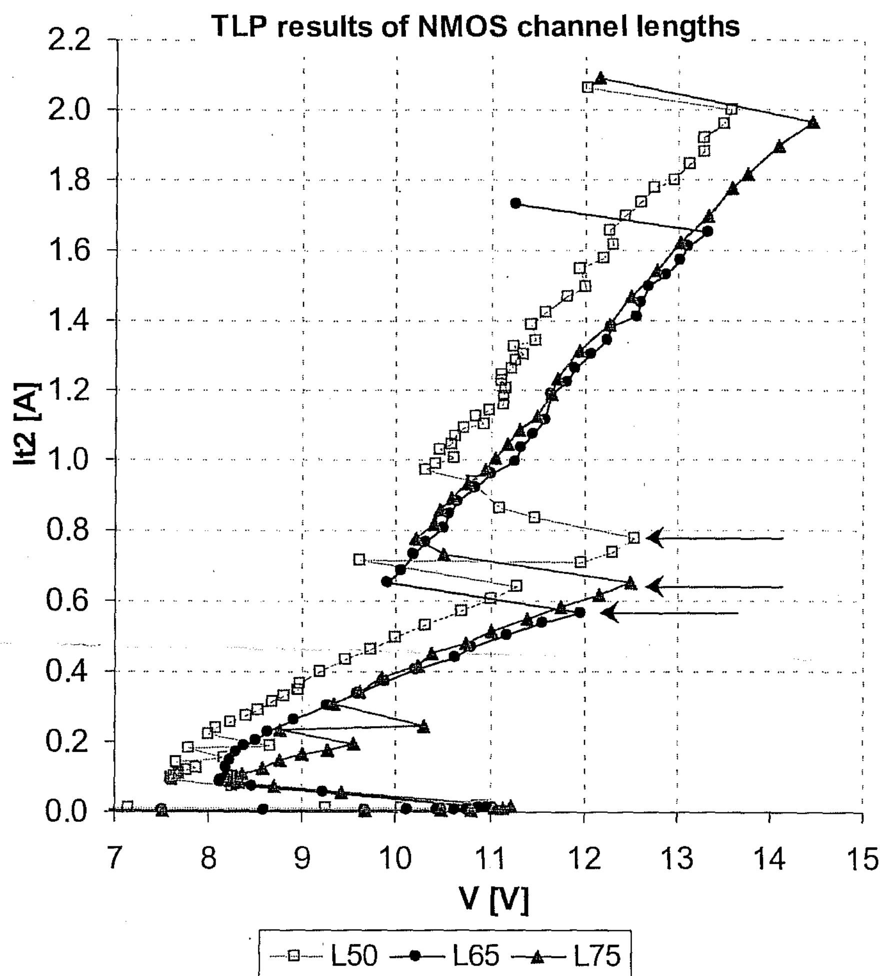

Figure 44 – TLP I-V curves for the L NMOS devices.

length is effectively the base width of the parasitic NPN device. Published results have shown that Vt1 and Vsp increase with longer channel lengths. Of the two parameters, the dependence of Vt1 is not nearly as high as the dependence of Vsp. The channel length sets the base-width of the parasitic NPN device, which directly sets the snap-back voltage. The Vt1 values in table 21 do show a slight dependence on channel length, but the difference in the Vt1 values is very low. The snap-back voltages do increase with an increase in channel length. The difference between the snap-back voltages is more dramatic between the 0.50 and 0.65 channel length devices. The on-resistance was expected to be independent of the channel length. The Ron values are within 1.2 ohms of each other and no pattern is observed to link the on-resistance with length dependence.

The HBM performance of the devices are summarized in table 22. The I-V curves have confirmed that current is flowing through path B, explaining the high HBM performance. Ironically, the 0.65 device was found to have the lowest It2 value, 1.65A, but was reported to have the highest HBM performance, about 3400V. No HBM results were reported for one of the 0.75um devices. Human error may have been the reason this pin was skipped during HBM testing of that particular sample.

Length	TC - Pin #	Ron	Vsp	Vt1	It2	It2d	It2p
[um]		[ohms]	[V]	[V]	[A]	[A]	[mA/um]
0.50	ESD03-03	8.70	5.71	10.9	2.00	0.916	10.35
0.65	ESD01-24	9.88	6.25	11.0	1.65	0.722	8.16
0.75	ESD01-13	9.41	6.30	11.2	1.97	0.835	9.44

Table 21– TLP results for the L NMOS Devices.

Length	TC - Pin #	B1	B2 +1	B2 +2	B2 +3	Avg
[um]		[V]	[V]	[V]	[V]	[V]
0.50	ESD03-03	3500	2500	2500	3500	3000
0.65	ESD01-24	3500	3000	3500	3500	3375
0.75	ESD01-13	2500	3000	2500	---	2667

Table 22– HBM results for the L NMOS Devices.

7.4 Silicon Controlled Rectifiers (SCRs)

On the ESD test chip, two types of silicon controlled rectifiers (SCRs) were designed: a Modified Lateral SCR (MLSCR) and a Low Voltage Triggered SCR (LVTSCR). A standard lateral SCR was not designed as its high trigger voltage makes it impractical as an ESD protection device. Only the width (W) parameter for these devcies was investigated. Most other parameters were designed to the minimum process design rule. One exception is the P+ anode to N-well tap space, labeled "A" in figure 45. This space could have been set to 0um as the diffusions are electrically connected to each other. This space was set to the minimum diffusion spacing (0.875um) to provide a larger N-well resistance to aide in the triggering of the PNP device. Most of the layout parameters are identical for both the MLSCR and the LVTSCR.

Using process evaluation monitors, the trigger voltages for the three SCR types is predicted in table 23. These values will be compared to the TLP extracted Vt1 values for both SCR types.

SCR Type	Trigger Mechanism	PROCESS MONITOR	Trig Voltage [V]
LVTSCR	Gated Diode	BVDSSN	11.7
MLSCR	BV N+/Pwl	BVDIODE1	12.8
LSCR	BV Nwl/Pwl	NWLDIODE	25.4

Table 23 – Predicted Trigger Voltages for SCR designs.

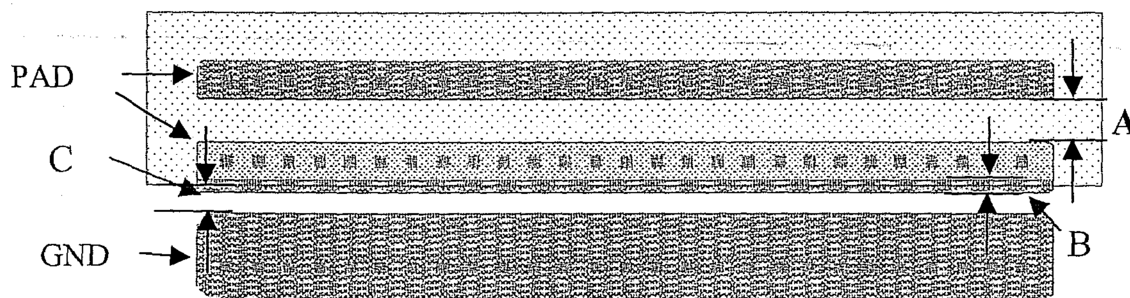

Figure 45 – Layout of the 35um wide MLSCR.

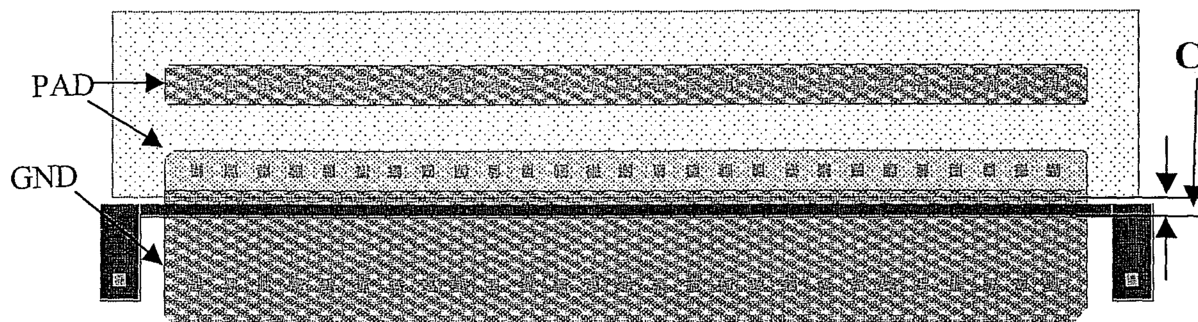

Figure 46 – Layout of the 35um wide LVTSCR.

Devices with widths of 35um and 70um were designed for both SCR types. For these devices, the width was defined as the width of the diffusion, not the width of the N-well. The MLSCR layout is shown in figure 45, while the LVTSCR layout is displayed in figure 46.

Both of these SCRs are designed with N+ diffusion placed across the N-well edge, which is generally not allowed in most process design rules. This space is labeled "B" in figure 45. During the HBM and TLP testing, the 70um LVTSCRs were found to have high junction leakage prior to testing. The leakage was found to be 0.66mA, with an applied voltage of only 0.5V. A layout review found that all of devices violated the design rule for P+ diffusion enclosure of N-well. The rule for this process was set to 1.0um, but the structures were designed with only a 0.25um distance. As a number of design rule violations were generated on this device, the general belief is that these design rule violations were misinterpreted as being "allowable".

The HBM failing voltage for condition 1+ are shown in table 24. Due to the high leakage observed on the 70um LVT device, the LVTSCR devices were not tested on third unit of the B2 set of tests. All of the failures were described as a direct short to the substrate. For the 70um LVTSCR device, the failure criteria was re-defined as a "significant" increase in DC leakage since over 5uA of leakage existed on the pin prior to HBM testing. Despite the high DC leakage, the device was observed to have good ESD robustness and a normal looking TLP I-V curve. The results show a fairly constant ESD performance for both types of devices at their respective widths. The 35um devices failed at voltages between 4500 and

5500 volts. The 70um devices had nearly twice the HBM failing voltages as they failed between 8500 and 9500 volts. The ESD immunity of both devices scaled quite well with device width. The ESD rating for the 35um and 70um devices was 134V/um and 129V/um respectively.

The TLP generated I-V curves are shown in figure 47. An interesting feature of the four devices is how closely the curves match one another. After the SCR fires, the I-V curves of both 70um wide devices closely match each other and the same is true of the 35um wide devices. The extracted TLP parameters are listed in table 25. The Vt1 values of both SCR types deviated from the expected values. The MLSCRs were expected to have Vt1 near 12.7V, as described in table 23. The TLP measured V_{t1} values were around 22V. The V_{t1} values are closer to N-well/P-well breakdown voltages than that of the N+/P-well breakdown voltages. In contrast, the LVTSCR Vt1 values were a few volts under the expected values. The LVT35 and LVT70 devices had Vt1 values under 9.8V.

A review of the Mask PG (Pattern Generation) flow, suggests that the source of the problem may be the N-well over sizing compensation coupled with the narrow N+ trigger diffusion. The minimum diffusion width for this process is 0.5um, which is the total width of N+ diffusion straddling the N-well. This process has a blanket P+ implant over N-well, so it is likely that the N+ in N-well region, 0.25um, was too narrow to be blocked and was

		HBM fail voltage [kV]					Lkg current @ 0.5V			
NAME	Chip-pin#	B1	B2			AVG	B1	B2		
ML35	E02 #20	4.5	4.5	5.0	4.5	4.6	shrt	shrt	shrt	shrt
LVT35	E02 #25	4.5	4.5	5.5	--	4.8	shrt	shrt	shrt	--
ML70	E02 #13	9.0	8.5	9.5	8.5	8.9	shrt	shrt	shrt	shrt
LVT70	E02 #18	9.0	8.5	9.5	--	9.0	shrt	shrt	shrt	--

Table 24 – Cond 1+ HBM results for the SCR devices.

SCR	Code	Vsp	Ron	It2	Vt1	Vh
ML35	ESD02-20	2.04	2.23	2.45	21.3	3.26
ML70	ESD02-13	1.98	1.62	4.71	22.8	3.06
LVT35	ESD02-25	1.91	2.07	2.35	9.73	2.20
LVT70	ESD02-16	1.75	1.80	4.67	7.68	1.87

Table 25 – TLP results of the SCR devices.

eliminated during the Pattern Generation (PG) flow. If this is what happened, the device was fabricated as a standard SCR, thus exhibiting the high trigger current. The TLP results certainly support this hypothesis. The expanding N-well may have also caused the N+ diffusion to be totally enclosed by N-well ultimately removing the N+/P-sub junction. The expanding N-well is the likely reason for the low V_{t1} values on both LVTSCRs and the leakages observed on LVT70.

A possible hypothesis for the source of the LVT70 leakage is as follows. The pad connected N-well expanded during the PG flow, enabling "punchthrough" to the grounded N+ source. All of the LVT70 devices measured were found to have excessive leakages, while none of the LVT35 devices were found to be leaky. As these test structures were

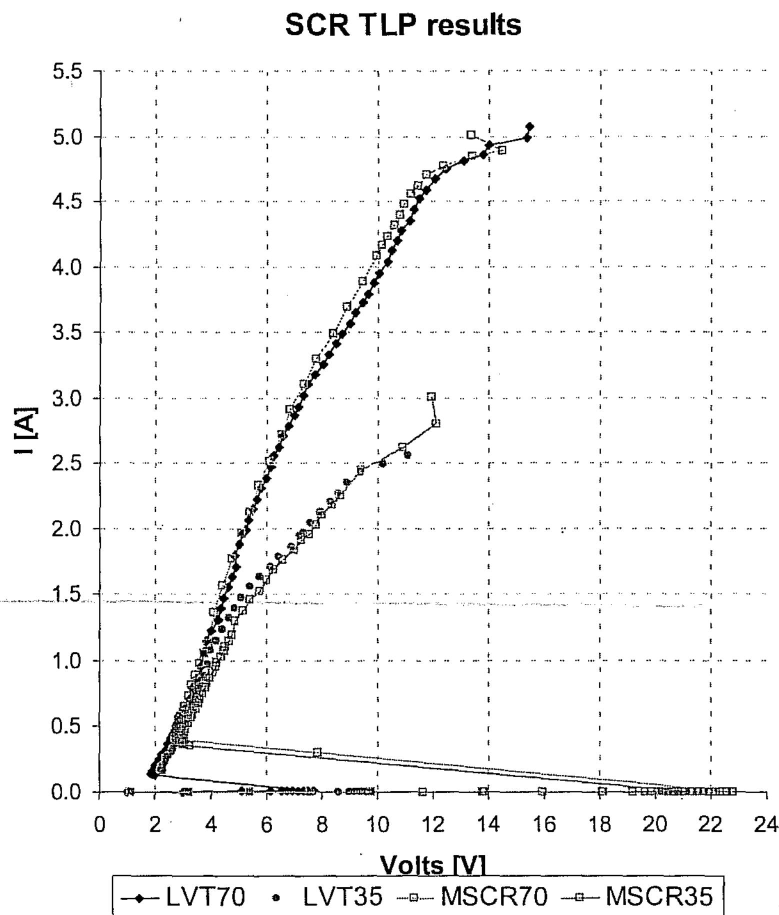

Figure 47 – TLP results of the SCR devices.

placed on adjacent sides of the test ring, misalignment is a possible reason why one device had excessive leakages and the other did not. The MLSCR devices did not exhibit excessive junction leakages, probably because the N-well to grounded N+ source space (labeled "C" on both figures) was found to 1.24um, compared to only 0.75um on the LVTSCR devices.

The snap-back voltage, with the exception of the LVT70 device, was found to be about 2V. The LVT70 devices were observed to have a slightly lower snap-back voltage of 1.75V. As expected, the 70um wide devices had lower on-resistance values than the 35um wide devices. The holding voltage values were higher for the MLSCR devices with the narrow devices found to have higher values than the wide devices. Like the HBM fail voltages, the It2 values seem to scale quite nicely with device width. These values are listed in table 26.

The normalized I_{t2} (It2p) values are quite high, but are close to the results published by Sarnoff Corporation in 2001 [23]. The normalized HBM voltage values are about twice as high as the 70V/um previously reported. The HBM to It2 comparison is shown in figure 48. The correlation resistance is about 1800 ohms, which is close to the ideal value of 1500 ohms. Unfortunately, the sample size consisted of only four (4) test structures.

All of the SCR devices were observed to have almost no leakage increase until the device was observed to reach the It2 point. At It2, the failure was observed on the leakage measurement, not an I-V kink. This implies that the failure observed during HBM testing, high junction leakage, was the same failure observed during the TLP characterization.

		Vhbm	Vhbm'	It2	It2'
SCR	Code	[kV]	[V/um]	[A]	[mA/um]
ML35	ESD02-20	4.6	131	2.45	70.0
ML70	ESD02-13	8.9	127	4.71	67.3
LVT35	ESD02-25	4.8	137	2.35	67.1
LVT70	ESD02-16	9.0	129	4.67	66.7

Table 26 – Normalized HBM and TLP results for the SCR devices.

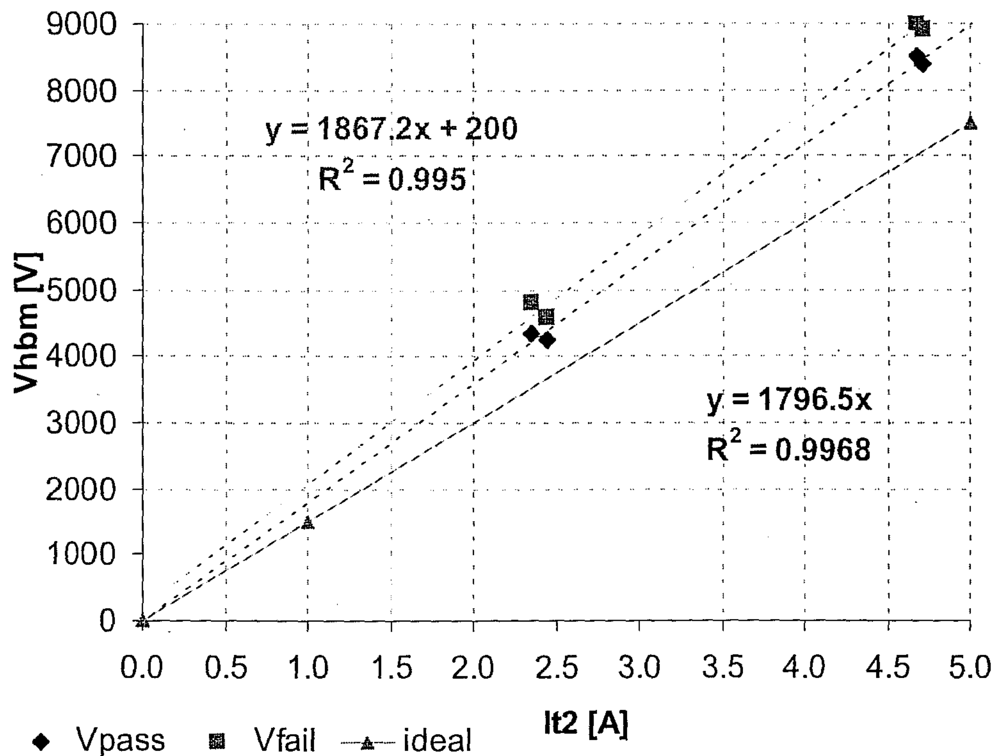

Figure 48 – MLSCR and LVTSCR It2 vs Vhbm.

The term "ideal" may not be appropriate for the correlation line at 1500-ohms. The TLP pulse is slightly wider than an equivalent HBM pulse, 100ns compared to 75ns, but the current measurement is taken at the last 20ns of the TLP pulse. Given these numbers, the TLP to HBM correlation line is expected to be slightly higher than the ideal case of 1500-ohms.

7.5 COMPARING TLP TO HBM FOR SNAP-BACK DEVICES

One important part of using TLP results to optimize and characterize ESD protection networks, is the correlation to HBM performance. This is basically a comparison between the HBM failing voltage and the TLP It2 value. Ideally, the It2 value would exactly match the HBM peak current (Ipeak) value. This would result in a correlation constant of 1500 ohms, the value of the series resistor in the HBM circuit model. Most published data reports correlation factors in the range of 1000 to 2000 ohms, depending on the process and the width of the TLP pulse. This analysis is limited to the NMOS and TFO devices as the both operate in snap-back conditions.

The NMOS based test structures were analyzed first. In Figure 49, the HBM failing voltages are on the y-axis with the TLP extracted I_{t2} values on the x-axis. The pink solid squares represent the HBM stress level that was found to invoke leakage on the device. The blue solid diamonds are the highest reported HBM voltages that the circuit was reported to pass without an observed failure. The delta between these two voltages depends on the magnitude of the step voltage. The step size is 200V up to 2000V and 500V after 2000V. Although some error does exist in the step size during the TLP analysis, this value has been neglected. The data points in this plot are either single NMOS devices or circuits containing both NMOS and PMOS devices. In either case, the failing device is assumed to be an NMOS device operating in the snap-back mode.

The grey, solid triangle, curve represents the ideal correlation of 1500-ohms. The results indicate that a correlation factor of about 1300-ohms is a good first pass estimate for the correlation. The data suggests a correlation factor of 85-88% of predicting the HBM threshold voltage with the TLP data.

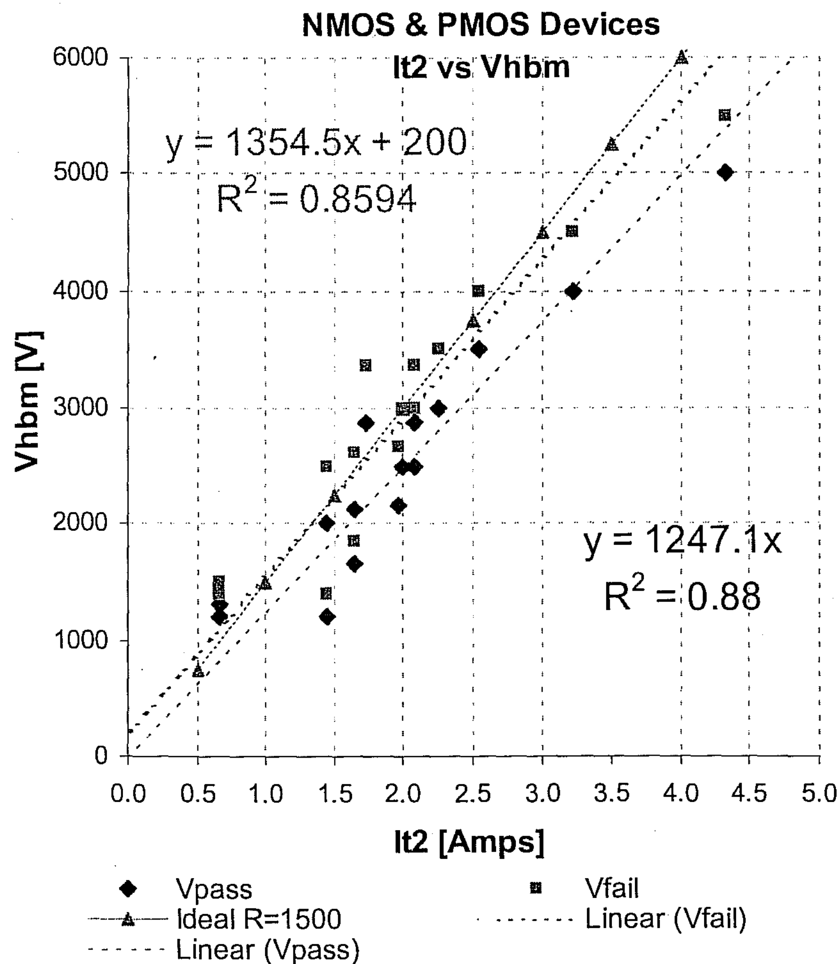

Figure 49. NMOS TLP vs HBM correlation.

One problem with correlating TLP results with HBM performance is the occurrence of soft failures. Soft failures are defined as increases in the leakage current above the background leakages, but not high enough to achieve the failure criterion. Figure 50 is a graphical display of this phenomenon on field devices (TFOs) and NMOS devices in a 0.5um process.

These results were determined using TLP methods, labeled TLM for "Transmission Line Method" on the x-axis. The blue solid data points are for an NMOS device, labeled GOX for "Gate OXide device" on the plot. The open circle data points are for a TFO, labeled FOX for "Field OXide device" on the plot. Two points are noted on the x-axis. The I_{ssb} (sub-surface breakdown current) has been noted at about 0.8A, with the I_{t2} point being

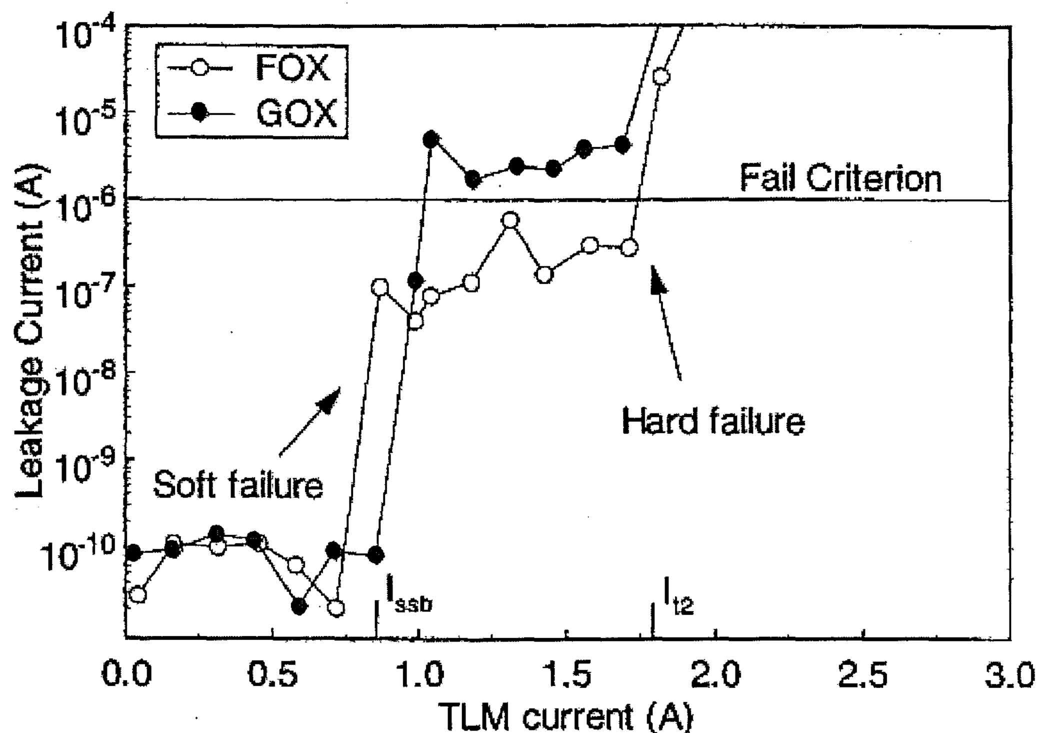

Figure 50. Soft and Hard failures of TFO and NMOS devices [14].

labeled at about 1.8A. The author of this paper has concluded that a strong correlation between HBM and TLP can be obtained if the It2 point is properly identified and not confused with I_{ssb}.

The TLP measurements on the devices in the paper were taken up to 4A, regardless of the status of the I-V curve or junction leakage value. The author states that sub surface failures (i.e. soft failures) do not cause latency problems for the device. Latency is a very old ESD definition coined for damage on devices that cause an increase in leakage, but not to the point of exceeding the data sheet parameters. This "damaged device" is considered a "walking wounded" as it is inherently weaker than an unstressed part. In contrast, many authors and ESD experts have indicated that any increase in the device leakage should be avoided and that a device with increased leakage is inherently not as robust as devices with the expected background leakage.

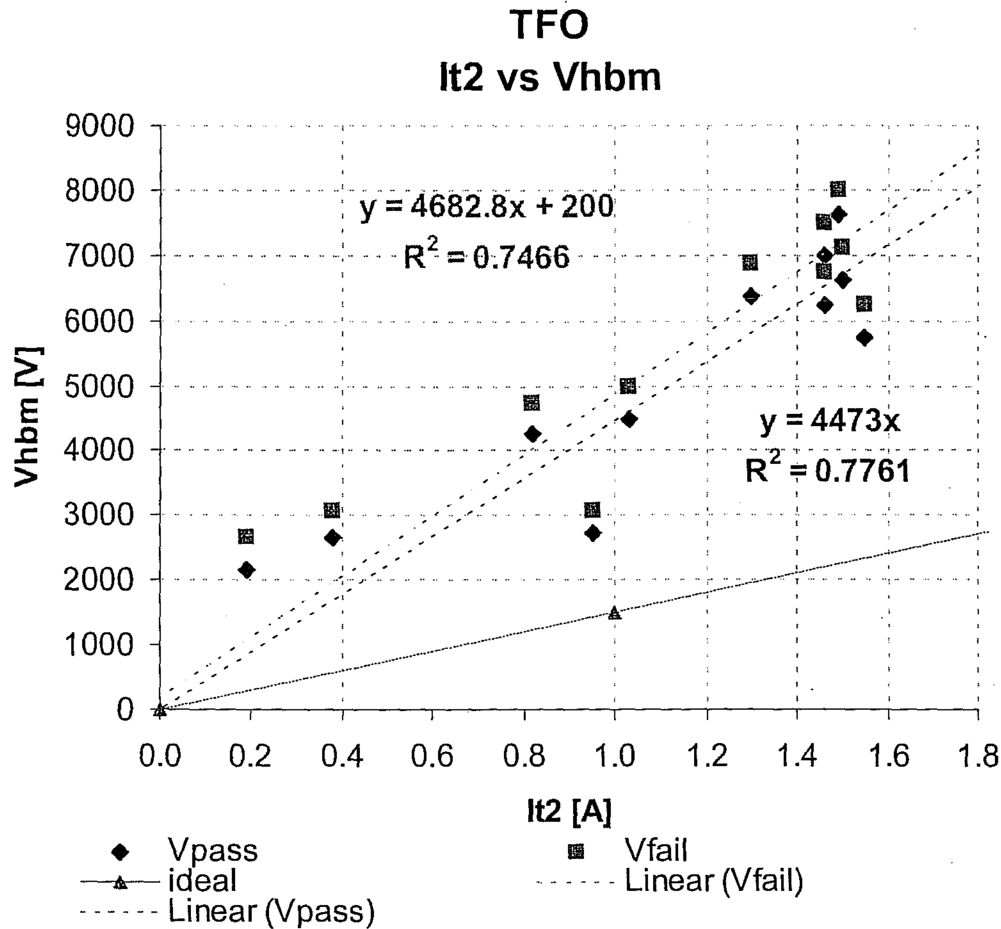

Figure 51. TLP It2 vs Vhbm for the Thick Field Oxide Devices (TFO).

The HBM and TLP results for the Thick Field Oxide (TFO) devices are compared in figure 51. Unlike the NMOS devices, the Thick Field Oxide devices deviate from the ideal correlation factor (1500-ohms) considerably. The grey, solid line represents the ideal correlation factor of 1500-ohms. The pass correlation factor is about 4500 ohms with coefficient of determination value of about 0.77. The failure correlation factor is about 4700 ohms with a coefficient of determination value of about 0.75.

The source of the deviation is likely to be the failure criteria used for both HBM and TLP testing. Both testing methods used an applied voltage of 0.5V to measure the post-stress junction leakage. The applied voltage should be the maximum voltage rating of the process,

which is 5.5V. This value was not using during the HBM testing as the junction leakage was measured using a curve tracer, with only the pin under test and the reference pin connected. On CMOS pins, a large applied voltage may raise the voltage of the chip's VCC signal through the parasitic vertical PNP inherent to the PMOS device connected to the pad. These leakages could be mistaken as ESD induced leakages. For this reason, the applied voltage was set to 0.5V to stay below the built-in voltage (Vbi) of the P+ diffusion/N-well junction and the threshold voltage (Vt) values of the MOS devices. This will avoid active devices from turning on, so that only the junction leakage will be measured. The applied voltage of 0.5V was also used during the TLP testing to match the HBM failure criteria.

In addition to a low applied voltage, the junction leakage HBM failure threshold of 5uA is likely to be too high. Most datasheets set input leakage specifications to about 1uA. The TLP measurements used the same applied voltage for the leakage measurement, but the lower of two (2) failure criteria's were used. The first failure criteria was set to a significant increase in junction leakage. The second failure criteria was set to a noticeable "kink" in the IV curve followed by an erratic waveform. All of the TFO devices were observed to have the "kink" in the IV curve prior to a significant increase in the junction leakage. This phenomena is quite common for field devices and has been reported by several authors [14] [21]. As TLP testing time was limited, testing on many of the structures was halted once one of the failure criteria's was achieved. This resulted in many of the It2 values being declared long before the junction leakages reached the HBM equivalent failure levels.

As the HBM testing was done using a manual HBM system, using an analog curve tracer (i.e. a Tektronix 575/576 series) only the failure leakage values were reported. It is interesting to note that many of the TFO devices were reported to have failing leakages values under 10uA, suggesting that devices were exhibiting a gradual increase in leakage across a wide voltage range. This can not be confirmed for the HBM testing as the leakage values were not recorded at each HBM stress level.

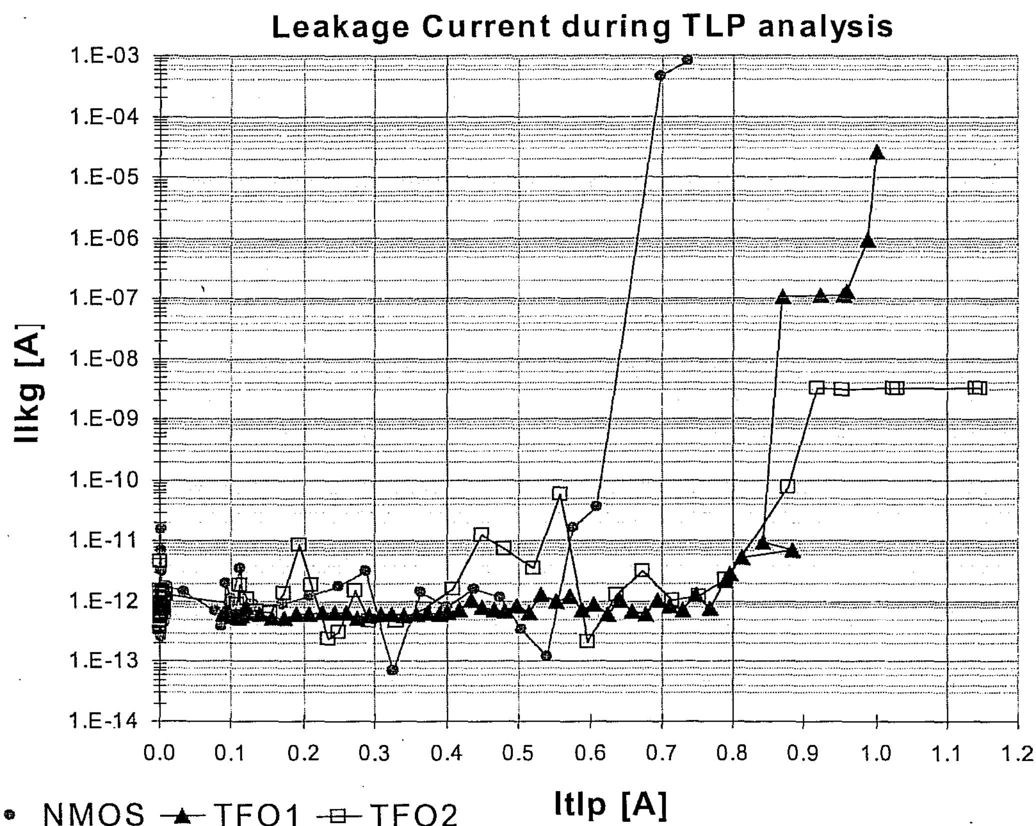

Figure 52. Post TLP stress, current leakage values for NMOS and TFO devices.

It is interesting to note that this phenomena does occur on MOS devices, but it is not frequent. The leakage evolution for an NMOS device and a pair of TFOs during TLP testing is shown in figure 52.

The NMOS leakage values are shown in magenta (solid circles). This device exhibits a dramatic increase in leakage current at around 0.7A of TLP current. The final leakage value is well above the 5uA failure criteria. The TFO1 device, shown in green (solid triangles), is observed to have an initial jump in the leakage current at around 0.9A of TLP current. A second increase in leakage current is observed near 1.0A of TLP current. Only the last data point is observed to achieve the HBM test failure criteria. The TFO2 device is similar to the TFO1 device, but the TLP testing was halted before the leakage current reached the HBM failure criteria. These initial increases in leakage could be sub-surface breakdown failures (i.e. soft failures), but no failure analysis was done to confirm this.

7.6 TEST CHIP SUMMARY

The diode test structures, due to a flaw in their design, were not properly HBM tested or TLP characterized. Adding the NMOS ESD device between the power supply rails created a parallel path for the ESD current with a lower trigger voltage than the reverse-biased junctions designed to be tested. Adding multiple devices to test pads always has some risk that a parallel path may be formed, causing test errors or invalidating a complete test circuit. This is true for both functional test circuits and ESD protection networks. Only the forward-biased P+/N-well diodes were characterized and this was only done on two test devices. The TLP testing was done under severe time constraints and a number of measurements were done to understand the unexpected results of the first set of devices characterized.

A few diode measurements were able to determine the normalized It2p value for the P+/N-well diodes. The It2p value is the second breakdown current, normalized to the diode perimeter, in units of mA/um. The It2p value for the diodes was found to be about 53mA/um.

Lack of N-well taps near the perimeter of the diodes was found to generate a very high clamp voltage across the diode under high currents in the forward-bias mode. A properly designed diode should be designed with high perimeter values with N-well or Substrate taps placed near the diode diffusions for improved ESD effectiveness.

The Thick Field Oxide (TFO) test structures were not found to have any major design problems. Increasing the range of some of the parameters, most specifically the channel length, may have produced better results, however. The HBM performance of the TFO devices was found to be significantly higher than TLP It2 values predicted. It has been hypothesized that the TFO devices are entering second breakdown without suffering catastrophic damage, as determined by the post-stress leakage measurement.

The TFO devices were found to have the following HBM and TLP characteristics. The HBM performance was improved by increasing the width and the contact to channel (CC) space. For the devices tested, no saturation in HBM or TLP performance was seen with an increase in CC space. The maximum CC value was only 5um, however. The narrow width device (W= 25um) device was found to have higher HBM performance, 86V/um, but the It2p value, 20mA/um, was found to be the same as the wider finger devices. This implies that the 25um device may be able to handle large HBM voltages without suffering catastrophic leakage, but the device have entered second breakdown during the pulse. Operating devices in second breakdown is not recommended. The device operation in second breakdown is likely to be unpredictable. This may explain the large spread of the data observed on many of the TFO device HBM results.

TFO devices designed to the minimum channel space, 0.875um, were found to have higher and more uniform HBM results. In contrast, the TLP results of this device indicated that the It2p value was equivalent to the channel devices. The snap-back voltage was confirmed to be dependent on the channel length. The on-resistance of the device was observed to increase for large CC values and decrease with width. The on-resistance parameter was also found to have channel length dependence, with narrow channels having higher on-resistance values. This result was not expected and is a possible subject of further research.

The NMOS devices were found to have the same design problem as the diode test structures. A large number of the structures had to be characterized using a circuit analysis technique that involved estimating the failing current through the device under stress at the measured, circuit level, It2 point. The HBM performance of the majority of the NMOS test devices could not be determined as significant current was predicted be shunted around the device under test.

The NMOS devices were found to have slightly higher It2p values for 25um wide devices. These devices had It2p values of 8.49mA/um. The multiple finger devices did

appear to have uniform finger turn-on issues, but this analysis was distorted by the existence of the parasitic ESD current path, initiated by the design error. The contact to gate space, CGS, was found to increase the it2p from 6.55 to 10.33mA/um. No saturation in performance was observed up to the 6um maximum CGS value tested. Increasing the CGS value did adversely affect the on-resistance of the device, however. Decreasing the channel length was observed to reduce the snap-back voltage (Vsp=5.71V) and improve the It2p (10.35mA).

The silicon controlled rectifiers test structures were found to have a minor design error on the LVTSCR design. The error caused one of the devices to have high initial leakage values, but design error was not found to significantly impact the performance of the device. All of the SCRs were found to have high HBM ratings, 130V/um, and It2p values, 67mA/um. The LVTSCR design looked very promising as a low capacitance ESD protection device.

The CMOS ESD test chip was able to characterize many of the ESD layout parameters that were designed. The existence of the ESD protection between the supply rails did limit the characterization of many of the devices. Care should be taken on future ESD test chips to ensure that similar design flaws do not invalidate well designed test structures. The TLP system was a very valuable tool for characterizing devices under ESD stress. The system was also very helpful in detecting the design problems on the diode and NMOS structures.

CHAPTER 8 - ESD TEST CHIP DESIGN GUIDELINES

A great number of lessons were learned from the design and analysis of the ESD Test Chip. Some important technical data was learned from the analysis of all device types and the effects of parallel current paths during ESD as well. Perhaps the most important lesson learned was… "A List of Things not to do when designing an ESD Test Chip".

DESIGN

- Limit the ESD test structures on a single pin or pad cell to a single device.
    - Unexpected parallel current paths distorted the results of the Diode and NMOS structures.
- Design large pad cell rings with the same device type and expected ESD immunity.
    - The cost of outside assembly is generally quite high, thus the more structures that can be tested on a single assembled unit lowers the overall cost per structure.
    - HBM testing takes less time if all of the devices are tested to the same test condition, with roughly the same robustness levels.
- Design the test chip for testability. Make sure the devices designed for HBM analysis can be easily bonded. Place TLP test modules of the same type near one another for easy TLP probing.
- If test chip silicon area is abundant and time is limited, fill up the extra space with repeated test modules. Additional structures available for measuring are always beneficial.
- Properly label the modules and pads with top level metals. During wafer level analysis, accessing the layout may be difficult.
- Avoid placing metal layers over critical sections of the ESD devices. Metal layers can shield the damage locations from Photoemission and liquid crystal analysis.
- Assemble and HBM test units in open cavity packages. This will save the decap step

of the Failure Analysis process. This also reduces risk of the die being damaged during decaping, possibly hindering the photoemission or liquid crystal analysis; which require the sample to be electrically active.

- Verify layouts using Automated Design Rule (DRCs) and Layout vs. Schematic (LVS) if applicable.
  - Many "novel" structures violate existing designs rules. These violations should be thoroughly reviewed by the designer and a third party process knowledge person as well.
  - A complete mask set can cost a quarter of a million dollars. A test chip is not simply a "test"; it is a validation of design Intellectual Property (IP) and should be designed with same level of diligence as a product. Even scribe structures are critical. The area may be free, but it will take 4-6 weeks for the structure to be fabricated.
  - Each element of a complicated circuit should also be placed as an isolated device.
    - This will aide in the analysis if the circuit performs "unexpectedly".

HBM TESTING

- Develop a test, or even a test circuit, to ensure that the devices were fabricated correctly.
  - Typically, process monitors are used to ensure that the lot was processed correctly. They generally don't ensure that devices are in the center of the process window. For production designs, yield determines if the devices are inside the process window. Yield analysis requires a product with an established test program, something test chips typically don't have.
  - Disregard devices that have unexpected performance prior to HBM testing.
    - Making critical decisions on questionable devices is bad engineering.
- Devices should be tested using repeated pulses of the same polarity.

  - Testing devices to all combinations complicates the failure analysis
- If step voltages are used (i.e. test voltage increased after each round of testing), the leakage current values should be saved after each test.
  - This method will help to identify "soft" and latent leakage failures.
- The applied voltage for the leakage failure criteria should be set to VCCmax (i.e. Maximum operating VCC + 10%).
  - This voltage may have to be reduced on structures with NMOS and PMOS devices. In these cases, the VCC value be the maximum voltage allowed, such that a good unit has leakage current close to the background leakage value.
- Record the leakage values after each HBM VZAP so that a leakage evolution plot can be generated.

DEVICE CHARACTERIZATION AND POST-HBM ANALYSIS

- Characterize all ESD structures using TLP analysis.
- As with HBM testing, the junction leakage test should be done to the maximum VCC voltage (VCCmax + 10%).
  - If this produces excessive leakage on good units, optimize the applied voltage to allow for leakage evolution plots.
- Carefully research all unexpected TLP results. Do not discount the results as "bad data" without a investigating.
- Complete the Failure Analysis on all tested units to identify failing structures
  - Photo emission or Liquid Crystal analysis may not be necessary. A simple strip-back, wright etch and SEM visual analysis alone will likely identify the damage.

CONCLUSION

The semiconductor industry continues to produce faster integrated circuits on smaller dice. The result is the development of smaller and faster devices, devices designed with shallow junctions and ultra thin gate oxides. Smaller devices are more at risk for ESD damage. Modern integrated circuits require effective and robustness ESD protection networks to ensure the long-term reliability of advanced sub-micron devices.

This thesis outlines some basic ESD background information and the impacts of reliability. The commonly accepted ESD testing methods are described and compared. An overview of the ESD device characterization methods is given along with the basic ESD induced failure mechanisms.

The basic ESD protection devices are diodes, NMOS devices, Thick Field Oxide devices (TFOs) and silicon controlled rectifiers. A basic overview of ESD protection methods is also discussed.

A CMOS ESD test chip was designed, fabricated, assembled and characterized using HBM and TLP. The results are summarized for each set of test structures. The problems encountered during the characterization were explained. A list of guidelines was published so that future ESD test chips may avoid some of the problems encountered on the ESD test chip designed here. A summary of the results has been included.

TOPICS FOR FURTHER RESEARCH

The most interesting aspects of the results from the Thick Field Devices and to a lesser extent, the was the possibility that the device may be entering second breakdown with out suffering catastrophic damage. This issue will be researched on devices fabricated in a 0.13um CMOS process.

APPENDIX

The Two path ESD circuit solver

The diode and NMOS test structures were found to have a parallel path for the ESD current through a parasitic P+/N-well diode and the large NMOS power clamp. This parallel path inflated the measured HBM threshold and TLP It2 values. Using the TLP parameters of the device under test prior to the conduction in the parasitic path, the current flowing the device at the point of failure can be approximated.

The I-V curve for the 100um wide two finger NMOS device will be used as an example. The TLP I-V curve and junction leakage curve are shown in figure 53. The I-V curve is observed to have an initial trigger voltage of 11V and a second snap-back region at about 12V.

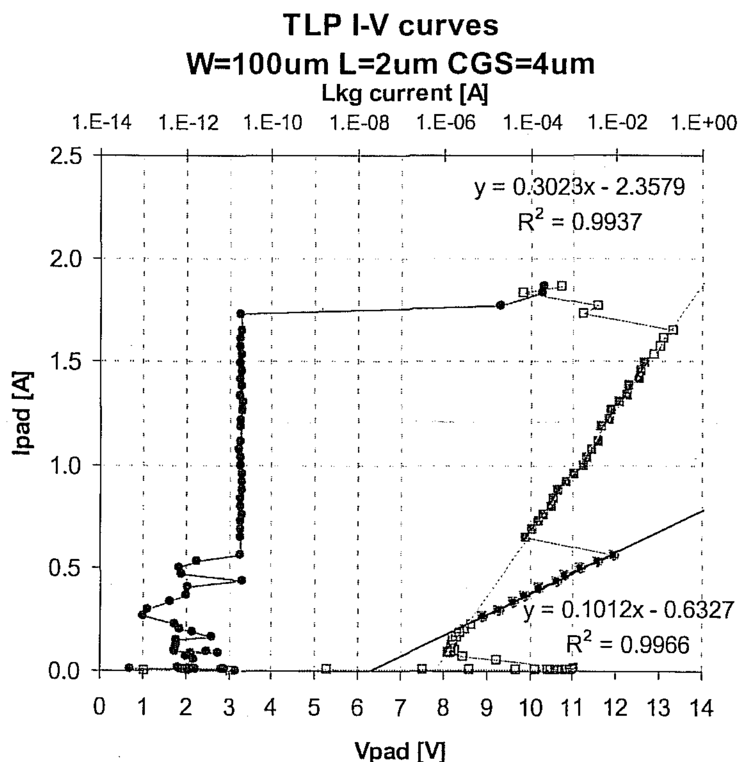

Figure 53. TLP curve example.

The TLP parameters for the snap-back voltage (Vsp) and on-resistance (Ron) are extracted between the initial trigger voltage (11V) and the second snap-back point (12V).

The on resistance is calculated from the reciprocal of the slope and the snap-back voltage is the x-intercept of the line. The device under test is simply modeled as DC voltage source set to the snap-back voltage and a series resistance equal to the device on-resistance. The parasitic path will use the same model, but it must be triggered before it conducts current.

Using a spreadsheet and elementary circuit techniques, the two path circuit can be solved for any ESD protection devices. The two path template is created and ready to be optimized for a given circuit. The critical parameters are the Ron and Vsp values for the device in path A and the trigger voltage of the second path. These parameters are entered in the spreadsheet and the circuit is ready for curve fitting as shown in figure 54 below. In the

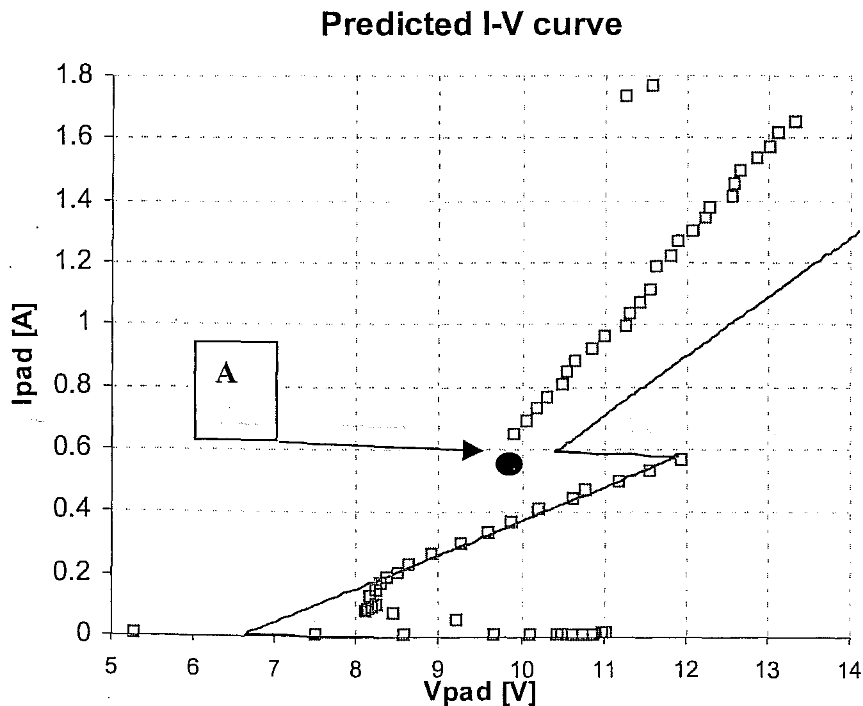

Figure 54. TLP Predicted I-V curve stage 1.

first snap-back region a the predicted curve should match the TLP extracted curve quite well. The next step is to adjust the snap-back voltage and on-resistance of the second path. The second path snap-back voltage should be adjusted to align point A with the first point after the circuit enters the second snap-back region. The second path on-resistance is then adjusted to align the slope of the predicted line to measured I-V line.

Other adjustments may be necessary to get the desired fit. Once the curve is aligned, as shown in figure 55, the circuit is effectively solved. A lookup table is created listing the current in branch A and B for any value of ESD current. The current flowing in branch A or branch B can be determined at the circuit's second breakdown current It2 or any current value.

The algorithm only works for two path networks and the devices must be modeled as a voltage source (snap-back or clamp voltage) and a series resistance (device on-resistance). For circuits with more than two paths a SPICE deck will have to be created. This two path solver can also be used to predict the I-V waveform of a two path circuit designed with

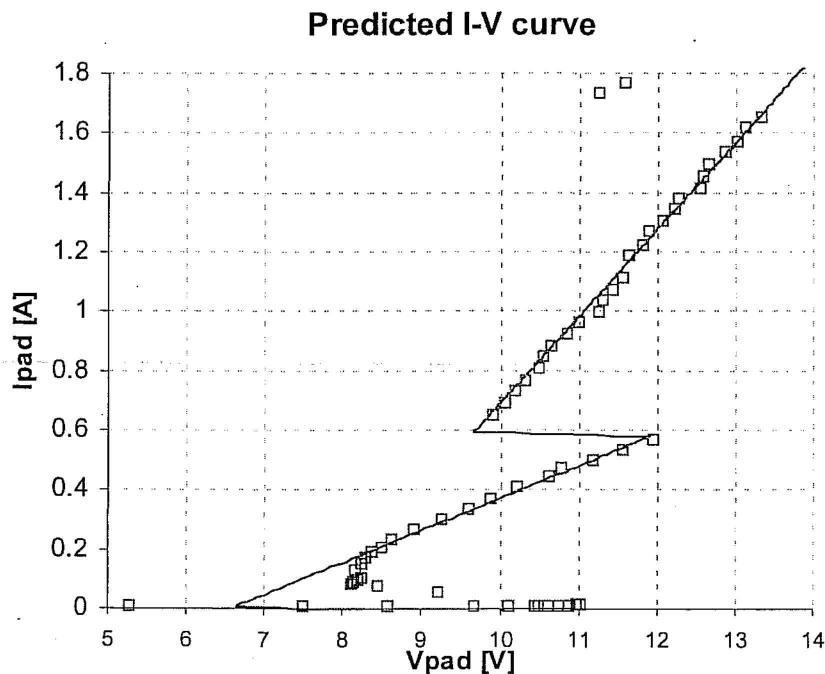

Figure 55. TLP I-V final.

previously characterized TLP devices. The critical device parameters (Ron, Vsp and Vt1) are entered in each path, along with the estimated interconnect resistance and a predicted I-V curve is generated.

Once the circuit is solved, the results are illustrated in a plot like figure 56, where the magnitude of current flowing in both branches is displayed. The figure illustrates that path A is the device under test, as it begins conducting current before path B, the path through the power clamp device. Current flow though path B does not begin until 600mA of ESD current.

The method will lose accuracy if the device appears to have a non-linear snap-back curve. This occurs in some devices near the It2 point and in multiple finger devices that don't have uniform ESD finger turn-on.

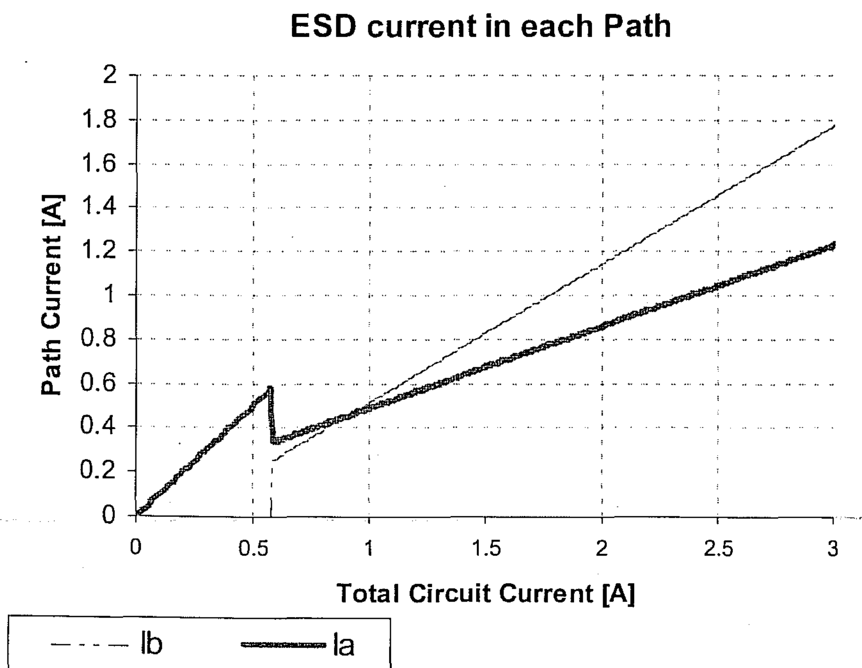

Figure 56 – ESD current path results.

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