DESIGN, LAYOUT, AND TESTING OF SIGE APDS

FABRICATED IN A BICMOS PROCESS

By

Dane Gentry

Bachelor of Science in Electrical and Computer Engineering

University of Nevada, Las Vegas

2016

A thesis submitted in partial fulfillment of the requirements for the

Master of Science in Engineering – Electrical Engineering

Department of Electrical and Computer Engineering

Howard R. Hughes College of Engineering

The Graduate College

University of Nevada, Las Vegas

December 2018

Approval Page Place Holder

Abstract

This Thesis is concerned with the design, layout, and testing of avalanche photodiodes (APDs). APDs are a type of photodetector and, thus, convert light signals into electrical signals (current or voltage). APDs can be fabricated using silicon (Si). In this Thesis, however, three integrated circuit (IC) chips containing various silicon-germanium (SiGe) APDs with different sizes, structures, and geometries were designed, laid out, and fabricated using the Austriamicrosystems (AMS) 0.35μm SiGe BiCMOS (S35) process. This was done in order to compare SiGe APDs to Si only APDs and investigate the hypothesis that SiGe APDs are capable of detecting longer wavelengths than Si only APDs. This is due to the smaller band gap energy associated with SiGe compared to that of Si.

The different SiGe APDs were tested and found to, indeed, have the capability of detecting slightly longer wavelengths than Si APDs. A 5μm x 5μm SiGe APD and 24μm x 24μm SiGe APD were found to have a spectral peak at 500nm and a cutoff wavelength (λ_c) of 1180nm compared to 480nm and 1100nm, respectively, for a 10μm x 10μm Si APD. The 24μm x 24μm SiGe APD was also found to have a responsivity of 0.34 A/W at 500nm and quantum efficiency (QE) of 85% at 450nm.

APDs differ from traditional photodiodes in that they possess an internal avalanche gain and, thus, produce a larger electrical signal than a traditional photodiode for the same amount of incident light. All photodiodes produce an undesired electrical signal, called dark current, even in a dark state with no light signal incident on the photodiode. Therefore, the gain and dark current associated with each of the fabricated APDs was also measured in order to determine the characteristics of the different SiGe APD variants. The 5μm x 5μm and 24μm x 24μm SiGe APDs have a zero bias (0V) dark current of 3pA and 5pA, respectively, compared to 3pA for the

10µm x 10µm Si APD. The 5µm x 5µm and 24µm x 24µm SiGe APDs and the 10µm x 10µm Si

APD also have gains of 88,000 (98dB), 1390 (63dB), and 1000 (60dB), respectively.

Acknowledgments

Having spent the past six and a half years as an electrical engineering student at UNLV, I am thankful to have had such a fortunate undergraduate and graduate experience. I feel accomplished in having achieved countless goals and to have earned a prestigious role in society as an educated electrical engineer dedicated to a journey of life-long learning. I have undoubtedly put forth a great deal of effort and persevered despite certain hardships, obstacles, and difficult decisions paired with great sacrifices. Nonetheless, I simply cannot express enough gratitude to the many people in my life whom have inspired me on a daily basis to live my life to the fullest.

First and foremost, I would like to thank every member of my family as well as my friends whom I consider family for their unconditional love and for always being there for me. I would also like to thank my favorite high school teachers, Mr. Taylor, Mr. Artmann, and Mr. Panik for having such a positive influence on me at such an impressionable age and motivating me to be the educated man I am today. I would also like to thank every member of Dr. Baker's research team, past and present, for all their help. Witnessing firsthand all the hard work and dedication of my colleagues has truly inspired me to try my hardest to excel in everything I do.

Last but certainly not least, I would like to thank my professor, my advisor, my boss, my mentor, Dr. R. Jacob Baker. Working as your student and research assistant these past three and a half years has had an immense impact on me that will stay with me the rest of my life. Just by simply knowing you and seeing how you operate has taught me a great deal about responsibility and work ethic. You have instilled in me a mentality of curiosity and intrigue that I will cherish the rest of my life. I don't think I could ever truly pay you back for all you have done for me, but I hope that somehow you know what your mentorship means to me and will always mean to me.

Thank you Dr. Baker. Thank you everyone for reading this as it signifies the ending of a great

chapter in my life and, hopefully, the beginning of an even better chapter.

Preface

This Thesis serves as a report documenting past, present, and future efforts of myself with the assistance of Dr. Baker, as well as his undergraduate and graduate research students at UNLV, in cooperation with Freedom Photonics in order to fulfill NASA funded research on a "Geiger Mode SiGe Receiver for Long-Range Optical Communications". This research is expected to continue beyond my graduation, and, as such, this Thesis is intended to be reviewed and, more importantly, expanded on by Dr. Baker's UNLV research team. Thus, an overview of the basic principles and foundations for which photodetectors are based on as well as a few of their numerous applications are presented in Chapter 1.

In order to effectively understand this presented summary of the research that has been undergone thus far, the reader is encouraged to review the material in Chapter 2 and Chapter 3. These chapters were written with the intention of allowing the reader to familiarize, or re-familiarize, their self with some foundations of semiconductor physics in conjunction with solid-state electronics. This includes the basics and formation of PN junction diodes as well as their implementation as photodiodes in addition to an overview of the modes of operation and characteristics of photodiodes.

Chapter 4 explains the foundations for which the presented research is based on. Chapter 5 details the three chips that were designed and fabricated. Chapter 6 summarizes the testing results of the APDs on Chip 1. Finally, Chapter 7 is a conclusion of the research followed by a description of future work for this research.

Table of Contents

List of Tables

List of Figures

List of Equations

Chapter 1: Introduction

1.1 Basic Principle and Applications of Photodetectors

Photodetectors are widely used in numerous products and applications in order to convert light signals into electrical signals. Used extensively in light detection and ranging (LiDAR) applications, photodetectors are capable of detecting low levels of reflected light in order to measure distances of objects and potentially generate a three-dimensional scan of the surrounding area, which is extremely useful for self-driving vehicles as shown in Figure 1.1 below.
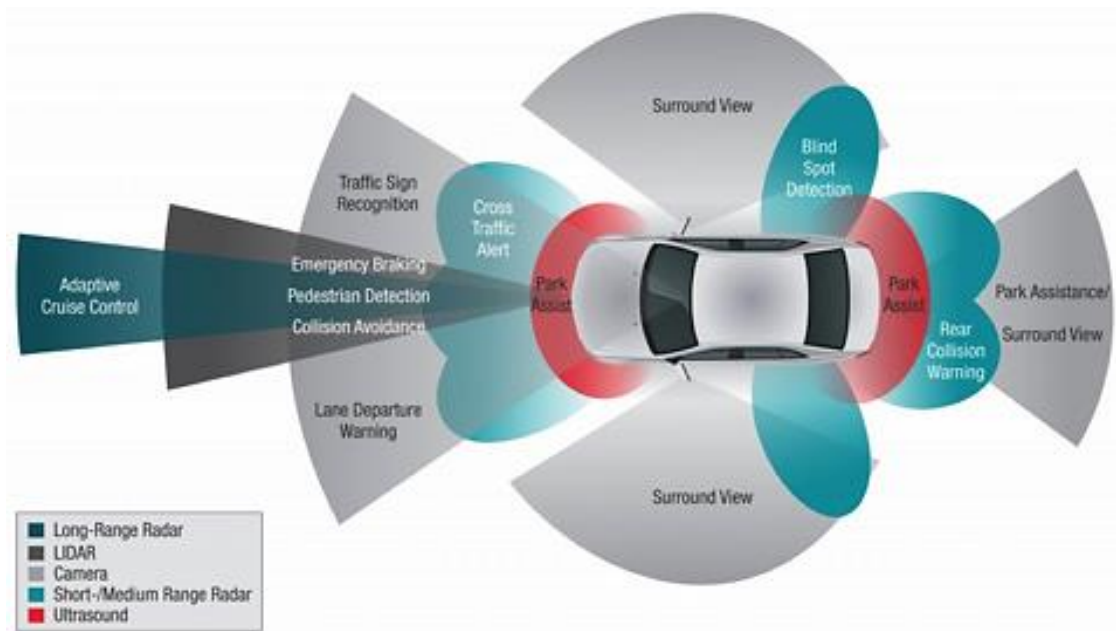
Figure 1.1 – 3-D LiDAR Mapping for Self-driving Vehicle [1]

LiDAR systems produce a short duration pulse of light which is reflected off the nearest object in its path. Some of the reflected light is then detected by the photodetector in the LiDAR system, and the time of flight (TOF), the time between the produced pulse and the received light, is recorded. The TOF is then used to calculate the corresponding distance between the LiDAR device and the measured object using Equation 1 below,

$$d = c \times \frac{\Delta t}{2}$$

<div align="right">Equation 1</div>

where d is the distance of the object in meters, c is the speed of light in a vacuum (3.0×10^8 m/s), and Δt is the TOF. Note the TOF is divided by two since the light pulse travels to the measured object and back to the LiDAR device as shown in Figure 1.2 below.
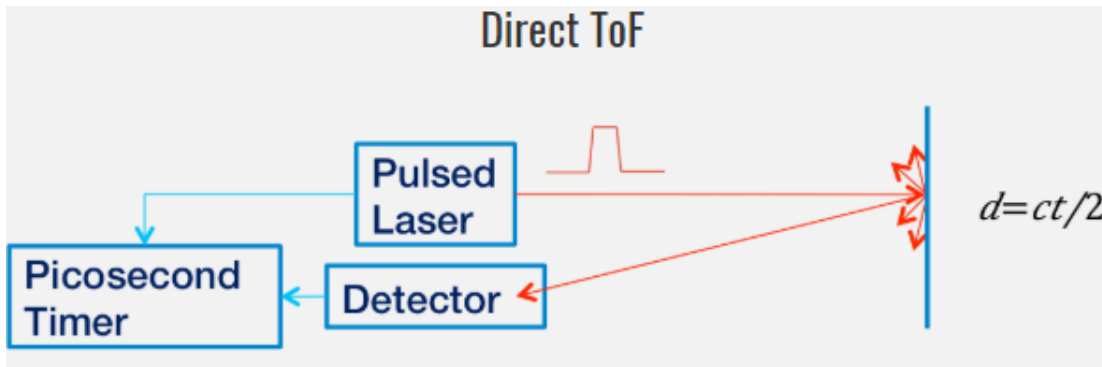
Figure 1.2 – Photodetector in a LiDAR System [2]

Numerous factors including the reflectivity of the measured object, the ambient light in the environment (namely sunlight), etc. affect the performance and accuracy of the LiDAR device.

Additional applications of photodetectors in which the number of incident photons is precisely determined include, but are certainly not limited to, image sensors, flow cytometry, radiation monitoring, spectroscopy, and optical communication [3]. Photodetectors are also utilized for security purposes as well as counting products on a conveyor belt by detecting the interruption of a light source (such as a laser beam) by an object.

1.2 Motivation

Since photodetectors convert light signals into electrical signals, an ideal photodetector would not generate any electrical signal under a dark condition in which no light is incident on the photodetector. In reality, however, current practical photodetectors produce undesired electrical signals called dark current when under a dark state. Additionally, depending on the

materials used for their construction, photodetectors are capable of detecting certain ranges of wavelengths within the electromagnetic spectrum shown in Figure 1.3 below.
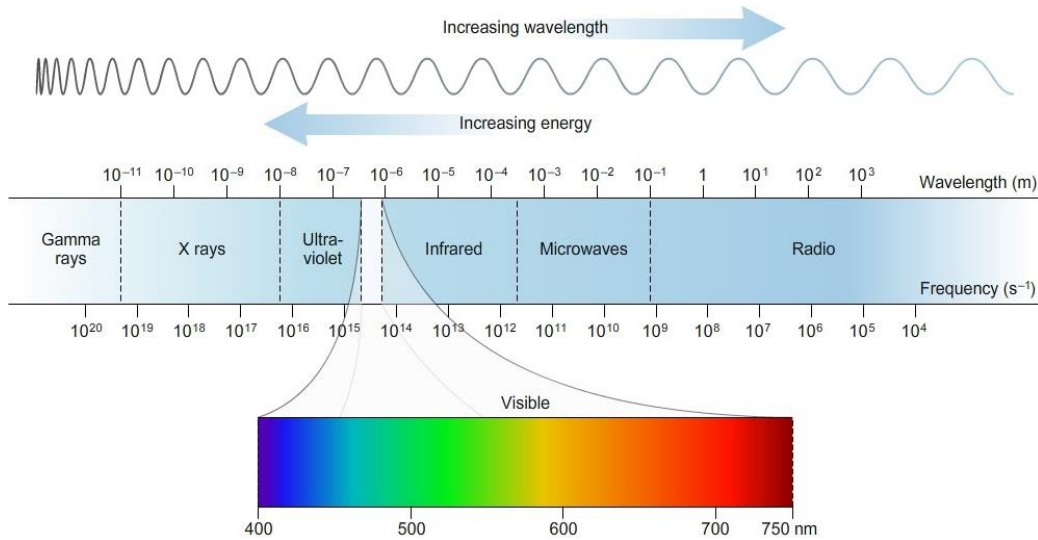
Figure 1.3 – Electromagnetic Spectrum [4]

Current conventional photodetectors fabricated using Silicon (Si), one of the most widely used semiconductor materials used in chip fabrication due to its vast availability and low cost, are capable of detecting wavelengths of light from 320 nm (or 190 nm for UV-enhanced Si photodetectors) up to a λ_c of 1100 nm with decreased responsivity, as the detection peaks then drops sharply for higher wavelengths [5]. There is a desire, however, to tailor photodetectors to detect higher wavelengths of light, namely 1550nm which lies in the near-infrared (NIR) region.

It is hypothesized that photodetectors comprised of Silicon-Germanium (SiGe) are capable of detecting higher wavelengths due to the lower band gap energy of Germanium (Ge) compared to that of Si, explained further in Chapter 3. In an effort to decrease dark current and tailor photodetector detection to higher wavelengths, this Thesis investigates the characteristics and performance of SiGe photodetectors designed with various structures, geometries, sizes, and layers and fabricated in the Austriamicrosystems (AMS) SiGe 350nm (S35) process as opposed to Si only based processes such as the ON Semiconductor 500nm (C5) process.

Chapter 2: Foundations of Semiconductor Physics

2.1 Semiconductor Basics

In solid state electronics, Si is one of the most commonly used semiconductor materials for chip fabrication due to its inexpensive nature and abundance in nature. Si has an atomic number of 14 which means that a single Si atom has 14 total electrons, two in the inner first shell, 8 in the second shell, and 4 in the outermost shell as seen in Figure 2.1 below.
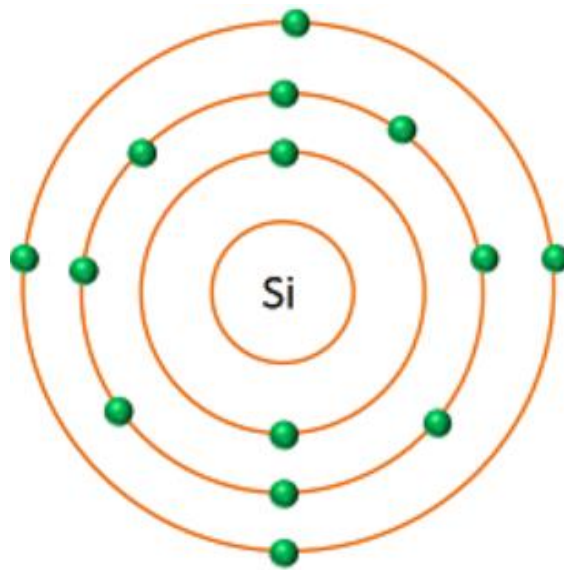
Figure 2.1 – Silicon Atom [6]

A simplified view of a Si atom in which only the four valence electrons in the outermost shell of the Si atom are shown is commonly used since these are the electrons that form chemical bonds.

Another common semiconductor material, Ge, also has four valence electrons but has more free electrons and, thus, higher conductivity than Si for a given temperature due its lower band gap energy. When numerous Si atoms come together in a crystalline structure to form a solid, the valence electrons of neighboring Si atoms bond with one another, creating covalent bonds between the neighboring atoms as shown in Figure 2.2 below.

Sharing of electrons
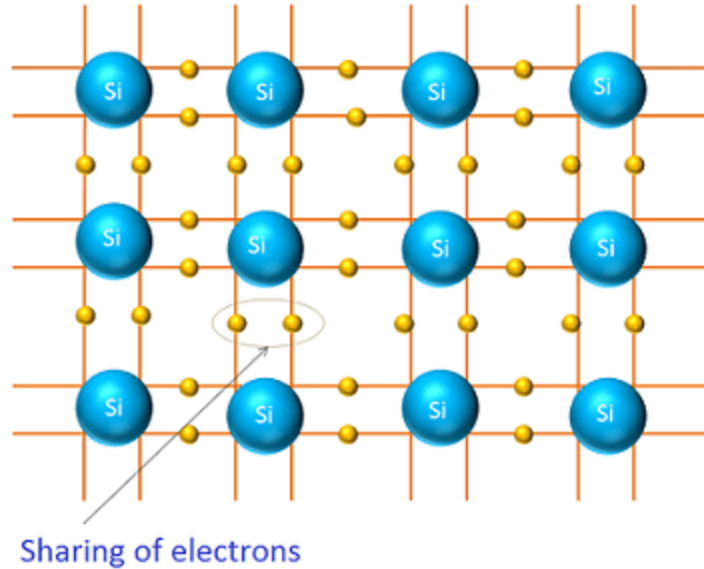
Figure 2.2 – Shared Covalent Bonds between Neighboring Silicon Atoms [7]

For intrinsic Si at zero Kelvin, all of the valence electrons of neighboring Si atoms are bonded to one another. However, as the temperature increases some electron can gain enough thermal energy in order to break free from their covalent bonds and get excited from the valence band up to the conduction band, leaving behind holes (or missing electrons) in their place in the valence band. This reduces the semiconductors resistance since there are more electrons in the conduction band capable of conducting electricity. The valence band and conduction band are separated by a band gap, as shown in Figure 2.3 below, which is the energy, in electron volts (eV), required for an electron to break free from the covalent bond and get excited from the valence band to the conduction band.
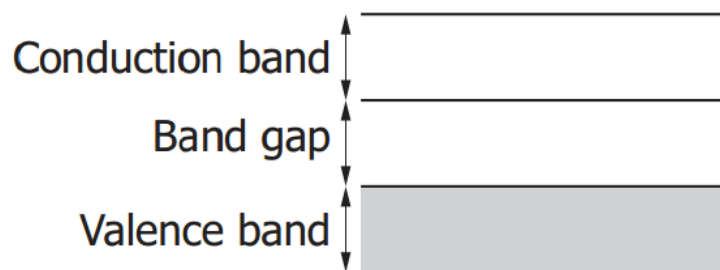
Figure 2.3 – Valence and Conduction Bands separated by Band Gap [8]

The band gap of intrinsic Si at room temperature is 1.12 eV [9]. Intrinsic semiconductors such as Si and Ge are Group IV elements since they have four valence electrons. An n-type semiconductor is formed by doping an intrinsic Group IV semiconductor with N_D donor atoms of a Group V (pentavalent) element, such as Phosphorous (P), having five valence electrons. N_D is simply the number of donor atoms the intrinsic semiconductor is doped with. Similarly, a p-type semiconductor is formed by doping an intrinsic Group IV semiconductor with N_A acceptor atoms (where N_A is the number of dopant acceptor atoms) of a Group III (trivalent) element, such as Boron (B), having three valence electrons.

Since an n-type semiconductor is doped with extra electrons, its majority charge carriers are electrons while holes are the minority charge carriers. Conversely, holes are the majority charge carriers and electrons the minority charge carriers for p-type semiconductors. Both n-type and p-type semiconductors, however, are still neutrally charged since the dopant impurity atoms, P for n-type and B for p-type, are initially electrically neutral.

2.2 PN Junction Diode

A diode is created when a p-type and n-type semiconductor are joined, forming a PN junction. The symbol for a diode is shown below in Figure 2.4.
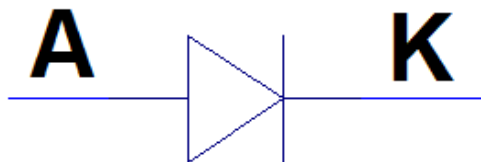
Figure 2.4 – Diode Symbol

The p-type acts as the anode (A) of the diode while the n-type acts as the cathode (K). In the region near the PN junction, some of the free majority carriers in the n-type (electrons) fill the holes in the p-type. The free carriers near the metallurgical junction combine and neutralize,

effectively vanishing. As a result, a thin region called the depletion region (since it is depleted of free carriers) is formed around the PN junction as shown in Figure 2.5 below.
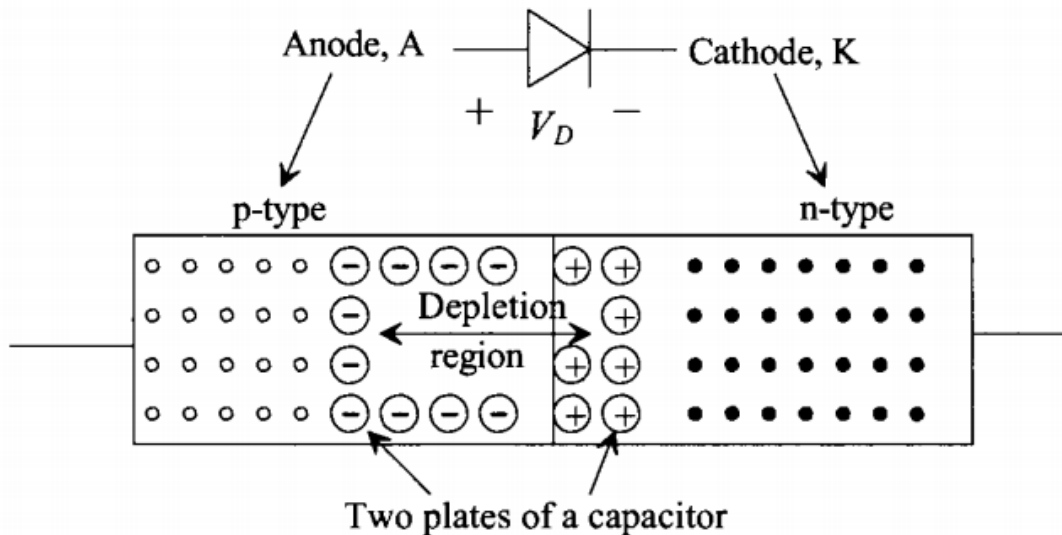
Figure 2.5 – PN Junction Depletion Region [10]

Notice the portion of the depletion region in the n-type contains only positive charges due to the positively charged dopant P atoms while the portion of the depletion region in the p-type contains only negative charges due to the negatively charged dopant B atoms. Thus, the depletion region is also known as a space charge region since it is the only region in the semiconductor material that has electrical charge.

Due to the net negative charge in the p-type side of the depletion region and the net positive charge in the n-type side of the depletion region, an electric field is created in the depletion region pointing from n-type to p-type (K to A). This also produces a junction voltage, or junction potential, across the depletion region. Figure 2.6 below shows the how the energy bands bend around the fermi level at the PN junction.
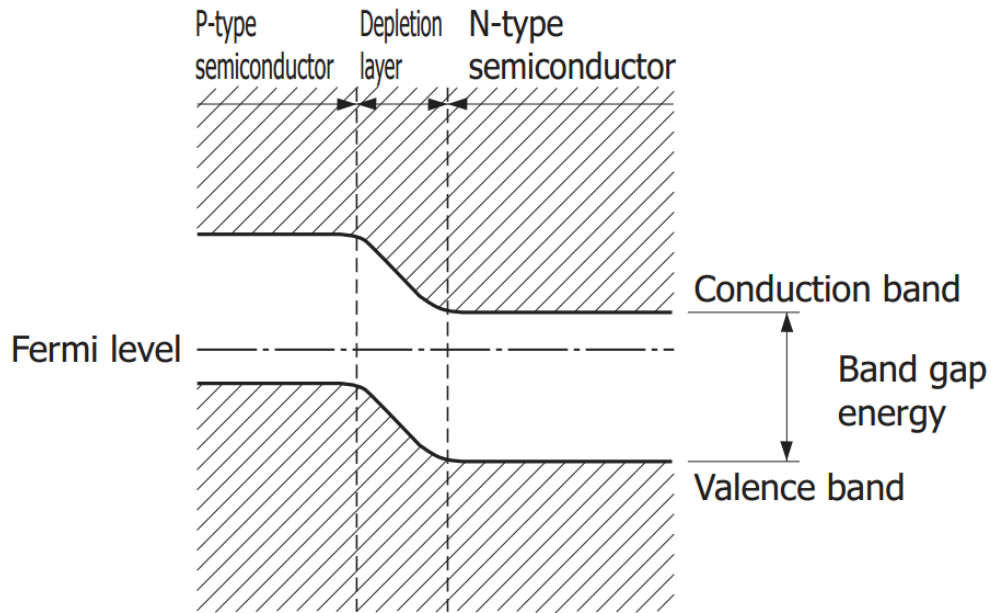
Figure 2.6 – PN Junction Energy Bands [11]

When the depletion region is initially formed, it is very thin, so the electric field and junction potential are relatively weak. Thus, majority carriers near the PN junction on opposite sides are attracted to one other enough to overcome the weak junction potential and electric field, allowing them to combine and neutralize, effectively vanishing. This, however, increases the width (and with it the electric field and voltage potential) of the depletion layer preventing additional free carriers from crossing the PN junction and combining. Thus, equilibrium is achieved. Also associated with the depletion region is a depletion, or junction, capacitance that is inversely proportional to the width of the depletion region as shown in Equation 2 below,

$$C = \frac{\varepsilon A}{d} \qquad\qquad \text{Equation 2}$$

where C is the depletion capacitance and d is the width of the depletion region.

If a PN junction diode is not biased with an external voltage, then the diode is under zero bias and thus operates in photovoltaic mode which is the principle for solar cells. If the diode is forward biased in which a higher potential is connected to the diode's anode and lower potential

connected to the diode's cathode, the diode will not conduct current until the external voltage exceeds, or overcomes, the junction potential of the diode. We are concerned, however, with reverse bias of PN junction diodes operating in photoconductive mode.

For reverse bias, higher potential is connected to the diode's cathode and lower potential connected to the diode's anode. The positive potential attracts electrons out of the n-type (or can be thought of as pushing holes in from the positive terminal of the battery which then combine with electrons in the n-type and neutralize/vanish), and the negative potential attracts holes out of the p-side (or can be thought of as pushing electrons in from the negative terminal of the battery which then combine with holes in the p-type and neutralize/vanish). As a result, the depletion region widens, and, thus, the depletion capacitance decreases. Under reverse bias, the diode current is negligible as it is in the nanoampere (nA) range.

Chapter 3: Photodiodes

3.1 Photodiode Basics

The PN junction diode is the basis for the simplest semiconductor photodetector, the photodiode. The symbol for a photodiode is shown below in Figure 3.1 below. Note its similarity to that of a regular diode except for the arrows indicating incident light.

A ◁ K
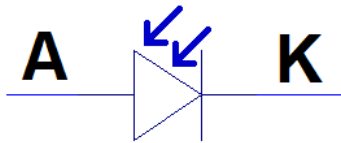
Figure 3.1 – Photodiode Symbol

When light is shined on a Si photodiode, photons strike, or collide with, the Si material in the depletion region (where there is an electric field). If the energy of an incident photon is greater than or equal to the band gap energy of Si ($E > E_g$), then it will knock one of the valence electrons of the impacted Si atom out of its covalent bond with a neighboring Si atom, generating an electron-hole (e-h) pair and resulting in photogenerated current (photocurrent) as illustrated below in Figure 3.2.
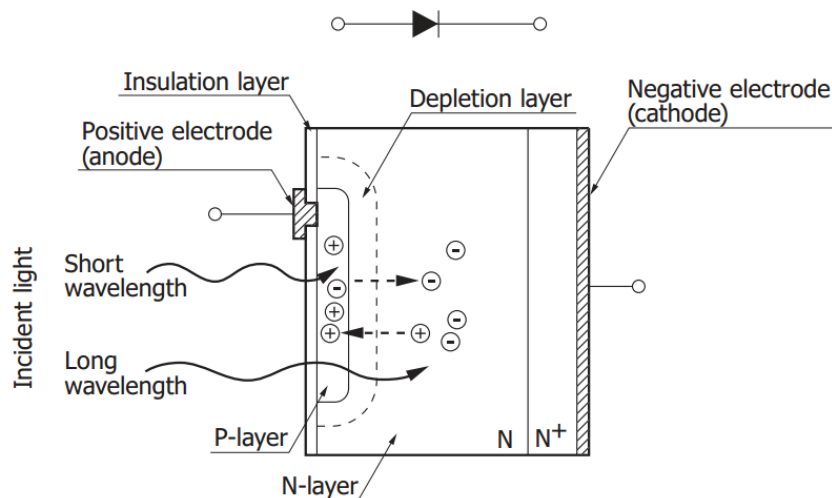
Figure 3.2 – Electron-Hole Pair Generation due to Incident Photons [12]

This phenomenon of absorbed light resulting in free electrons is known as the photoelectric effect.

Recall that wavelength and frequency are related by the speed of light as shown in Equation 3 below,

$$c = \lambda \times v$$
Equation 3

where λ is wavelength in meters, v is frequency in Hertz (Hz), and c is the speed of light in a vacuum (3.0 x 10^8 m/s). Thus, the energy of a photon is calculated using Equation 4 below,

$$E = hv = \frac{hc}{\lambda}$$
Equation 4

where h = 6.626 x 10^{-34} J-s (Planck's constant), v is the frequency of the photon in Hz, and E is the photon energy in Joules (J). Recall 1 eV = 1.602 x 10^{-19} J or 1 J = 6.242 x 10^{18} eV. It can be seen that the maximum cutoff wavelength (λ_c) that can be detected by a semiconductor material is inversely proportional to the material's band gap (E_g). Since wavelength and energy are inversely proportional, the wavelength of the incident light must be short enough in order to be detected by the photodiode since the energy of incident photons must be greater than or equal to the band gap energy of the semiconductor (Si for this discussion). This is shown by Equation 5 below,

$$\lambda_c = \frac{hc}{E_g} = \frac{1.24}{E_g}\ um$$
Equation 5

where E_g is the band gap of the semiconductor (in eV), and λ_c is the maximum cutoff wavelength in μm.

Recall that a photodiode is reverse-biased such that it operates in photoconductive mode. Photogenerated e-h pairs in the depletion region are affected by its electric field such that photogenerated electrons move toward the n-type (connected to higher potential) and their

respective holes toward the p-type (connected to lower potential). Since conventional current flow is defined as the opposite direction of electron flow, the direction of the hole movement (in the direction of the electric field) signifies the direction of photocurrent (reverse current). The magnitude of the photocurrent generated by a photodiode is proportional to the light level (intensity or brightness) as shown in the current-voltage (IV) plot in Figure 3.3 below.
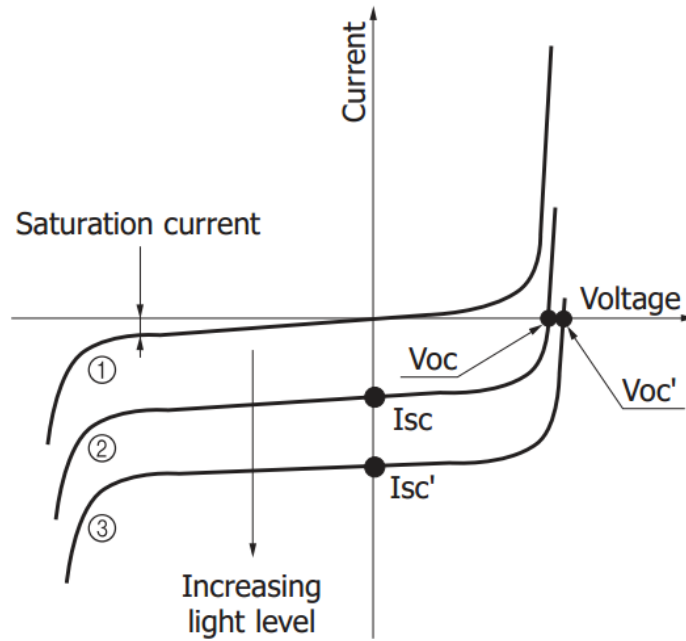
Figure 3.3 – Photodiode I-V Curve for Increasing Light Levels [13]

The light level is essentially determined by the number of incident photons per second as shown in Equation 6 below,

$$W = NE = Nh\nu = \frac{Nhc}{\lambda} \qquad \text{Equation 6}$$

where W is the light level, and N is the number of incident photons per second (pcs/s) [14].

3.2 Types of Photodiodes

In addition to the PN photodiode, similar devices such as PIN photodiodes and Schottky photodiodes exist and have slightly different properties, characteristics, operations, and

applications. The IR-enhanced PIN photodiode shown in Figure 3.4 below has drastically

improved sensitivity in the NIR region for wavelengths from 900nm to 1100nm [15].
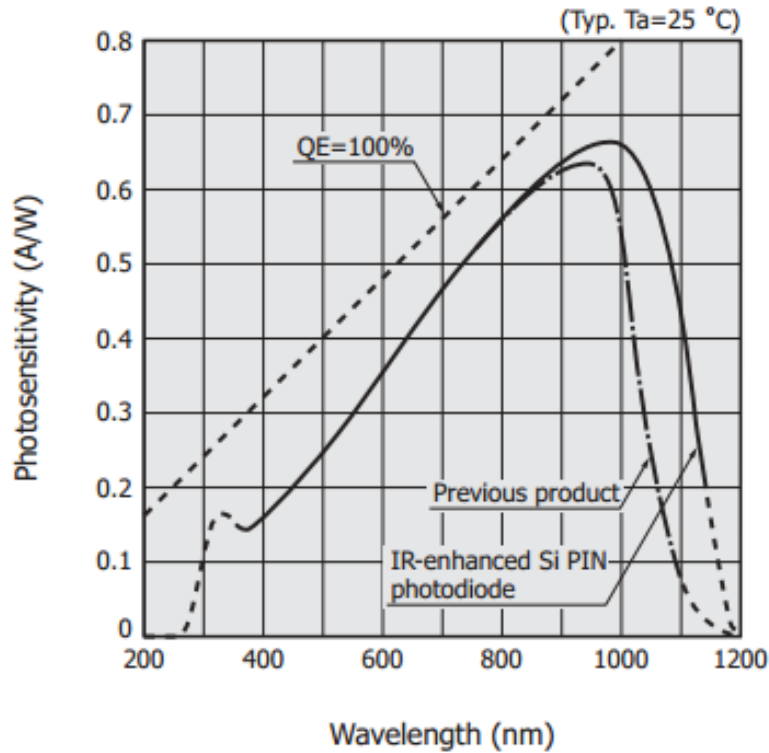
Figure 3.4 – Spectral Responsivity of IR-enhanced PIN photodiode [16]

An avalanche photodiode (APD) is a photodiode with a high internal (built-in first stage)

gain that results in an amplified photocurrent, allowing for measurement of low-level light

signals and higher signal-to-noise ratio (SNR) than PIN photodiodes [17]. For relatively low

reverse bias voltages, an APD operates as a normal photodiode in photoconductive mode. As the

applied reverse voltage increases, however, the APD enters linear mode in which avalanche

multiplication results. Avalanche multiplication is due to the electric field becoming so strong in

the high gain avalanche region, shown in Figure 3.5 below, that primary photogenerated carriers

(e-h pairs) are accelerated with enough kinetic energy to knock loose secondary carriers from

impacted Si atoms. The secondary carriers, in turn, knock loose more and more tertiary e-h pairs

and so on resulting in an avalanche effect.
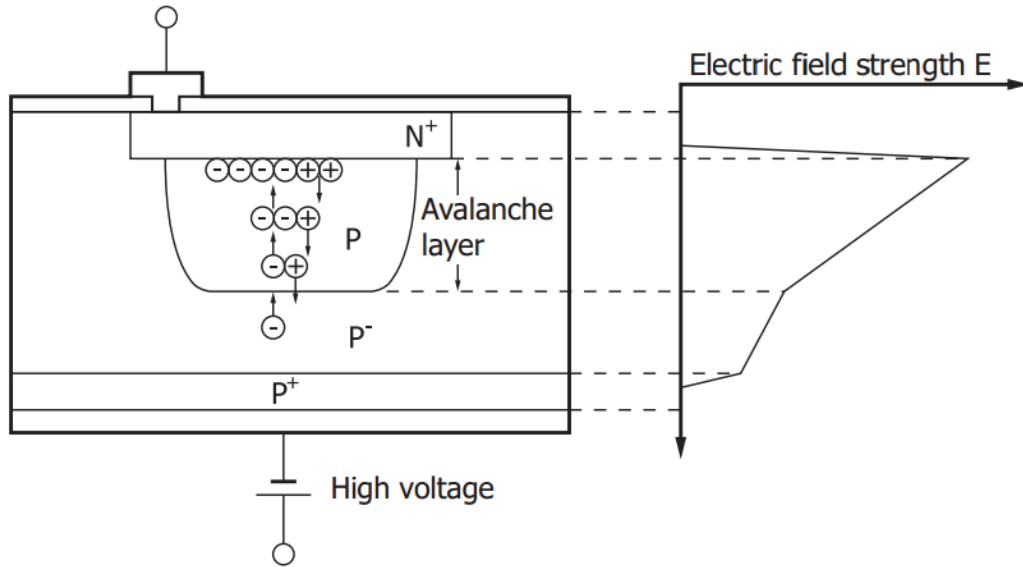
Figure 3.5 – Avalanche Multiplication in an APD [18]

As the reverse bias voltage is increased further to the breakdown voltage, an abrupt increase in current will occur, and the APD is said to operate in the Geiger mode allowing for the possibility of single photon detection. Figure 3.6 below shows an I-V plot detailing photoconductive, linear, and Geiger mode.
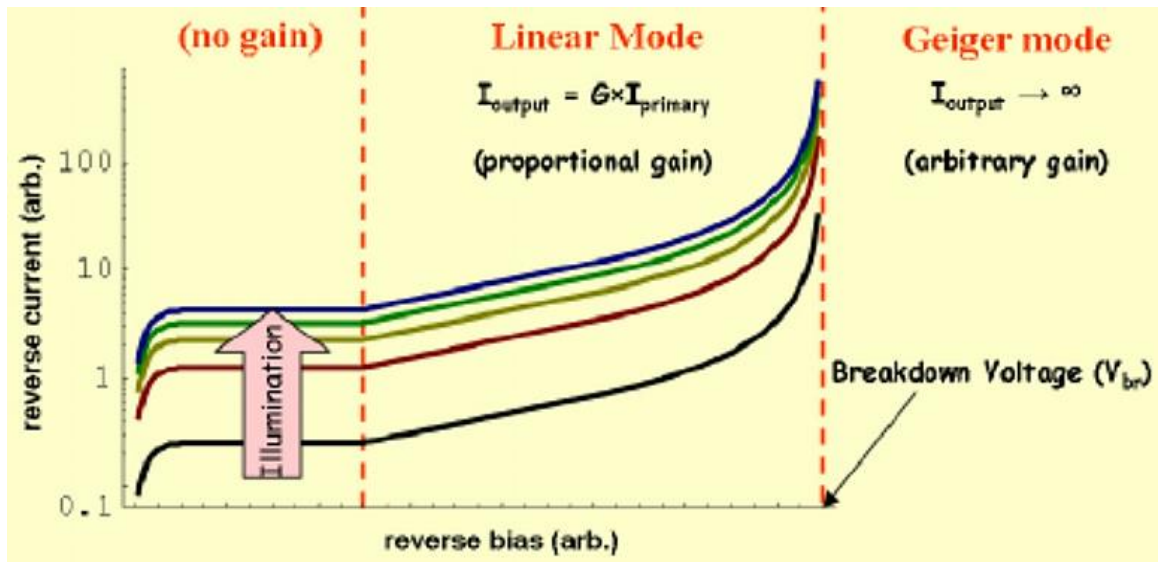
Figure 3.6 – Photoconductive, Linear, and Geiger Mode on I-V Plot [19]

It is worth commenting at this point that photodiodes operate under reverse bias since an apparent fractional change in current is noticeable for varying intensity of incident light. If the photodiode were operated under forward bias, the difference in current magnitudes is virtually unnoticeable. In addition, the depletion region is much thinner under forward bias, so there is a smaller electric field and less photoactive area to absorb incident light.

Whereas APDs are typically operated slightly below the breakdown voltage in linear mode, a single-photon avalanche diode (SPAD) is an APD designed to operate exclusively beyond the breakdown voltage in Geiger mode. Thus, a single charge carrier is capable of causing a self-sustaining avalanche. As some authors refer to SPADs as Geiger-mode APDs (GmAPD), we will simply, for convenience, use APD as a blanket term regardless of the mode of operation throughout the remainder of this paper.

A silicon photomultiplier (SiPM), also known as a multi-pixel photon counter (MPPC), is an array of multiple APD pixels connected in parallel and operating in Geiger mode. A SiPM is capable of detecting weaker light levels than a single APD due to its significantly higher gain and also has single-photon counting capability [20]. A SiPM outputs a pulse with amplitude corresponding to the number of pixels that detect a photon at a given time. Each pixel is only capable of producing a pulse with amplitude corresponding to one photon, so an output pulse corresponding to a pixel detecting one photon is identical to an output pulse corresponding to a pixel detecting more than one photon at time. Thus, it is necessary for a SiPM to have enough pixels to match the number of incident photons.

3.3 Photodiode Parameters

An ideal photodiode would not generate any current under a dark state in which no light is incident on the photodiode. In practical photodiodes, however, a small undesirable current

called dark current exists even in a dark state. Dark pulses are pulses of current due to thermal generation of carriers in a SiPM or APD operated in Geiger mode. The number of dark pulses is referred to as the dark count while the number of dark pulses per second is defined as the dark count rate (DCR) with units of counts per second (cps). Since dark counts lead to detection errors, it is desired to minimize the number of dark counts in an APD. Dark counts increase with increasing reverse voltage and can be reduced by lowering the temperature. Figure 3.7 below shows the indistinguishable nature of dark counts from true output signal pulses in a SiPM.
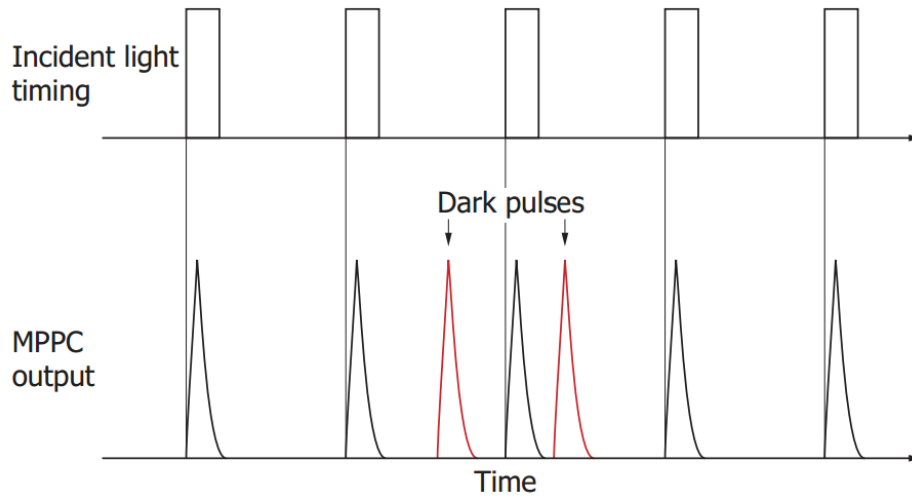
Figure 3.7 – Dark Pulses in a SiPM [21]

The gain, *M*, of an APD is expressed as the ratio of the number of carriers that are output after avalanche multiplication to the number of primary carriers. *M* is calculated as in Equation 7 below,

$$M = \frac{I_p}{I_{p0}}$$
Equation 7

where I_p is the multiplied photocurrent resulting from a high reverse voltage, and I_{p0} is the photocurrent (that doesn't experience multiplication) resulting from a low reverse bias voltage. Quantum efficiency (QE) is defined, for a SiPM, as the probability that carriers will be generated by light incident on a pixel and is dependent on the wavelength of the incident light. For a SiPM,

responsivity, or photosensitivity, (S; unit: A/W) is the ratio of output photocurrent (I_{SiPM}) to the incident light level (unit: W) and is expressed by Equation 8 below.

$$S = \frac{I_{SiPM}}{Incident\ Light\ Level}$$
Equation 8

Photosensitivity is proportional to gain and, therefore, increases with reverse voltage. The spectral responsivity (S vs. λ) and responsivity as a function of reverse bias voltage (S vs. V) for a Hamamatsu Si SiPM with a pixel pitch of 25μm is shown in Figure 3.8 below.
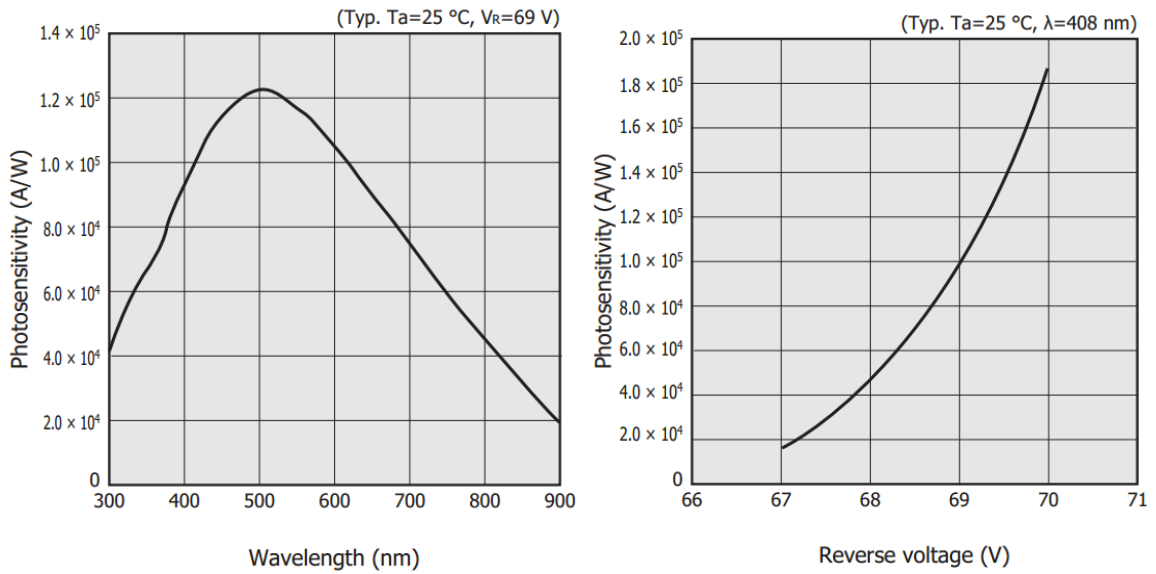
Figure 3.8 – S vs. λ (left) and S vs. Reverse Voltage (right) for a Hamamatsu Si SiPM [22]

For a SiPM, photon detection efficiency (*PDE*), expressed by Equation 9 below, is a ratio of the number of detected photons to the number of incident photons during photon counting.

$$PDE = \frac{\#\ of\ detected\ photons}{\#\ of\ incident\ photons}$$
Equation 9

PDE can also be expressed as the product of fill factor (*Fg*), *QE*, and avalanche probability (*Pa*) as shown in Equation 10 below,

$$PDE = Fg \times QE \times Pa$$
Equation 10

where *Fg* is the ratio of photosensitive (light detectable) area to the total area of the APD or SiPM, and *Pa* is the probability that avalanche multiplication will occur due to carriers generated in a pixel [23]. Figure 3.9 below shows PDE as a function of wavelength (PDE vs. λ) and PDE as a function of reverse voltage (PDE vs. V) for a Hamamatsu Si SiPM with a pixel pitch of 25μm.
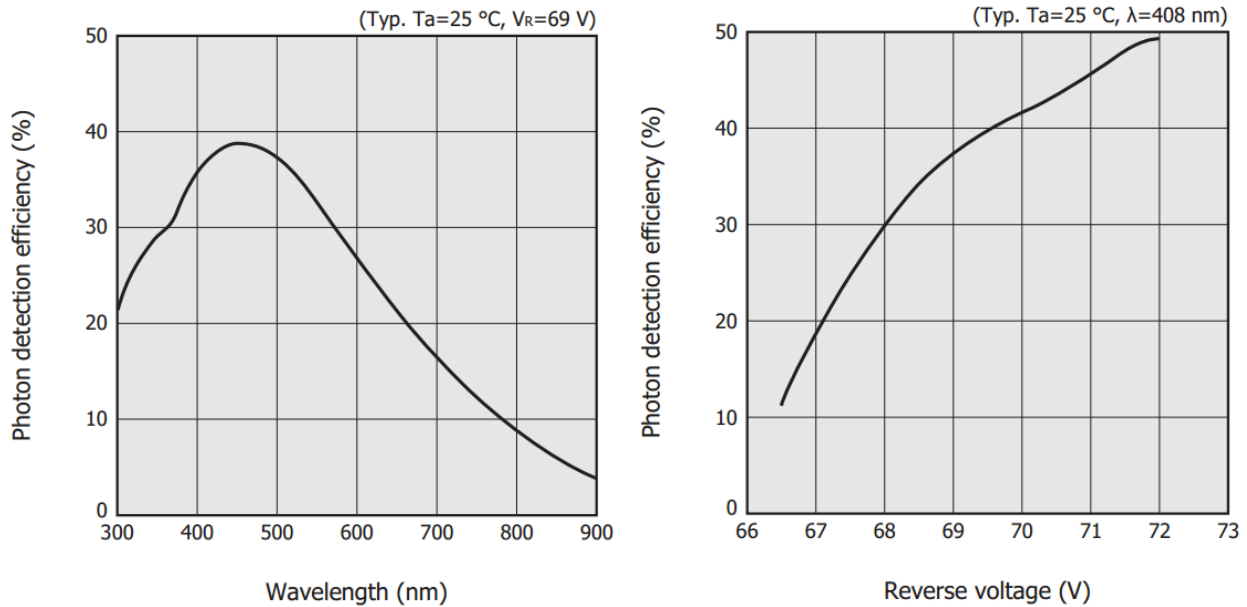
Figure 3.9 – PDE vs. λ (left) and PDE vs. Reverse Voltage (right) for a Hamamatsu Si SiPM [24]

In order to detect a single photon, an APD is operated in Geiger mode at a reverse voltage above its breakdown voltage. As a result, a saturation output called Geiger discharge, independent of the light level, is produced and continues as long as the high electric field is maintained. Therefore, an external circuit such as a quenching resistor (R_Q) (passive quenching), shown in Figure 3.10 below, connected in series with the APD must be used in order to lower the operating, or bias, voltage back down below the breakdown voltage and cease the Geiger discharge.
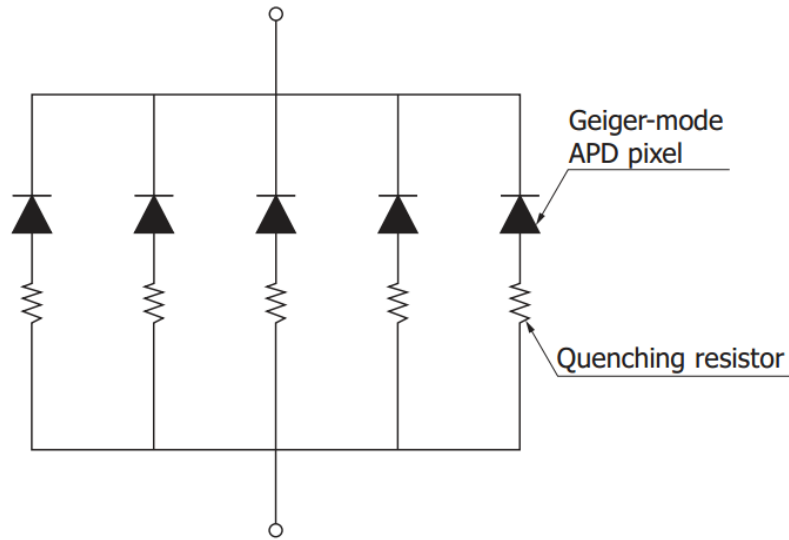
Figure 3.10 – Passive Quenching Resistor in Series with Geiger-mode APD Pixel [25]

When the output current due to Geiger discharge flows through the resistor, a voltage drop occurs and stops the avalanche multiplication, allowing for detection of the next photon as shown in Figure 3.11 below.
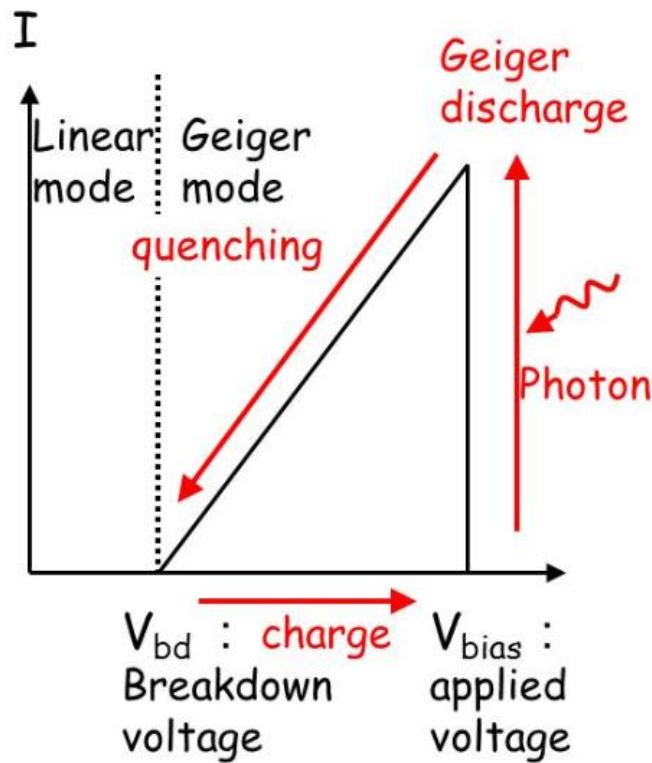
Figure 3.11 – Passive Quenching Operation on Geiger-mode APD I-V Curve [26]

A phenomenon termed crosstalk can cause detection errors in a SiPM by a primary electrical discharge, resulting from a pixel detecting a photon, leaking into a neighboring adjacent pixel. Crosstalk is the result of secondary photons being generated by an incident photon through the avalanche multiplication process of the pixel and the secondary photons being detected by other pixels in the SiPM. Crosstalk is almost independent of temperature but increases with reverse voltage. In addition, undesirable afterpulses may occur as a delayed pseudo signal resulting from the true signal output pulse. Afterpulses are due to generated carriers being trapped by defects in the crystal lattice then released after some delay time. Afterpulses are another cause of detection errors and increase with decreasing temperature due to a higher probability of generated carriers being trapped by crystal defects.

4.1 Research Foundations

Figure 4.1 below shows the layout and corresponding cross-sectional view of a 10μm x 10μm Si APD designed in Electric and fabricated in ON Semiconductor's C5 (500nm = 0.5μm = 0.5 Micron) process.
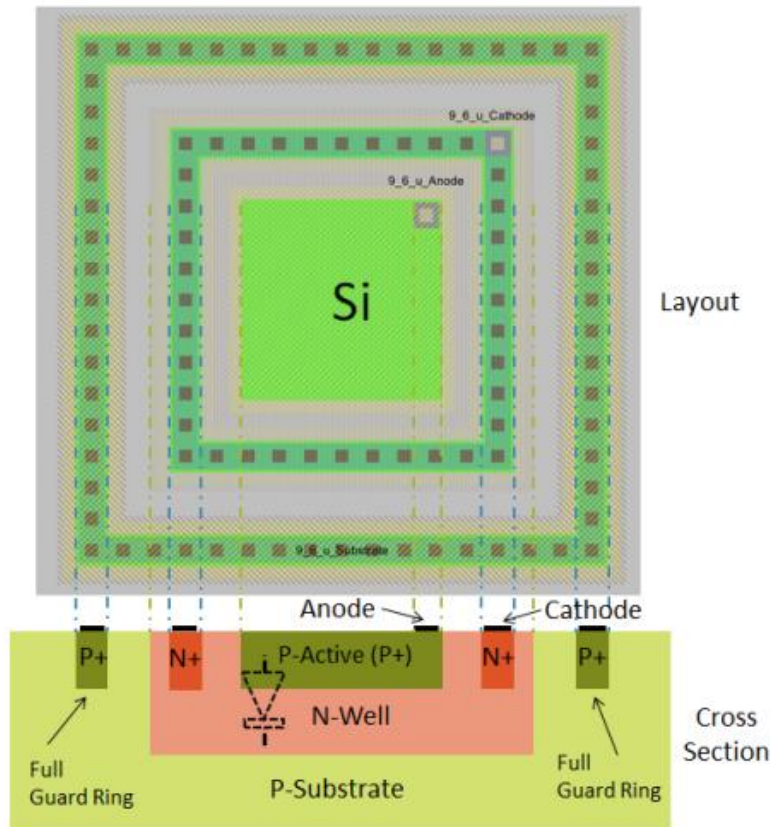
Figure 4.1 – Layout of 10μ Si APD

Note the diode formed between the P+ and N-Well in the cross section. Also, notice the presence of a full guard ring for preventing premature edge breakdown [27]. The presented research consists of characterization of the performance and properties of APDs fabricated using SiGe due to the lower band gap of SiGe compared to Si, allowing for detection of higher wavelengths. Using Equation 5 from Chapter 3, pg. 11, the maximum λ_c for Si, which has a band gap energy

of 1.12eV, is 1100 nm. Ge, however, has a lower band gap of 0.67 eV which yields a higher λ_c of

1850 nm. The concentration of Ge in SiGe is typically 12% which results in a band gap of 1.00

eV, yielding a λ_c of 1240nm. These results are summarized in Table 4.1 below.

Composition	Band Gap (E_g)	Maximum Cutoff Wavelength (λ_c)
Si	1.12 eV	1100 nm
Ge	0.67 eV	1850 nm
SiGe (12% Ge concentration)	1.00 eV	1240 nm

Table 4.1 – Maximum Cutoff Wavelength vs. Band Gap Energy for Si, Ge, and SiGe

Since SiGe optical devices exhibit extended infrared (IR) response compared to Si,

various APD test structures were laid out in the AMS S35 process which allows for both high-

speed optical devices and electronic circuits on the same chip. The APD variants were fabricated

and tested in order to investigate the effect on the APDs performance, characteristics, and

properties for different sizes, structures, layers, geometries, etc. Furthermore, one main goal of

this research is to determine what layers the SiGe contribution comes from. The cross-sectional

view for high speed (3.3V) and high voltage (5V) HBT modules in the S35 process is shown

below in Figure 4.2.
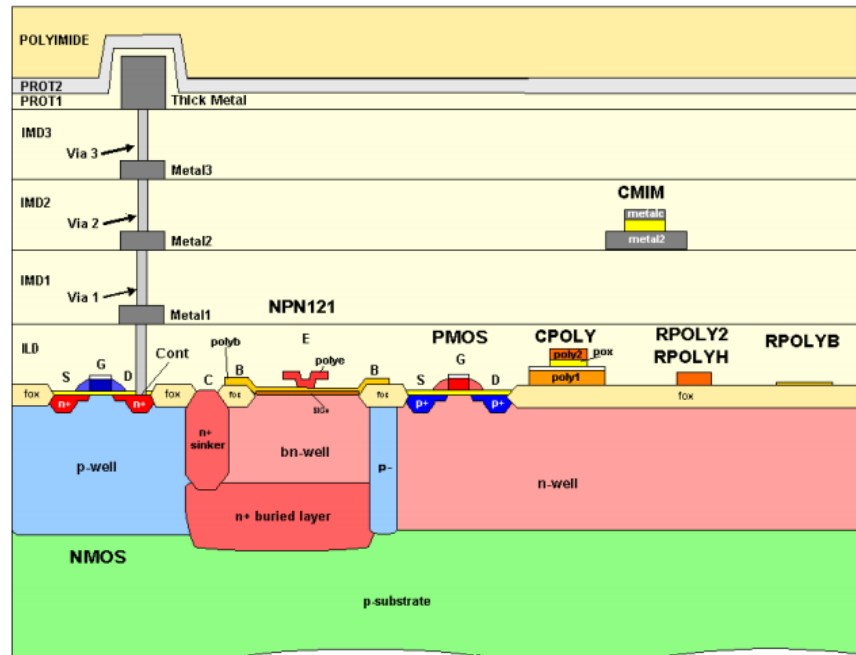
Figure 4.2 – Cross Section for High Speed and High Voltage HBT Modules in S35 Process

[28]

The S35 layers referenced throughout the remainder of this paper are presented in Table 4.2

below [29].

Layer	Layer Description
BNTUB (WB)	n-tub layer for bipolar transistors
BNTUB2 (WB2)	n-tub layer for high voltage BJT's (encloses BNTUB)
NTUB (NW)	n-tub layer
NBUR (BN)	n+ buried layer
DIFF (OD)	diffusion layer
COLL (IS)	sinker implant layer
BPOLY (BP)	base poly layer
EPOLY (PE)	emitter poly layer
EMITT (EC)	emitter opening layer
NPLUS (NP)	n+ implant layer
PPLUS (PP)	p+ implant layer
CONT (CO)	contact layer (connects MET1 to DIFF/BPOLY/EPOLY)
MET1 (M1)	metal1 layer

Table 4.2 – Relevant S35 Layers

4.2 Elementary APD

Figure 4.3 below shows the Cadence layouts and cross-sectional views of a SiGe NPN

high voltage (5V) HBT in the S35 process as well as the SiGe NPN modified to create a two

terminal device, an APD. This was done by deleting the emitter poly layer (EPOLY) in order to

allow light to strike the SiGe. By deleting EPOLY, the emitter of the NPN is removed and results

in a PN structure (APD) where P is the base (anode) and N is the collector (cathode).

23
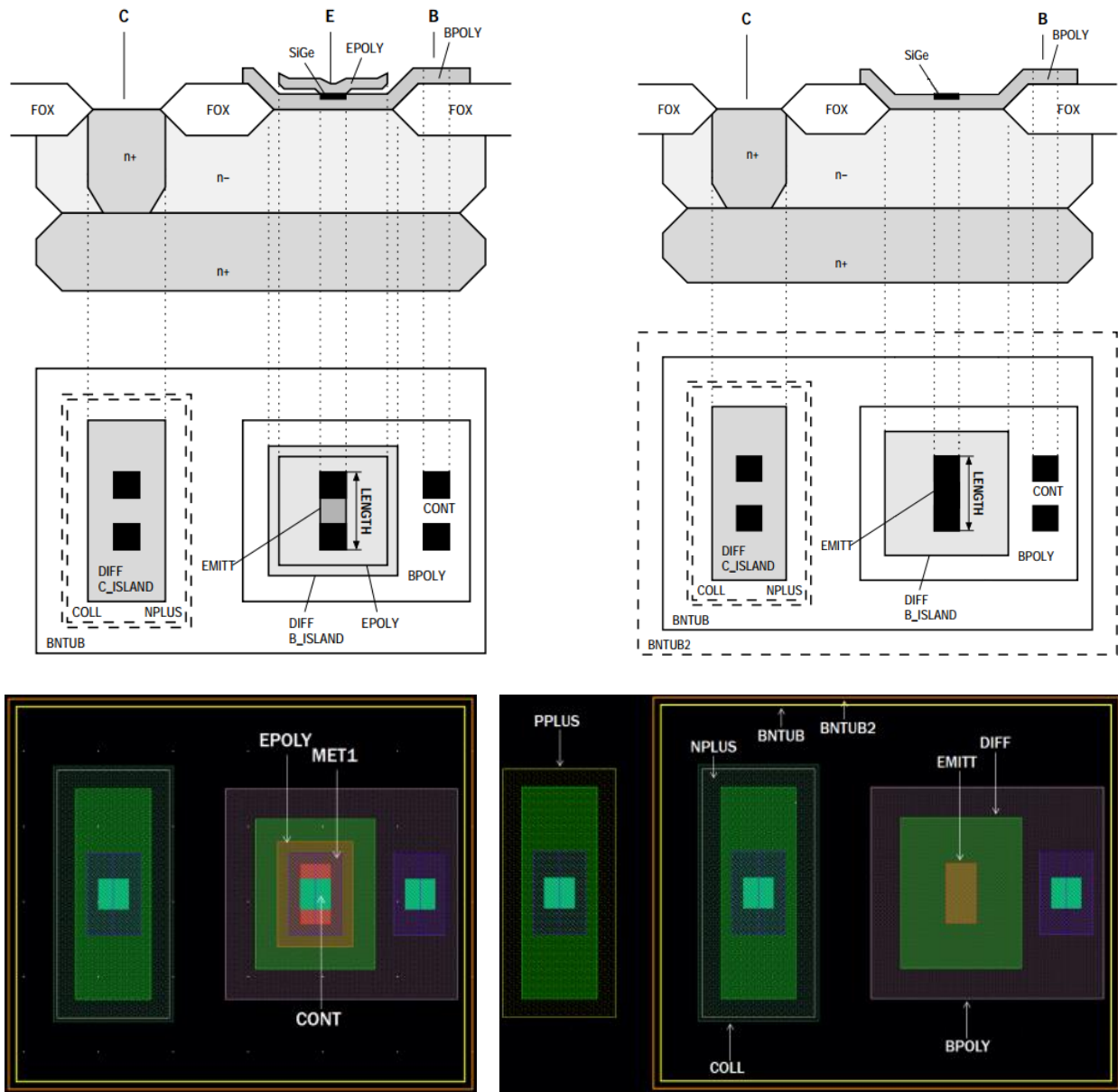
Figure 4.3 – Cross Section and Layout for SiGe NPN High Voltage (5V) HBT (left) and Modified NPN (APD) (right) [30]

The metal1 (MET1) and contact (CONT), which connects MET1 to EPOLY, layers around the emitter opening layer (EMITT) were also deleted. Also note that a P-substrate connection (guard ring) was added to the modified SiGe NPN (APD). The P-substrate connection consists of the P+ implant layer (PPLUS), the diffusion layer (DIFF), MET1, and CONT (which connects MET1 to DIFF).

The dimensions of EMITT are 0.4μm x 0.8μm (minimum size) and signifies the active area of the APD. Additional base (anode) and collector (cathode) contacts (CONT) were added in MET1 rings around the active area (EMITT) of the APD to ensure proper connection. P-substrate (guard ring) contacts were also added, yielding the basis of the APDs presented throughout the remainder of this paper. This base case APD is classified as the Minimum Partial Guard Ring (Min-P) APD and is shown in Figure 5.2 in Chapter 5, pg. 28. Modifying the Min-P APD such that the P-substrate rings around the entire APD results in the Minimum Full Guard Ring (Min-F) APD, shown in Figure 5.3 in Chapter 5, pg. 28.

Chapter 5: Chip Design, Layout, and Fabrication

5.1 Description of Chips

Three IC chips containing numerous APD variants were designed and laid out by the researchers and submitted to MOSIS for fabrication. Chip 1 was received and tested, Chip 2 is expected to be received in November 2018, and Chip 3 is expected to be received in January 2019. Though it was necessary to violate certain DRC rules for various APD designs, all APDs were designed with minimal DRC errors and laid out to be as small as possible for each respective variant in order to conserve space.

5.2 Chip 1

Chip 1 has 53 pads containing 6 APD test structures, a single SiPM pixel, and a 16 x 16 SiPM array. The APD variants are partial and full guard rings structures with EMITT layer dimensions of 0.4μm x 0.8μm (minimum), 5μm x 5μm, and 24μm x 24μm (maximum). The SiPM pixel is comprised of the 24μm full guard ring structure with a 350kΩ serpentine resistor in series with its cathode. The SiPM array is comprised of 256 SiPM pixels connected in parallel and arranged in a 16x16 array. Figure 5.1 below shows the design of the chip in Cadence.
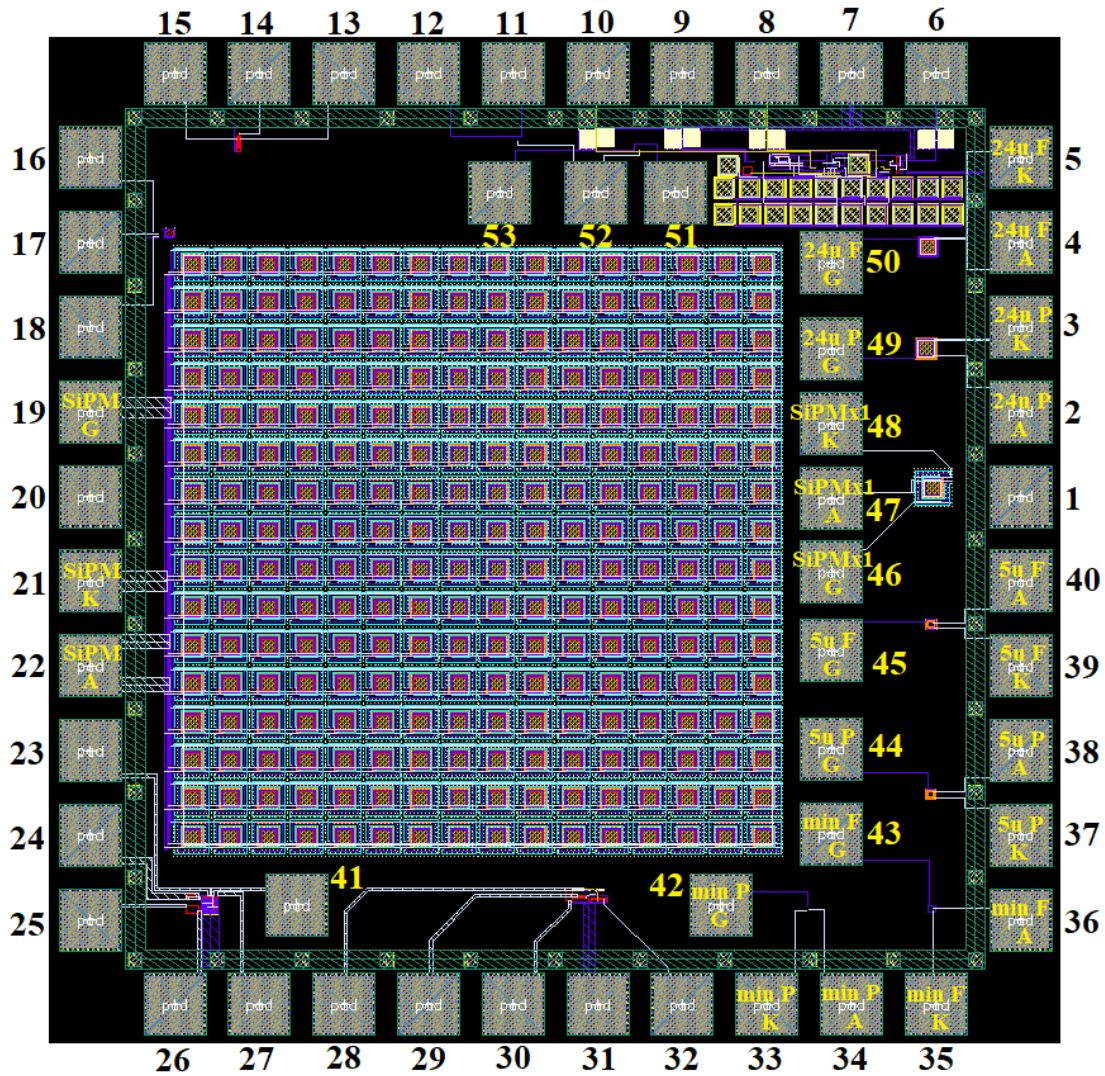
Figure 5.1 – Cadence Layout of Chip 1

Note the use of interior pads in order to maximize space. The pin table for Chip 1 is shown in Table 5.1 below. A "P" signifies partial guard ring while "F" signifies full guard ring.

APD	Anode (A)	Cathode (K)	Guard Ring (G)
Min-P	34	33	42
Min-F	36	35	43
5μ-P	38	37	44
5μ-F	40	39	46
24μ-P	2	3	49
24μ-F	4	5	50
SiPM Pixel	47	48	46
SiPM Array	22	21	19

Table 5.1 – Chip 1 Pin Table

The layouts of each APD are shown in Figures 5.2 through 5.9 below.
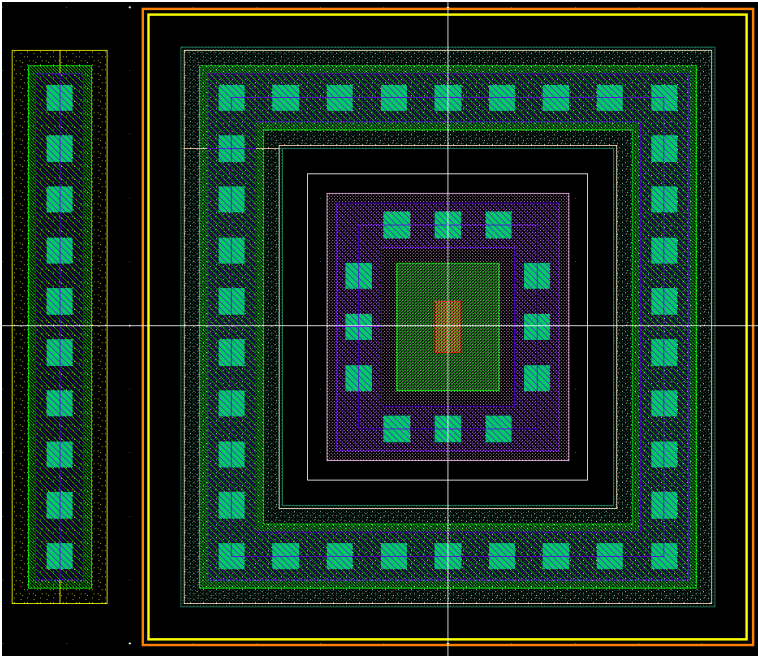
Figure 5.2 – Cadence Layout of Min-P
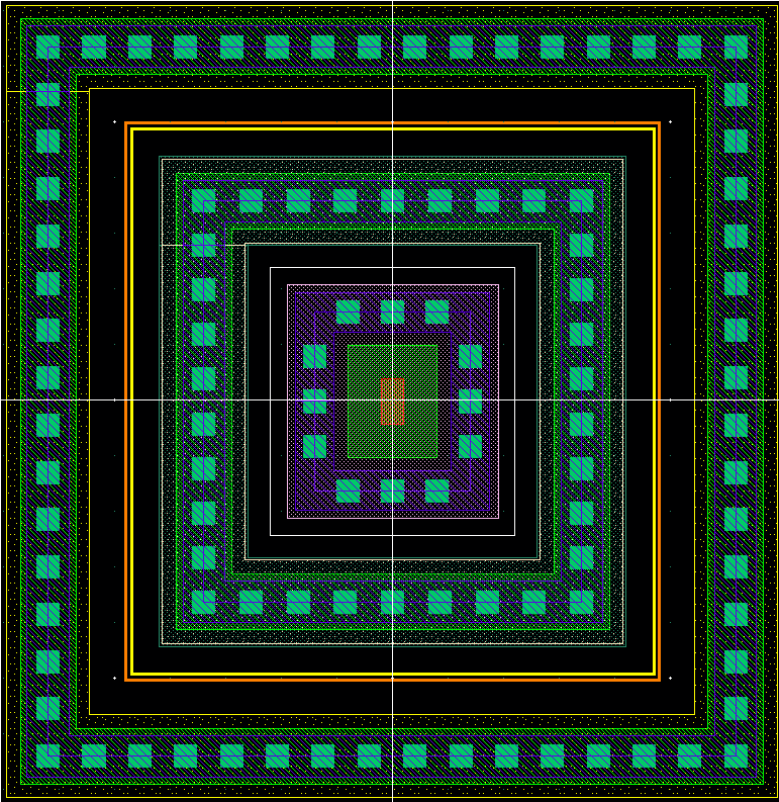
Figure 5.3 – Cadence Layout of Min-F
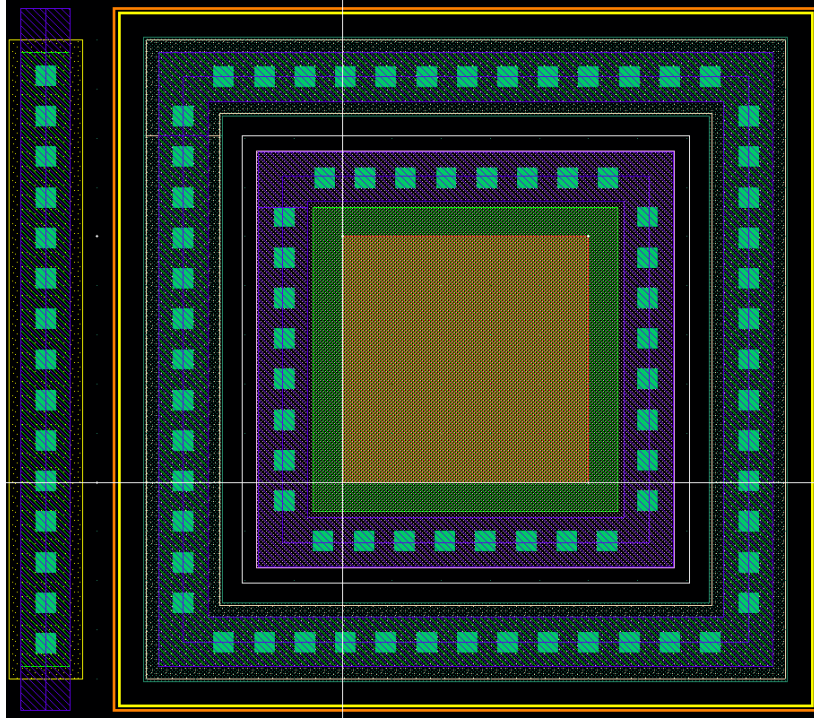
Figure 5.4 – Cadence Layout of 5μ-P
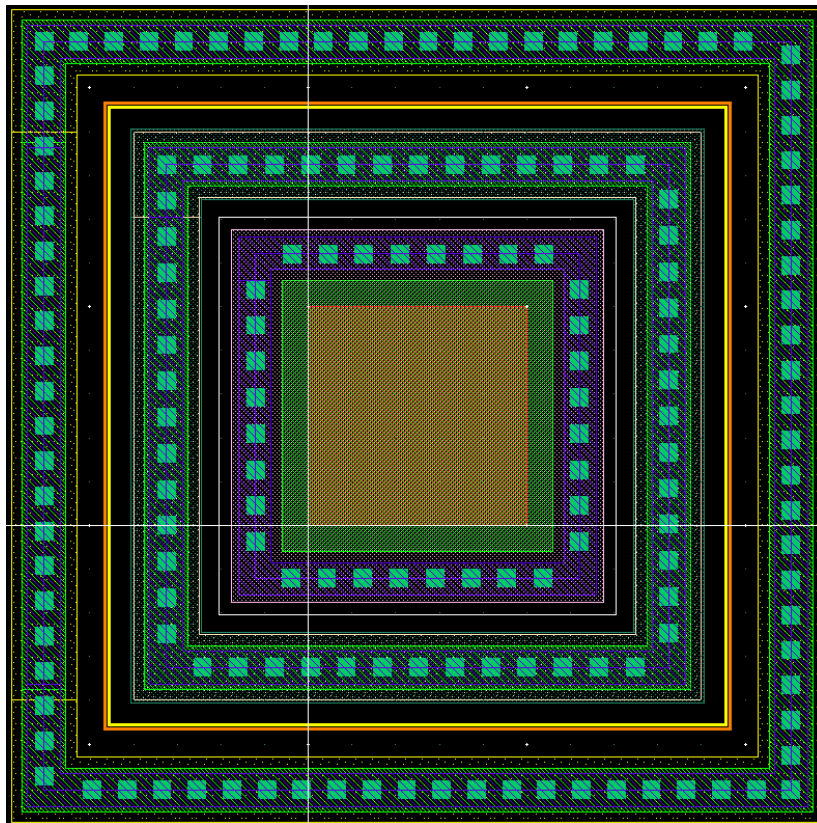
Figure 5.5 – Cadence Layout of 5μ-F
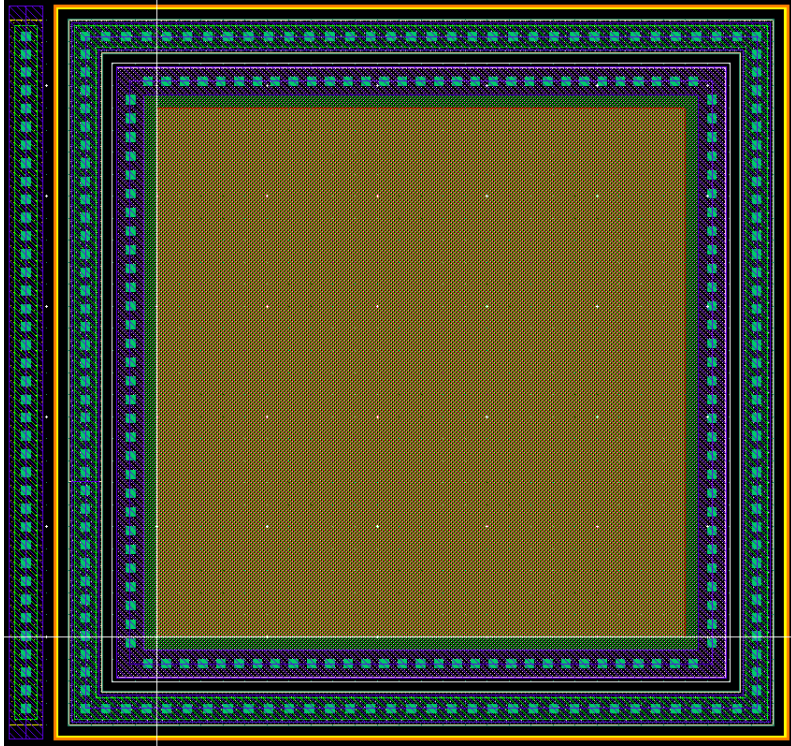
Figure 5.6 – Cadence Layout of 24µ-P
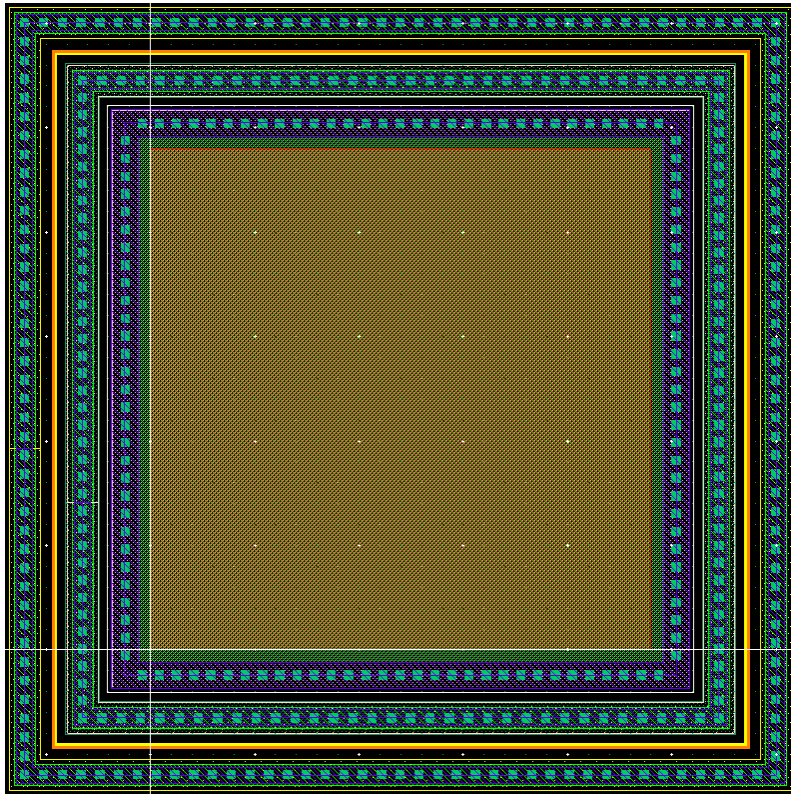
Figure 5.7 – Cadence Layout of 24µ-F
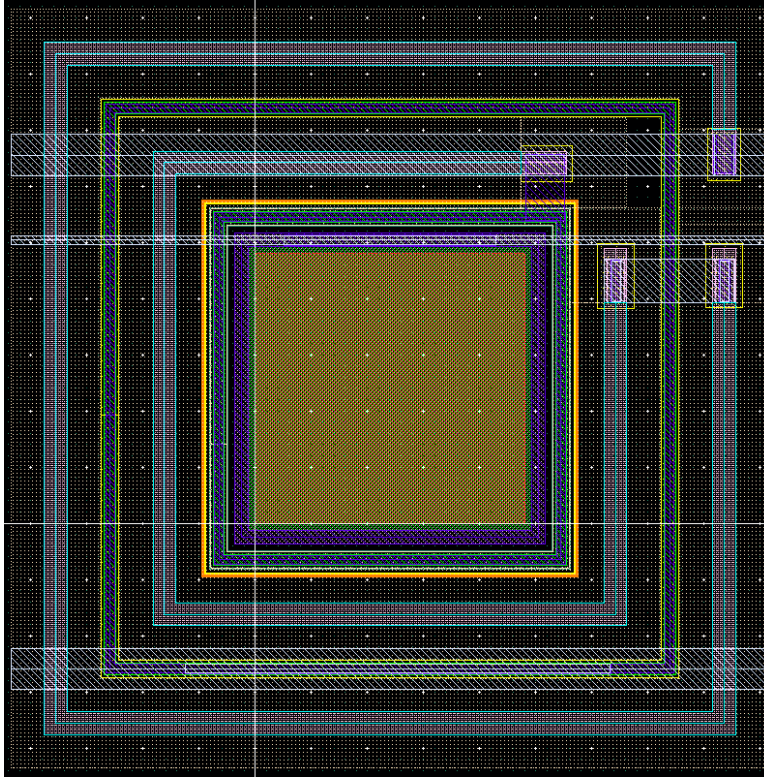
Figure 5.8 – Cadence Layout of SiPM Pixel (24µ-F w/ 350kΩ serpentine resistor)

Figure 5.9 – Cadence Layout of SiPM Array (16x16 Array of SiPM pixels)

Figure 5.10 below shows the layouts and corresponding cross-sectional views of the 5μ-P and 5μ-F APDs for comparison to the 10μ Si APD in Figure 4.1 in Chapter 4, pg. 21. Note the presence of the graded SiGe in the active area of the APD.
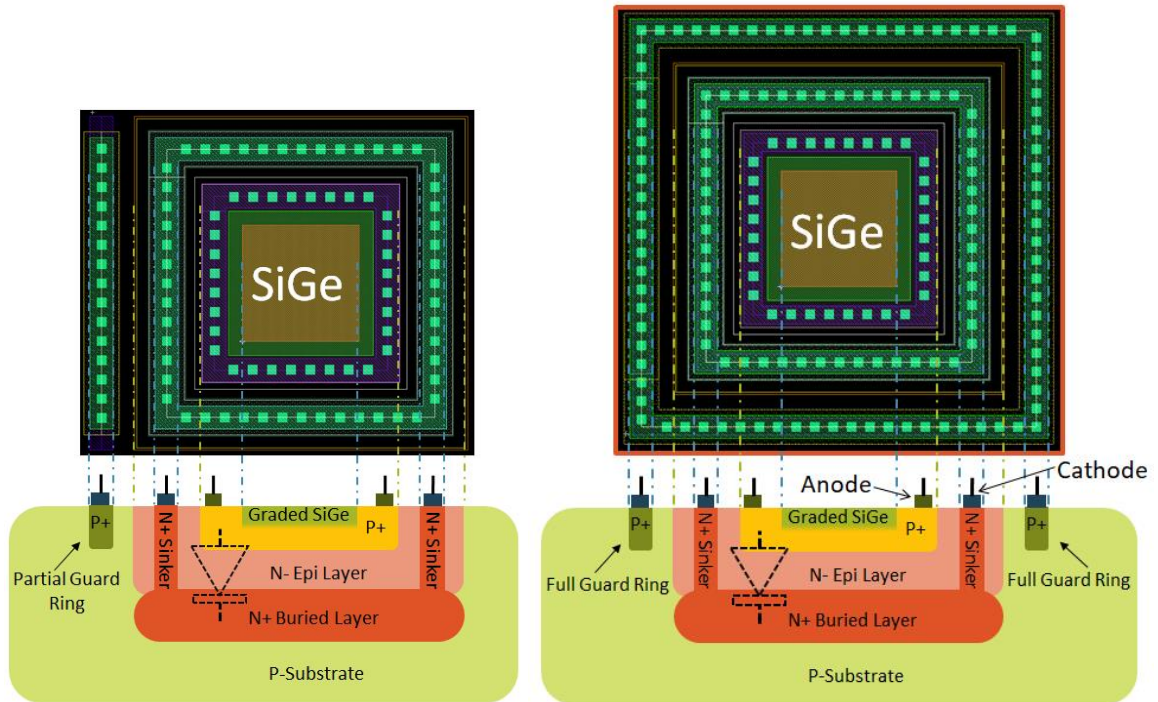
Figure 5.10 – Cadence Layout and Cross Section of 5μ-P (left) and 5μ-F (right)

Figure 5.11 below shows the fabricated chip.
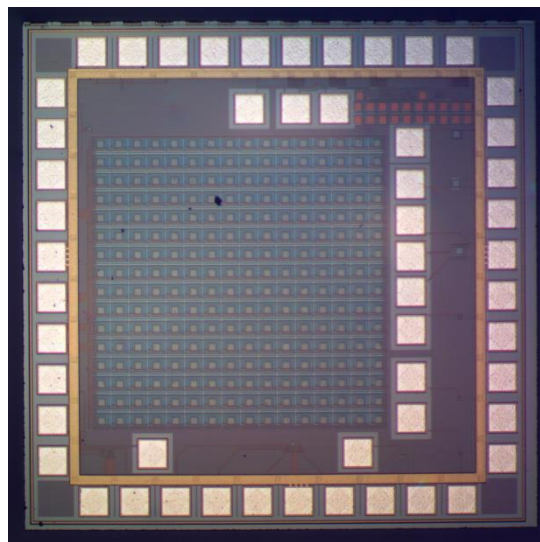
Figure 5.11 – Fabricated Chip 1

The fabricated chip die was wire bonded to SOIC-28 packages, using the K & S 4526 Wire

Bonder in the lab at UNLV shown in Figure 5.12 below, according to the two bonding diagrams

shown in Figure 5.13 below.

Figure 5.12 – K & S 4526 Wire Bonder [31]
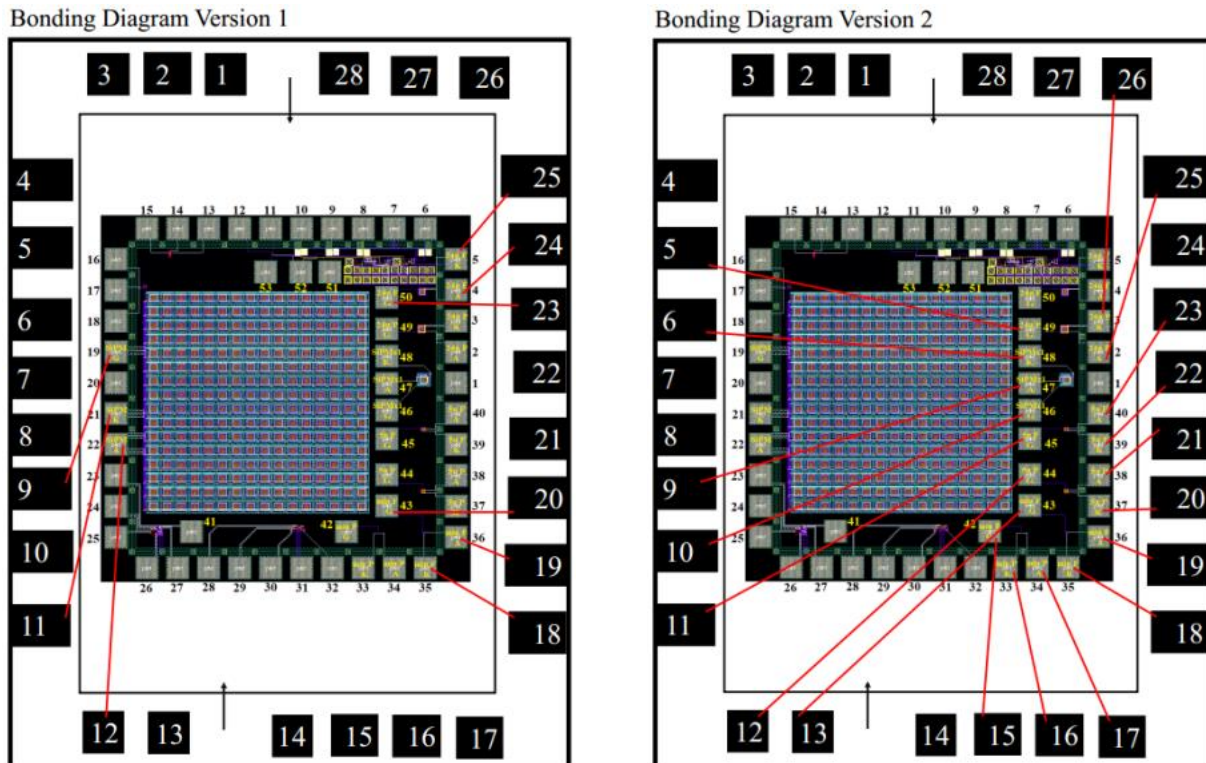
Figure 5.13 – SOIC-28 Bonding Diagram Version 1 (left) and Version 2 (right) for Chip 1

Tables 5.2 and 5.3 below show the bonding tables for Chip 1.

APD	Anode (A)		Cathode (K)		Guard Ring (G)	
	Chip Pin #	Package Pin #	Chip Pin #	Package Pin #	Chip Pin #	Package Pin #
Min-F	36	19	35	18	43	20
24μ-F	4	24	5	25	50	23
SiPM Array	22	12	21	11	19	9

Table 5.2 – SOIC-28 Package Bonding Table Version 1 for Chip 1

APD	Anode (A)		Cathode (K)		Guard Ring (G)	
	Chip Pin #	Package Pin #	Chip Pin #	Package Pin #	Chip Pin #	Package Pin #
Min-P	34	17	33	16	42	15
Min-F	36	19	35	18	43	13
5μ-P	38	21	37	20	44	12
5μ-F	40	23	39	22	46	11
24μ-P	2	25	3	26	49	5
SiPM Pixel	47	9	48	6	50	10

Table 5.3 – SOIC-28 Package Bonding Table Version 2 for Chip 1

The SOIC-28 package was then soldered to its respective printed circuit board (PCB) as shown in Figure 5.14 below.
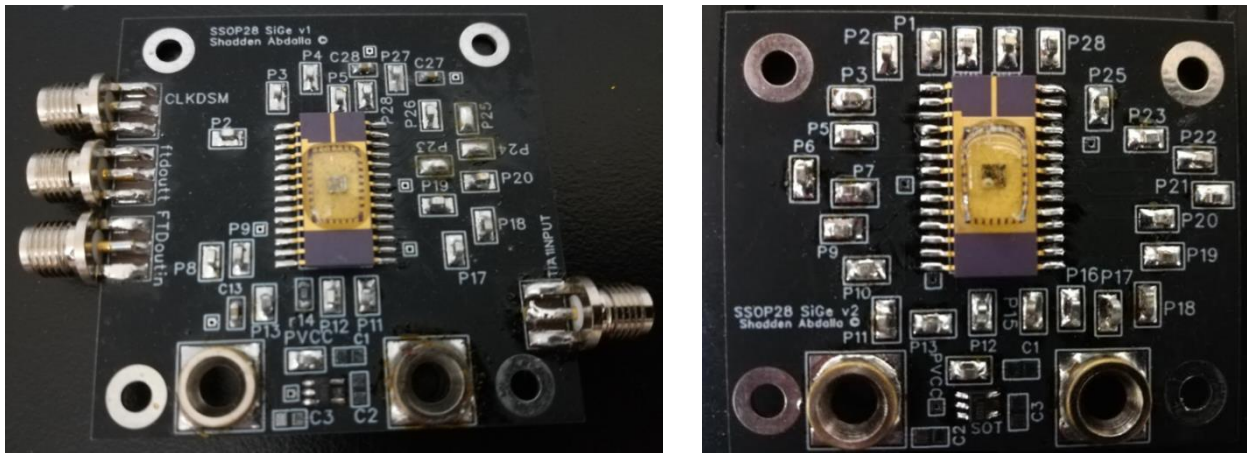
Figure 5.14 – SOIC-28 Soldered to PCB Version 1 (left) and Version 2 (right) for Chip 1

The PCBs were designed using FreePCB as shown in Figure 5.15 below.
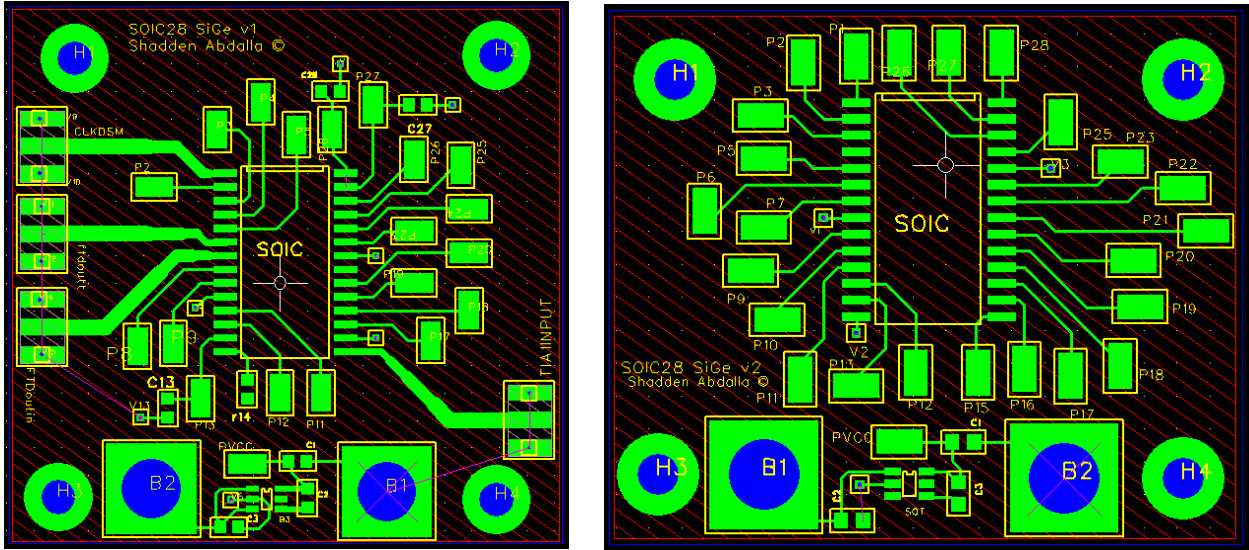
Figure 5.15 – PCB Design Version 1 (left) and Version 2 (right) for Chip 1

The fabricated chip die was also wire bonded to a TO-8 package according to the bonding

diagram shown in Figure 5.16 below as well as those in Appendix 5a.
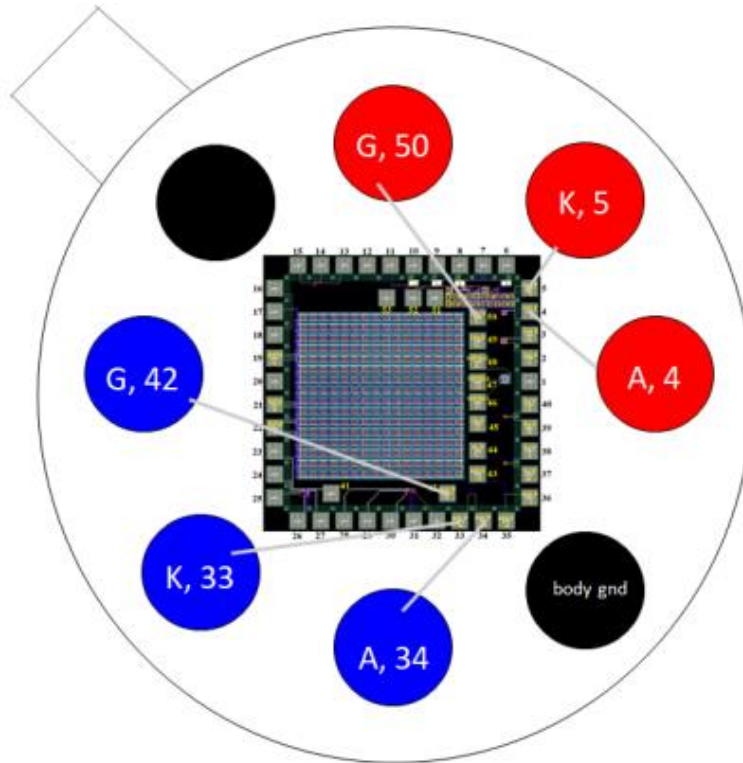
Figure 5.16 – TO-8 Package Bonding Diagram Version 1 for Chip 1

Note each TO-8 is bonded in the same manner as shown in Figure 5.17 below.
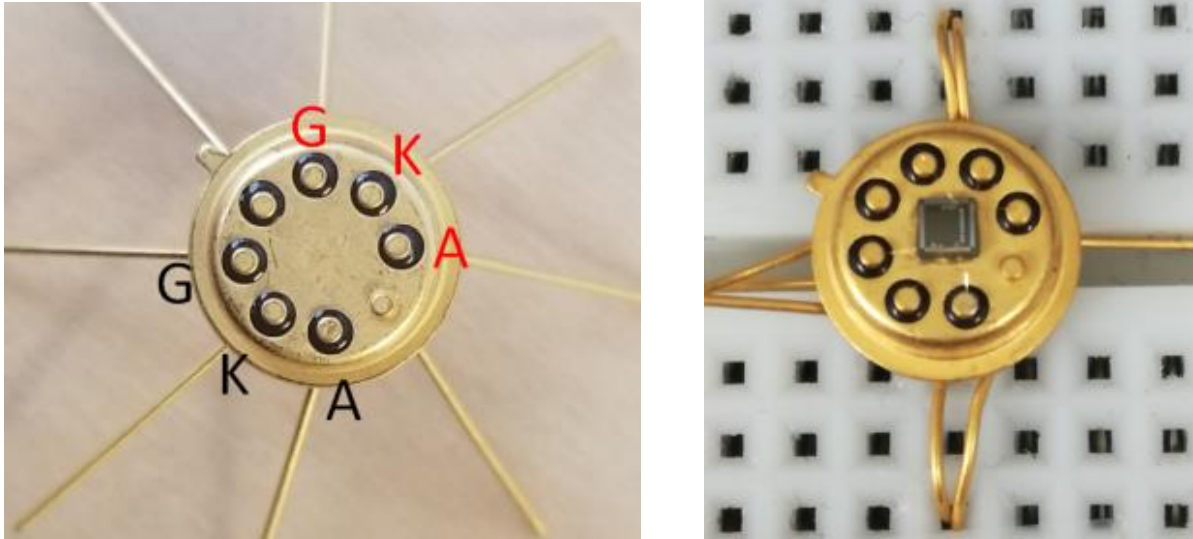
Figure 5.17 – TO-8 Package (left) and Wire Bonded Chip 1 in TO-8 Package (right)

Table 5.4 below shows the bond plan table (TO-8 package pins) for Chip 1.

Chip Pin #	Pin Description	APD	Bond Plan #
34	Anode (A)		
33	Cathode (K)	Min-P	1
42	Guard Ring (G)		
36	A		
35	K	Min-F	2
43	G		
38	A		
37	K	5μ-P	3
44	G		
40	A		
39	K	5μ-F	3
46	G		
2	A		
3	K	24μ-P	2
49	G		
4	A		
5	K	24μ-F	1
50	G		
47	A		
48	K	SiPM Pixel	4
46	G		
22	A		
21	K	SiPM Array	4
19	G		

Table 5.4 – TO-8 Package Bond Plans 1, 2, 3, and 4 for Chip 1

5.3 Chip 2

Chip 2, shown in Figure 5.18 below, contains 24 APD test structures and 66 pads.
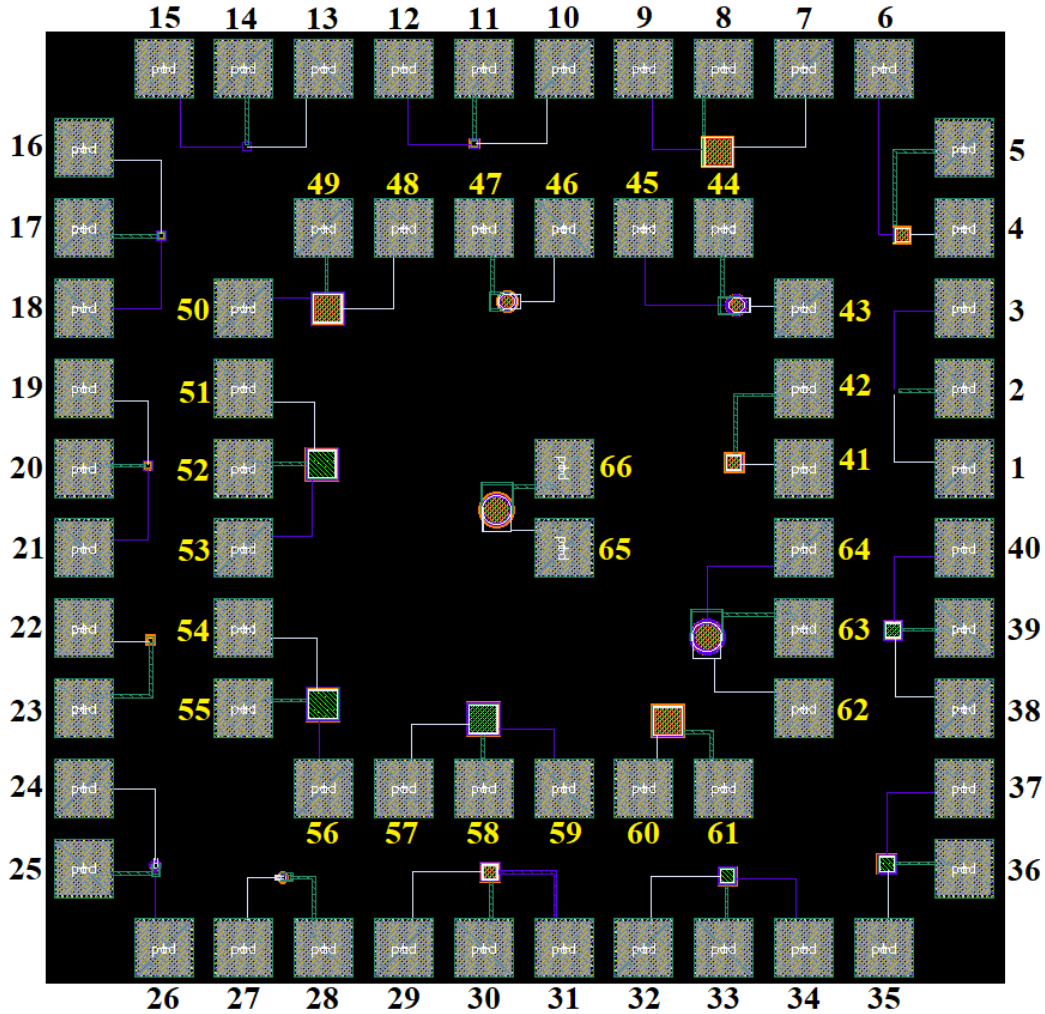
Figure 5.18 – Cadence Layout of Chip 2

The APD's on Chip 2 are classified into three sizes with EMITT layer dimensions of 5μm x 5μm, 24μm x 24μm, and 50μm x 50μm, and all have full guard rings unless specifically mentioned. For each size (5μ, 24μ, and 50μ), the APD variants are documented below, and their corresponding layouts are presented in Appendix 5b.

Elementary – These structures are the APD design in Figure 4.3 (right) from Chapter 4, pg. 24, with no rings around the active area but additional contacts to ensure proper connection.

Standard – These structures are full guard ring structures, the basis for the following test structures. 5μ and 24μ are equivalent to 5μ-F and 24μ-F on Chip 1.

No EMITT - These structures are simply the **Standard** structures with the EMITT layer removed in order to determine if the SiGe contribution is due solely to EMITT. Figure 5.19 below shows the layout and corresponding cross-sectional view of the 5μ No EMITT APD.
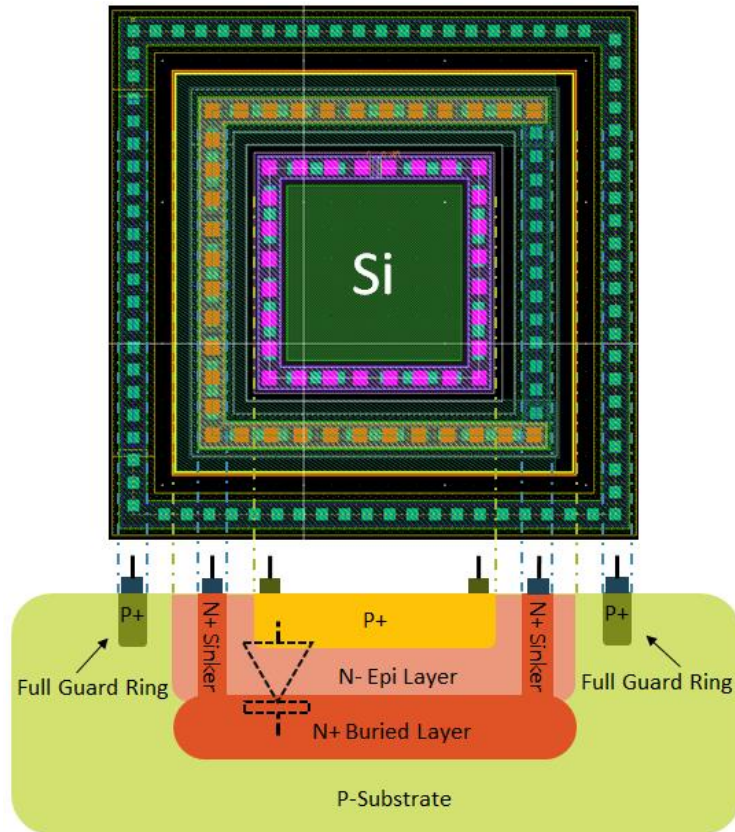
Figure 5.19 – Cadence Layout and Cross Section of No EMITT

BPOLY/PPLUS – These structures are the **No EMITT** structures but with the BPOLY layer replaced with PPLUS in order to determine if the SiGe contribution is, in fact, NOT due solely to EMITT but rather from the BPOLY layer. PPLUS maintains the same dimensions as the BPOLY layer it replaces, but this requires the dimensions of the active area DIFF layer to increase in order to satisfy design rules. Figure 5.20 below shows the layout and corresponding cross-sectional view of the 5μ BPOLY/PPLUS APD.

38
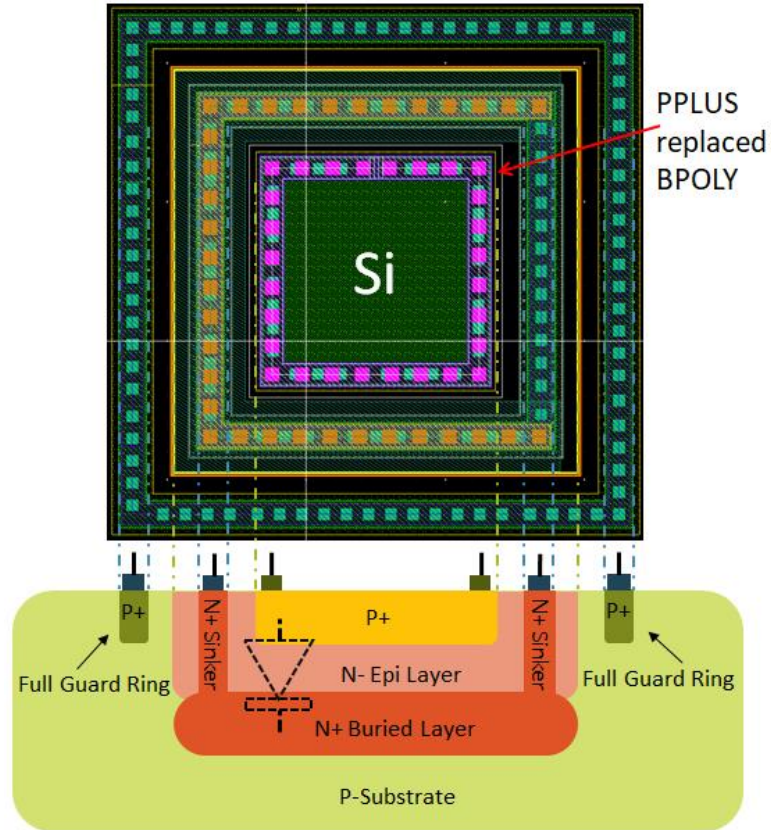
Figure 5.20 – Cadence Layout and Cross Section of BPOLY/PPLUS

BPOLY/PPLUS Smaller – These structures are the **BPOLY/PPLUS** structures, but the active area DIFF layer maintains the same dimensions as in the **No EMITT** and **Standard** structures to maintain consistent active area. As a result, however, PPLUS is required to have smaller dimensions than the BPOLY layer it replaces in order to satisfy design rules.

No Sub - These structures are simply the **Standard** structures with the substrate guard ring removed in order to investigate its effect on the APDs performance.

Circle – These structures are simply the circular versions of the **Standard** structures with their sizes characterized by the diameter of the EMITT layer circle. This was done to eliminate high electric field at sharp corners of the APD which lead to a high DCR [32].

Circle No Sub - These structures are simply the **Circle** structures with the substrate guard ring removed in order to investigate its effect on the APDs performance.

The fabricated chip die will be wire bonded to TO-8 packages according to the bond plan and pin table for Chip 2 shown in Appendix 5c. The nine bonding diagrams for Chip 2 are shown in Appendix 5d. Note each TO-8 is bonded in the same manner.

5.4 Chip 3

Chip 3, shown in Figure 5.21 below, contains 67 pads and 22 APD test structures.
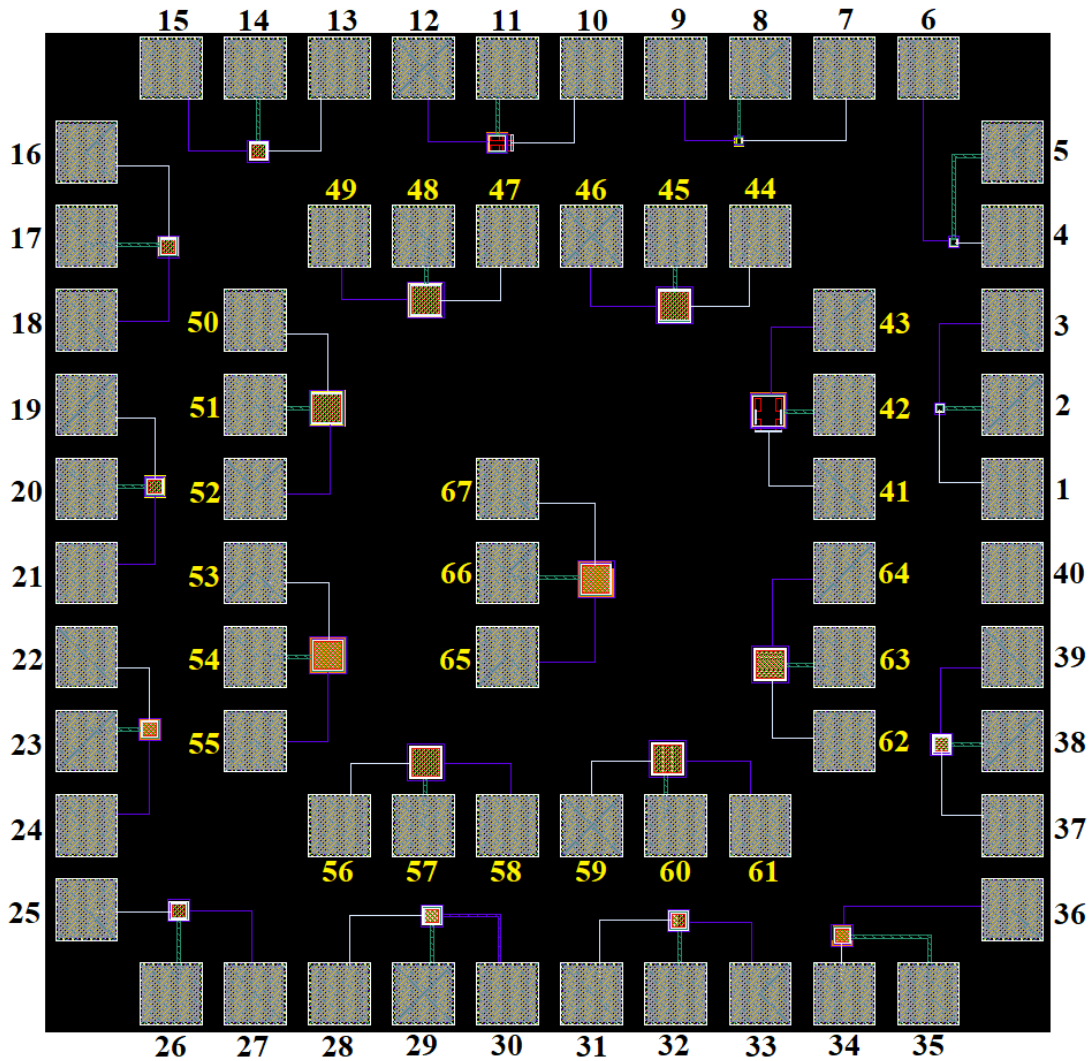
Figure 5.21 – Cadence Layout of Chip 3

The APD's on Chip 3 are classified into three sizes with EMITT layer dimensions of 5μm x 5μm, 24μm x 24μm, and 50μm x 50μm, and all have full guard rings unless specifically

mentioned. For each size (5μ, 24μ, and 50μ), the APD variants are documented below, and their corresponding layouts are presented in Appendix 5e.

noBNTUB2 – These structures are the **Standard** structures but with BNTUB2 deleted in order to investigate the impact of BNTUB2, which is used for high voltage (5V) HBTs, compared to only BNTUB, used for low voltage (3.3V) high speed HBT's. The researchers are interested to see if BNTUB2 is a buried "deep" N-well or if it is simply used for BJTs rather than MOSFETs which are suspected to utilize NTUB and NBUR. Figure 5.22 below shows the cross-sectional view of a SiGe NPN low voltage (3.3V) high speed HBT, which does not contain BNTUB2, in the S35 process to be compared to Figure 4.3 (left) in Chapter 4, pg. 24. As both cross sections in Figures 4.3 (left) and 5.22 contain a N+ buried layer, it is suspected that both BNTUB and BNTUB2 yield a N+ buried layer despite the absence of the NBUR layer.

Figure 5.22 – Cross Section for SiGe NPN Low Voltage (3.3V) High Speed HBT [33]

TUBBUR – These structures have BNTUB and BNTUB2 replaced by NTUB and NBUR and are to be compared to **Standard** and **noBNTUB2** in order to determine the effect of BNTUB, BNTUB2, NTUB, and NBUR as explained in the description of **noBNTUB2** above.
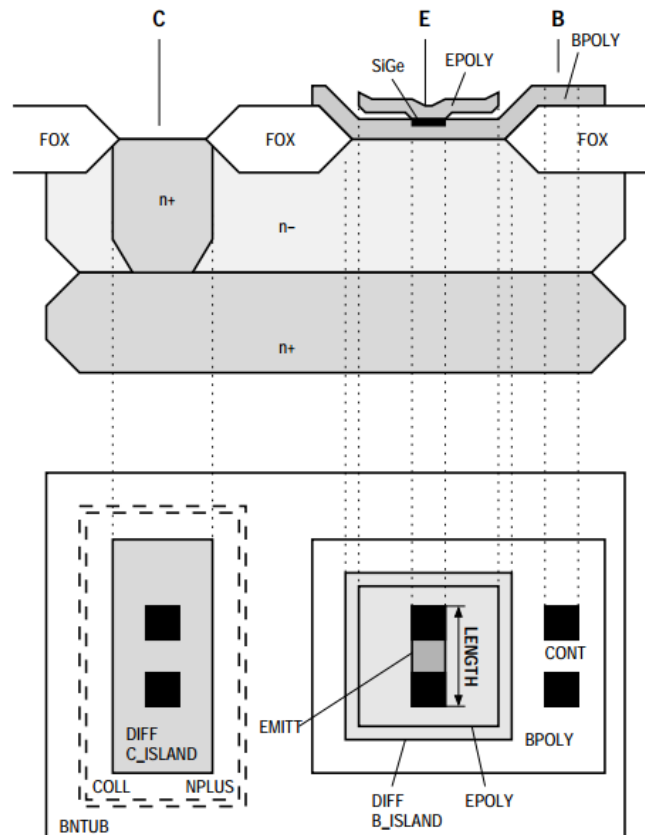
TUB – These structures have BNTUB and BNTUB2 replaced by only NTUB and are to be compared to **Standard** and **noBNTUB2** in order to determine the effect of BNTUB, BNTUB2, NTUB, and NBUR as explained in the description of **noBNTUB2** above.

The following APD variants were laid out for sizes of 24μ and 50μ.

Cyl – These structures contain four cylindrical photodiodes connected in parallel similar to Figure 5.23 shown below.
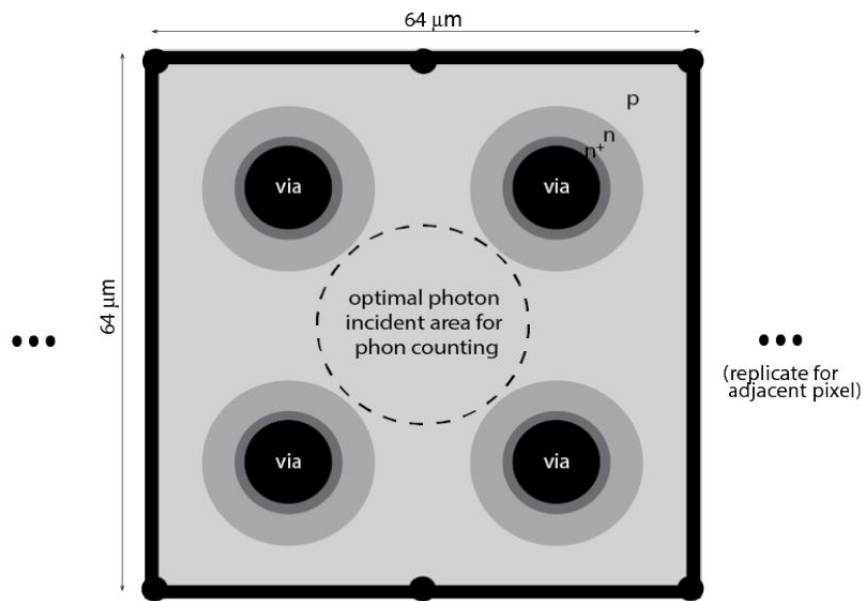
Figure 5.23 – Four Cylindrical Photodiodes Connected in Parallel [34]

Striped BNTUB2 – These structures are comparable to **Standard** but with BNTUB2 laid out in strips in order to create an APD with striped n-wells.

Striped Half BNTUB2 – These structures are the same as **Striped BNTUB2** but with the BNTUB2 strips laid out with a 50% concentration such that the strips of BNTUB2 are half the total area of the homogeneous BNTUB2 in the **Standard** structures.

Striped TUBBUR – These structures are comparable to **TUBBUR** but with TUB & BUR both laid out in strips as shown in Figure 5.24 below in order to create an APD with striped n-wells to be compared to **Striped BNTUB2**. The following structures are simply variations of these structures, or can be thought of as variations of the **TUBBUR** structures with TUB and BUR independently laid out in strips.
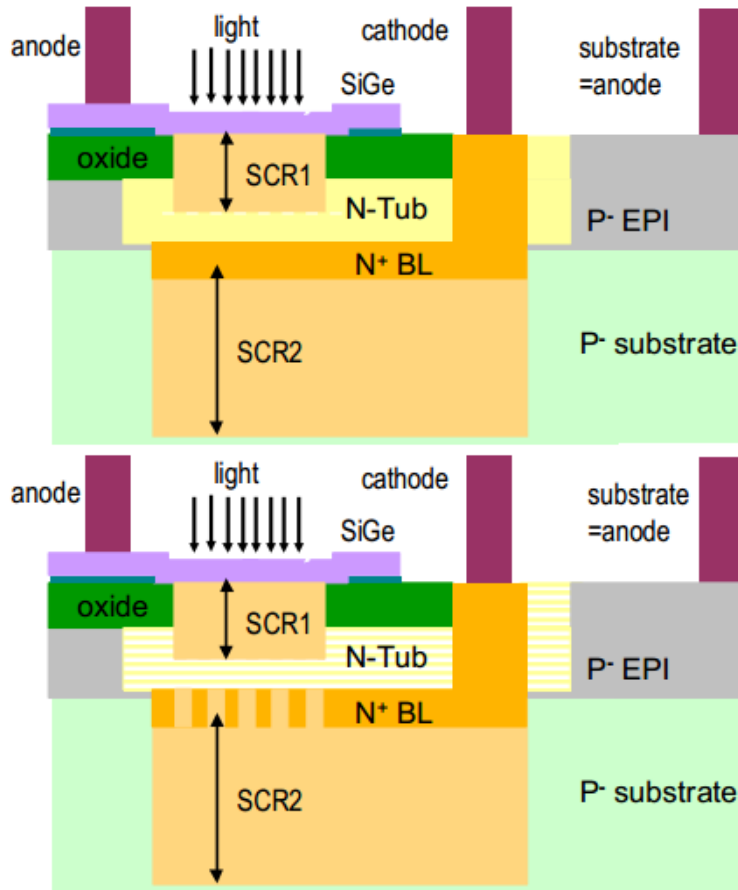
Figure 5.24 – APD Layout with Striped N-Wells [35]

Striped BUR hTUB – These structures are the same as **Striped TUBBUR** but with only BUR striped and TUB left homogenous as in **TUBBUR**.

Striped BUR Half TUB – These structures are the same as **Striped BUR hTUB** but with TUB strips laid out with a 50% concentration such that the strips of TUB are half the total area of the homogeneous TUB in the **Striped BUR hTUB** structures.

The following APD variant was laid out only for a size of 24μ.

24μ Striped Half TUB hBUR – These structures are the same as **Striped BUR Half TUB** but with BUR homogeneous, so the only difference between these structures and the **TUBBUR** structures is that TUB strips are laid out with a 50% concentration such that the strips of TUB are half the total area of the homogeneous TUB in the **TUBBUR** structures.

The fabricated chip die will be wire bonded to TO-8 packages according to the bond plan and pin table for Chip 3 shown in Appendix 5f. The eleven bonding diagrams for Chip 3 are shown in Appendix 5g. Note each TO-8 is bonded in the same manner, just as in Chip 2.

Chapter 6: Chip Testing Explanation and Procedure

6.1 Testing Explanation

Chip 1 is the only chip that has been tested as Chip 2 and Chip 3 have yet to be received from MOSIS. I-V characteristic curves, responsivity, and QE for the APDs on Chip 1 were tested at Freedom Photonics using SOIC-28 packages. I-V curves for the APDs on Chip 1 were also tested by the researchers at UNLV in order to compare results to those obtained at Freedom Photonics and determine the reliability of the testing equipment and procedure set up by the researchers at UNLV. In addition, at the request of Freedom Photonics, DCR and light count rate (LCR) tests were performed by the researchers at UNLV. Though Chip 1 was tested at UNLV in both SOIC-28 and TO-8 packages, only TO-8 package testing results for Chip 1 in TO-8 packages are presented as the testing results for Chip 1 in SOIC-28 packages are similar yet less consistent compared to those of the TO-8 packages.

6.2 Description of Testing Equipment

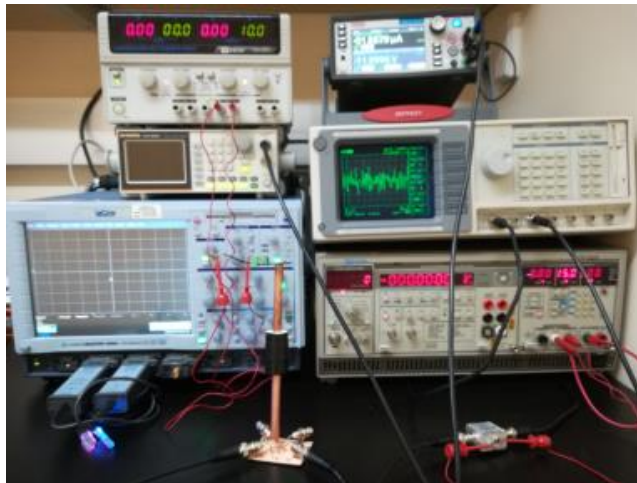The testing equipment utilized is presented in Figures 6.1 through 6.12 below.

Figure 6.1 – Full Test Equipment Set Up
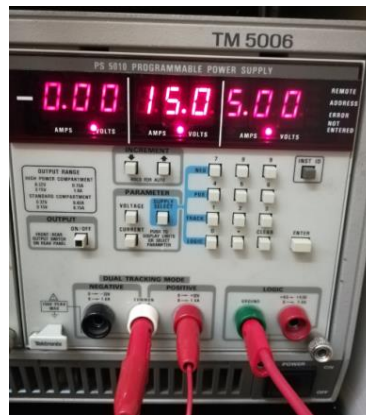
Figure 6.2 – Keithley 2450 SourceMeter

Figure 6.3 – GW Instek GPS-3303 Programmable Power Supply

Figure 6.4 – Tektronix PS 5010 Programmable Power Supply

Figure 6.5 – GW Instek AFG-2225 Arbitrary Function Generator

Figure 6.6 – Stanford Research Systems SR430 Multi-Channel Scaler

Figure 6.7 – Lecroy WaveMaster 8300A 3 GHz Oscilloscope

Figure 6.8 – Mini-Circuits ZFL-500LN-BNC+ Small Signal, Low Noise Amplifier (LNA)

with a gain of 24dB

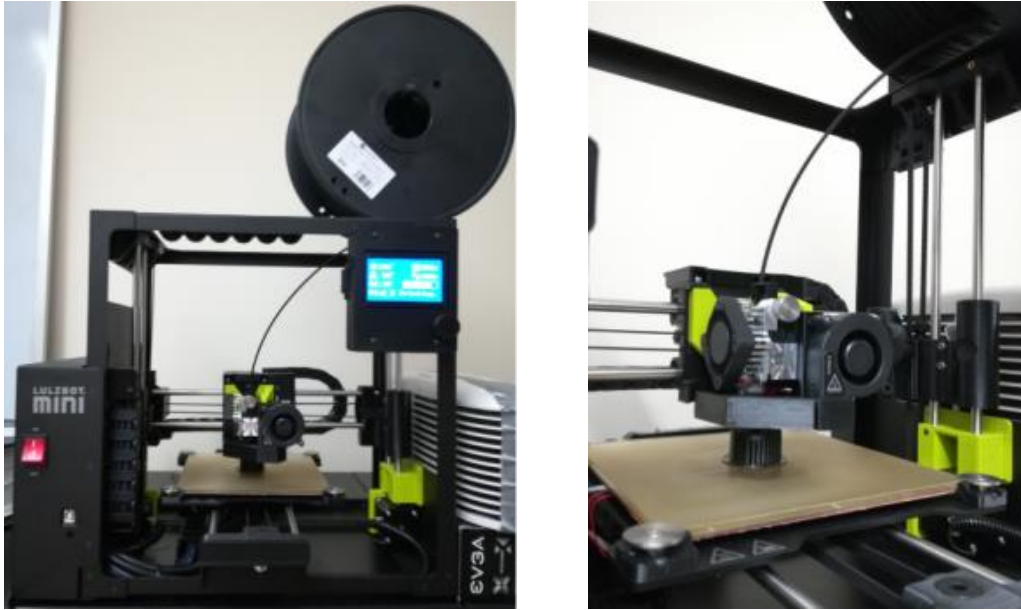**Figure 6.9 – Thorlabs PM100USB Power and Energy Meter Interface**

Figure 6.10 – LulzBot Mini 3D Printer (left) Zoomed in on Printed Component (right)
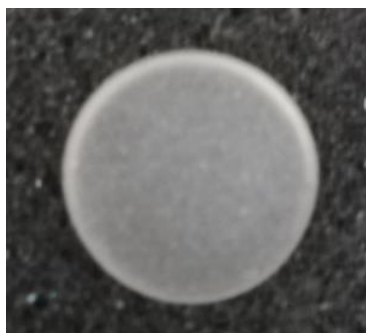

Figure 6.11 – Dark Box

Figure 6.12 – Thorlabs Ground Glass Diffuser, 12.7mm, 220 GRIT

An LED driver PCB was also designed using EAGLE in order to supply a fixed amount of current (determined by resistor values) to a diffused LED with a certain wavelength such that the APD's could be tested for fixed wavelengths and light intensities. The PCB schematic is

shown in Figure 6.13, the PCB design and fabricated PCB are shown in Figure 6.14, and the

populated PCB (containing a diffused LED, a 1N4148 diode, and a LM334 adjustable current
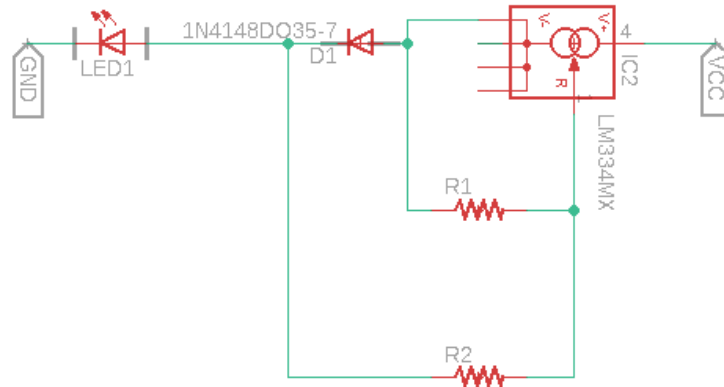
source) is shown in Figure 6.15, all below.

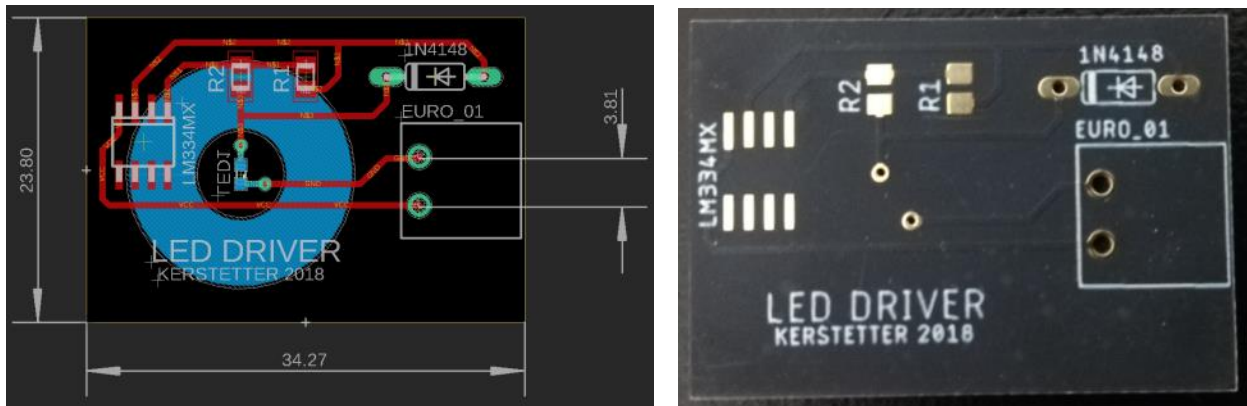**Figure 6.13 – PCB Schematic using EAGLE**

Figure 6.14 – LED Driver PCB Design using EAGLE (left) and Fabricated PCB (right)

Figure 6.15 – Populated LED Driver PCB

Copper tubes and 3D printed connector components were also utilized for reliable connection between the LED driver PCB and TO-8 package. The design of the 3D printed connector, component 1, and the fabricated component 1 are shown in Figures 6.16 and 6.17, respectively, below.
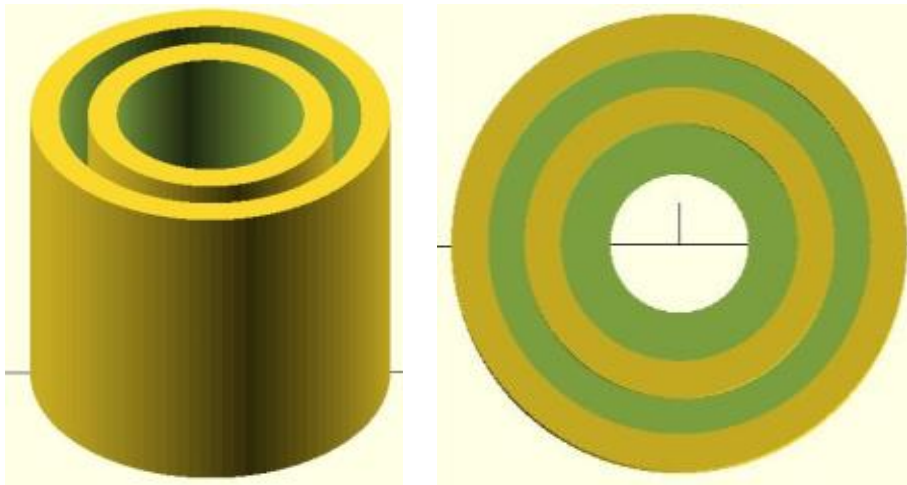

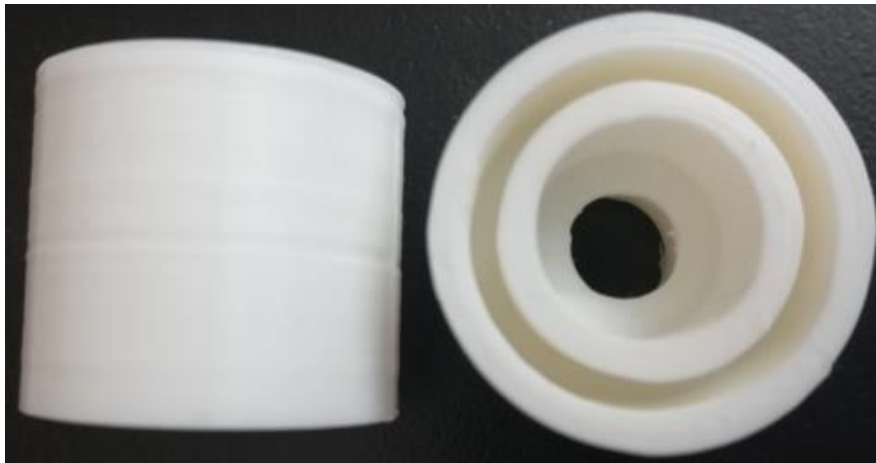**Figure 6.16 – Design of 3D Printed Connector, Component 1**

Figure 6.17 – Fabricated Component 1

The bottom opening of component 2a was modified to be a 1.5mm hole in component 2b which was modified to have the 1.5mm hole offset by 1mm in component 2c. The designs of the 3D printed connectors, component 2a, component 2b, and component 2c are shown in Figure 6.18 below, and the fabricated components are shown in Figure 6.19 below.
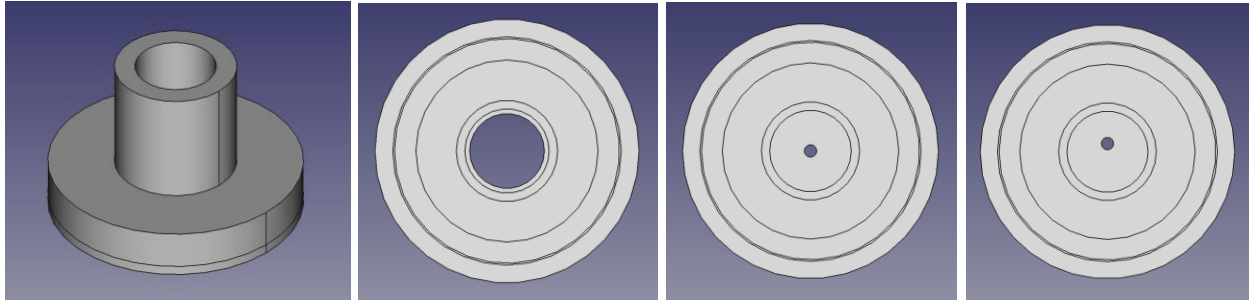
Figure 6.18 – Designs of 3D Printed Connectors (from left to right): Components 2a, 2b, and 2c (side view), Component 2a (bottom view), Component 2b (bottom view), and Component 2c (bottom view)
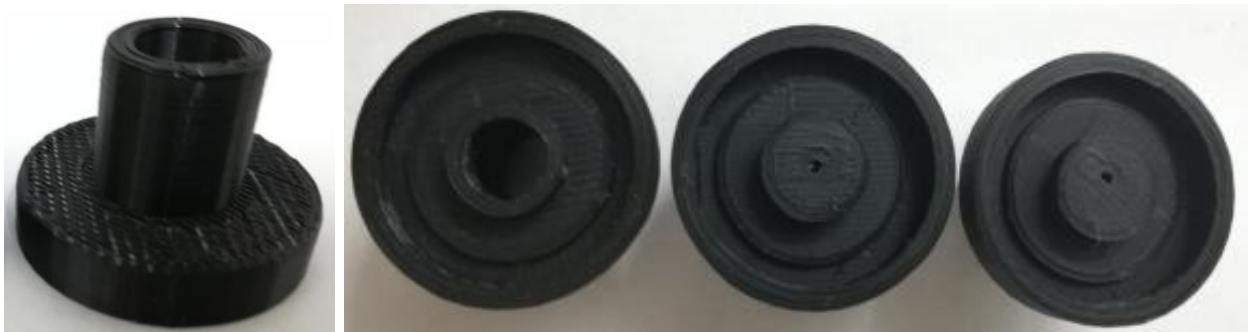

Figure 6.19 – Fabricated Components (from left to right): Components 2a, 2b, and 2c (side view), Component 2a (bottom view), Component 2b (bottom view), and Component 2c (bottom view)

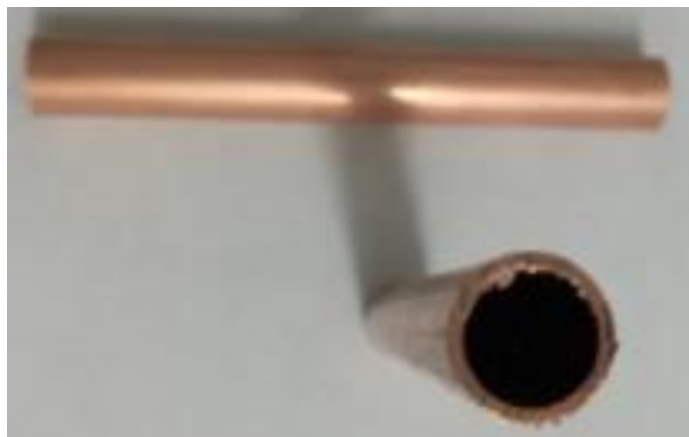The copper tubes utilized are shown in Figure 6.20 below.

Figure 6.20 – Copper Tubes: Side View (left) and Top View (right)

6.3 Description of Testing Procedure

6.3a I-V Curves

I-V curves were performed for the APDs using the Keithley 2450 SourceMeter in order to determine current magnitudes for a voltage sweep from 0V to 13V. As a current limit of 1mA (and later 200μA) was used to prevent damaging the APDs, some I-V curves do not reach the upper voltage limit of 13V. The 2450 SourceMeter was connected via BNC cable to the cathode of the APD while the anode and guard ring were grounded. I-V curves were performed for a dark state using the dark box as well as an arbitrary light condition using the ambient room light.

6.3b DCR

Tests of DCR were performed for voltages ranging from the breakdown voltage of the APD to 16V. In order to observe the amplitude of dark pulses, the output of the LNA was originally connected to the Lecroy 8300A Oscilloscope. As a result, it was determined to set the discriminator level on the SR430 to 200mV as shown in Figure 6.21 below. Also notice in Figure 6.21 below that the screen of the SR430 only displays from bin 64 at 10.24μs to bin 191 at 30.56μs and sums the "Total" counts over 10,000 records. The SR430 can only perform the math functions used to calculate the "Total" counts on the data displayed on the screen between bin 64 and bin 191. Thus, the assumption was made that the counts displayed on the screen of the SR430 in the 20.32μs from bin 64 to bin 191 accurately represents the count trend for 1 second.

Figure 6.21 – SR430 Screen Displaying 200mV Discriminator Level, Bin 64 at 10.24μs, and

Bin 191 at 30.56μs

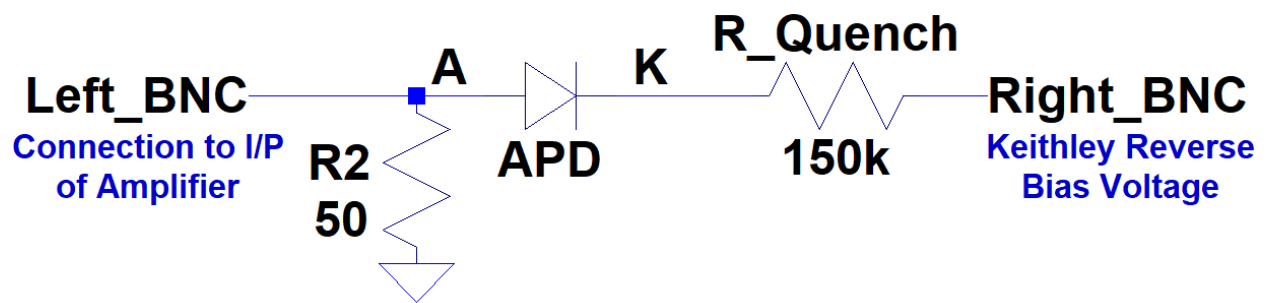The tested APD was then connected in the dark box as shown in Figures 6.22 and 6.23 below.

Figure 6.22 – LTSpice Schematic of APD Connection for DCR Tests

Figure 6.23 – Dark Box Connection of an APD in an SOIC-28 Package for DCR Tests

A BNC cable was connected from the 2450 SourceMeter to the cathode of the APD through a

150kΩ resistor. Another BNC cable was connected from the anode of the APD to the input of the

Mini-Circuits LNA. The LNA was powered with 15V from the 5010 Power Supply, and its

output was connected to the SR430 Signal In. A 50Ω resistor was also connected from the anode

of the APD to ground, and the guard ring was connected to ground. The 2225 function generator

was set to a 50% duty cycle square wave with a frequency of 1KHz, amplitude of 2.5Vpp, and

offset of 1.25VDC and was connected to the Trigger In of the SR430. The voltage of the 2450

SourceMeter was increased in varying increments up to 16V starting from the breakdown

voltage of the APD, where dark counts began to be present on the SR430. The "Total" counts

value on the SR430, shown in Figure 6.24 below, was recorded for each voltage step.
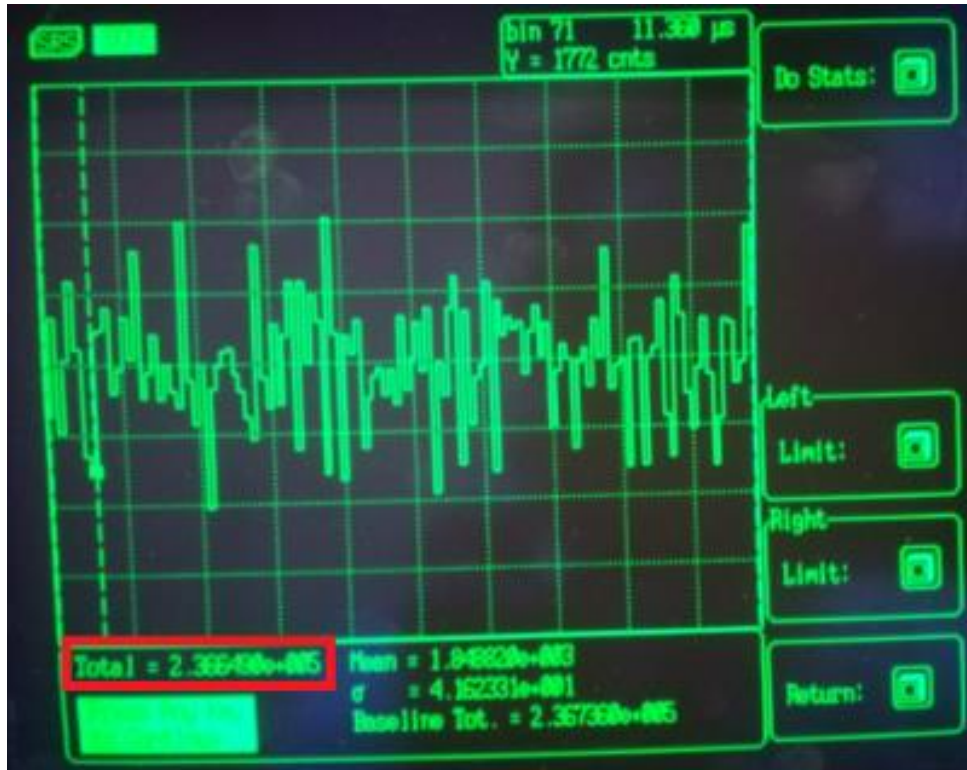
Figure 6.24 – SR430 Screen Displaying Total Counts

The "*Total*" counts value was then used to calculate *DCR* using Equation 11 below,

$$DCR = Total \times \frac{49,212.6}{10,000} = Total \times 4.92126 \qquad \text{Equation 11}$$

where *10,000* is the number of records in the scan over which "*Total*" is summed, and *49,212.6*

is the number of 20.32µs periods in a second, calculated using Equation 12 below, due to the

screen of the SR430 being set to display from *10.24µs* to *30.56µs*.

$$\frac{1\ second}{(30.56 - 10.24)\text{µs}} = 49,212.6 \qquad \text{Equation 12}$$

In order to confirm the accuracy of this method, a similar calculation was done using the bin

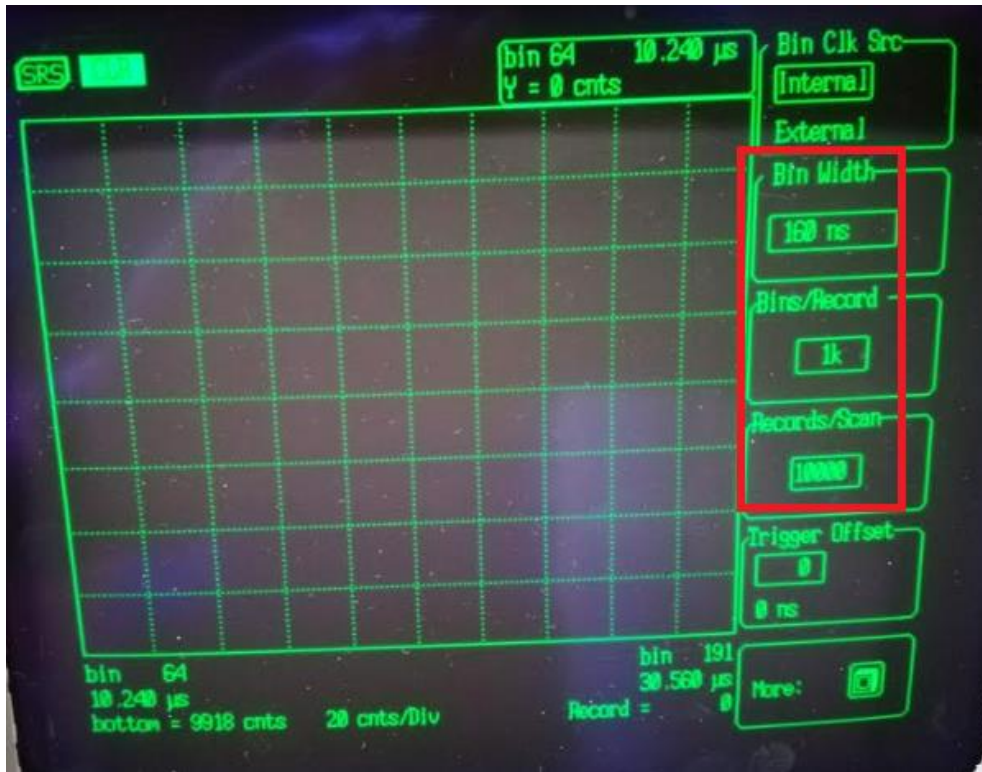width, bins per record, and records per scan as shown in Figure 6.25 below.

Figure 6.25 – SR430 Screen Displaying Bin Width, Bits per Record, and Records per Scan

6.3c LCR

For the TO-8 packages, LCR tests were also performed using various diffused LEDs of different wavelengths and powered by the LED driver PCB connected to the TO-8 package through two copper tubes. The copper tubes were connected by two component 1 connectors in Figure 6.17, pg. 50, with the Thorlabs Diffuser in Figure 6.12, pg. 48, between them (to evenly distribute the LED light for better uniformity) as shown in Figure 6.26 below.
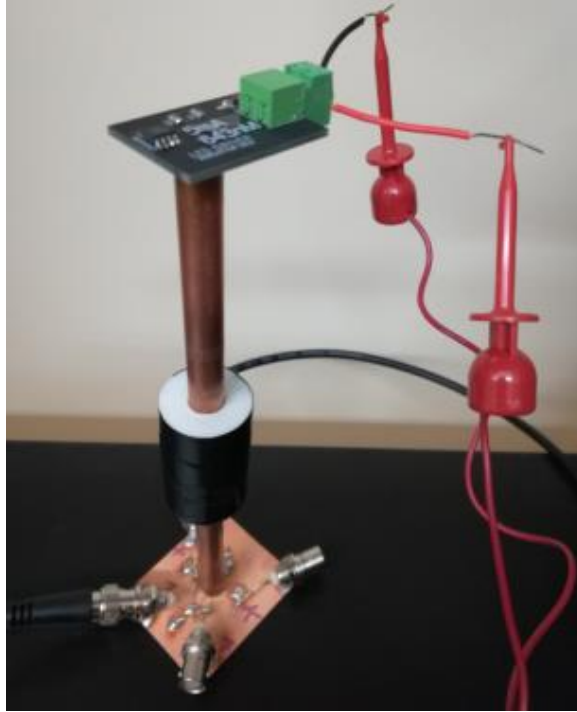
Figure 6.26 – Connection of LED Driver to TO-8 Package through Two Copper Tubes,

Two Component 1 Connectors, and a Diffuser for LCR Tests

The TO-8 package was connected as shown in Figure 6.27 below with dead bug techniques using a copper clad board. The TO-8 package was connected exactly the same as it was in the dark box according to Figure 6.22, pg. 53.
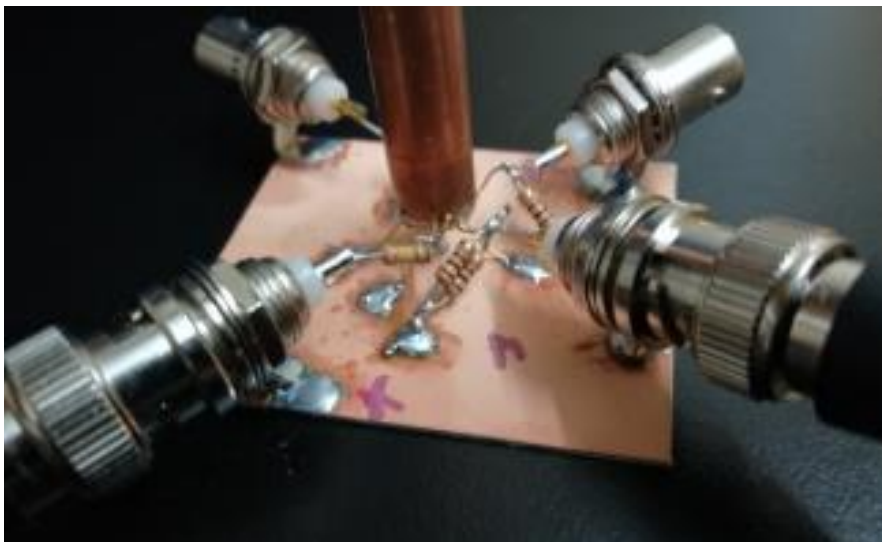

Figure 6.27 – Dead Bugged TO-8 Package

The LED driver PCB was connected to 10V from the 3303 Power Supply, and the resistor values on the LED driver PCB were calculated using Equation 13 and Equation 14 below from the LM334 datasheet such that R_1 and R_2 were set to 27Ω and 267Ω, respectively, in order to supply the LED with a current of 5mA [36].

$$I_{SET} \approx \frac{0.134\ V}{R_1}$$
Equation 13

$$R_2 = 10 \times R_1$$
Equation 14

An LTSpice schematic shown in Figure 6.28 below was also drafted and simulated to ensure the accuracy of the resistor calculations for a current of 5mA.
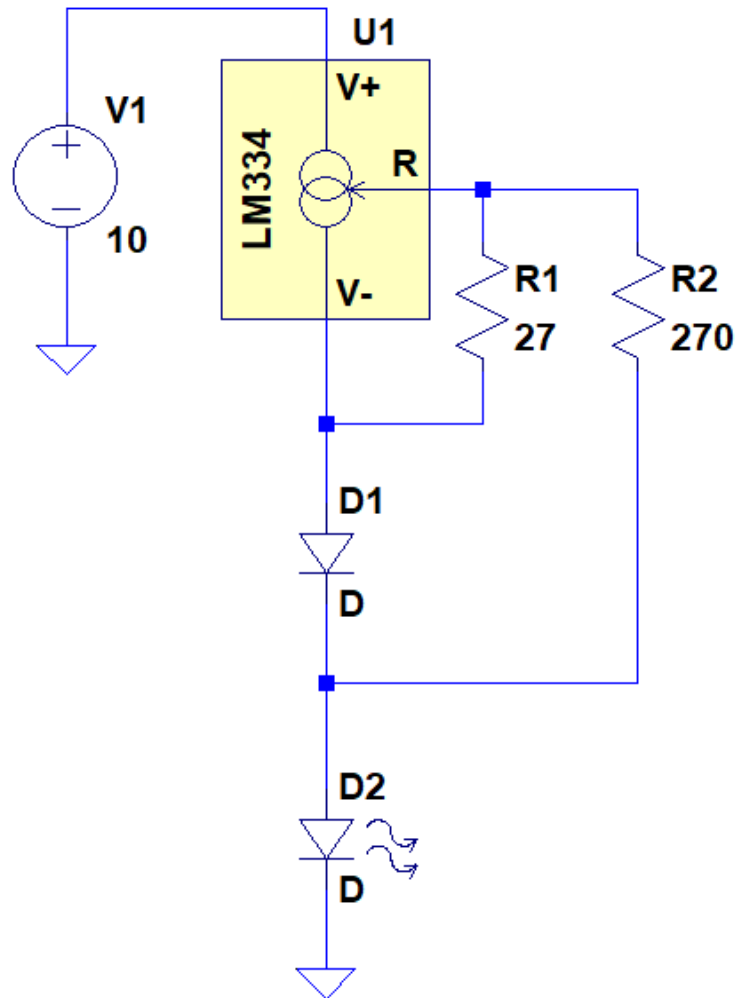
Figure 6.28 – LTSpice Schematic of LED Driver PCB

Note the intensity of the incident light due to the LED can be increased by supplying the LED with more current. The LCR tests were then performed exactly like the DCR tests described previously.

6.3d Power Uniformity

In order to test responsivity and QE of an APD, the power resulting from light incident on the tested APD must be known. Thus, the researchers first needed to determine the uniformity of the power supplied by a LED used as the source of incident light such that the power of the incident light striking a single APD on the chip could be accurately determined. For uniform power supplied by the LED, the power of the incident light striking a single APD on the chip could be accurately determined by multiplying the total power measured in the area of the entire chip by the ratio of the area of the tested APD to the area of the entire chip. Thus, the LED driver PCB was connected as it was for the light count tests. However, instead of the lower copper tube connected to a TO-8 package, it was connected to the Thorlabs Power Meter. This was done using the 3D printed connector components 2a, 2b, and 2c shown in Figure 6.19, pg. 51, as shown in Figure 6.29 below. The three different 3D printed connector component variations were used in order to measure the power at various areas and determine the uniformity of the power due to the LED.

Figure 6.29 – Copper Tube Connected to Power Meter using Component 2a (shown), 2b,

and 2c

The power measured at various areas was consistent, suggesting uniformity of the power

supplied by the LED. By looking at the beam produced by the LED, however, it was evident that

the light was clearly not uniform. Furthermore, multiple issues and concerns arose surrounding

the comparison of the power measured in the area of the sensor in the Power Meter to the power

of the light incident on the chip in a TO-8 package. As a result, it was apparent that further

calibration and power uniformity tests using more reliable testing equipment is required in order

to accurately measure responsivity and QE of an APD.

7.1 I-V Curve Test Results

The I-V curve for the SiPM pixel in an arbitrary light state using the ambient room light is shown in Figure 7.1 below.
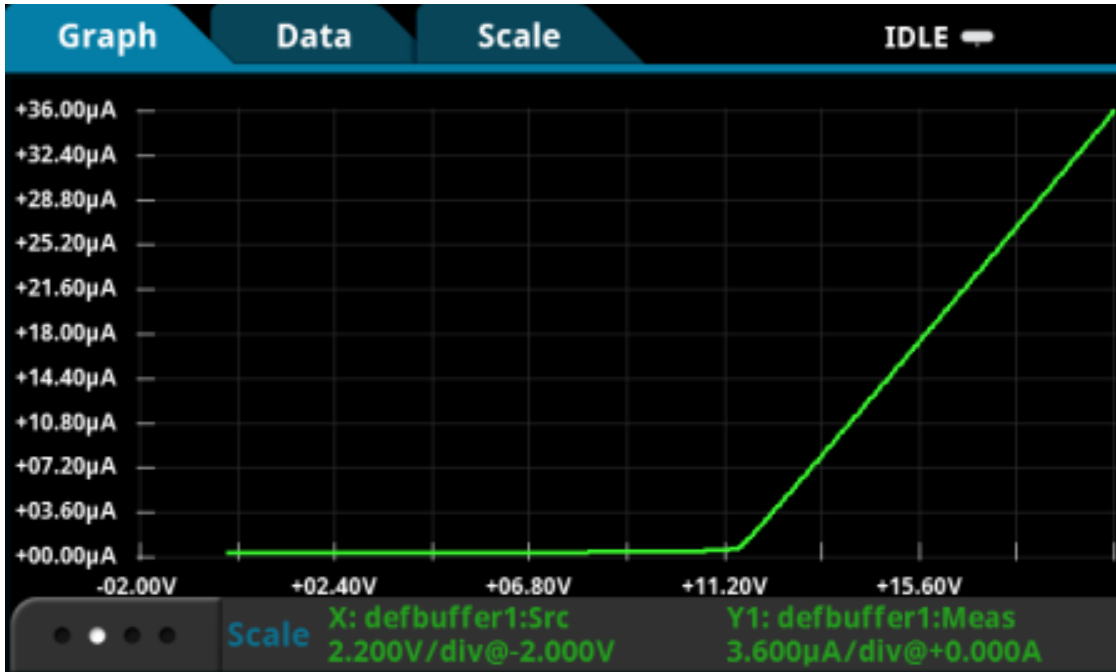
Figure 7.1 – I-V Curve of SiPM Pixel

The I-V curve data on the Keithley 2450 SourceMeter was exported to Microsoft Excel in order to examine the data and generate customized graphs with both dark and light states on the same plot. The raw data is available upon request. The SiPM pixel has lower current than the other APDs due to the 350kΩ resistor in series with its anode, allowing to clearly see the increase in current amplitude from dark to light state on the same plot. Thus, the I-V curve of the SiPM Pixel in a dark state as well as an arbitrary light sate, labeled Total Current, using the ambient room light is shown in Figure 7.2 below for comparison to Figure 3.3 in Chapter 3, pg. 12.
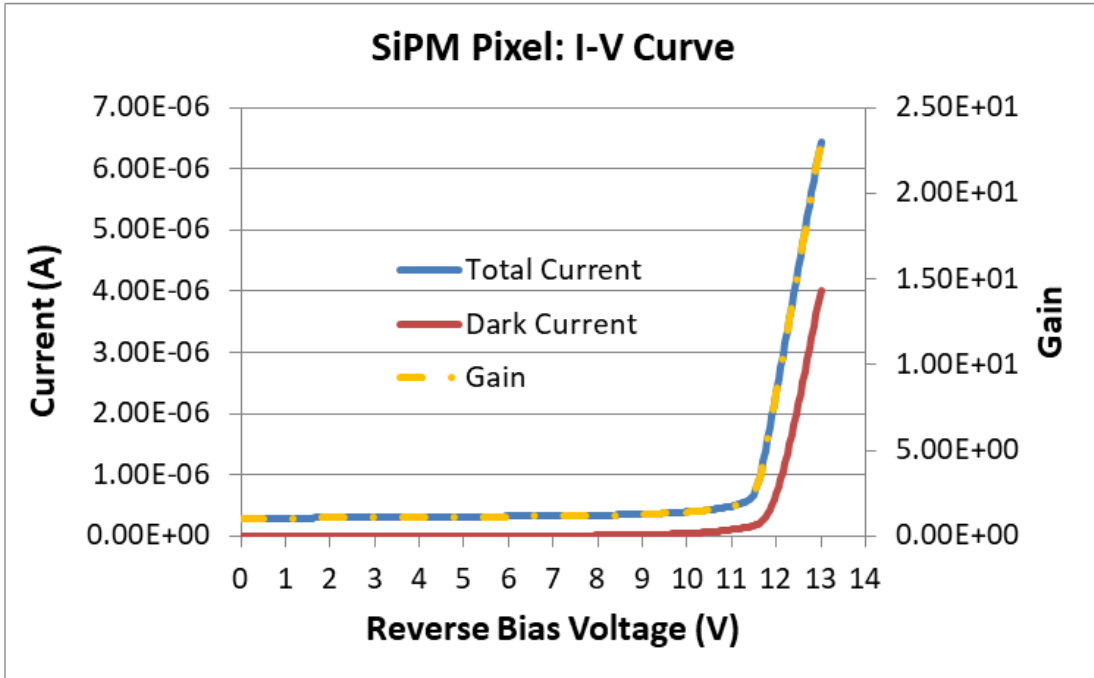
Figure 7.2 – I-V Curve of SiPM Pixel Plotted in Microsoft Excel

The same plot with current and gain on the y-axes expressed in logarithmic form for better

distinction between Dark and Total Current is shown in Figure 7.3 below.
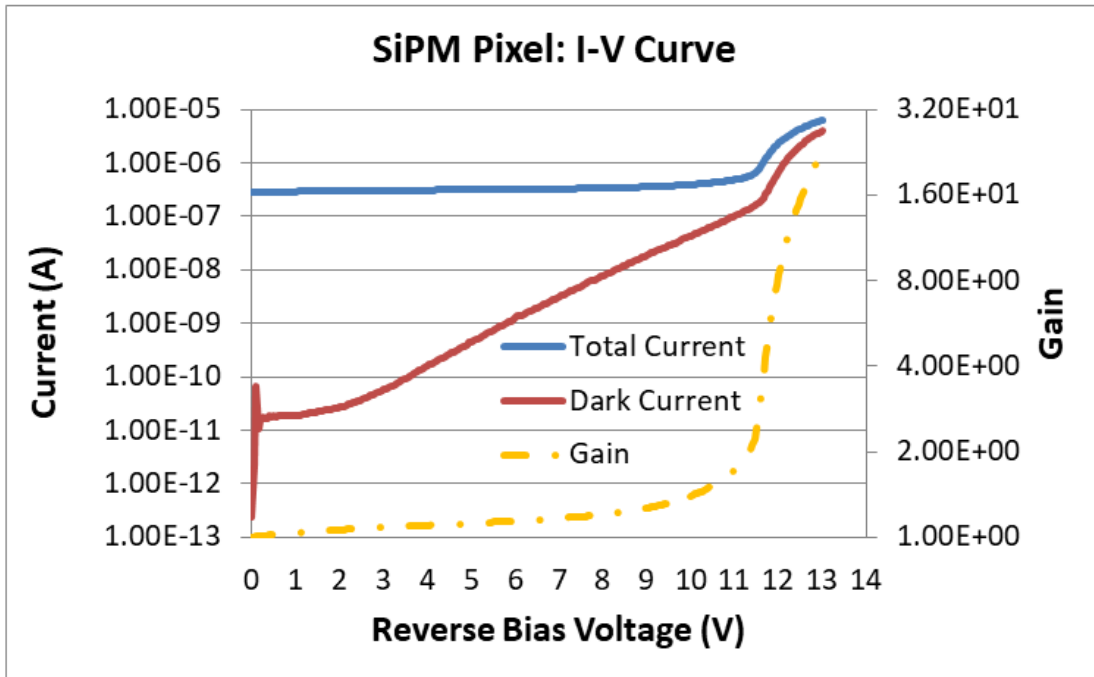
Figure 7.3 – I-V Curve of SiPM Pixel with Y-axes in Logarithmic Form

Note the Photo Current is equal to the Dark Current subtracted from the Total Current, and the Gain is plotted by dividing the Total Current at each voltage increment by the Total Current at 0V such that there is a gain of 1 at 0V. Figure 7.4 below shows the I-V curve zoomed in around the tested APDs breakdown voltage.
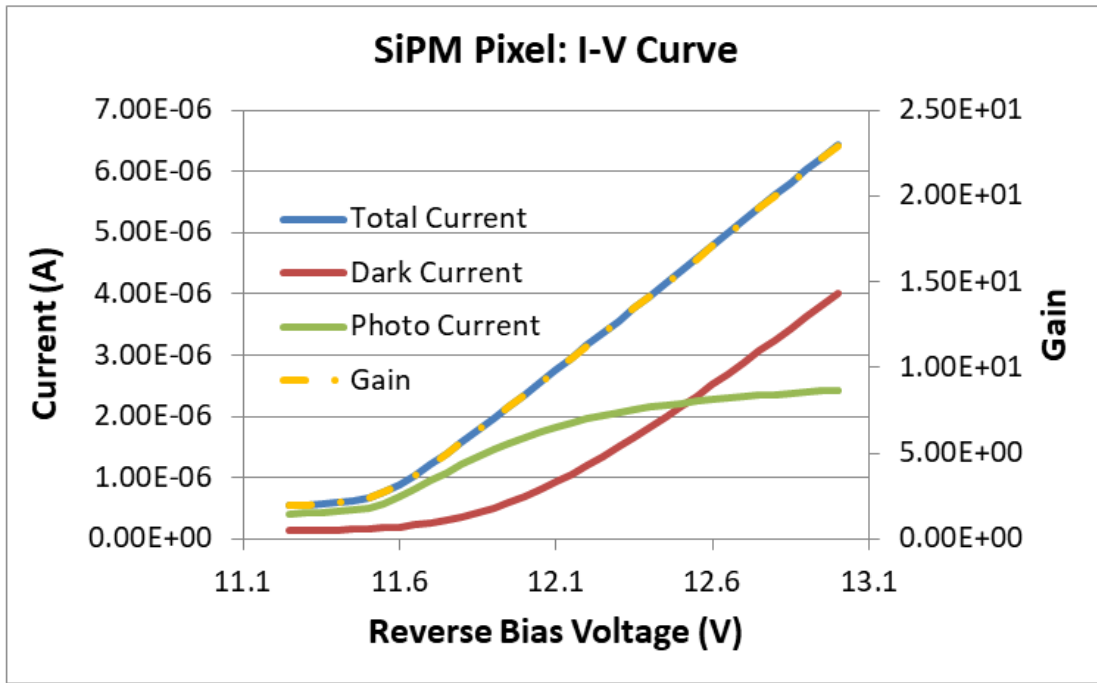
Figure 7.4 – I-V Curve of SiPM Pixel Zoomed in around Breakdown Voltage

These three I-V curves for the remaining structures on Chip 1 (Min-P, Min-F, 5μ-P, 5μ-F, 24μ-P, and 24μ-F) are shown in Appendix 7a. Note in the zoomed in plots that the Dark Current may overtake the Total Current, resulting in the Photo Current peaking then decreasing and even going slightly negative in some cases. This point should be noted as the breakdown voltage where the Total Current begins to abruptly increase, signifying the APD entering Geiger mode. I-V curve measurements were repeated multiple times with both TO-8 and SOIC-28 packages, yielding consistent results. In Geiger mode, gain is arbitrary as the Total Current begins to tend to infinity. Note that if the gain was determined using the Photo Current, as is commonly done, the gain would drop off as the APD enters Geiger mode. Thus, to accommodate both methods,

Table 7.1 below shows the maximum linear gain for each APD at the breakdown voltage where

the Photo Current reaches its peak.

APD	Breakdown Voltage (V)	Peak Photo Current (µA)	Maximum Linear Gain
Min-P	11	149	271
Min-F	10.9	129	2,110
5µ-P	11.45	725	22,900
5µ-F	11.45	715	23,400
24µ-P	11.4	516	7,190
24µ-F	11.525	641	4,570
SiPM Pixel	13	2.43	22.9

Table 7.1 – Breakdown Voltage, Peak Photo Current, and Maximum Linear Gain of Chip

1 APDs

Note that the 350kΩ resistor associated with the SiPM pixel limits its Photo Current resulting in

a significantly lower gain than the 24µ-F APD.

7.1a Freedom Photonics I-V Curve Test Results

The I-V curves for the 5µ-F and 24µ-F APDs were tested at Freedom Photonics for a

dark state as well as response to 560nm light from zero bias (0V) to 11V and are shown in
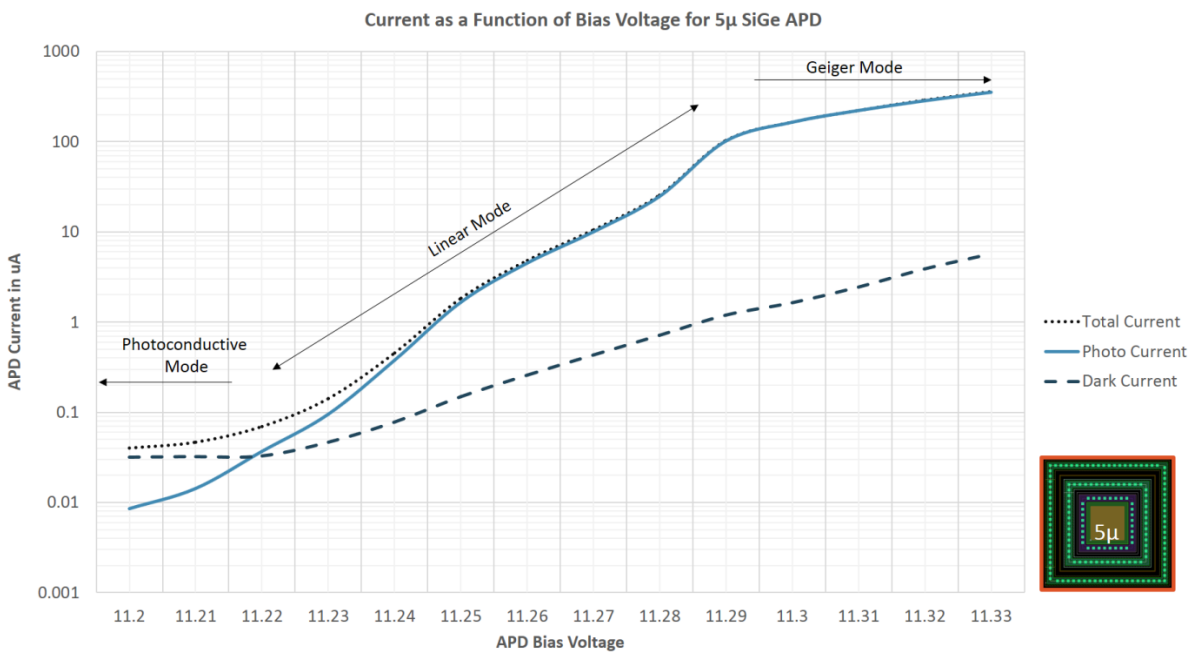
Figures 7.5 and 7.6, respectively, below.
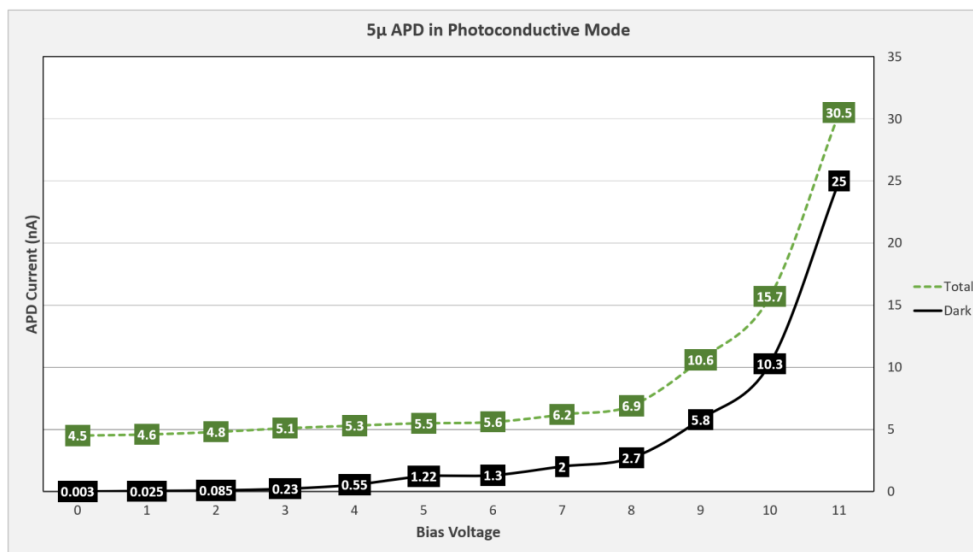
Figure 7.5 – I-V Curve of 5µ-F APD Tested at Freedom Photonics
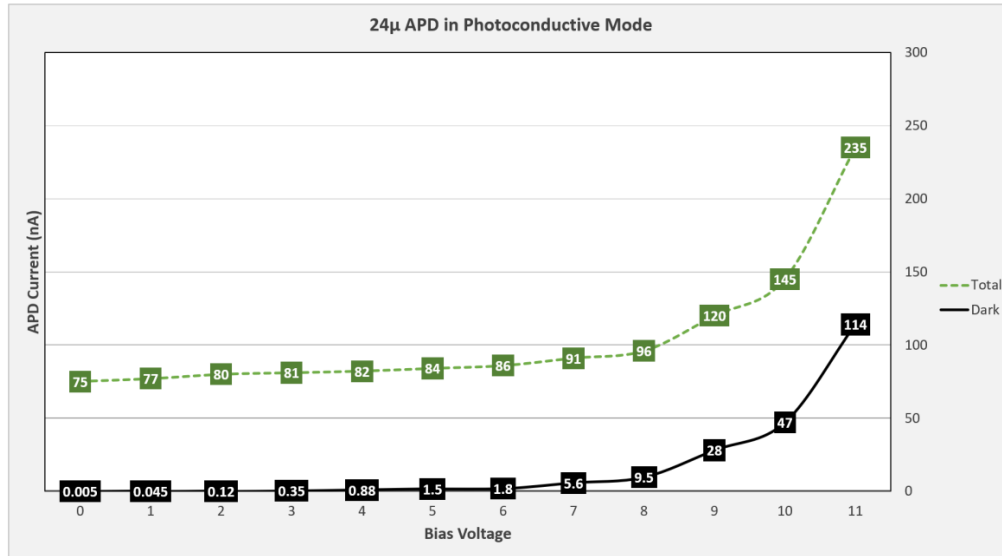
Figure 7.6 – I-V Curve of 24µ-F APD Tested at Freedom Photonics

The dark current results are fairly higher than those measured at UNLV as shown in Table 7.2

below.

Voltage (V)	UNLV 5µ-F Dark Current (nA)	Freedom Photonics 5µ-F Dark Current (nA)	UNLV 24µ-F Dark Current (nA)	Freedom Photonics 24µ-F Dark Current (nA)
0	0.0049	0.003	0.0127	0.005
1	0.0076	0.025	0.0309	0.045
2	0.0065	0.085	0.02041	0.12
3	0.0074	0.23	0.02096	0.35
4	0.0083	0.55	0.02527	0.88
5	0.0149	1.22	0.04879	1.5
6	0.0428	1.3	0.07505	1.8
7	0.1337	2	0.2697	5.6
8	0.4049	2.7	0.6934	9.5
9	1.15	5.8	2.01	28
10	3.14	10.3	5.6	47
11	9.07	25	16.3	114

Table 7.2 – Dark Current as a Function of Bias Voltage for 5µ-F and 24µ-F APDs Tested at

UNLV and Freedom Photonics

Figure 7.7 below shows the difference in photocurrents for the 5µ-F and 24µ-F APDs is roughly

proportional to the area, which is 23.04 times larger for the 24µ-F APD.
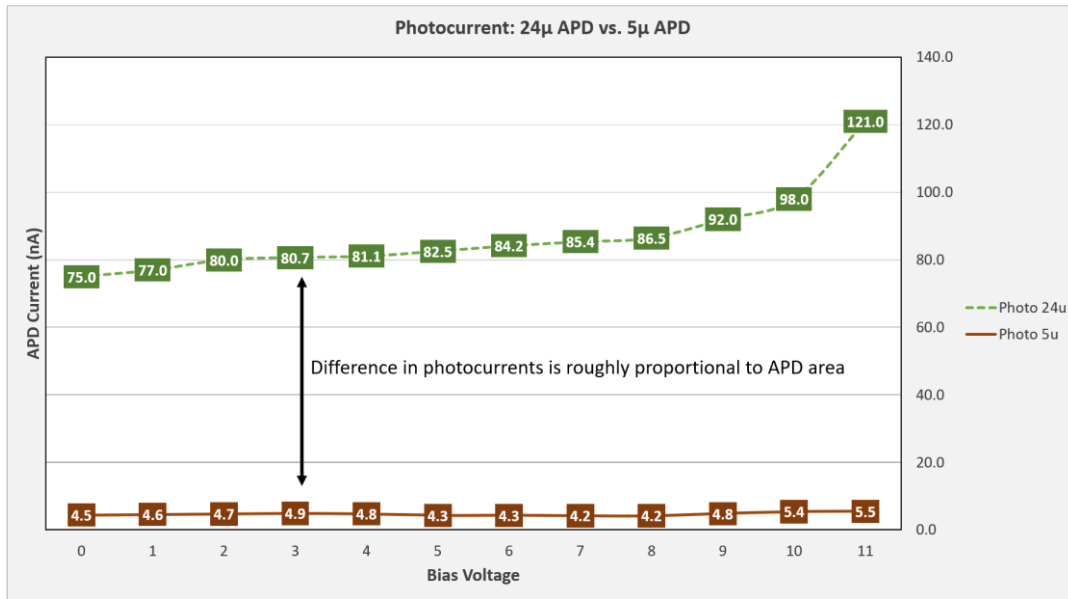
Figure 7.7 – Difference in Photocurrents for 5μ-F and 24μ-F APDs

The I-V curves of the 5μ-F and 24μ-F APDs from 11.2V to 11.33V are shown in Figures 7.8 and 7.9, respectively, below, displaying the Dark Current, Total Current, and Photo Current using 560nm light as well as the different regions of operation including photoconductive, linear, and Geiger mode.

Figure 7.8 – I-V Curve of 5μ-F APD Tested at Freedom Photonics

66
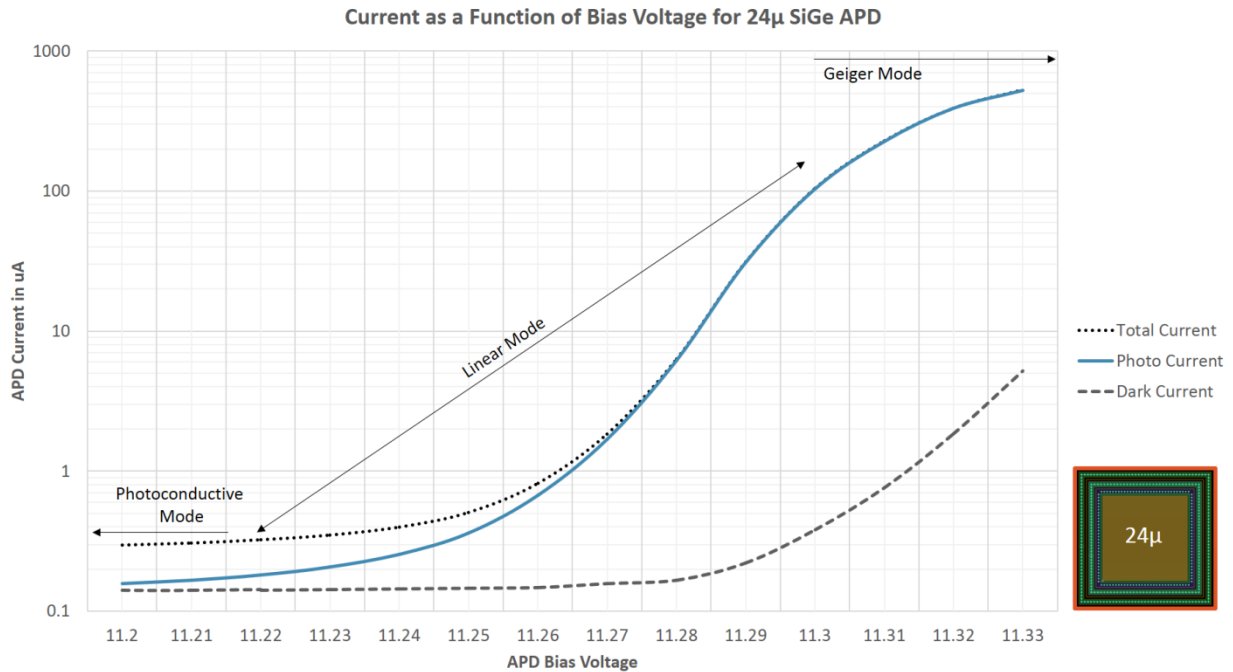
Figure 7.9 – I-V Curve of 24μ-F APD Tested at Freedom Photonics

As 560nm light was used as opposed to the ambient room light for the APDs tested at UNLV,

the only comparison that will be made is that of breakdown voltage, defined by where the APD

enters Geiger mode. Table 7.3 below shows a comparison of breakdown voltage values obtained

at UNLV (in Table 7.1, pg. 64) to those obtained at Freedom Photonics for the 5μ-F and 24μ-F

APDs.

APD	Breakdown Voltage (V)
UNLV 5μ-F	11.45
Freedom Photonics 5μ-F	11.29
UNLV 24μ-F	11.525
Freedom Photonics 24μ-F	11.3

Table 7.3 – Comparison of Breakdown Voltage of 5μ-F and 24μ-F APDs obtained at UNLV

vs. Freedom Photonics

The gain of the 5μ-F and 24μ-F APDs from 11.2V to 11.33V are shown in Figures 7.10 and 7.11,

respectively, below.
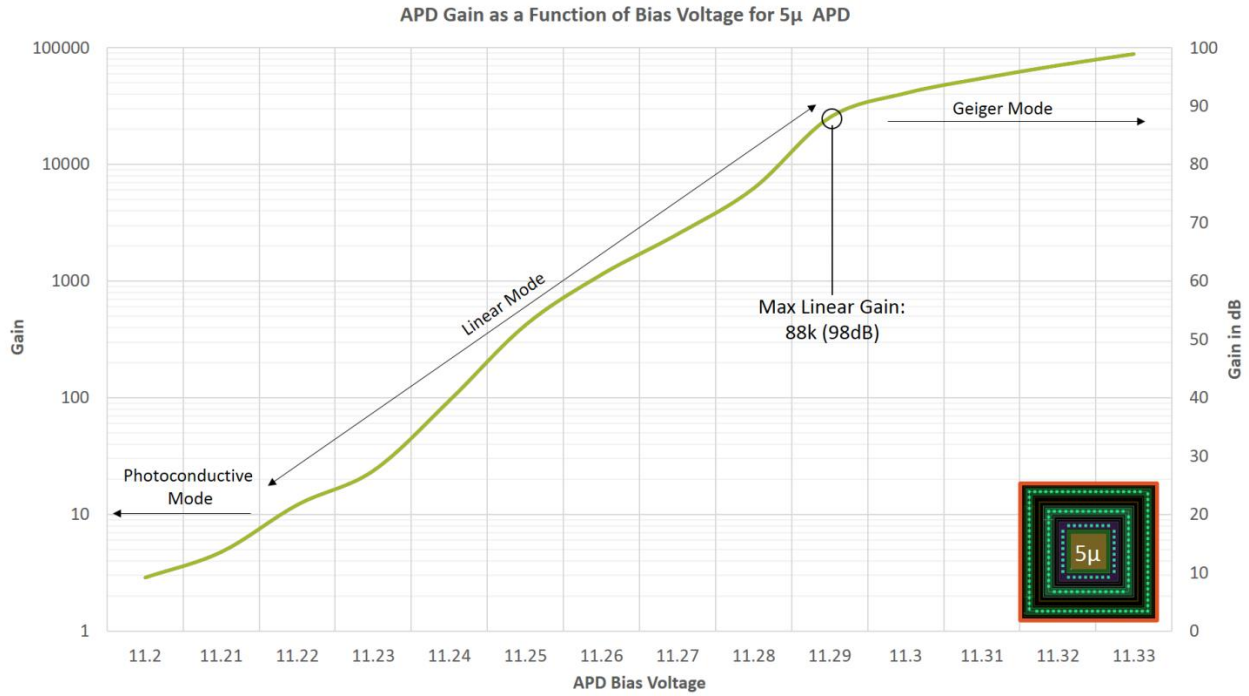
Figure 7.10 – Gain vs. Bias Voltage for 5μ-F APD Tested at Freedom Photonics
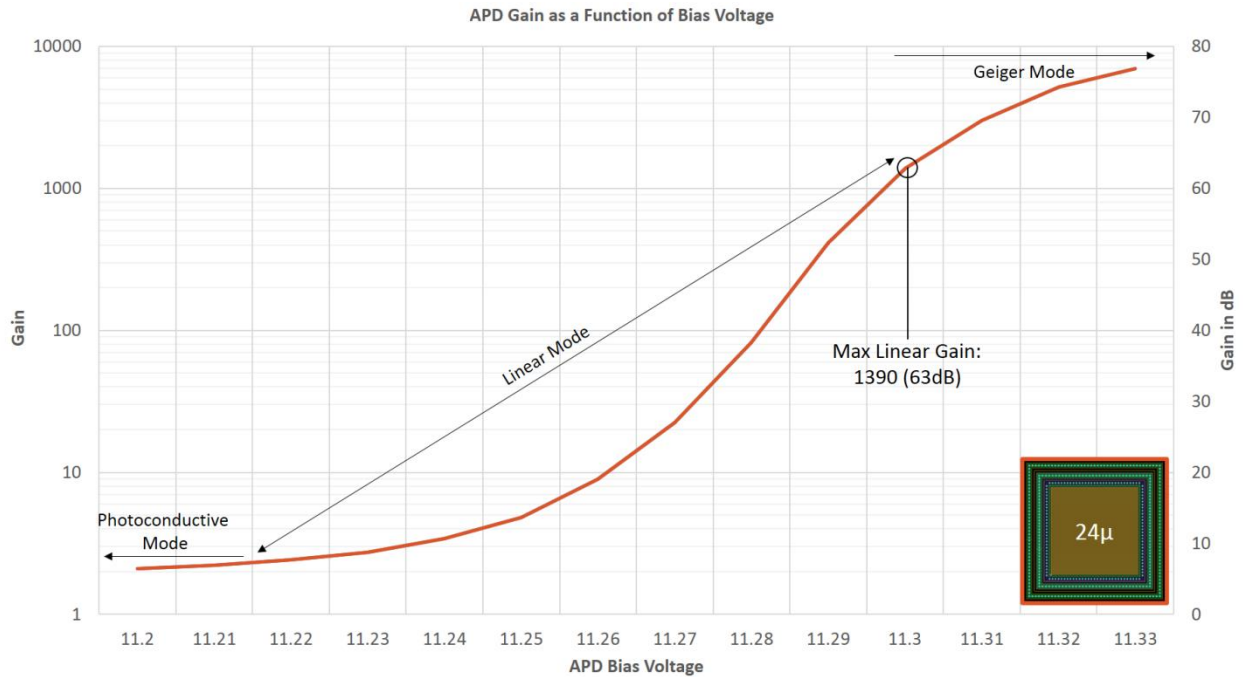
Figure 7.11 – Gain vs. Bias Voltage for 24μ-F APD Tested at Freedom Photonics

A comparison of the maximum linear gain for the APDs tested at UNLV to those tested at

Freedom Photonics is shown in Table 7.4 below.

APD	Maximum Linear Gain
UNLV 5μ-F	23,400
Freedom Photonics 5μ-F	88,000
UNLV 24μ-F	4,570
Freedom Photonics 24μ-F	1,390

Table 7.4 – Comparison of Maximum Linear Gain of 5μ-F and 24μ-F APDs obtained at

UNLV vs. Freedom Photonics

The difference in measurements between the APDs tested at UNLV and those tested at

Freedom Photonics could be due to many factors including temperature and equipment

differences. Additionally, the APDs tested at Freedom Photonics were packaged using SOIC-28s

while those tested at UNLV were packaged using TO-8s.

7.2 DCR and LCR Test Results

Figure 7.12 below shows the resulting DCR and LCR, using a 643nm (red) diffused

LED, for the 5μ-F APD.
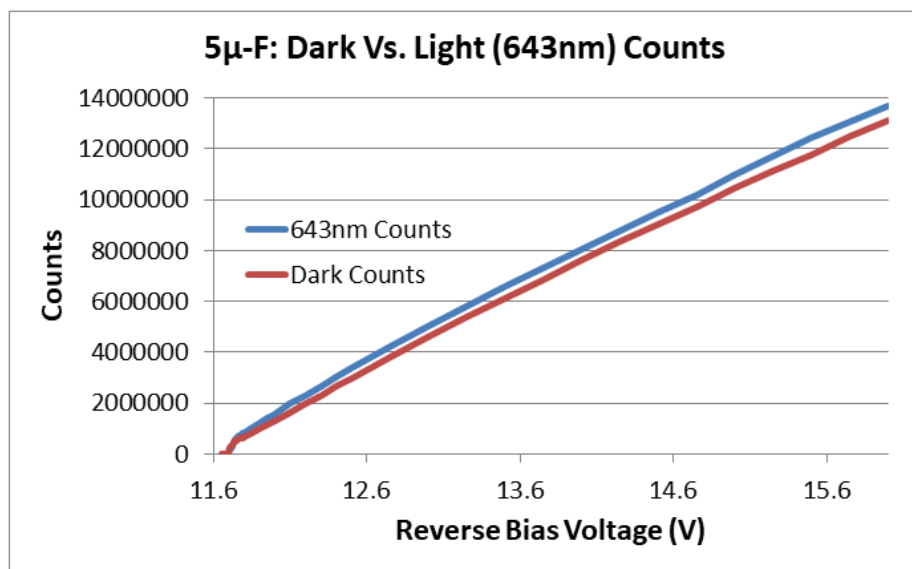
Figure 7.12 – DCR and LCR (643nm) vs. Bias Voltage for 5μ-F APD

DCR and LCR were measured from the breakdown voltage of the APD, defined as the voltage

where dark counts began to be present, up to 16V. Table 7.5 below shows the breakdown voltage

for each APD as well as the DCR at 13V, in which each APD is clearly in Geiger mode for single photon detection.

APD	Breakdown Voltage (V)	DCR @ 13V
Min-P	11.54	1,474,635.874
Min-F	11.45	2,031,397.703
5μ-P	11.75	3,698,961.733
5μ-F	11.65	4,605,167.47
24μ-P	11.73	5,228,326.939
24μ-F	11.82	4,285,885.964

Table 7.5 – Breakdown Voltage Determined from DCR Tests and DCR at 13V for Chip 1

APDs

Note that 13V in Table 7.5 above was simply used for comparison between APDs at an arbitrary voltage in which each APD is in Geiger mode. A lower voltage could have been used for comparison resulting in lower DCRs. At 13V, 24μ-P has the highest DCR and Min-P has the lowest. Figure 7.13 below shows the photon counts due solely to incident photons from the 643nm LED such that the DCR was subtracted from the 643 nm LCR which initially includes dark counts.
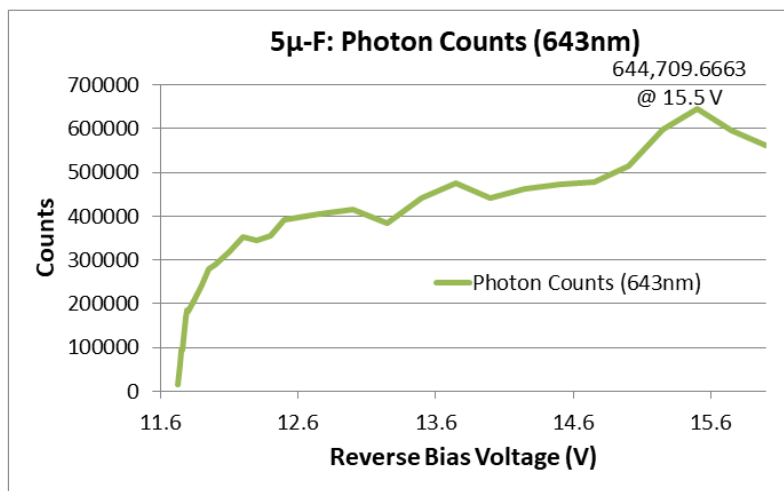
Figure 7.13 – Photon Counts vs. Bias Voltage for 5μ-F APD

Note that the maximum photon count for the 5μ-F APD appears at 15.5 V. Recall, however, that the photon counts do not reflect the number of incident photons. Instead, the photon counts

reflect the total number of photogenerated carriers due to incident photons after avalanche multiplication. These two plots for the remaining structures on Chip 1 (Min-P, Min-F, 5µ-P, 24µ-P, and 24µ-F) are shown in Appendix 7b. Table 7.6 below shows the maximum Photon Count for each APD up to 16V.

APD	Voltage (V)	Maximum Photon Count
Min-P	12.75	170,674.2181
Min-F	12	21,313.97706
5µ-P	16	1,241,766.772
5µ-F	15.5	644,709.6663
24µ-P	15	430,221.4705
24µ-F	16	946,732.3138

Table 7.6 – Maximum Photon Count and Corresponding Bias Voltage for Chip 1 APDs

Note that at some voltages, DCR is larger than LCR for some APDs, likely due to measurement error such as varying temperature, resulting in negative photon count in some instances which should be neglected. Note the count tests were only conducted up to 16V at which the maximum photon count occurs for some APDs, so the maximum photon count may increase with further reverse bias voltage, especially for the 5µ-P and 24µ-F APDs which have the largest maximum photon counts. It can be seen that Min-F has the lowest maximum photon count by a significant amount.

7.3 Spectral Response (Responsivity and QE) Test Results

The spectral response (responsivity and QE) for the 5µ-F and 24µ-F SiGe APDs on Chip 1 as well as the 10µ Si APD in Figure 4.1 in Chapter 4, pg. 21, were tested at Freedom Photonics using an optical test setup including a monochromator and a dark box. Figure 7.14 below shows the normalized spectral response for the 5µ-F SiGe APD measured at zero bias and using 10nm increments.
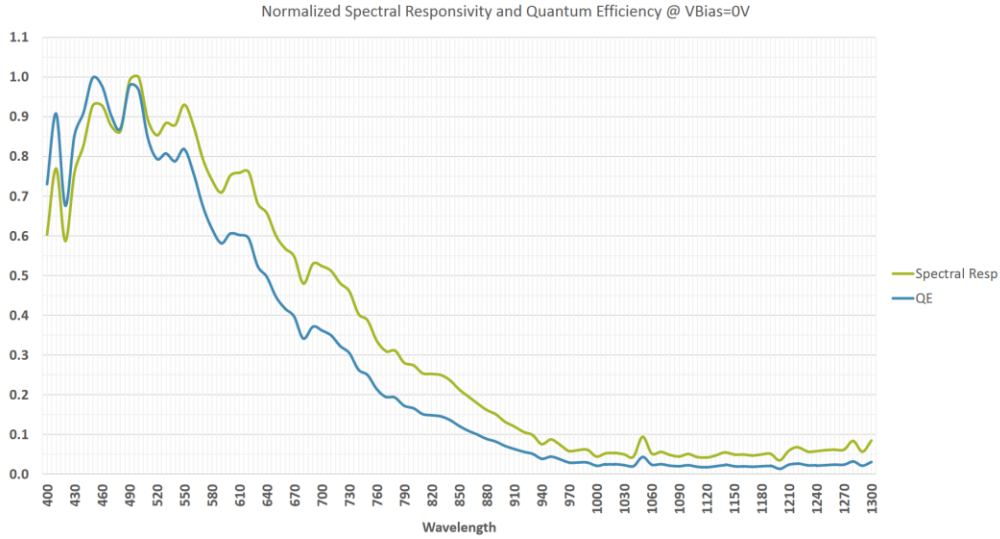
Figure 7.14 – Normalized Spectral Response for 5µ-F APD at Zero Bias

Note that the responsivity and QE peak at approximately 500nm then decrease exponentially with increasing wavelength. The aberrations in the spectral responses of the tested APDs are not due to noise but rather due to reflections since the APD does not have an anti-reflective (AR) coating. Figure 7.15 below shows the normalized spectral response for the 5µ-F APD measured in avalanche mode at 11.25V, 11.26V, and 11.27V using 40nm increments.
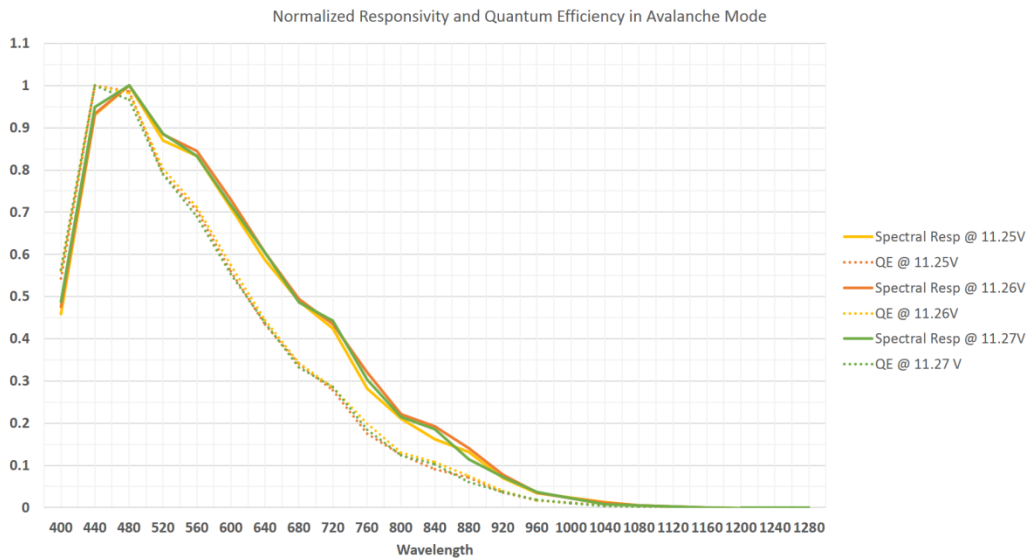
Figure 7.15 – Normalized Spectral Response for 5µ-F APD in Avalanche Mode at 11.25V, 11.26V, and 11.27V

Note that the spectral response is constant for varying reverse bias voltage. Figure 7.16 below

shows the normalized responsivity at zero bias for the 10µ Si APD for comparison to the 5µ-F
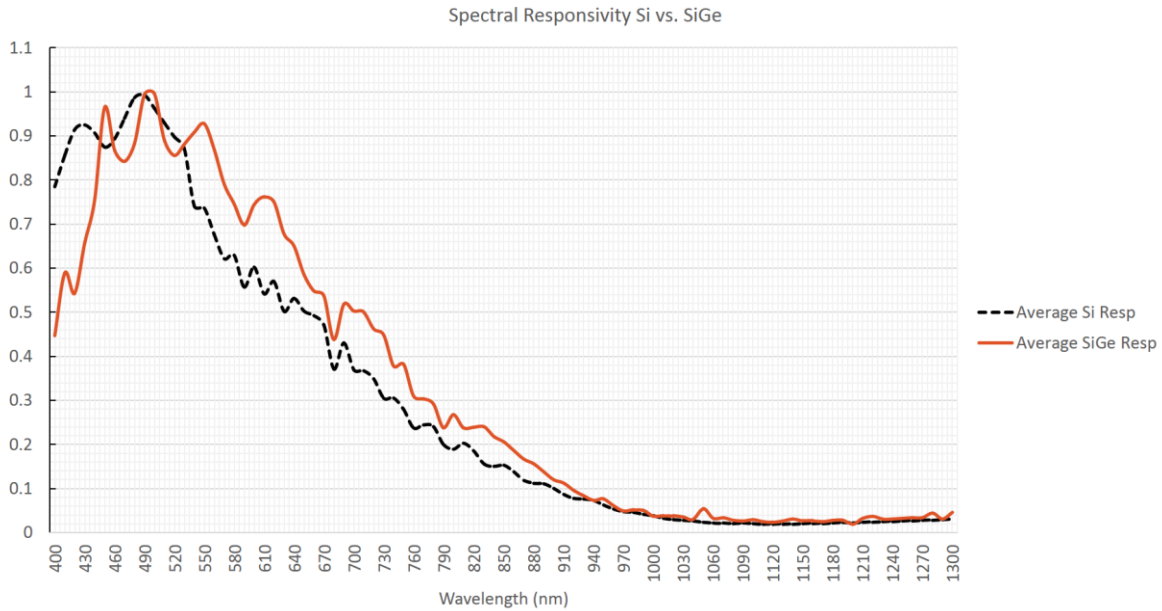
SiGe APD.

Figure 7.16 – Comparison of Normalized Responsivity for 10µ Si vs. 5µ-F SiGe APDs at

Zero Bias

Notice the peak responsivity for the 10µ Si APD is at 480 nm and 500 nm for the 5µ-F SiGe

APD. Furthermore, the 5µ-F SiGe APD exhibits consistently enhanced response from 530 nm to

1,000 nm compared to the 10µ Si APD, confirming the initial hypothesis detailed in Table 4.1 in

Chapter 4, pg. 22. The attenuated response at wavelengths longer than 1000 nm is likely due to

the graded SiGe P+ layer shown in Figure 5.10 in Chapter 5, pg. 32, being only approximately

200 nm thick, thus limiting the enhanced response of SiGe over Si at NIR wavelength. This

shortcoming can be remedied by a thicker SiGe layer added through post-processing. Beyond

1000 nm the response of both types of APDs are at the noise floor of the instrument. However,

an additional test was done to show that the SiGe APDs still have usable response up to 1200

nm. The 5µ-F SiGe APD was extensively tested between 1000 nm to 1200 nm to determine the

true detection limits in the NIR region. Figure 7.17 below shows the spectral response with current as a function of reverse bias voltage for the 5μ-F APD operating in photoconductive mode from 0V to 11V for varying wavelengths of 1000nm, 1050nm, 1100nm, 1150nm, and 1200nm compared to the dark current.
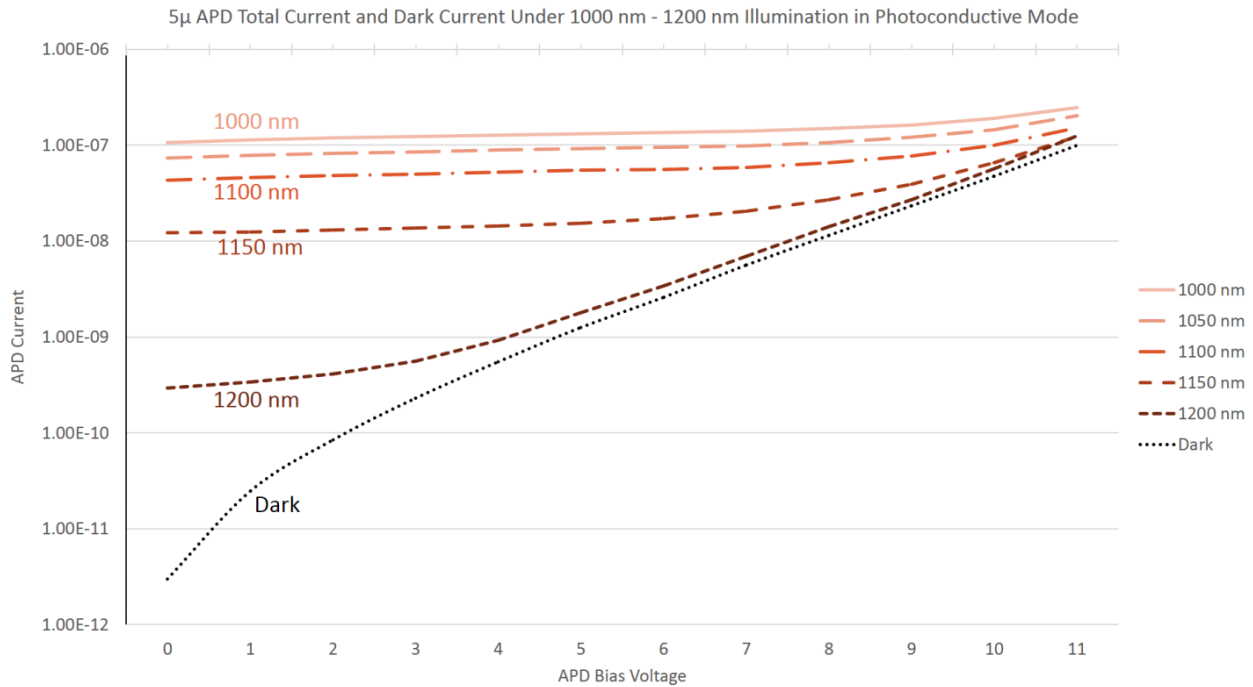
Figure 7.17 – Spectral Response (Current vs. Bias Voltage) of 5μ-F APD in Photoconductive Mode (0V to 11V) for Dark State and Wavelengths of 1000nm, 1050nm, 1100nm, 1150nm, and 1250nm

Notice that detection out to 1200 nm is possible at zero bias since the dark current contribution is minimal. At higher bias voltages nearing 11V, however, distinction between dark current and total current for a wavelength beyond 1100 nm becomes unlikely especially when considering other factors such as noise. Figure 7.18 below illustrates the same principle as above for reverse bias voltages in the avalanche region of the 5μ-F APD showing that avalanche mode operation is only useful for wavelengths up to 1100 nm as the dark current multiplication exceeds that of photocurrent for wavelengths beyond 1100 nm.
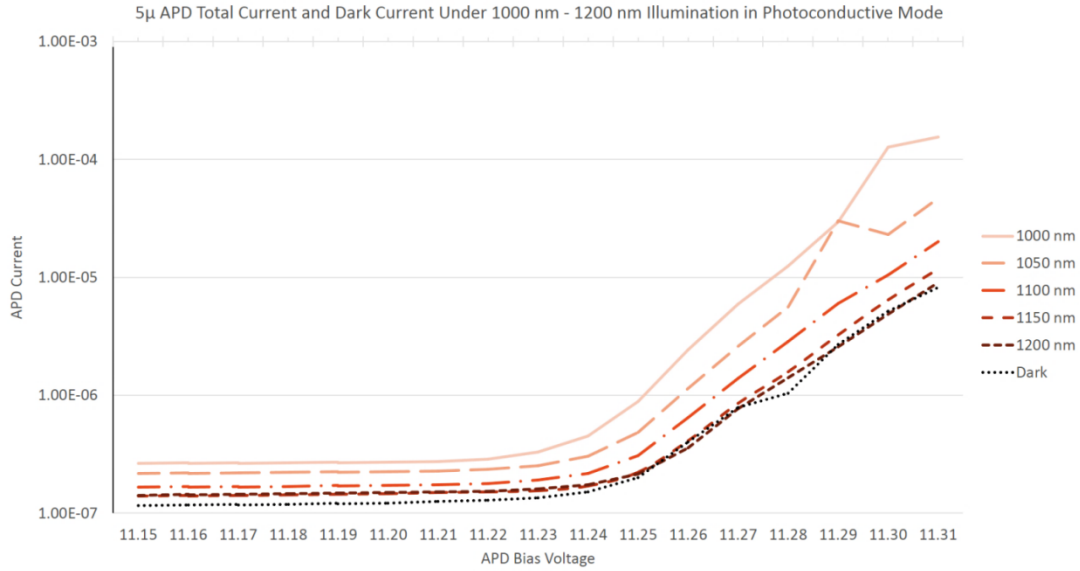
Figure 7.18 – Spectral Response (Current vs. Bias Voltage) of 5µ-F APD in Avalanche Mode (11.15V to 11.31V) for Dark State and Wavelengths of 1000nm, 1050nm, 1100nm, 1150nm, and 1250nm

Figure 7.19 below provides an alternative way at looking at this data by observing the ratio of photocurrent to dark current as a function of wavelength and reverse bias voltage such that detection of a wavelength is not possible for a ratio below 1 since the dark current exceeds the photocurrent.
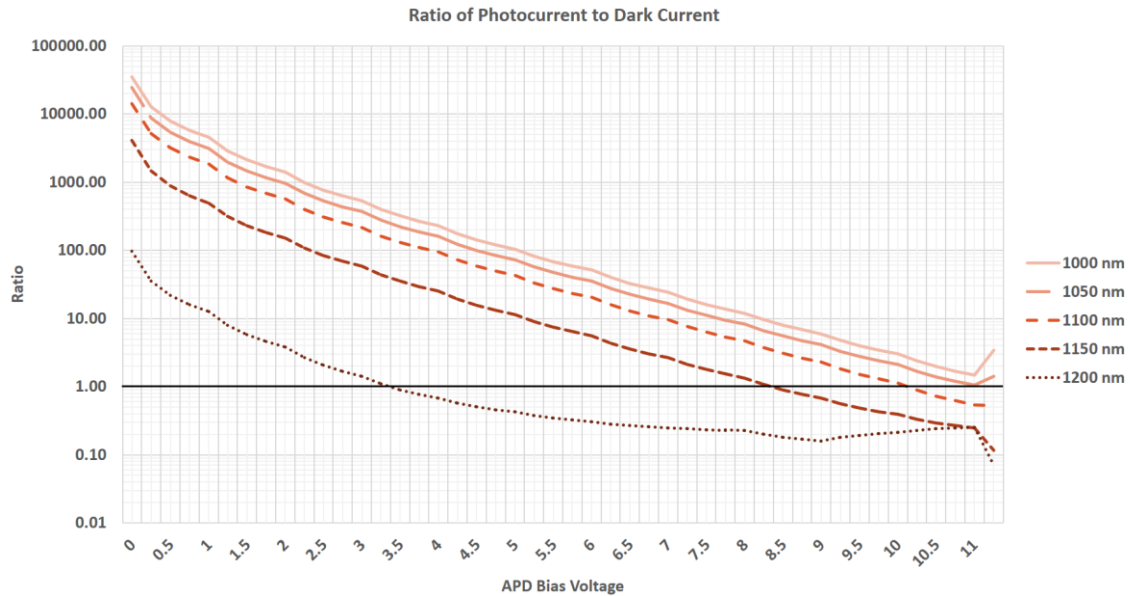
Figure 7.19 – Spectral Response (Ratio of Photocurrent to Dark Current vs. Reverse Bias Voltage) of 5µ-F APD in Photoconductive Mode (0V to 11V) or Wavelengths of 1000nm, 1050nm, 1100nm, 1150nm, and 1250nm

Notice that detection of wavelengths up to 1200 nm is possible for a reverse bias below 3V. Furthermore, observing the lower edge of the avalanche region beyond 11V, it is apparent that the ratio of photocurrent to dark current begins to increase for wavelengths up to 1050 nm due to the avalanche gain. Longer wavelengths such as 1150 nm and 1200, however, appear not to benefit from this gain as their photocurrent to dark current ratios decrease at the onset of avalanche multiplication.

7.3a Extending Spectral Response (Double Anode)

In order to further extend the spectral response of SiGe APDs without any process modifications, the graded SiGe P+ (anode) can be connected to the substrate in a "double" anode configuration as shown in Figure 7.20 below such that the substrate induced photocurrent is added to the total current.
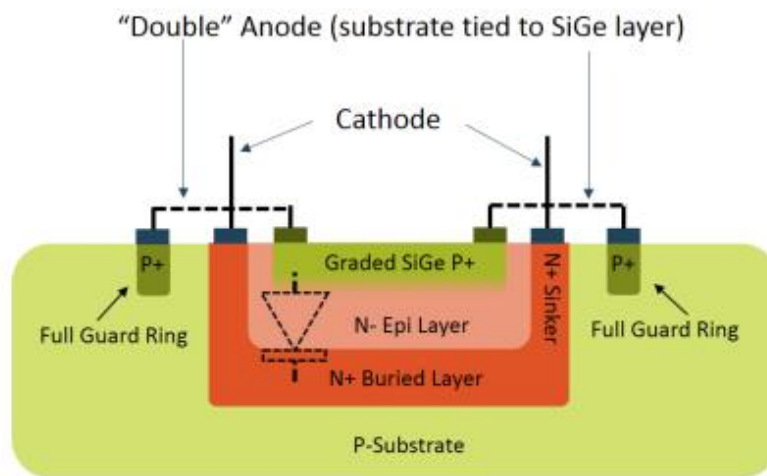
Figure 7.20 – Cross Section of APD Connected in Double Anode Configuration

As a result, the cathode becomes surrounded by the anode on all sides and significantly improves the NIR response. This is shown in Figure 7.21 below displaying the normalized spectral response of the 24μ-F SiGe APD for zero bias due to the contribution from the SiGe P+ anode as well as the substrate.
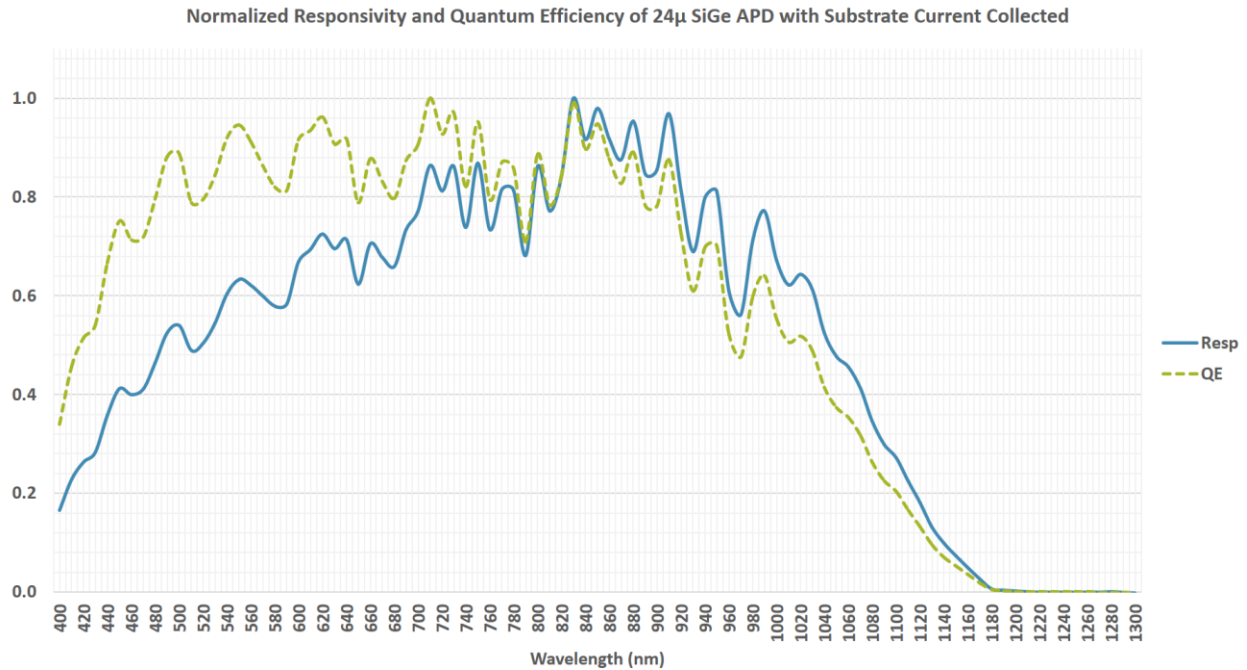
Figure 7.21 – Normalized Spectral Response for 24μ-F APD at Zero Bias Connected in Double Anode Configuration

Notice the high responsivity from approximately 550 nm to 1050 nm, with peak responsivity at 830 nm after which the response sharply drops off toward a final λ_c of 1180 nm. This allows for a broad range of applications.

The double anode connection, however, has the caveat that no electronics can be implemented on the same chip die since noise from electronics, particularly fast digital edges, on the same chip will couple into the substrate near the APD and be indistinguishable from photocurrent. Additionally, the double anode connection is not able to be connected to a transimpedance amplifier (TIA), so a different topology such as a current sense amplifier would

have to be used to measure the photocurrent. Regardless, a two-chip solution is appropriate for many applications particularly due to the low cost of the photodetector chip as no additional wafer processing is required with the double anode connection.

Figure 7.22 below shows responsivity and QE of the 10u Si APD connected in the double anode configuration, exhibiting a spectral response extended further into the NIR region compared to the normalized spectral response in Figure 7.16, pg. 73, in which the substrate current was not collected.
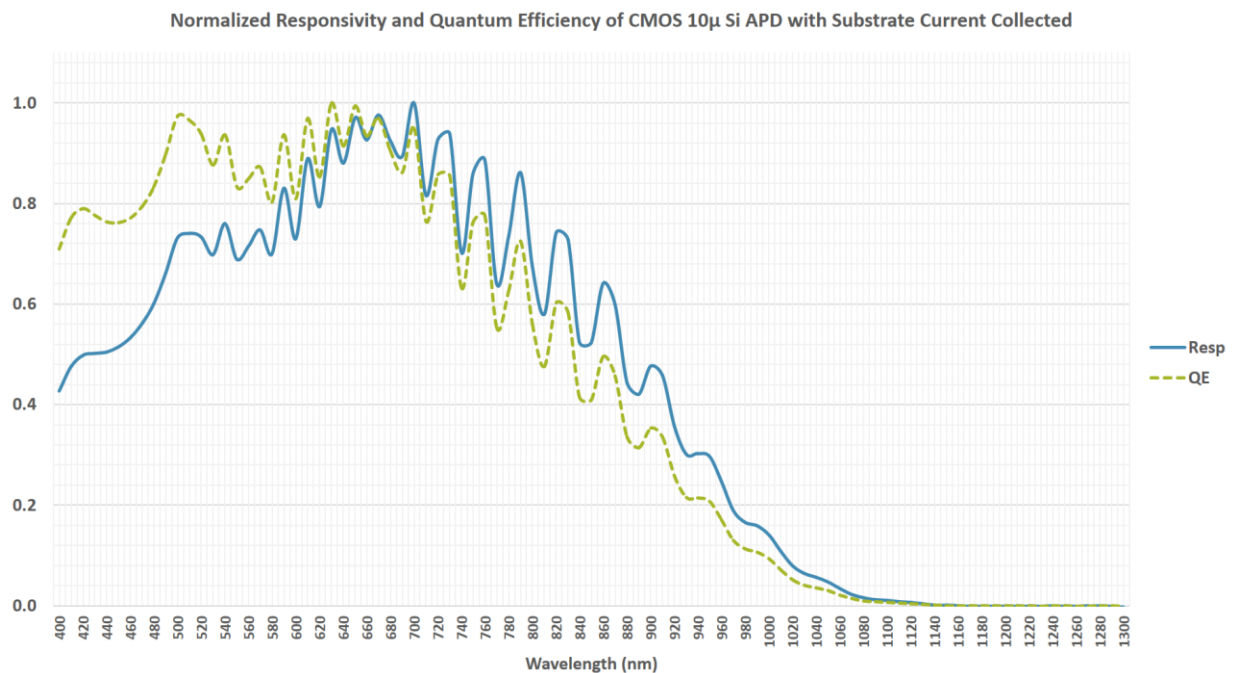
Figure 7.22 – Normalized Spectral Response for 10μ Si APD at Zero Bias Connected in

Double Anode Configuration

Notice the peak responsivity occurs at 720 nm with the response falling sharply beyond 1000 nm with a λ_c around 1100 nm. Figure 7.23 below shows the previous two normalized spectral response figures plotted together for comparison of the 10μ Si and 24μ-F SiGe APDs, both connected in the double anode configuration.
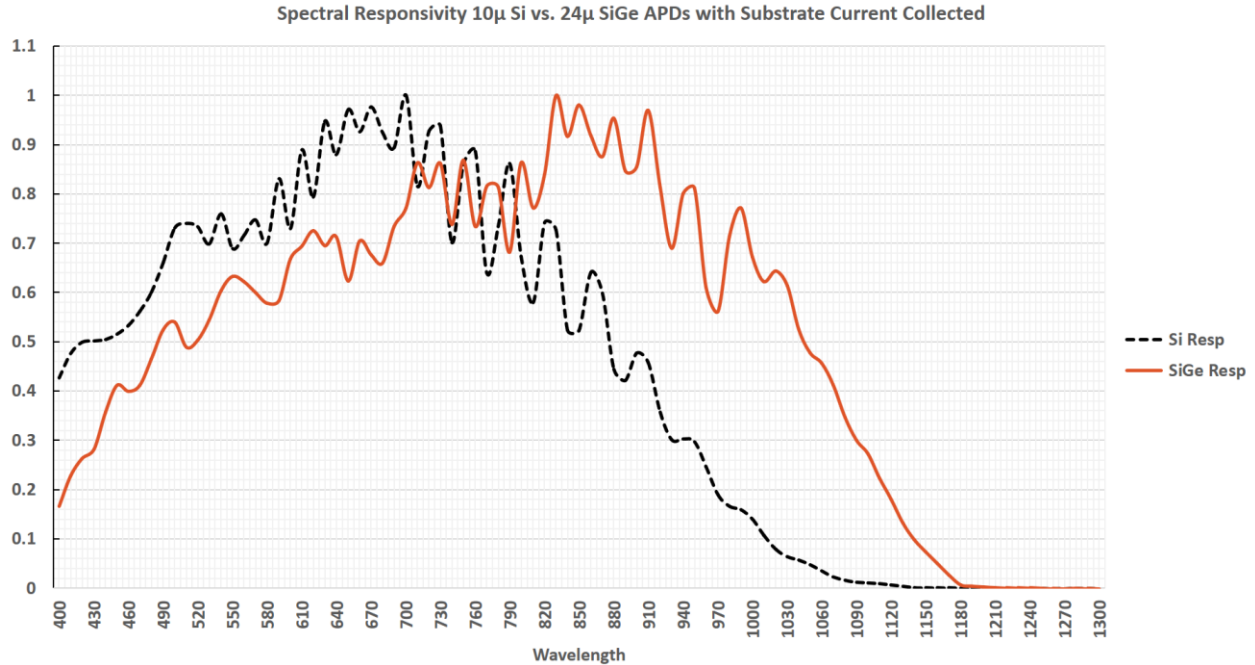
Figure 7.23 – Comparison of Normalized Spectral Responsivity for 10µ Si and 24µ-F SiGe APDs at Zero Bias Connected in Double Anode Configuration

As expected, while the spectral response has been extended for both APDs by connecting them in the double anode configuration, the 24µ-F SiGe APD exhibits enhanced NIR response compared to the 10µ Si APD. The 24µ-F SiGe APD has a peak responsivity at 830 nm and λ_c of approximately 1180 nm compared to 720 nm and 1100 nm, respectively, for the 10µ Si APD.

It is hypothesized that the reason for the SiGe APD's enhanced NIR performance is not due to the shallow SiGe layer (around 200 nm) but rather due to the deep buried N-well layer. The buried N-well for the SiGe process is at a depth of 6 µm while the N-well in the Si process is at 3.5 µm. This may account for the shifted peak from 730 nm to 820 nm and the enhanced NIR response in SiGe.

Though the previous normalized spectral response plots demonstrate a valid shape of the spectral responses, they do not display responsivity with proper units of A/W. In order to get a true indication of responsivity, a calibrated 850 nm laser was coupled to the tested APDs with a

fiber probe and a dark box was utilized to keep out all ambient light and ensure a highly accurate

responsivity measurement. The spot size of the single mode fiber probe used was 10 μm and able

to fit within the total photoactive area for the 24μ APDs. The smaller SiGe APDs as well as the

10μ Si APD, however, were too small for the spot size and were not tested for responsivity.

Figure 7.24 below shows the spectral response with responsivity in A/W for the 24μ-F SiGe

APD with standard as well as double anode connection.
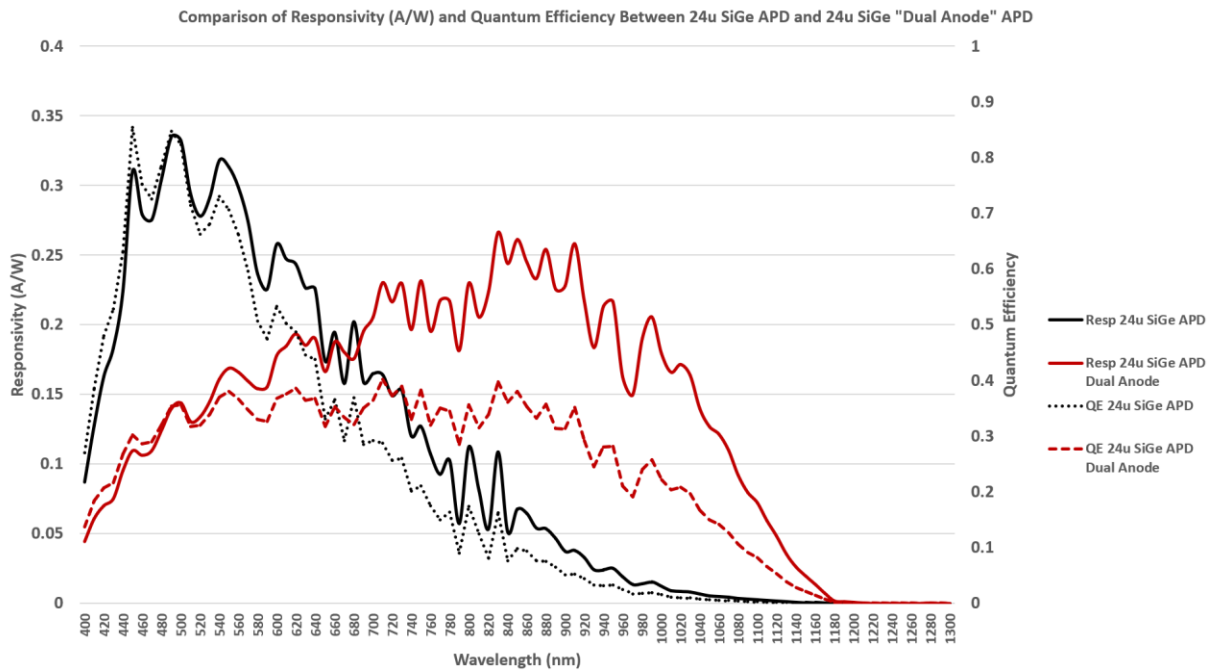
Figure 7.24 – Comparison of Spectral Response (with Responsivity in A/W) for 24μ-F vs.

Double Anode Connected 24μ-F APDs at Zero Bias

Notice the standard connected APD has a peak responsivity of 0.34 A/W at 500 nm and a high

QE peak of 85% at 450 nm. The double anode connected APD has a slightly lower peak

responsivity of 0.27 A/W at 830 nm but a significantly lower QE peak of 39% also at 830 nm.

This allows for much flexibility with these SiGe APDs as one could choose either a blue

sensitive or NIR sensitive response simply by changing the connection of one pin. Table 7.7

below summarizes the spectral response results of the APDs tested at Freedom Photonics.

80

Type of APD	SiGe	SiGe	Si
Dimensions	24μ x 24μ	5μ x 5μ	10μ x 10μ
Area	576 μ^2	25 μ^2	100 μ^2
Dark Current	5 pA	3 pA	3 pA
Max APD Gain	1390 (63dB)	88,000 (99 dB)	1000 (60 dB)
Spectral Peak	500 nm (single anode) 830 nm (dual anode)	500 nm	480 nm (single anode) 660 nm (dual anode)
Cutoff Wavelength	1180 nm	1180 nm	1100 nm
Responsivity	0.34 A/W @ 500 nm (single anode) 0.27 A/W @ 830 nm (dual anode)	Not Tested	Not Tested
QE	85% @ 450 nm (single anode) 39% @ 830 nm (dual anode)	Not Tested	Not Tested

Table 7.7 – Summary of Spectral Responses for 5μ-F SiGe, 24μ-F SiGe, and 10μ Si APDs

Tested at Freedom Photonics

Chapter 8: Conclusion

Extensive research, design, data collection, and analysis requiring meticulous documentation and organization was performed in order to accurately and effectively characterize several APDs and ensure success in characterizing more APDs in the future. The current information surrounding the APDs tested thus far including the analysis of their I-V curves, gain, DCRs, responsivities, and QEs as well as scrutiny of the current test setups and procedures at both UNLV and Freedom Photonics provides significant insight for the next stages regarding this research.

Much future work remains in order to develop APDs for use in numerous applications including, but not limited to, a monolithic integrated photon-counting receiver for use by NASA. Overall, the tested SiGe APDs exhibit improved characteristics compared to Si APDs and possess versatile qualities associated with their different modes of operation and vast range of gains, allowing for much potential in countless applications. The spectral response of these SiGe APDs, however, is desired to be extended further which will likely require process modifications including additional selective growth of SiGeSn on top of the finished CMOS wafer [37]. Furthermore, readout circuitry including a TIA and time-to-digital converter (TDC) will need to be designed on a readout integrated circuit (ROIC) for practical use of a final APD design.

The APD variants on Chip 2 and Chip 3 as well as the SiPM pixel and SiPM array on Chip 1 will need to characterized, and all APDs require further characterization in regard to response time, capacitance characteristics, dark count temperature dependence, etc. which will greatly benefit from the use of software for APD modeling. The APD variants on Chip 2 and Chip 3 will also be specifically tested in order to accurately determine how much of the NIR

enhancement is due to the SiGe material system, while holding other parameters constant. The use of anti-reflective (AR) coating on the APDs will also be investigated.

In order to more efficiently test the large number of APD structures on Chip 2 and Chip 3, the test setup at UNLV should be improved by use of a monochromator and spectrometer. A general purpose interface bus (GPIB) should also be utilized in order to connect the testing equipment for more automated testing and recording of data. Lastly, the power uniformity tests and LED calibration will be continued in order to allow testing of responsivity, quantum efficiency, and, likely more importantly, PDE at UNLV.

Chapter 5 Appendix

Appendix 5a: Chip 1 TO-8 Bonding Diagrams
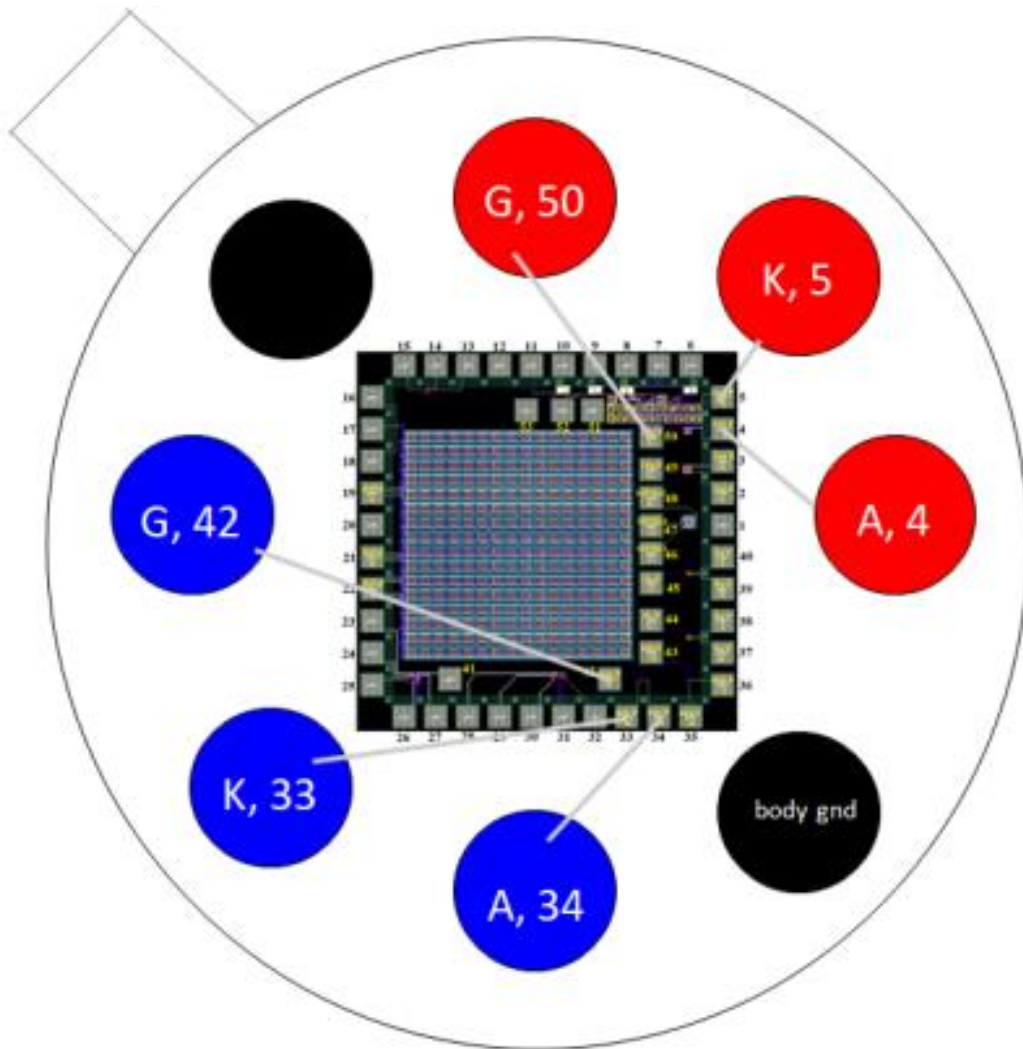
Figure A.5a.1 – Version 1
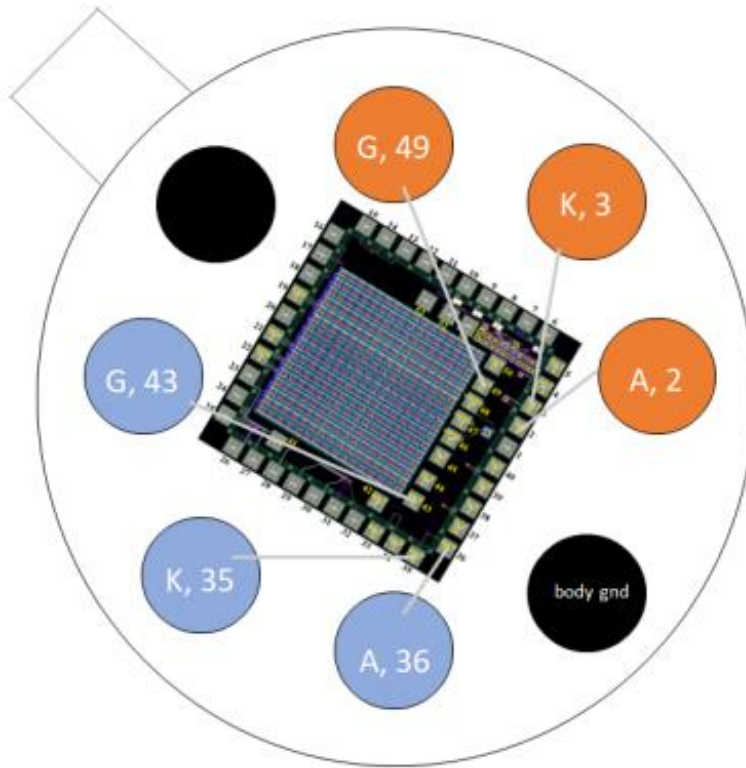
Figure A.5a.2 – Version 2
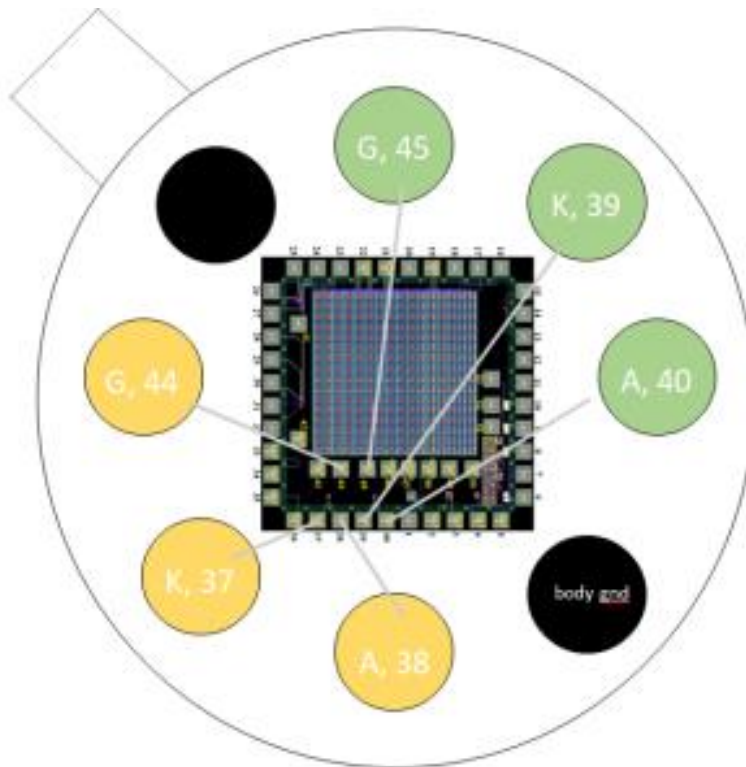
Figure A.5a.3 – Version 3
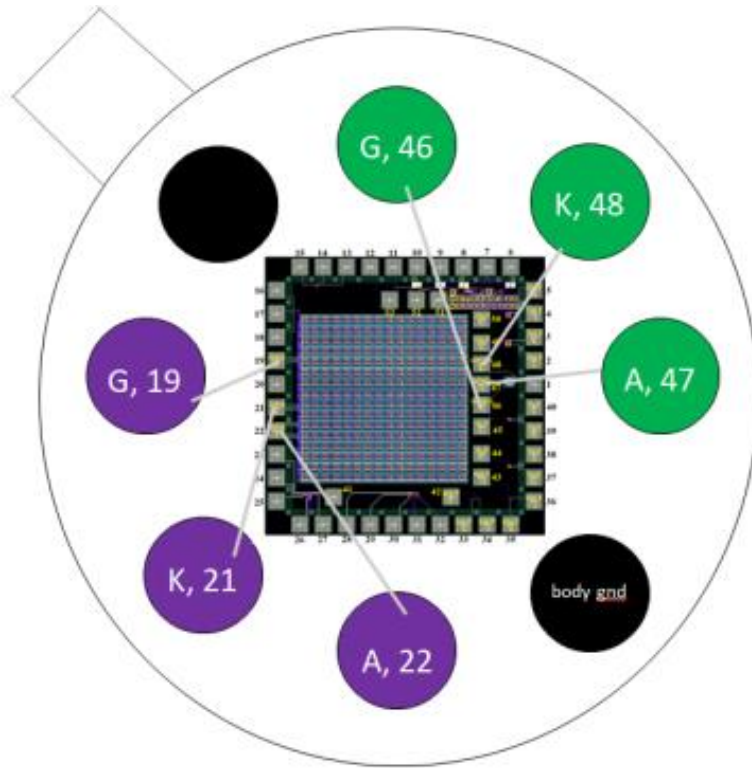
Figure A.5a.4 – Version 4

Appendix 5b: Chip 2 APD Layouts
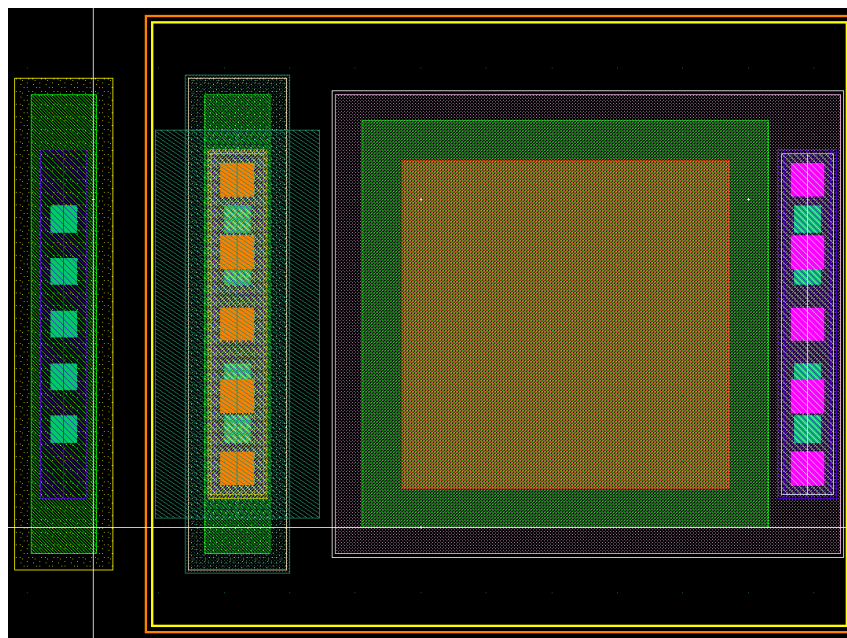
Figure A.5b.1 – 5μ Elementary
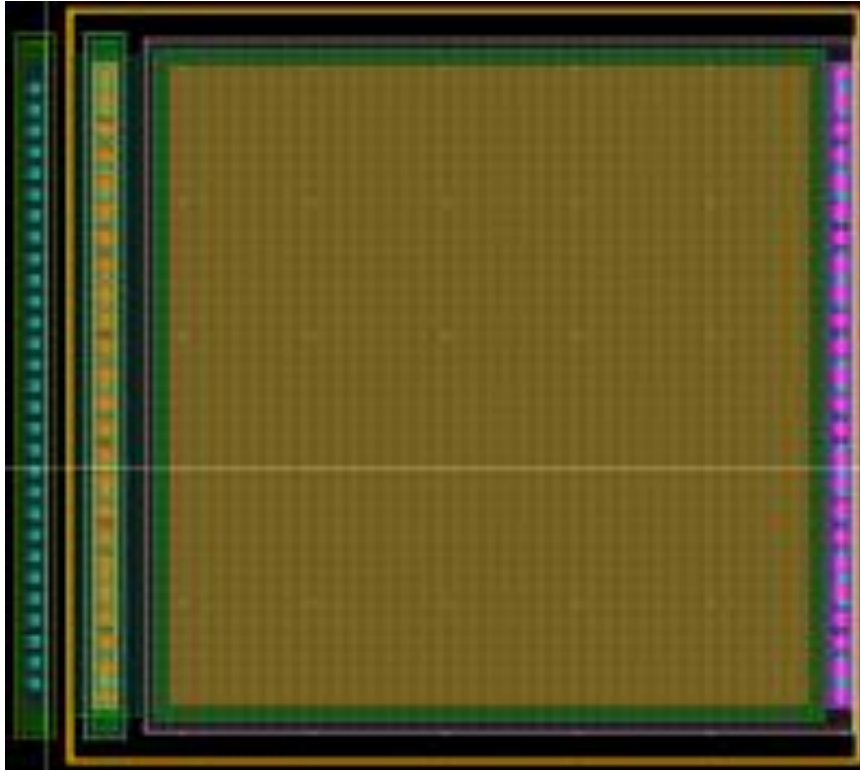
Figure A.5b.2 – 24μ Elementary
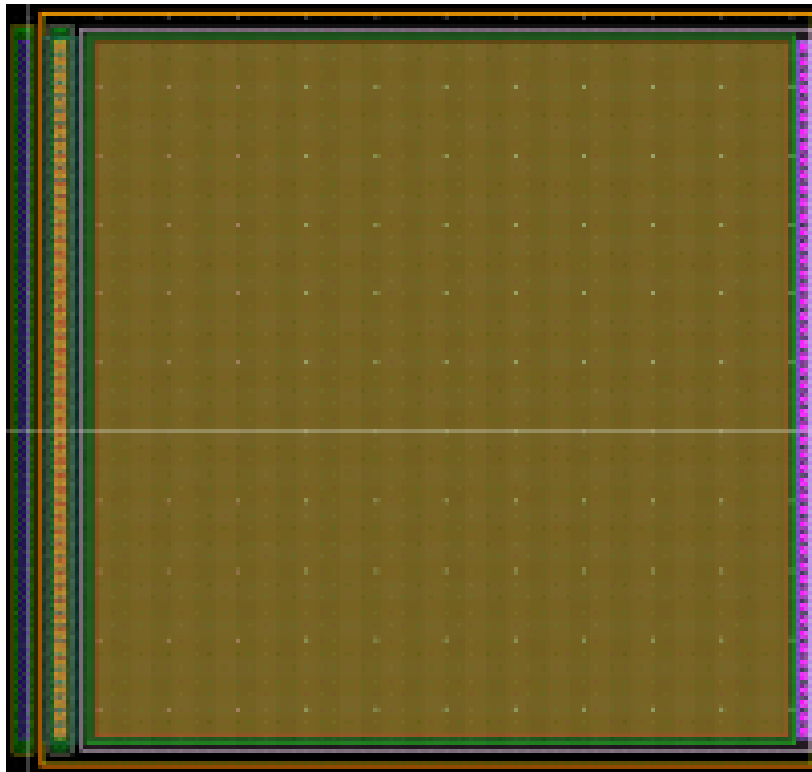
Figure A.5b.3 – 50μ Elementary
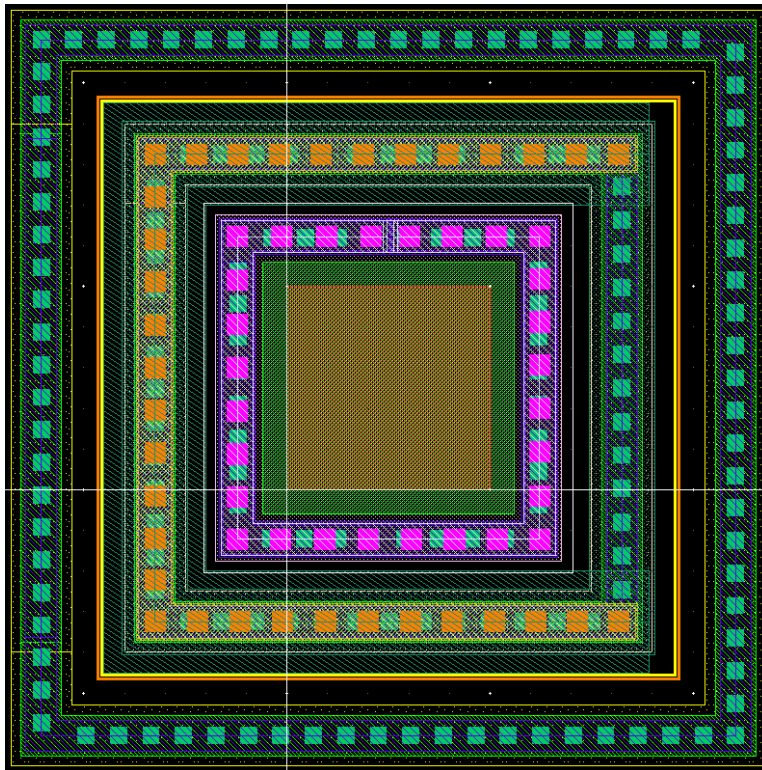
Figure A.5b.4 – 5µ Standard
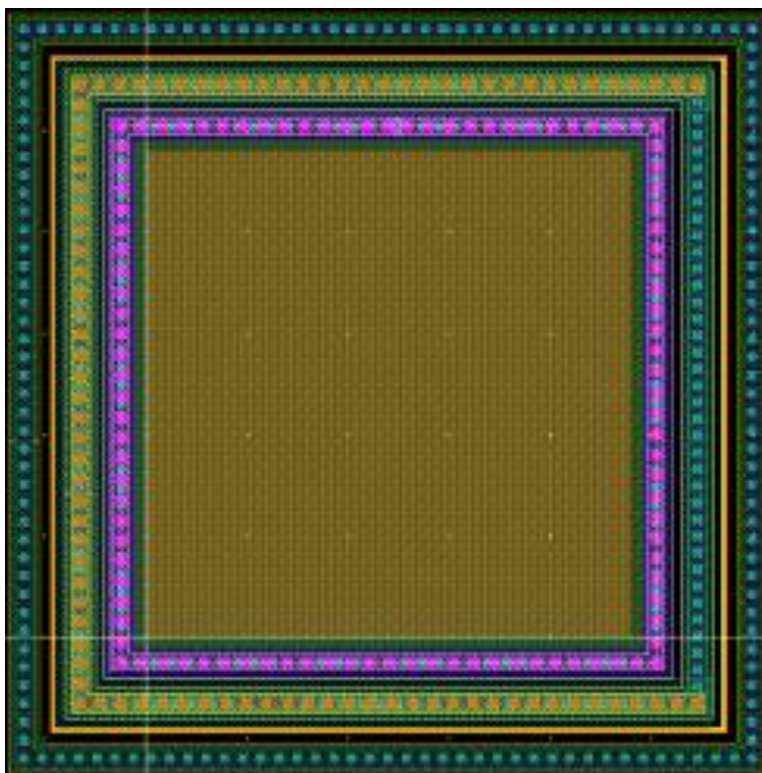
Figure A.5b.5 – 24µ Standard
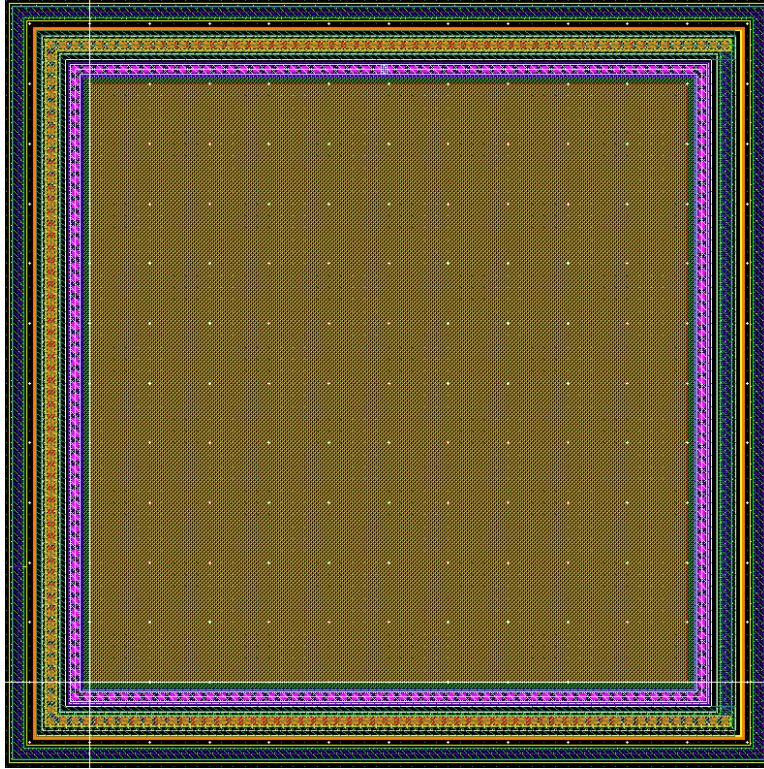
Figure A.5b.6 – 50μ Standard
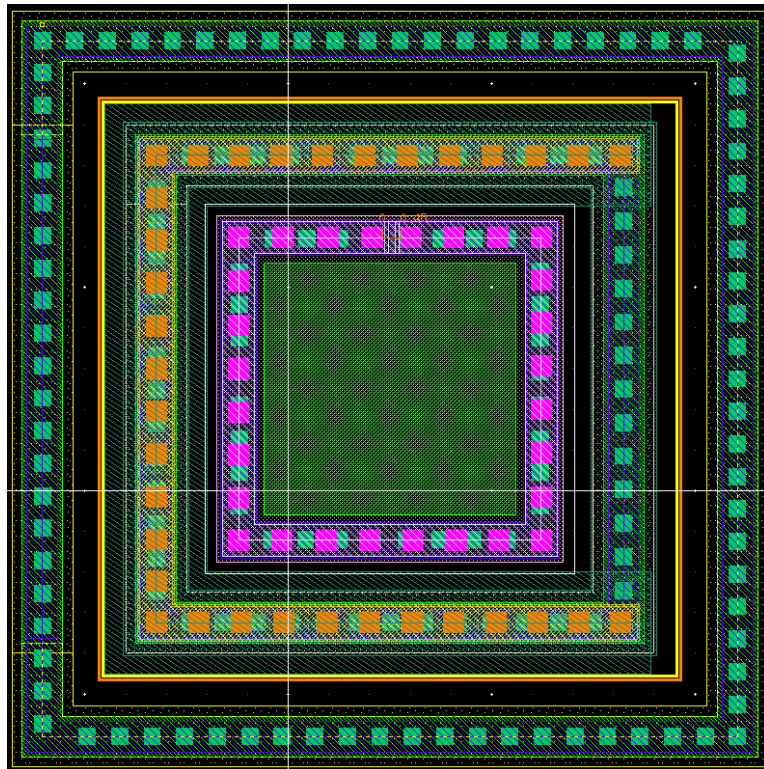
Figure A.5b.7 – 5μ No EMITT
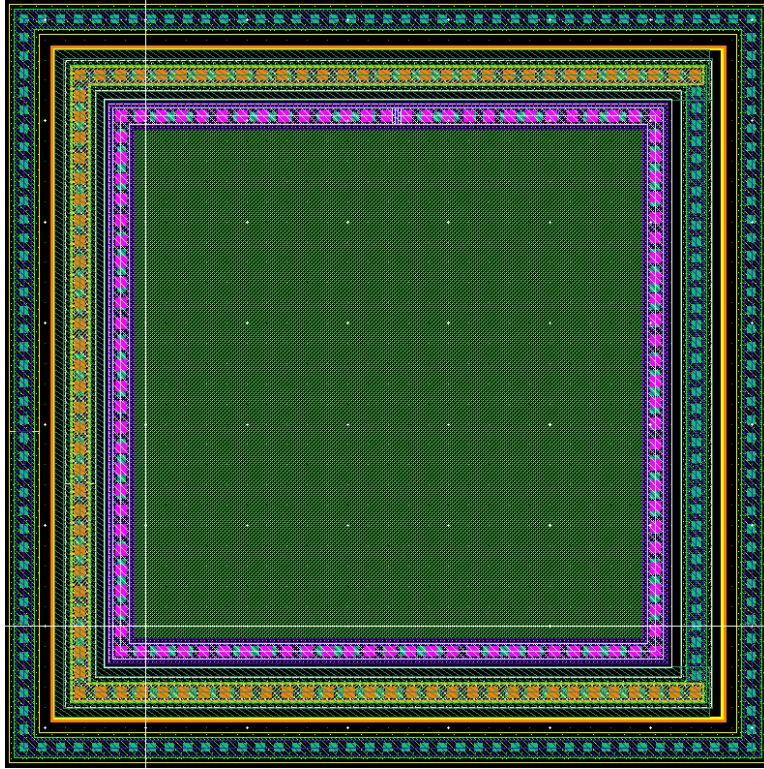
Figure A.5b.8 – 24µ No EMITT
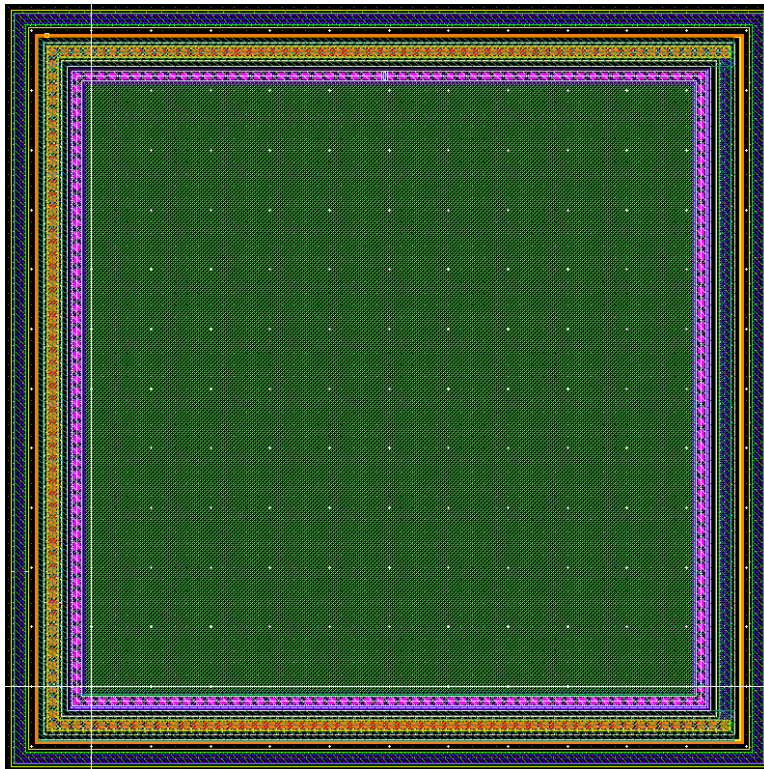
Figure A.5b.9 – 50µ No EMITT
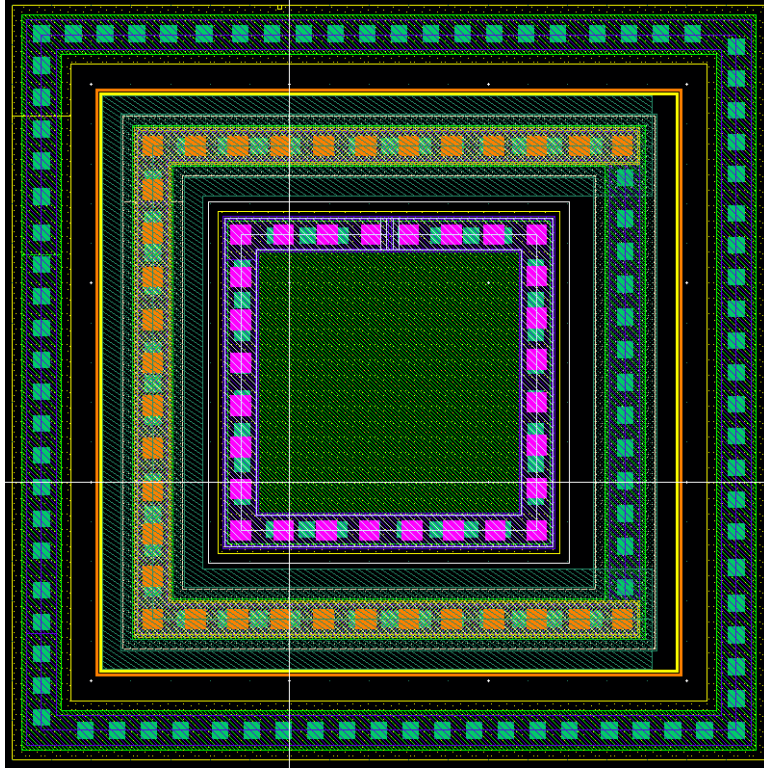
Figure A.5b.10 – 5µ BPOLY/PPLUS
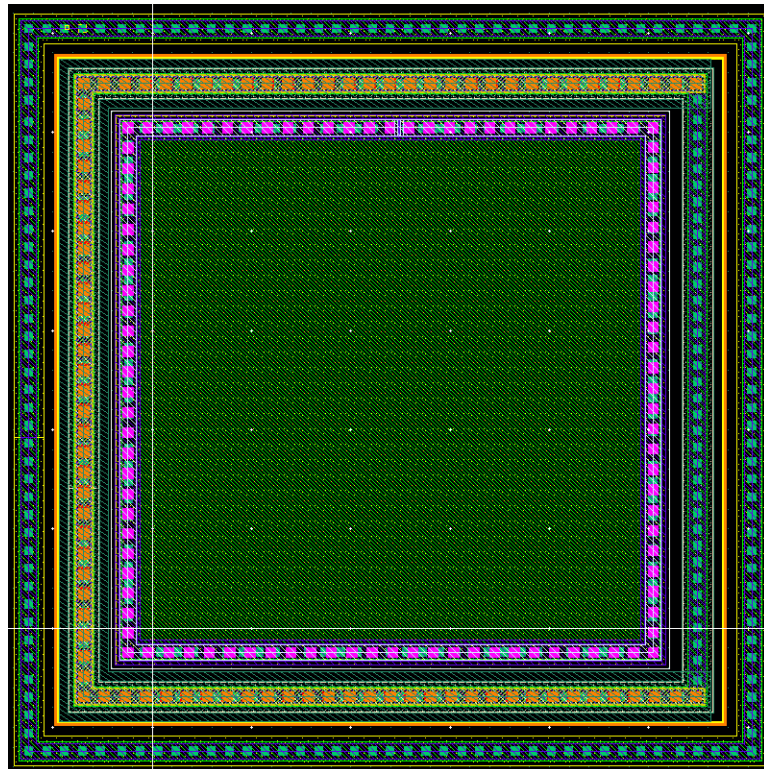
Figure A.5b.11 – 24µ BPOLY/PPLUS
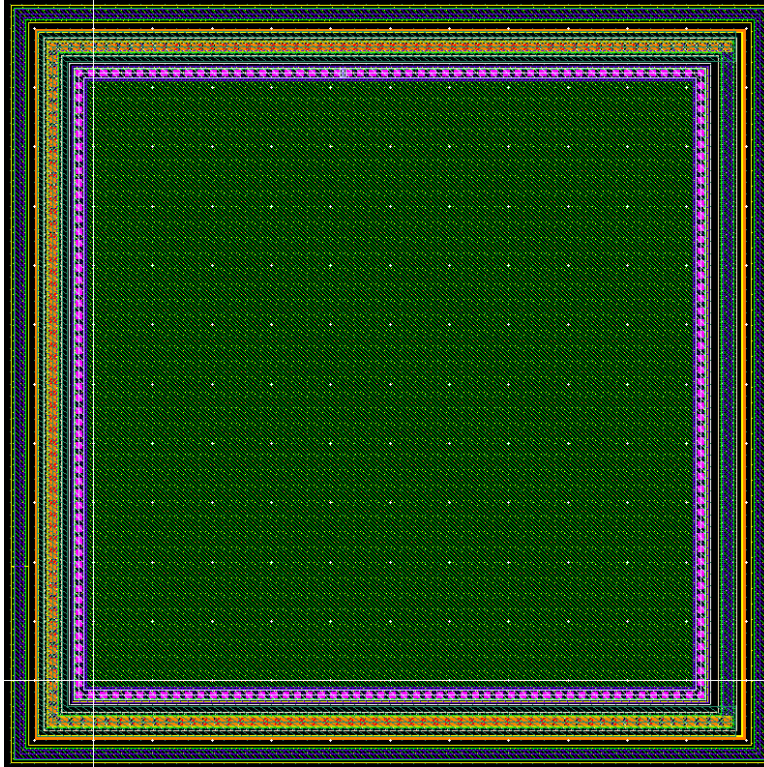
Figure A.5b.12 – 50μ BPOLY/PPLUS
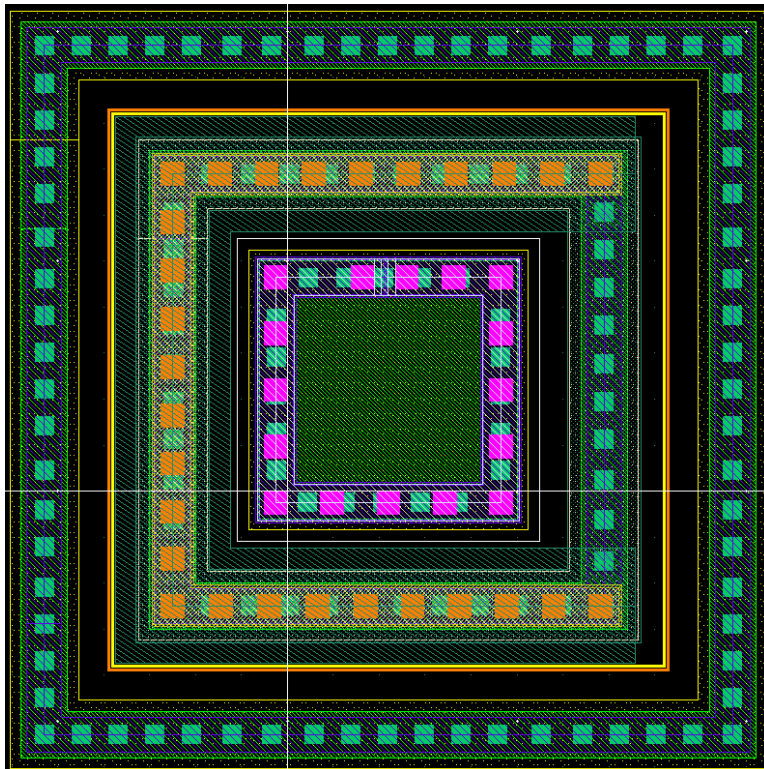
Figure A.5b.13 – 5μ BPOLY/PPLUS Smaller
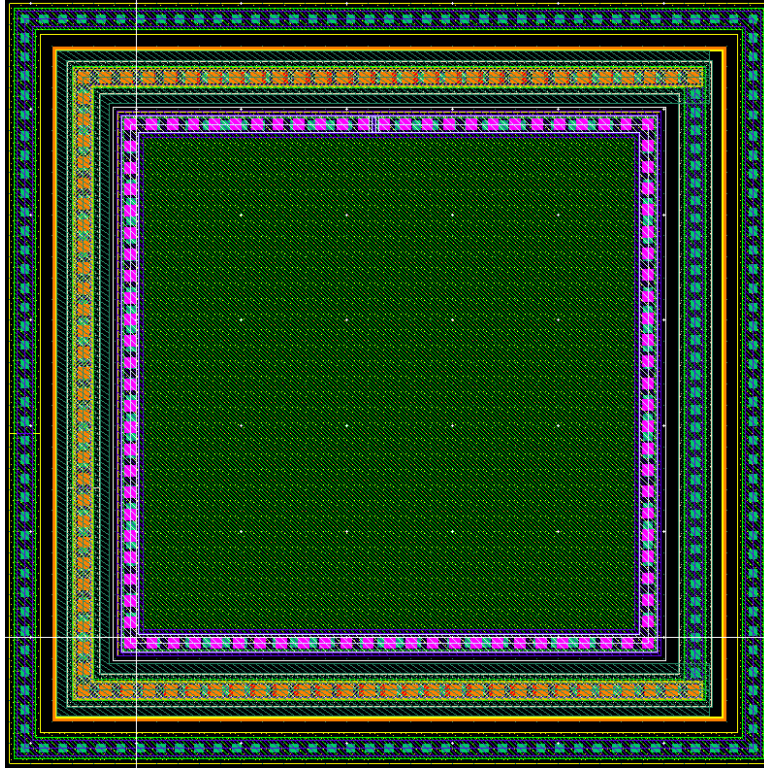
Figure A.5b.14 – 24μ BPOLY/PPLUS Smaller
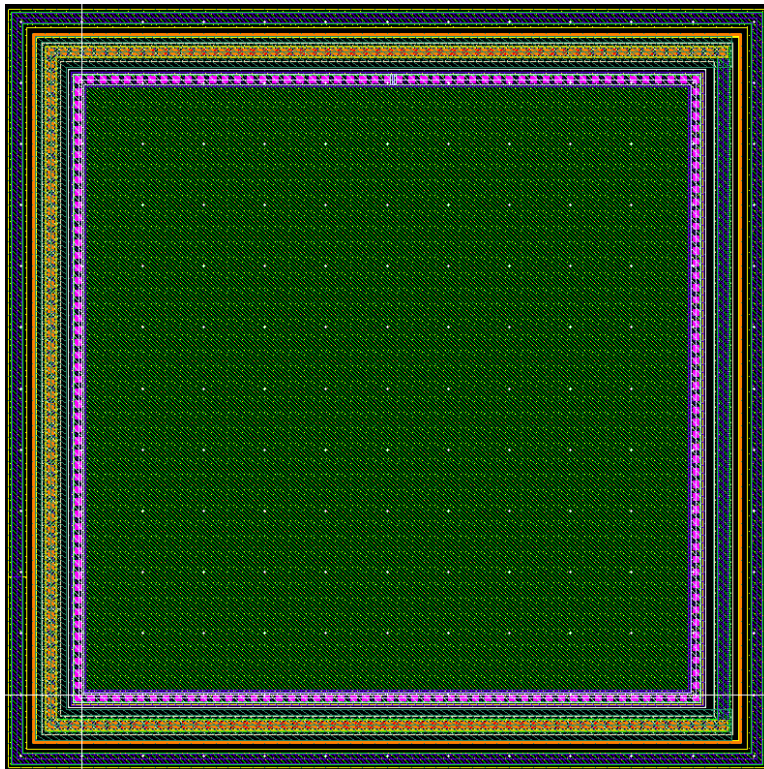
Figure A.5b.15 – 50μ BPOLY/PPLUS Smaller
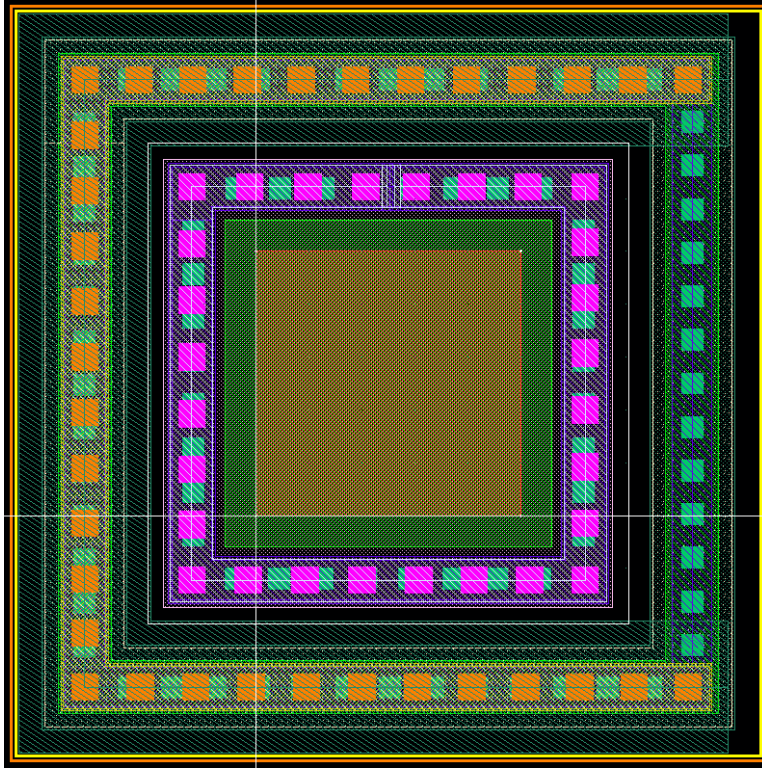
Figure A.5b.16 – 5µ No Sub
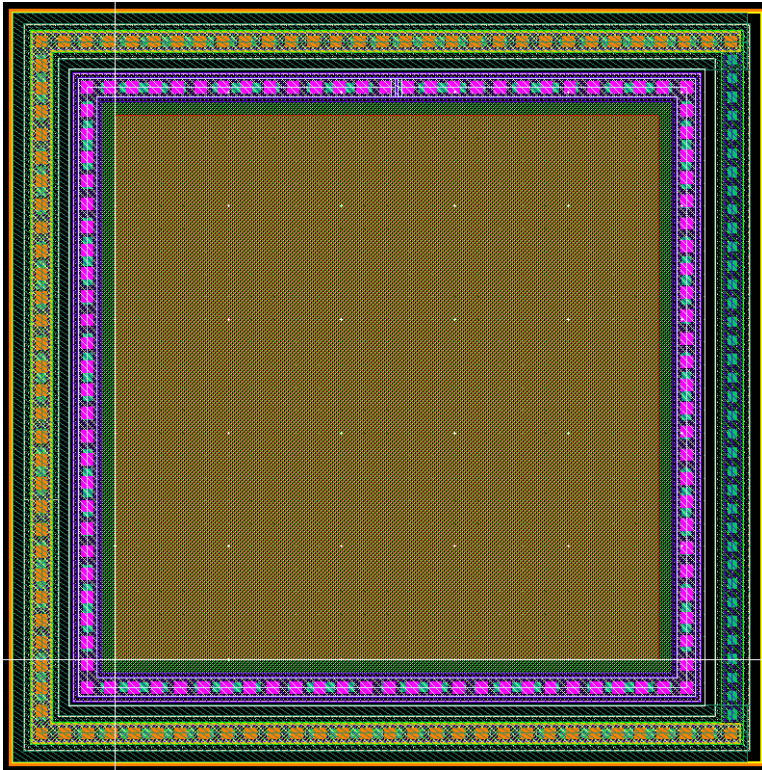
Figure A.5b.17 – 24µ No Sub
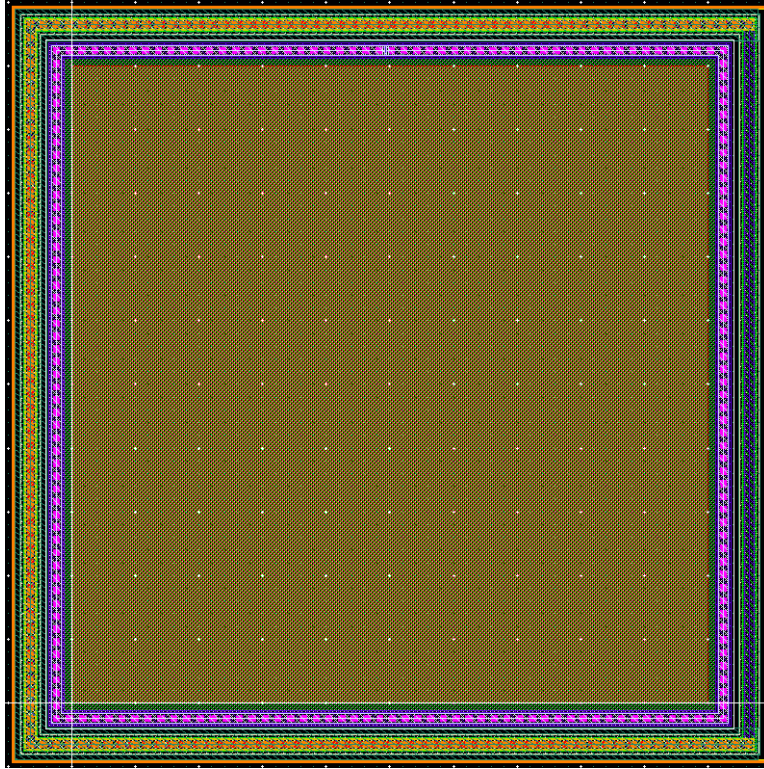
Figure A.5b.18 – 50μ No Sub
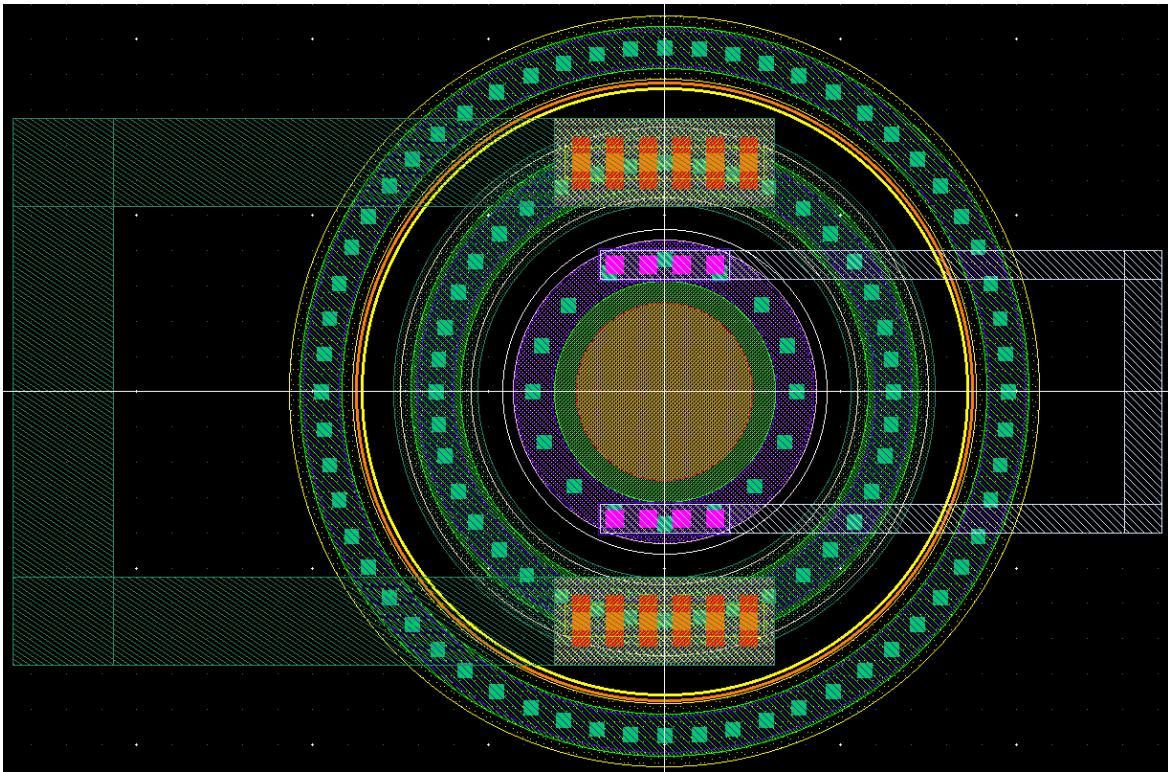
Figure A.5b.19 – 5μ Circle
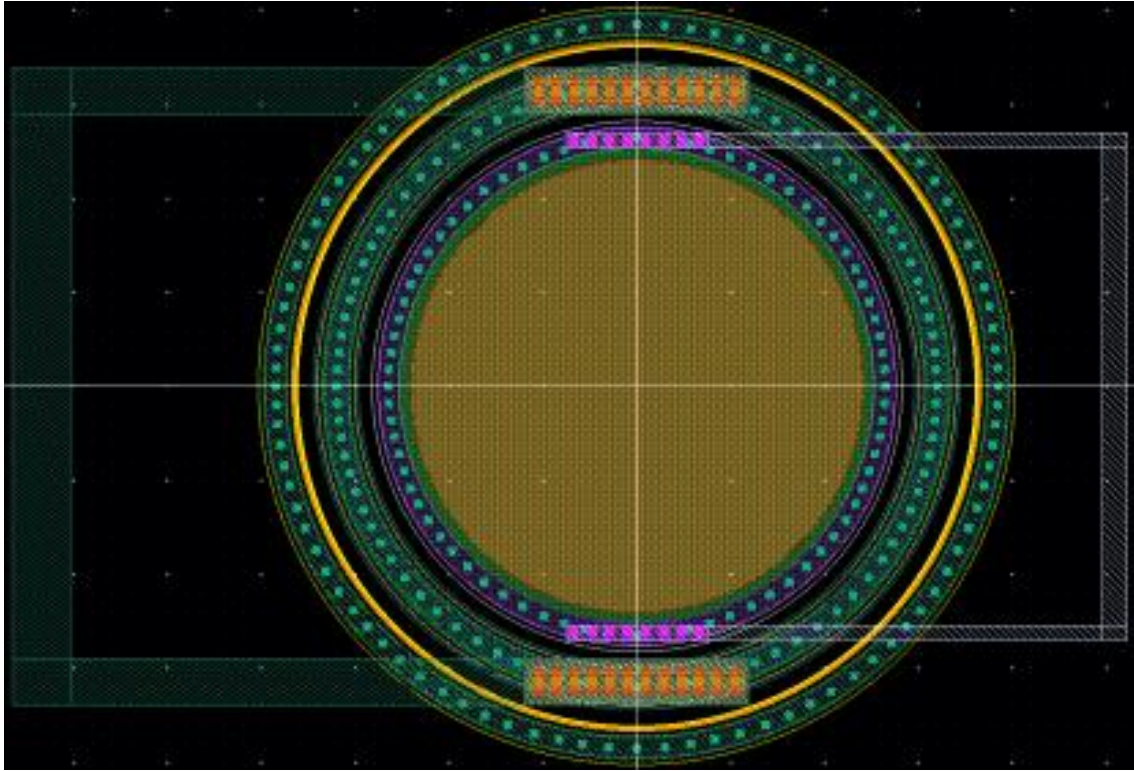
Figure A.5b.20 – 24µ Circle
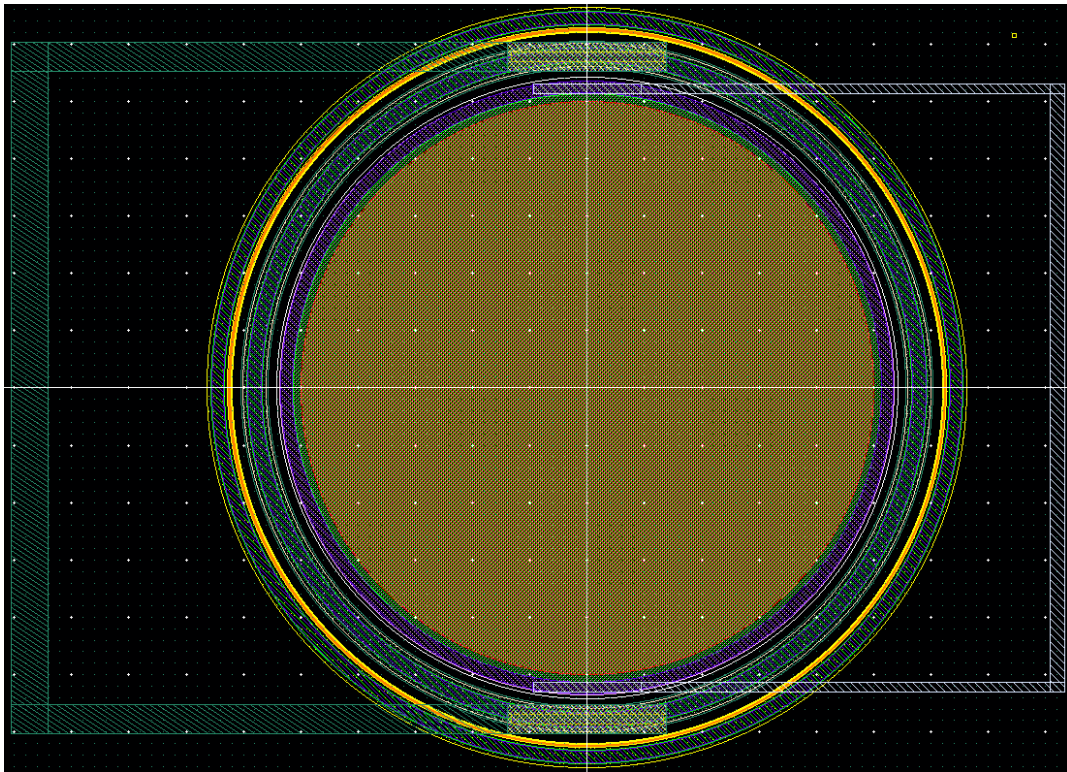
Figure A.5b.21 – 50µ Circle
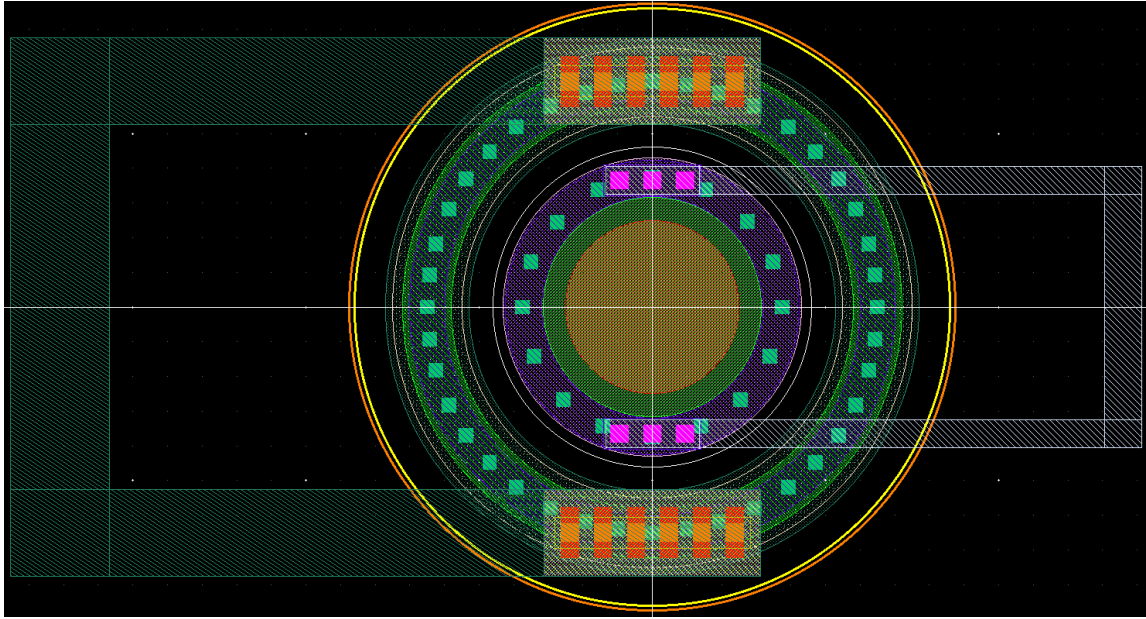
Figure A.5b.22 – 5μ Circle No Sub
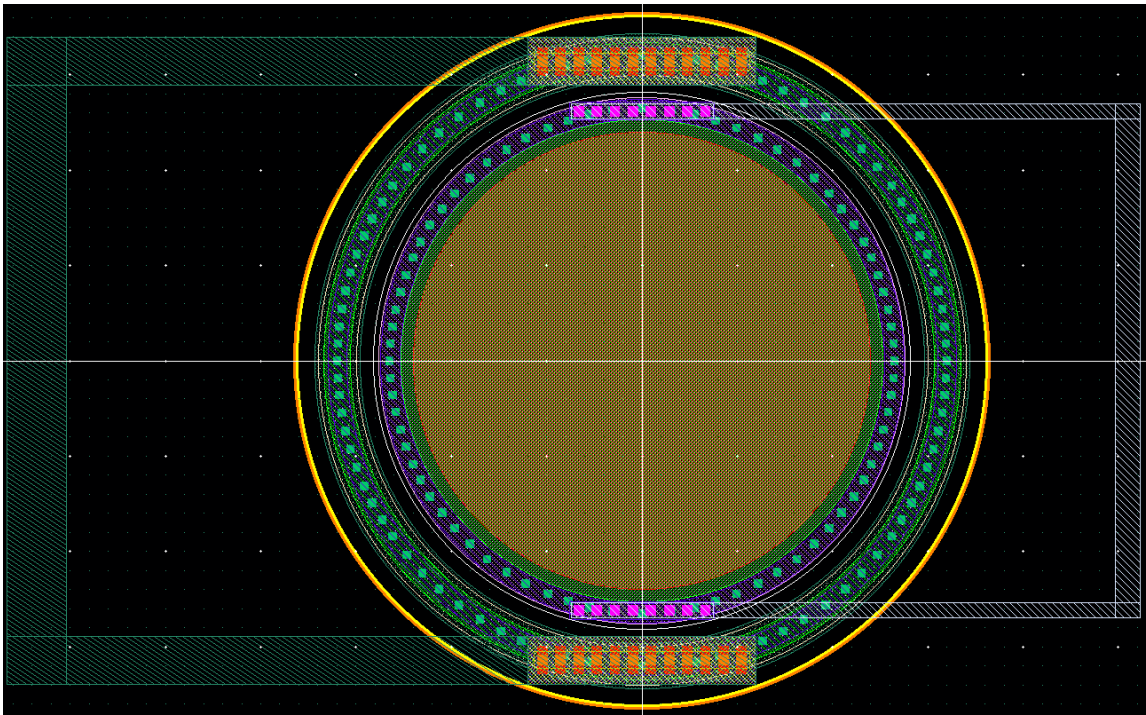
Figure A.5b.23 – 24μ Circle No Sub
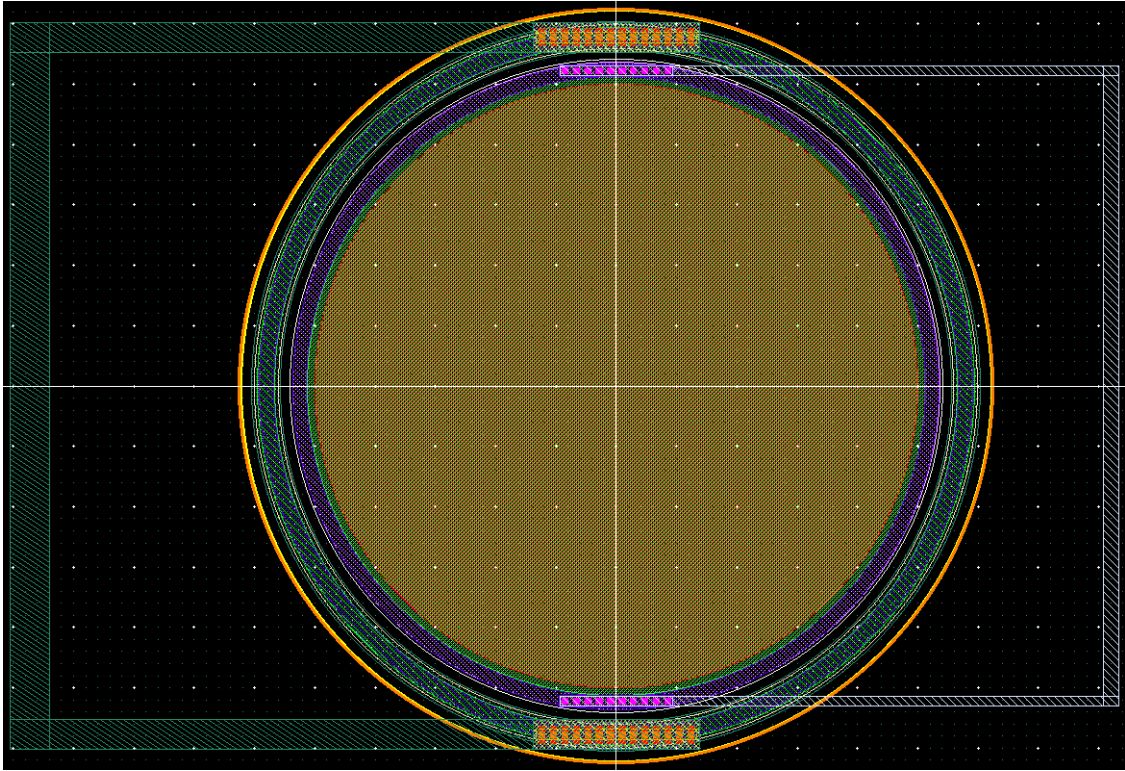
Figure A.5b.24 – 50μ Circle No Sub

Appendix 5c: Chip 2 Bond Plan and Pin Table

Chip Pin #	Pin Description	APD	Bond Plan #
1	Anode (A)		
2	Cathode (K)	5μ Elementary	5
3	Guard Ring (G)		
4	A		
5	K	24μ Elementary	8
6	G		
7	A		
8	K	50μ Elementary	6
9	G		
10	A		
11	K	5μ Standard	1
12	G		
13	A		
14	K	5μ BPOLY/PPLUS Smaller	4
15	G		
16	A		
17	K		9

18	G	5μ BPOLY/PPLUS	
19	A		
20	K	5μ No EMITT	2
21	G		
22	A	5μ No Sub	1
23	K		
24	A		
25	K	5μ Circle	6
26	G		
27	A	5μ Circle No Sub	5
28	K		
29	A		
30	K	24μ Standard	3
31	G		
32	A		
33	K	24μ BPOLY/PPLUS Smaller	8
34	G		
35	A		
36	K	24μ BPOLY/PPLUS	2
37	G		
38	A		
39	K	24μ No EMITT	1
40	G		
41	A	24μ No Sub	4
42	K		
43	A		
44	K	24μ Circle	9
45	G		
46	A	24μ Circle No Sub	2
47	K		
48	A		
49	K	50μ Standard	5
50	G		
51	A		
52	K	50μ BPOLY/PPLUS Smaller	3
53	G		
54	A		
55	K	50μ BPOLY/PPLUS	7
56	G		
57	A		
58	K	50μ No EMITT	4
59	G		
60	A	50μ No Sub	6
61	K		

62	A	50μ Circle	7
63	K		
64	G		
65	A	50μ Circle No Sub	3
66	K		

Table 5c.1 – TO-8 Package Pin Table and Bond Plans 1 through 9 for Chip 2

Appendix 5d: Chip 2 TO-8 Bonding Diagrams
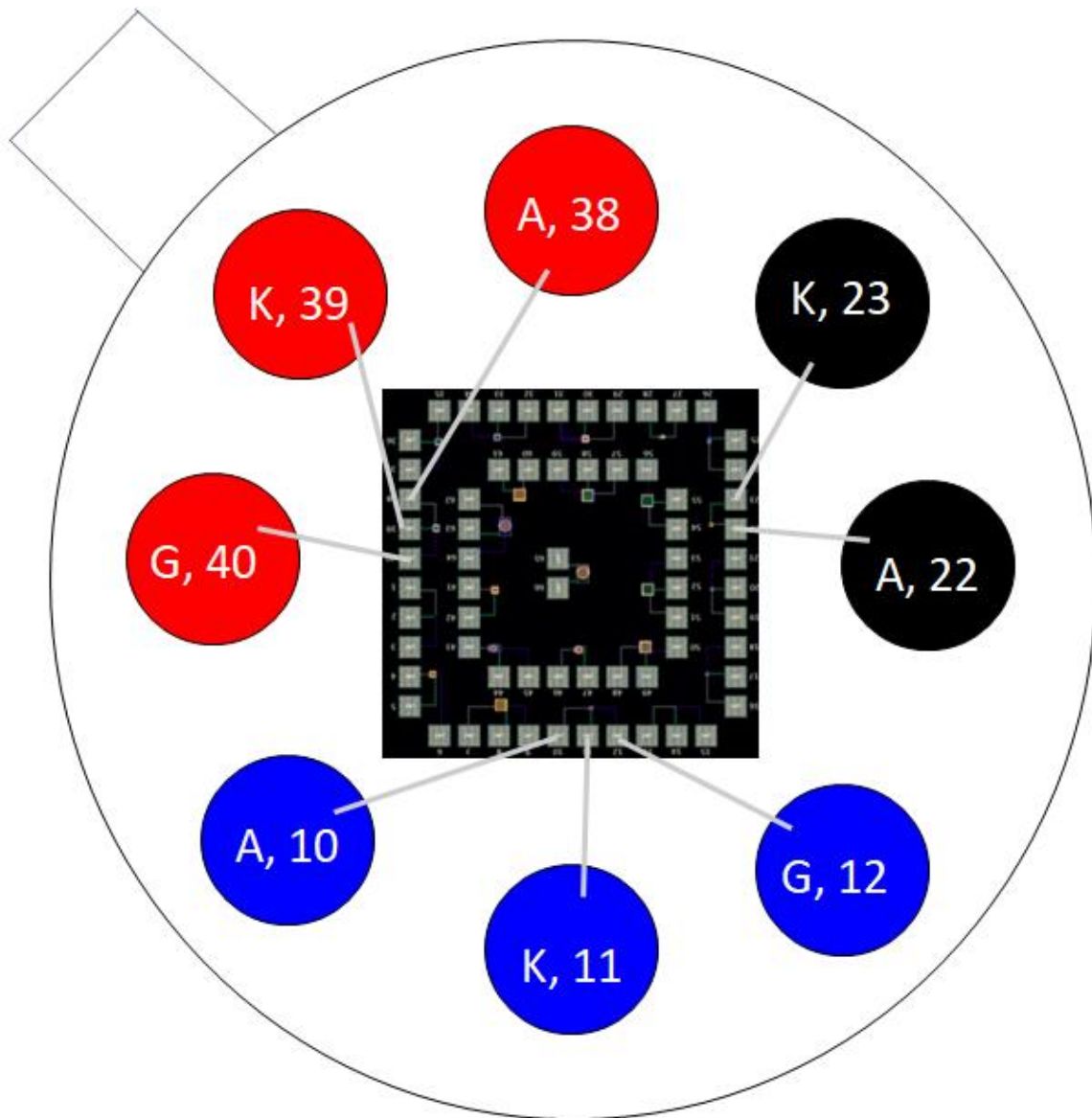
Figure A.5d.1 – Version 1
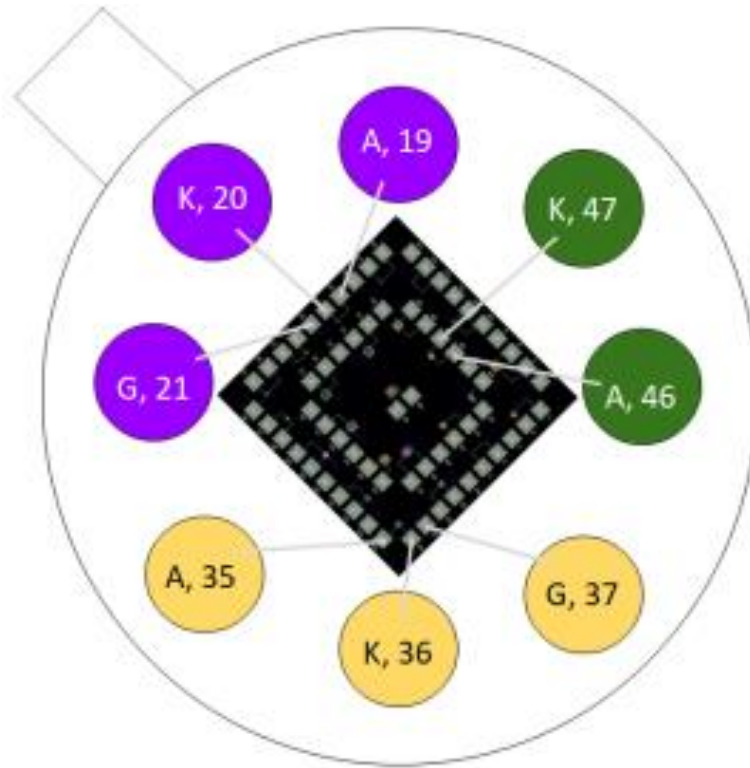
Figure A.5d.2 – Version 2
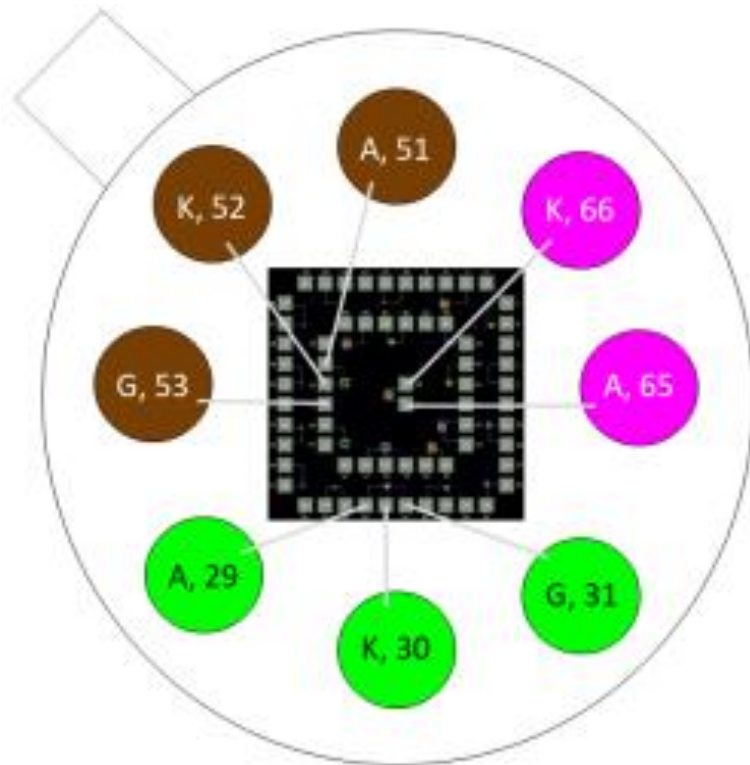
Figure A.5d.3 – Version 3
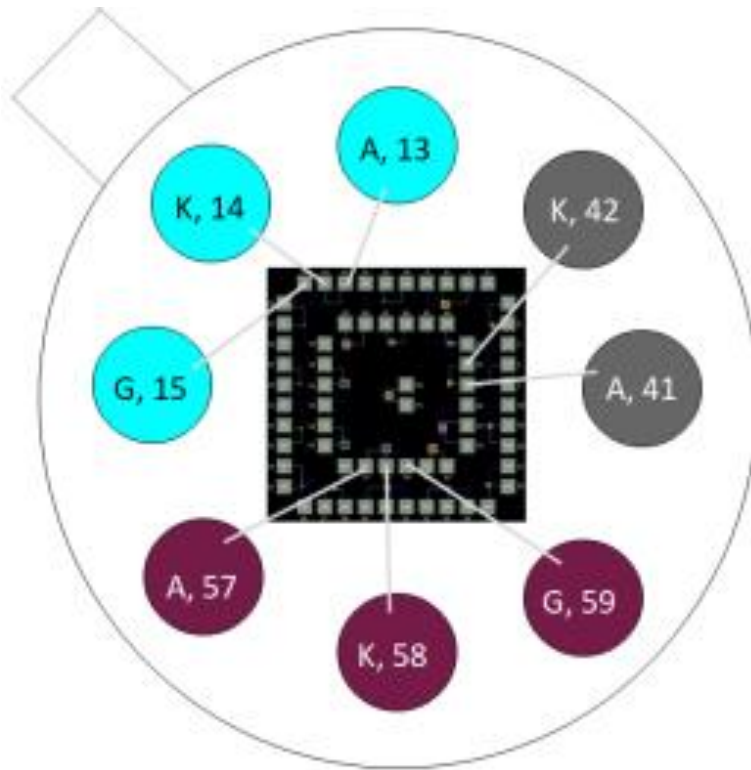
Figure A.5d.4 – Version 4
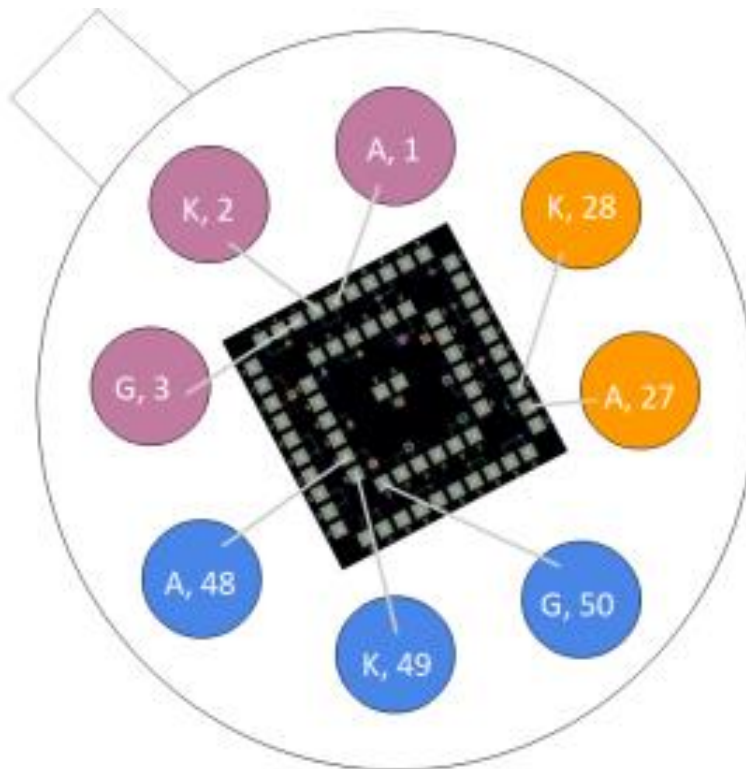
Figure A.5d.5 – Version 5
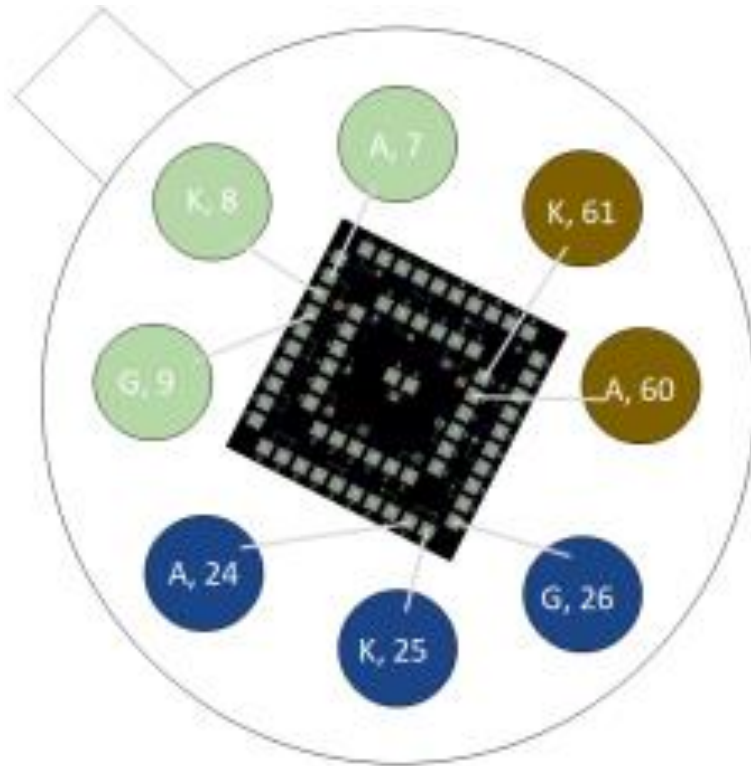
Figure A.5d.6 – Version 6
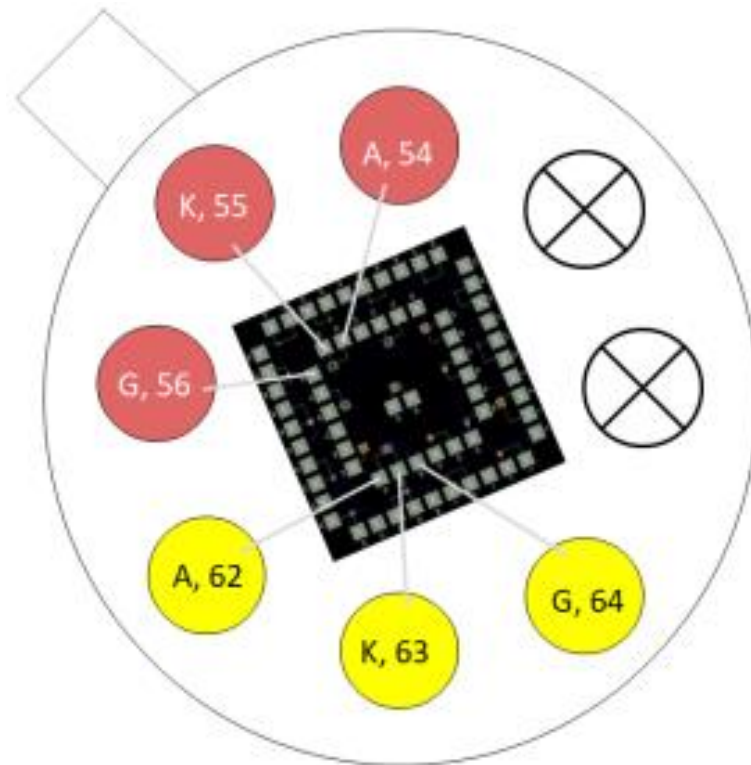
Figure A.5d.7 – Version 7
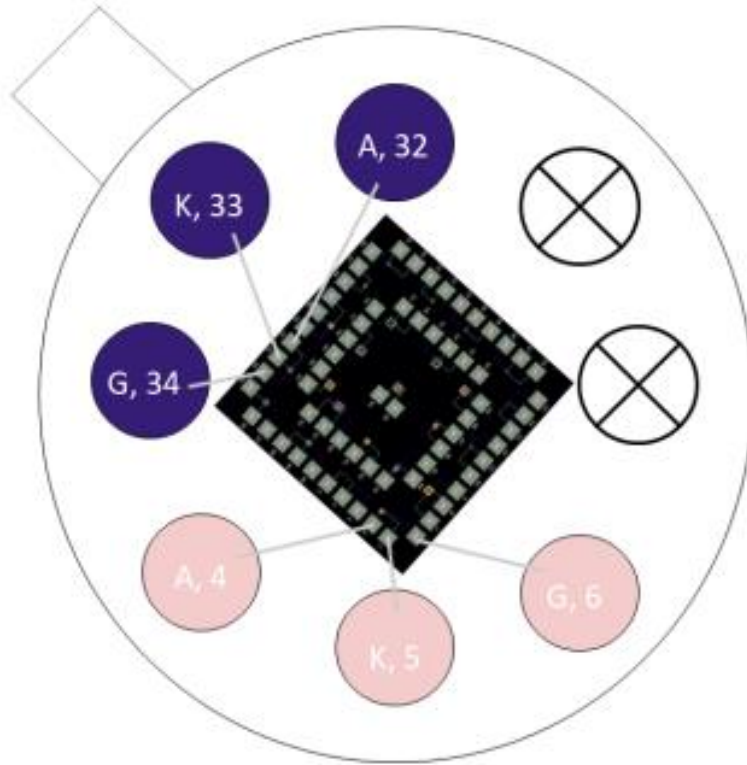
Figure A.5d.8 – Version 8
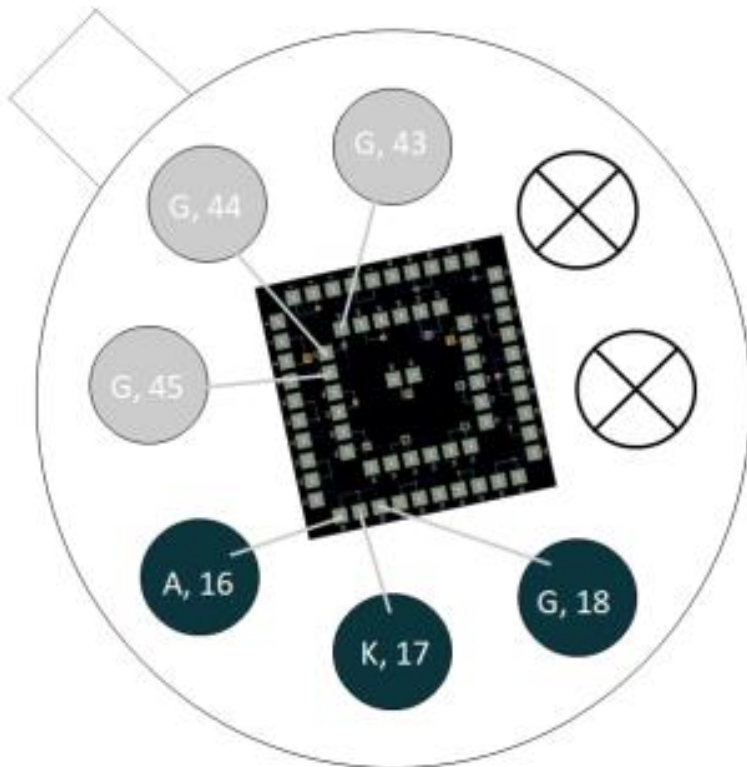
Figure A.5d.9 – Version 9

Appendix 5e: Chip 3 APD Layouts
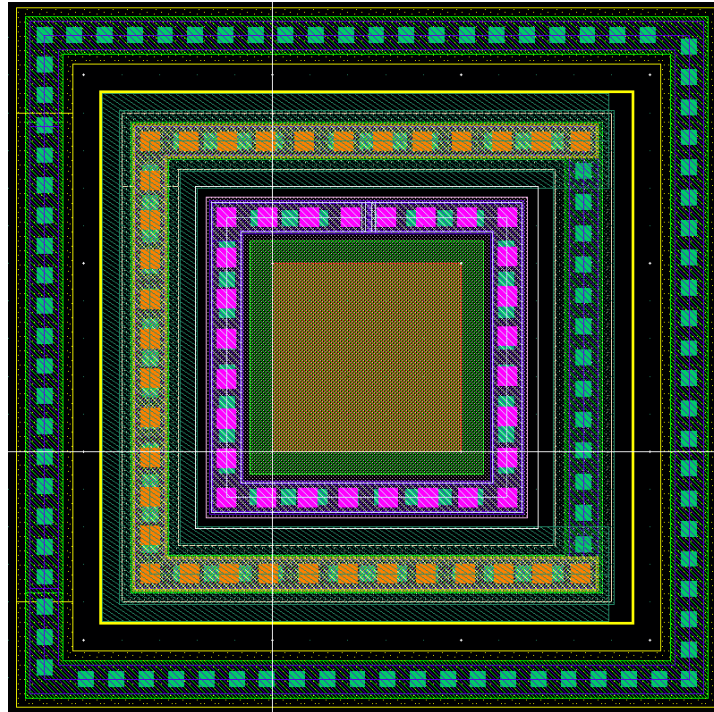
Figure A.5e.1 – 5µ noBNTUB2
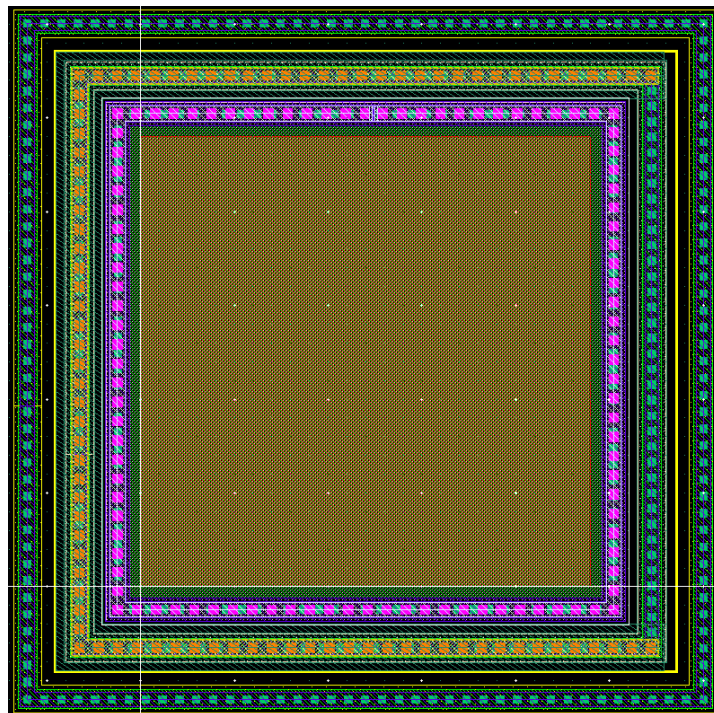
Figure A.5e.2 – 24µ noBNTUB2
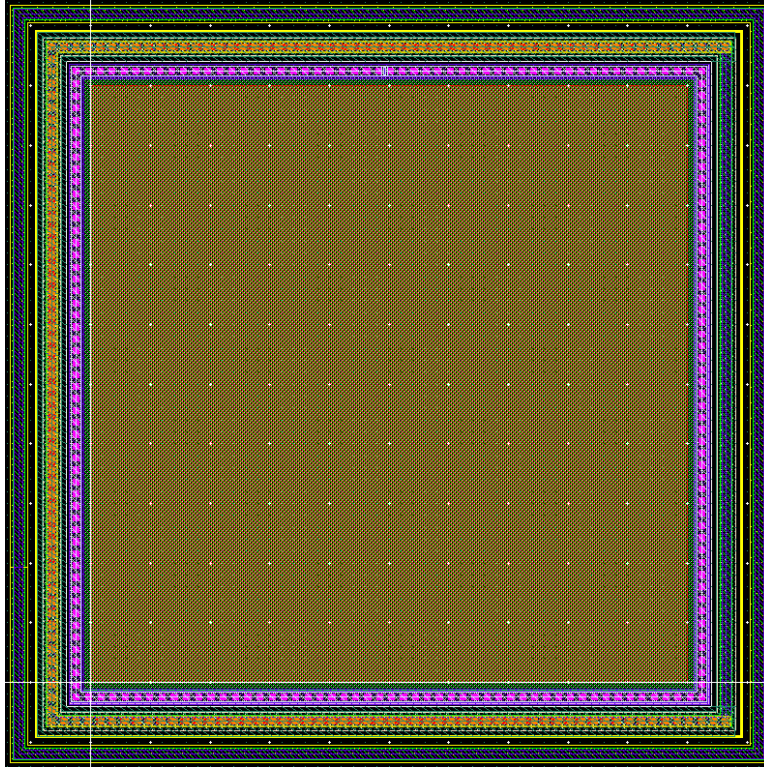
Figure A.5e.3 – 50μ noBNTUB2
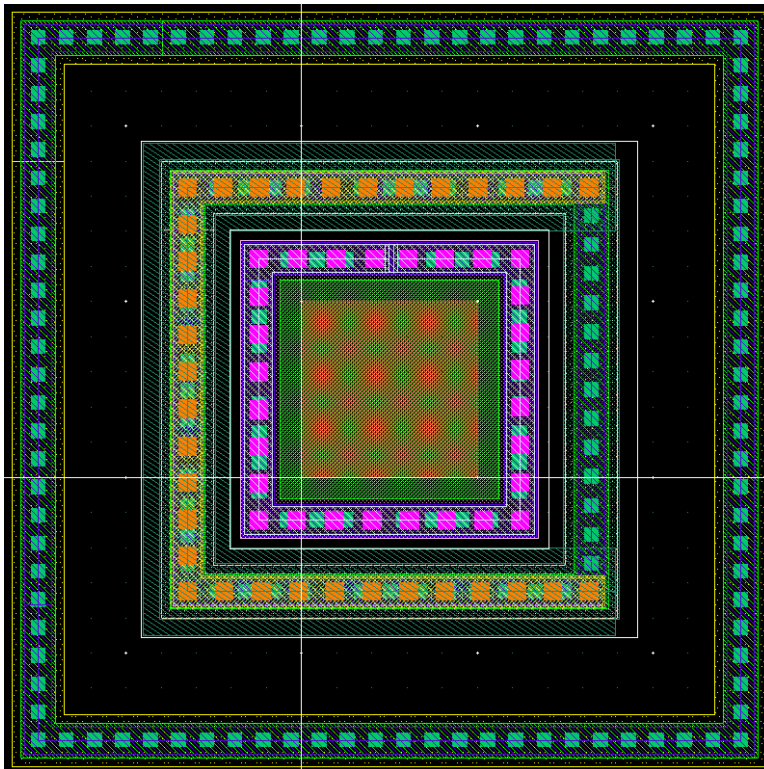
Figure A.5e.4 – 5μ TUBBUR
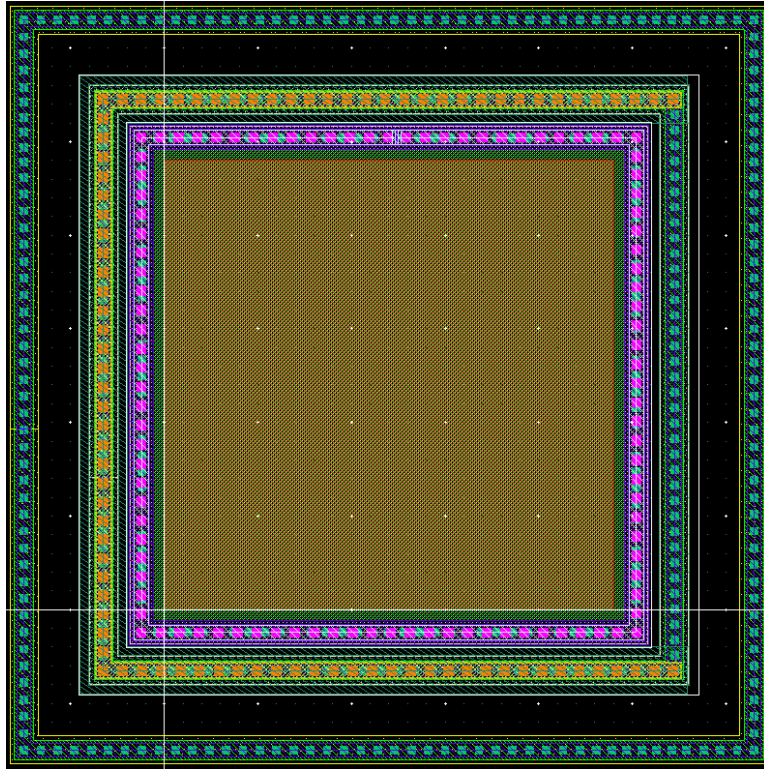
Figure A.5e.5 – 24μ TUBBUR
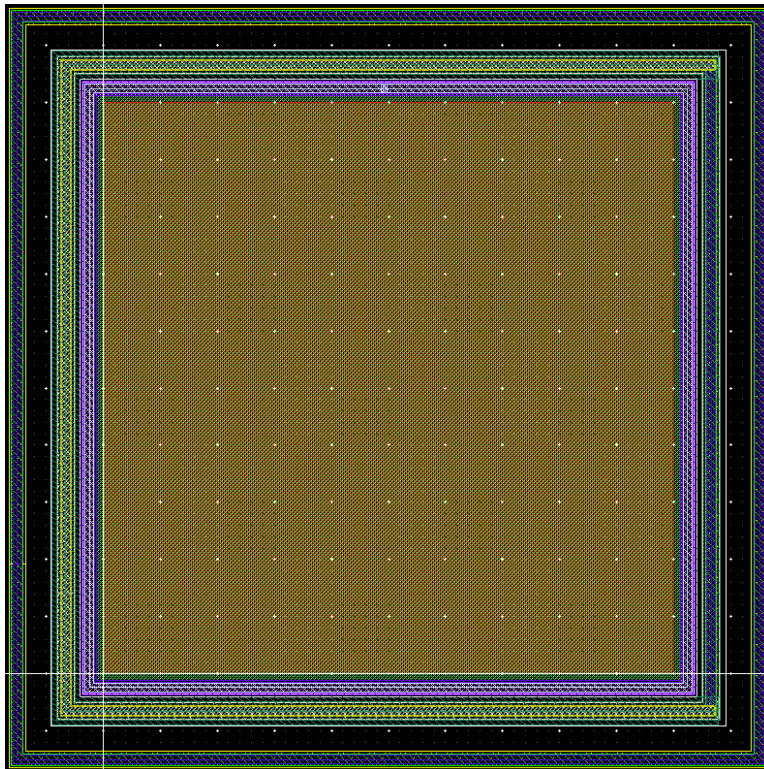
Figure A.5e.6 – 50μ TUBBUR
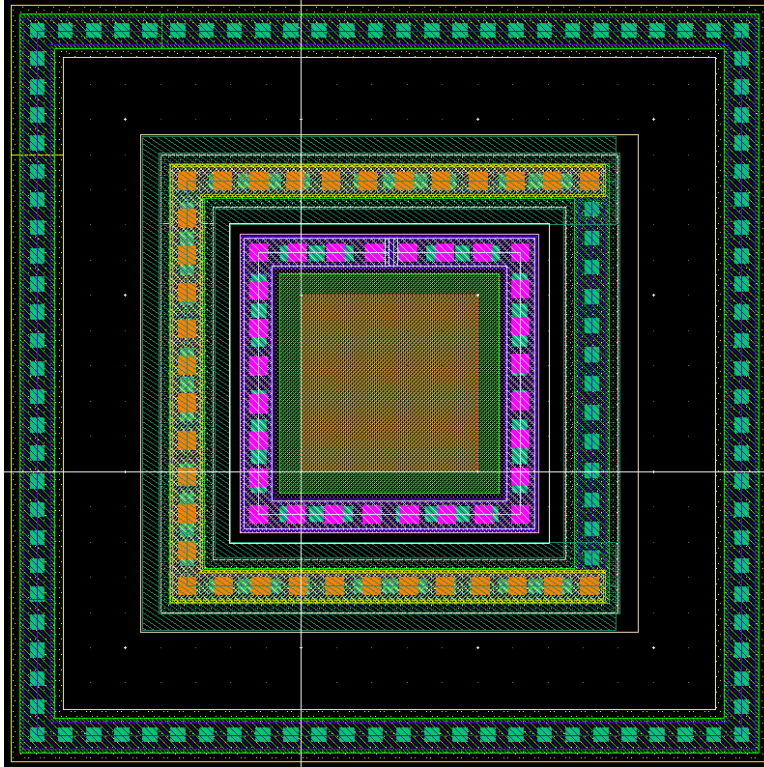
Figure A.5e.7 – 5μ TUB
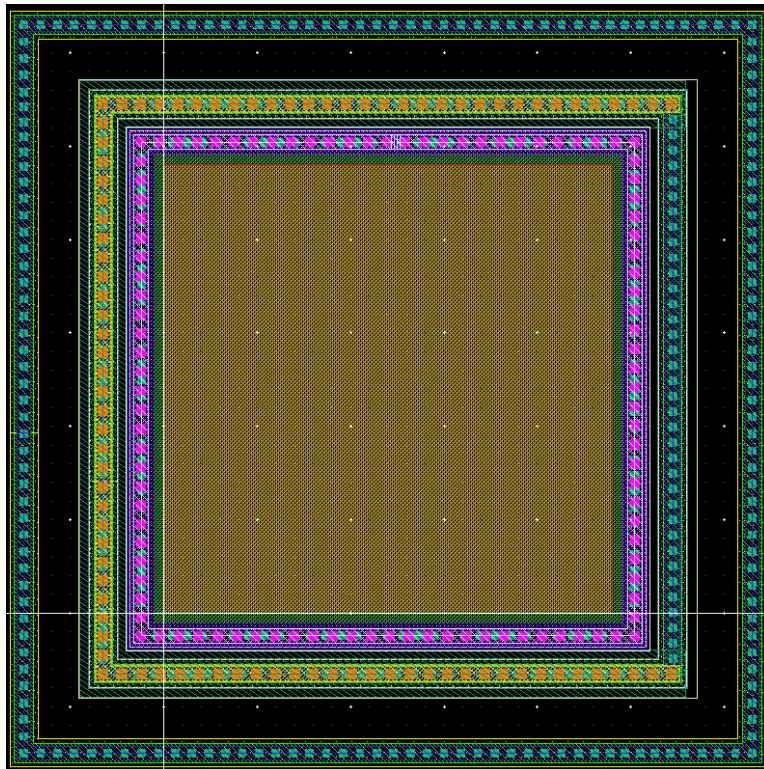
Figure A.5e.8 – 24μ TUB
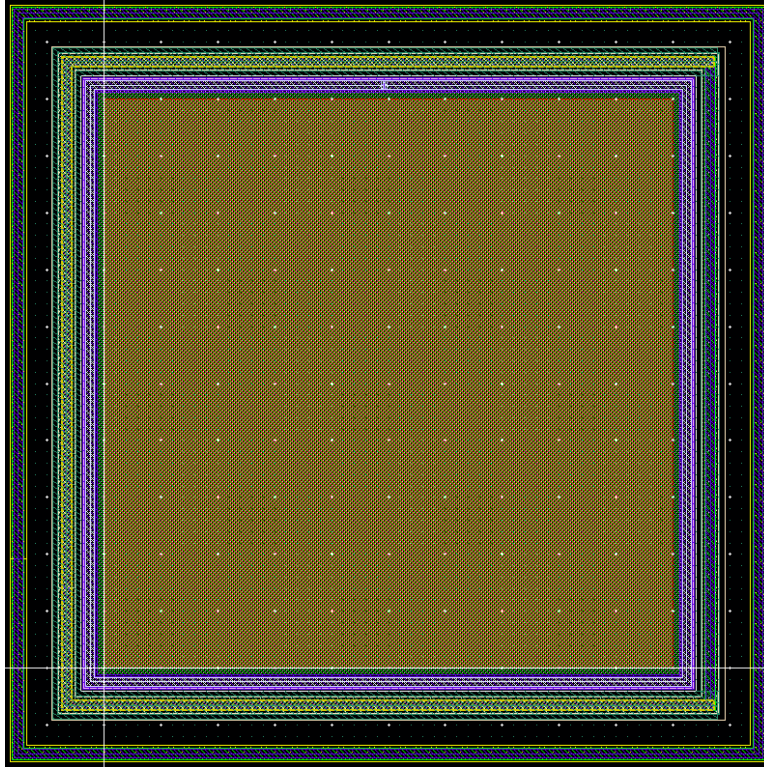
Figure A.5e.9 – 50μ TUB
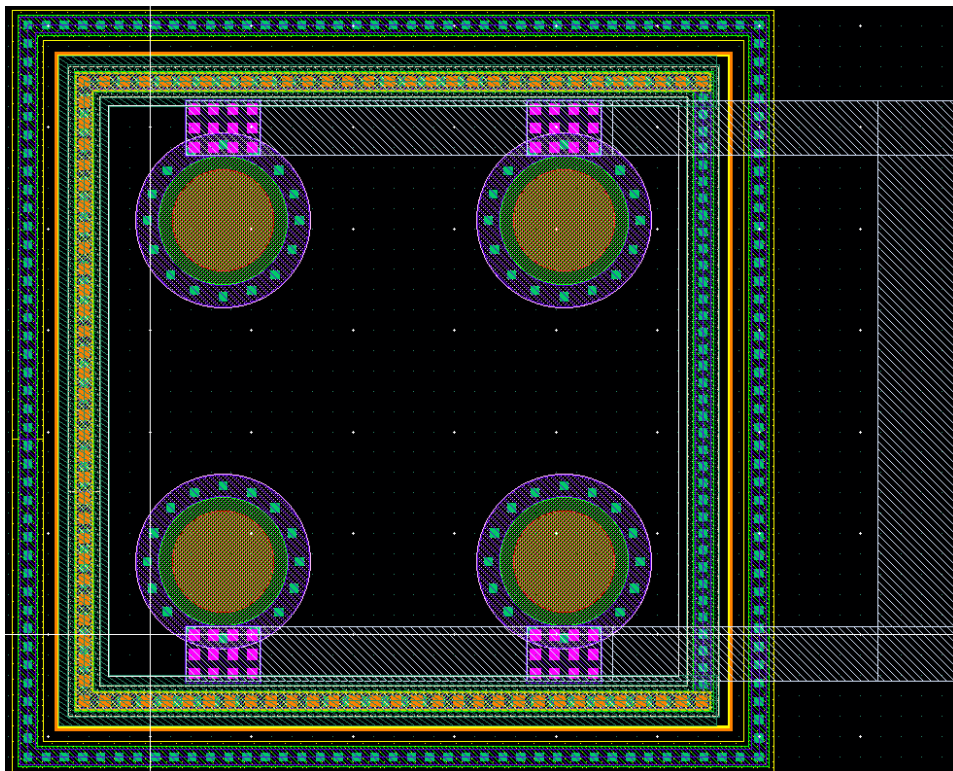
Figure A.5e.10 – 24μ Cyl
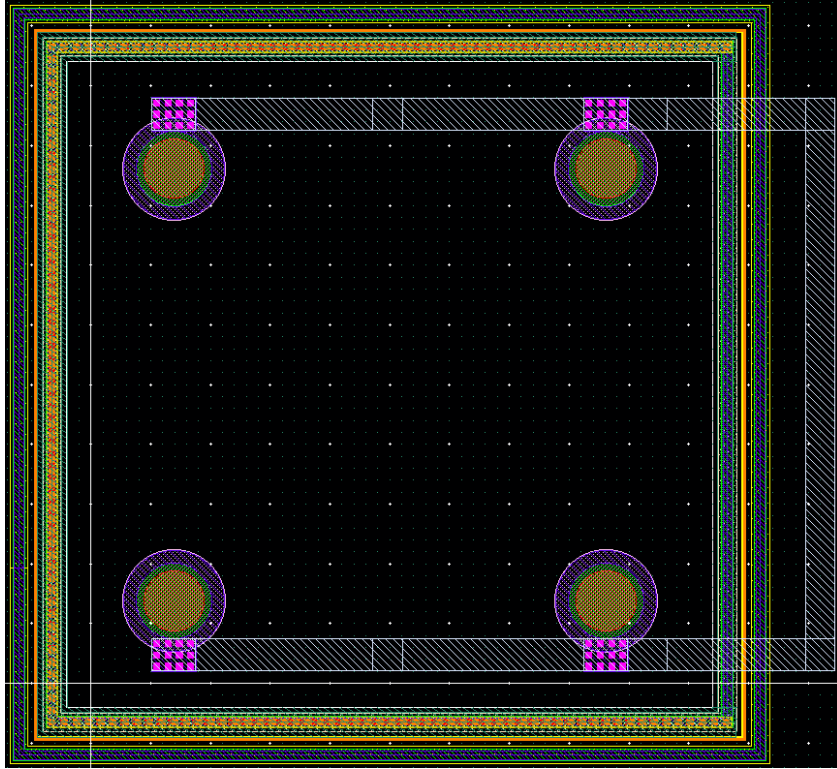
Figure A.5e.11 – 50µ Cyl
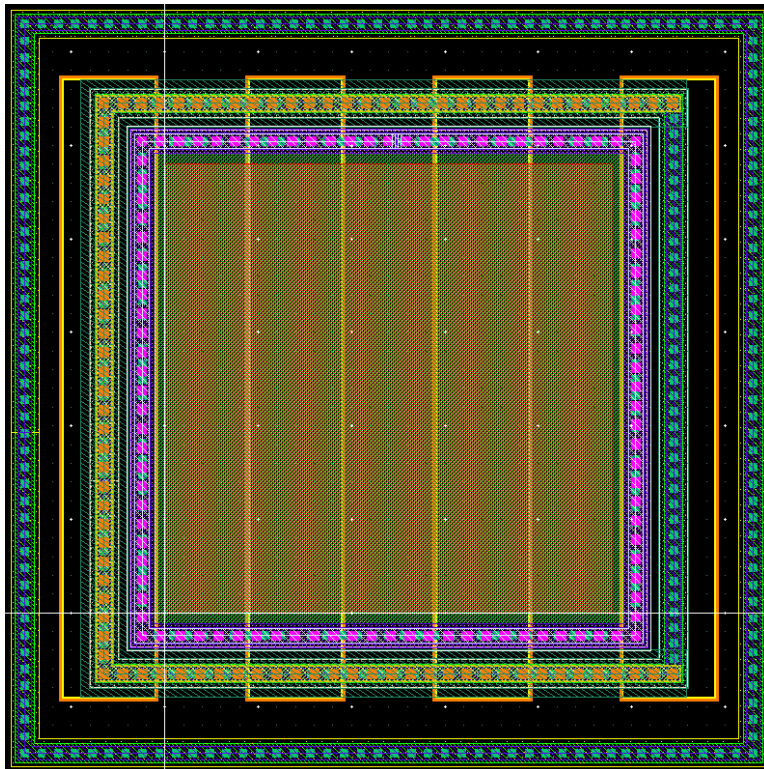
Figure A.5e.12 – 24µ Striped BNTUB2
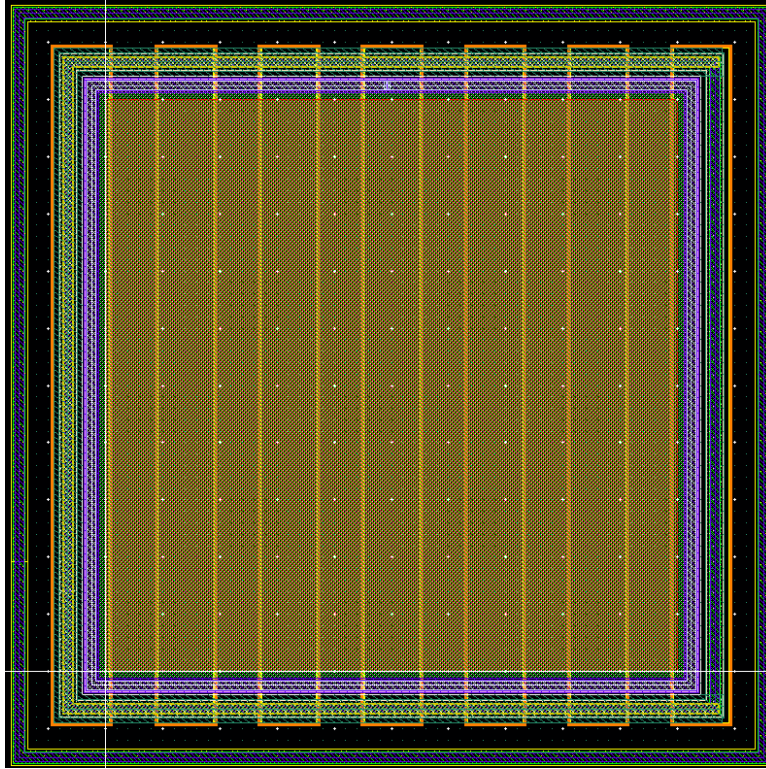
Figure A.5e.13 – 50µ Striped BNTUB2
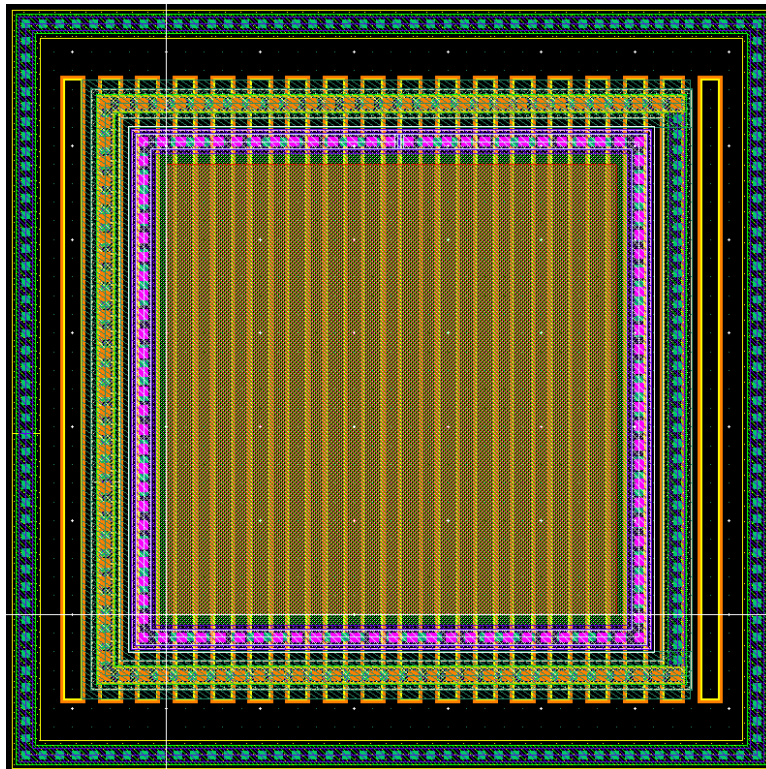
Figure A.5e.14 – 24µ Striped Half BNTUB2

111
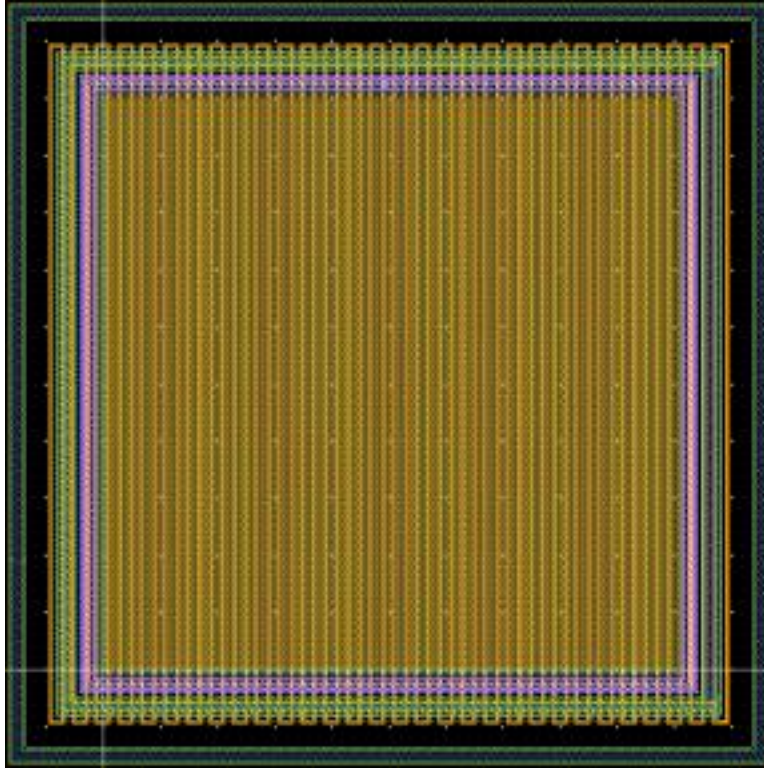
Figure A.5e.15 – 50μ Striped Half BNTUB2

Figure A.5e.16 – 24μ Striped TUBBUR

112
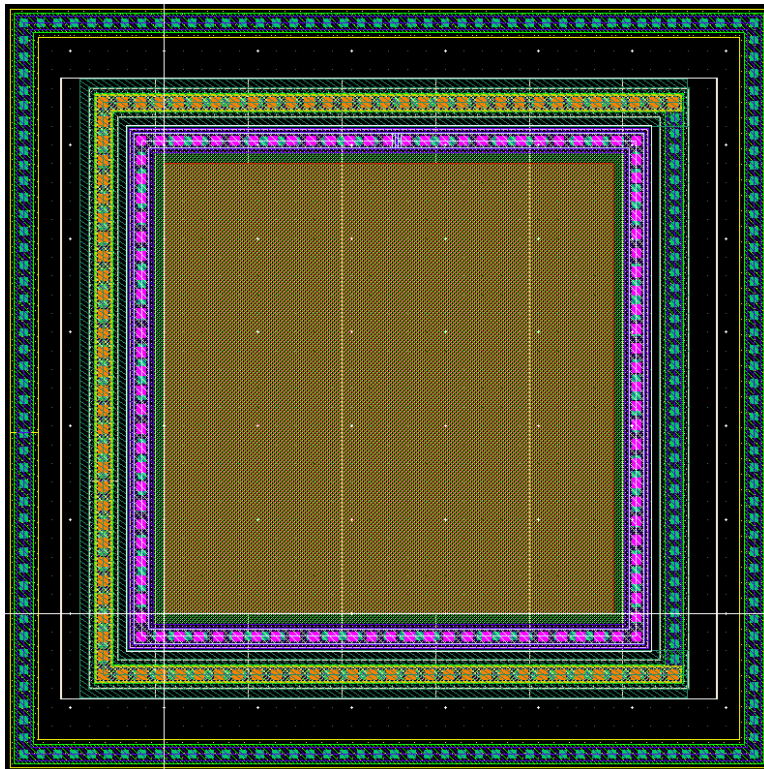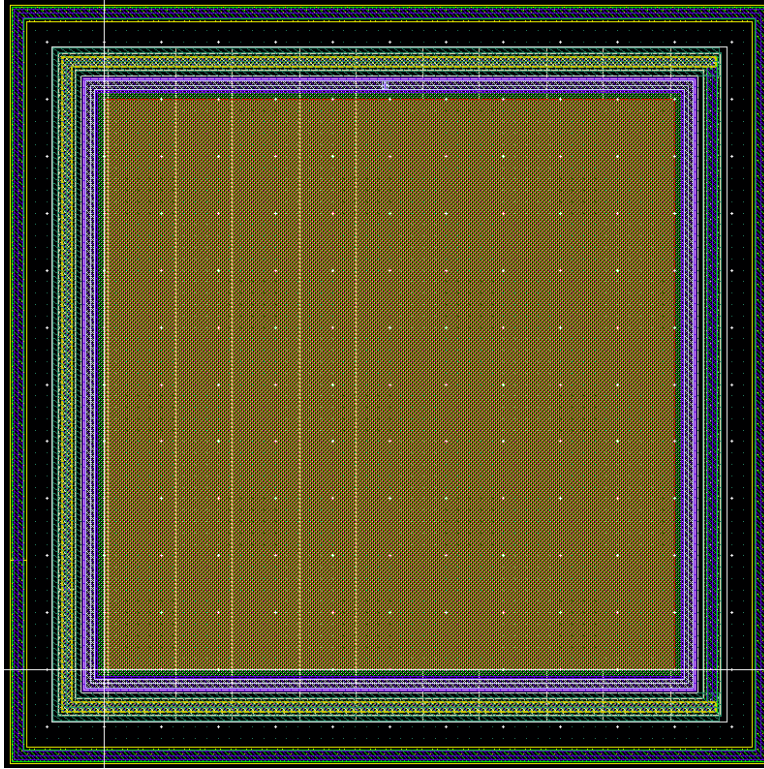
Figure A.5e.17 – 50µ Striped TUBBUR
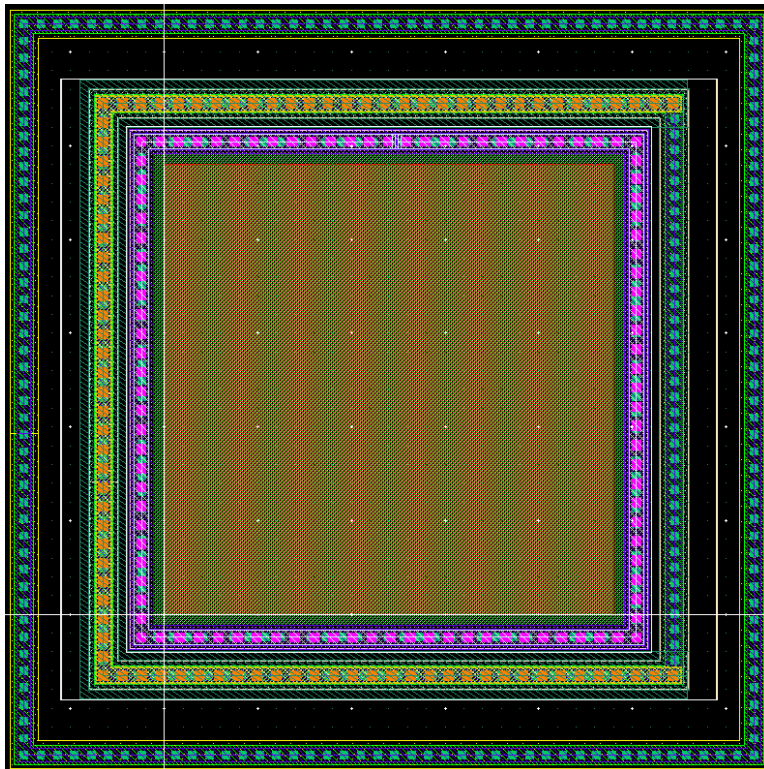
Figure A.5e.18 – 24µ Striped BUR hTUB
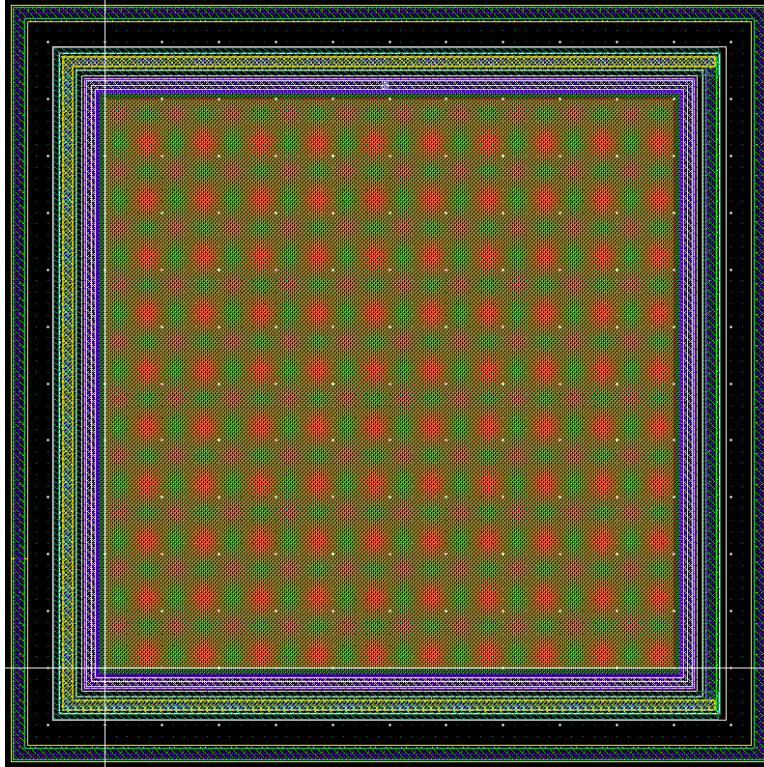
Figure A.5e.19 – 50μ Striped BUR hTUB

Figure A.5e.20 – 24μ Striped BUR Half TUB

114
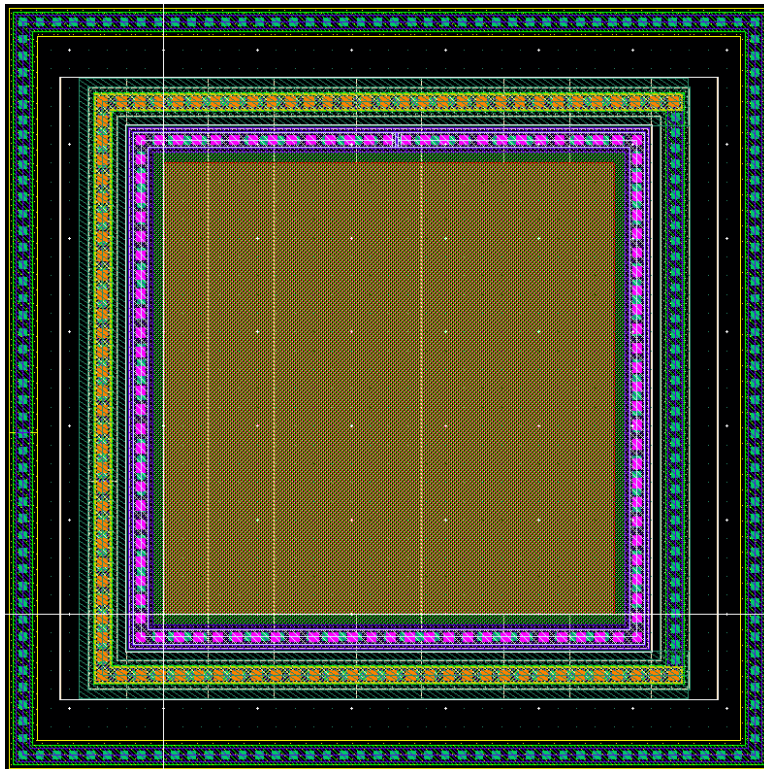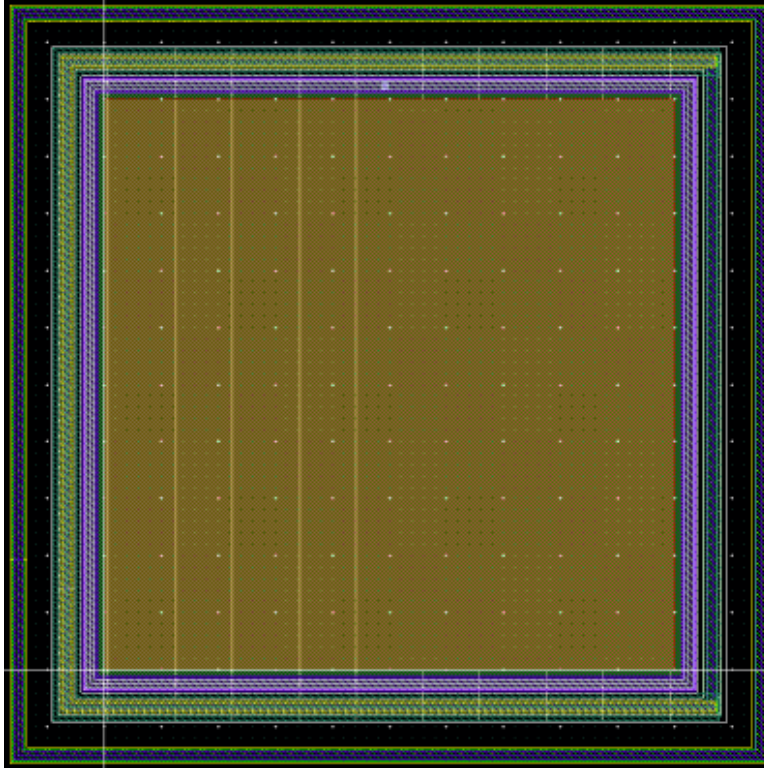
Figure A.5e.21 – 50μ Striped BUR Half TUB
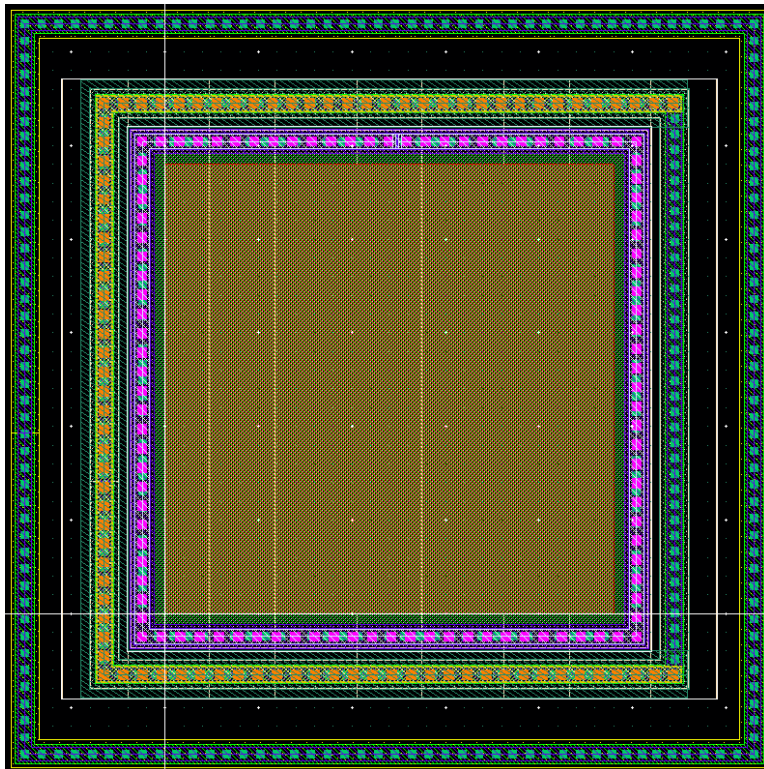
Figure A.5e.22 – 24μ Striped Half TUB hBUR

Appendix 5f: Chip 3 Bond Plan and Pin Table

Chip Pin #	Pin Description	APD	Bond Plan #
1	Anode (A)	5µ TUBBUR	3
2	Cathode (K)		
3	Guard Ring (G)		
4	A	5µ TUB	4
5	K		
6	G		
7	A	5µ noBNTUB2	5
8	K		
9	G		
10	A	24µ Cyl	2
11	K		
12	G		
13	A	24µ TUBBUR	1
14	K		
15	G		
16	A	24µ TUB	3
17	K		
18	G		
19	A	24µ noBNTUB2	4
20	K		
21	G		
22	A	24µ Striped BNTUB2	6
23	K		
24	G		
25	A	24µ Striped BUR hTUB	2
26	K		
27	G		
28	A	24µ Striped BUR Half TUB	1
29	K		
30	G		
31	A	24µ Striped TUBBUR	11
32	K		
33	G		
34	A	24µ Striped Half BNTUB2	9
35	K		
36	G		
37	A	24µ Striped Half TUB hBUR	7
38	K		
39	G		
40			

41	A		
42	K	50μ Cyl	11
43	G		
44	A		
45	K	50μ TUBBUR	8
46	G		
47	A		
48	K	50μ TUB	7
49	G		
50	A		
51	K	50μ noBNTUB2	9
52	G		
53	A		
54	K	50μ Striped BNTUB2	10
55	G		
56	A		
57	K	50μ Striped BUR hTUB	5
58	G		
59	A		
60	K	50μ Striped BUR Half TUB	8
61	G		
62	A		
63	K	50μ Striped TUBBUR	6
64	G		
65	A		
66	K	50μ Striped Half BNTUB2	10
67	G		

Table 5f.1 – TO-8 Package Pin Table and Bond Plans 1 through 11 for Chip 3

Appendix 5g: Chip 3 TO-8 Bonding Diagrams
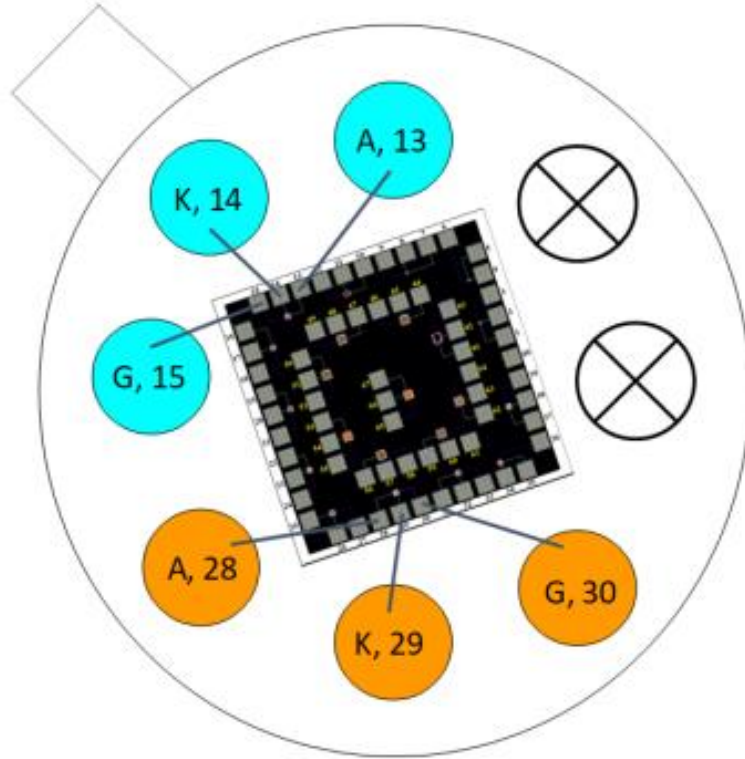
Figure A.5g.1 – Version 1
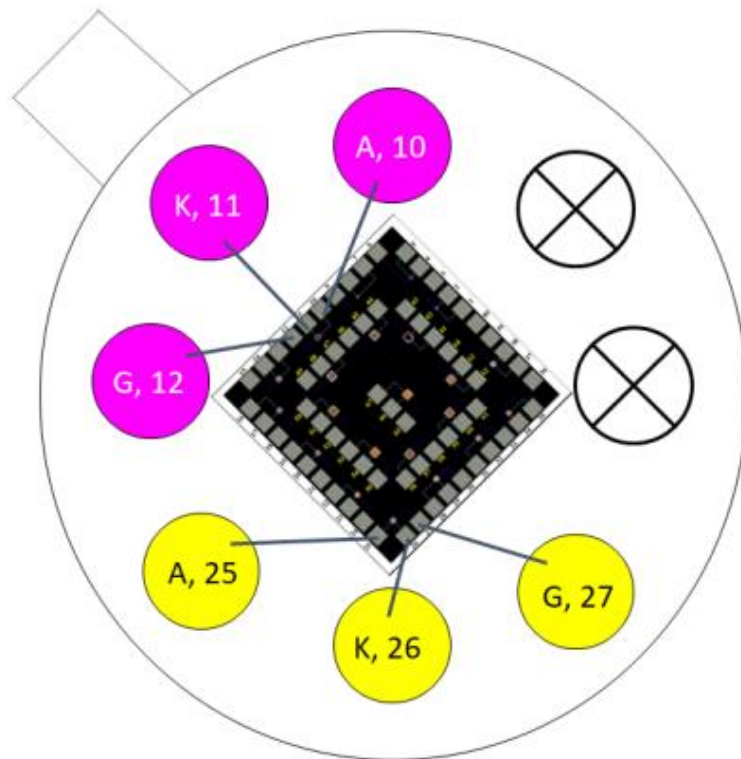
Figure A.5g.2 – Version 2
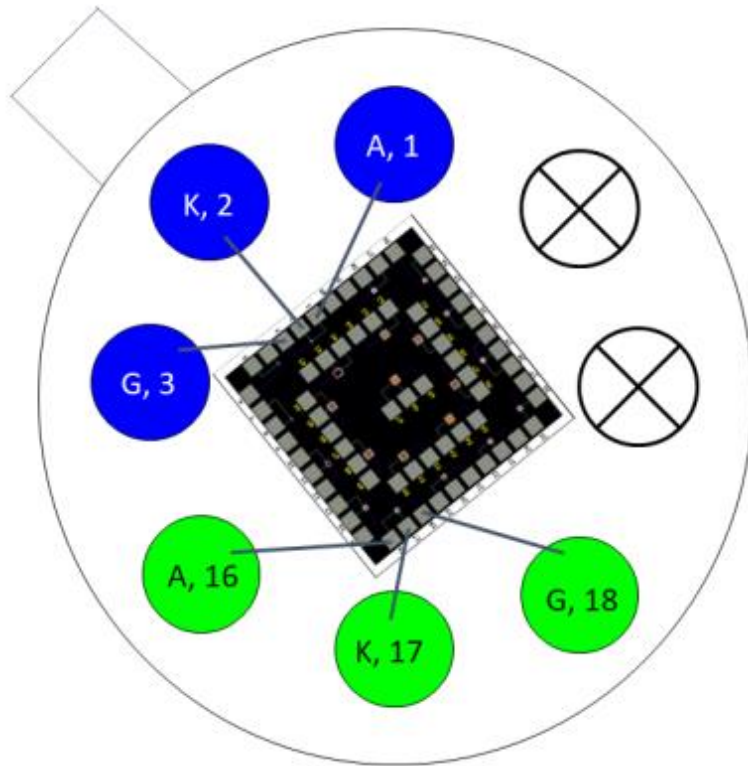
Figure A.5g.3 – Version 3
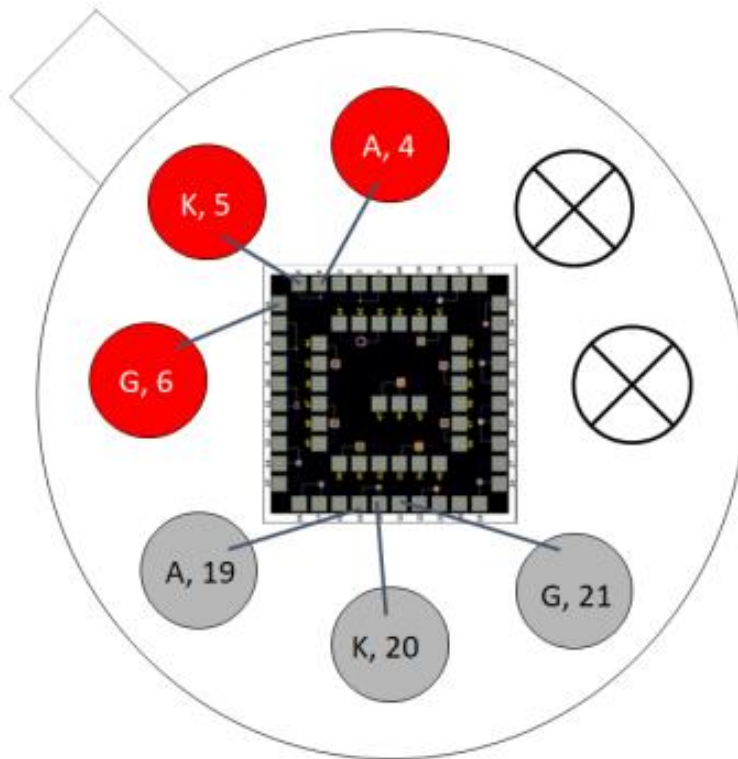
Figure A.5g.4 – Version 4
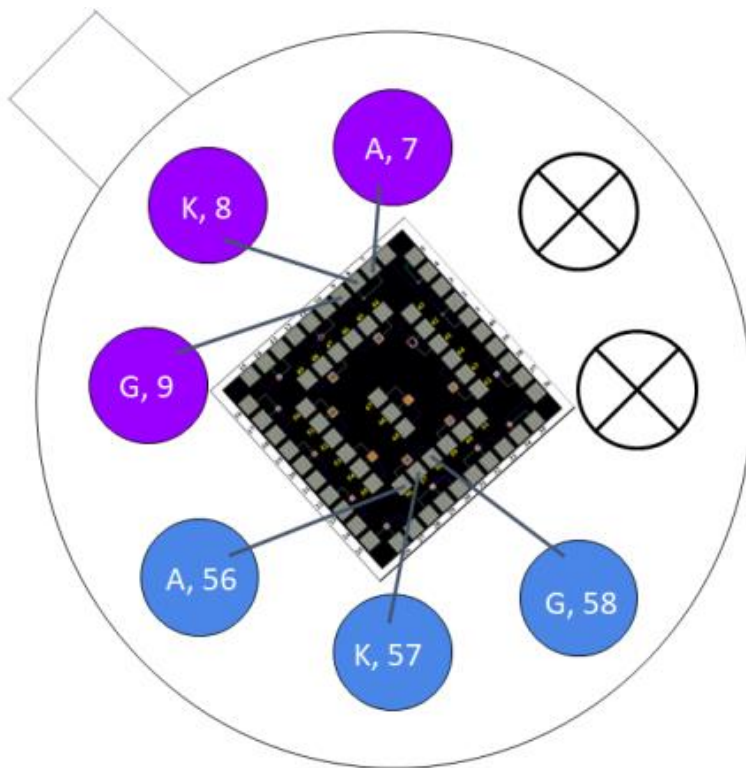
Figure A.5g.5 – Version 5
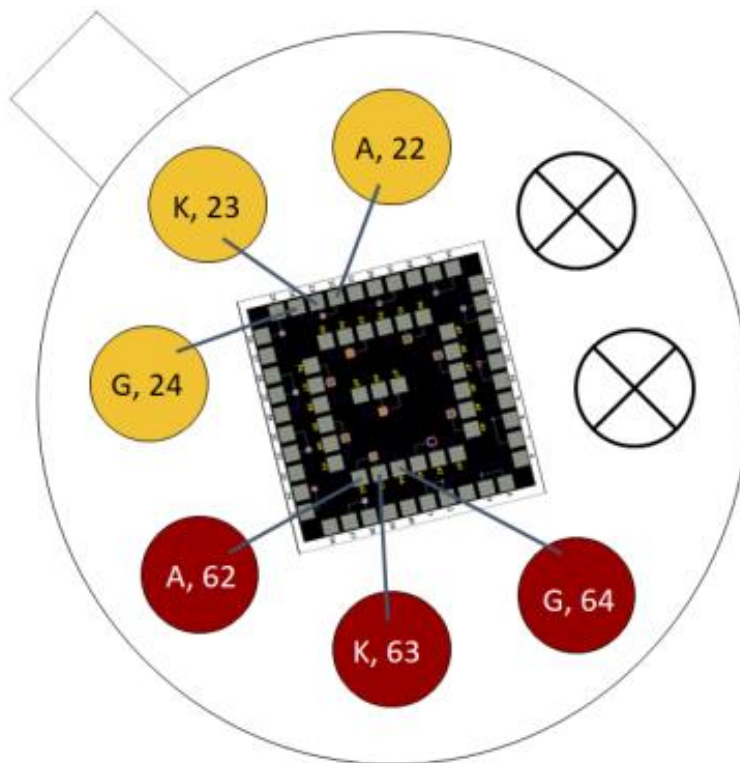
Figure A.5g.6 – Version 6
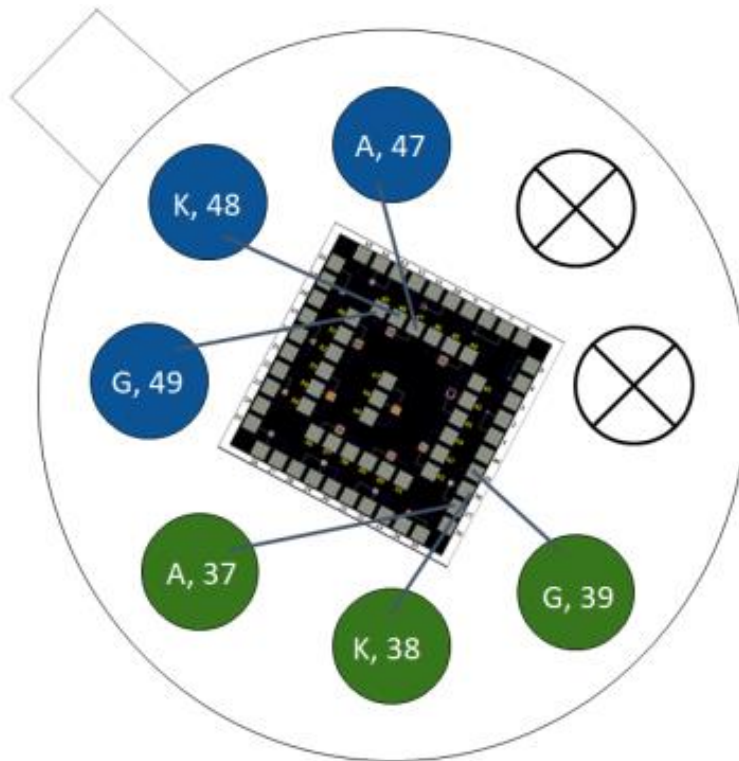
Figure A.5g.7 – Version 7
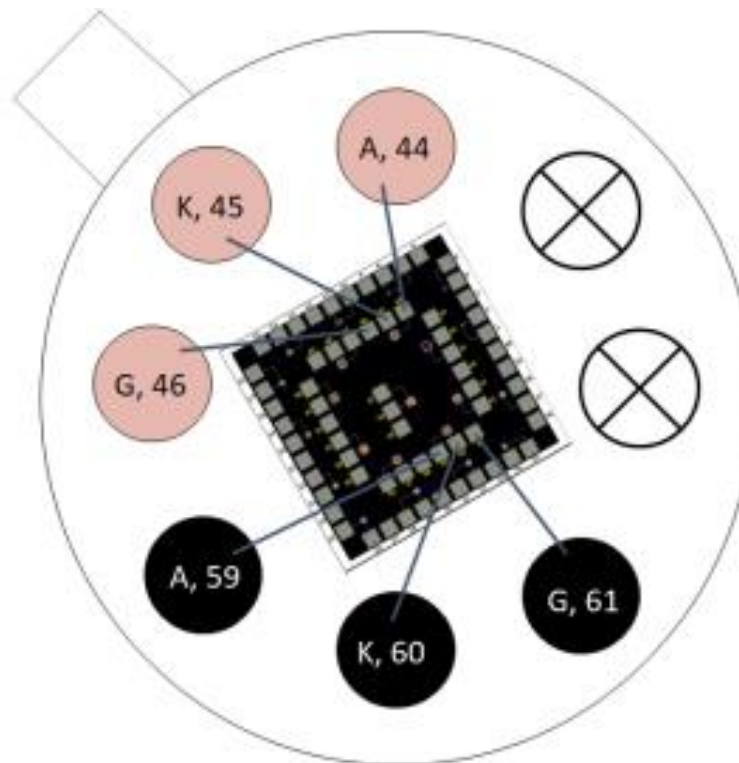
Figure A.5g.8 – Version 8
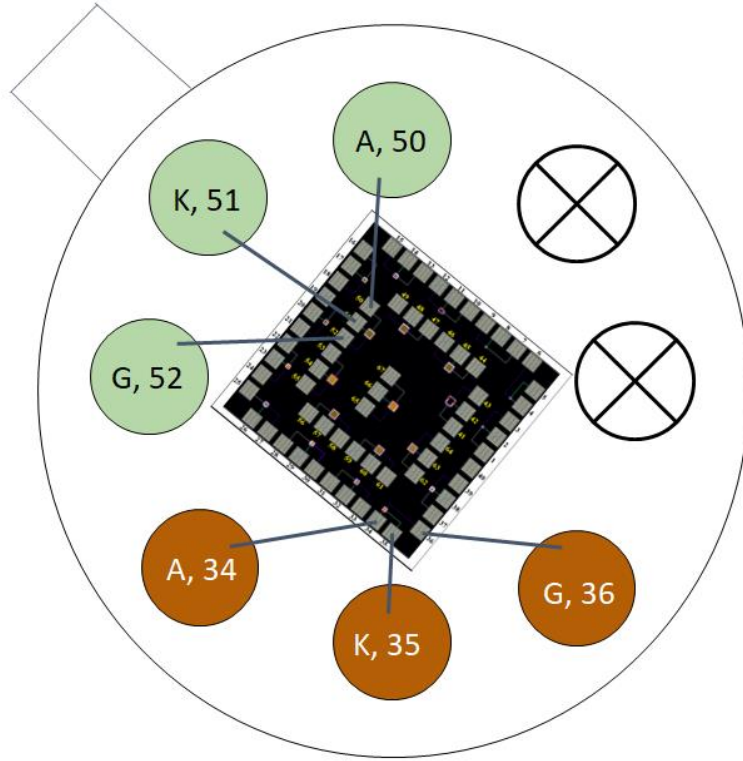
Figure A.5g.9 – Version 9
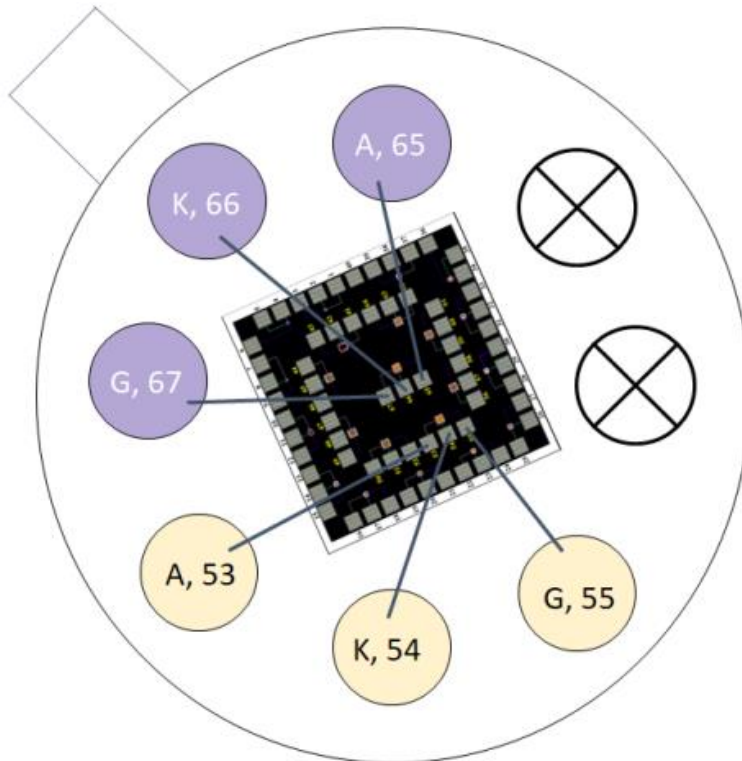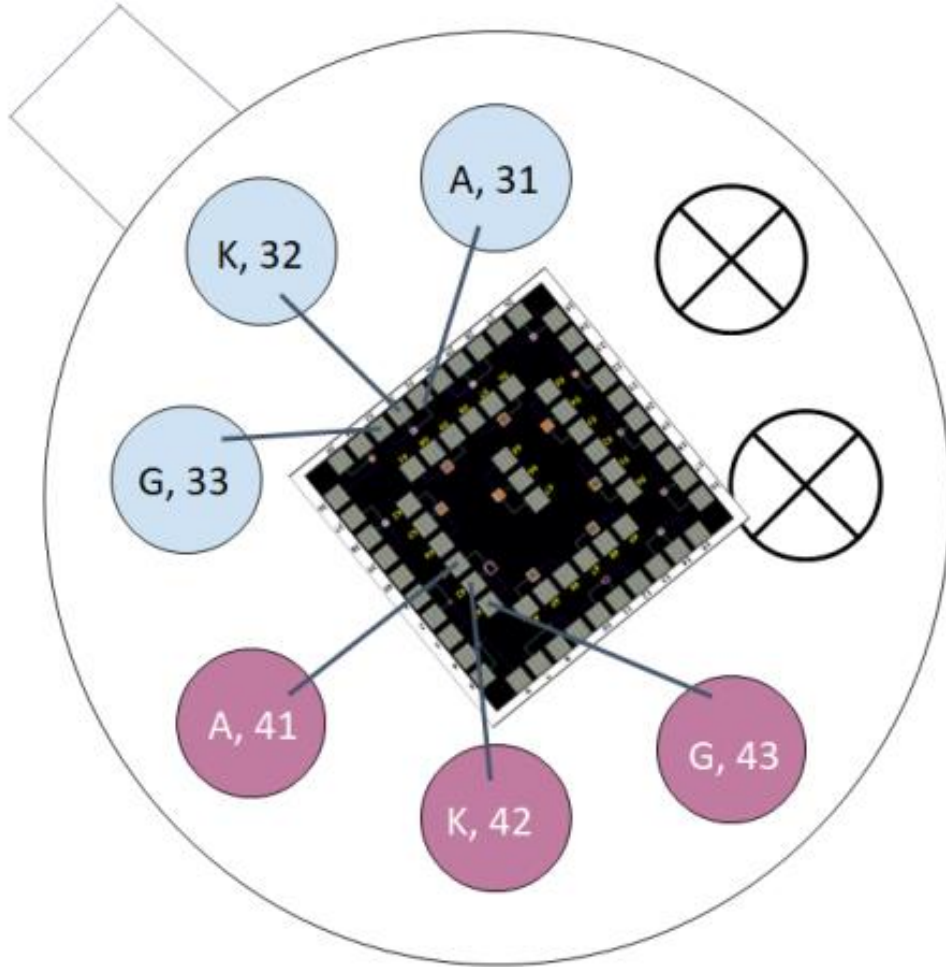

Figure A.5g.10 – Version 10

Figure A.5g.11 – Version 11
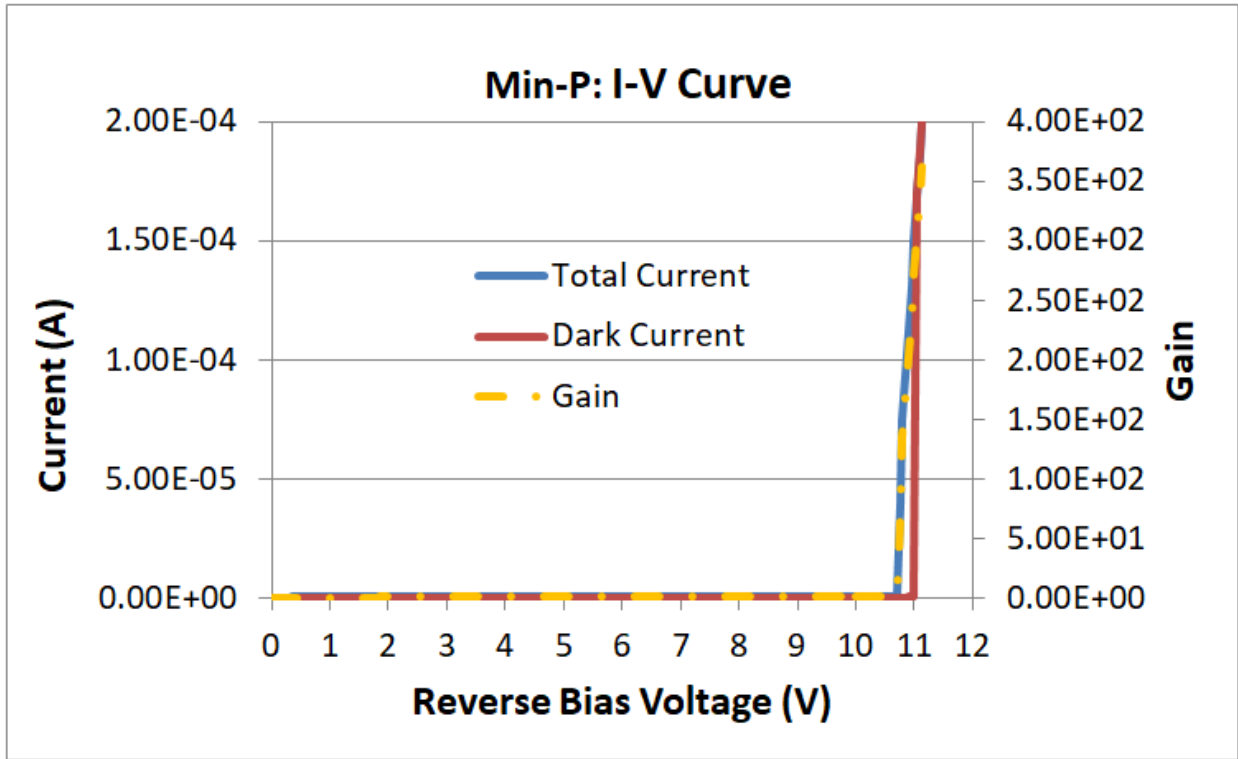
Chapter 7 Appendix

Appendix 7a: Chip 1 I-V Curves
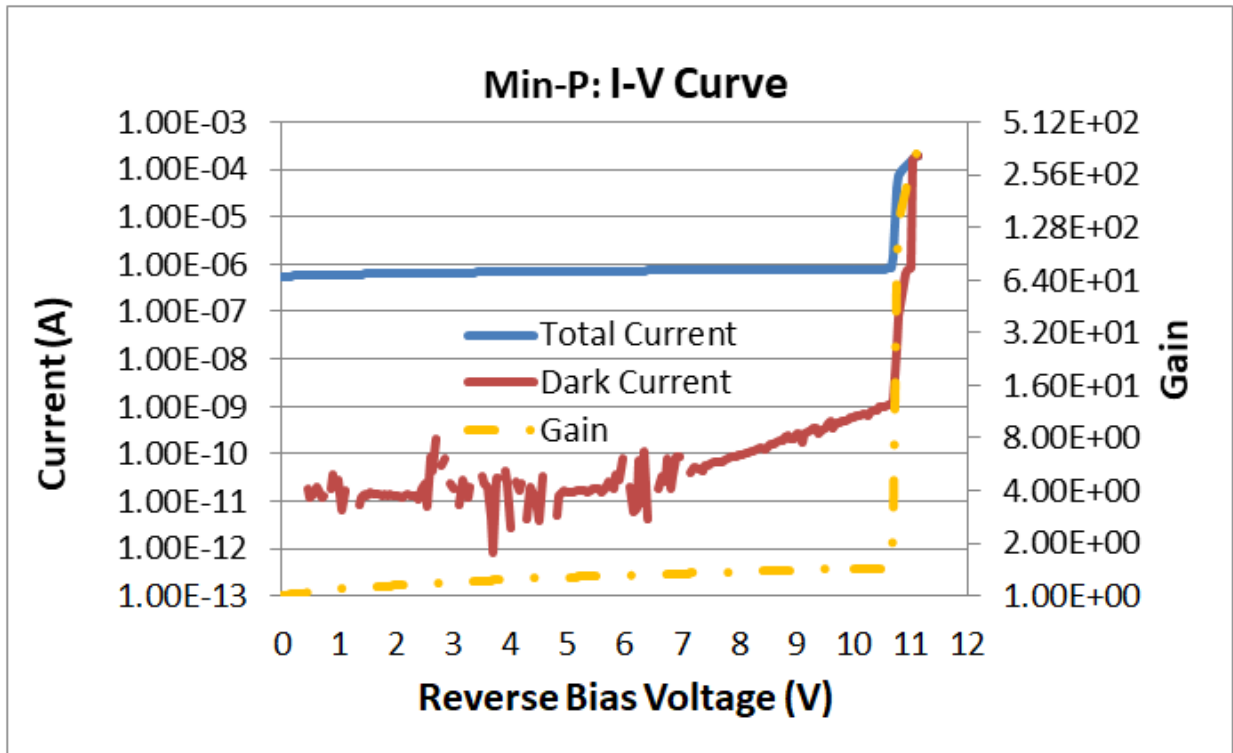
Figure A.7a.1 – I-V Curve of Min-P APD

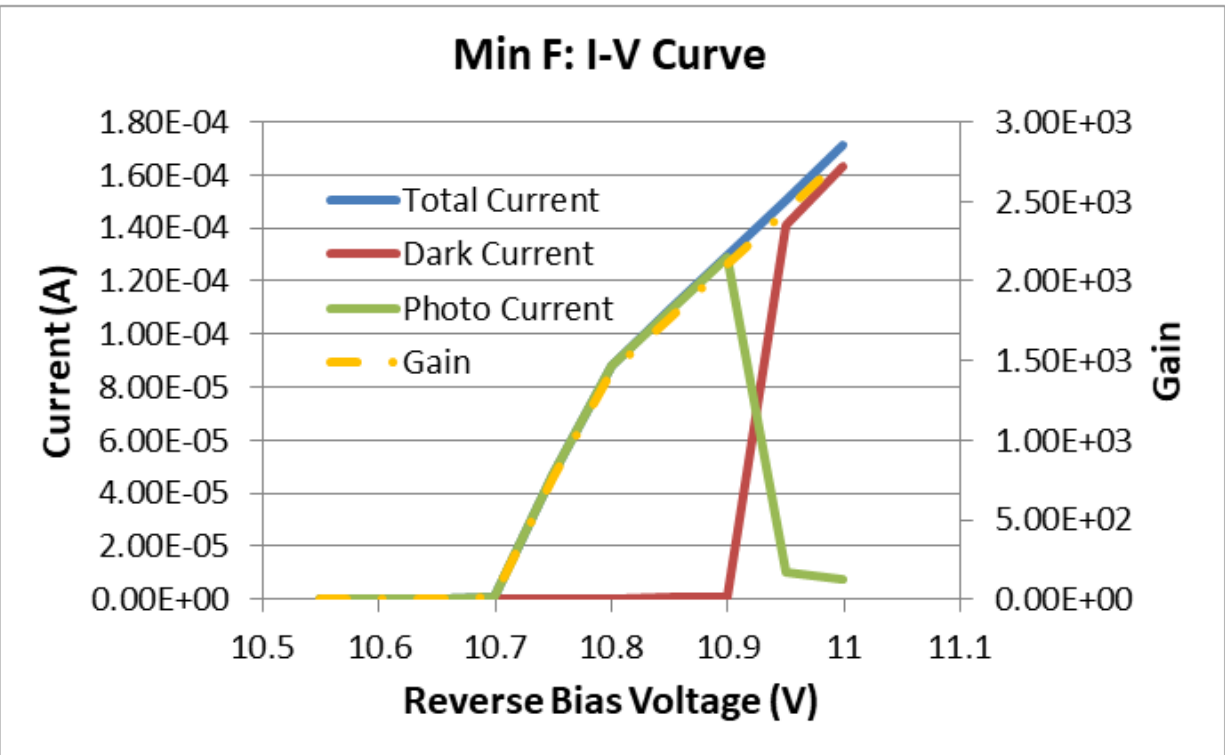**Figure A.7a.2 – I-V Curve of Min-P APD with Y-axes in Logarithmic Form**

124
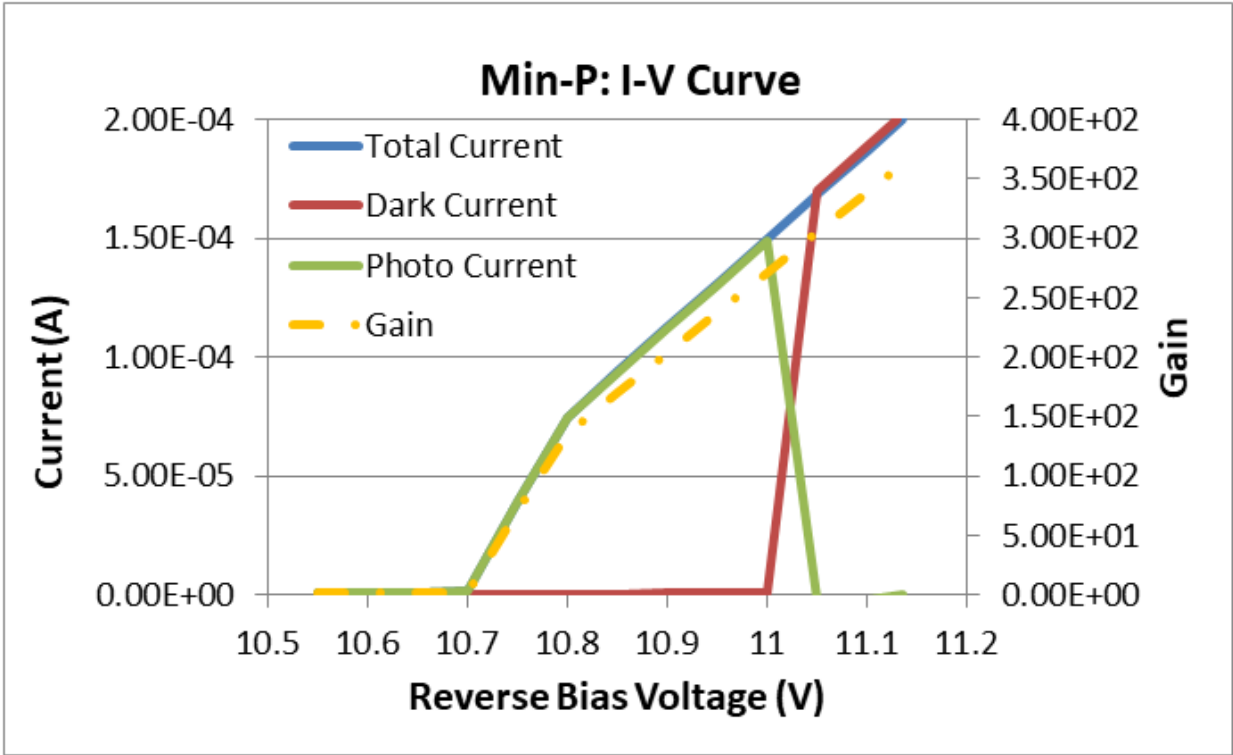
Figure A.7a.3 – I-V Curve of Min-P Zoomed in around Breakdown Voltage
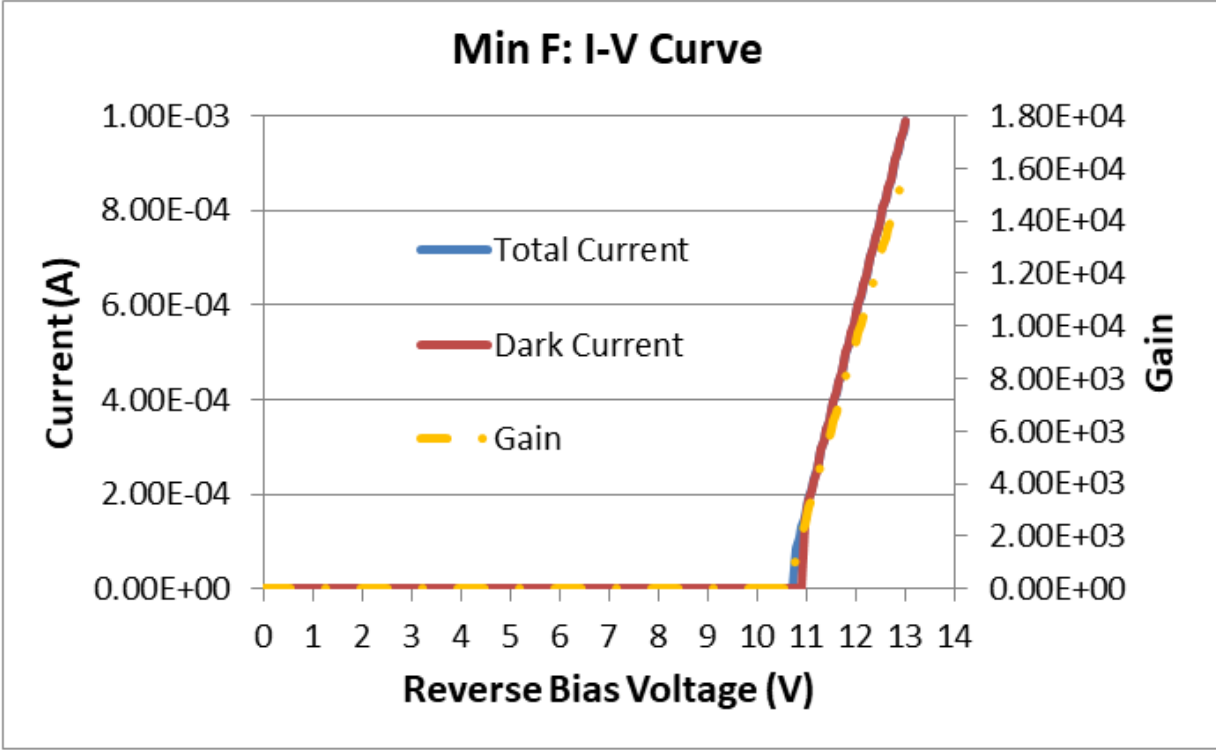
Figure A.7a.4 – I-V Curve of Min-F APD
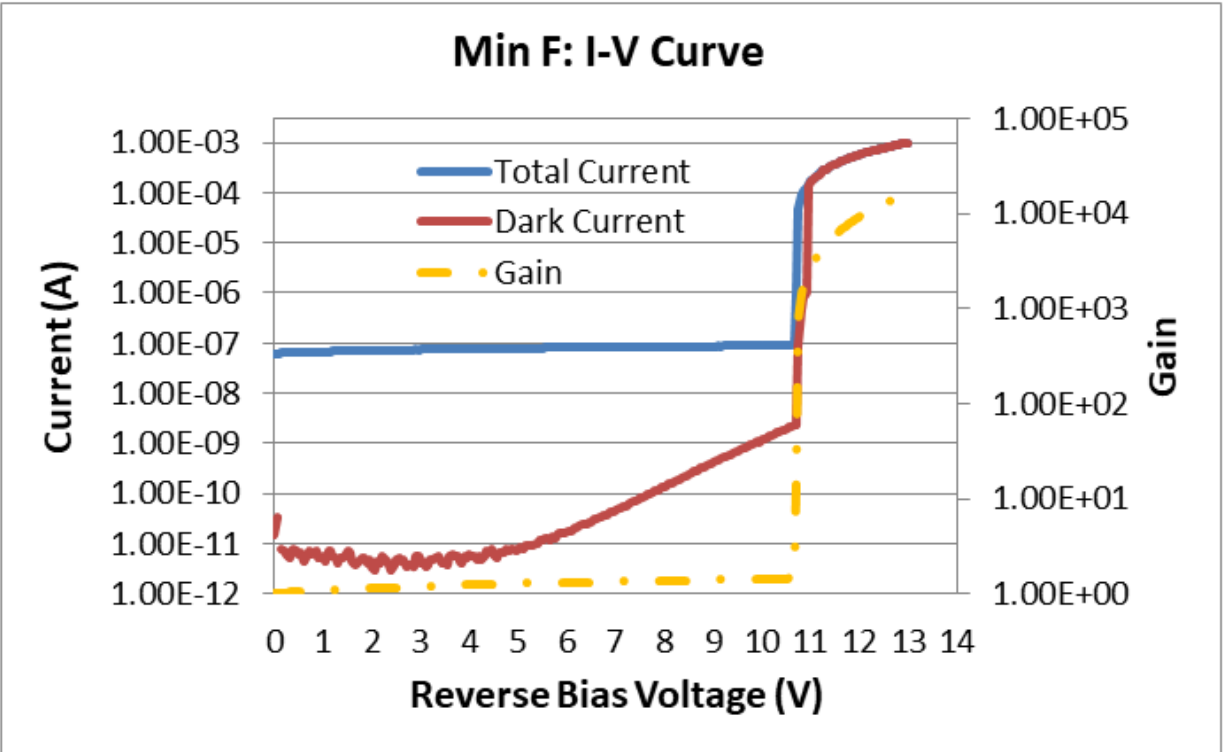
Figure A.7a.5 – I-V Curve of Min-F APD with Y-axes in Logarithmic Form

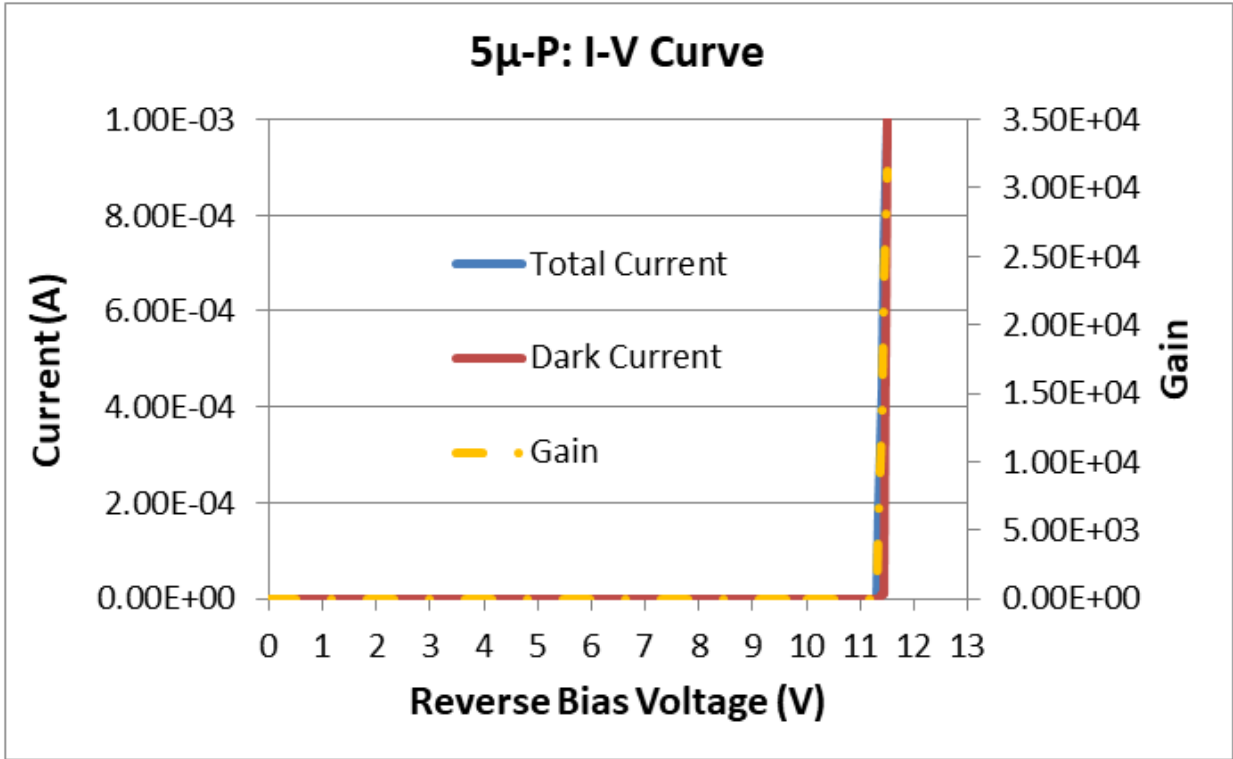**Figure A.7a.6 – I-V Curve of Min-F Zoomed in around Breakdown Voltage**
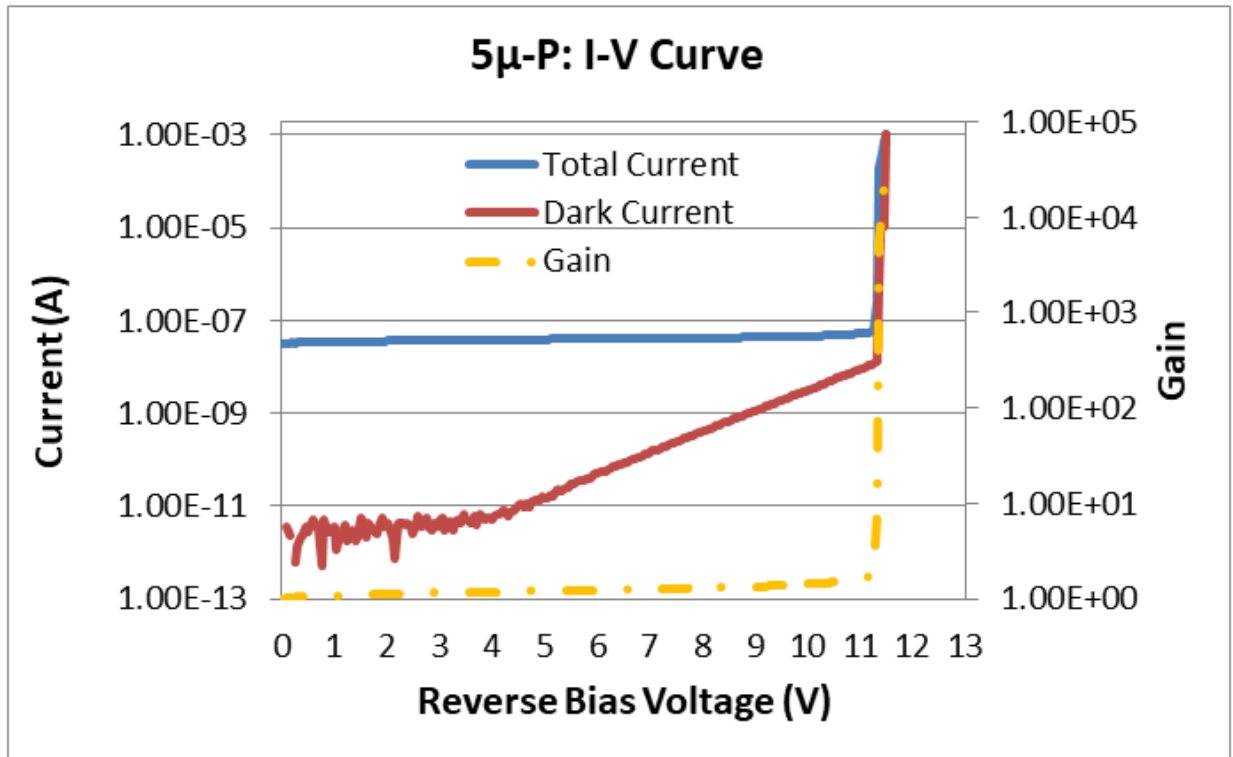
126

Figure A.7a.7 – I-V Curve of 5μ-P APD

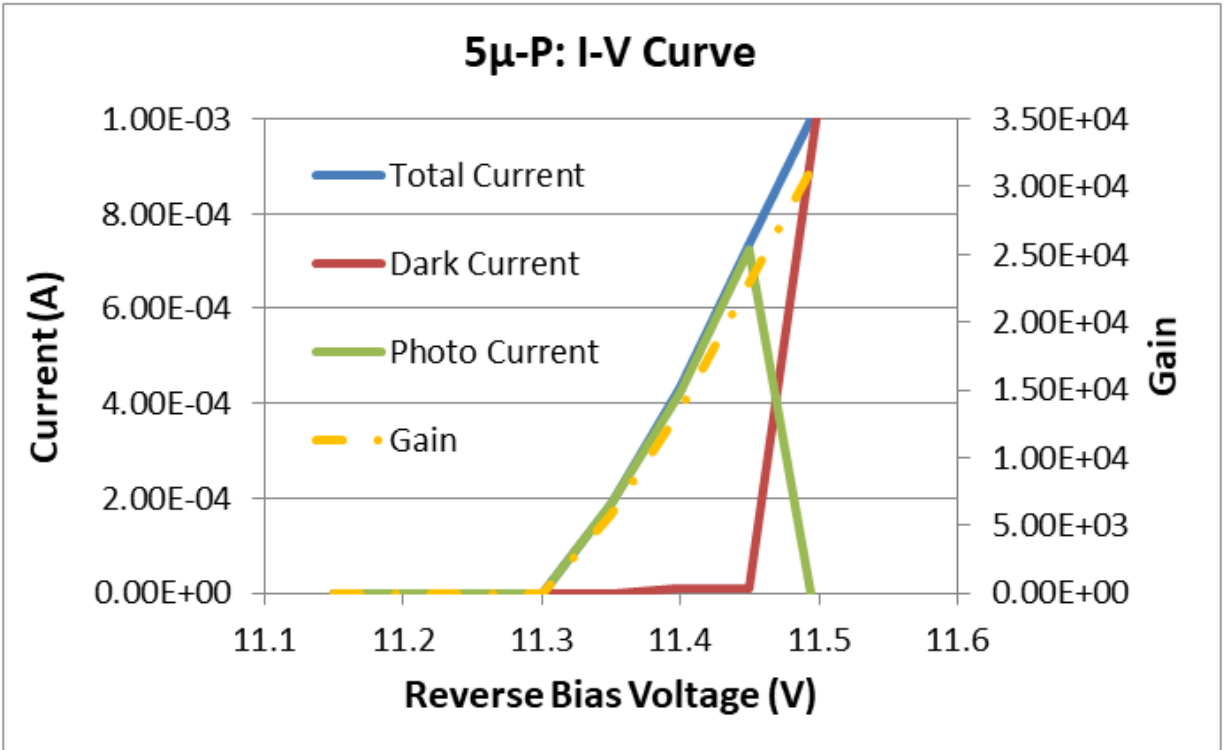**Figure A.7a.8 – I-V Curve of 5μ-P APD with Y-axes in Logarithmic Form**

127

Figure A.7a.9 – I-V Curve of 5μ-P Zoomed in around Breakdown Voltage
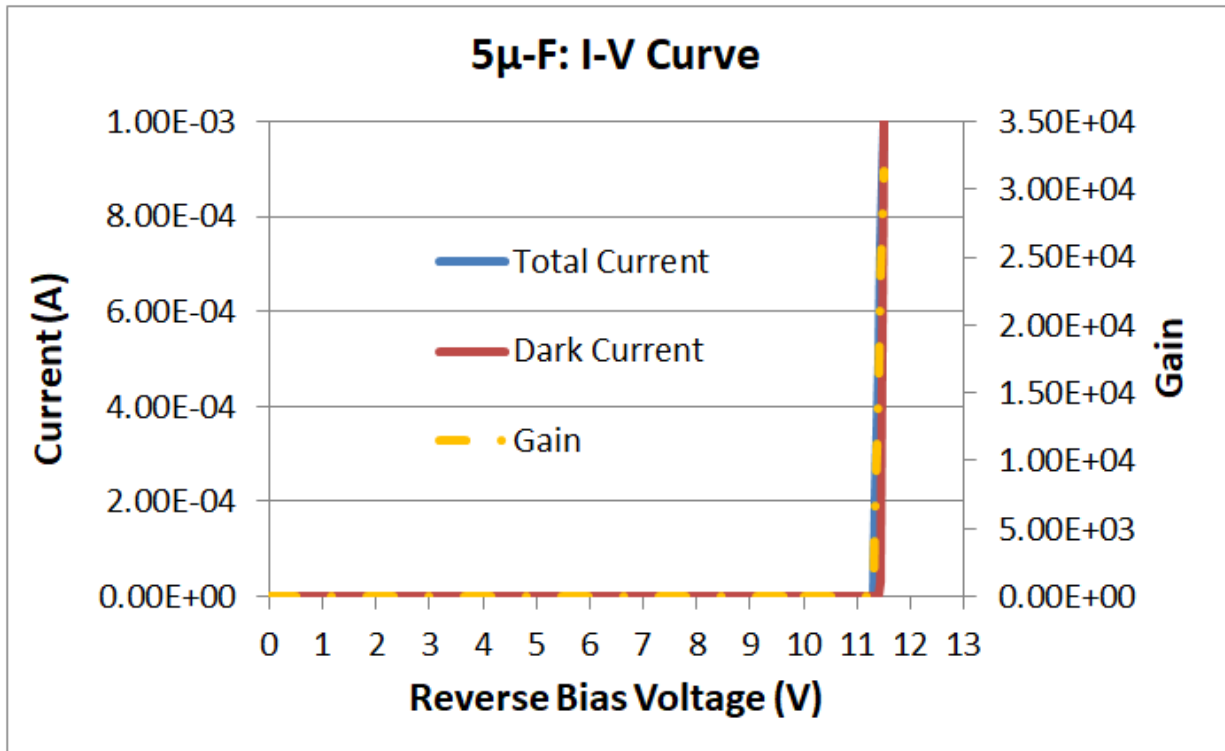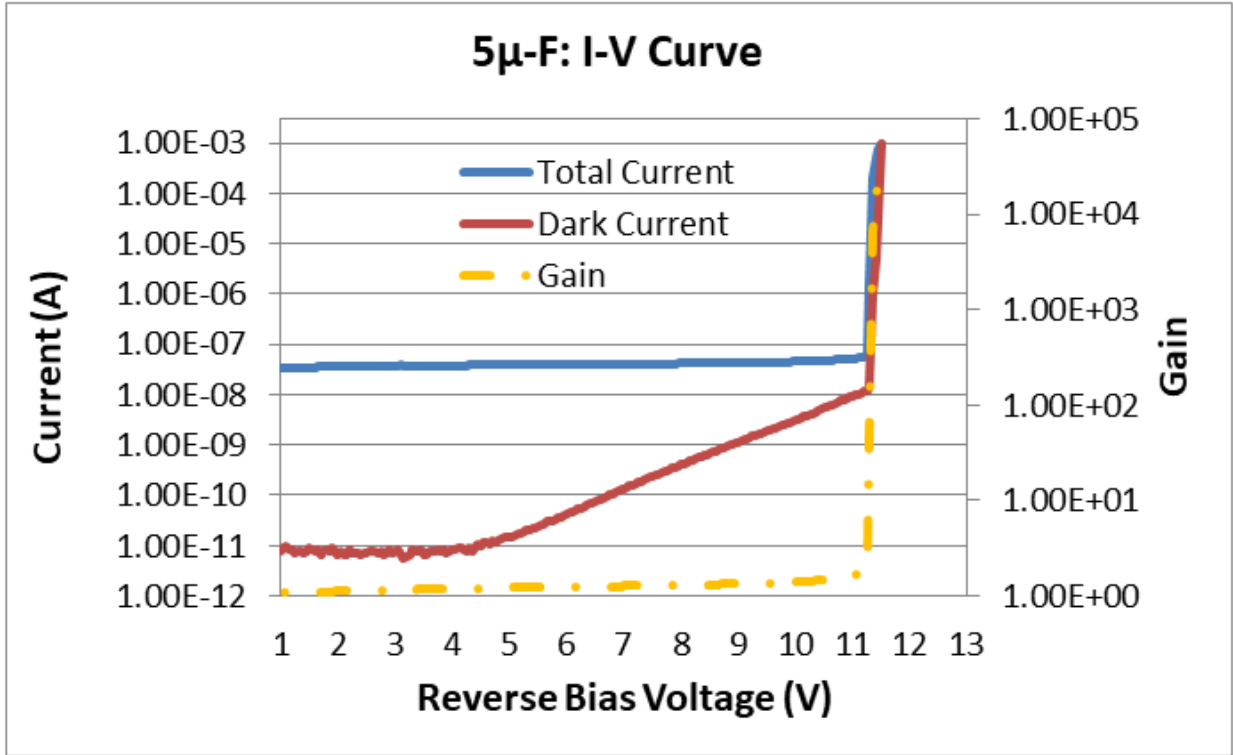

Figure A.7a.10 – I-V Curve of 5μ-F APD

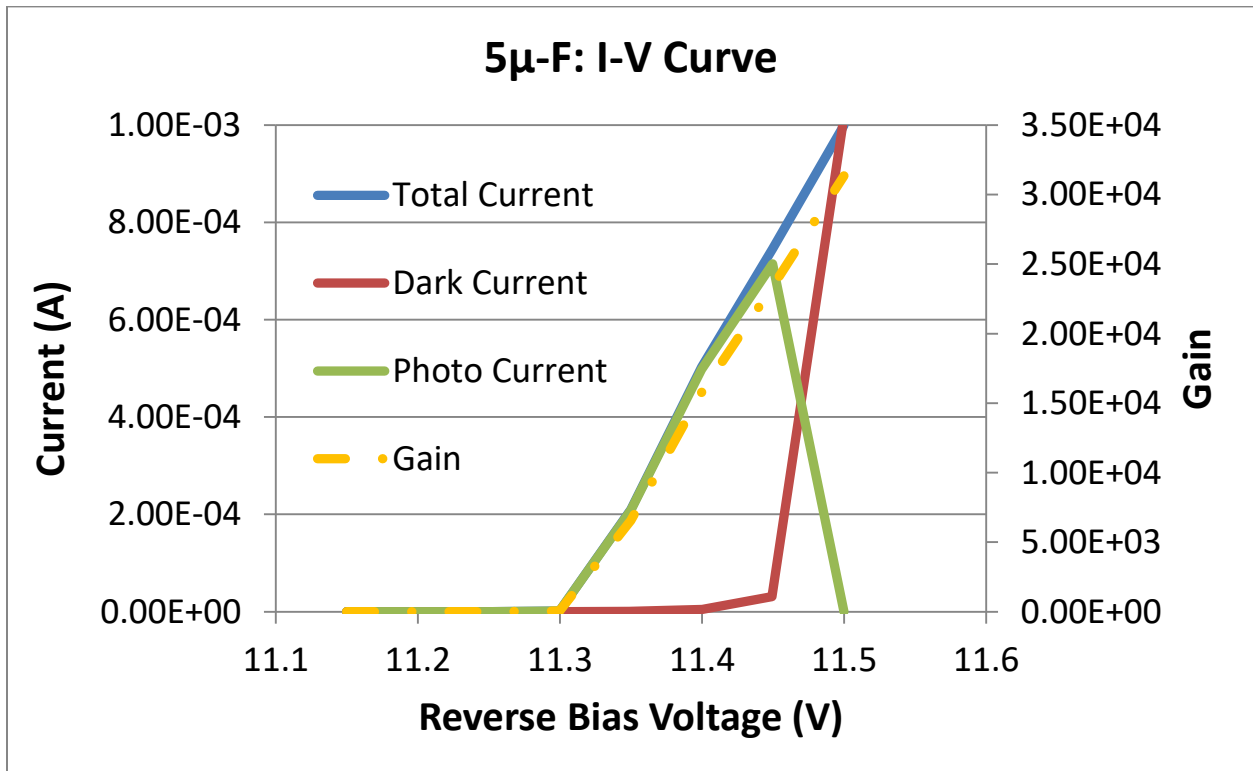**Figure A.7a.11 – I-V Curve of 5μ-F APD with Y-axes in Logarithmic Form**

Figure A.7a.12 – I-V Curve of 5μ-F Zoomed in around Breakdown Voltage

129

Figure A.7a.13 – I-V Curve of 24μ-P APD

Figure A.7a.14 – I-V Curve of 24μ-P APD with Y-axes in Logarithmic Form

130

Figure A.7a.15 – I-V Curve of 24μ-P Zoomed in around Breakdown Voltage

Figure A.7a.16 – I-V Curve of 24μ-F APD

131

Figure A.7a.17 – I-V Curve of 24μ-F APD with Y-axes in Logarithmic Form
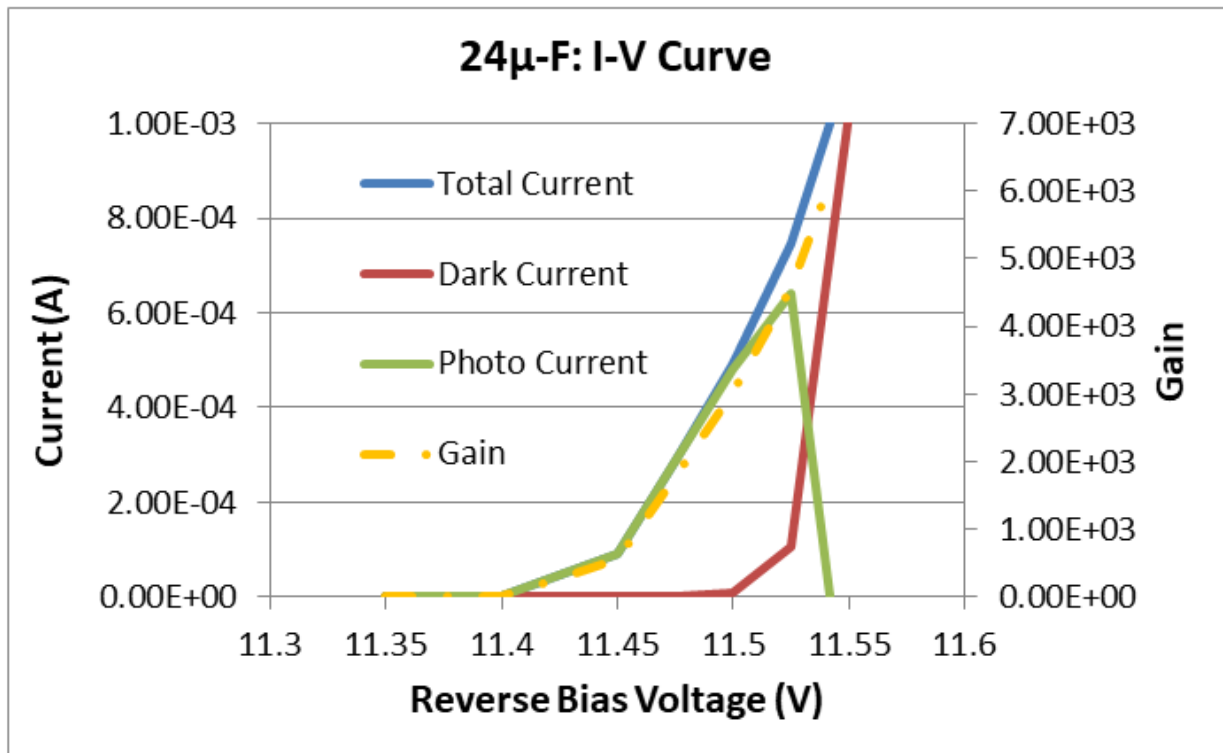
Figure A.7a.18 – I-V Curve of 24μ-F Zoomed in around Breakdown Voltage
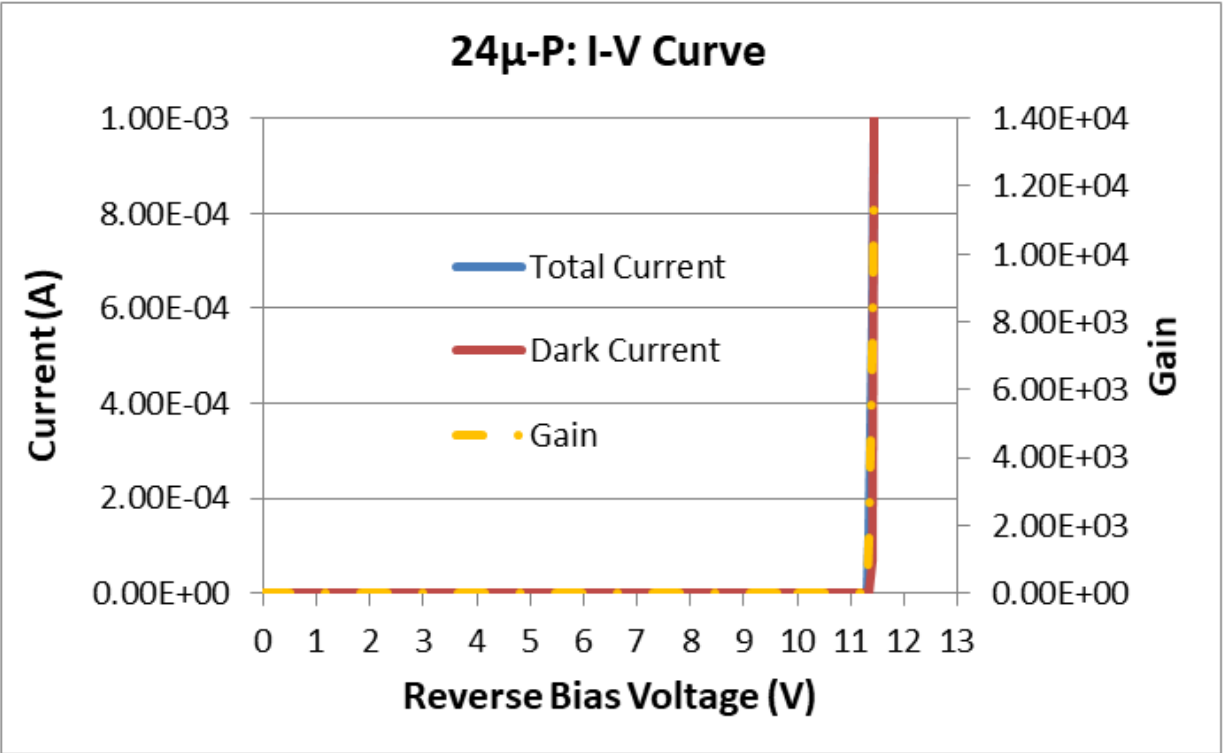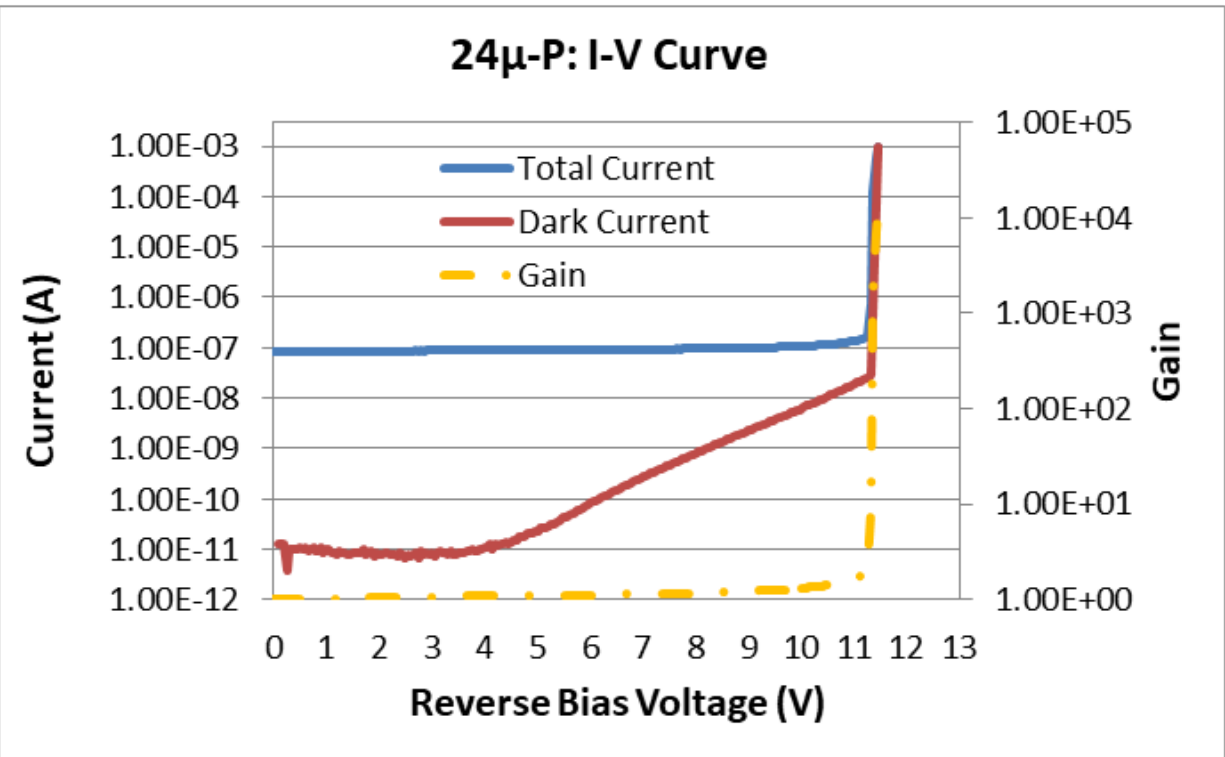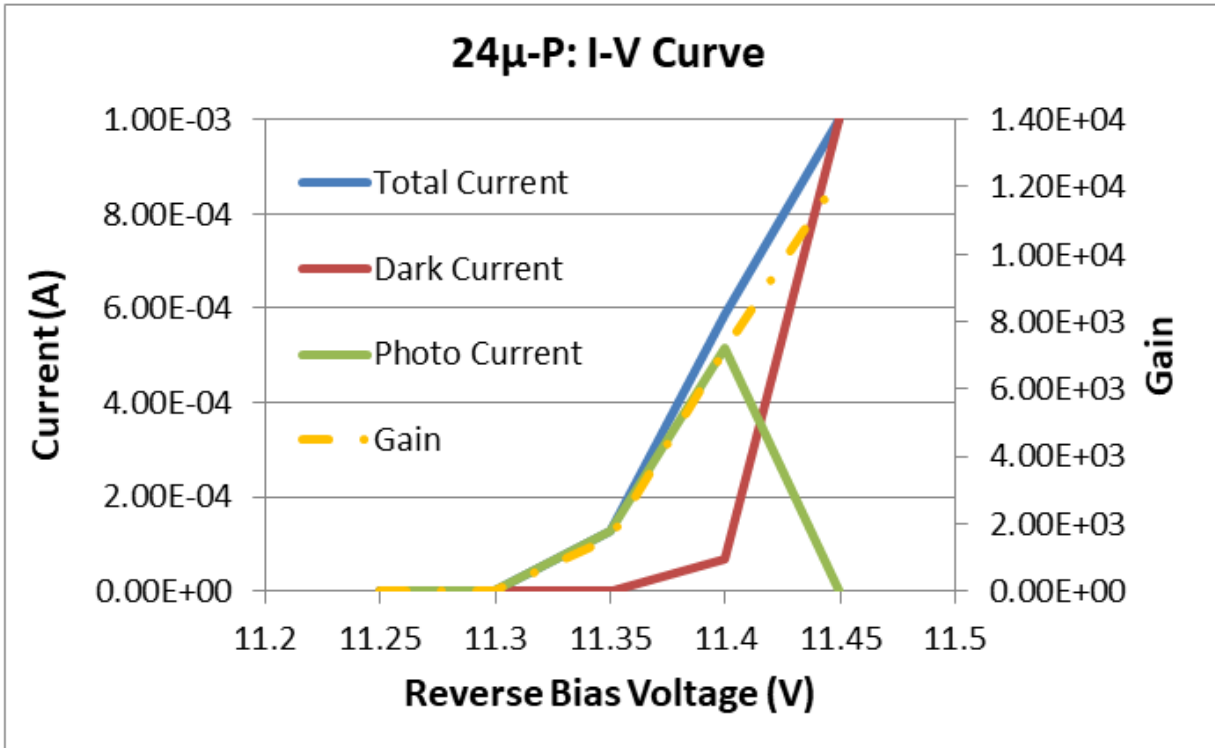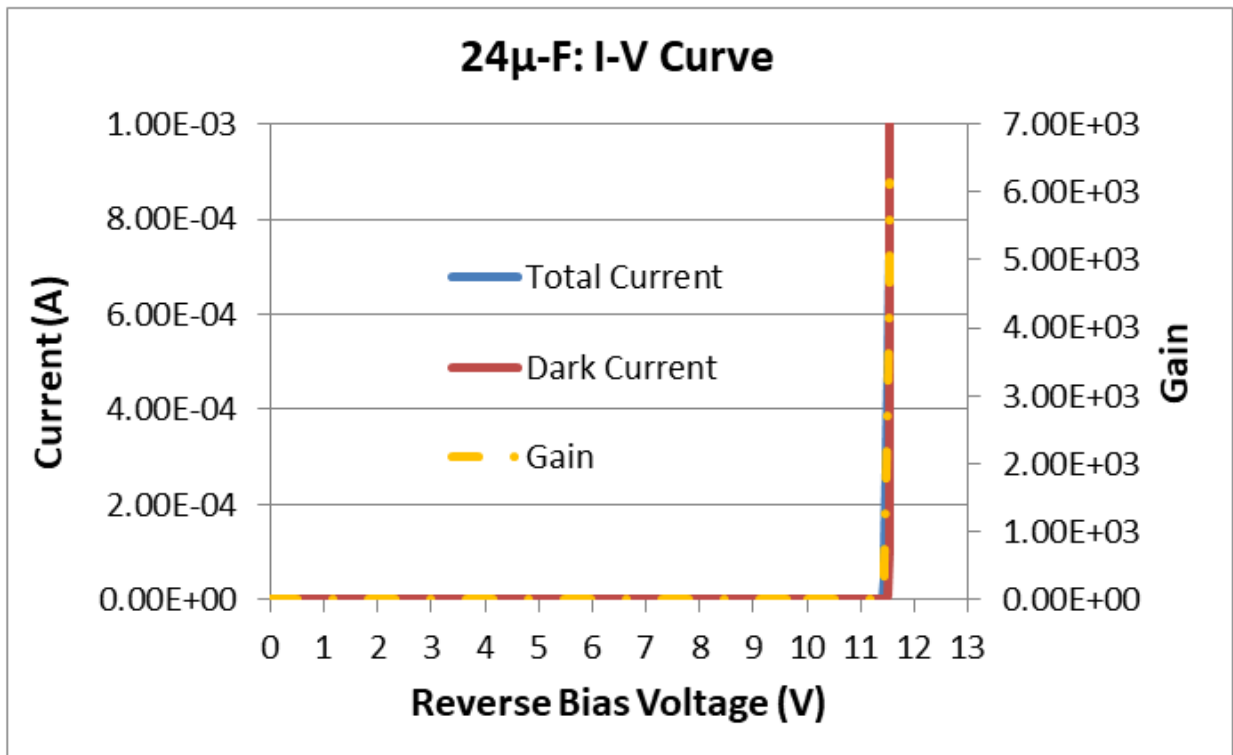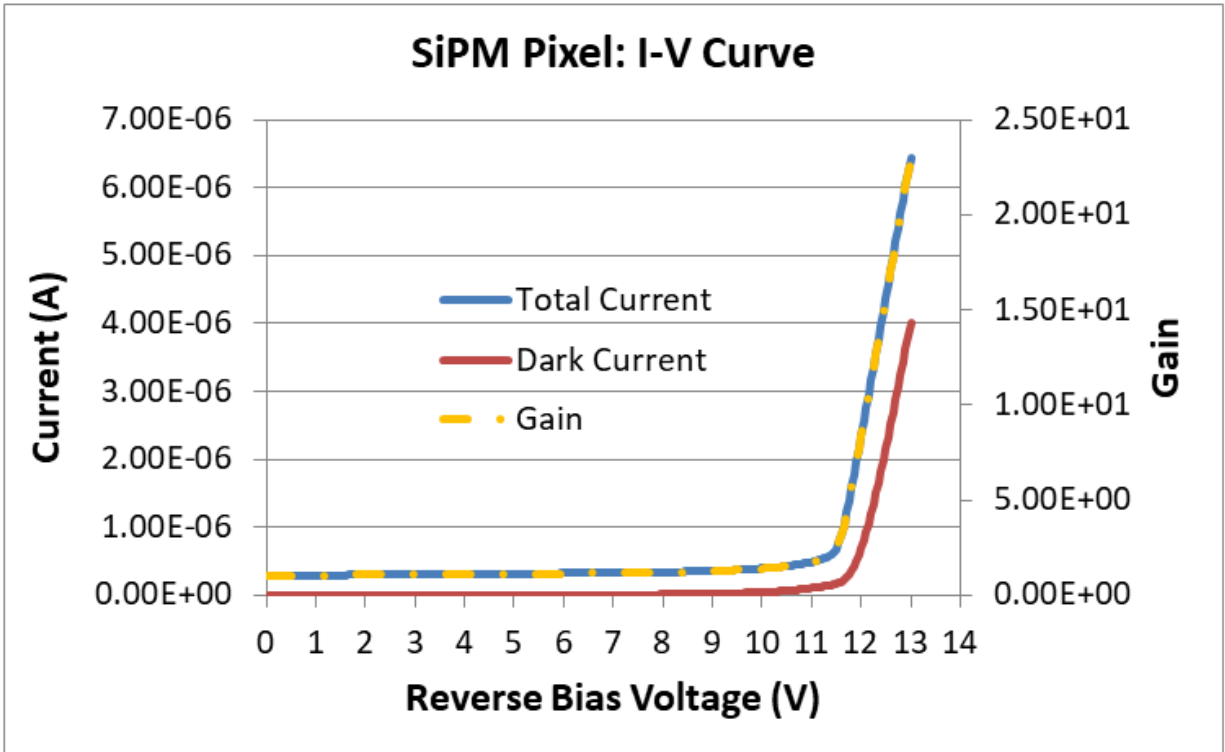
Figure A.7a.19 – I-V Curve of SiPM Pixel
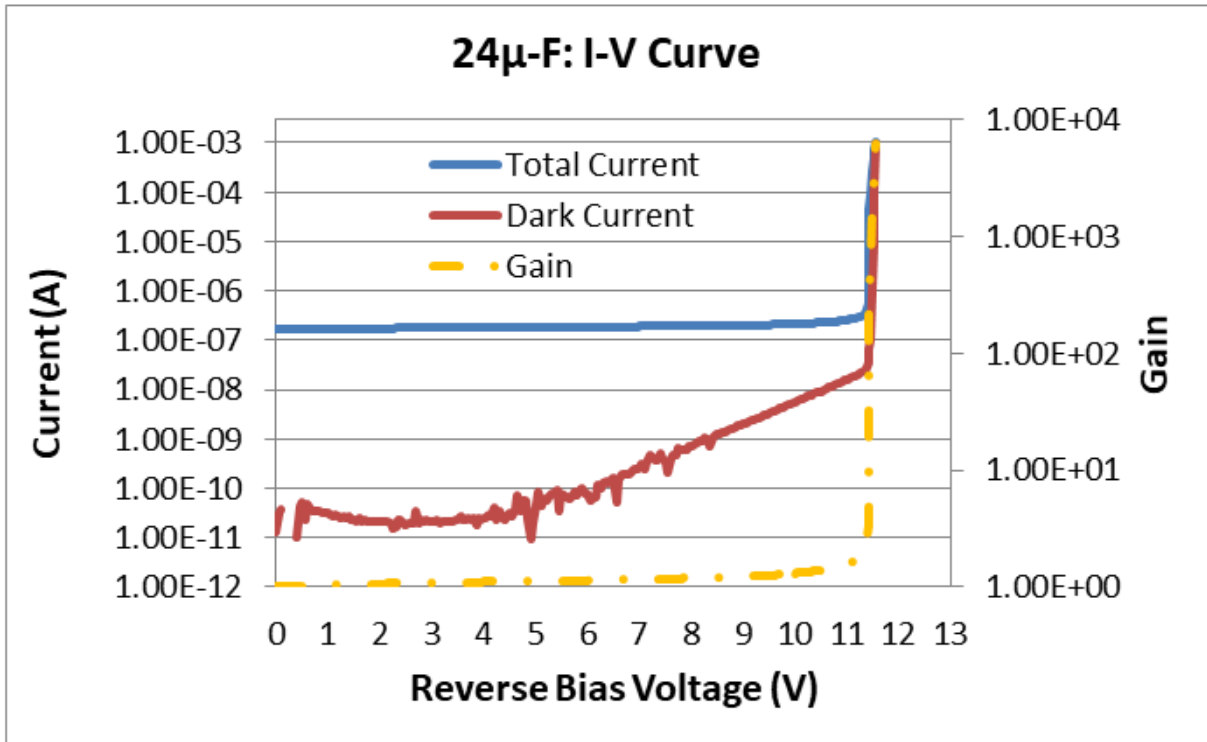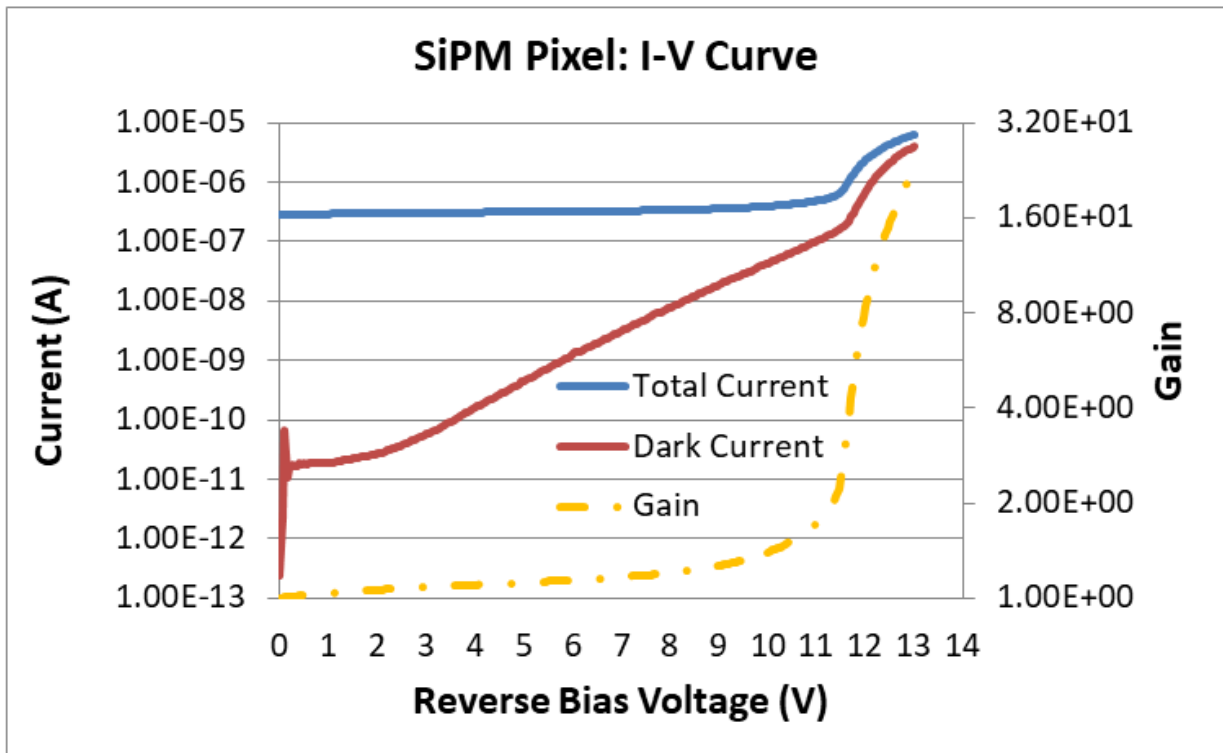

Figure A.7a.20 – I-V Curve of SiPM Pixel with Y-axes in Logarithmic Form

133
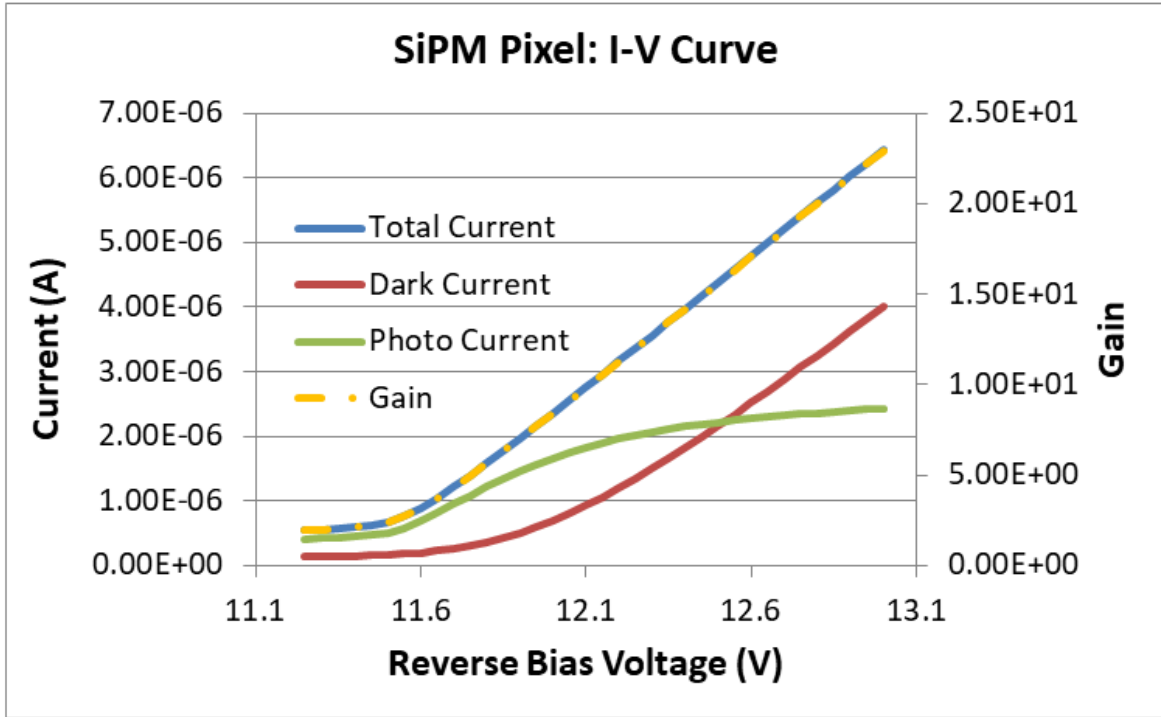
Figure A.7a.21 – I-V Curve of SiPM Pixel Zoomed in around Breakdown Voltage

Appendix 7b: Chip 1 Dark and Light Count Graphs

Figure A.7b.1 – DCR and LCR (643nm) vs. Bias Voltage for Min-P APD

Figure A.7b.2 – Photon Counts vs. Bias Voltage for Min-P APD

Figure A.7b.3 – DCR and LCR (643nm) vs. Bias Voltage for Min-F APD

Figure A.7b.4 – Photon Counts vs. Bias Voltage for Min-F APD

Figure A.7b.5 – DCR and LCR (643nm) vs. Bias Voltage for 5μ-P APD

Figure A.7b.6 – Photon Counts vs. Bias Voltage for 5μ-P APD

Figure A.7b.7 – DCR and LCR (643nm) vs. Bias Voltage for 5µ-F APD

Figure A.7b.8 – Photon Counts vs. Bias Voltage for 5µ-F APD

Figure A.7b.9 – DCR and LCR (643nm) vs. Bias Voltage for 24μ-P APD

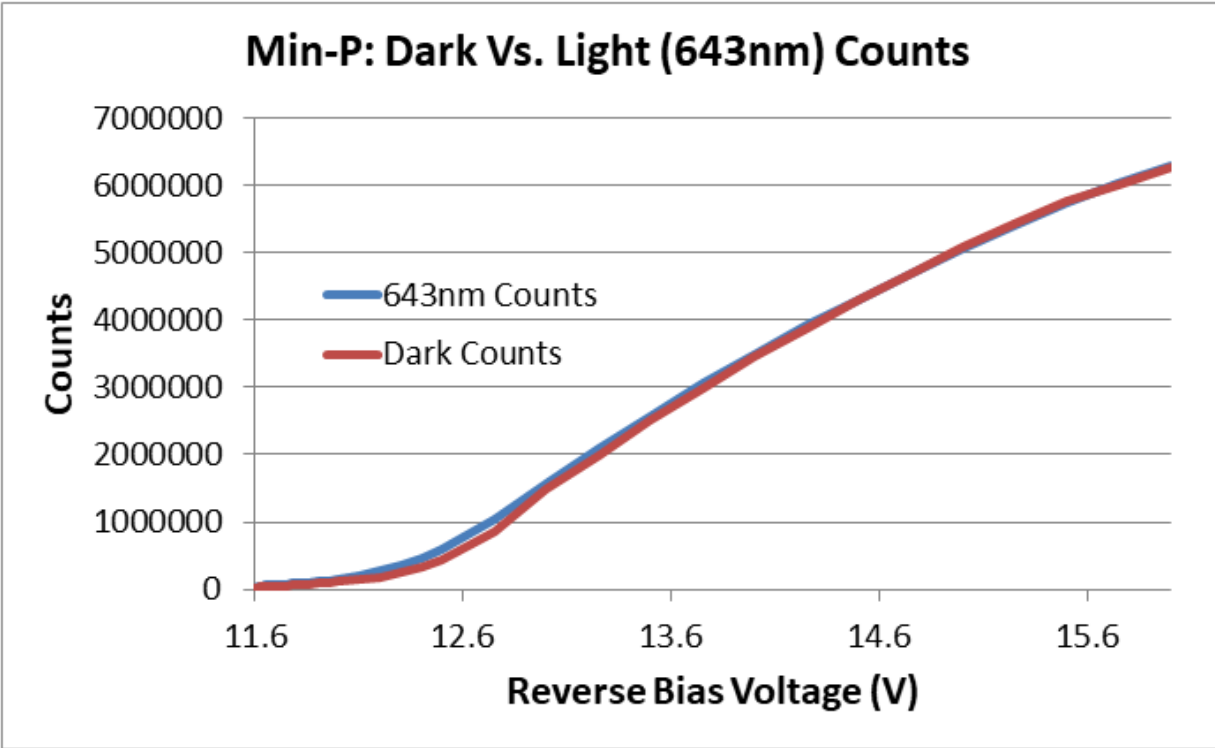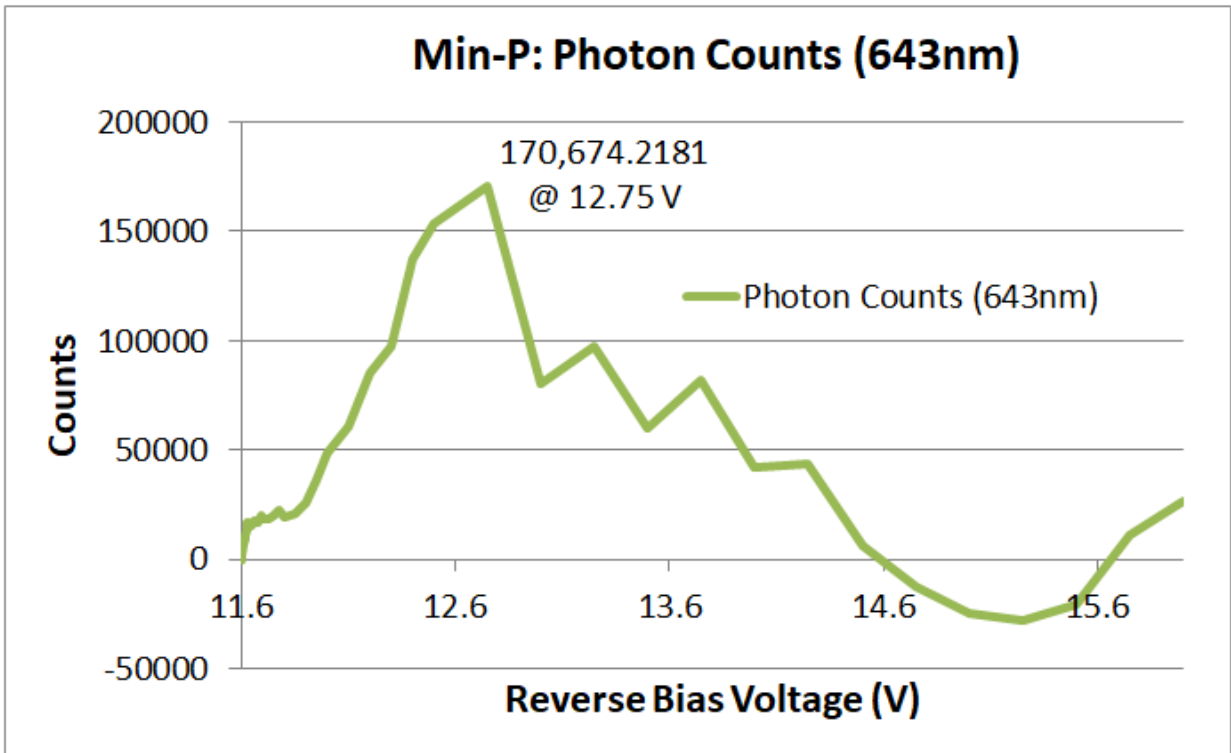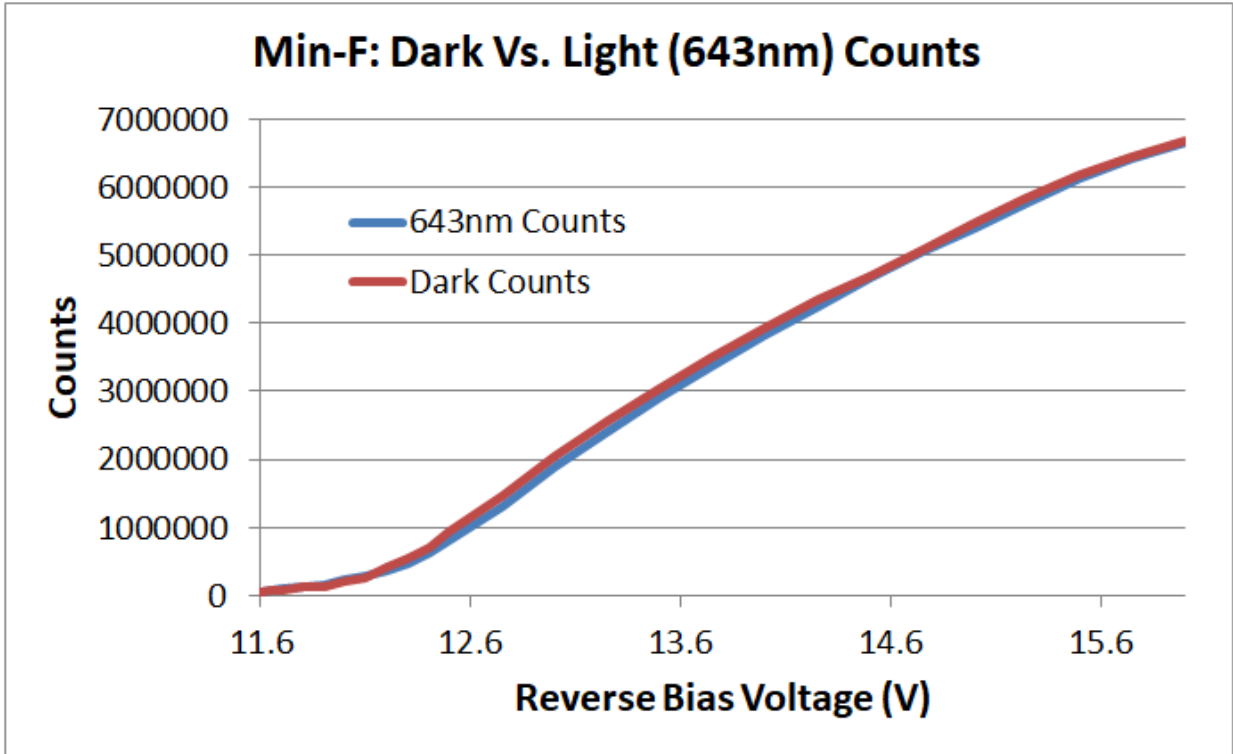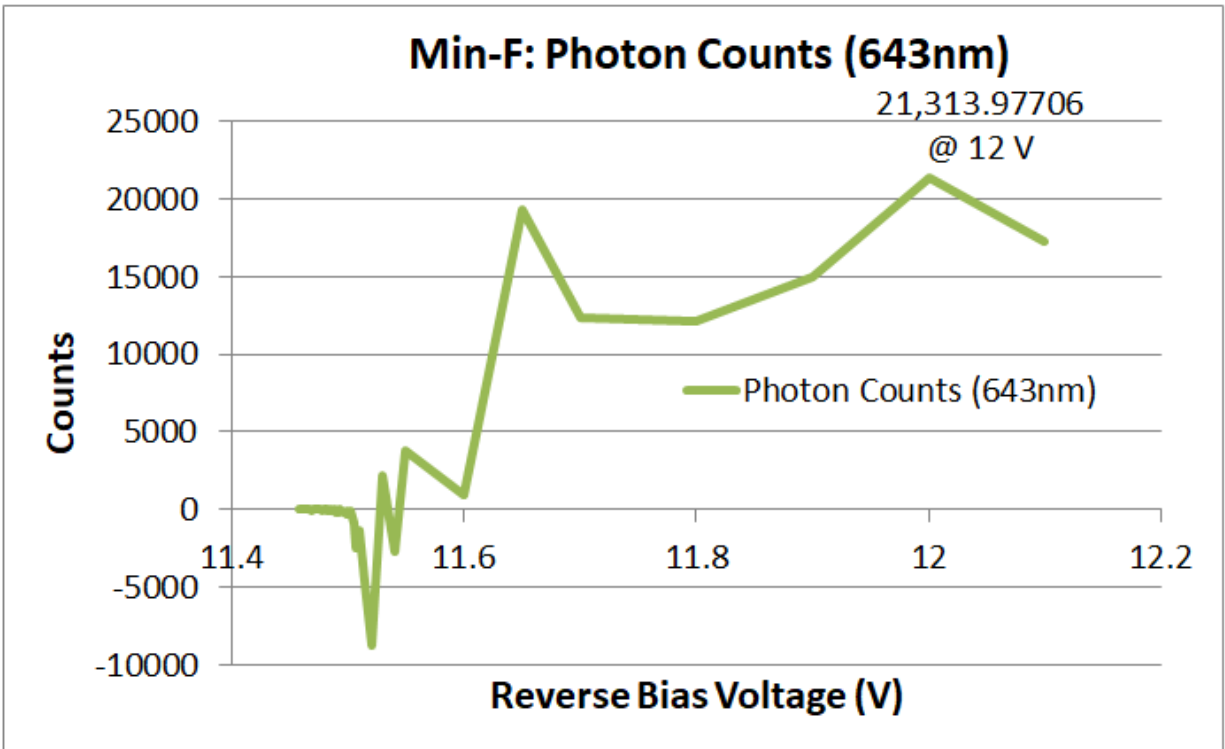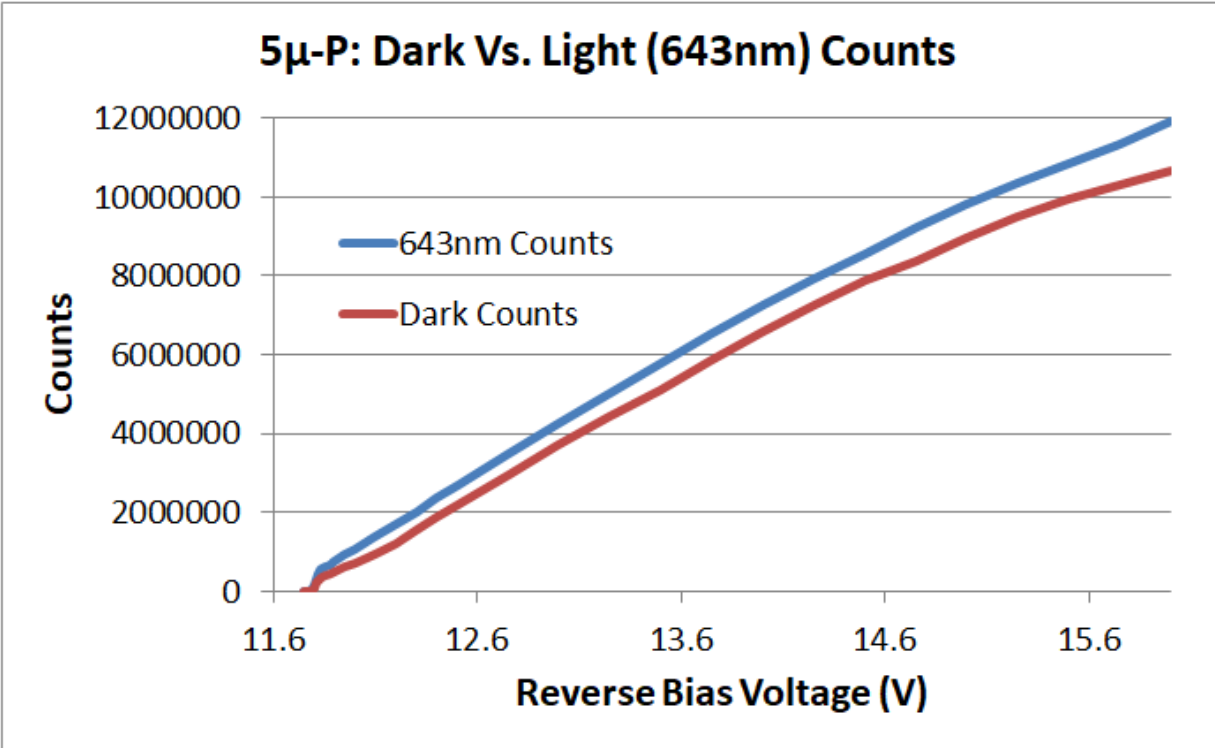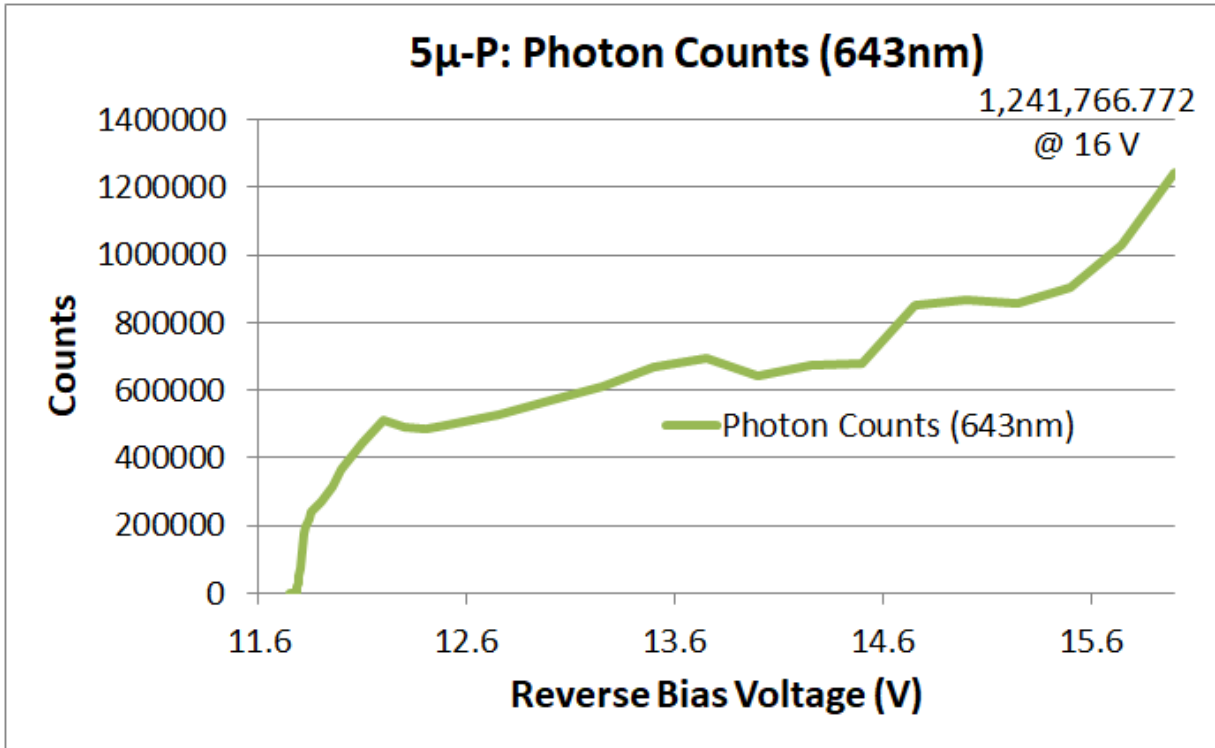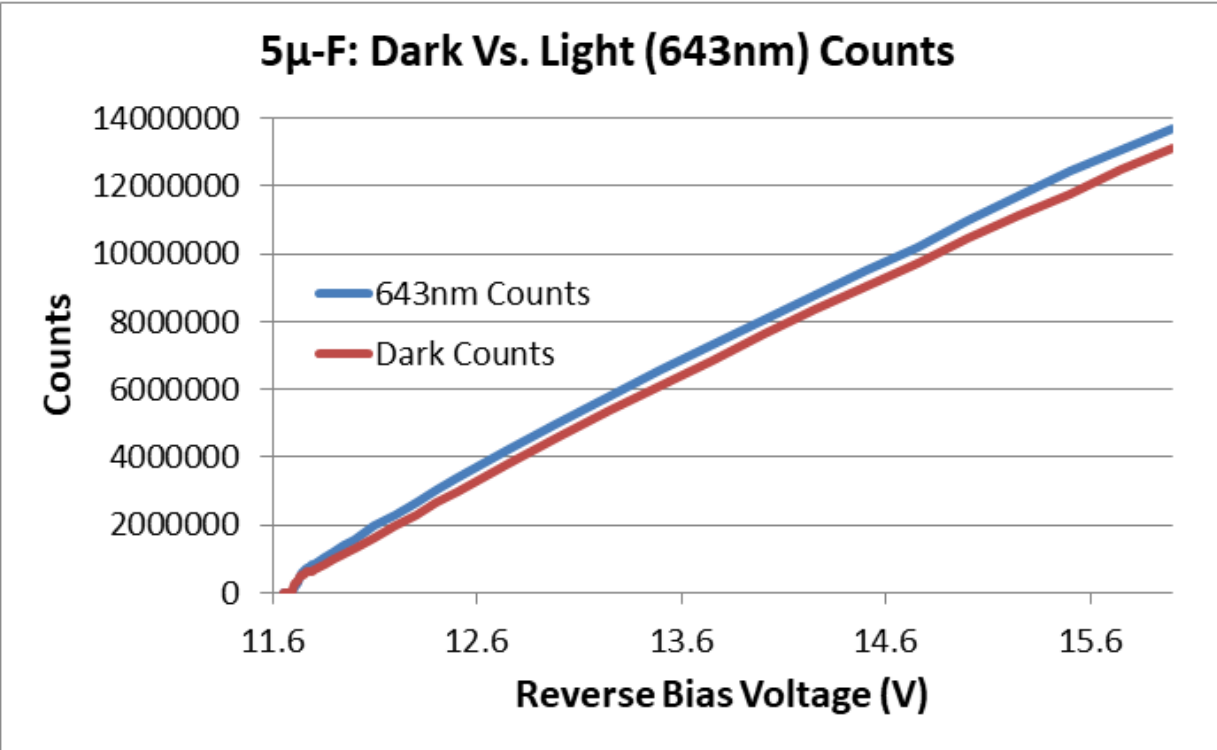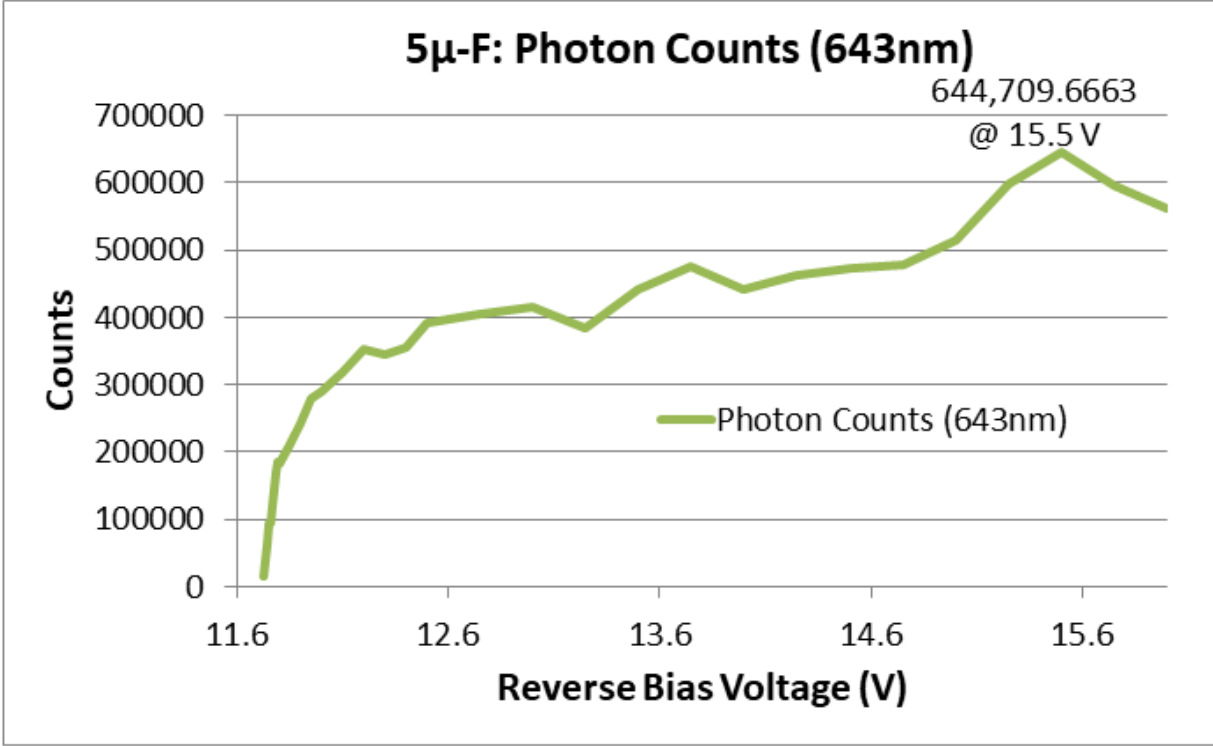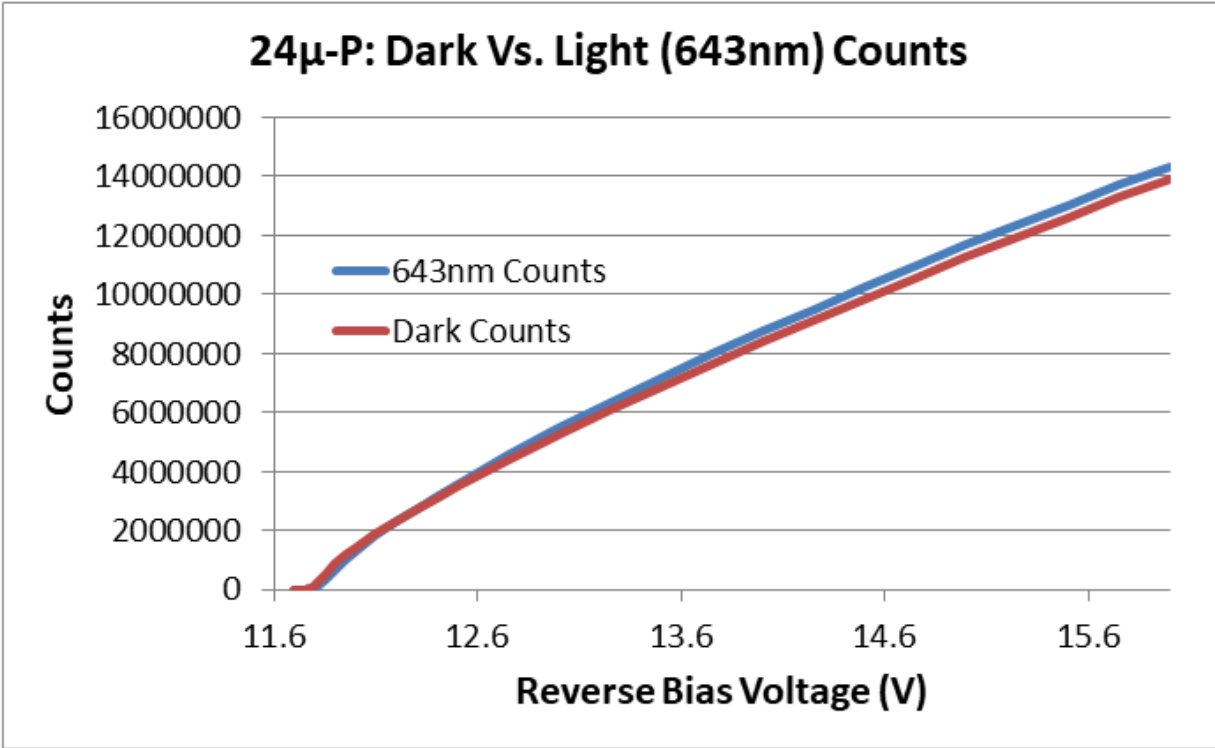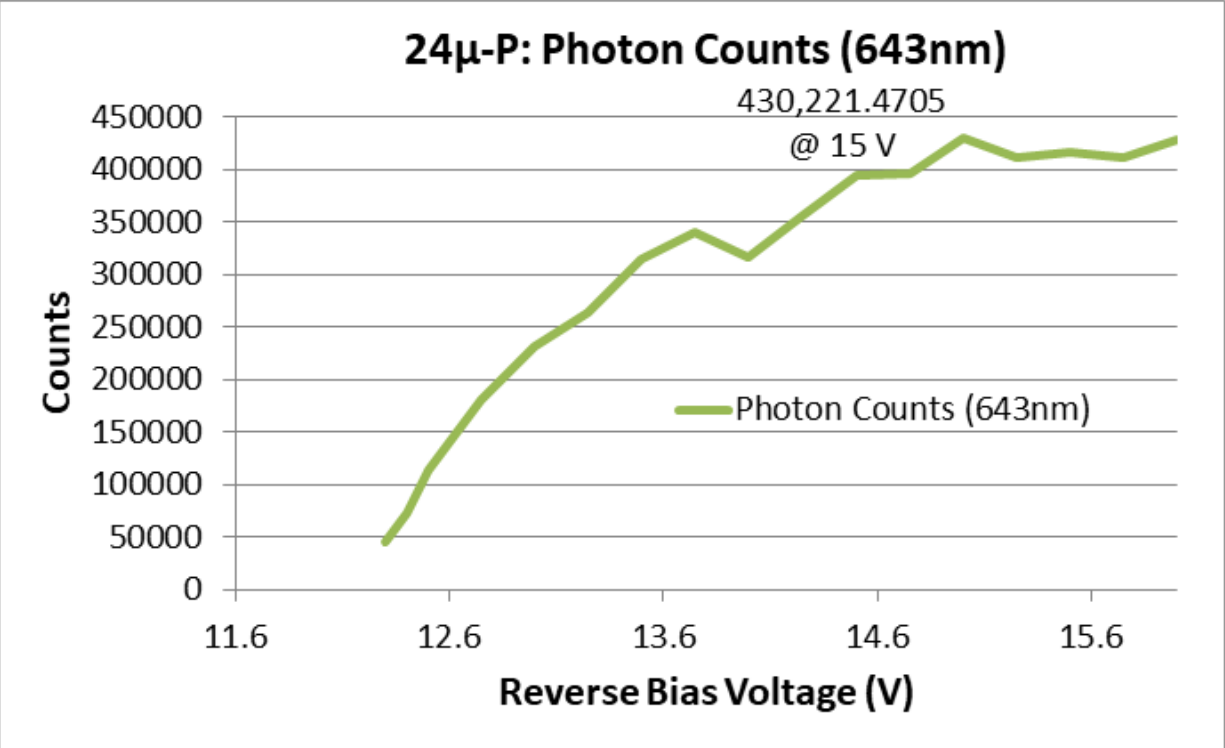**Figure A.7b.10 – Photon Counts vs. Bias Voltage for 24μ-P APD**
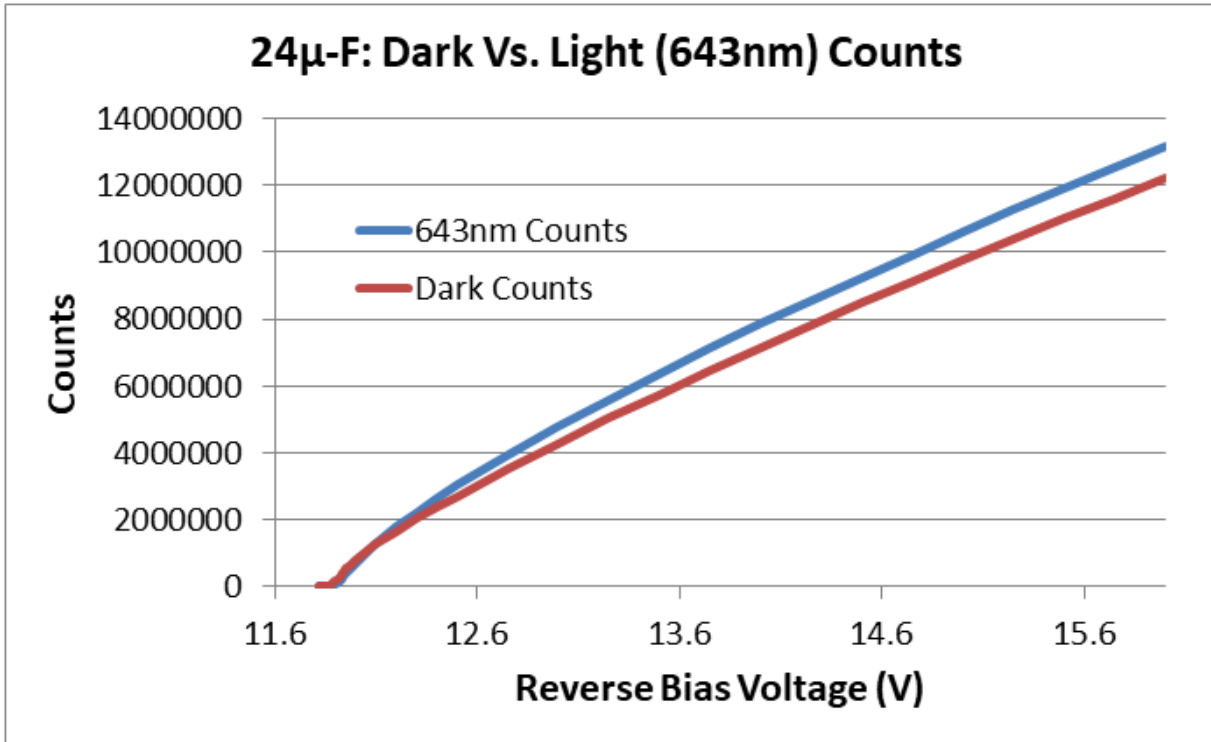
Figure A.7b.11 – DCR and LCR (643nm) vs. Bias Voltage for 24μ-F APD
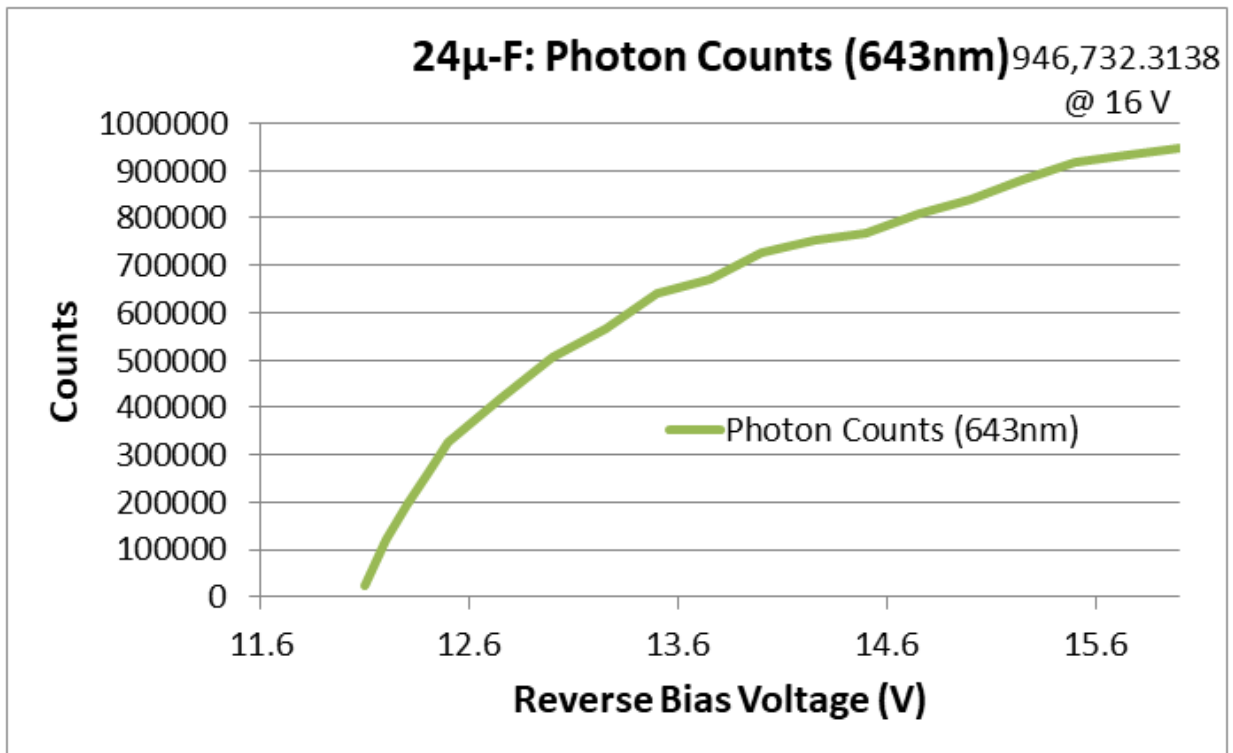
Figure A.7b.12 – Photon Counts vs. Bias Voltage for 24μ-F APD

140

References

[1]   "Automotive ADAS," SensL. [Online]. Available at:

https://sensl.com/applications/lidar1/adas/. [Accessed: 2018].

[2]   "Automotive ADAS," SensL. [Online]. Available at:

https://sensl.com/applications/lidar1/adas/. [Accessed: 2018].

[3]   E. Vilella, A. Vilà, F. Palacio, M. López, and A. Diéguez, "Characterization of linear-

mode APDs in standard CMOS," *Procedia Engineering 87*, pp. 728-731, 2014.

[4]   "Electromagnetic Spectrum," [Online]. Available at:

https://sites.google.com/site/chempendix/em-spectrum. [Accessed: 2018].

[5]   Hamamatsu Optosemiconductor Handbook, *Chapter 2: Si Photodiode*, pp. 6.

[6]   "Intrinsic Semiconductor," [Online]. Available at: http://www.physics-and-radio-

electronics.com/electronic-devices-and-circuits/semiconductor/intrinsic-

semiconductor/atomic-structure-of-silicon-and-germanium.html. [Accessed: 2018].

[7]   "Intrinsic Semiconductor," [Online]. Available at: http://www.physics-and-radio-

electronics.com/electronic-devices-and-circuits/semiconductor/intrinsic-

semiconductor/covalent-bonding-ins-si-and-ge.html. [Accessed: 2018].

[8]   Hamamatsu Optosemiconductor Handbook, *Glossary*, pp. 1.

[9]   Hamamatsu Optosemiconductor Handbook, *Chapter 2: Si Photodiode*, pp. 6.

[10]   Baker, R. J, *CMOS Circuit Design, Layout, and Simulation*, *Third Edition*, John Wiley

and Sons, Inc. , 2010. pp. 43.

[11]   Hamamatsu Optosemiconductor Handbook, *Chapter 1: Introduction*, pp. 5.

[12]   Hamamatsu Optosemiconductor Handbook, *Chapter 2: Si Photodiode*, pp. 3.

[13] Hamamatsu Optosemiconductor Handbook, *Chapter 6: Compound Semiconductor Photosensors*, pp. 4.

[14] Hamamatsu Optosemiconductor Handbook, *Chapter 1: Introduction*, pp. 2.

[15] Hamamatsu Optosemiconductor Handbook, *Chapter 2: Si Photodiode*, pp. 6.

[16] Hamamatsu Optosemiconductor Handbook, *Chapter 2: Si Photodiode*, pp. 7.

[17] Hamamatsu Optosemiconductor Handbook, *Chapter 3: Si APD, MPPC*, pp. 2.

[18] Hamamatsu Optosemiconductor Handbook, *Chapter 3: Si APD, MPPC*, pp. 3.

[19] "Schematic APD I-V Curves Showing the Linear Mode," [Online]. Available at: https://www.researchgate.net/figure/Schematic-APD-I-V-curves-showing-the-Linear-Mode_fig1_238553582. [Accessed: 2018].

[20] Hamamatsu Optosemiconductor Handbook, *Chapter 3: Si APD, MPPC*, pp. 2.

[21] Hamamatsu Optosemiconductor Handbook, *Chapter 3: Si APD, MPPC*, pp. 14.

[22] Hamamatsu Optosemiconductor Handbook, *Chapter 3: Si APD, MPPC*, pp. 16.

[23] Hamamatsu Optosemiconductor Handbook, *Chapter 3: Si APD, MPPC*, pp. 16.

[24] Hamamatsu Optosemiconductor Handbook, *Chapter 3: Si APD, MPPC*, pp. 17.

[25] Hamamatsu Optosemiconductor Handbook, *Chapter 3: Si APD, MPPC*, pp. 9.

[26] "Development of Multi-Pixel Photon Counters (MPPC)," [Online]. Available at: https://slideplayer.com/slide/8970282/. [Accessed: 2018].

[27] C. Niclass, P. Besse, and E. Charbon, "Arrays of Single Photon Avalanche Photodiodes in CMOS Technology: Picosecond Timing Resolution for Range Imaging," *Proceedings of 1st RIM*, 2005, pp. 1-13.

[28] AMS AG, *0.35 μm HBT BiCMOS Process Parameters*, 2009, pp. 8.

[29] AMS AG, *0.35 μm HBT BiCMOS Design Rules*, 2011, pp. 7-9.

[30]   AMS AG, *0.35 μm HBT BiCMOS Design Rules*, 2011, pp. 58.

[31]   Kulicke & Soffa Ltd. "*K & S 4500 Series Manual Wire Bonders Operation and Maintenance Manual,*" 2002.

[32]   E. Vilella, A. Vilà, F. Palacio, M. López, and A. Diéguez, "Characterization of linear-mode APDs in standard CMOS," *Procedia Engineering 87*, pp. 728-731, 2014.

[33]   AMS AG, *0.35 μm HBT BiCMOS Design Rules*, 2011, pp. 54.

[34]   X. Sun, J. Abshire, M. Krainak, W. Lu, J. Beck, W. Sullivan, P. Mitra, D. Rawlings, R. Fields, D. Hinkley, B. Hirasuna, " Single Photon HgCdTe Avalanche Photodiode and Integrated Detector Cooler Assemblies for Space Lidar Applications," *Proc. SPIE 10659, Advanced Photon Counting Techniques XII*, May 14, 2018, pp. 1-14.

[35]   G. Meinhardt et al., "High-speed blue-, red-, and infrared-sensitive photodiode integrated in a 0.35 /spl mu/m SiGe:C-BiCMOS process," *IEEE InternationalElectron Devices Meeting, 2005. IEDM Technical Digest.*, Washington, DC, 2005, pp. 803-806.

[36]   "LM134/LM234/LM334 3-Terminal Adjustable Current Sources," Texas Instruments. [Online]. Available at: http://www.ti.com/lit/ds/symlink/lm334.pdf. [Accessed: 2018].

[37]   "Silicon-based silicon-germanium-tin heterostructure photonics" *Philosophical transactions. Series A, Mathematical, physical, and engineering sciences* vol. 372, 2012, January 13, 2013, pp. 1-12.

Curriculum Vitae

Dane Gentry

Contact Information:

Email: danegentry416@gmail.com

Education/Degree:

University of Nevada, Las Vegas

Bachelor of Science in Electrical and Computer Engineering w/ Mathematics Minor

December 2016

Employment:

University of Nevada, Las Vegas (UNLV)

2015 – Present

Thesis Title:

Design, Layout, and Testing of SiGe APDs Fabricated in a BiCMOS Process

Thesis Advisory Committee:

Chairperson, Dr. R. Jacob Baker, Ph. D.

Committee Member, Dr. Biswajit Das, Ph. D.

Committee Member, Dr. Yahia Baghzouz, Ph. D.

Graduate College Representative, Dr. Andrew Cornelius, Ph. D.