DESIGN OF A CMOS 6-BIT FOLDING AND INTERPOLATING ANALOG TO DIGITAL CONVERTER

A Thesis

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by

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AUTHORIZATION TO SUBMIT THESIS

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ABSTRACT

This thesis describes the design of a 6-bit CMOS folding and interpolating Analog to Digital Converter (ADC). Folding and interpolating techniques can be used in CMOS flash type ADCs so that less die area and power dissipation are used, while at the same time maintaining high-speed operation. The fundamentals of the CMOS folding and interpolating circuits are covered, and some of the major design issues are reviewed and discussed. Simulation and experimental results from a 6-bit ADC test chip fabricated in a 1.2um process are also presented.

ACKNOWLEDGMENTS

I would like to thank the members of my committee: R. Jacob Baker, Harry W. Li and Peter Goodwin. I would like to thank Dr. Baker for giving me the opportunity to develop, design, layout and fabricate a CMOS folding and interpolating analog to digital converter and for his insightful guidance throughout this project. I would like to thank Dr. Li for his teaching and help on analog circuit design, which aroused my great interest in this field. Finally and especially, I would like to thank my wife, Rong, for her sacrifice and unselfish support for me throughout my MS study.

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CHAPTER 1

FUNDAMENTALS OF THE FOLDING A/D CONVERTER

1.1 The Folding Architecture for A/D Conversion

High-speed A/D converters (Analog to Digital converters, or ADCs) have found many applications in communication circuits and network interfaces. The fastest architectures for A/D conversion are the full flash ADC in which the whole A/D conversion finishes in one single step, and the pipeline ADC which, after an initial delay of N clock cycles, conversion is accomplished in one clock cycle. The full flash ADC, however, suffers from large die area when the resolution is greater than 6 bits. The number of the comparators needed in full flash ADC explodes exponentially with the resolution. The two-step or multiple-step ADCs require much fewer comparators than flash ADC but need two or several steps to finish conversion and are therefore slow. Although the pipeline technique can be used to improve the throughput in multiple-step ADCs, they still pose a high initial latency as well as overhead of the T/H (Track and Hold) circuitry needed between the stages, which makes their implementation more challenging.

A number of circuit architectures have been developed to alleviate the area problem while maintaining the one-step conversion. Among them is the folding ADC [1]. Figure 1.1.1 shows the basic block diagram of a 6-bit folding A/D converter.

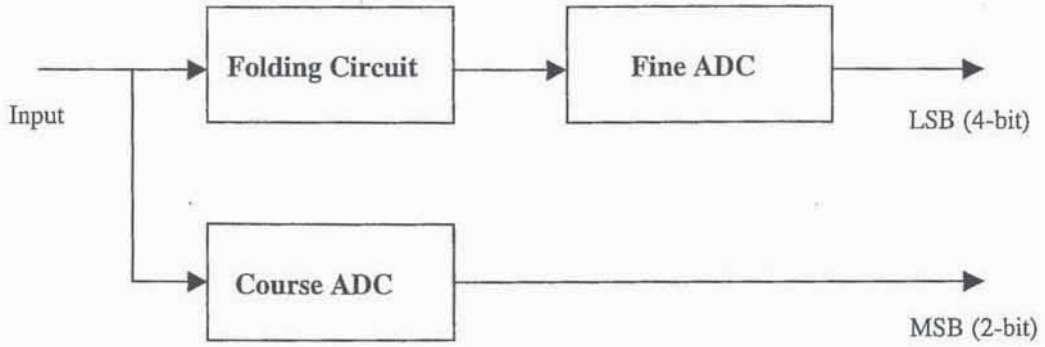

Figure 1.1.1 Block diagram of a 6-bit folding ADC

The operation of the folding ADC can be illustrated by the transfer curve of the folding circuit shown in Figure 1.1.2. Here the input analog signal is "folded" into 4 folds (4- times folding). The output of the folding circuit (folding signal) therefore needs to be converted to only 16 levels corresponding to the four least significant bits (LSB's). In order to distinguish between the four possible inputs that correspond to the same folded signal output, a 2-bit coarse ADC is needed, which generates the two most significant bits (MSB's).

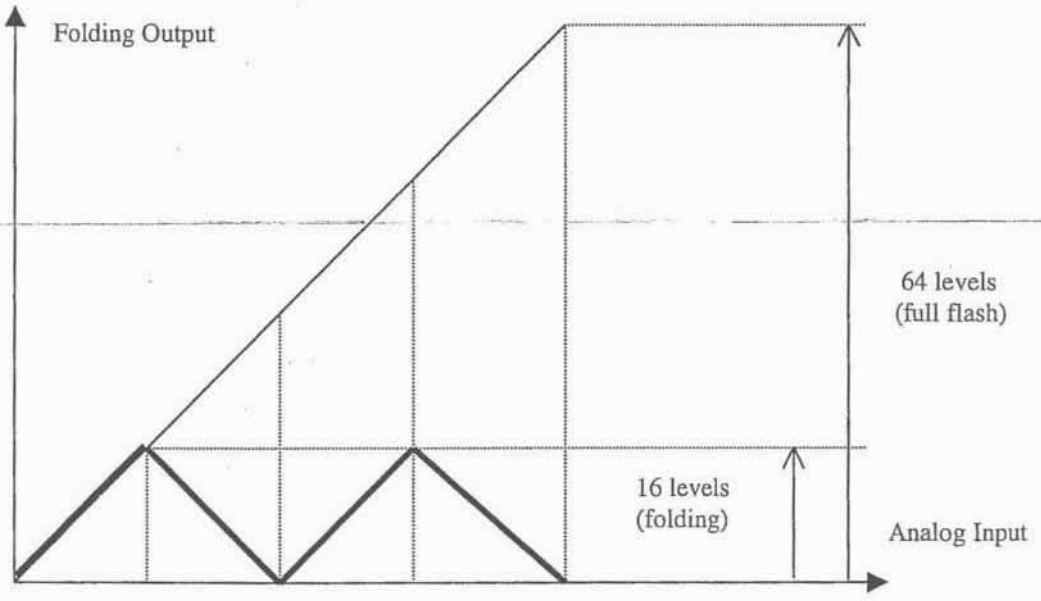

Figure 1.1.2 Transfer curve of the folding circuit

The number of the comparators needed for the 6-bit folding ADC shown above is 16 + 4 = 20, which is much less than 64 required for a full flash. As the resolution of the ADC increases, further savings in area can be expected. For example, an 8-bit folding ADC divided in to a 5-bit fine and a 3-bit coarse ADC, requires only 40 comparators in comparison to the 255 needed for a full flash ADC. The significant decrease in the number of comparators also means much less power dissipation.

Besides the savings in the die area and power dissipation, there are some other important benefits of the folding ADC:

1) One step operation guarantees high speed conversion

Unlike the two-step or multi-step ADC, which do the post-signal processing on the input signal (subtracting the residue), the folding ADC uses pre-signal processing (i.e. folding) to achieve one-step conversion. The throughput of the folding ADC is equal to that of a full flash, while the two-step or multi-step converters require several clock cycles to convert the data.

2) No front-end T/H circuitry needed

The parallel or one step conversion also eliminates the overhead of the T/H circuitry. On the other hand, the two-step or multi-step ADCs require T/H circuitry to store the data value for used in different conversion steps.

1.2 The Goal of the Thesis

The folding and interpolating ADC first appeared in bipolar circuits. The advantage of the CMOS technology over bipolar is that the CMOS ADC can be integrated on the same die as digital signal processing core, resulting in compact and efficient integrated systems.

The purpose of the thesis is to investigate the performance of the folding and interpolating technique in fast CMOS A/D conversion. A 6-bit CMOS folding and interpolating ADC has been fabricated in AMI 1.2 um process. The thesis will describe some of the design issues as well as the simulation and experimental results from the test chip.

CHAPTER 2

CMOS FOLDING AND INTERPOLATING CIRCUIT

2.1 CMOS Folding Circuit

Figure 2.1.1 shows the basic scheme for the CMOS folding circuit (a 4-times folder) for use in a 6-bit ADC. The folder consists of four differential pairs with outputs of the odd- and even- number diff-pairs cross-coupled. One of the inputs of the diff-pair is connected to the input voltage and the other one is connected to the reference voltage. The outputs of the folder are differential too.

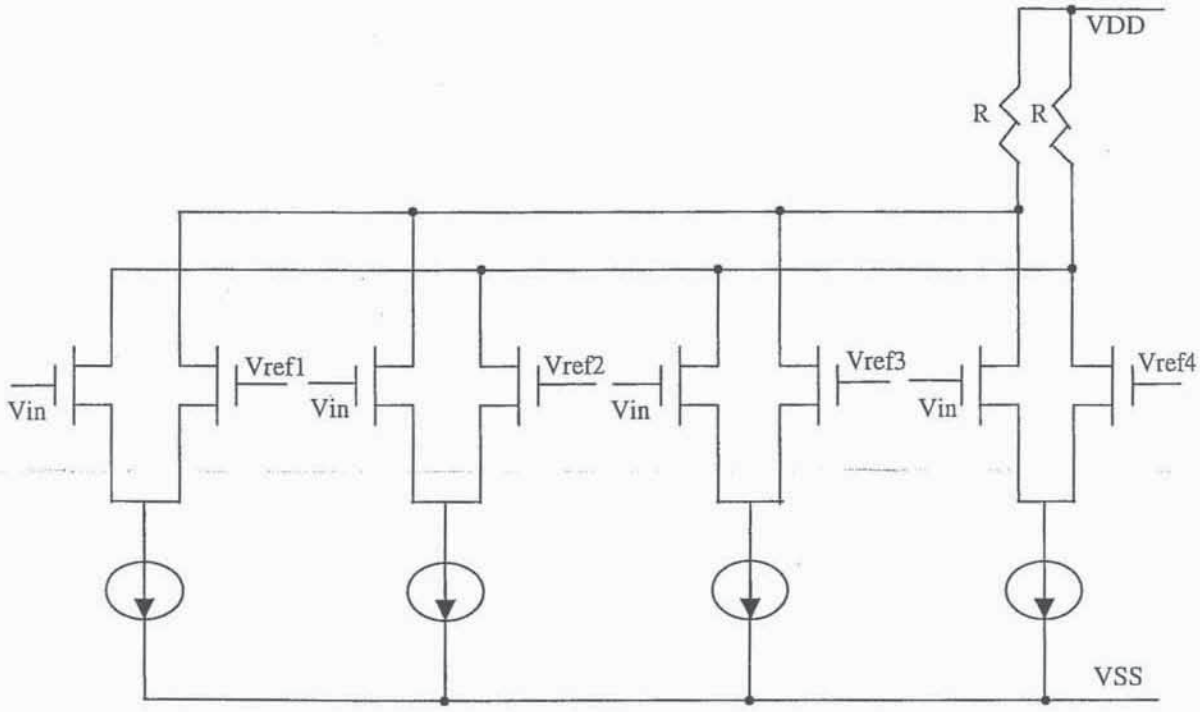

Figure 2.1.1 CMOS folder

Figure 2.1.2 shows the DC transfer curve of the folder. Compared to the ideal folder transfer curve shown in Figure 1.1.2, we can see that the top and bottom of the curve are "flat", in other words, highly non-linear. Although this non-linearity can be decreased by using larger MOSFETs, it can not be eliminated. As a result, in practical applications we can not do the signal folding solely based on one such folder. One solution is to use two folders to generate two "shifted" folding signals.

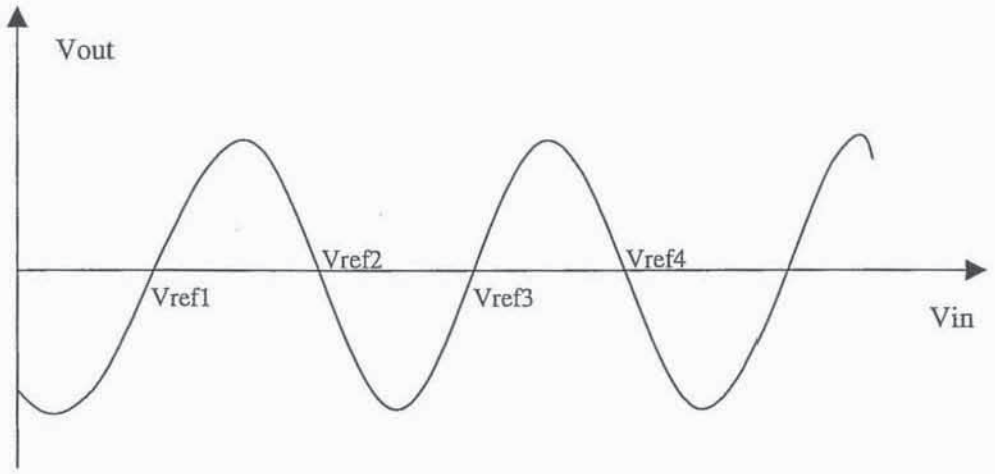

Figure 2.1.2 DC transfer curve of the CMOS folder

Figure 2.1.3 shows the situation when two folding signals with different offset are used. If the offset is properly designed, there is always one folding signal in its linear region for the whole input range. Now each folding signal needs to detect only 8 levels, instead of 16 levels. We can further increase the number of folding signals with each folding signal requiring detection of less number of levels. For example, if we use 4 folders then each folding signal needs detection of only 4 levels. This will ease the linearity requirement of the

folder circuit. The question is: how many folding signals are needed to guarantee the linear operation of the folding circuit?

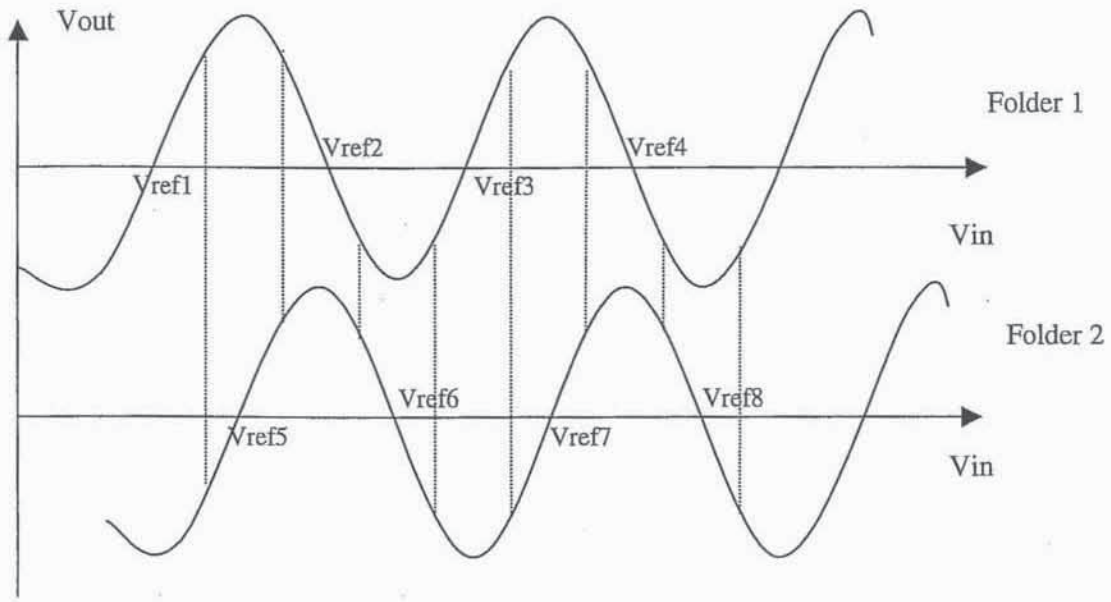

Figure 2.1.3 Using two folders to generate two "shifted" folding signals

The answer to this question is dependent on the fact that any practical CMOS circuit design should be maximally independent of the process, temperature and power supply. An important observation here is that as long as each folding signal uses multiple-level detection (more than one), it will be susceptible to process, power supply and temperature variations.

Figure 2.1.4 shows the case that more than one level (Level_0 and Level_1) of detection is needed for each of the folding signals. With the process, power supply and temperature variations, the absolute value of Level_1 deviates from its ideal value which is designed to be the switching point of the following comparators and thus causes error.

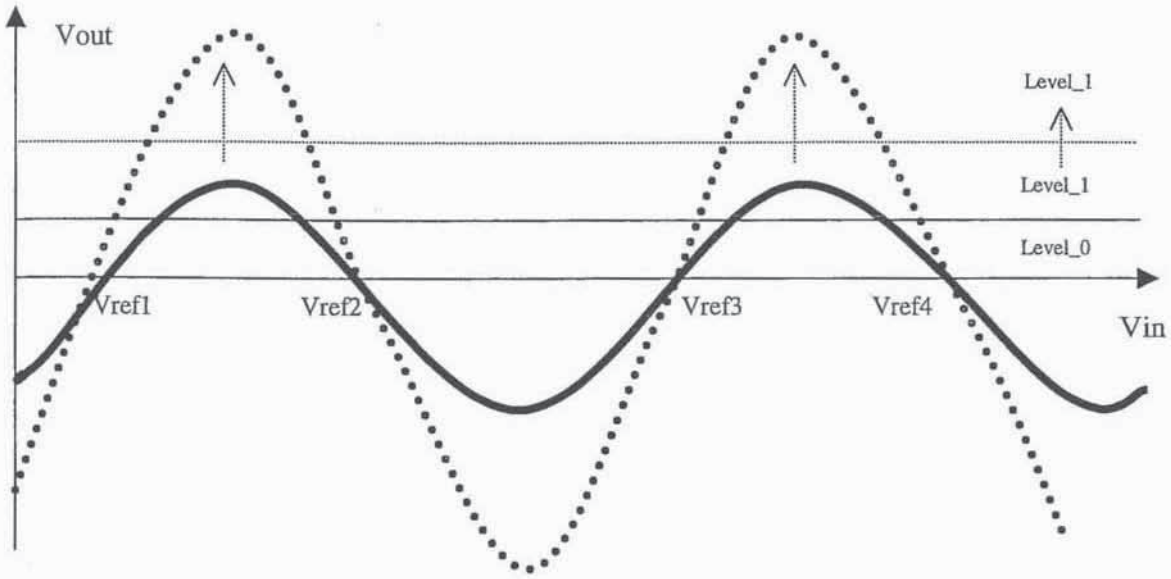

Figure 2.1.4 Multiple levels of detection

An important observation that should be made after reviewing Figure 2.1.4 is that the zero-crossing points of the folder output are defined by the reference voltages and are highly independent of the process and temperature variations due to the differential structure (recall the outputs of the folder are differential). The implication is, therefore, for practical use, we should extend the number of folding signals such that each folding signal needs the detection of only one level, i.e., the zero-crossing point of that signal. For the 6-bit ADC with four times folding circuits, the number of folders needed is 16.

The problem now is that generating 16 shifted folding signals with 16 X 4 diff-pairs is as much hardware as (if not more than) the full flash ADC. Interpolation can be used to solve this problem.

2.2 Interpolating

The basic principle of interpolation is shown in Figure 2.2.1 and 2.2.2. Folder A and B generate two shifted folding signals, VA and VB. Another folding signal that lies between VA and VB can be generated using the resistor chain (averaging). This being the case, for the 6-bit folding ADC, we only need 8 folders and can use the interpolating circuit to generate the other 8 folding signals. Note that the top and bottom of the interpolated signals are somewhat nonideal. This is not important, however, since only the zero-crossing points are actually used.

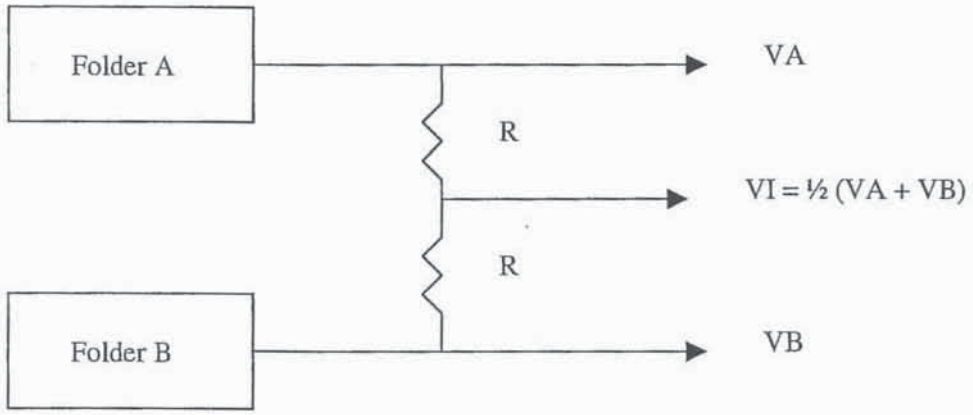

Figure 2.2.1 Block diagram of the interpolating circuit

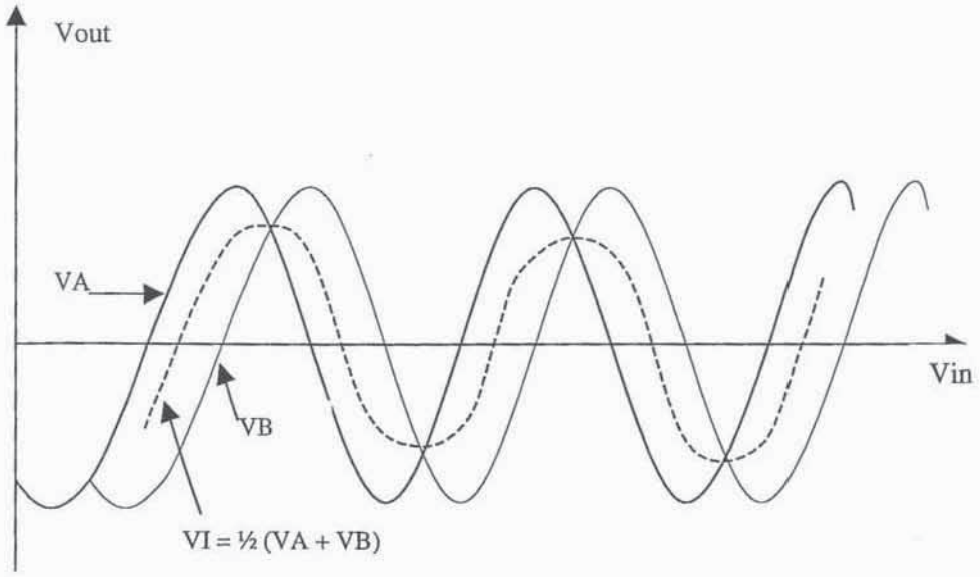

Figure 2.2.2 Transfer curve of the interpolating signal

Figure 2.2.3 shows the complete block diagram of the 6-bit CMOS folding and interpolating ADC. Note that by using 8 folders (instead of 1 folder in the basic scheme shown in Figure 1.1.1) and a total of 16 folding signals, we can get 5 LSB's from the folding and interpolating outputs (instead of 4 LSB's in the basic scheme), and therefore, the coarse ADC now only needs to be 1 –bit (MSB).

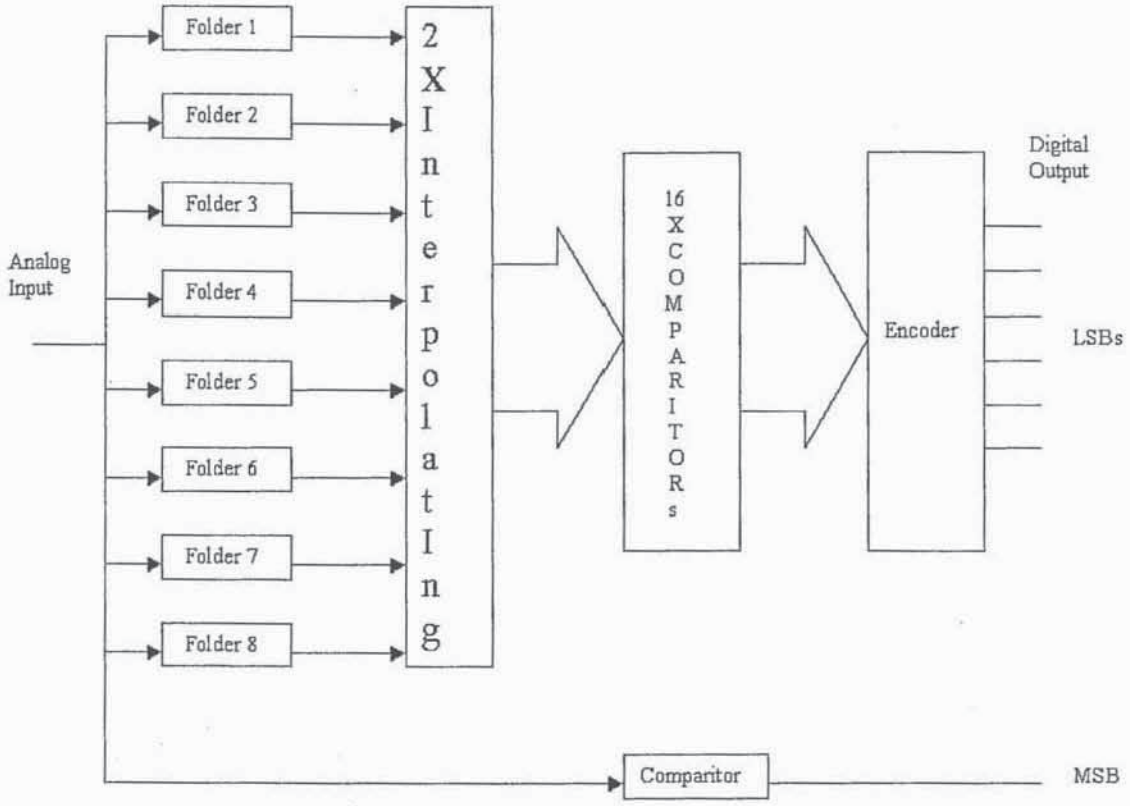

Figure 2.2.3 Block diagram of the 6-bit folding and interpolating ADC

2.3 Design Considerations

There are some considerations that deserve mention when designing the folding and interpolating circuits for used in ADCs. First, the size of the MOSFETs in the diff-pairs of the folding circuit should be large enough to ensure good linearity of the transfer curve and thus the linearity of the ADC. Larger devices also help to improve the matching and thus decrease the offset voltage that contributes to the Integral Non-Linearity (INL) and Differential Non-Linearity (DNL).

On the other hand, however, large devices pose large parasitic capacitance and lower the bandwidth (speed) of the folding circuit. The size of the MOSFETs used in the diff-pairs, therefore, is limited by the speed and area requirements of the ADC. A 40/1 ratio is used in this design.

There are also some tradeoffs when selecting the value of the load resistor R in the folding circuit. Basically, R should be large enough to maintain an adequate gain of the folders. The bandwidth of the folders, however, is inversely proportional to the resistor value. A resistor value of 5 K is adopted in this design. Some techniques were developed to deal with the bandwidth and gain tradeoffs, such as using trans-resistance amplifier or current steering methods [2] [3] [6].

An important issue in folding and interpolating ADCs is the timing error between the coarse stage and the folding and interpolating circuit. Since the delays of the two circuits are different, the coarse stage may point to the wrong cycle in the folding characteristics [1]. One way to correct this problem is to insert some delay elements in the clock circuits of the coarse ADC.

As a conclusion to this chapter, Figures 2.3.1 and 2.3.2 show the simulated DC transfer curves of the folding and interpolating circuit used in this design. Figure 2.3.3 shows the block diagram of the circuit simulated.

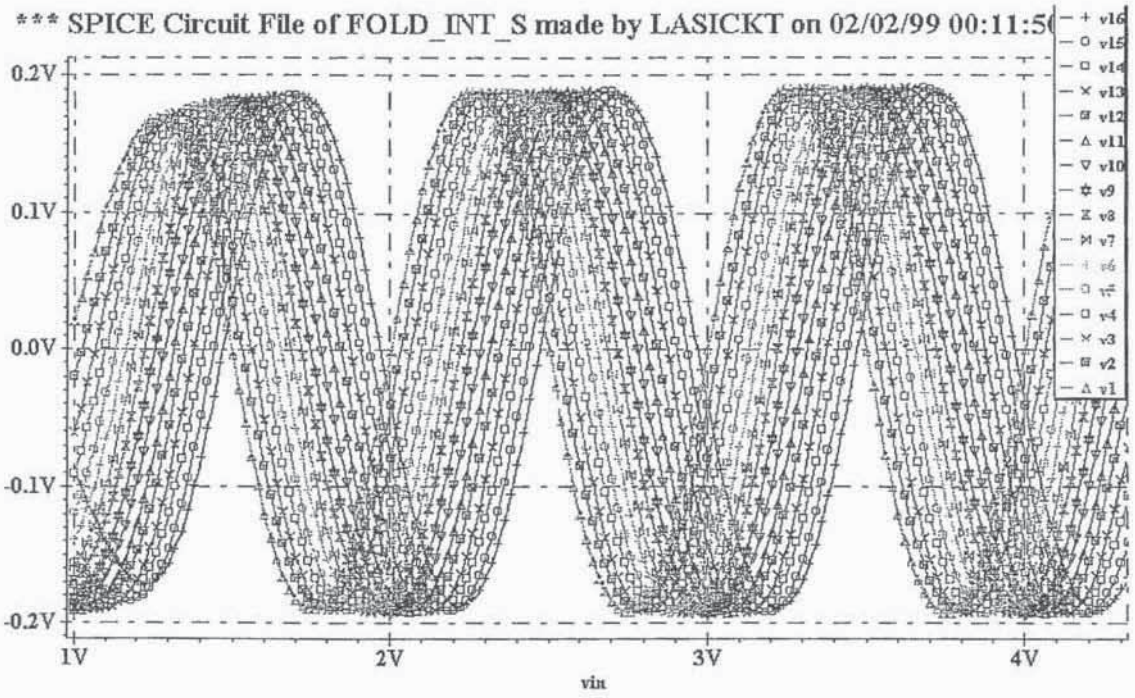

Figure 2.3.1 Simulated DC transfer curves of the folding and interpolating circuit

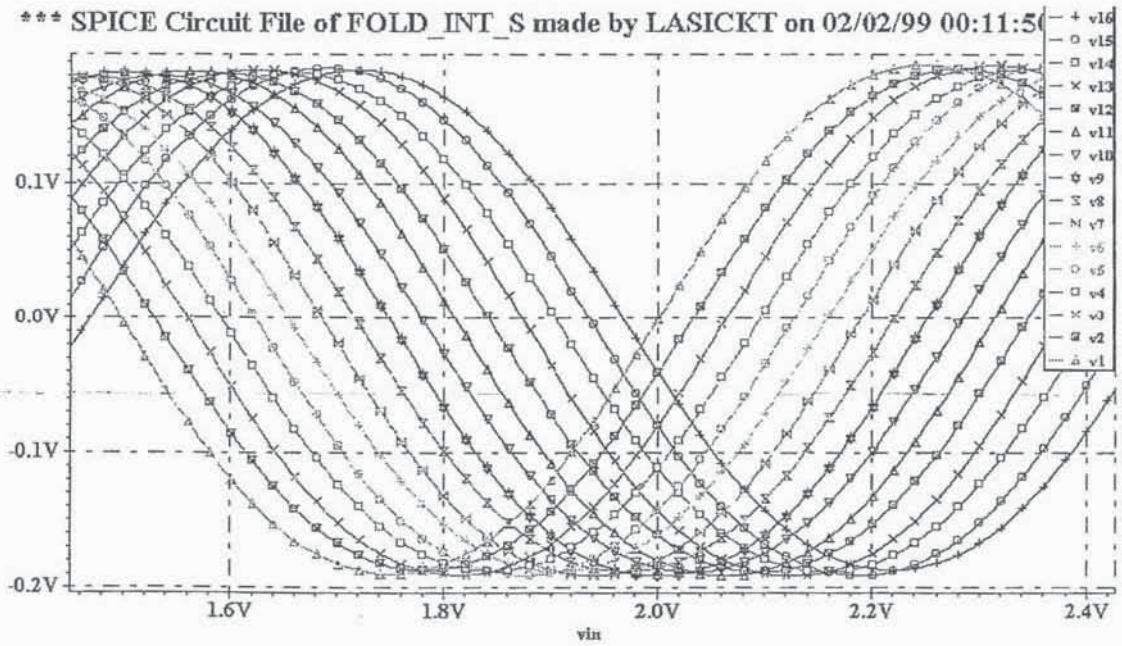

Figure 2.3.2 A closer look of the simulated DC transfer curves

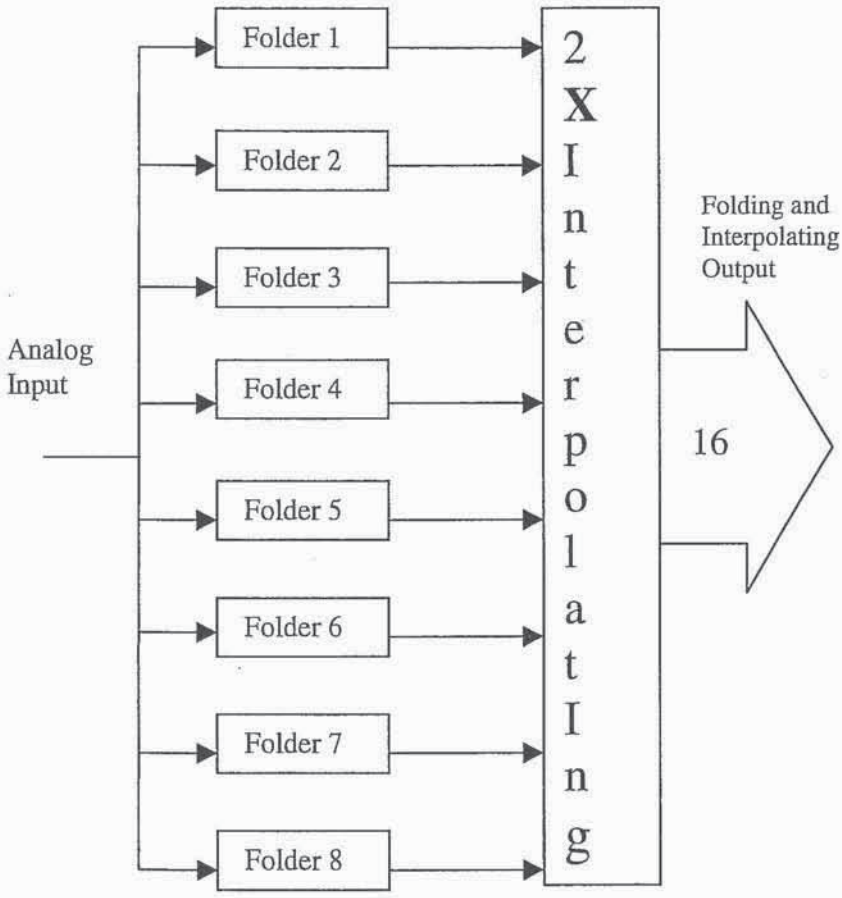

Fig 2.3.3 Block diagram of the circuit simulated

CHAPTER 3

CLOCKED COMPARATORS

3.1 Operation

The comparator is the heart of A/D converters that don't use a T/H. In particular, the performance of the flash and folding A/D converters which employee parallelism to achieve a high speed strongly depend on that of their constitute comparators. As mentioned in Chapter 1, folding ADCs do not need front-end T/H circuits. The tracking and holding are executed by the clocked comparators.

Figure 3.1.1 shows the schematic of the clocked comparator [3] used in the design. The comparator consists of three stages: pre-amplifier (M1 – M4), decision circuit (M5 – M10, ML1 and ML2) and output buffer (not shown in Figure 3.1.1). The pre-amplifier is a fully differential amplifier that provides adequate gain to ensure that the desired sensitivity is achieved. The pre-amp also isolates the input of the comparator from the switching noise coming from the decision circuit.

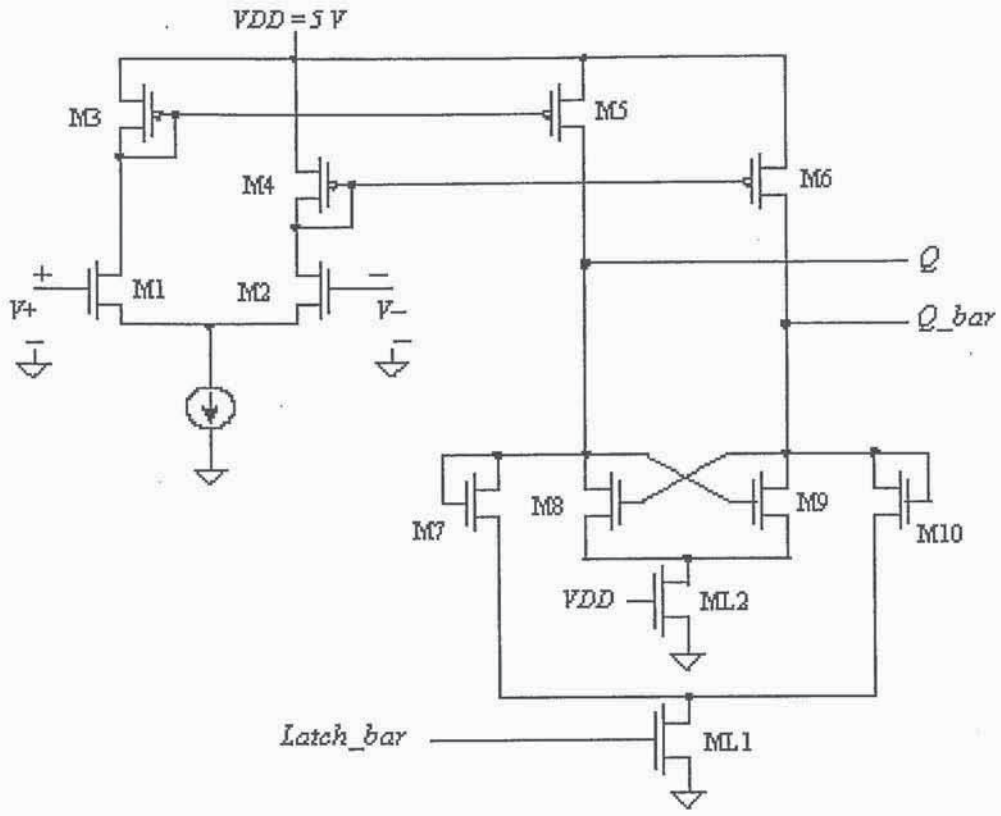

Figure 3.1.1 Scheme of the clocked comparator

The decision circuit is capable of discriminating mV level signals. The core of the decision circuit employees positive feedback and also could provide some hysteresis (for use in noise rejection). The hysteresis is decided by the ratio of size of M7 and M8. When Latch_bar is high, the output of the decision circuit depends on the input signal and the comparator is in a mode similar to that of tracking. When Latch_bar is low, ML1 shuts off and latches the output as logic high or low. Now the comparator is in its holding mode.

The output buffer provides additional gain for the comparator as well as isolates the load capacitance from the decision circuit.

3.2 Design Considerations

The performances of the comparators are vital for proper operation of the A/D converter. In particular, the offset voltage of the comparator contributes to the offset voltage of the ADC, as well as INL and DNL. For the 6-bit ADC, the maximum INL and DNL should not exceed ½ LSB that is 15.6mV in this design (More on this issue in Chapter 4). The offset voltage of the comparator is due to the mismatch of the MOSFETs (sizes, threshold voltages and etc.). Generally, we want to use large input devices (M1 and M2) for the input diff-pair to improve the matching. This will also improve the gain of the comparator.

The speed of the comparator is another concern. Increasing the current through M5 and M6 can improve the speed of the decision circuit. This can be achieved by increasing the size of the M5 and M6. They should not be too large, however, because large devices also have large parasitic capacitances and the slew rate on the output nodes may become a concern.

Figure 3.2.1 shows the simulated transient response of the clocked comparator used in this ADC design. Figure 3.2.2 shows the block diagram of the circuit simulated. The comparator has a delay time of about 2ns.

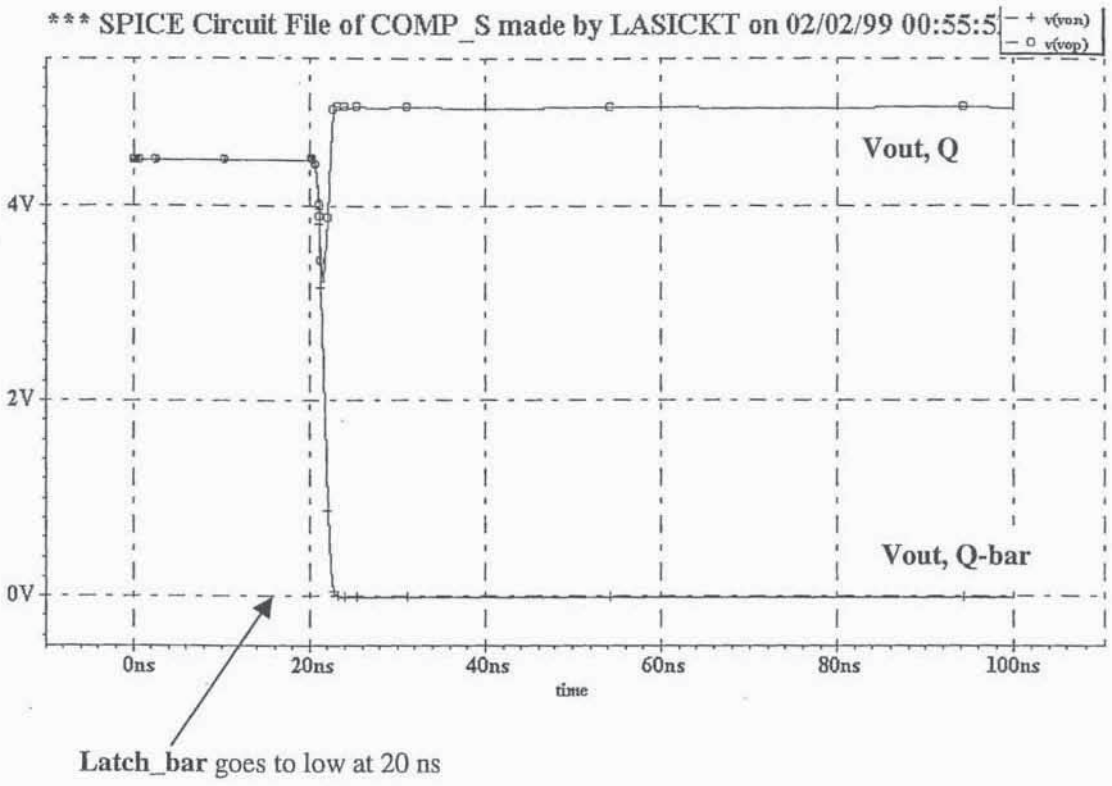

Figure 3.2.1 Transient response of the outputs of the clocked comparator

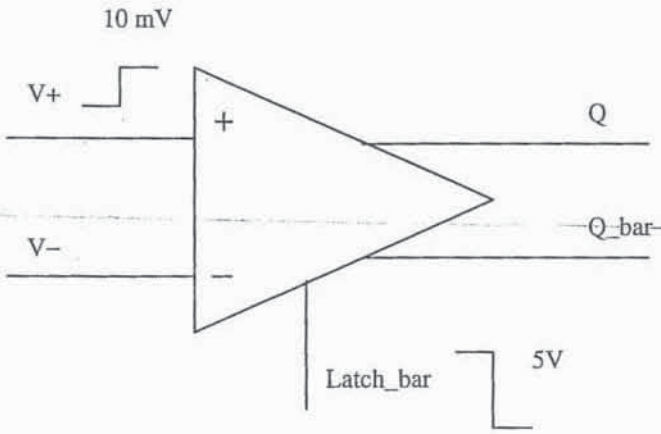

Figure 3.2.2 Block diagram of the circuit simulated

CHAPTER 4

SPECIFICATIONS FOR THE A/D CONVERTER

4.1 Accuracy

There are several specifications describing the accuracy (DC behavior) of the ADC: INL, DNL, offset voltage and gain error. In this section we will concentrate on the INL and DNL.

Generally, the INL and DNL of an A/D converter should be less than ½ LSB. The input range of the 6-bit ADC in this design is 2V (1.5 V – 3.5V) and therefore ½ LSB means $2V/2^{6+1}$, or 16.5 mV. The combined non-linearity and offset voltage of the different components of the ADC, therefore, should be less than 16.5 mV.

It is known that the INL and DNL of the flash type ADC mainly depend on the matching of the resistor string and the offset voltage of the comparators [4]. The INL exerts more stringent requirement on the resistor matching and is therefore the limiting factor. For a full flash ADC the maximum INL due to resistor mismatch can be estimated by the following equation [4]:

$$\left|INL\right|_{max} = \frac{Vref}{2}\left|\frac{\Delta R}{R}\right|_{max} + \left|Vos,\ c\right|_{max} \qquad (4.1.1)$$

where Vref is the value of the reference voltage, ΔR is the variation in the resistor value from its ideal value (R), and Vos, c is the offset voltage of the comparator.

In the folding ADCs, however, the estimation of the worst case INL is more involved. Now there are two resistor strings: one is used to generate the reference voltages for the folding circuit, and the other one is used for the interpolation. For the 6-bit folding and interpolating ADC, each resistor string generates 32 divisions along the input range. Figure 4.1.1 shows the reference points generated by the two resistor strings along the input range.

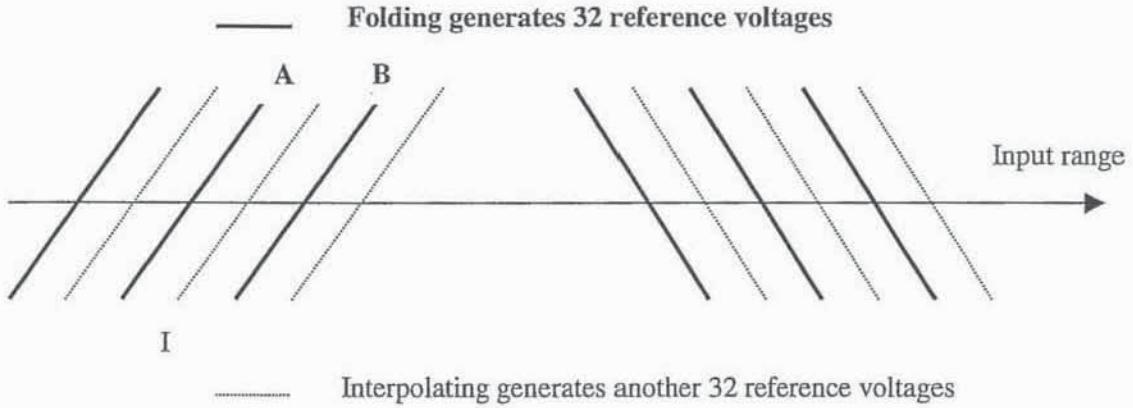

Figure 4.1.1 The reference voltages generated by the two resistor strings.

From Figure 4.1.1 we can see that in terms of the error analysis, the outputs of the folding and interpolating circuit fall into two groups: the direct outputs of the folding circuit (point A and B in Figure 4.1.1) and the outputs of the interpolating circuit (point I in Figure 4.1.1). The worst case INL of the direct folding outputs due to mis-match of the resistors is the same as that for a full flash and given by equation 4.1.1.

The INL of the interpolating outputs consists of two parts: the non-linearity forwarded from the folding signals (i.e., the error of point I due to the error of point A and B in Figure 4.1.1) and the non-linearity due to the mismatch of the interpolating resistors (i.e., the error of I caused by the mis-match of the two resistors in the interpolating resistor string).

In the worst case, the INL of the folding signals (point A and B in Figure 4.1.1) will feed 100% of the nonlinearity to the interpolating signals (point I of the Figure 4.1.1), which value is given by equation 4.1.1. The INL caused by the mis-match of the interpolating resistors, on the other hand, is negligible and approximately equals $\frac{\text{Vref}}{2^6}\left|\frac{\Delta R}{R}\right|$. Therefore, for the estimation purpose, we can still use the equation 4.1.1 to calculate the worst case INL due to the mismatch of the two resistor strings in the folding and interpolating ADCs.

In regard to the INL due to the offset voltage, the offset voltage of the folding diff-pairs and comparators adds. The total worst case INL of the folding and interpolating ADC, therefore, is given by:

$$|\text{INL}|\max = \frac{\text{Vref}}{2}\left|\frac{\Delta \text{R}}{\text{R}}\right|\max + |\text{Vos, c}|\max + |\text{Vos, f}|\max \qquad (4.1.2)$$

where Vref is the value of the reference voltage, ΔR is the variation of the resistor value from their ideal value, and Vos, c and Vos, f is the offset voltage of the comparator and folder, respectively.

The total INL should be less than 16.5 mV for the 6-bit ADC with 2V input range. Simulation results showed that the systematic offset voltage of the folding circuit is about 1 mV. The mis-match of the n+ resistors used for the both resistor strings is about 0.25%. Thus the offset voltage requirement for the comparators is about 13 mV for the 6-bit accuracy.

4.2 Speed

The speed of three major parts of the folding and interpolating ADC, i.e., the folding and interpolating circuit, comparators and encoding logic, is of concerns in this section.

The speed (bandwidth) of the folding and interpolating circuit is mainly limited by its high impedance output nodes. As a result, there is a time difference between the signal held when clock goes high and the analog input signal. This time difference introduces an error into the ADC as well as limits the highest frequency of the input signal. As mentioned in chapter 2, there is a tradeoff between the gain and the bandwidth of the folding and interpolating circuit. For high-speed ADC, other technique, such as trans-resistance amplification and current steering, can be used to deal with the problem.

The simulated transition time of the folding and interpolating circuits of this design is about 20nS. This limits the highest input frequency to about 25 MHz.

The clock frequency of any one-step ADC is mainly limited by the propagation delay of the comparator and encoding logic. Figure 4.2.1 shows the timing diagram of the one-step ADC. The simulated transition (rise and fall) time of the comparator and encoding logic (with output buffer) is about 2ns and 23ns. The highest clock frequency for the ADC designed in this thesis is then about 40 MHz (ignore the setup time of the subsequent registers).

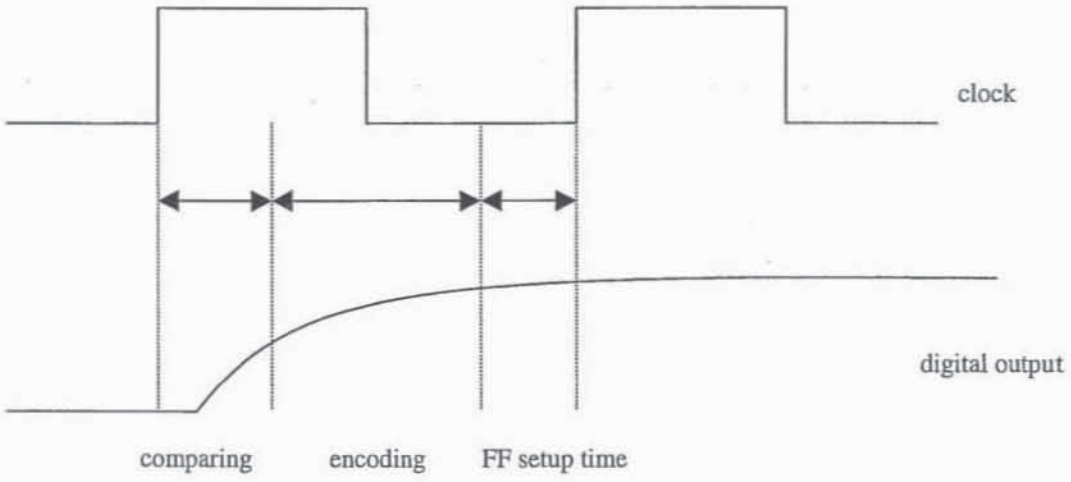

Figure 4.2.1 Timing diagram of the one –step ADC

CHAPTER 5

TEST CHIP AND SOME EXPERIMENTAL RESULTS

5.1 Test Chip

A 6-bit folding and interpolating ADC has been fabricated in the MOSIS AMI 1.2 um process with a concentration on testing the folding and interpolating circuit. Figure 5.1.1 shows the layout of the chip. Figure 5.1.2 shows the die photo.

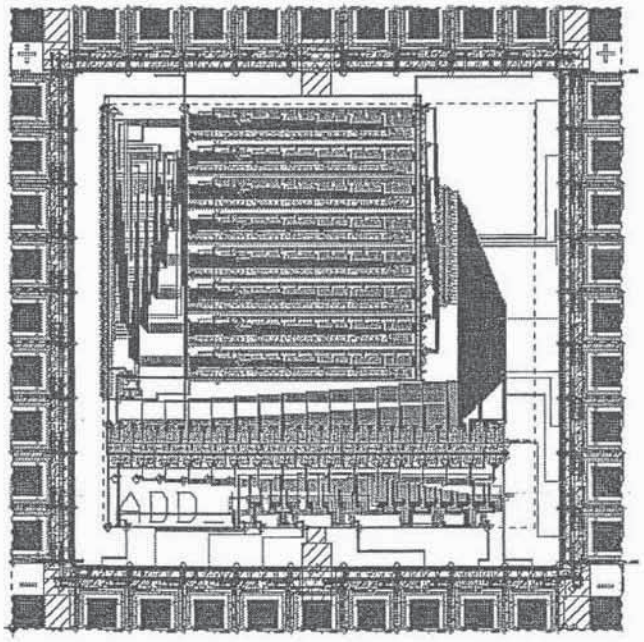

Figure 5.1.1 Chip layout

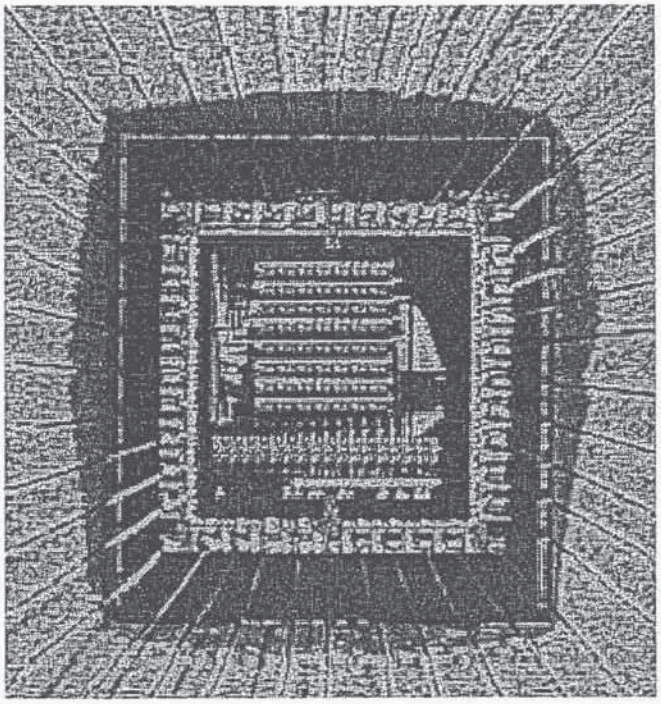

Figure 5.1.2 Die photo

5.2 Experimental Results from the Folding and Interpolating Circuit

Figure 5.2.1 shows the measured DC transfer curve of one of the output signals of the folding and interpolating circuit. The measured curve is very similar to that from the simulation run (as shown in Figures 2.3.1 and 2.3.2) except that the offset voltage is larger. The maximum measured offset voltage is about 5 mV (SPICE simulation gives 1 mV). Random offset voltage, which is not revealed by the simulation, is the main cause for the larger measured offset voltage. Since one LSB of the 6-bit ADC with 2V input range is about 31 mV, this offset voltage is on an acceptable level. In short, the function of the folding and interpolating circuit in this design is verified by the experimental results.

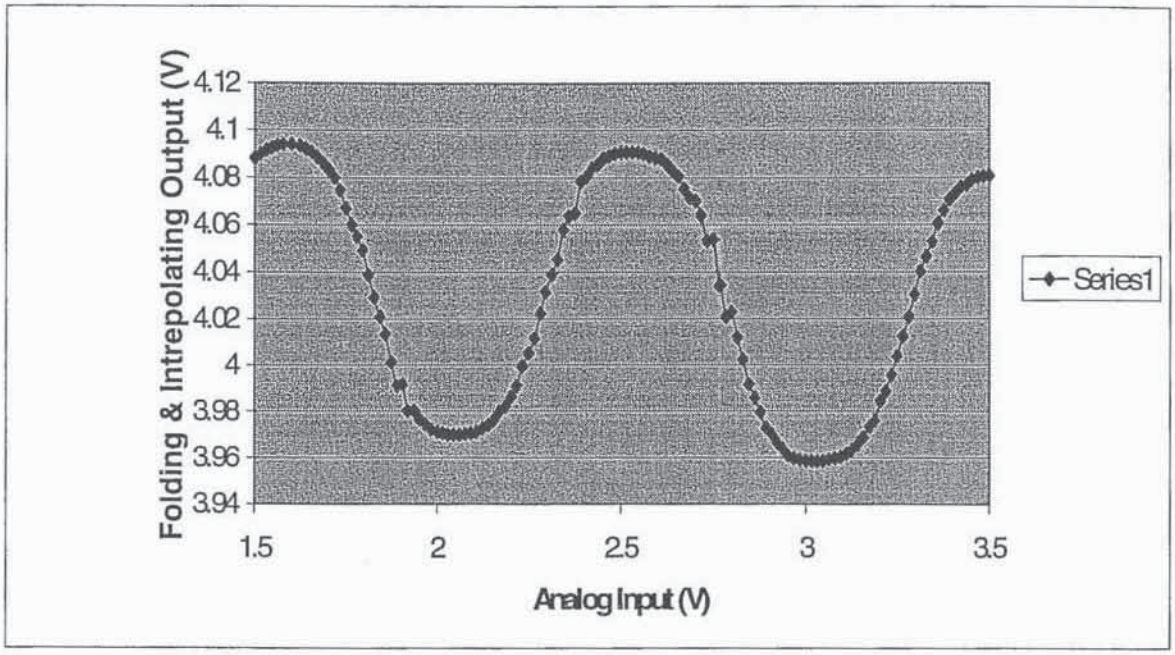

Figure 5.2.1 Measured DC transfer curve of the folding and interpolating circuit

The measured power dissipation of the test chip is 95 mW. The total effective area of the converter is about 1.5 mm^2.

SUMMARY

The folding and interpolating technique can be used in the CMOS flash type A/D converters that result in less die area and power dissipation. The one–step operation of folding and interpolating ADC provides a mechanism for high-speed conversion. The bandwidth of the folding and interpolating circuits, however, could become one of the limiting factors of this architecture in high-speed applications. The accuracy issues are basically the same as that of the full flash architecture, provided now we also have to take the offset voltage of the folding circuits into account.

A 6–bit CMOS folding and interpolating ADC was designed with a small area (1.5 mm^2 in 1.2 um technology) and power dissipation (95 mW at 5 V supply). The DC operation of the ADC was verified with the HSPICE and the function of the folding and interpolating circuit was verified by the experimental results. Further improvements can be expected by more elaborate design and layout of each of the ADC components.

REFERENCES

[1] Behzad Razavi, *Data Conversion System Design*, IEEE Press, 1995.

[2] Bram Nauta and Ardie G. W. Venes, "A 70-MS/s 110-mW 8-b CMOS Folding and Interpolating A/D Converter", in *IEEE Journal of Solid-State Circuits*, Vol. 30, No. 12, December 1995.

[3] Michael P. Flynn and Ben Sheahan, "A 400-Msample/s, 6-bit CMOS Folding and Interpolating ADC", in *IEEE Journal of Solid-State Circuits*, Vol. 33, No.12, December 1998.

[4] R. Jacob Baker, Harry W. Li and David Boyce, *CMOS Circuit Design, Layout and Simulation*, IEEE Press, 1998

[5] Pieter Vorenkamp and Raf Roovers, "A 12-b, 60-Msample/s Cascaded Folding and Interpolating ADC", in *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 12, December 1997.

[6] Michael P. Flynn and David J. Allstot, "CMOS Folding A/D Converters with Current-Mode Interpolation", in *IEEE Journal of Solid-State Circuits*, Vol. 31, No.9, September 1996.

[7] Xicheng Jiang, Yunti Wang and Alan N. Willson Jr., "A 200 MHz 6-Bit Folding and Interpolating ADC in 0.5-um CMOS", ISCAS, 1998.